THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

The control of VSC-HVDC and its use for large industrial power systems

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Abstract

With the recent developments in semiconductors and control equipment, Voltage Source Converter based High Voltage Direct Current (VSC-HVDC) has become feasible. Due to the use of VSC technology and Pulse Width Modulation (PWM), it has a number of potential advantages: short circuit current reduction; rapid, independent control of the active and reactive power, etc. With such very favorable advantages VSC-HVDC will likely be part of future transmission and distribution systems which supply industrial systems with a high load density, high reliability and quality requirements, and high costs associated with production stoppages.

The thesis deals with the control of VSC-HVDC, the use of VSC-HVDC in a passive industrial system and the system design with different dc voltage levels. The objective of the work is to assess the potential and limitation of the use of dc distribution in industrial power systems.

A model of a VSC based dc link using PWM Technology and IGBT semiconductors is designed. A mathematical model of the control system based on the relationships between voltage and current is described for the VSC connected to the transformer secondary side. A control system is developed combining an inner current loop controller which is divided into positive current controller and negative current controller and a number of outer controllers. Different control strategies are studied and corresponding dynamic performance under step changes and different types of faults is investigated in PSCAD/EMTDC simulation package. The simulation results verify that the model can fulfill bi-directional power transfers, ac system voltage adjustment and fast response control and that the system has good transient and steady state performance.

VSC-HVDC is investigated for its ability to supply a passive industrial system. In this thesis the comparison of a pure ac supplied distribution system and a dc supplied distribution system is performed based on balanced and unbalanced faults on the grid side and motor starting on the load side. The influence of the current limitation on the performance is studied. It is shown that VSC-HVDC applied to industrial systems is able to mitigate voltage dips. it is also shown that the rating of the dc link significantly influences its ability to mitigate voltage dips.

The possibilities of multi-level dc networks and a mixed ac/dc system are investigated. The control of the dc/dc converter is developed for this. Again the rating of the converters has a significant effect on the performance of the system during faults and motor starting.

A discussion is started on the relation between converter rating and industrial power-system design.

Keywords: VSC-HVDC, PWM, inner current controller, outer controller, dc/dc converter, voltage dips, dc networks

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Contents

Chapter 1

Introduction

1.1 Background

Industrial power systems are characterized by high concentration of load and high costs associated with equipment mal-operation. Many industrial loads cause disturbances in the system like equipment starting dips and transients, harmonic distortion and flicker. Industrial loads are also very sensitive to voltage dips and other disturbances originating from the grid. So electric power systems are faced with the challenge of providing high-quality power to industrial loads and at the same time limiting the disturbances originating in the industrial systems.

Power-electronics solutions have been suggested to solve specific power quality and other problems in industrial distribution systems. An uninterruptible power supply (UPS) can provide 'ride-through' capability against voltage interruptions and dips for small loads[1]. DVR can alleviate a range of dynamic power quality problems such as voltage dips and swells for large loads (up to a few MVA)[2]. STATCOM has the ability to either generate or absorb reactive power at a faster rate than classical solutions allowing for the mitigation of flicker and alleviation of stability problems[3]. Several options are explained in the literature[4][5][6].

HVDC traditionally has been used to transfer large amounts of power over long distances. Sometimes also for control purposes[7][8][9]. But for traditional HVDC the reactive power cannot be controlled independently of the active power. Recent development in power systems is voltage source converters (VSC) based HVDC which is referred to as VSC-HVDC in the thesis. There is an additional degree of freedom which make it possible to control the reactive power and the active power independently. Application of such dc links is expected to solve power-quality related problems in industrial power systems.

1.2 Contributions of the work

This thesis studies a control scheme for a VSC-HVDC link connecting two grids and isolated loads. Different control schemes are studied to investigate the behavior of VSC-HVDC during the disturbances.

This thesis presents a control scheme for a VSC-HVDC link connecting a grid and a passive industrial network.

This thesis investigates the advantages/disadvantages of using VSC-HVDC to supply large industrial installations. During this investigation current limitation is included and its effect on VSC-HVDC's ability to mitigate voltage dips is studied during faults and during motor starting.

This thesis investigates the possibilities of multi-level dc networks supplying industrial loads and the possibility of a mixed ac/dc system. A control scheme for a dc/dc converter is included. The influence of the rating of the converters on the performance of the system is studied.

This thesis starts a discussion on the relation between current limitation, rating of converters, and the design of industrial power systems.

1.3 Outline of the thesis

Chapter 2 presents classic HVDC and VSC-HVDC. In this chapter the arrangements of HVDC systems, the configurations, the advantages and the applications of classic HVDC systems and VSC-HVDC are described.

Chapter 3 emphasizes the design and operation of VSC-HVDC. The structure of VSC-HVDC, for instance, converter, harmonic filter, dc capacitor, is described in detail. The operation of VSC-HVDC is also explained.

Chapter 4 focuses on the control system of VSC-HVDC. The overall control structure of the VSC-HVDC is studied. A mathematical model of the control system is described in detail. Different outer controllers are also included.

Chapter 5 discusses some simulations about VSC-HVDC between two grids and to isolated loads. In this chapter two different control strategies are used, the step changes, the balanced fault and the unbalanced faults are simulated to evaluate the proposed control system of VSC-HVDC.

Chapter 6 discusses the comparison of an ac supplied system and a dc supplied system. The balanced fault, the unbalanced faults on the grid side, and starting of motor on the load bus are investigated.

Chapter 7 demonstrates some possible applications about dc networks. The dc/dc converter is used, two different dc medium-voltage systems and a mixed ac/dc system are studied.

Finally, the conclusions of the work and some suggestions for the future are pointed out in chapter 8.

Chapter 2

Classic HVDC and VSC-HVDC

2.1 Introduction

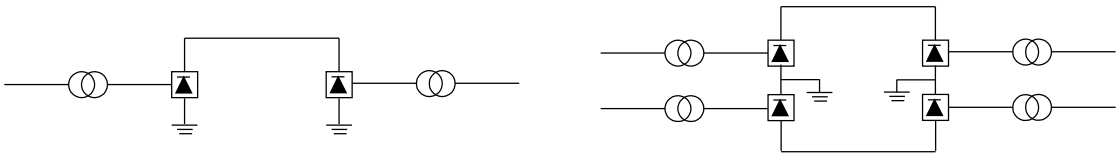
The HVDC technology is a high power electronics technology used in electric power systems. It is an efficient and flexible method to transmit large amounts of electrical power over long distances by overhead transmission lines or underground/submarine cables. It is also used to interconnect separate power systems, where traditional alternating current (ac) connections can not be used. HVDC is used at many places all around the world. Until recently HVDC based on thyristors, which is called traditional HVDC or classic HVDC, was used for conversion from ac to dc and vice versa.

Recently a new type of HVDC has become available. It makes use of more advanced semiconductor technology instead of thyristors for power conversion between ac and dc. The semiconductors used are IGBTs (Insulated Gate Bipolar Transistors), the converters are VSCs (Voltage Source Converters) and they operate with high switching frequency (1-2kHz) utilizing PWM (Pulse Width Modulation). The technology is commercially available as HVDC light [10] or HVDC plus [11]. In this thesis we will refer to the new technology as VSC-HVDC (VSC based HVDC), where VSC stands for voltage source converter. VSC-HVDC is currently available for small to medium scale power transmission applications [12][13][14]. The technology is claimed to extend the economic power range of dc transmission down to just a few megawatts. One of the reasons for this is the development of a newly type of cable for dc power transmission. In this chapter a brief overview will be given of classic HVDC and its applications. Next the differences between VSC-HVDC and classic HVDC will be discussed followed by possible applications of VSC-HVDC.

2.2 Arrangements of HVDC systems

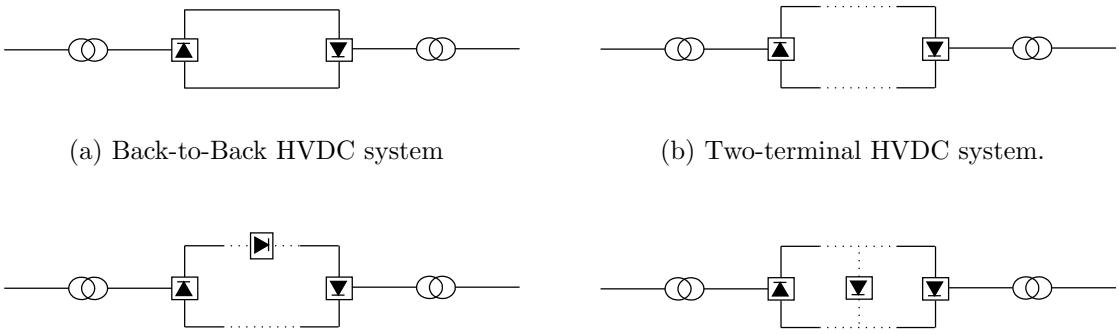
HVDC converter bridges and lines or cables can be arranged into a number of configurations for effective utilization. Converter bridges may be arranged either monopolar or bipolar as shown in Figure 2.1 and are described as follow:

1. Monopolar HVDC system.
   In monopolar links, two converters are used which are separated by a single



(a) Monopolar HVDC with earth return. (b) Bipolar HVDC

Figure 2.1: Monopolar and bipolar connection of HVDC converter bridges.



(a) Back-to-Back HVDC system (b) Two-terminal HVDC system.

(c) Series multi-terminal HVDC system (d) Parallel multi-terminal HVDC system

Figure 2.2: Some arrangements of HVDC systems.

pole line and a positive or a negative dc voltage is used. In Figure 2.1(a), there is only one insulated transmission conductor installed and the ground is used for the return current. For instance, the Konti-Skan(1965) project and Sardinia-Italy(mainland)(1967) project use monopolar links[7]. Instead of using the ground as a return path, a metallic return conductor may be used.

2. Bipolar HVDC system.
   This is the most commonly used configuration of HVDC power transmission systems[7]. The bipolar circuit link, shown in Figure 2.1(b), has two insulated conductors used as plus and minus poles. The two poles can be used independently if both neutrals are grounded. It increases power transfer capacity. Under normal operation, the currents flowing in each pole are equal, and there is no ground current. In case of failure of one pole power transmission can continue on the other pole, so its reliability is high. Most overhead line HVDC transmission systems are bipolar [7].

The selection of configurations of HVDC system depends on the function and location of the converter stations. Various schemes and configurations of HVDC systems are shown in simplified form in Figure 2.2[8]:

1. Back-to-back HVDC system.
   In this case the two converter stations are located at the same site and no transmission line or cable is required between the converter bridges. The connection

may be monopolar or bipolar. A block diagram of a back-to-back system is shown in Figure 2.2(a). The two ac systems interconnected may have the same or different nominal frequency, i.e. 50Hz and 60Hz (The back-to-back link can be used to transmit power between two neighboring non-synchronous systems). Examples of such system can be found in Japan and South America [15]. The dc voltage in this case is quite low (i.e. 50kV -150kV) and the converter does not have to be optimized with respect to the dc bus voltage and the associated distance to reduce costs, etc.

2. Transmission between two substations.
When it is economical to transfer electric power through dc transmission from one geographical location to another, a two-terminal or point-to-point HVDC transmission shown in Figure 2.2(b) is used. In other words, dc power from a dc rectifier terminal is transported to the other terminal operating as an inverter. This is typical of most HVDC transmission systems. The link may connect two non-synchronous systems (e.g. between Sweden and Denmark) or connect two substations within one interconnected system (e.g. between Sweden and Finland, or the Three-gorges to Shanghai link in China).

3. Multi-terminal HVDC transmission system.
When three or more HVDC substations are geographically separated with interconnecting transmission lines or cables, the HVDC transmission system is multi-terminal. If all substations are connected to the same voltage then the system is parallel multi-terminal dc shown in Figure 2.2(d). If one or more converter bridges are added in series in one or both poles, then the system is series multi-terminal dc shown in Figure 2.2(c). A combination of parallel and series connections of converter bridges is a hybrid multi-terminal system. Multi-terminal dc systems are more difficult to justify economically because of the cost of the additional substations. Examples of multi-terminal HVDC were implemented in the connection Sardinia-Corsica-Italy(SACOI), the Pacific Intertie in the US and the connection Hydro Quebec-New England Hydro from Canada to the US[16].

2.3 Classic HVDC Systems

2.3.1 Configuration of classic HVDC systems

A classic HVDC system operating in bipolar mode, shown in Figure 2.3, consists of ac filters, shunt capacitor banks or other reactive-compensation equipment, converter transformers, converters, dc reactors, dc filters, and dc lines or cables[9].

Converters
The HVDC converters are an HVDC system's hearts. They perform the conversion from ac to dc (rectifier) at the sending end and from dc to ac (inverter) at the receiving end. HVDC converters are connected to the ac system by means of converter transformers. The classic HVDC converters are current source converters (CSCs). The dc current is kept constant. Magnitude and direction of power flow are controlled by changing magnitude and direction of the dc voltage[17]. The main components are the

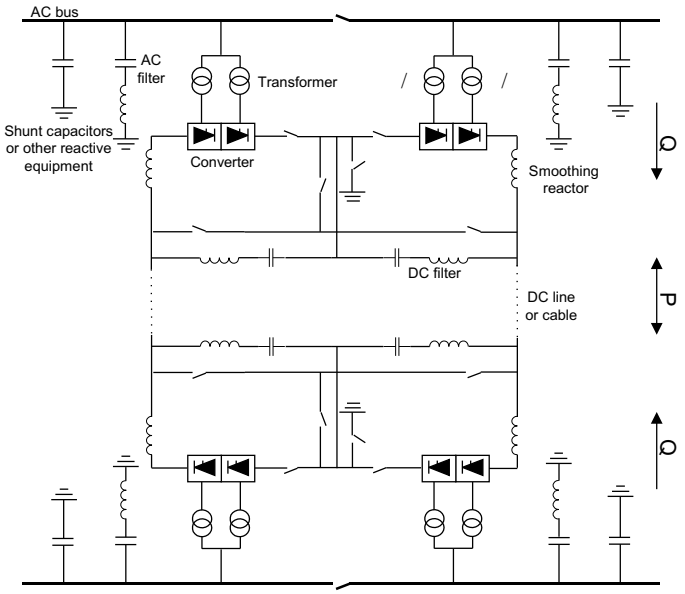


Figure 2.3: A basic configuration for a classic HVDC system.

thyristor valves. The six pulse valve bridge of Figure 2.4 as the basic converter unit of classic HVDC is used equally well for rectification and inversion. The inductance is normally in the form of a transformer. A 12 pulse converter bridge can be built by connecting two six pulse bridges in series or parallel. Each single bridge consists of a certain amount of series connected thyristors with their auxiliary circuits. The bridges are then connected separately to the ac system by means of converter transformers, one of Y-Y winding structure and another Y-Δ winding structure, as shown in Figure 2.3. In this way the 5th and 7th harmonic currents through the two transformers are in opposite phase. This significantly reduces the distortion in the ac system due to the HVDC converters[18][19].

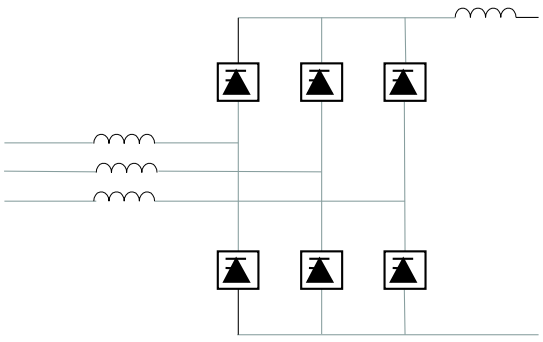


Figure 2.4: Configuration of the basic six pulse valve group.

Transformers

The transformers connect the ac network to the valve bridges, and adjust the ac voltage level on the rectifier terminals to a suitable level based on the dc voltage used for the transmission. The transformers can be of different design depending on the power to be transmitted, and possible transport requirements. The most common type is a single-phase-three-winding design. The windings on network side are connected in star. The

windings on converter side are connected in star for one converter and in delta for the other converter. Three identical transformers are then needed per converter.

Ac-side Harmonic Filters
The HVDC converters produce current harmonics on the ac side, these harmonics are prevented from entering into the connected ac network by ac filters. For example, on the ac side of a 12-pulse HVDC converter, current harmonics of the order of 11, 13, 23, 25 and higher are generated. Filters are installed in order to limit the amount of harmonics to a level allowed by the network. In the conversion process the converter consumes reactive power which is compensated in part by the filter banks and the rest by capacitor banks. In the case of the CCC (capacitor commutated converter) the reactive power is compensated by series capacitors installed in series between the converter valves and the converter transformer. The elimination of switched reactive power compensation equipment simplifies the ac switchyard and minimizes the number of circuit-breakers needed, which will reduce the area required for an HVDC station built with CCC [20] [21].

Dc filters
The HVDC converters produce ripple on the dc voltage. Voltage ripple in the frequency band between a few hundred Hz and a few kHz causes interference to telephone circuits near the dc line. Therefore, specially designed dc filters are used in order to reduce the ripple. Usually no dc filters are needed for pure cable transmission nor for Back-to-Back HVDC stations. However, it is necessary to install dc filters if an overhead line is used in part or all of the transmission system. The filters needed to take care of the harmonics generated on the dc end, are usually considerably smaller and less expensive than the filters on the ac side. Both passive and active dc filters can be used. In active filters power electronics is used to compensate the harmonic distortion. In modern installations active dc filters are used. Active filters are considered more flexible than passive filters, and become cheaper than passive filters for more complex tasks[22].

HVDC cables or overhead lines
HVDC cables are normally used for submarine transmission. No serious length limitation exists for HVDC cables. For a back to back HVDC system, no dc cable or overhead line is needed. For connections over land, overhead lines are typically used. However the tendency is to also move to cables for connections over land, due to environmental concerns.

Control of Classic HVDC Systems
The power transmitted over the HVDC link is controlled through the control system where one of the converters controls the dc voltage and the other converter controls the current through the dc circuit. The control system acts through firing angle adjustments of the valves and through tap changer adjustments on the converter transformers to obtain the desired combination of voltage and current. The control systems of the two stations of a bipolar HVDC system usually communicate with each other through a telecommunication link.

Protection of Classic HVDC Systems
Dc converter stations form an integral part with the ac system, and their basic protection philosophy is thus greatly influenced by ac-system protection principles. However, the limitations of dc circuit breakers and the speed of controllability of HVDC converters influence some departure from the conventional protection philosophy. Fur-

thermore, the series connection for converter equipment also presents some special problems not normally encountered in ac substations.

2.3.2 Advantages of Classic HVDC Systems

It is important to remark that an HVDC system not only transmits electrical power, but it also has a lot of value added which should have been necessary to solve by other means in the case of using conventional ac transmission. Some of these aspects are:

- No limits in transmitted distance. This is valid for both overhead lines and sea or underground cables.
- Very fast and accurate control of power flow, which implies stability improvements, not only for the HVDC link but also for the surrounding ac system.
- Magnitude and direction of power flow can be changed very quickly (bi-directionality).
- An HVDC link does not increase the short-circuit power in the connecting point. This means that it will not be necessary to change the circuit breakers in the existing network.
- HVDC can carry more power for a given size of conductor.
- The need for right-of-way is much smaller for HVDC than for an ac connection, for the same transmitted power. The environmental impact is therefore smaller with HVDC, and it is easier to obtain permission to build.
- Power can be transmitted between two ac-systems operating at different nominal frequencies or at the same frequency but without being synchronized.

2.3.3 Applications of Classic HVDC systems

The first application for classic HVDC systems was to provide point to point electrical power interconnections between asynchronous ac power networks. There are other applications which can be met by HVDC converter transmission which include:

- Interconnections between asynchronous systems. Some continental electric power systems consisting of asynchronous networks such as the East, West, Texas and Quebec networks in North America make use of HVDC interconnections.
- Deliver energy from remote energy sources. Where generation has been developed at remote sites of available energy, HVDC transmission has been an economical means to bring the electricity to load centers. The main application has been the connection of remote hydro-stations to load centers.
- Import electric energy into congested load areas. In areas where new generation is impossible to bring into service to meet load growth or replace inefficient or decommissioned plant, underground dc cable transmission is a viable means to import electricity.

- Increasing the capacity of existing ac transmission by conversion to dc transmission. New transmission rights-of-way may be impossible to obtain. Existing overhead ac transmission lines upgraded to or overbuilt with dc transmission can substantially increase the power transfer capability on the existing right-of-way.

- Power flow control. Ac networks do not easily accommodate desired power flow control. Power marketers and system operators may require the power flow control capability provided by HVDC transmission.

- Stabilization of electric power networks. Some wide spread ac power system networks operate at stability limits well below the thermal capacity of their transmission conductors. HVDC transmission is an option to consider to increase utilization of network conductors along with the various power electronic controllers which can be applied on ac transmission.

- An HVDC transmission line has lower losses than ac lines for the same power capacity. The losses in the converter stations have of course to be added, but above a certain break-even distance, the total HVDC transmission losses become lower than the ac losses. HVDC cables also have lower losses than ac cables.

Although thyristor-based HVDC systems represent mature technology, there are still exciting developments worth mentioning such as:

- active ac and dc filtering.

- capacitor commutated converter(CCC) based systems[9].
  An improvement in the thyristor-based commutation, the CCC concept is characterized by the use of commutation capacitors inserted in series between the converter transformers and the thyristor valves. The commutation capacitors reduce the risk of commutation failure of the converters when connected to weak networks.

- air-insulated outdoor thyristor valves.

- new and advanced cabling technology.

- direct connection of generators to HVDC converters.

2.4 VSC-HVDC system

2.4.1 Configuration

The configuration of a VSC-HVDC system shown in Figure 2.5, consists of ac filters, transformers, converters, phase reactors, dc capacitors and dc cables. The detail is described in Chapter 3.

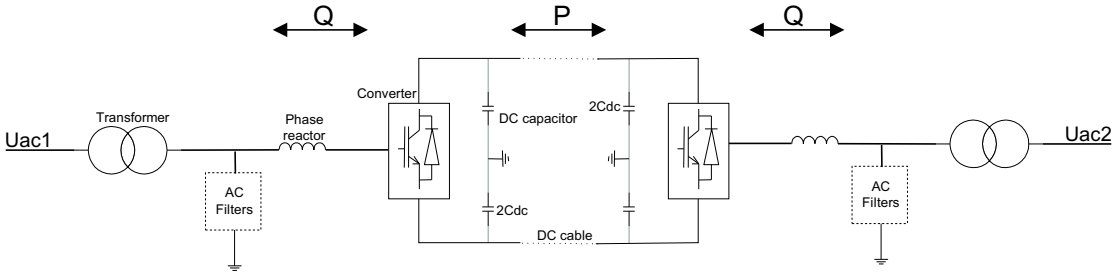


Figure 2.5: A VSC-HVDC system.

2.4.2 Advantages and Applications of VSC-HVDC

The main difference in operation between classic HVDC and VSC-HVDC is the higher controllability of the latter. This leads to a number of new advantages and applications, some of which are given below. This is a very new technology and the number of installations in use is still very limited. Most of the examples given below are only potential applications[9][23][24]. The general agreement appears that the technical potential is very large, the limitations are mainly on the economic side.

- Independent control of active and reactive power without any needs for extra compensating equipment.
  With PWM, VSC-HVDC offers the possibility to control both active and reactive power independently. While the transmitted active power is kept constant the reactive power controller can automatically control the voltage in the ac-network. Reactive power generation and consumption of a VSC-HVDC converter can be used for compensating the needs of the connected network within the rating of a converter.

- Mitigation of power quality disturbances.
  The reactive power capabilities of VSC-HVDC can be used to control the ac network voltages, and thereby contribute to an enhanced power quality. Furthermore, the faster response due to increased switching frequency(PWM) offers new levels of performance regarding power quality control such as flicker and mitigation of voltage dips, harmonics etc. Power quality problems are issues of priority for owners of industrial plants, grid operators as well as for the general public[4].

- No contribution to short circuit currents.
  The converter works independently of any ac source, which makes it less sensitive for disturbances in the ac network and ac faults do not drastically affect the dc side. If ac systems have ground faults or short circuits, whereupon the ac voltage drops, the dc power transmitted is automatically reduced to a predetermined value.

- Reduced risk of commutation failures.
  Disturbances in the ac system may lead to commutation failures in classic HVDC system. As VSC-HVDC uses self-commutating semiconductor devices, the presence of a sufficiently-high ac voltage is no longer needed. This significantly re-

duces the risk of commutation failures, and extends the use of the HVDC system in stability control.

- communication not needed.
  The control systems on rectifier and inverter side operate independently of each other. They do not depend on a telecommunication connection. This improves the speed and the reliability of the controller.

- Feeding islands and passive ac networks.
  The VSC converter is able to creates its own ac voltage at any predetermined frequency, without the need for rotating machines. It may be used to supply industrial installations or large wind farms.

- Multi-terminal dc grid.
  VSC converters are very suitable for creating a dc grid with a large number of converters, since very little coordination is needed between the interconnected VSC-HVDC converters.

In the forthcoming chapters the design and the control of VSC-HVDC will be discussed in more detail. Some of the issues mentioned in this section will be addressed in more detail later.

Chapter 3

Design and operation of VSC-HVDC

3.1 Introduction

VSC-HVDC is a new dc transmission system technology. It is based on the voltage source converter, where the valves are built by IGBTs and PWM is used to create the desired voltage waveform. With PWM it is possible to create any waveform (up to a certain limit set by the switching frequency), any phase angle and magnitude of the fundamental component. Changes in waveform, phase angle and magnitude can be made by changing the PWM pattern, which can be done almost instantaneously. Thus, the voltage source converter can be considered as a controllable voltage source. This high controllability allows for a wide range of applications. From a system point of view VSC-HVDC acts as a synchronous machine without mass that can control active and reactive power almost instantaneously. In this chapter, the topology of the investigated VSC-HVDC is discussed. Design considerations and modelling aspects of the VSC-HVDC are given. The topology selection for the VSC-HVDC is based on the desired capabilities.

3.2 System description

3.2.1 Physical structure

The main function of the VSC-HVDC is to transmit constant dc power from the rectifier to the inverter. As shown in Figure 3.1, it consists of dc-link capacitors C_{dc}, two converters, passive high-pass filters, phase reactors, transformers and dc cable.

Converters

The converters are VSCs employing IGBT power semiconductors, one operating as a rectifier and the other as an inverter. The two converters are connected either back-to-back or through a dc cable, depending on the application. This is described in section 3.2.2 in detail.

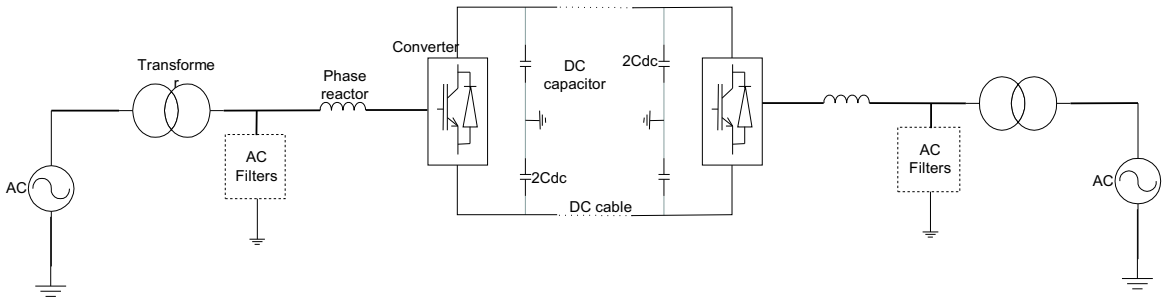


Figure 3.1: Topology of VSC-HVDC.

Transformers

Normally, the converters are connected to the ac system via transformers. The most important function of the transformers is to transform the voltage of the ac system to a value suitable to the converter. It can use simple connection (two-winding instead of three to eight-winding transformers used for other schemes[5]). The leakage inductance of the transformers is usually in the range 0.1-0.2p.u..

Phase reactors

The phase reactors are used for controlling both the active and the reactive power flow by regulating currents through them. The reactors also function as ac filters to reduce the high frequency harmonic contents of the ac currents which are caused by the switching operation of the VSCs. The reactors are essential for both the active and reactive power flow, since these properties are determined by the power frequency voltage across the reactors. The reactors are usually about 0.15p.u. impedance.

Ac filters

The ac voltage output contains harmonic components, derived from the switching of the IGBT's. These harmonics have to be taken care of preventing them from being emitted into the ac system and causing malfunctioning of ac system equipment or radio and telecommunication disturbances. High-pass filter branches are installed to take care of these high order harmonics. With VSC converters there is no need to compensate any reactive power consumed by the converter itself and the current harmonics on the ac side are related directly to the PWM frequency. The amount of low-order harmonics in the current is small. Therefore the amount of filters in this type of converters is reduced dramatically compared with natural commutated converters. This is described in section 3.2.3 in detail.

Dc capacitors

On the dc side there are two capacitor stacks of the same size. The size of these capacitors depends on the required dc voltage. The objective for the dc capacitor is primarily to provide a low inductive path for the turned-off current and an energy storage to be able to control the power flow. The capacitor also reduces the voltage ripple on the dc side. This is described in section 3.2.4 in detail.

Dc cables

The cable used in VSC-HVDC applications is a new developed type, where the insulation is made of an extruded polymer that is particularly resistant to dc voltage.

Polymeric cables are the preferred choice for HVDC, mainly because of their mechanical strength, flexibility, and low weight[24].

3.2.2 Converters

The converters so far employed in actual transmission applications are composed of a number of elementary converters, that is, of three-phase, two-level, six-pulse bridges, as shown in Figure 3.2, or three-phase, three-level, 12-pulse bridges, as shown in Figure 3.3.

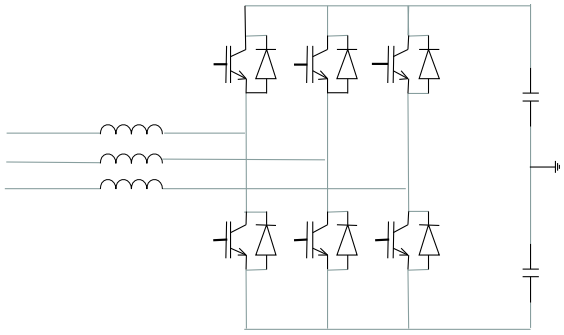


Figure 3.2: Two-level VSC converter.

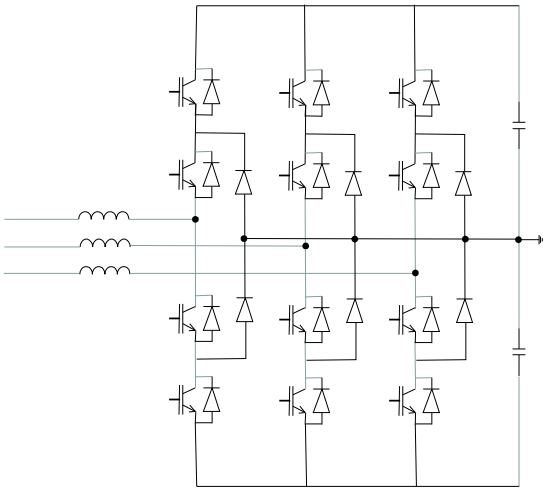


Figure 3.3: Three-level VSC converter.

The two-level bridge is the most simple circuit configuration that can be used for building up a three-phase forced commutated VSC bridge. It has been widely used in many applications at a wide range of power levels. As shown in Figure 3.2, the two-level converter is capable of generating the two-voltage levels $-0.5 \cdot U_{dcN}$ and $+0.5 \cdot U_{dcN}$.

The two-level bridge consists of six valves and each valve consists of an IGBT and an anti-parallel diode. In order to use the two-level bridge in high power applications series connection of devices may be necessary and then each valve will be built up of a number of series connected turn-off devices and anti-parallel diodes. The number of

devices required is determined by the rated power of the bridge and the power handling capability of the switching devices.

With a present technology of IGBTs a voltage rating of 2.5kV has recently become available in the market and soon higher voltages are expected. The IGBTs can be switched on and off with a constant frequency of about 2kHz. The IGBT valves can block up to 150kV. A VSC equipped with these valves can carry up to 800A (rms) ac line current. This results in a power rating of approximately 140MVA of one VSC and a ±150kV bipolar transmission system for power ratings up to 200MW[24].

3.2.3 Harmonic filtering

As described above, due to the commutation valve switching process, the currents and the voltages at the inverter and rectifier are not sinusoidal (for example, V_{2i} and i_{vi} in Figure 3.5) . These non-sinusoidal current and voltage waveforms consist of the fundamental frequency ac component plus higher-order harmonics. Passive high-pass ac filters are essential components of the VSC-HVDC topology to filter the high harmonic components. Hence, sinusoidal line currents and voltages can be obtained from the transformer secondary sides (for example, V_{1i} and i_{Ti} in Figure 3.5). Furthermore, the reactive power compensation may be accomplished by high-pass filters.

As stated in [25], a PWM output waveform contains harmonics $M'f_c \pm N'f_1$, where f_c is the carrier frequency, f_1 is the fundamental grid frequency. M' and N' are integers, and the sum $M'+N'$ is an odd integer. Next to the fundamental frequency component, the spectrum of the output voltages contains components around the carrier frequency of the PWM and multiples of the carrier frequency. This is illustrated in Table 3.1, where a summary of the output voltage harmonics obtained by triangular carrier PWM with the frequency modulation ratio m_f equal to 40 corresponding to a switching frequency of 2000 Hz. Here, m_f is defined as:

$$m_f = \frac{f_c}{f_1} \tag{3.1}$$

The selection of m_f depends on the balance between switching losses and harmonic losses. A higher value of m_f (i.e. a higher number of commutations per second) increases the switching losses but reduces the harmonic losses.

M'	1	2	3
Harmonic	$40f_1$	$80f_1$	$120f_1$
	$40f_1 \pm 2f_c$	$80f_1 \pm 1f_c$	$120f_1 \pm 2f_c$
	$40f_1 \pm 4f_c$	$80f_1 \pm 3f_c$	$120f_1 \pm 4f_c$
	$40f_1 \pm 6f_c$	$80f_1 \pm 5f_c$	$120f_1 \pm 6f_c$
	etc.	etc.	etc.

Table 3.1: Spectrum of the output voltage

From Table 3.1, the harmonic contents can be obtained. The higher m_f, the higher the frequency of the lowest order harmonics produced. With the use of PWM, passive high-pass damped filters are selected to filter the high order harmonics. Normally

second and third-order passive high-pass filters shown in Figure 3.4 are used in HVDC schemes. These are designed to reduce the injection of harmonics above the 17th order into the ac network[7].

When designing the high damping filters the quality factor Q is chosen to obtain the best characteristic over the required frequency band. There is no optimal Q with tuned filters. The typical value of the quality factor Q is between 0.5 and 5[7].

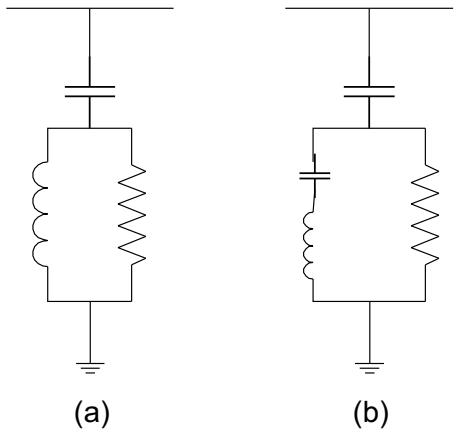


Figure 3.4: Passive high-pass filter. (a)Second-order filter (b)Third-order filter

3.2.4 Design of dc capacitor

The design of dc side capacitor is an important part for the design of an HVDC system. Due to PWM switching action in VSC-HVDC, the current flowing to the dc side of a converter contains harmonics, which will result in a ripple on the dc side voltage. The magnitude of the ripple depends on the dc side capacitor size and on the switching frequency.

The design of the dc capacitor should not only be based on the steady-state operation. During disturbances in the ac system (faults, switching actions) large power oscillations may occur between the ac and the dc side. This in turn will lead to oscillations in the dc voltage and dc overvoltages that may stress the valves. It is important to consider the transient voltage variation constraint when the size of the dc capacitors is selected.

Here, a small dc capacitor C_{dc} can be used, which should theoretically result in faster converter response and to provide an energy storage to be able to control the power flow. The dc capacitor size is characterized as a time constant τ, defined as the ratio between the stored energy at the rated dc voltage and the nominal apparent power of the converter:

$$\tau = \frac{\frac{1}{2}C_{dc}U_{dcN}^2}{S_N} \tag{3.2}$$

where U_{dcN} denotes the nominal dc voltage and S_N stands for the nominal apparent power of the converter. The time constant is equal to the time needed to charge the

capacitor from zero to rated voltage U_{dcN} if the converter is supplied with a constant active power equal to S_N[1]. The time constant τ can be selected less than 5ms to satisfy small ripple and small transient overvoltage on the dc voltage, which will be verified in the simulation. This relatively small time constant allows fast control of active and reactive power. Controller speed of less than 5ms is not practical because the connection will not react. This holds for the control of active power, not for the control of reactive power. Reactive power is generated locally and does not require the dc link.

3.3 Operation of VSC-HVDC

The fundamental operation of VSC-HVDC may be explained by considering each terminal as a voltage source connected to the ac transmission network via series reactors. The two terminals are interconnected by a dc link, as schematically shown in Figure 3.5.

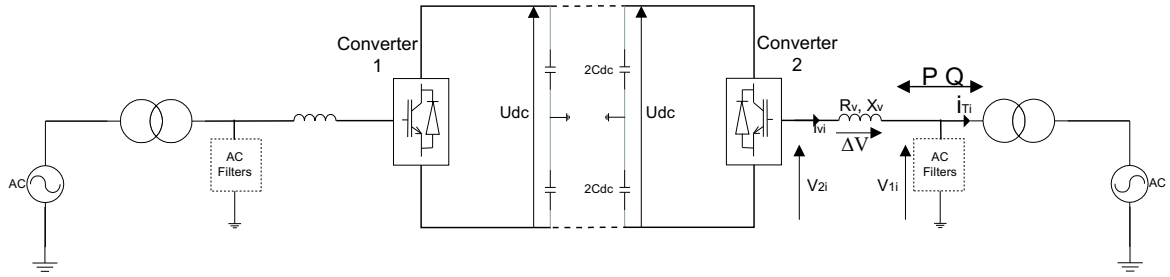


Figure 3.5: Topology of a VSC-HVDC connection.

As mentioned above the converter can be represented as a variable ac voltage source where the amplitude, the phase and the frequency can be controlled independently of each other. It means that the VSC bridge can be seen as a very fast controllable synchronous machine with the instantaneous phase voltage (V_{2i} in Figure 3.5), as described by the following equation.

$$V_{2i} = \frac{1}{2} U_{dc} M \sin(\omega t + \varphi) + \text{ harmonic terms} \tag{3.3}$$

where M is the modulation index which is defined as the ratio of the peak value of the modulating wave and the peak value of the carrier wave; ω is the fundamental frequency, φ is the phase shift of the output voltage, depending on the position of the modulation wave[25].

Variables M and φ can be adjusted independently by the VSC controller to give any combination of voltage magnitude and phase shift in relation to the fundamental-frequency voltage in the ac system. As a result, the voltage drop (ΔV shown in Figure 3.5) across the reactor (X_v shown in Figure 3.5) can be varied to control the active and reactive power flows.

Figure 3.6 shows the fundamental frequency phasor representation for a VSC operating as an inverter and supplying reactive power to the ac system. In this case the

VSC output voltage has a larger amplitude and is phase advanced with respect to the ac system.

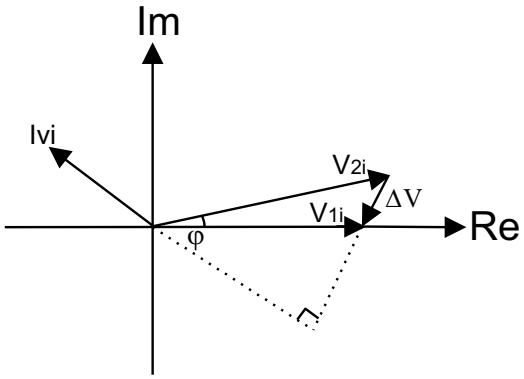


Figure 3.6: Phasor diagram.

The active power flow between the converter and the network can be controlled by changing the phase angle (φ) between the fundamental frequency voltage generated by the converter (V_{2i}) and the voltage (V_{1i}) on the bus[26][27]. The power is calculated according to Equation (3.4) assuming a lossless reactor (X_v).

$$P = \frac{V_{2i} V_{1i} \sin \varphi}{X_v} \tag{3.4}$$

The reactive power flow is determined by the amplitude of V_{2i} which is controlled by the width of the pulses from the converter bridge[26][27]. The reactive power is calculated according to Equation (3.5). The maximum fundamental voltage out from the converter depends on the dc voltage.

$$Q = \frac{V_{2i}(V_{2i} - V_{1i} \cos \varphi)}{X_v} \tag{3.5}$$

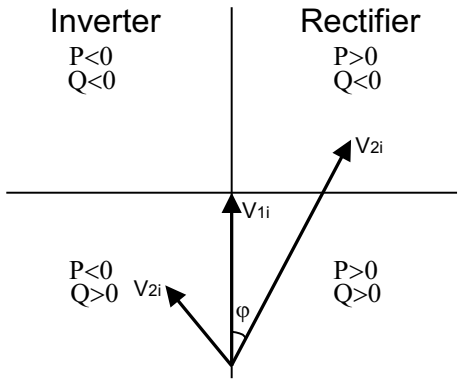


Figure 3.7: Phasor diagram (fundamental) and direction of power flows. The location of the V_{2i} phasor determines the operation mode (rectifier or inverter).

The phasor diagram in Figure 3.7 indicates how the signs of the active and reactive powers depend on the phase and the amplitude of the converter bridge voltage if the

line voltage phasor is assumed constant. For example, if the line voltage V_{1i} is leading the bridge voltage V_{2i}, the active power flows from the ac network to the converter.

In VSC-HVDC connections the active power flow on the ac side is equal to the active power transmitted from the dc side in steady state (losses disregarded). This can be fulfilled if one of the two converters controls the active power transmitted at the same time as the other converter controls the dc voltage. The reactive power generation and consumption can be used for compensating the needs of the connected network. The active /reactive power capabilities can easily be seen in a P-Q diagram shown in Figure 3.8. For the sake of simplicity, the P-Q characteristics are drawn by using per unit values with the assumption that the ac systems at both sides are operated at 1.0 p.u. voltage. Several important properties of the dc links are evident from Figure 3.8[11]. The VSC-HVDC is able to operate at any point within the circle. The radius of which represents the converter MVA rating. The reactive power capabilities can be used to control the ac voltages of the networks connected to the converter. The controllable active power can be transferred in both directions with equal maximum value which is only limited by the power rating.

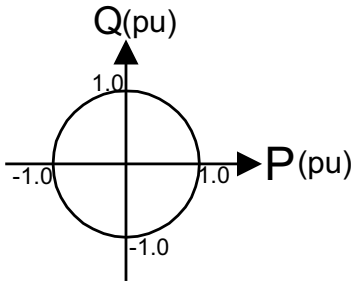


Figure 3.8: P-Q characteristics of an VSC-HVDC.

Chapter 4

Control system

The transfer of energy is controlled in the same way as for a classical HVDC connection: the rectifier side controls the dc voltage; the inverter side controls the active power. Like with classical HVDC the power flow can be in either direction.

With classic HVDC the reactive power cannot be controlled independently of the active power. With VSC-HVDC there is an additional degree of freedom. As described in chapter 2 and 3, VSC-HVDC using PWM technology makes it possible to control the reactive power and the active power independently. The reactive power flow can be controlled separately in each converter by the ac voltage that is requested or set manually without changing the dc voltage. The active power flow can be controlled by dc voltage on the dc side or the variation of frequency of ac side, or set manually. Thus, the active power flow, the reactive power flow, the ac voltage, the dc voltage and the frequency can be controlled when using VSC-HVDC.

The control system of the VSC-HVDC is based on a fast inner current control loop controlling the ac current. The ac current references are supplied by the outer controllers. The outer controllers include the dc voltage controller, the ac voltage controller, the active power controller, the reactive power controller or the frequency controller. The reference value of the active current can be derived from the dc voltage controller, the active power controller and the frequency controller, the reference value of the reactive current can be obtained from the ac voltage controller, the reactive power controller. In all these controllers, integrators can be used to eliminate the steady state errors. For example, as shown in Figure 4.1, either side of the link can choose between ac voltage control and reactive power control. Each of these controllers generates a reference value for the inner current controller. The inner current controller calculates the voltage drop over the converter reactor that will lead to the desired current.

Obviously not all controllers can be used at the same time. The choice of different kinds of controllers to calculate the reference values of the converter current will depend on the application and may require some advanced power system study. For example: the active power controller can be used to control the active power to/from the converter; the reactive power controller can be used to control the reactive power; the ac voltage controller which is usually used when the system supplies a passive network can be used to keep the ac voltage. If the load is a passive system, then VSC-HVDC can control frequency and ac voltage. If the load is an established ac system, then the VSC-HVDC can control ac voltage and power flow. But it should be known that be-

cause the active power flow into the dc link must be balanced, the dc voltage controller is necessary to achieve power balance. Active power out from the network must equal the active power into the network minus the losses in the system, any difference would mean that the dc voltage in the system will rapidly change. The other converters can set any active power value within the limits for the system. The dc voltage controller will ensure active power balance in all cases.

The inner current controller and the various outer controllers will be described in detail in this chapter. Simulation results will be presented in the next chapter.

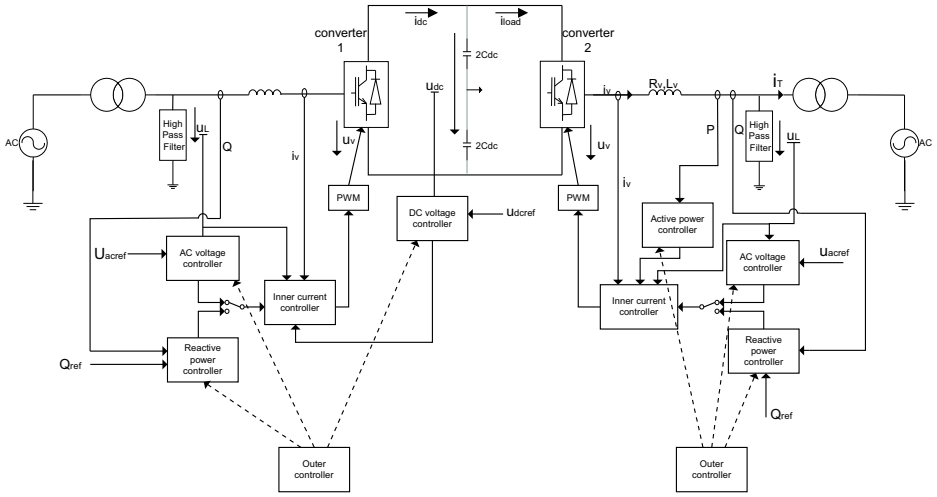


Figure 4.1: Overall control structure of the VSC-HVDC.

4.1 The inner current controller

The inner current control loop can be implemented in the *dq*-frame which is based on the basic relationship of the model. It consists of a PI regulator, a current dependent decoupling factor, and a feedforward control of ac voltage.

The basic relationship is given in [28] between the internal ac bridge voltage, the bus voltage and the ac current. For balanced steady-state operation the *dq* voltages and currents are constant (neglecting waveform distortion, which allows for simple control algorithms). But for unbalanced operation, the positive and negative components of the ac system have to be considered in the control system. To design the control system to meet different operation conditions the inner current controller is divided into two parts: the positive-sequence current controller and the negative-sequence current controller. At the same time, a method for separating positive and negative sequence is adopted.

In order to have a detailed overview of the control system, the control based on the equation for the model shown in Figure 4.1 is presented as follows.

The phase voltages of the transformer secondary side and the phase currents which flow into the converter are decomposed into two balanced positive and negative se-

quences components. For the voltages this reads as:

$$\begin{aligned} u_{La} &= u_{Lap} + u_{Lan} \\ u_{Lb} &= u_{Lbp} + u_{Lbn} \\ u_{Lc} &= u_{Lcp} + u_{Lcn} \end{aligned} \tag{4.1}$$

and for the currents:

$$\begin{aligned} i_{va} &= i_{vap} + i_{van} \\ i_{vb} &= i_{vbp} + i_{vbn} \\ i_{vc} &= i_{vcp} + i_{vcn} \end{aligned} \tag{4.2}$$

where u_{La}, u_{Lb}, u_{Lc} are the phase voltages of the transformer secondary side, i_{va}, i_{vb}, i_{vb} are the phase currents which flow into the VSC, u_{Lap}, u_{Lbp}, u_{Lcp}, u_{Lan}, u_{Lbn}, u_{Lcn}, i_{vap}, i_{vbp}, i_{vcp}, i_{van}, i_{vbn}, i_{vcn} are the corresponding positive sequence components and negative sequence components of voltages and currents. When the system operates in balanced condition, u_{Lan}, u_{Lbn}, u_{Lcn}, i_{van}, i_{vbn}, i_{vcn} are equal to zero.

For each of the phases we can write:

$$u_v - u_L = L_v \frac{\mathrm{d}i_v}{\mathrm{d}t} + R_v i_v \tag{4.3}$$

During unbalanced operation, the expression for the voltage drop over the reactor holds for positive as well as for negative-sequence voltages and currents.

The positive-sequence voltages over the reactor $R_v + j\omega$Ł$_v$ are described by the differential equation:

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{vap} \\ i_{vbp} \\ i_{vcp} \end{bmatrix} &= \begin{bmatrix} -\frac{R_v}{L_v} & 0 & 0 \\ 0 & -\frac{R_v}{L_v} & 0 \\ 0 & 0 & -\frac{R_v}{L_v} \end{bmatrix} \begin{bmatrix} i_{vap} \\ i_{vbp} \\ i_{vcp} \end{bmatrix} \\ + \begin{bmatrix} \frac{1}{L_v} & 0 & 0 \\ 0 & \frac{1}{L_v} & 0 \\ 0 & 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{vap} \\ u_{vbp} \\ u_{vcp} \end{bmatrix} &- \begin{bmatrix} \frac{1}{L_v} & 0 & 0 \\ 0 & \frac{1}{L_v} & 0 \\ 0 & 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{Lap} \\ u_{Lbp} \\ u_{Lcp} \end{bmatrix} \end{aligned} \tag{4.4}$$

and the negative-sequence voltages:

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{van} \\ i_{vbn} \\ i_{vcn} \end{bmatrix} &= \begin{bmatrix} -\frac{R_v}{L_v} & 0 & 0 \\ 0 & -\frac{R_v}{L_v} & 0 \\ 0 & 0 & -\frac{R_v}{L_v} \end{bmatrix} \begin{bmatrix} i_{van} \\ i_{vbn} \\ i_{vcn} \end{bmatrix} \\ + \begin{bmatrix} \frac{1}{L_v} & 0 & 0 \\ 0 & \frac{1}{L_v} & 0 \\ 0 & 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{van} \\ u_{vbn} \\ u_{vcn} \end{bmatrix} &- \begin{bmatrix} \frac{1}{L_v} & 0 & 0 \\ 0 & \frac{1}{L_v} & 0 \\ 0 & 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{Lan} \\ u_{Lbn} \\ u_{Lcn} \end{bmatrix} \end{aligned} \tag{4.5}$$

where u_{vap}, u_{vbp}, u_{vcp}, u_{van}, u_{vbn}, u_{vcn} are the corresponding positive sequence components and negative sequence components of voltages of the VSC side, respectively.

Equation (4.4) and (4.5) can be transformed to the $\alpha\beta$-frame. This gives for the positive-sequence voltages and currents:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{v\alpha p} \\ i_{v\beta p} \end{bmatrix} = \begin{bmatrix} -\frac{R_v}{L_v} & 0 \\ 0 & -\frac{R_v}{L_v} \end{bmatrix}\begin{bmatrix} i_{v\alpha p} \\ i_{v\beta p} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix}\begin{bmatrix} u_{v\alpha p} \\ u_{v\beta p} \end{bmatrix} - \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix}\begin{bmatrix} u_{L\alpha p} \\ u_{L\beta p} \end{bmatrix} \tag{4.6}$$

and for the negative-sequence:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{v\alpha n} \\ i_{v\beta n} \end{bmatrix} = \begin{bmatrix} -\frac{R_v}{L_v} & 0 \\ 0 & -\frac{R_v}{L_v} \end{bmatrix}\begin{bmatrix} i_{v\alpha n} \\ i_{v\beta n} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix}\begin{bmatrix} u_{v\alpha n} \\ u_{v\beta n} \end{bmatrix} - \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix}\begin{bmatrix} u_{L\alpha n} \\ u_{L\beta n} \end{bmatrix} \tag{4.7}$$

The following transformation from the three-phase system to $\alpha\beta$-frame has been used, by assuming $x_a + x_b + x_c = 0$:

$$\bar{x}_{\alpha\beta} = x_\alpha + jx_\beta = k[x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{j\frac{4\pi}{3}}] \tag{4.8}$$

where the factor k is usually equal to $\sqrt{\frac{2}{3}}$ for ensuring power invariance between the two systems. Equation (4.8) can be written as:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{6}} \\ 0 & \sqrt{\frac{1}{2}} & -\sqrt{\frac{1}{2}} \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{4.9}$$

The inverse transformation is:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\sqrt{\frac{1}{6}} & \sqrt{\frac{1}{2}} \\ -\sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{2}} \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{4.10}$$

The transformation from phase quantities to symmetrical component quantities, is normally defined for complex phasors. This transformation is not very efficient however for time-domain signals as it would require a DFT (Digital Fourier Transform) and an inverse DFT to be applied. Several algorithms have been proposed that are more efficient in time domain. The method used in this thesis is shown in Figure 4.2. The $\alpha\beta$ transformation is the same for positive and negative-sequence so that one transformation is sufficient.

Figure 4.2 illustrates the block diagram for calculating the positive and negative sequence dq components[1].

The equations implemented in this block diagram in the digital control system for obtaining the positive and negative sequence $\alpha\beta$ components can be expressed as[1]:

$$x_{\alpha n}(k) = \frac{1}{2}\left[x_\alpha(k) + x_\beta(k - \frac{1}{4}\frac{T}{Ts})\right] \tag{4.11}$$

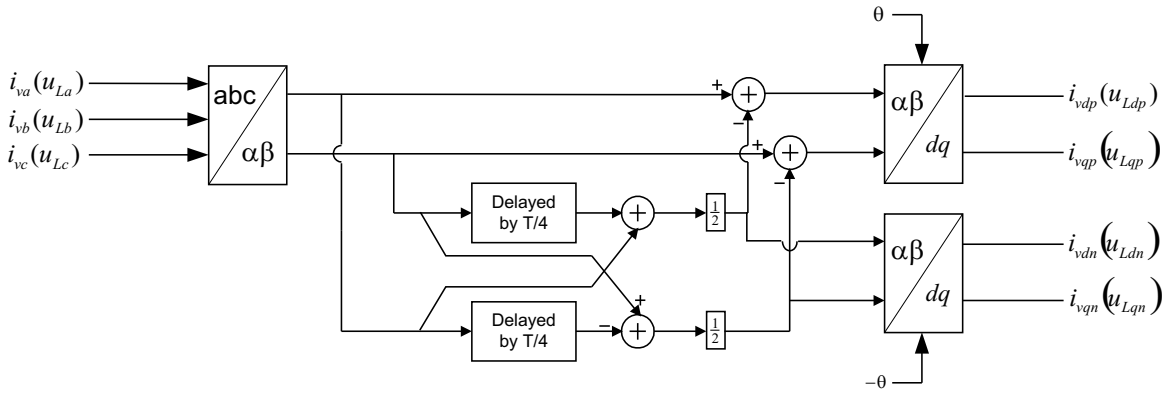


Figure 4.2: Separation of the negative and positive sequence components.

$$x_{\beta n}(k) = \frac{1}{2}\left[x_\beta(k) - x_\alpha(k - \frac{1}{4}\frac{T}{Ts})\right] \tag{4.12}$$

$$x_{\alpha p}(k) = x_\alpha(k) - x_{\alpha n}(k) = \frac{1}{2}\left[x_\alpha(k) - x_\beta(k - \frac{1}{4}\frac{T}{Ts})\right] \tag{4.13}$$

$$x_{\beta p}(k) = x_\beta(k) - x_{\beta n}(k) = \frac{1}{2}\left[x_\beta(k) + x_\alpha(k - \frac{1}{4}\frac{T}{Ts})\right] \tag{4.14}$$

where $x_{\alpha p}, x_{\alpha n}, x_{\beta p}$ and $x_{\beta n}$ are the positive and negative sequence components in the α and β axis, respectively. T corresponds to one cycle period of the network fundamental frequency. T_s is the sampling period of the control system.

And the transformations are made from $\alpha\beta$-frame to dq-frame. For positive-sequence quantities, the transformation is.

$$\begin{bmatrix} x_{dp} \\ x_{qp} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{\alpha p} \\ x_{\beta p} \end{bmatrix} \tag{4.15}$$

For negative-sequence voltages and currents the rotation is in the opposite direction.

$$\begin{bmatrix} x_{dn} \\ x_{qn} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{\alpha n} \\ x_{\beta n} \end{bmatrix} \tag{4.16}$$

where θ is equal to ωt, and ω is the fundamental angular frequency.

Equation (4.6) and (4.7) can be further transferred into the rotating dq-frame:

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} = \begin{bmatrix} -\frac{R_v}{L_v} & \omega \\ -\omega & -\frac{R_v}{L_v} \end{bmatrix} \begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{vdp} \\ u_{vqp} \end{bmatrix} \\ - \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{Ldp} \\ u_{Lqp} \end{bmatrix} \end{aligned} \tag{4.17}$$

and

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} = \begin{bmatrix} -\frac{R_v}{L_v} & -\omega \\ \omega & -\frac{R_v}{L_v} \end{bmatrix} \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{vdn} \\ u_{vqn} \end{bmatrix} \\ - \begin{bmatrix} \frac{1}{L_v} & 0 \\ 0 & \frac{1}{L_v} \end{bmatrix} \begin{bmatrix} u_{Ldn} \\ u_{Lqn} \end{bmatrix} \end{aligned} \tag{4.18}$$

where i_{vdp}, i_{vdn}, i_{vqp}, i_{vqn} are referred to the positive-sequence reactive current, the negative-sequence reactive current, the positive-sequence active current, and the negative-sequence active current, respectively.

Similarly, the transformations from the dq-frame to $\alpha\beta$-frame are given by

$$\begin{bmatrix} x_{\alpha p} \\ x_{\beta p} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{dp} \\ x_{qp} \end{bmatrix} \tag{4.19}$$

for the positive-sequence quantities. And by

$$\begin{bmatrix} x_{\alpha n} \\ x_{\beta n} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_{dn} \\ x_{qn} \end{bmatrix} \tag{4.20}$$

for the negative-sequence quantities.

The positive and negative sequence voltages of the VSC side are obtained from (4.17) and (4.18):

$$u_{vdp} = u_{Ldp} + R_v i_{vdp} - \omega L_v i_{vqp} + L_v \frac{\mathrm{d}}{\mathrm{d}t} i_{vdp} \tag{4.21}$$

$$u_{vqp} = u_{Lqp} + R_v i_{vqp} + \omega L_v i_{vdp} + L_v \frac{\mathrm{d}}{\mathrm{d}t} i_{vqp} \tag{4.22}$$

and

$$u_{vdn} = u_{Ldn} + R_v i_{vdn} + \omega L_v i_{vqn} + L_v \frac{\mathrm{d}}{\mathrm{d}t} i_{vdn} \tag{4.23}$$

$$u_{vqn} = u_{Lqn} + R_v i_{vqn} - \omega L_v i_{vdn} + L_v \frac{\mathrm{d}}{\mathrm{d}t} i_{vqn} \tag{4.24}$$

The mean voltages over the sample period k to $k+1$ are derived by integrating (4.21), (4.22), (4.23) and (4.24) from kT_s to $(k+1)\,T_s$ and dividing by T_s(where T_s is the sampling time).

$$\bar{u}_{vdp} = \bar{u}_{Ldp} + R_v \bar{i}_{vdp} - \omega L_v \bar{i}_{vqp} + \frac{L_v}{T_s}\{i_{vdp}(k+1) - i_{vdp}(k)\} \tag{4.25}$$

$$\bar{u}_{vqp} = \bar{u}_{Lqp} + R_v \bar{i}_{vqp} + \omega L_v \bar{i}_{vdp} + \frac{L_v}{T_s}\{i_{vqp}(k+1) - i_{vqp}(k)\} \tag{4.26}$$

and

$$\bar{u}_{vdn} = \bar{u}_{Ldn} + R_v \bar{i}_{vdn} + \omega L_v \bar{i}_{vqn} + \frac{L_v}{T_s}\{i_{vdn}(k+1) - i_{vdn}(k)\} \tag{4.27}$$

$$\bar{u}_{vqn} = \bar{u}_{Lqn} + R_v \bar{i}_{vqn} - \omega L_v \bar{i}_{vdn} + \frac{L_v}{T_s}\{i_{vqn}(k+1) - i_{vqn}(k)\} \tag{4.28}$$

where the average voltages over the sampling period are defined as:

$$\begin{aligned} \bar{u}_{vdp} &= \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} u_{vdp}(t)\mathrm{d}t \\ \bar{u}_{vqp} &= \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} u_{vqp}(t)\mathrm{d}t \\ \bar{u}_{vdn} &= \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} u_{vdn}(t)\mathrm{d}t \\ \bar{u}_{vqn} &= \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} u_{vqn}(t)\mathrm{d}t \end{aligned}$$

By assuming linear current and constant network voltage (The network voltage varies very little during a switching time period[29]) during one sample period T_s, we obtain from (4.25) through (4.28).

$$u_{vdp}(k+1) = u_{Ldp}(k) + \frac{R_v}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\} - \frac{\omega L_v}{2}\{i_{vqp}(k+1) + i_{vqp}(k)\} + \frac{L_v}{T_s}\{i_{vdp}(k+1) - i_{vdp}(k)\} \tag{4.29}$$

$$u_{vqp}(k+1) = u_{Lqp}(k) + \frac{R_v}{2}\{i_{vqp}(k+1) + i_{vqp}(k)\} + \frac{\omega L_v}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\} + \frac{L_v}{T_s}\{i_{vqp}(k+1) - i_{vqp}(k)\} \tag{4.30}$$

$$u_{vdn}(k+1) = u_{Ldn}(k) + \frac{R_v}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\} + \frac{\omega L_v}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\} + \frac{L_v}{T_s}\{i_{vdn}(k+1) - i_{vdn}(k)\} \tag{4.31}$$

$$u_{vqn}(k+1) = u_{Lqn}(k) + \frac{R_v}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\} - \frac{\omega L_v}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\} + \frac{L_v}{T_s}\{i_{vqn}(k+1) - i_{vqn}(k)\} \tag{4.32}$$

The control is based on (4.29), (4.30), (4.31) and (4.32). Furthermore, the inner current loop control usually gives a time delay of one sample due to the calculation time and the introduction of a very short dead-time between the turn-off of one valve and the turn-on of the valve in the same leg to avoid that the dc side is short-circuited through the leg. The voltages and currents at time step $(k+1)$ are thus equal to the reference values at time step k.

$$v_{vdp}(k+1) = v^*_{vdp}(k) \tag{4.33}$$
$$v_{vqp}(k+1) = v^*_{vqp}(k) \tag{4.34}$$
$$v_{vdn}(k+1) = v^*_{vdn}(k) \tag{4.35}$$
$$v_{vqn}(k+1) = v^*_{vqn}(k) \tag{4.36}$$
$$i_{vdp}(k+1) = i^*_{vdp}(k) \tag{4.37}$$
$$i_{vqp}(k+1) = i^*_{vqp}(k) \tag{4.38}$$
$$i_{vdn}(k+1) = i^*_{vdn}(k) \tag{4.39}$$
$$i_{vqn}(k+1) = i^*_{vqn}(k) \tag{4.40}$$

where $v^*_{vdp}(k), v^*_{vdn}(k), i^*_{vdp}(k), i^*_{vqn}(k), v^*_{vqp}(k), v^*_{vqn}(k), i^*_{vqp}(k), i^*_{vdn}(k)$, are the reference values of the positive and negative voltages and reactive currents, the positive and negative voltages and active currents, respectively.

The resulting control equations can be written as:

$$u^*_{vdp}(k) = u_{Ldp}(k) + R_v i_{vdp}(k) - \frac{\omega L_v}{2}(i^*_{vqp}(k) + i_{vqp}(k)) + k_p(i^*_{vdp}(k) - i_{vdp}(k)) \quad (4.41)$$

$$u^*_{vqp}(k) = u_{Lqp}(k) + R_v i_{vqp}(k) + \frac{\omega L_v}{2}(i^*_{vdp}(k) + i_{vdp}(k)) + k_p(i^*_{vqp}(k) - i_{vqp}(k)) \quad (4.42)$$

$$u^*_{vdn}(k) = u_{Ldn}(k) + R_v i_{vdn}(k) + \frac{\omega L_v}{2}(i^*_{vqn}(k) + i_{vqn}(k)) + k_p(i^*_{vdn}(k) - i_{vdn}(k)) \quad (4.43)$$

$$u^*_{vqn}(k) = u_{Lqn}(k) + R_v i_{vqn}(k) - \frac{\omega L_v}{2}(i^*_{vdn}(k) + i_{vdn}(k)) + k_p(i^*_{vqn}(k) - i_{vqn}(k)) \quad (4.44)$$

where the gain is

$$k_p = k_{pf}(\frac{L_v}{T_s} + \frac{R_v}{2}) \quad (4.45)$$

As the positive and negative sequence circuit impedances are identical, the same decoupling factor can be used for the positive and negative currents controllers. The gain of the P-parts is altered by the factor k_{pf} to stabilize the controller.

Finally, the three-phase reference voltages to control VSC are derived through: (i) Convert derived $v^*_{vdp}(k), v^*_{vdn}(k), v^*_{vqp}(k), v^*_{vqn}(k)$ into $\alpha\beta$-frame. (ii) Separate the positive sequence voltages and the negative sequence voltages in $\alpha\beta$-frame and dq-frame and get the reference voltages in dq-frame and $\alpha\beta$-frame. (iii) Convert obtained results in step(ii) into the three-phase coordinate system to get the three-phase reference voltages. The block diagram of the inner current controller is shown in Figure 4.3. The reference values for the reactive current and the active current ($i^*_{vdp}, i^*_{vqp}, i^*_{vdn}$ and i^*_{vqn} respectively) are obtained from the outer controllers.

Stability analysis of the system can give the proper value for the gain factor k_{pf} of the P-controller. The root locus method is usually applied to analyze the system response with respect to the gain of P-controllers. It is known that the stability boundary for discrete time system is defined as the unit circle. Hence, if the poles of the system are inside the unit disc, the discrete system is stable.

4.2 The outer controllers

4.2.1 The dc voltage controller

The instantaneous active power $P_{ac(abc)}$ and reactive power $Q_{ac(abc)}$ transmitted in the three-phase system on the ac side and the power P_{dc} transmitted on the dc side of the

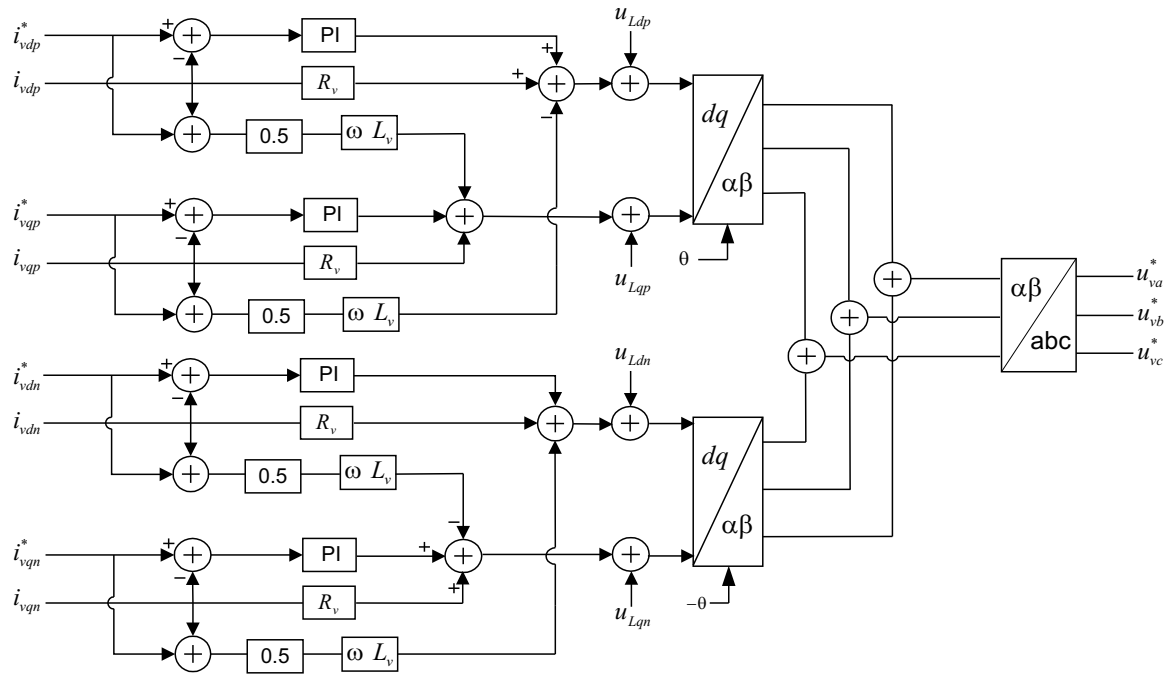


Figure 4.3: Inner current controller.

VSC shown in Figure 4.1 are expressed as:

$$\begin{aligned} P_{ac(abc)} &= u_{La}i_{va} + u_{Lb}i_{vb} + u_{Lc}i_{vc} && (4.46)\\ Q_{ac(abc)} &= (u_{La} - u_{Lb})i_{vc} + (u_{Lb} - u_{Lc})i_{va} \\ &\quad +(u_{Lc} - u_{La})i_{vb} && (4.47)\\ P_{dc} &= u_{dc}i_{dc} && (4.48) \end{aligned}$$

As described above, the three-phase voltages are balanced in normal operation condition, the u_{Lan}, u_{Lbn}, u_{Lcn}, are equal to zero, so the $u_{L\alpha n}$, $u_{L\beta n}$ in the $\alpha\beta$-frame and u_{Ldn}, u_{Lqn} in the dq-frame are equal to zero. So the u_{Ldp}, u_{Lqp} can be described as:

$$\begin{aligned} u_{Ldp} &= 0 \\ u_{Lqp} &= U && (4.49) \end{aligned}$$

Where U is the amplitude of the phase voltage. The instantaneous active and reactive power $P_{ac(dq)}$ and $Q_{ac(dq)}$ in dq-frame can be obtained from (4.46), (4.47), (4.48) and (4.49).

$$\begin{aligned} P_{ac(dq)} &= u_{Ldp}i_{vdp} + u_{Lqp}i_{vqp} \\ &= u_{Lqp}i_{vqp} && (4.50)\\ Q_{ac(dq)} &= u_{Lqp}i_{vdp} - u_{Ldp}i_{vqp} \\ &= u_{Lqp}i_{vdp} && (4.51) \end{aligned}$$

Note that it is assumed here only that the network-side voltage u_L is balanced. No assumption has been made concerning the converter voltage and the converter current.

Normally, the response of the inner current controller is very fast and the dc voltage controller is much slower than the inner current controller. At the time-scale of interest

to the dc voltage controller, the currents may thus be assumed equal to their reference values. The expressions for active and reactive power will be:

$$P_{ac(dq)} = u_{Lqp} i^*_{vqp} \tag{4.52}$$
$$Q_{ac(dq)} = u_{Lqp} i^*_{vdp} \tag{4.53}$$

If the power balance between the ac and the dc side of the converter is ideal (i.e. the converter losses and the losses in the reactor can be neglected), the power transmitted is

$$P_{ac(dq)} = u_{Lqp} i^*_{vqp} = P_{dc} = u_{dc} i_{dc} \tag{4.54}$$

So

$$i_{dc} = \frac{u_{Lqp} i^*_{vqp}}{u_{dc}} \tag{4.55}$$

Any unbalance between ac and dc power leads to a change in voltage over the dc-side capacitors. The continuous-time equation for the dc voltage over the capacitors is:

$$C_{dc} \frac{\mathrm{d}}{\mathrm{d}t} u_{dc} = i_{dc} - i_{load} \tag{4.56}$$

where i_{load} is the current through the dc cable or line shown in Figure 4.1.

By integrating between kT_s and $(k+1)T_s$ and then dividing by T_s , the following equation can be obtained from (4.56).

$$\frac{C_{dc}}{T_s}\{u_{dc}(k+1) - u_{dc}(k)\} = \bar{i}_{dc} - \bar{i}_{load} \tag{4.57}$$

where the average currents over the sampling period are defined as:

$$\bar{i}_{dc} = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} i_{dc}(t) \mathrm{d}t$$
$$\bar{i}_{load} = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} i_{load}(t) \mathrm{d}t$$

Here, the currents i_{dc} and i_{load} on the dc side are both constant in steady state. So their average values are equal to these constant values, thus

$$\frac{C_{dc}}{T_s}\{u_{dc}(k+1) - u_{dc}(k)\} = i_{dc}(k) - i_{load}(k) \tag{4.58}$$

The dc voltage reference can be obtained due to the consideration of the one sample time delay in the controller

$$u_{dc}(k+1) = u^*_{dc}(k) \tag{4.59}$$

Substituting (4.55) and (4.59) into (4.58) yields

$$\frac{C_{dc}}{T_s}(u^*_{dc}(k) - u_{dc}(k)) = \frac{u_{Lqp}(k) i^*_{vqp}(k)}{u_{dc}(k)} - i_{load}k) \tag{4.60}$$

So the current reference $i^*_{vq}(k)$ can be obtained by (4.60), that is

$$i^*_{vqp}(k) = \frac{u_{dc}(k)}{u_{Lqp}(k)}\{\ \frac{C_{dc}}{T_s}(u^*_{dc}(k) - u_{dc}(k)) + i_{load}(k)\} \tag{4.61}$$

So

$$i^*_{vqp}(k) = k_{dcp}(u^*_{dc}(k) - u_{dc}(k)) + k_{load}i_{load}(k) \tag{4.62}$$

where

$$\begin{aligned} k_{dcp} &= k_{dcpf}\frac{u_{dc}(k)}{u_{Lqp}(k)}\frac{C_{dc}}{T_s} \\ &= k_{dcpf}\frac{u^*_{dc}(k)}{u_{Lqp}(k)}\frac{C_{dc}}{T_s} \end{aligned} \tag{4.63}$$

$$\begin{aligned} k_{load} &= \frac{u_{dc}(k)}{u_{Lqp}(k)} \\ &= \frac{u^*_{dc}(k)}{u_{Lqp}(k)} \end{aligned} \tag{4.64}$$

where the factor k_{dcpf} can alter the gain of the dc voltage controller to stabilize the controller.

The resulting block diagram of the dc voltage controller is illustrated in Figure 4.4.

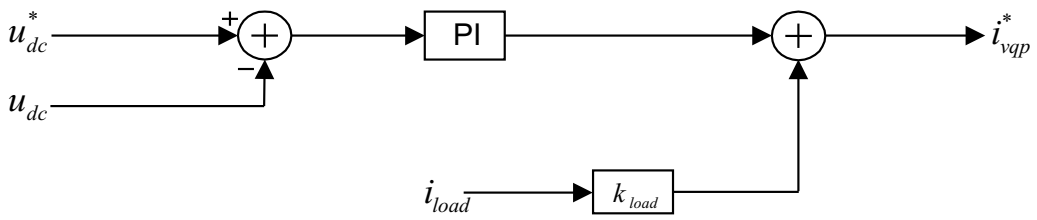


Figure 4.4: Dc voltage controller.

4.2.2 The active power controller

The simple method to control the active power is an open-loop controller. The reference of the active current is obtained by using (4.52) (which assumes balanced voltages), resulting in:

$$i^*_{vqp} = \frac{P^*}{u_{Lqp}} \tag{4.65}$$

If more accurate control of the active power is needed, a combination of a feedback loop and an open loop can be used. The structure of the resulting active power controller is illustrated in Figure 4.5.

4.2.3 The reactive power controller

The reactive power controller is similar to the active power controller.

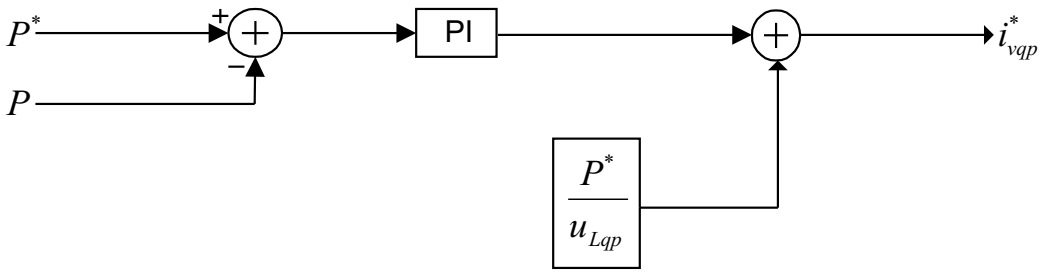


Figure 4.5: Active power controller.

An open-loop controller is obtained by using (4.52), that is:

$$i^*_{vdp} = \frac{Q^*}{u_{Lqp}} \tag{4.66}$$

Another method is to combine a feedback loop with an open loop. The block diagram of the reactive power controller is in Figure 4.6.

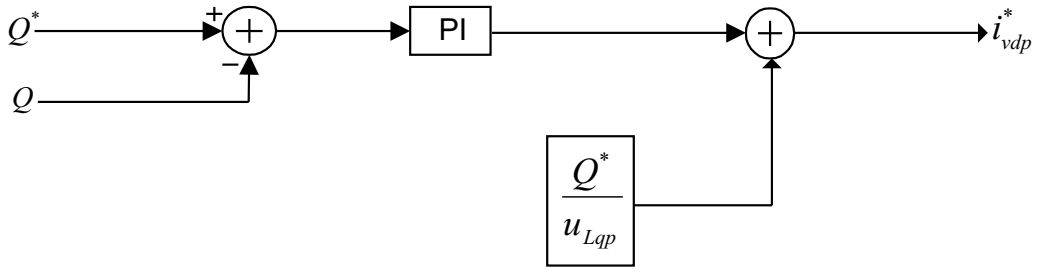


Figure 4.6: Reactive power controller.

4.2.4 The frequency controller

The purpose of the frequency controller is to keep the frequency at its reference value. The change in power for a given change in the frequency in an interconnected system is known as the stiffness of the system[17]. The power-frequency characteristic may be approximated by a straight line and

$$\Delta P/\Delta f = K \tag{4.67}$$

where ΔP is the power unbalance, Δf is the frequency drift, K is a constant.

So according to the (4.52) and (4.67) it is sufficient to use PI-controller in the feedback loop of the controlled frequency and the control error can be reduced to zero in steady state. The block diagram of the frequency controller is shown in Figure 4.7.

It should be noted that such a frequency controller can only be used for the supply to a system without other sources of frequency control. In a system with more sources of frequency control, a P-controller should be used to share the load variations over the source.

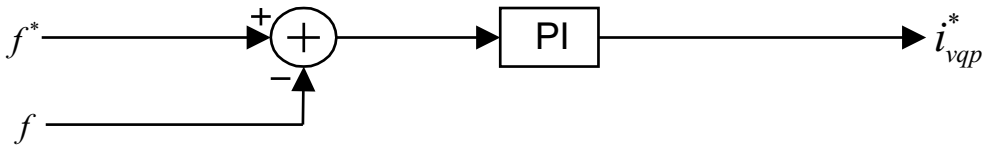


Figure 4.7: Frequency controller.

4.2.5 The ac voltage controller

As shown in Figure 3.5 in chapter 3, the voltage drop ΔV over the reactor X_v can be described as:

$$\begin{aligned} \Delta V &= V_{2i} - V_{1i} \\ &= \Delta V_p + j\Delta V_q \\ &= \frac{R_v P + X_v Q}{V_{1i}} + j\frac{X_v P - R_v Q}{V_{1i}} \end{aligned} \tag{4.68}$$

If

$$\Delta V_q \ll V_{1i} + \Delta V_p \tag{4.69}$$

then

$$\Delta V \approx \frac{R_v P + X_v Q}{V_{1i}} \tag{4.70}$$

For ac networks most power circuits satisfy $X_v \gg R_v$, therefore the voltage drop ΔV depends only on the reactive power flow Q.

So the variation of ac voltage V_{1i} depends only on the reactive power flow. From (4.53) and (4.70), the block diagram of the ac voltage controller can be obtained as shown in Figure 4.8.

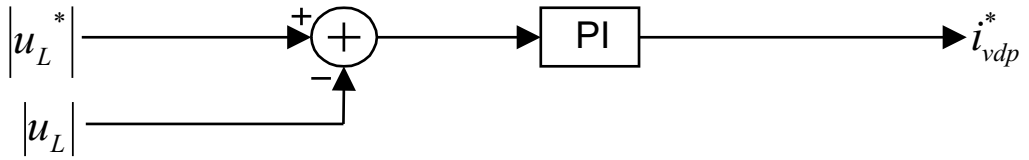


Figure 4.8: Ac voltage controller.

where $|u_L|$ is the amplitude of the line voltage, $|u_L{}^*|$ is the reference value of the amplitude of the line voltage.

It should be noted that implementing the control in the dq-frame has the disadvantage that the measured ac voltages and currents have to be transformed from phase quantities to dq quantities through a phase-locked loop (PLL) which synchronizes the converter control with the line voltage (usually the ac bus voltage is used). The behavior of the design of PLL will determine the performance of the control system.

Chapter 5

VSC-HVDC between two grids and to isolated loads

5.1 Introduction

To analyze the designed control system, the system shown in Figure 5.1 is simulated and the control system is implemented using the electromagnetic transient simulation program PSCAD/EMTDC[30]. Simulation results are presented in this chapter. The study is focused on the performance of the VSC-HVDC at steady state, load changes and disturbances in supplying network and supplying the passive loads.

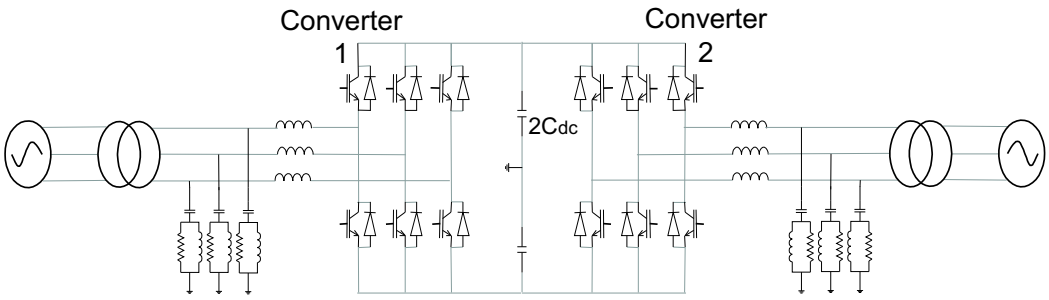


Figure 5.1: The studied system

As shown in Figure 5.1, all simulations have been performed with two two-level converters. The converter bridge valves are represented as a turn-off IGBT and an anti-parallel diode with ideal switches in PSCAD/EMTDC models. State losses and switching losses are neglected. The ac system voltages at both sides are 33kV and 150kV, respectively. The rated dc voltage is 160kV, the set reference value of the dc voltage is 160kV, the rated power flow is 60MW, the reactors are 0.15p.u., the switch frequency used in the VSC is 2000Hz, the fundamental frequency of the ac systems is 50Hz. Two dc capacitors ($2C_{dc} = 37.6\mu F$) corresponding to the time constant of 4ms are used on the dc side of the converter.

As stated in chapter 4, the outer control loop implemented will depend on the application. If the load is an established ac system, then the VSC-HVDC can control ac voltage, reactive power and active power flow. Here, Two different control strategies

are implemented to evaluate their performances:

Strategy 1:

converter 1 controls dc voltage and ac voltage.

converter 2 controls the active power and ac voltage

Strategy 2:

converter 1 controls dc voltage and reactive power.

converter 2 controls the active power and reactive power.

On the other hand, if the load is a passive system, then VSC-HVDC can control frequency and ac voltage. Here, the same control scheme is used, that is, the dc voltage controller and the ac voltage controller are used at converter 1, and the frequency controller and ac voltage controller are used at converter 2, when isolated loads are connected at the converter 2 side.

5.2 Dc link control between two grids by using strategy 1

5.2.1 Steady state

Figure 5.2 illustrates the voltages and currents from the transformer secondary sides and the dc voltage under steady state operation conditions. It can be seen that high quality balanced three phase ac voltages and currents are obtained at both sides. The dc voltage is a constant equal to the set reference value. In fact dc voltage includes $\pm 0.5\%$ ripple at steady state due to the use of small capacitors on the dc side. The reference voltages and the carrier waves at both sides are also illustrated.

The high-frequency ripple on the ac voltages is due to the switching of the converter valves. This ripple is relatively high in the simulation for two reasons:

- the harmonic filters on grid-side of the converter reactors have not been optimized.
- the supplying grid was modelled in insufficient detail to get a correct response for the harmonic frequencies involved. Both capacitance and resistance of the system have not been included, leading most likely to an overestimation of the voltage distortion. Especially the various contributions to the damping are hard to model correctly[31].

The limitation and correct modelling of harmonic distortion due to voltage-source converters are beyond the scope of this thesis.

5.2.2 Ac voltage controller

In order to test the operation of the VSC-HVDC as an ac voltage controller, a test case has been studied. The setting of the ac voltage controller for converter 2 is

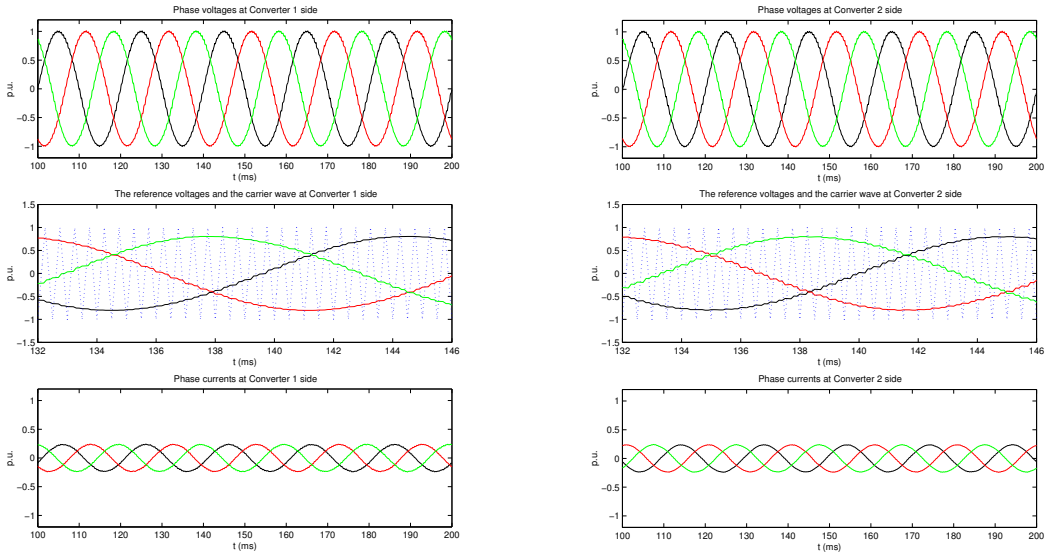


Figure 5.2: Voltages and currents under steady-state operating condition.

instantaneously increased from 0.95 p.u. to 1.05 p.u.. The set active power flow is 0.3 p.u., which is transmitted from converter 1 to converter 2 and is not changed when the step is applied. The results are shown in Figure 5.3. It can be seen that a step of the ac voltage reference value causes a change of VSC-HVDC operating point from reactive power absorption to generation.

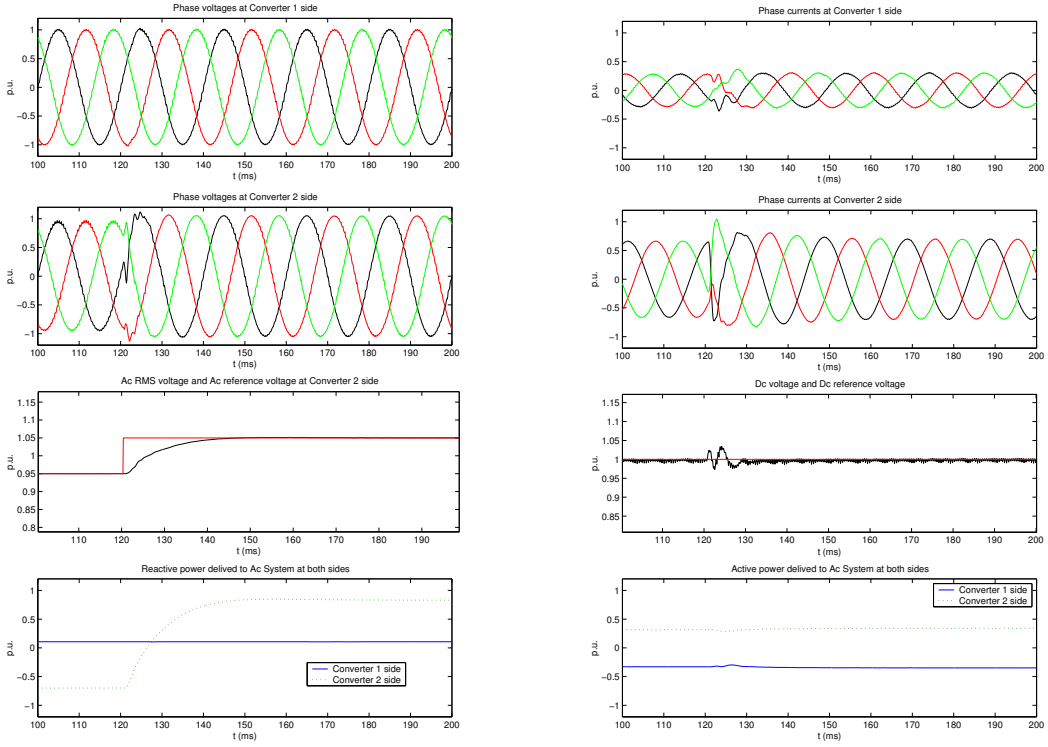


Figure 5.3: Step change of the ac voltage at the converter 2 side.

Here, the ac value is measured by (5.1) and a smoothing function which is $1/(1+sT')$

to eliminate noise, the time constant T' is selected as 0.01s.

$$u_L = \sqrt{u_{L\alpha}^2 + u_{L\beta}^2} \tag{5.1}$$

The active and reactive power are measured by (5.2) and a smoothing function to eliminate noise.

$$P = u_{La}i_{La} + u_{Lb}i_{Lb} + u_{Lc}i_{Lc} \tag{5.2}$$

$$Q = \frac{1}{\sqrt{3}}\left[u_{La}(i_{Lc} - i_{Lb}) + u_{Lb}(i_{La} - i_{Lc}) + u_{Lb}(i_{Lb} - i_{La})\right] \tag{5.3}$$

From the simulation results, it can be concluded that when the ac voltage reference at converter 2 is equal to 0.95p.u., the converter 2 operates on the active and reactive power absorption states that absorb active power 0.3 p.u. from the dc link and reactive power 0.7 p.u. from the ac system. As soon as the step change in the reference voltage is applied around 120ms, the ac voltage is increased to the ac voltage reference value 1.05 p.u. after approximately 2 cycles. From the phase voltages at both sides, it can be seen that the step change does not affect the phase voltages at converter 1 side, but affects the phase voltages at converter 2 side at the beginning of the application of the step. The phase currents at converter 2 are displaced by 180 degree after the step change is applied and have an overcurrent duration of about 0.25 cycle. The phase currents at converter 1 have some oscillations. It should be noted that the response of the dc voltage is fast due to using the small capacitors and the dc voltage can be maintained to the set reference value except some variations about 10ms during the step change of the ac voltage. If a more constant dc voltage is required, the size of the capacitors should be increased.

5.2.3 Active power controller

In order to test the operation of the converter as an active power controller, another test case has been studied. The value of the active power can be chosen by setting the reference value of the active converter current directly. The setting of the active power controller for converter 2 is instantaneously changed from +0.3p.u. to -0.3 p.u.. The ac voltage controllers at both sides are to control ac voltage references to 1.0p.u., which are not changed when the step is applied. The results are shown in Figure 5.4.

From the simulation results, it can be seen that the step of the active power setting changes the direction of the transmitted power. When the active power reference at converter 2 is equal to 0.3 p.u., the converter 2 operates in the active power absorption state. As soon as the step change in the reference voltage is applied around 120ms, the active power flow is changed to the active power reference value -0.3 p.u. after approximately 2 cycles. The step change does not affect the phase voltage at converter 1 side, but affects the phase voltages at converter 2 side at the beginning of the application of the step. The phase currents at both sides are affected after the step change is applied. The response of the dc voltage only shows some minor oscillation at the beginning of the step change of active power.

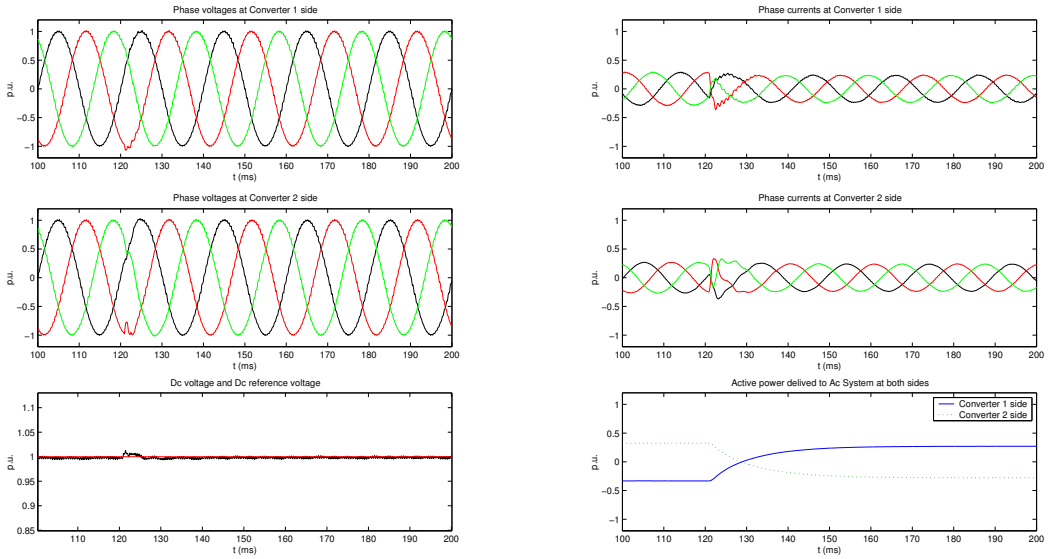


Figure 5.4: Step change of the active power at the converter 2 side.

5.2.4 Fault simulations at the converter 2 side

Short-circuit faults in the grid are likely the most severe disturbance for the VSC-HVDC link. The resulting voltage dips at the converter terminals will severely hamper the ability of the link to transfer power. This may even lead to tripping of the link. In this section the response of the dc link will be studied for different faults in the grid, with emphasis on the following:

- the ability of the dc link to recover from the disturbance.
- the ability of the dc link to maintain the ac voltage at the non-faulted side.

Three-phase-to-ground fault at the converter 2 side

A three-phase-to-ground fault is analyzed to investigate the performance of the VSC-HVDC. Typical simulation results are illustrated by the dc power transfer behavior in Figure 5.5.

A three-phase-to-ground fault is applied at converter 2 at 100ms and is cleared at 5 cycles after the fault, i.e., at 200ms. The set power flow is 0.5 p.u. from the converter 1 to converter 2 and isn't changed during the fault. The ac voltage at converter 1 side, which is controlled to keep its terminal voltage at 1.0 p.u., is maintained to 1.0 p.u. except small oscillations during the fault. The ac voltage at converter 2 side, which is also controlled to 1.0p.u., is decreased to 0.1 p.u. during the fault and recovers fast and successfully to the reference voltage after clearing the fault. The real power flow is reduced to very low value during the fault and recovers to 0.5 p.u. after the fault. The dc voltage, which can be controlled to 1.0 p.u. during the fault, has some oscillations at the beginning of the fault and at clearing the fault, and its maximum transient value is about 1.1 p.u.. So the operation of the VSC-HVDC is as expected. On the other hand, the phase currents at converter 1 side decrease to low values to reduce the power flow. The phase currents at converter 2 side increase from 0.44 p.u. to 0.72p.u., and

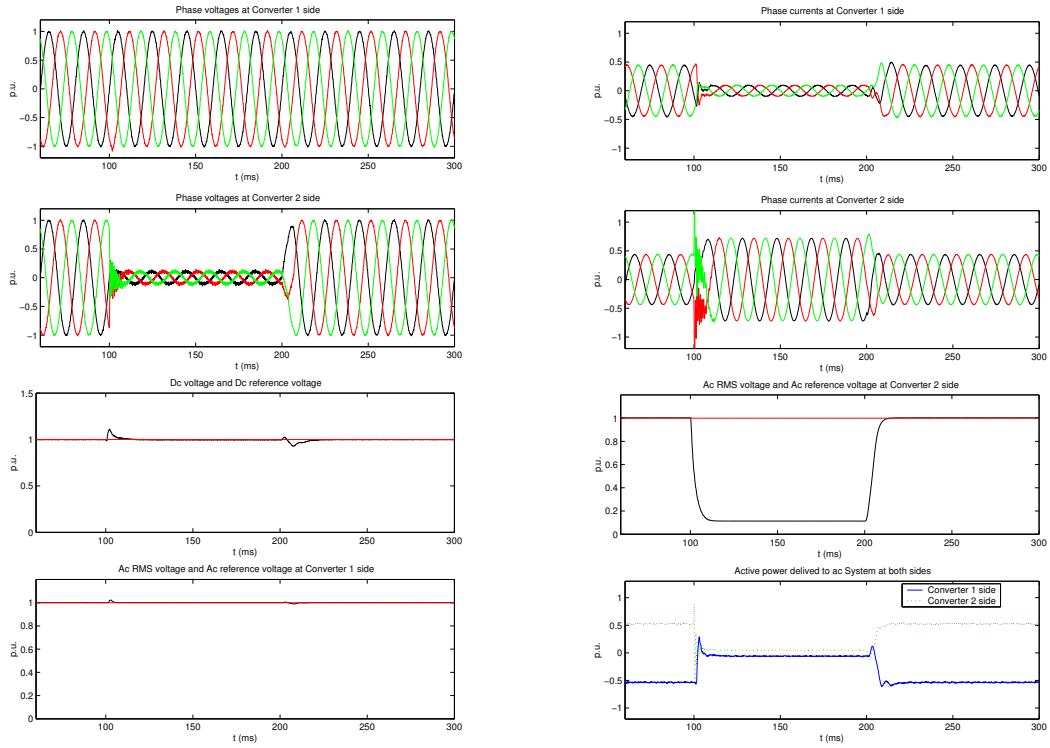


Figure 5.5: Three-phase to ground fault at the converter 2.

have overcurrent transient at the beginning of the fault, which is due to the delay of one fourth cycle during detaching the voltages and currents, shown in Figure 4.2 in chapter 4.

From the simulation, it can be obtained that during a three-phase fault, the decreased voltage at the converter terminals strongly reduces the power flow by the dc link. When the fault is cleared, normal operation is recovered fast. So the severity of three-phase short circuit currents is reduced with an ac interconnection because of the dc link. The voltage dip occurring with an ac interconnection would have a much more severe effect.

5.2.5 Unbalance Faults

The main studies for the VSC-HVDC have so far been concentrated on symmetrical ac network conditions, that is, steady state, step change and three-phase balanced fault. As we know, ac networks are usually affected by unavoidable disturbances or unbalanced faults, for instance, switching of the loads, single-phase fault, phase-to-phase fault, these events may lead to asymmetrical operating conditions. It is therefore necessary to study the responses of VSC-HVDC during asymmetrical conditions, i.e., the supplying ac systems are non-symmetrical.

Single-phase-to-ground fault at the converter 2 side

A single-phase-to-ground fault is simulated in order to investigate the behavior of VSC-HVDC. The initial operating state is that the active current value is set to 0.5p.u.,

which is not changed during the fault. A single phase fault is made in phase A at the receiving side at 100ms, which drops the ac bus voltage on the faulted phase to ground during the time interval 100ms to 200ms. Figure 5.6 presents the simulation results.

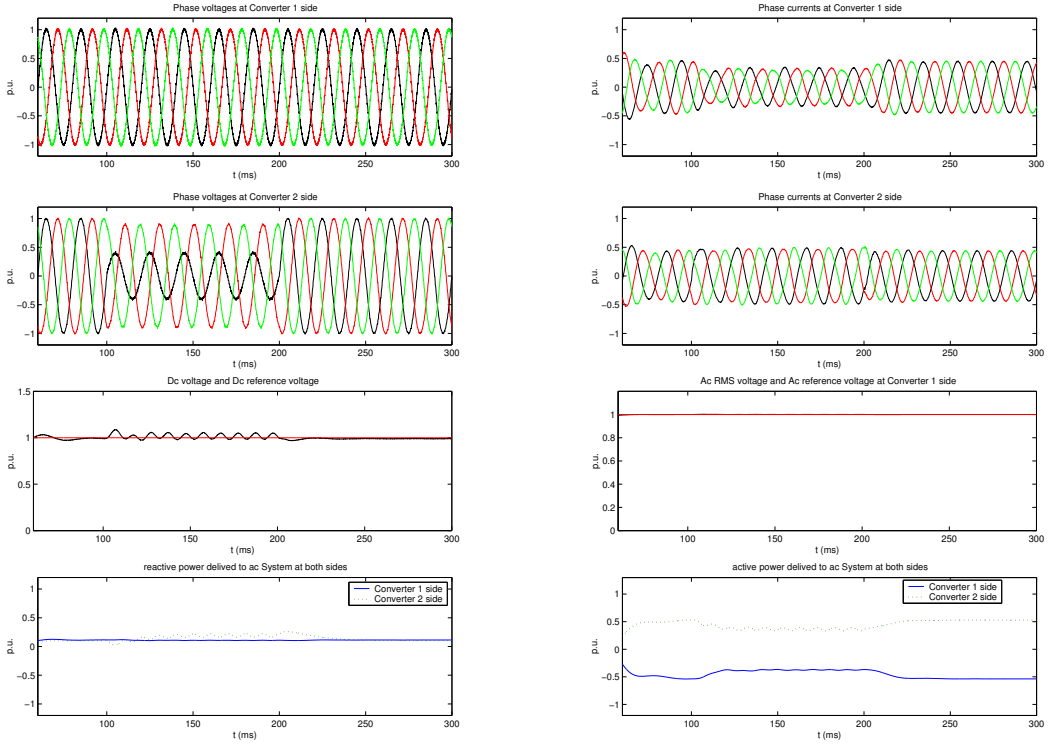


Figure 5.6: Single-phase-to-ground fault at the converter 2 side.

As shown in Figure 5.6, the voltages at converter 1 side are not affected by the unbalanced voltage at the receiving side. The voltage in the faulted phase a at converter 2 side is dropped from 1.0 p.u. to 0.34 p.u. during the fault and the other two phases have very small drops during the fault. This is a normal voltage dip due to a single-phase fault. These voltages are not affected by the dc link. Note that the converter transformer is Y-Y connected but with isolated star point, therefore the voltages at the converter-side of the transformer do not contain any zero-sequence component[4]. The phase currents at converter 1 are affected and include some harmonics. The reason is that the dc voltage contains a second harmonic of the power-system frequency, so the produced positive active current reference includes harmonics. As a result the three phase currents derived contain harmonics. The phase currents in the faulted phase a is increased about 0.05 p.u. from 0.43 p.u. to 0.48 p.u.. in this case. The active power and the reactive power at converter 2 side have a second harmonic component due to the unbalanced fault. The corresponding active power at converter 1 side is reduced during the fault, but the reactive power at converter 1 side does not change. The dc side voltage is well controlled except for the transient caused by the fault.

From the simulation, it can be noted that even the positive current controllers and the negative current controllers (here the negative current reference values are set to zero) are used in the control system of VSC-HVDC, the second harmonic ripple about 7% (from 0.98 p.u. to 1.05 p.u.) on the dc side appears during non-symmetrical conditions, i.e. during unbalanced faults. So a detailed analysis of the origin of the second-harmonic oscillation is given below.

Origin of the Second Harmonic

In the system, the instantaneous apparent power S is given by considering only the fundamental components[32].

$$\begin{aligned} S(t) &= P(t) + jQ(t) \\ &= (e^{j\omega t}v^{dqp} + e^{-j\omega t}v^{dqn})(e^{-j\omega t}i^{dqp^*} + e^{j\omega t}i^{dqn^*}) \end{aligned} \tag{5.4}$$

where i^{dqp^*} and i^{dqn^*} are the complex conjugate of the positive and negative current vectors, respectively.

Thus, the instantaneous real power $P(t)$ is

$$P(t) = P_0 + P_{c2}\cos(2\omega t) + P_{s2}\sin(2\omega t) \tag{5.5}$$

where

$$P_0 = (v_{dp}i_{dp} + v_{qp}i_{qp} + v_{dn}i_{dn} + v_{qn}i_{qn}) \tag{5.6}$$
$$P_{c2} = (v_{dp}i_{dn} + v_{qp}i_{qn} + v_{dn}i_{dp} + v_{qn}i_{qp}) \tag{5.7}$$
$$P_{s2} = (v_{qn}i_{dp} - v_{dn}i_{qp} - v_{qp}i_{dn} + v_{dp}i_{qn}) \tag{5.8}$$

When the control strategy as introduced in chapter 4 is applied, the negative converter current reference values are set to zero. So (5.9) and (5.10) are obtained as follows,

$$P_{c2} = (v_{dn}i_{dp} + v_{qn}i_{qp}) \tag{5.9}$$
$$P_{s2} = (v_{qn}i_{dp} - v_{dn}i_{qp}) \tag{5.10}$$

The presence of the coefficients P_{c2}, P_{s2} is caused by the voltage unbalance. Therefore, if $P(t)$ varies with time due to P_{c2} and P_{s2} not being equal to zero, the dc link voltage fluctuates, i.e. 100Hz ripple appears.

Phase-to-phase fault at the converter 2 side

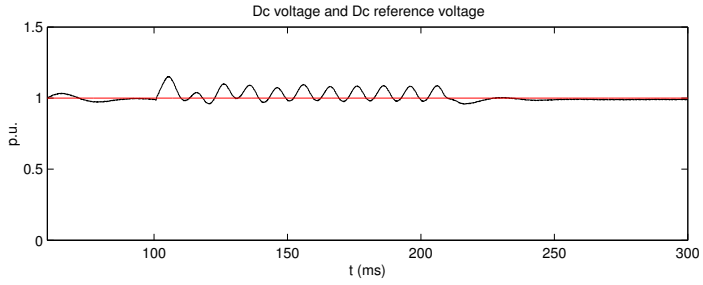


Figure 5.7: Dc voltage under a phase-to-phase fault at converter 2 side.

A phase-to-phase fault is simulated between phases a and b at the receiving side ac network at 100ms. The VSC-HVDC line is the same as in former cases. Figure 5.8 and Figure 5.7 presents the simulation results.

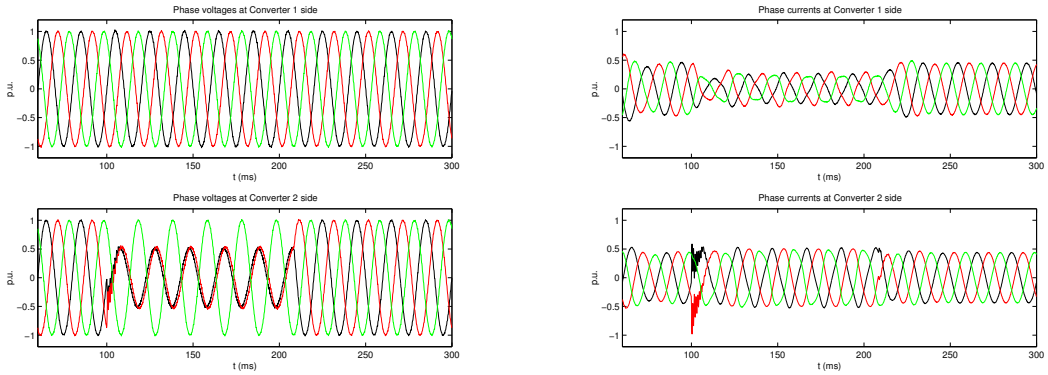


Figure 5.8: Phase-to-phase fault at converter 2 side.

From the phase voltages at converter 2 side it is observed that the voltage in phase c is not affected by the fault while the voltages in phase a and b are reduced. Like the results of the previous three-phase-to-ground fault case, the higher current peak only appears at the beginning of the fault. The dc voltage ripple appears during the fault, the ripple is about 10% from 0.98 p.u. to 1.08 p.u., which is bigger than the dc ripple produced by the single-phase-to-ground fault. The phase currents at converter 1 include some harmonics which are larger than the harmonics in the phase currents due to the single-phase-to-ground fault.

Phase-to-phase to ground fault at the converter 2 side

Another case is simulated when phases a and b are grounded at the receiving ac network at 100ms. The VSC-HVDC line is again the same as in former cases. Figure 5.9 and Figure 5.10 present the simulation results.

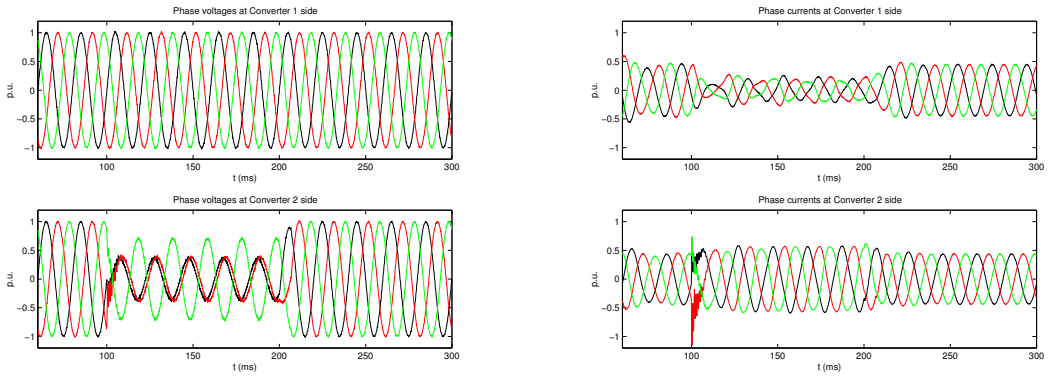


Figure 5.9: Phase-to-phase-to-ground fault at the converter 2 side.

The phase voltages at the receiving side are reduced in magnitude. Like the results of the previous cases, the higher current peak only appears at the beginning of the fault.

Overall, the reaction of the dc link to a phase-to-phase-to-ground fault is similar to the reaction to a phase-to-phase fault without ground. On ac side the voltage in the non-faulted phase also drops leading to a larger drop in dc link voltage but a smaller second-harmonic ripple.

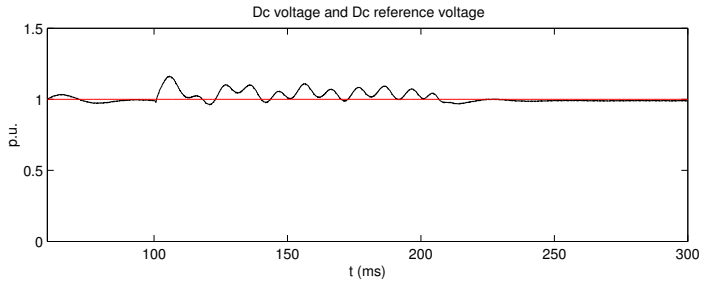


Figure 5.10: Dc voltage under a phase-to-phase-to-ground fault at converter 2 side.

5.2.6 Three-phase-to-ground fault at the converter 1 side

A three-phase-to-ground fault in the sending ac network is simulated to analyze the performance of the VSC-HVDC. The active power flow from the converter 1 to converter 2 is set to 0.5p.u.. The simulation results are illustrated in Figure 5.11.

In Figure 5.11 the simulation results are shown for three changes:

- at t=100ms the three-phase-to-ground fault occurs at the converter 1 side and the active power order at the converter 2 side is kept to 0.5p.u.. It can be observed that the three phase voltages at the converter 1 side are reduced from 1.0p.u. to 0.5p.u. and the dc voltage can not be maintained to the set value 1.0 p.u., but is reduced to 0.9 p.u..

- at t=180ms the active power setting of converter 2 is changed from 0.5 p.u. to 0.1 p.u., and the fault still exists. It can be observed that the dc voltage is increased from 0.9 p.u. to 0.97 p.u..

- at t=250ms the fault is cleared. It can be seen that the dc voltage recovers to the set reference value and the converter 1 can also recover to the pre-fault status.

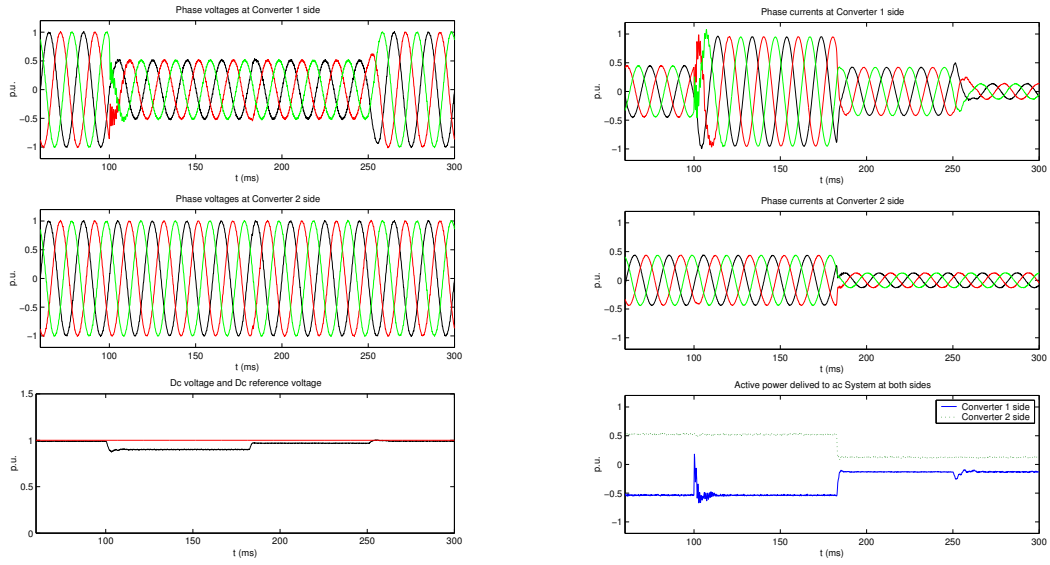


Figure 5.11: Three-phase-to-ground fault at the converter 1 side.

Some current transients are also seen in Figure 5.11. For this fault it should be noted that the overcurrents occur at the converter 1 side when the fault occurs.

5.2.7 Phase-to-phase fault at the converter 1 side

A phase-to-phase fault is simulated at the ac system at the converter 1 side in order to investigate the behavior of VSC-HVDC . The initial operating state is set to the active current values to 0.5p.u., which is kept constant during the fault. A phase-to-phase fault occurs in phase a and b at the sending side at 130ms, which drops the faulted phase voltages during the time interval 130ms to 230ms. Figure 5.12 and Figure 5.13 presents the simulation results.

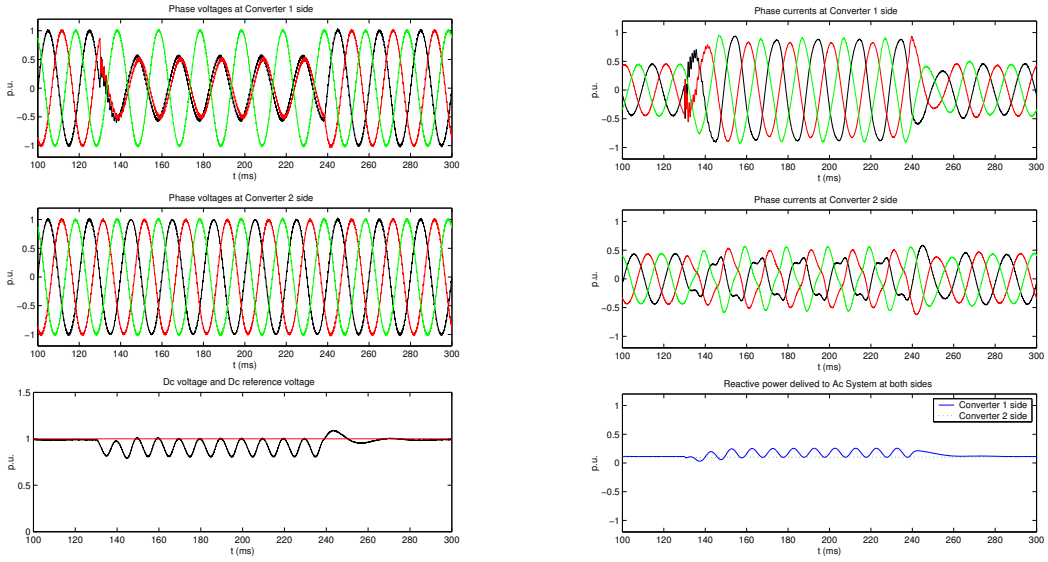


Figure 5.12: Phase-to-phase fault at the converter 1 side.

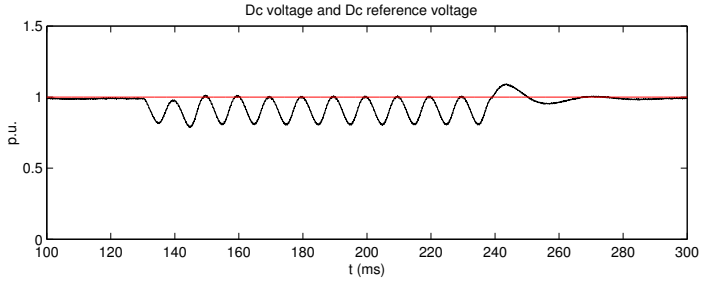


Figure 5.13: Dc voltage under phase-to-phase fault at the converter 1 side.

The phase voltages at converter 1 side are unbalanced, where two phase voltages drop from 1.0 p.u. to about 0.6 p.u.. The third phase is not affected by the fault. The phase voltages at converter 2 side are not affected by this fault which occurs at the sending side. The phase currents at converter 1 increase due to the fault, the phase currents at converter 2 are affected too much and include some harmonics. The dc side voltage has big oscillation during the fault due to the second harmonic ripple, whose value is between about 0.8 p.u. and 1.0p.u.. The dc voltage ripple in this case is bigger than the dc voltage ripple produced by phase-to-phase fault at the receiving side.

If we compare this case's results with the results of a previous case which has same type of fault at the receiving side, shown in Figure 5.7, it can be noted that the dc voltage in this case is reduced due to the constant active power reference at the receiving side.

5.3 Dc link between two grids by using strategy 2

5.3.1 power flow controller

In order to investigate the operation of the VSC-HVDC as active and reactive power flow controllers, two test cases have been studied. The reference values of the active and reactive power can be chosen by giving the reference values of the active and reactive converter current directly, which are described in chapter 4.

The first case, the VSC-HVDC operates at steady-state with active and reactive current reference values at converter 2 side set to +0.5 p.u. and +0.5 p.u., respectively. In Figure 5.14 and Figure 5.15 the simulation results are shown for three changes in power setting:

- at t=80ms the reactive current setting of converter 2 is changed from +0.5 p.u. to -0.5 p.u..
- at t=140ms the reactive current setting of converter 2 is changed from -0.5 p.u. to -0.3 p.u..
- at t=170ms the reactive current setting of converter 1 is changed from +0.4 p.u. to -0.5 p.u..

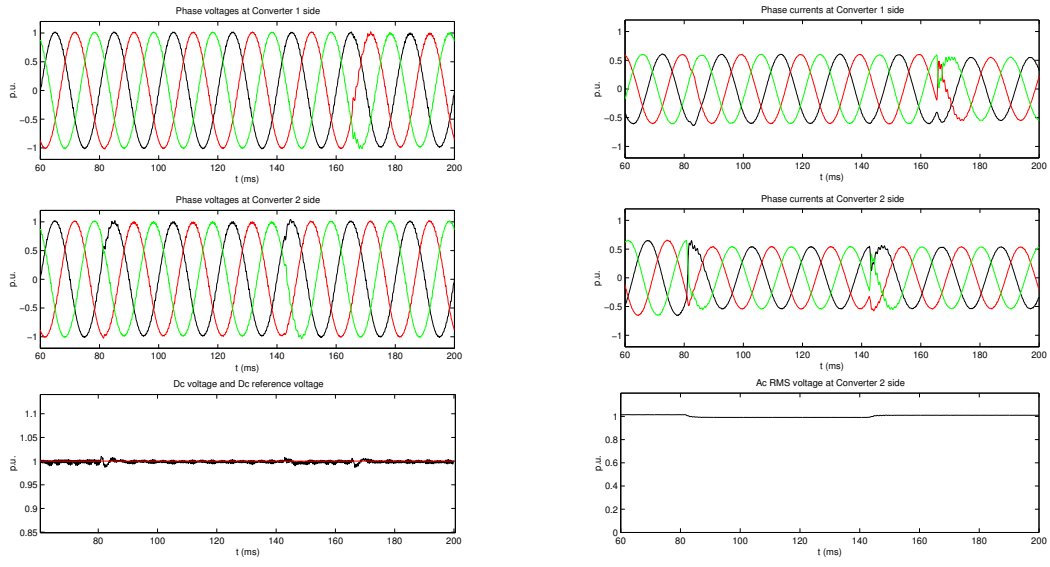


Figure 5.14: Step changes of reactive current at both sides at Strategy 2.

The measured reactive current at converter 2 side follows the setting in about 10ms, while the active power is scarcely affected. The reactive power reacts almost instantaneously to the change in setting. But it should be noted that there is a slight voltage

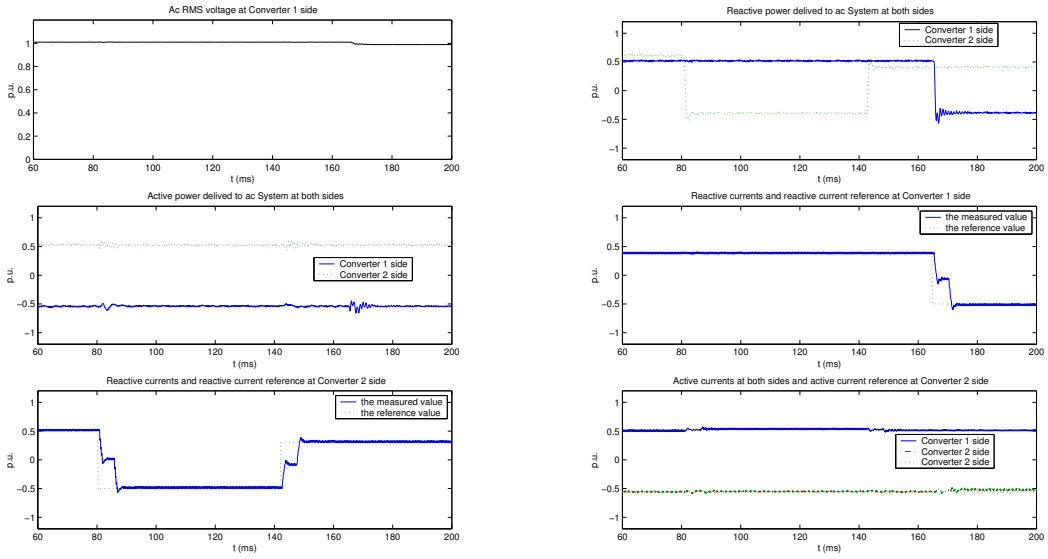


Figure 5.15: Step changes of reactive current at both sides at Strategy 2.

drop at the converter 2 side when the reactive current is changed at the converter 2 side. The fast change of the converter operating voltage causes a small transient on the dc voltage and a very small transient on the ac network via the converter 1. These disturbances affect the active power flow at the converter 1 side, although the deviations in the measured active power are still small. The same phenomenon can be observed at the converter 1 side when the reactive current step is applied at the converter 1 side. The behavior of the line currents at both sides are rapid, and the phase currents change 180 degrees.

From the above simulation cases, it can be concluded that converter 1 and converter 2 can control their reactive power independently.

The Second case, two step changes equal to -0.5 p.u. and 0.4 p.u. are applied to the active converter current at converter 2 side at 100ms and 150ms. The simulation results are shown in Figure 5.16. From the simulation results, it can be observed that the active current reaches the new value after half cycle. On the other hand, the fast change of the active current causes a transient on the dc side voltage, whose transient is bigger than the transient in Figure 5.14 and Figure 5.15, but finally the dc voltage reaches the set operating point. The reactive power flow at the converter 2 side is transiently changed. The active power at the converter 1 side has a large overshoot, in fact a higher transient dc voltage is also verified in this interval. Also the phase currents show an overshoot. It should be also noted that there are minor voltage variations at both sides when step changes are applied. These voltage changes on ac side are however not of any concern.

Both cases show a delay of about 5ms between the measured currents and reference currents. This is due to the delay of one quarter cycle in order to separate the positive and negative components of the voltages and currents at both sides, which is described in chapter 4. The much faster reaction in measured active and reactive power is due to the fact that the controlled reference voltages are changed to compensate this delay of currents during the delay time.

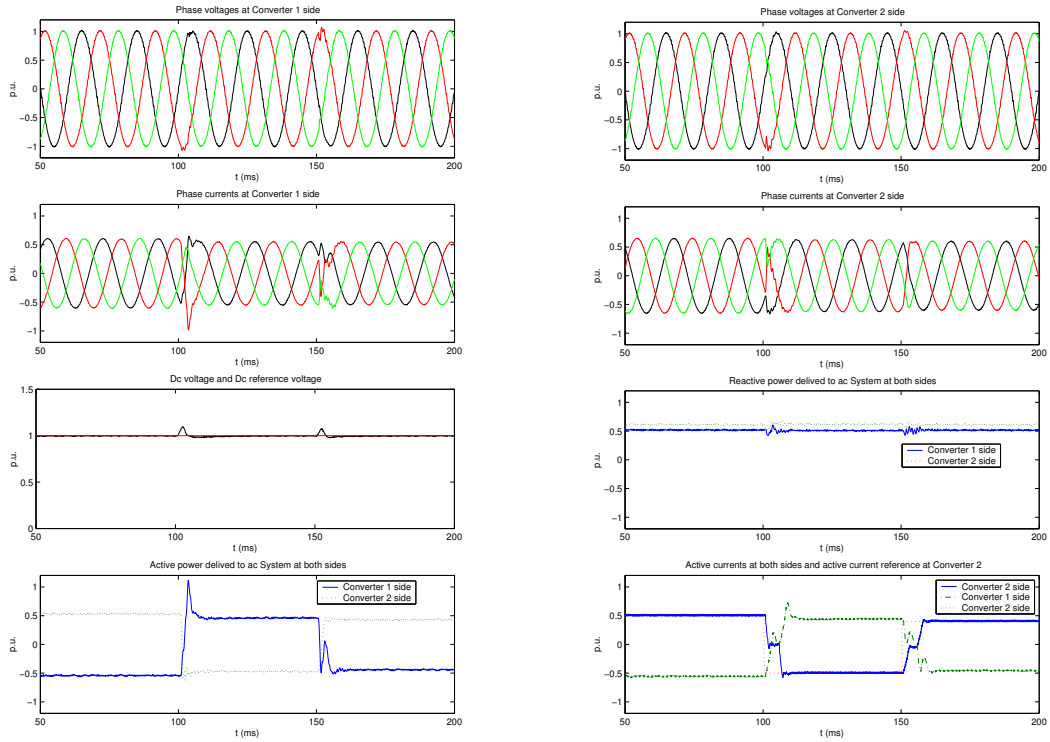


Figure 5.16: Step changes of active current at both sides at Strategy 2.

5.4 Dc link supplies to isolated loads

5.4.1 Steady state

As described before, the VSC-HVDC can supply isolated loads. In order to test this advantage of the VSC-HVDC, a test system, where the passive loads are connected to converter 2, has been simulated. The simulated system is shown in Figure 5.17

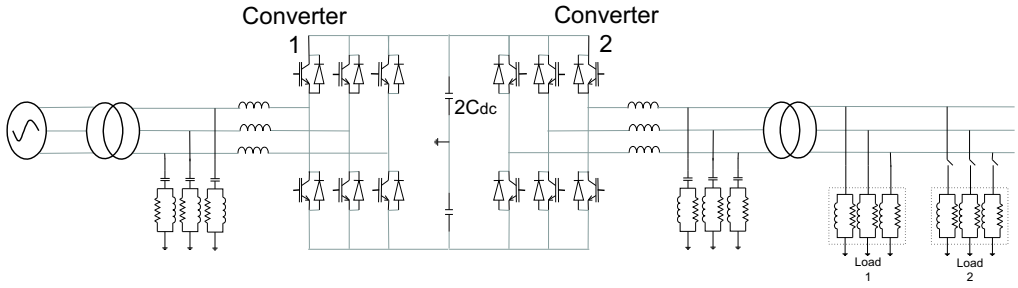


Figure 5.17: VSC-HVDC supplies to isolated loads

The converter 2 controls the frequency and the ac bus voltage and consequently operates as a generator with the active power fed from the dc link. In this case, the simple load models (resistors and inductors) are used. As shown in Figure 5.17, the reference voltage at converter 1 side is controlled to 1.0 p.u., while the dc reference voltage is set to 1.0p.u.. The reference voltage at converter 2 side is also controlled to 1.0p.u. and the frequency is controlled to 50Hz; the load 1 is 15MW and 30MVar; the load 2 is 10MW and 10MVar. The breaker is open. The simulation results are

presented in Figure 5.18 and Figure 5.19. From the simulation results, it can be seen that at steady-state the ac voltages are kept to the set reference values (1.0 p.u.) at both converters, and the dc voltage is also kept to the set reference value.

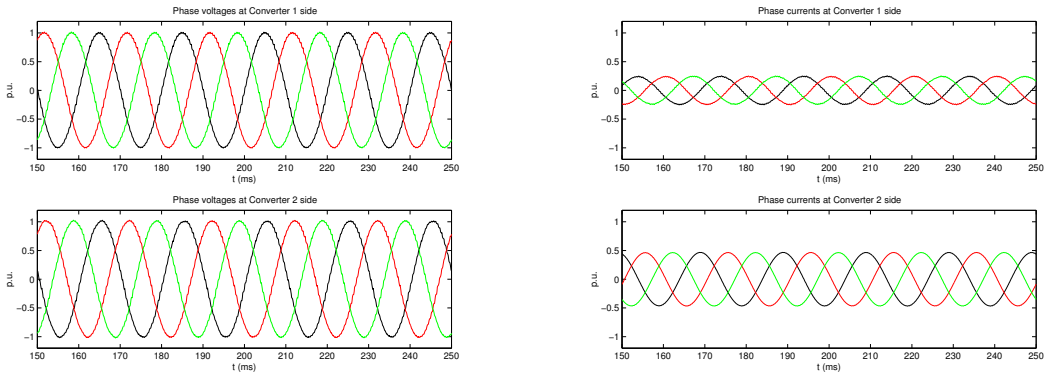


Figure 5.18: Dc link supplying passive loads at steady state.

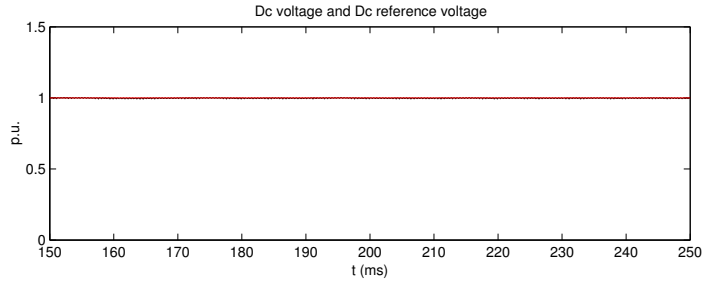


Figure 5.19: Dc voltage of dc link supplying passive loads at steady state.

5.4.2 Variable passive Loads Results

In order to investigate the dc link performance to variable passive loads, another test case is simulated. The load 1 is changed to 15MW and 20MVar, the load 2 is switched on at 200ms and switched off at 370ms. The simulation results for this case are shown in Figure 5.20. It can be observed that the voltage at converter 2 side is maintained at 1.0p.u. except some transient. The total power transmitted to loads is 15MW and 20MVar before 200ms and 25MW and 30MVar between 200ms and 370ms. The dc voltage is kept to 1.0p.u. except the small variation when the load 2 is turned on and turned off. Now, we analyze the system transients when the load 2 is on and off. When load 2 is connected, it causes a transient ac voltage drop at converter 2 side. It is also observed that when the ac voltage at converter 2 is transiently decreased, the dc voltage is also transiently decreased.

The results show the VSC-HVDC performance is adequate in transmitting the power flow as well as keeping the sending and receiving end voltages at the ordered magnitudes.

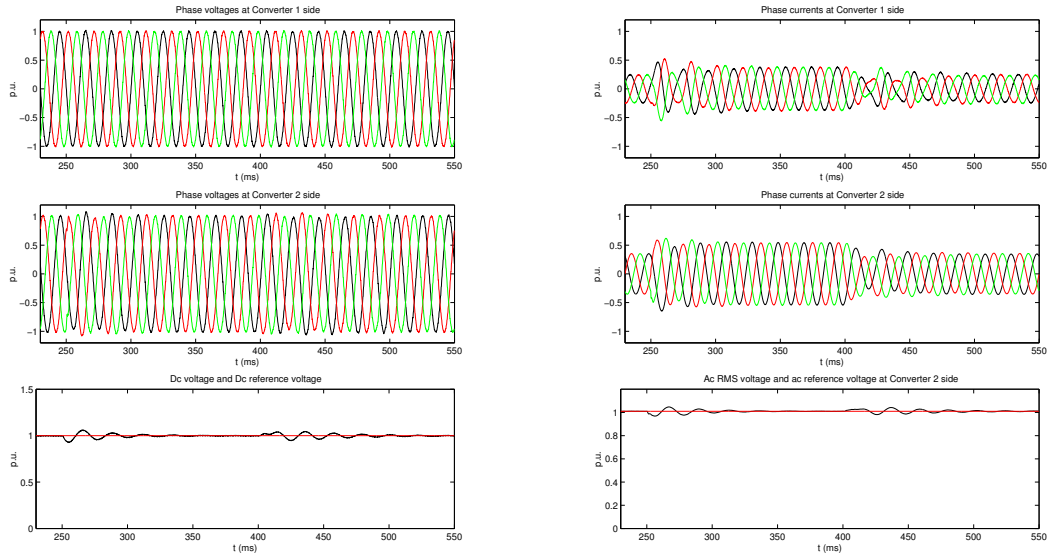


Figure 5.20: Dc link supplying passive loads at varied loads state.

5.5 summary

This chapter presents PSCAD/EMTDC implementation of the VSC-HVDC. As described before, the VSC-HVDC control strategies can be varied regarding different objectives. Some of the most significant control schemes are simulated in detail here.

From the simulation results, it is verified that

- VSC-HVDC can control both active and reactive power independently and bi-directional. While the transmitted active power is kept constant the reactive power controller can automatically control the voltages at the ac network or can continue to operate as SVC and control the required reactive power flow, so power quality is enhanced. But it should be noted that it is necessary to use dc voltage controller to balance between the ac side and dc side active powers.

- Due to the use of the PWM the high quality ac voltages and ac currents can be obtained from the transformer secondary sides, and the harmonics caused by disturbances in the power system are reduced.

- The control system can either reduce or eliminate the power flow by the dc link when the ac faults occur, and can resume normal operation as soon as possible after the fault is cleared.

- These control schemes in some cases can eliminate the overcurrent during unbalanced ac network faults except for very short overcurrent when the fault occurs.

Chapter 6

Passive industrial system

6.1 Introduction

In the previous chapters a control algorithm has been developed for a VSC-HVDC link. In this chapter such a link will be investigated for its ability to supply a passive industrial system. A hypothetical system has been chosen as an example. This system will be supplied in two different ways: through two 150kV lines; through a $\pm 80kV$ VSC-HVDC link.

6.2 A passive industrial system.

The difference between a pure industrial ac system and a dc link supplied industrial system has been investigated, a comparison between an ac grid supplying a passive industrial system and a dc link supplying the same industrial system is done. The investigations in each case study are carried out for single-phase-to-ground fault, two-phase-to-ground fault, two-phase fault, three-phase fault. In each case the effect of fault duration and fault recovery on the system are studied. The investigations are chiefly concerned with the quality of supply within the industrial distribution system itself and so the studies are concerned only with that section of the network between the point of connection to the main utility and the load. An important aspect of industrial distribution system analysis is the reaction of the main loads to disturbances. The system is used for fault investigations and the study of fault propagations throughout a network.

The two systems shown in Figure 6.1 and Figure 6.2 are simulated in PSCAD/EMTDC. A fictitious passive industrial distribution system is used as the system model. This system contains different types of loads and is feed from the public supply. For example, this system includes a synchronous machine, three different induction motors, an ac drive which is shown in Figure 6.3, a dc drive and some smaller loads (for instance, heating, lighting, computers). In the simulation, simplified models (only resistor and inductor) are used for the smaller loads. At this stage of the study, the aim is not to create a feasible design for an industrial distribution network, but to study the effect of disturbances on different types of loads and fault propagation. Here the different

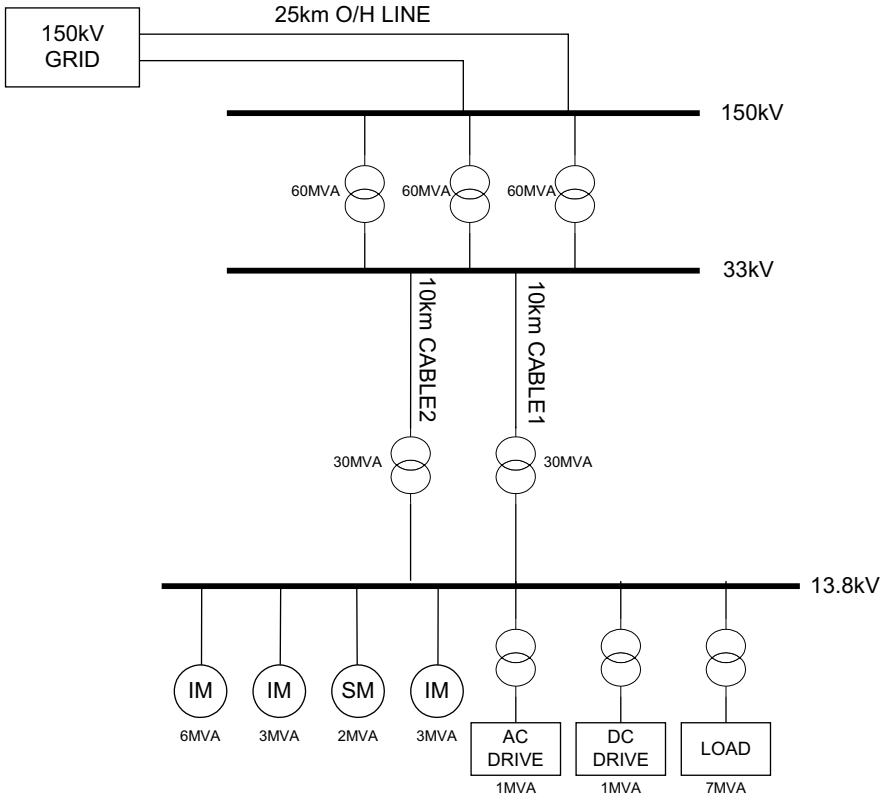


Figure 6.1: A pure ac industrial system

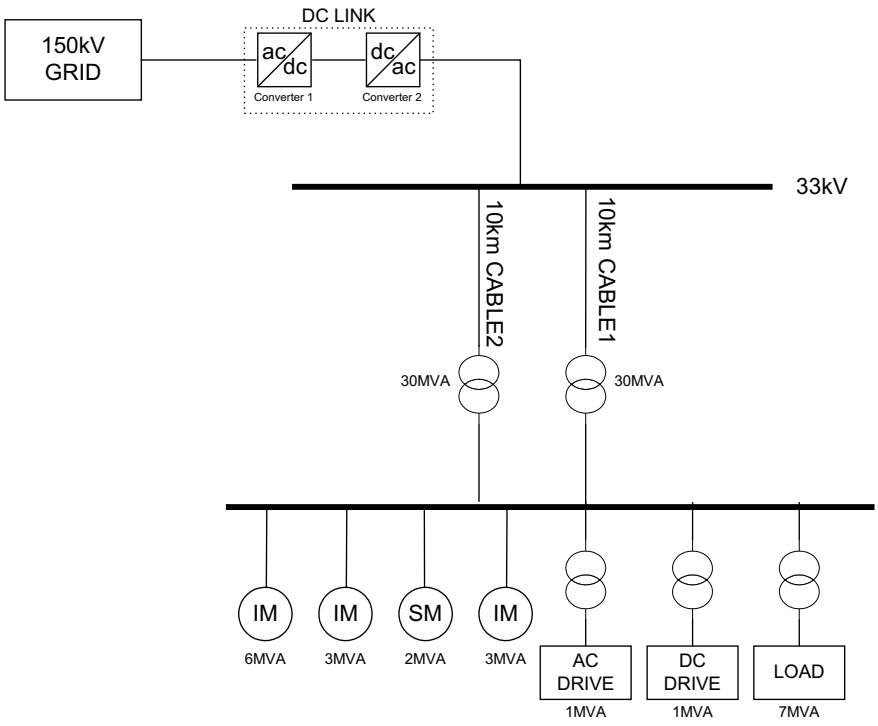


Figure 6.2: A dc link supplied ac industrial system

types of machines and drives are connected to the same 13.8kV bus, the total rating is 23MVA.

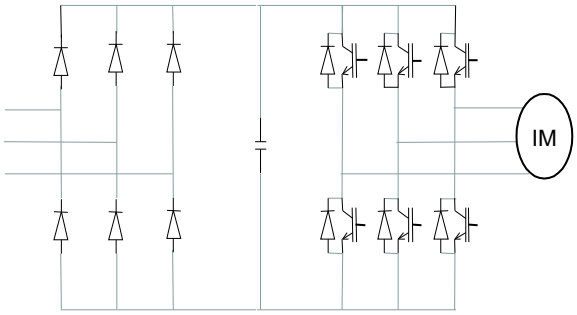


Figure 6.3: A typical ac drive

6.3 Simulations

Different cases are simulated and compared according to Figure 6.1 and Figure 6.2. In all simulations, the fault duration is 0.2s, which is sufficient to show the response of the system components. Voltage waveforms and rms voltages are obtained at 33kV and 13.8kV load buses. The total currents have been obtained for 150kV side and 33kV side of the ac or dc connection.

6.3.1 Upstream fault

Balanced (three phase fault) and unbalanced faults (two-phase-to-ground fault, two-phase fault, single-phase-to-ground fault) are simulated in the 150kV grid.

Balanced fault

A voltage dip with 50% retained voltage at the 150kV bus is created by simulating a three-phase fault behind a reactance connected to the 150kV bus. The size of the reactance is chosen such that the remaining voltage at the 150kV terminals of the link is equal to 50% of the pre-fault voltage. The resulting voltage waveforms and rms voltages are shown in Figure 6.4 for the pure ac system.

Some oscillations at 150kV voltage occur at the beginning of the fault. These oscillations are due to the resonance between the capacitance of the 150kV lines and the inductance to the fault. The presence of this oscillation is realistic but its frequency and damping are not, because the capacitance and damping of the 150kV network have not been modelled in sufficient detail.

The voltage dips at 33kV and 13.8kV buses are about 50% at an ac supplied system. It should be said that the voltages at 33kV and 13.8kV buses slowly decay actually because the induction machines take an increasing current during the fault.

The currents before, during and after the three-phase-to-ground fault are shown in Figure 6.5. As the fault occurs upstream, the during-fault currents do not show any

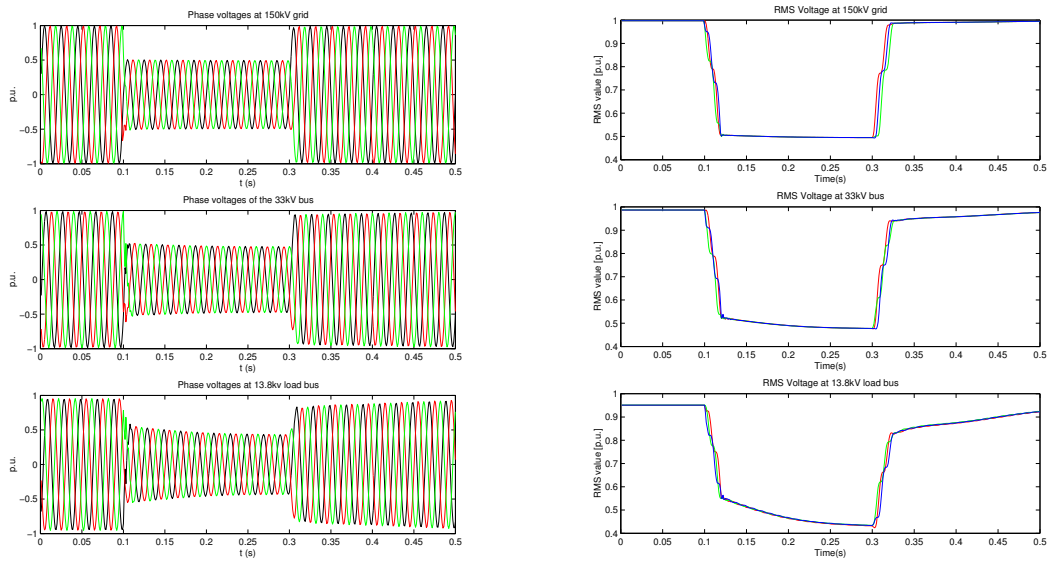


Figure 6.4: Voltage of ac supplied system under three-phase-to-ground fault at 150kV grid.

significant increase. However the voltage recovery upon fault clearing causes a post-fault inrush current. When the fault is cleared, the three phase currents in the grid side go up to about 0.6kA (6 times the normal currents) which is due to the transformer connection. The currents in the 33kV side go up to about 1.5kA (3 times the normal currents). This is due to the extra current taken by the motor load.

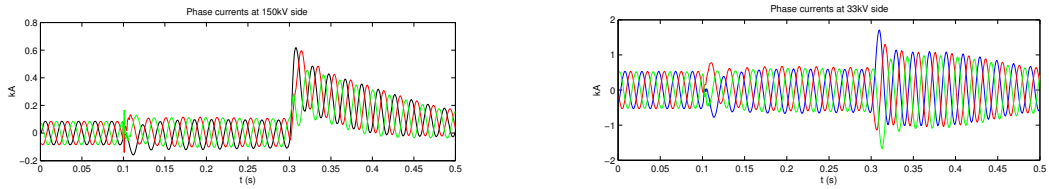


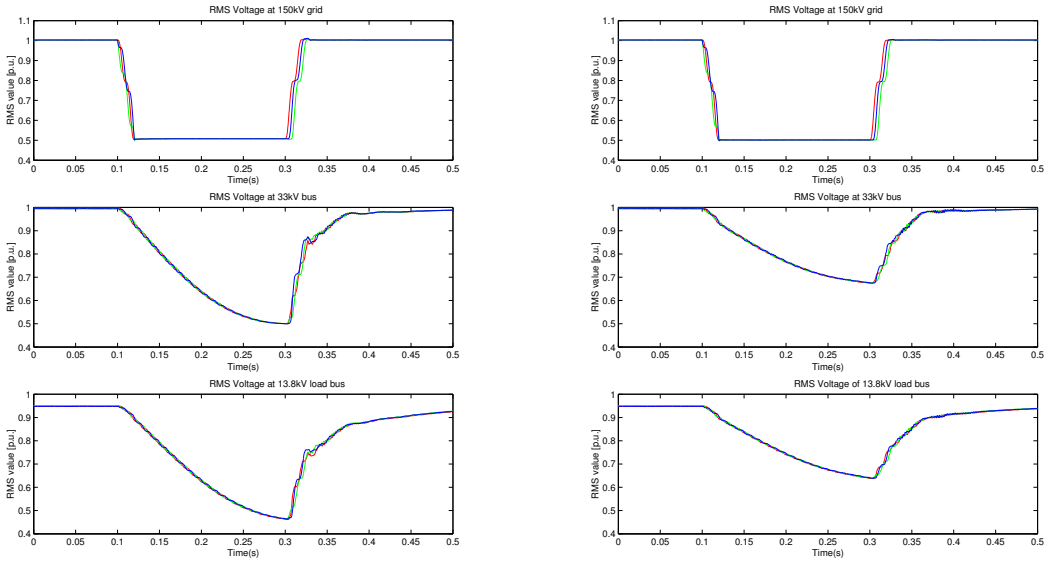
Figure 6.5: Current of ac supplied system under three-phase-to-ground fault at 150kV grid.

Next the same fault is applied for a system with a dc connection. The rating of the dc link, i.e. the setting of the current limitation, has been chosen equal to the total load: 23MVA. The controller has two options:

- First: the controller tries to maintain the ac voltage at 150kV grid;
- Second: the controller tries to keep up the dc voltage.

Both options are simulated. The resulting voltage waveforms are shown in Figure 6.6 for the same three-phase-to-ground fault as before. The fault duration is taken as 200ms.

The simulation results in Figure 6.6 show that when the voltage dip at 150kV side is 50%, the remaining voltages at 33kV and 13.8kV buses slowly go down to about 50% for maintaining ac voltage and about 65% for keeping up the dc voltage. This means that different control goals have different influence on voltage dips when the current

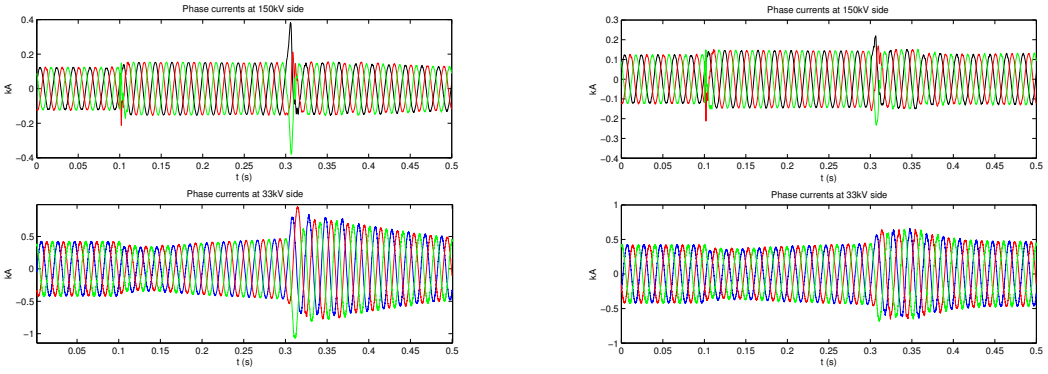


(a) for maintaining ac voltage at 150kV

(b) for keeping up dc voltage

Figure 6.6: Voltage of dc supplied system under three-phase-to-ground fault at 150kV grid.

limitation is considered. The slow decay in rms voltage at the 13.8kV and 33kV buses at both cases is due to a combination of a slow drop of the dc voltage of the dc link and an increasing current of the induction machine during the fault. The effect of current limitation will be discussed in more detail below.



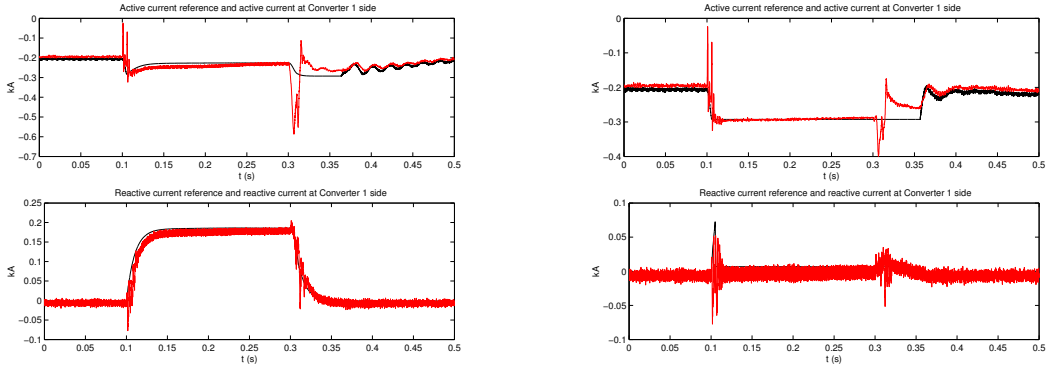
(a) for maintaining ac voltage at 150kV

(b) for keeping up dc voltage

Figure 6.7: Current of dc supplied system under three-phase-to-ground fault at 150kV grid.

The different control goals influence not only voltage dips but also the overcurrents. As shown in Figure 6.7, when the fault occurs and is cleared, the currents at 150kV side reach up to 0.4kA and 0.25kA for two goals respectively. These overcurrents are due to the control system. As shown in Figure 6.8, when the fault is cleared, the reference active currents generated from the dc voltage controller reach the current limits, but

the actual active currents do not follow the reference active currents, the overcurrents occur. The currents in the 33kV side of the link are also increased to about 1.2kA (2.5 times the normal currents) and 0.75kA.



(a) to maintain ac voltage at 150kV

(b) to keep up dc voltage

Figure 6.8: Active and reactive current of dc supplied system under three-phase-to-ground fault at 150kV grid.

The influence of the first option on performances of the system is bigger, therefore all following simulation results are obtained from the first option which is to try to maintain the ac voltage at 150kV grid.

When the rating of dc link is increased from 23MVA to 28MVA, the dc link is able to mitigate the voltage dips, but they are not completely compensated.

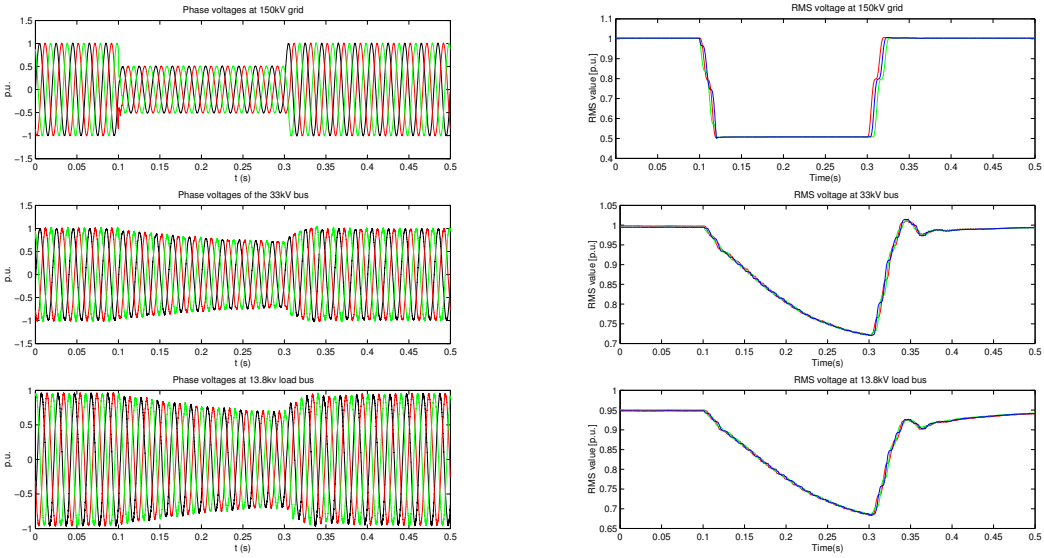


Figure 6.9: Voltage of dc supplied system under three-phase-to-ground fault at 150kV grid, increased rating of dc link.

With the rating of the dc link increasing, the voltage dips at 33kV and 13.8kV buses are decreased to about 28% and 32% (compared to a 50% drop in the other cases). The voltage waveforms are shown in Figure 6.9. Compared with the lower-rating dc link,

the voltage decay is slower and its recovery is faster (see Figure 6.6). The time below 90% of pre-event voltage (a standard measure for voltage-dip duration) is therefore less for the higher-rating dc link.

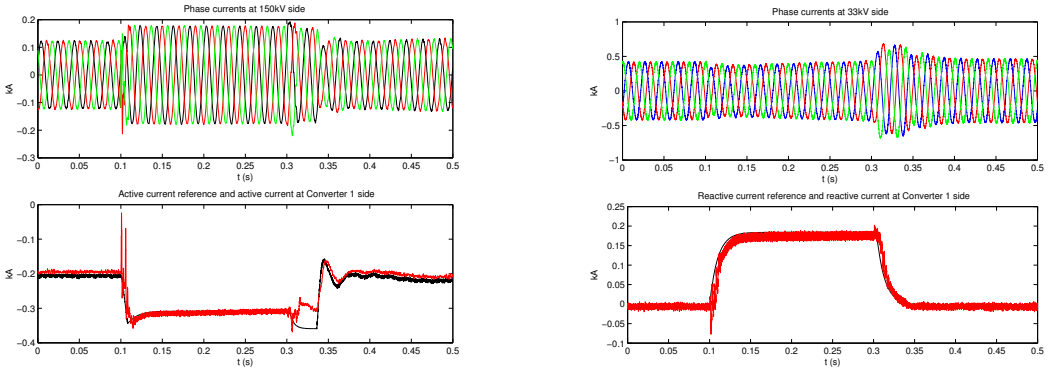


Figure 6.10: Current of dc supplied system under three-phase-to-ground fault at 150kV grid increased rating of dc link.

In Figure 6.10 when the fault occurs and is cleared, the highest currents at the grid side go up to 0.22kA, the currents in the 33kV side are also up to about 0.6kA. It should be noted that the current at the grid side increases even the current limitation is used.

Voltage dips are characterized by the so-called retained voltage, which is defined as the lowest of the rms voltages in the three phases [Draft of IEEE std.1564] [IEC 61000-4-30]. The retained voltages at different buses are shown in Figure 6.11.

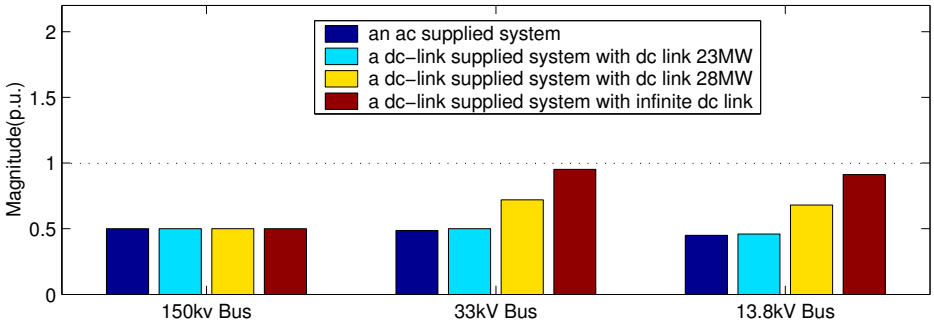


Figure 6.11: Voltage dip of different buses for a three-phase-to-ground fault in the 150kV grid.

It can be seen from Figure 6.11 that if the rating of dc link is same as the load, voltage drop in an ac supplied system is almost same as that in a dc supplied system. On the other hand, if the rating of dc link is increased, the voltage drop is reduced, the dc link can mitigate voltage drop on the load buses. Simulations with a very high rating for the dc link have shown that such a system will only result in very shallow dips.

The second voltage-dip characteristic is the so-called "dip duration". The dip duration is the time during which the rms voltage is less than 90% of the nominal or pre-event voltage. The dip durations for the different supply alternatives are shown in Figure 6.12.

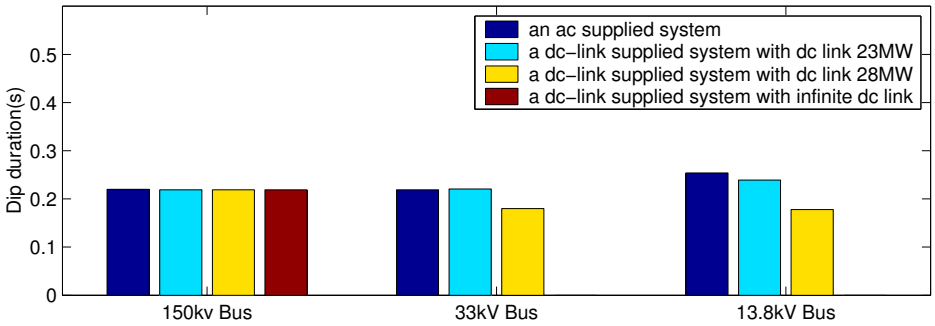


Figure 6.12: Voltage dip duration of different buses for a three-phase-to-ground fault in the 150kV grid.

In Figure 6.12 the voltage dip durations at both systems are almost same when the rating of dc link is same as the load. When the rating of dc link is increased, the voltage dip durations are less than those of ac system. This means that the voltage recovery at load bus in a dc supplied system is faster than that in an ac supplied system. For the dc link supplied system with infinite dc link the rms voltages do not drop below 90% at all, the dip durations are zero according to the definition used here. So the dc link can filter voltage dip to downstream loads.

Unbalanced fault

Unbalanced faults (single-phase-to-ground fault,two-phase-to-ground fault, phase-to-phase fault) close to the 150kV substation are simulated. The simulation results during the single-phase-to-ground and the resulting voltage dip and voltage dip duration characteristics at different buses during three types of faults are shown below.

The simulation results show that voltage dip during unbalanced faults at 33kV and 13.8kV buses are different in both systems.

- In an ac supplied system, voltage dip Type B at 150kV grid has become voltage dip Type C (Two phases down to about 60% and the third phase close to 100%) at 33kV side, a Type D dip (one phase with voltage about 30% is much lower than the other two with voltage about 80%) on the 13.8kV bus[4].

- In a dc-link supplied system, the during-fault voltages are balanced (Type A) at 33kV and at 13.8kV.

Voltage and currents due to a single-phase-to-ground fault at 150kV, for the ac-supplied system, are shown in Figure 6.13 and Figure 6.14, respectively. The voltage waveforms also include the symmetrical components. The zero-sequence voltage at 150kV is removed by the 150/30kV transformers. The positive-sequence voltage shows a slow decay. The negative-sequence voltage is constant during the fault. This is a normal behavior for motor load[33]. Large currents during the fault appear to be in phase in the three phases. These large currents include large zero-sequence components which are due to the existence of zero-sequence voltage during the unbalanced fault, in combination with the winding connection of the 150/30kV transformers (Yn-D connection).

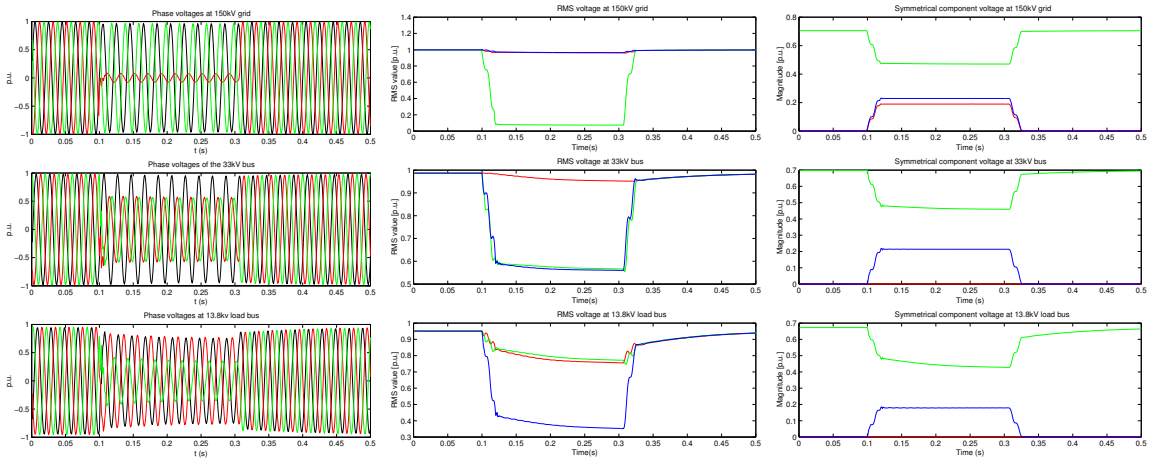


Figure 6.13: Voltage of ac supplied system under single-phase-to-ground fault at 150kV grid.

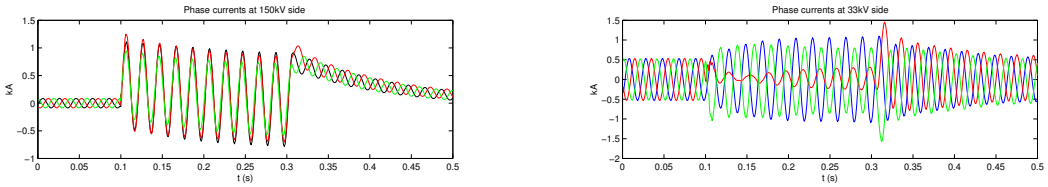


Figure 6.14: Current of ac supplied system under single-phase-to-ground fault at 150kV grid.

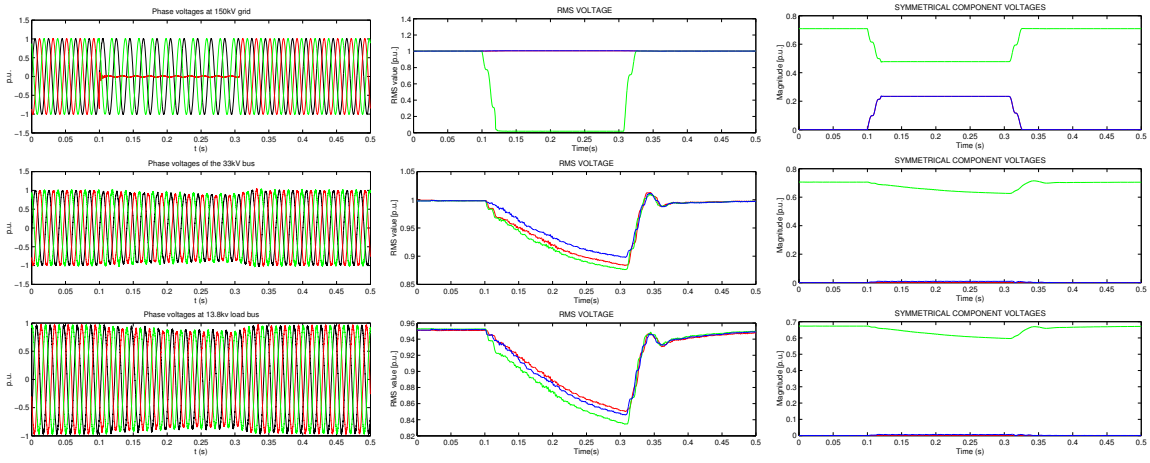


Figure 6.15: Voltage of dc supplied system under single-phase-to-ground fault at 150kV grid.

The results for the dc-link supplied system are shown in Figure 6.15. The voltage dips at 33kV and 13.8kV buses are small in a dc link supplied system during the fault even if the rating of the dc link is set to 23MVA (equal to the load size). The dips are not only more shallow, they are also shorter than in the pure ac system. The latter is again due to the slower decay of the voltage in the dc-link supplied system.

The effect of unbalanced faults at 150kV side on the voltages in the dc supplied system also causes a very small unbalance in the voltages on the 33kV bus and 13.8kV load bus. This means that the unbalanced disturbance is not completely removed by the dc link, but the unbalance is only a few percent, which will not adversely affect any loads.

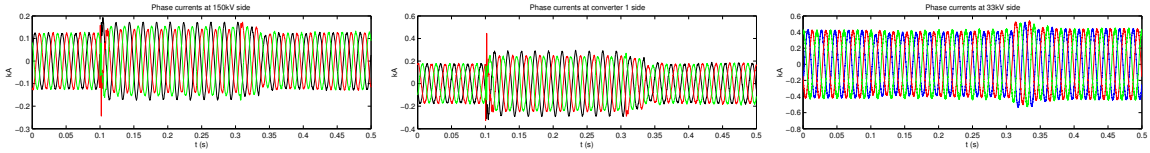


Figure 6.16: Current of dc supplied system under single-phase-to-ground fault at 150kV grid.

During the fault the converter current also exceeds the rated value even if the current limitation is used, especially at the beginning of the fault. For instance, in Figure 6.16 the fault occurs at 0.1s, following the voltage drop, the currents at converter 1 side increase from 0.18kA to 0.28kA to support the bus voltage at the 150kV side. The highest current is up to 0.44kA at the beginning of the fault. This is due to the one fourth cycle delay in the control system which is described in chapter 4.

The resulting voltage dip magnitude and voltage dip duration at different bus due to single-phase-to-ground fault, two-phase-to-ground fault, phase-to-phase fault are illustrated in Figure 6.17, Figure 6.18, and Figure 6.19.

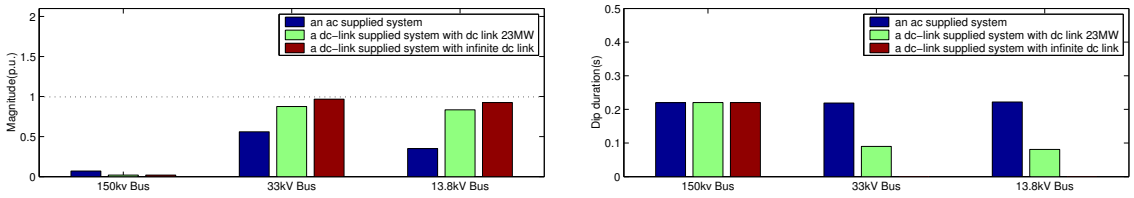


Figure 6.17: Remaining voltage(left) and duration(right) for a single-phase-to-ground fault at 150kV.

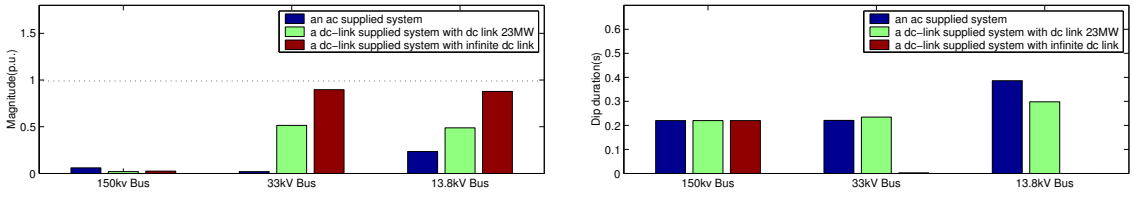


Figure 6.18: Remaining voltage(left) and duration(right) for a two-phase-to-ground fault at 150kV.

Finally, it can be concluded that

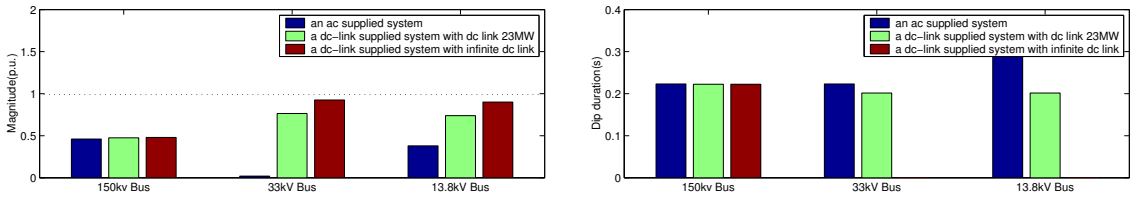


Figure 6.19: Remaining voltage(left) and duration(right) for phase-to-phase fault at 150kV.

- With a dc-link rating equal to the load rating, the voltage dips due to unbalanced faults are already less severe than those of a pure ac system. Increasing the dc-link rating will further mitigate the dips.

- Under balanced faults the dc link can mitigate voltage dip propagation towards downstream loads to some extent. The reduction is also in the duration of the dip. For short-duration faults even the remaining voltage is improved.

- The rating of the dc link has a big influence on the voltage dip propagation when the system has balanced faults. With the rating of the dc link increasing, the extent of mitigating voltage dip is increased. On the other hand, the rating of the dc link has less effects on the voltage dip propagation if the system faults are unbalanced.

- The voltage dip durations during unbalanced faults in the dc-supplied system are reduced to some extent depending on the rating of dc link.

6.3.2 Motor starting at 13.8kV bus

The voltage dip due to starting of induction motors is also investigated. The simulation results are shown in Figure 6.20 through Figure 6.23 and summarized in Figure 6.24.

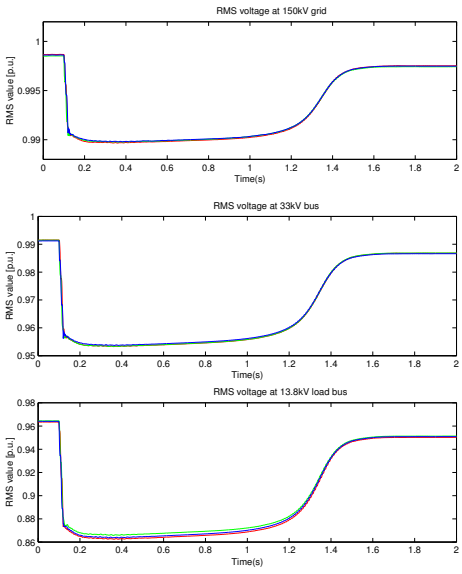


Figure 6.20: Ac supplied system

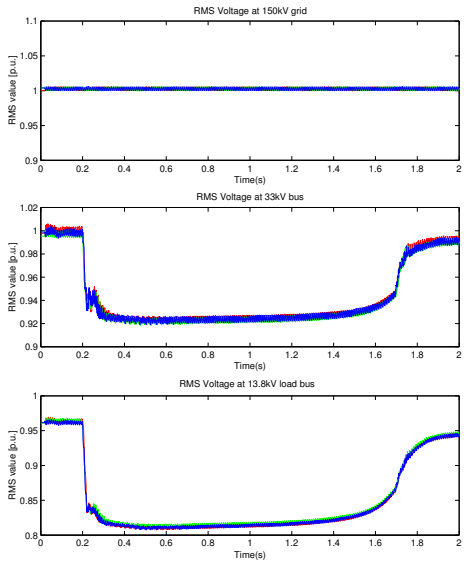


Figure 6.21: Dc supplied system

To an ac supplied industrial system, starting of an induction machine at 13.8kV bus causes a 5% voltage drop at 13.8kV bus, a 14% voltage drop at 33kV bus and a 1% voltage drop at 150kV grid (see Figure 6.20).

To a dc supplied industrial system, starting of the same induction machine at 13.8kV bus causes a 8% voltage drop at 13.8kV bus, a 18% voltage drop at 33kV bus, no voltage drop at 150kV bus (see Figure 6.21). So dc link can mitigate voltage dip propagation to upstream voltage levels. In this specific system voltage dips due to motor starts are not a concern for the public supply (at 150kV grid). However, if the connection to the public supply would have been at 13.8kV (e.g. with a smaller industrial system), the dc link could have been used to mitigate motor-starting dips in the public supply. Comparing Figure 6.20 and Figure 6.21 shows that the motor-starting dip is deeper and longer in the dc-supplied system. The same current limitation that reduces the dip upstream of the link causes a more severe dip downstream. However none of the resulting dips should be of much concern to standard industrial load.

The motor currents during motor starting and the motor speed at both systems are shown in Figure 6.22 and Figure 6.23. During the starting of an induction motor, the motor takes a larger current than normal, typical five to six times as large. This current remains high until the motor reaches its nominal speed.

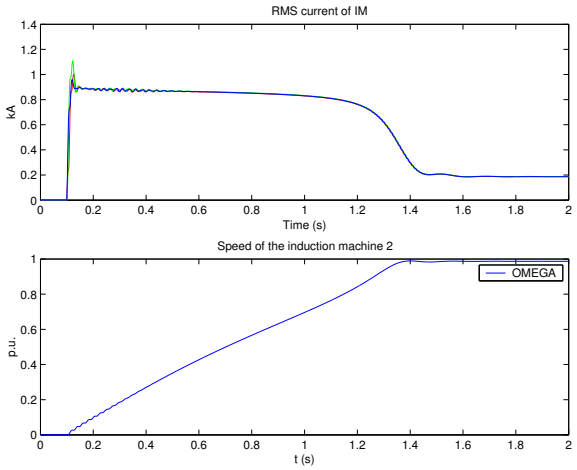


Figure 6.22: Ac supplied system

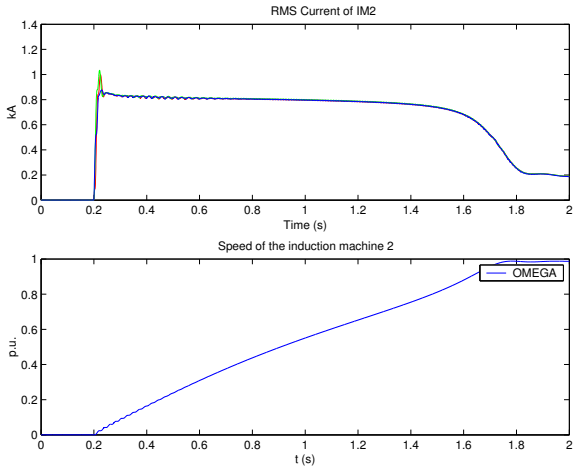


Figure 6.23: Dc supplied system

The resulting voltage dips at different bus due to motor starting are illustrated in Figure 6.24

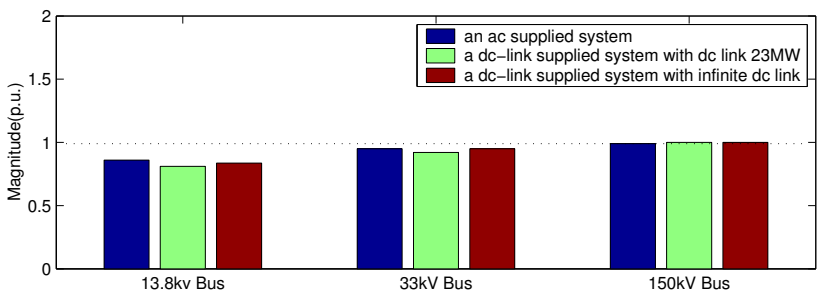


Figure 6.24: Voltage dip of different buses during motor starting at 13.8kV bus.

6.3.3 Equipment Behavior

To investigate the influence to different loads in an ac supplied industrial system and a dc link supplied industrial system, currents are measured at different loads: the synchronous motor, the induction motors, the ac drive and the dc drive. The case of single-phase-to-ground fault, which is a most common occurrence at 150kV grid, is simulated and the simulation results are illustrated.

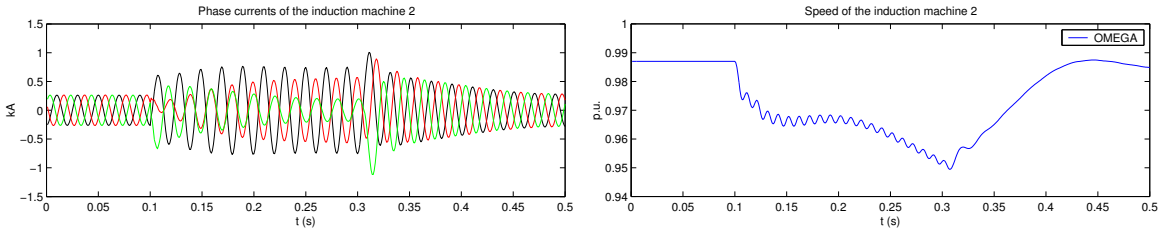


Figure 6.25: Induction motor under an ac supplied industrial system.

The induction motor is sensitive to disturbances in the supply voltage. The drop in voltages at 13.8kV load bus causes a drop in speed, the motor slows down. While the motor slows down, it takes a larger current with a smaller power factor. This also brings down the voltage even more. When the voltage recovers the motor takes a high inrush current. This large current slows down the voltage recovery. After that, the motor re-accelerates until it reaches its pre-speed. During the re-acceleration the motor again takes a larger current, which can cause a post-fault dip with a duration of one second or more [34]. This can best be understood from the model of a voltage source behind reactance. Thereby a distinction should be made between the positive and negative-sequence voltages and currents. Positive-sequence currents increase during the voltage dip, negative-sequence currents stay about constant[33].

Current and speed for the induction motor are shown in Figure 6.25. The highest current of the induction motor is 1kA for induction motor 2(6MVA). The speed slows down from 0.987 p.u. to 0.95 p.u..

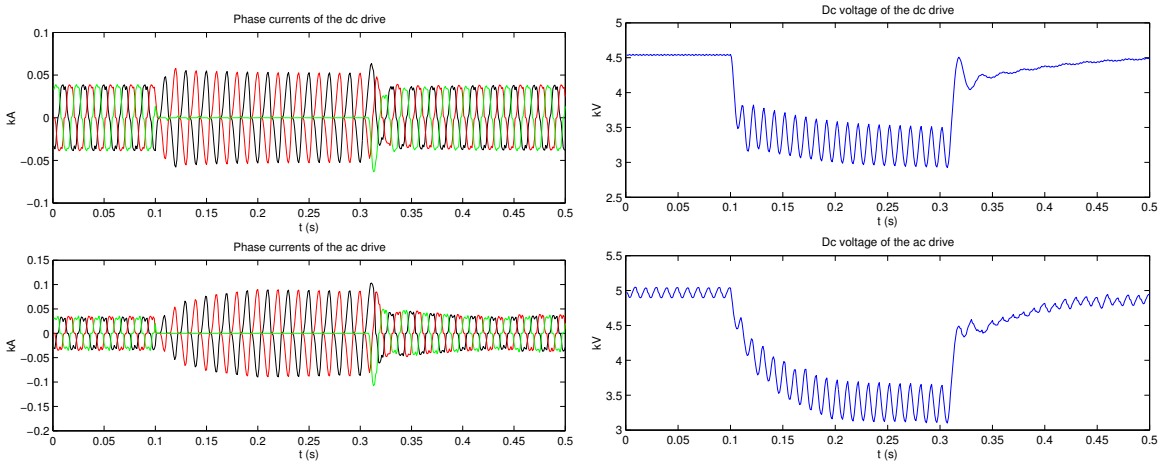


Figure 6.26: Drive under an ac supplied industrial system.

To the drives, the unbalance of the input ac voltages not only causes a large unbalance in ac currents, but also increases the ripple in the dc voltage. For the voltages

at 13.8kV load bus, one voltage is lower than the other two voltages, the rectifier only delivers current when the ac voltage is larger than the dc voltage, so the drop of phase voltages results in missing pulses. On the other hand, the capacitor charging six times per cycle in normal operation is now charging four pulses per cycle as the same amount of charge as the original six pulses, finally the magnitude of the pulses is increased [4].

Currents and dc voltage for the drives are shown in Figure 6.26. For ac drive, the dc bus voltage is obtained from the 13.8kV load bus through a transformer and a diode rectifier. When all three ac voltages at 13.8kV load bus drop, the dc voltage goes down if the size of the capacitor is not too big, as has been reported in some studies [4]. The highest current of ac drive is 0.1kA, the dc voltage goes down to 3kV. For dc drive, the dc bus voltage is obtained from the load bus through a transformer and a thyristor-controlled rectifier. As all three voltages go down in magnitude the dc voltage also drops. There is no capacitor present so the dc bus voltage drops instantaneously. The highest current of dc drive is 0.06kA, the dc voltage goes down to 3kV.

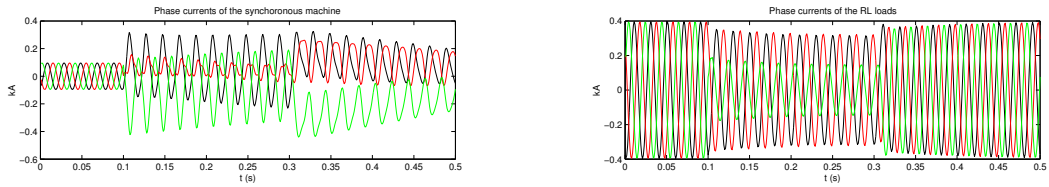


Figure 6.27: Current under an ac supplied industrial system.

The synchronous motor is also very sensitive to faults in the supply voltage. The magnitude of the transient current depends on the excitation current and on the ratio of direct axis transient inductance, the dc component will die out by damping resistances. From Figure 6.27 the highest current of synchronous motor is about 0.32kA.

The results for a dc-supplied system are shown in Figure 6.28 through Figure 6.30.

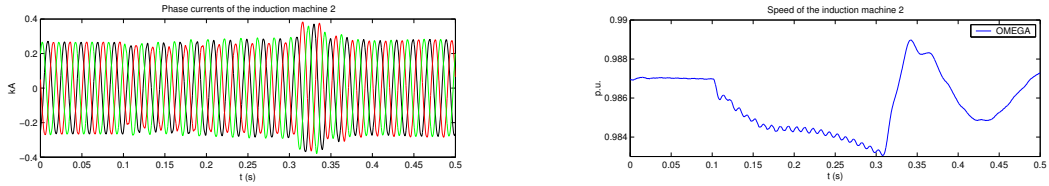


Figure 6.28: Induction motor under a dc supplied industrial system.

Current and speed of the induction motor are shown in Figure 6.28. The influence to induction motor is not so severe. The highest current of the induction motor is 0.38kA. The speed slows down from 0.987 p.u. to 0.983 p.u.. So the highest current of the induction motor is decreased, the drop of the speed is also reduced.

From Figure 6.29 small unbalance in the supply voltage still leads to the difference between the current pulses of the ac drive and dc drive, but the influences are not too much. The highest current of ac drive is less than 0.05kA, the dc voltage goes down to about 4.18kV. The highest current of dc drive is less than 0.05kA, the dc voltage goes down to about 4.18kV. So the same influences are seen from the dc drive and ac drive: the highest currents go down, the drops of the dc voltage go down.

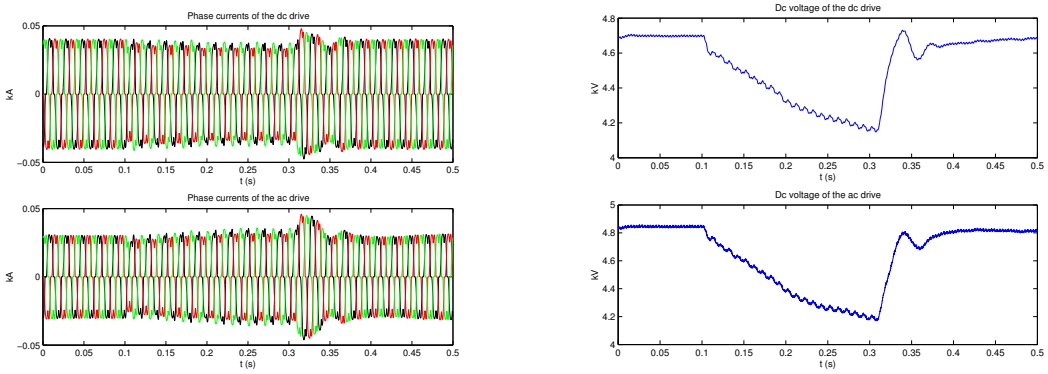


Figure 6.29: Drive under a dc supplied industrial system.

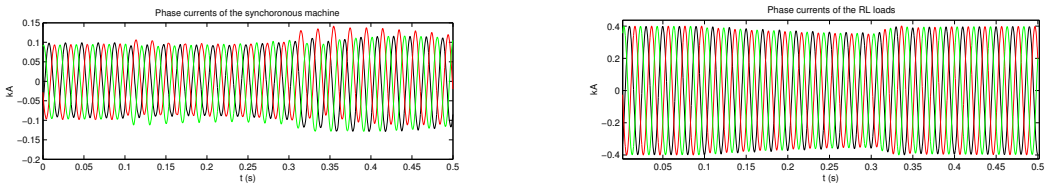


Figure 6.30: Current under a dc supplied industrial system.

The influence to synchronous motor is not so severe. From Figure 6.30 the highest current is 0.14kA, the dc components are much smaller.

The influences on the induction motor and ac drive in both systems are also compared through Table 6.1 and Table 6.2.

IM2	ac	dc
Max I	$1.0kA$	$0.38kA$
Min ω	$0.95p.u.$	$0.983p.u.$

Table 6.1: Comparison of induction motor

Ac drive	ac	dc
Max I	$0.1kA$	$0.048kA$
Min dc voltage	$3kV$	$4.18kV$

Table 6.2: Comparison of ac drive

Chapter 7

Dc networks

7.1 Introduction

In the previous chapter a dc-supplied network was compared with an ac-supplied network. In this chapter we will go a step further and consider design alternatives with different dc voltage levels.

Before the design alternatives are studied, the control of the dc/dc converter is discussed.

7.2 Dc-dc converter

7.2.1 Introduction

The dc/dc converter can be used as a voltage regulator to convert an unregulated dc voltage to a regulated dc output voltage. The dc/dc converter in most computers is such an example. The dc/dc converter can also be used to connect two different dc voltage levels. The preferred dc/dc converter topology in high-power applications has been the full-bridge circuit operated at constant frequency under a pulse-width control strategy[35][36].

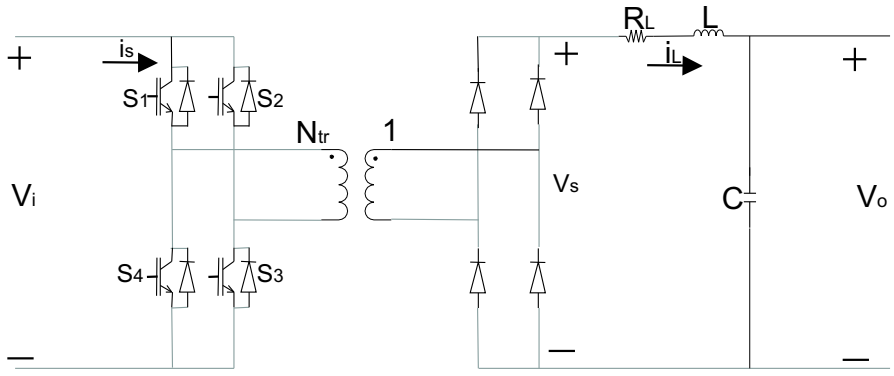


Figure 7.1: The PWM full-bridge converter

The full-bridge converter as shown in Figure 7.1, consists of a dc input voltage source v_i, four controllable switches S_1, S_2, S_3, S_4, a high frequency transformer, four diodes, an ideal inductor L, a very small resistance R_L, a capacitor C, and the dc output voltage v_o.

Its equivalent circuit is shown in Figure 7.2, which is modelled under the following assumption:

- Transistors and diodes are ideal.

- Passive components are linear.

- The inductor current i_L is constant during the entire switching period.

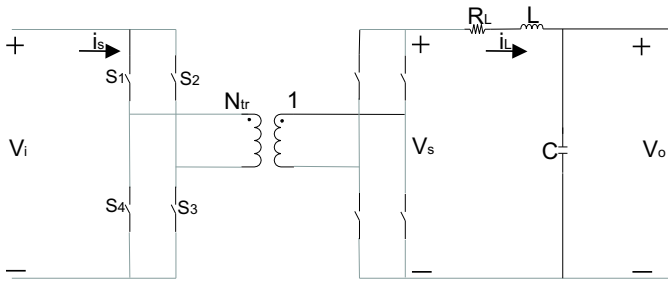


Figure 7.2: The equivalent circuit of the full-bridge converter

The switches $S1, S3$ and $S2, S4$ are turned on alternatively, each for an interval t_{on}. Here

$$t_{on} = T_s D \tag{7.1}$$

$$T_s = 1/f_s \tag{7.2}$$

where D is the ON duty ratio, f_s is the switching frequency.

So the relationships between primary-side and secondary-side quantities for the full-bridge converter can be written as

$$i_s = \frac{2Di_L}{N_{tr}} \tag{7.3}$$

$$v_s = \frac{2Dv_i}{N_{tr}} \tag{7.4}$$

where i_L is the current through the inductor L, i_s is the average current over one switching period, v_s is the average voltage over one switching period, and N_{tr} is the ratio of the high frequency transformer.

Finally the simplified circuit of the full-bridge converter is shown in Figure 7.3.

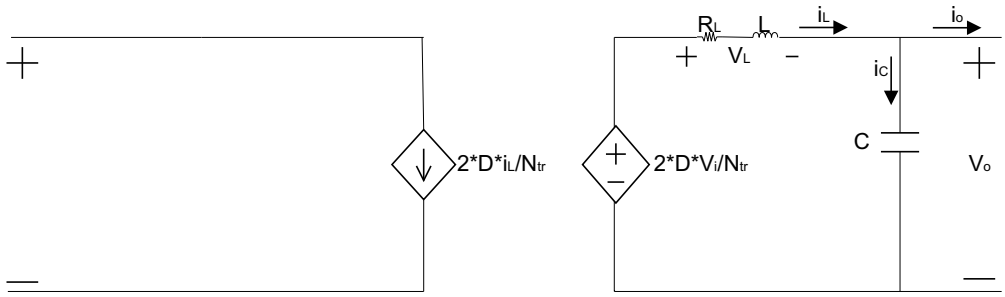


Figure 7.3: The simplified circuit of the full-bridge converter

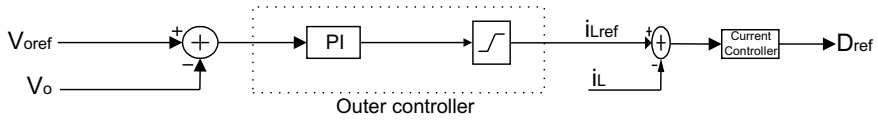


Figure 7.4: The control block diagram

7.2.2 Controller of the dc-dc converter

The output voltage of the dc/dc converter can be regulated in response to changes of output load and input voltage. The controller of the dc-dc converter uses a negative-feedback control system, consisting of the inner current controller and the outer voltage controller. The reference value of the current can be obtained from the outer voltage controller. The overall controller is shown in block diagram form in Figure 7.4.

As shown in Figure 7.4, the actual output voltage v_o is compared with its reference value v_{oref}, then produces the reference current through a PI controller and a limiter. The measured current of the inductor i_L is compared with the produced reference current i_{Lref}, then produces the reference value of the on duty ratio D_{ref} through the current controller.

Current controller

As shown in Figure 7.3, the voltage drop over the reactor is:

$$v_L = L\frac{\mathrm{d}i_L}{\mathrm{d}t} + R_L i_L \tag{7.5}$$

The current controller can consist of a simply PI controller[37]:

$$F_e(s) = k_p + \frac{k_i}{s} \tag{7.6}$$

where $k_p = \alpha_e L$ and $k_i = \alpha_e R$. Here α_e is the close-loop system bandwidth.

On the other hand, the voltage drop over the reactor can be also expressed as:

$$v_L = \frac{2Dv_i}{N_{tr}} - v_o \tag{7.7}$$

so the output D can be derived as:

$$D = \frac{N_{tr}(v_L + v_o)}{2v_i} \tag{7.8}$$

Finally the current controller can be written by considering the voltage saturation and anti-windup :

$$e = i_{Lref} - i_L \tag{7.9}$$

$$\frac{\mathrm{d}I}{\mathrm{d}t} = e + \frac{2v_i}{N_{tr}k_p}(D - d) \tag{7.10}$$

$$d = \frac{N_{tr}v_o}{2v_i} + \frac{(k_p e + k_i I)N_{tr}}{2v_i} \tag{7.11}$$

$$D = s(d) \tag{7.12}$$

$$s(d) = \begin{cases} D_{max}, & d > D_{max} \\ s(d), & 0 \leq d \leq D_{max} \\ 0, & d < 0 \end{cases} \tag{7.13}$$

Where e is the control error, I is the integrator state variable, d is unlimited duty ratio and D is the limited duty ratio.

Voltage controller

Equation (7.14) for the voltage across the capacitor can be obtained from the Figure 7.3.

$$C\frac{\mathrm{d}v_o}{\mathrm{d}t} = i_o - i_L \tag{7.14}$$

where i_o is the output current.

So the voltage controller can be derived:

$$i_{Lref} = i_o + (k_{pv} + \frac{k_{iv}}{s})(v_{oref} - v_o) \tag{7.15}$$

where k_{pv} and k_{iv} are the controller parameters, i_{Lref} is the reference or the desired value of the current i_L, v_{oref} is the reference or the desired value of the output dc voltage v_o.

It should be noted that i_{Lref} is limited in order to prevent overcurrent.

7.2.3 Simulation of the dc-dc converter

To test the controller of the dc-dc converter, the step response for change of output dc voltage is simulated. The simulation results are shown in Figure 7.5.

In Figure 7.5 the responses for two steps in the reference of the output dc voltage from 1kV to 0.5kV at 0.25s and from 0.5kV to 1kV at 0.5s are displayed. The results are from simulations with constant input voltage, i.e. Vin is 16kV, the transformer ratio is 14.4762, and constant impedance. The output dc voltage reaches the new setting value at about 0.35s and 0.6s. The current through the inductor follows the derived reference currents very well.

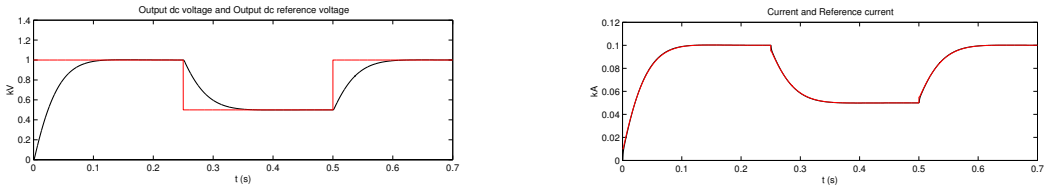


Figure 7.5: Step changes of dc-dc converter.

7.3 Multi-level dc systems

7.3.1 introduction

Three different networks with multiple dc voltage levels have been simulated. They are shown in Figure 7.6, Figure 7.7 and Figure 7.8. A multi-level dc network can be used to transport the electricity all the way from the transmission system to the drives. At the final stage an ac voltage of controllable frequency and amplitude is created.

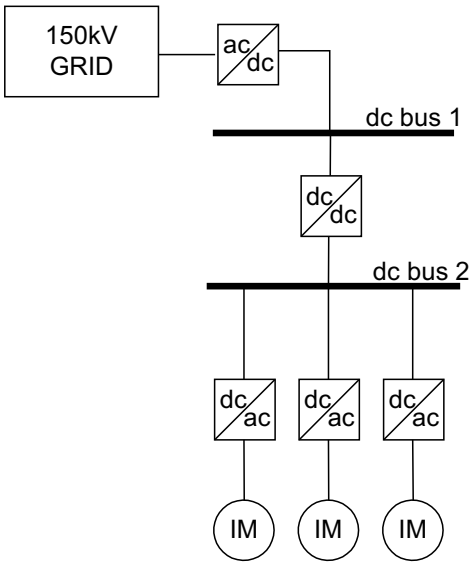


Figure 7.6: Multi-level dc system 1

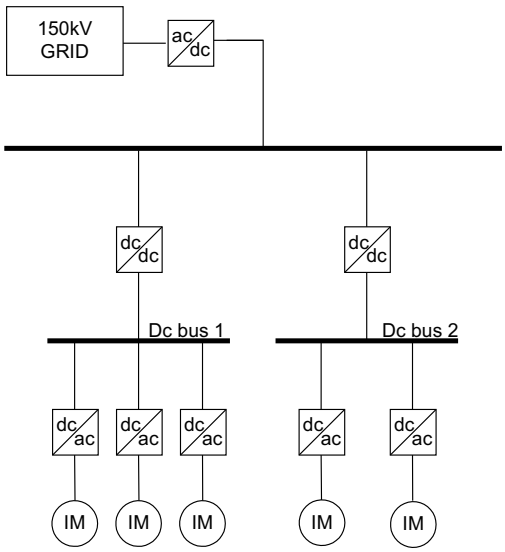


Figure 7.7: Multi-level dc system 2

7.3.2 Multi-level dc system 1

The network shown in Figure 7.6 supplies three large induction motors via two dc voltage levels. The voltages and frequencies of the three induction motors are 13.8kV, 10kV, 6kV and 60Hz, 50Hz, 25Hz, respectively, the sizes of the induction motors are 6MVA, 5MVA and 4MVA, respectively, so the total load is 15MVA. The dc voltages of the dc bus 1 and dc bus 2 are 160kV and 30kV. The control modes of the converters are

- For ac/dc converter at the 150kV side the dc voltage controller and the ac voltage controller are used.
- For dc/dc converter the dc voltage controller is used.

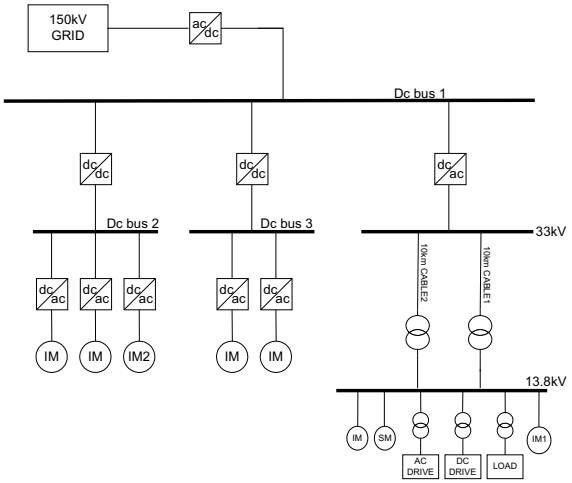


Figure 7.8: A possible mixed ac/dc system

- For dc/ac at the loads side the frequency and ac voltage controller are used.

To study the feasibility of such a system the starting of the motors was simulated. The three induction motors are switched on at 0.2s, 3.2s and 5s. The process of the starting of three induction motors is: the biggest induction motor (6MVA) is started first, then the 5MVA induction motor is started after the first induction motor reaches the steady state, finally the 4MVA induction motor is started. The switching instants are chosen such that each motor reaches its steady state before the next motor is started.

When the ratings of the ac/dc converter and dc/dc converter were set to 15MVA, simulation was not successful. It was not possible to start the motors.

When the ratings of the ac/dc converter and dc/dc converter are set to 21MVA it is possible to start the motors. Some results are shown in Figure 7.9.

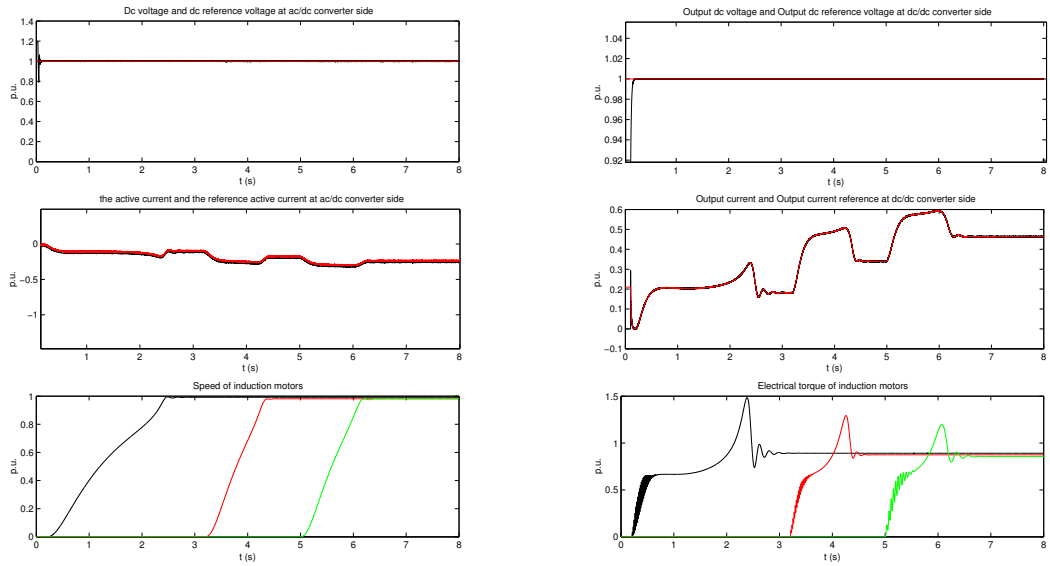


Figure 7.9: Multi-level dc system 1

From Figure 7.9, it can be concluded that the dc voltage is not affected by the consecutive starting of the three induction motors. All the three induction motors reach their steady-state speeds.

To investigate the effects on dc/dc converter and loads a three-phase-to-ground with a voltage dip of 50% is generated at 150kv side of the dc link. The ratings of the ac/dc converter and dc/dc converter are set to 21MVA like in the previous simulation. The simulation results are shown in Figure 7.10.

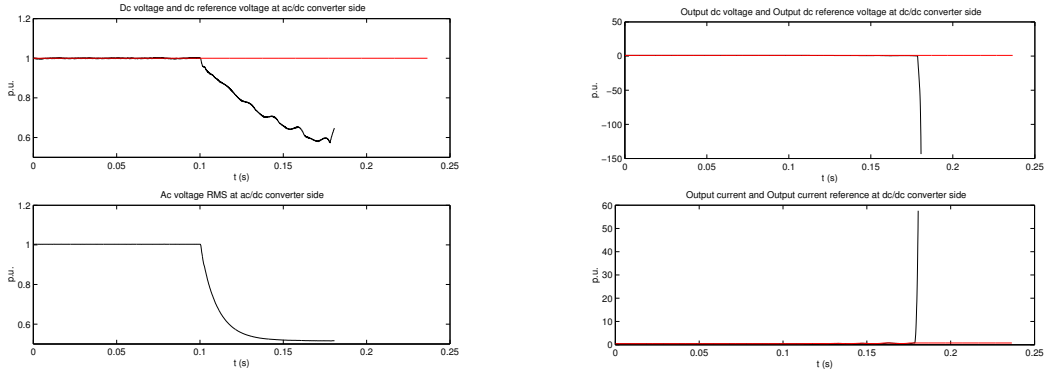


Figure 7.10: Three-phase-to-ground with voltage dip 50% at 150kV side for multi-level dc system 1

In Figure 7.10 the ac voltage rms value of ac/dc converter at 150kV side is decreased from 1.0p.u. to 0.5p.u. during the fault, and the system collapses after 0.18s. The current through the dc/dc converter reaches a very high value. In reality such a value would never be reached as some kind of protection would simply turn off the converter. The result would be a loss of supply to the induction motors and an interruption of the production process.

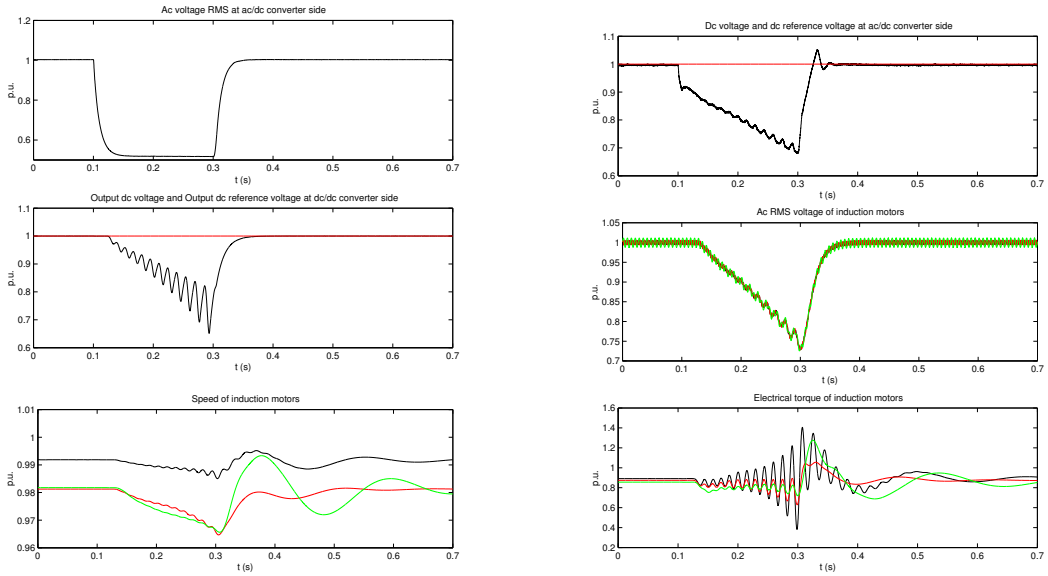


Figure 7.11: Three-phase-to-ground with voltage dip 50% at 150kV side for multi-level dc system 1

When the rating of the ac/dc converter and dc/dc converter are increased to 30MVA the converter can ride through the voltage dip. The simulation results are shown in Figure 7.11.

In Figure 7.11 the ac voltage rms value of ac/dc converter at 150kV side is decreased from 1.0p.u. to 0.5p.u. during the fault, the dc voltage of ac/dc converter is also decreased from 1.0p.u. to about 0.65 p.u., the output dc voltage of dc/dc converter also drop to 0.65 p.u., the ac rms voltage of the induction motors drop to 0.7 p.u.. Finally the speeds of three induction motors drop during the fault and show some oscillations after the voltage recovery.

7.3.3 Multi-level dc system 2

The multi-level dc system 2 shown in Figure 7.7 is base on the multi-level dc system 1. The new dc bus voltage is 20kV, the ac voltages of two load buses are 13.8kV and 10kV, respectively, the frequencies of two load buses are 60Hz and 50Hz, respectively. The induction motors are 6MVA and 5MVA, respectively. The process of motor starting is the same as before. Again when the rating of ac/dc converter, dc/dc converter 1, dc/dc converter 2 are set to 26MVA, 15MVA, 11MVA, the system collapses after a few seconds. But when the rating of ac/dc converter, dc/dc converter 1, dc/dc converter 2 are set to 30MVA, 18MVA, 16MVA, the system can reach steady state. The simulation results for the starting of the 5MVA induction motor are shown in Figure 7.12, Figure 7.13, and Figure 7.14. Before starting the 5MVA induction motor all other motors have reached their steady-state speeds.

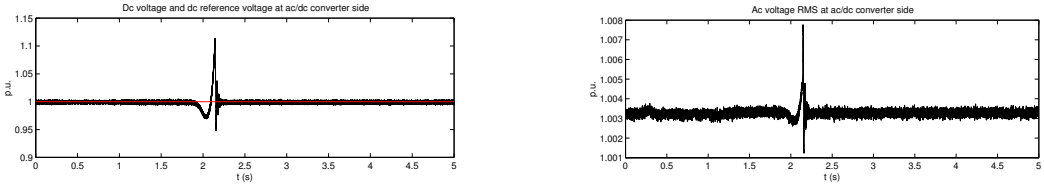


Figure 7.12: Voltage of the ac/dc converter for multi-level dc system 2

As shown in Figure 7.12, the dc voltage and the ac rms voltage of the ac/dc converter show a small transient during the starting of the last induction motor. When the induction motor is started, the dc voltage varies between 0.95 p.u. and 1.1 p.u., the ac rms voltage only varies between 1.001 p.u. and 1.0075 p.u..

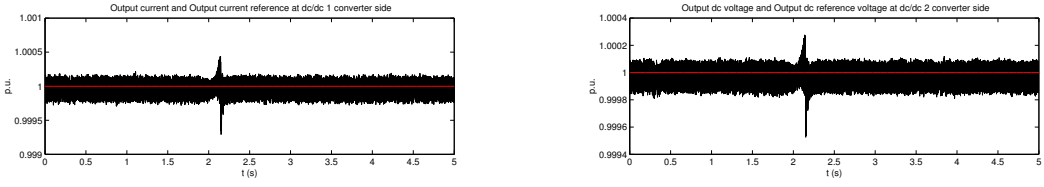


Figure 7.13: Dc voltage of the dc/dc converter for multi-level dc system 2

From Figure 7.13, it can be obtained that the dc voltage at dc bus 1 and 2 also can reach the set value except some transients at motor starting, the starting of the last motor does not affect the speeds of any of the other motors.

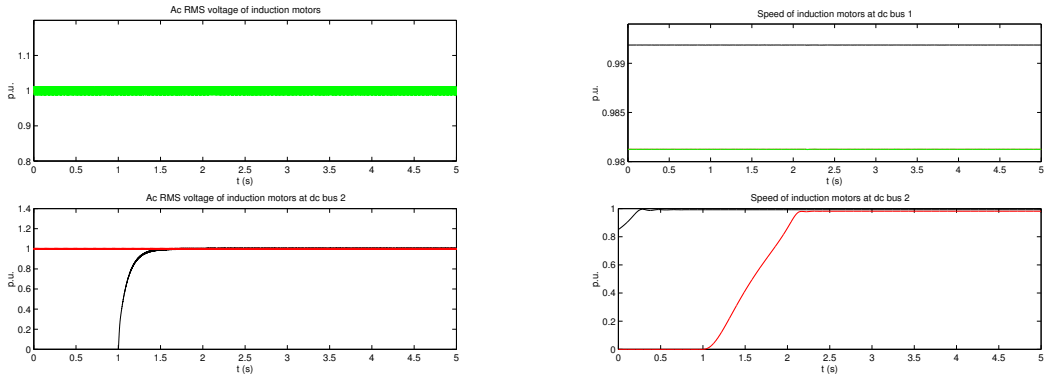


Figure 7.14: Induction motors for multi-level dc system 2

In Figure 7.14 the ac rms voltages, and the speeds of induction motors connected to dc bus 1 can run at steady state even if one induction motor at dc bus 2 is switched on. The ac rms voltage, the speed of the started motor can be ramped from zero.

7.4 Mixed ac/dc system

This system shown in Figure 7.8 is a combination of the multi-level dc system 2 and the passive industrial system shown in chapter 6. The same control modes which are explained before are used at the converters. The ratings of ac/dc converter, dc/dc converters are set to 49MVA, 18MVA, 16MVA. The industrial load is 23MVA. At this setting the system can reach steady state. Two cases are simulated to evaluate this system.

One case is that induction motor 1 (6MVA) is switched on at 0.1s. The results of this simulation are shown in Figure 7.15

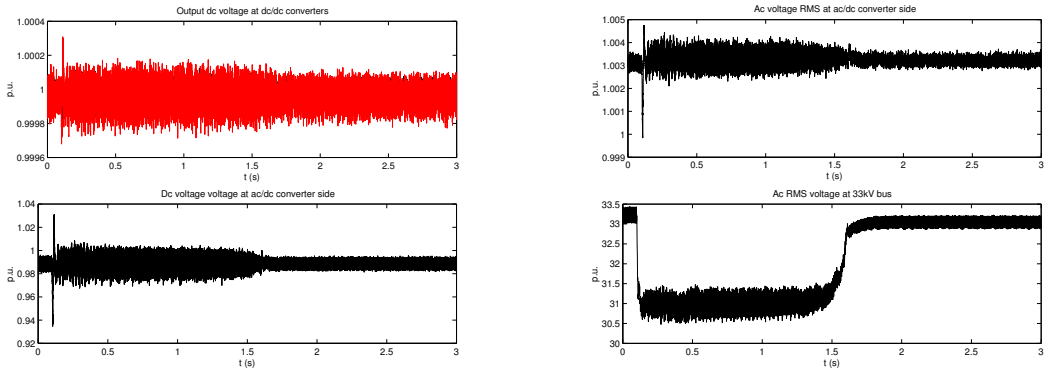


Figure 7.15: Switching on induction motor 1

From the simulation results in Figure 7.15 the switching of induction motor 1 causes a voltage dip at the 33kV load bus. The effect of motor starting on the dc voltage of ac/dc converter, the output dc voltage of dc/dc converter is very small. The only noticable effect is an increase in the amplitude of the oscillations. The loads connected to dc/dc converter side will not be affected.

The other case is that the induction motor 2 (6MVA) is switched on at 0.1s. The results are shown in Figure 7.16

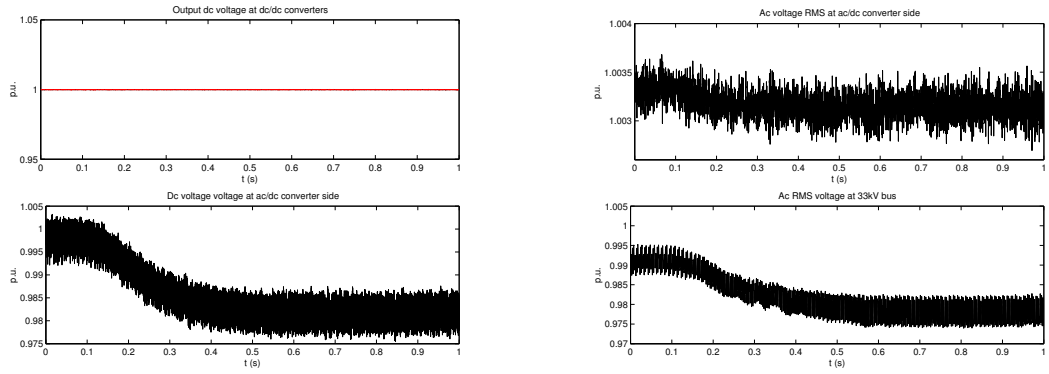


Figure 7.16: Switching on induction motor 2

In Figure 7.16 the dc voltage and ac voltage of ac/dc converter, the dc voltage of dc/dc converter, the ac voltage of 33kV load bus decrease during starting of induction motor 2.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

A model of a VSC-HVDC system and different control strategies are presented in this thesis. Two different control strategies are described and implemented in PSCAD/EMTDC. A comparison between an ac grid supplying a passive industrial system and a dc link supplying the same industrial system has been done by using PSCAD/EMTDC. Investigations of some possible applications of the dc medium-voltage system have been modelled and evaluated.

8.1.1 Control system

Using pulse-width modulation (PWM) for voltage-source converters enables independent control of real and reactive power within the equipment limits. The HVDC control objectives and schemes will change significantly because of this. Different kinds of controllers can be used depending on the application. A decision on which controller to use may require advanced power system study. But the active power flow through the dc link must be the same with both terminals, the dc voltage controller is necessary to achieve this balance.

The control system of the VSC-HVDC is based on a fast inner current control loop controlling the ac current in combination with a number of outer controllers. For the inner current controller, a feedback control scheme has been developed, which controls the negative sequence line current to zero. The validity of the proposed control has been confirmed in PSCAD/EMTDC.

From the simulation results, it is concluded that the system response is fast; control accuracy can be derived; high quality ac voltages and ac currents can be obtained; and that the active power and the reactive power can be controlled independently and are bi-directional. But fast transient variations of the operating point of the converter will cause transients in the dc voltage. Overcurrents at fault initiation can not be avoided. For IGBTs, it might be acceptable to run through very high current for very short time, and thus these overcurrents are not necessarily a problem.

Simulation results have also shown that the converter applied to supply industrial

distribution systems may have some effect on mitigating voltage dips. The extent to which voltage dips are mitigated depends on the setting of the current limitation. Normally maximum current capability for the VSC is determined by the requirements for steady state operation, which means that the current overload capability is very limited. This will limit the performance of the converters during faults and during load switching involving high currents (e.g. motor starting). In one case the peak current could actually be reduced by increasing the current-limit setting. It is not clear if this holds general or only for specific systems.

8.1.2 Dc-supplied ac system

A number of design alternatives for the supply to an industrial power system have been studied by using PSCAD/EMTDC simulations: one pure ac system, and four systems with various amounts of dc links. In all those four cases the power is supplied through a VSC-HVDC link. The difference between the design alternatives is in the way in which the power is distributed to the loads.

The following conclusions are drawn for the dc-supplied industrial system with normal ac distribution.

- It is possible to supply the ac industrial system through a dc link with the same rating as the total rating of the load.
- For balanced faults the dc link will delay the drop in voltage. This delay is due to a combination of the energy stored in the dc link and the energy stored in the rotating machines. For equal dc-link rating as the total load the lowest rms voltage is the same as for the pure ac system. However the slower drop in rms voltage will make that the dips are less deep and of shorter duration for faults with normal fault-clearing times (100 to 200 ms).
- The performance during a voltage dip depends significantly on the behavior of the control system when current limitation is activated. The strategy for using the limited amount of current depends on the type of application of the dc link.
- Increasing the rating of the dc link will mitigate to some extent the voltage dips due to a balanced fault.
- For unbalanced faults the voltage dips in the dc-supplied ac system are less severe than in the pure ac system, without the need to overrate the dc link. Overrating the dc link will further mitigate the dips.
- The dc link mitigates the effect of motor starting on the public supply. However the resulting voltage dip in the industrial system is longer and deeper. This is not necessarily a problem as sensitive load may be supplied from another part of the system as the large motors.

8.1.3 The multi-level dc systems

The following conclusions are obtained for the multi-level dc systems.

- Overrating of the converters is needed to allow starting of the induction motors with almost full load. This problem does not occur in the dc-supplied ac system because the proportion of motor load on the converter is less in that system.
- Overrating of the converters is needed to withstand voltage dips due to symmetrical faults in the public supply.
- Further investigation of the control system is needed to allow building of these networks without having to overrate the converters.

8.1.4 The mixed ac/dc system

The following conclusions are derived for the mixed ac/dc system.

- Overrating of the dc/dc converters is needed to allow starting of the induction motors with almost full load.
- For ac/dc converter it is possible to supply the mixed ac/dc system with the same rating as the total rating of the load.

8.1.5 Design of VSC industrial power systems

It is found during the various studies that the choice of the current limit setting (thus of the rating of the converter) is an important factor in the design of industrial power systems with power-electronic converters (like VSC-HVDC links). The design process of any industrial power system contains three "levels".

- the system should be able to supply any possible steady-state load.
- the system should be able to provide "normal overloads" like starting of equipment.
- the system should be able to withstand internal and external faults. Such faults may lead to an interruption of plant operation (a production stoppage), but the voltages and currents due to the fault should not lead to permanent damage of equipment.

Steady-State Operation

During steady-state operation the voltages at the equipment terminals should be within the pre-defined limits. Typical limits are 95 - 105% and 90 - 110%. Strictly-speaking these limits are only applicable to the equipment terminals. There is no strict need for voltage limits elsewhere in the system. However the way power systems are currently designed and operated requires voltage limits are kept at all voltage levels. This more or less guarantees that the voltage levels are kept with the equipment terminals as well. Using power-electronic converters may make that it will be no longer needed to maintain the voltage at each voltage level. This alternative is not investigated in this study.

The currents during steady-state operation should not exceed the rating for any of the components in the system.

Both conditions should hold for any steady-state operation, but the most severe case is in most cases the highest steady-state load. For the voltage criterion a low-load situation may sometimes lead to overvoltages. These should also be within the required range.

At this level of design there is no difference between a pure ac system and a VSC system. A possible difference may be that the various converters may help in keeping the voltage at the equipment terminals within their limits, without the need for strict voltage limits in the dc parts of the system.

Normal Overloads

The loading of the system sometimes exceeds the maximum steady-state loading. A typical example is the starting of a large induction motor, but also other normal switching actions may lead to temporary overload situations. The system should be able to withstand these loads and the voltage at the equipment terminals should be such that the equipment continues to operate as normal. The voltage may be temporarily outside of the steady-state limits as long as the end-user equipment can tolerate this. There are no generally-accepted standards for end-user equipment with respect to short-duration voltage deviations, so that the design of the system should include the definition of the voltage-tolerance requirements of the load. A solution would be to ensure that even during normal overloads the voltage stays within the steady-state limits.

In the design of pure ac systems this was taken care of mainly by designing the components in such a way that they can tolerate short-duration overloads, e.g. a transformer can be loaded at 150% of its rating during 1 minute (hypothetical example, no quote from a standard). With converters this is no longer possible, as the overload capacity of power-electronic components is very small, even for very short duration. Therefore the converters should be able to supply not only the highest possible steady-state load but also any "normal overload".

The rating of the converters in a VSC system should thus at least be equal to the highest normal overload. To know this value the details of the industrial process need to be known. A safe value would be to assume starting of the largest induction motor while all other loads are at maximum power. But this could lead to an overrated (and thus too expensive) system.

An other approach would be to reduce the voltage to its lowest limit during the starting of a large load. This will reduce the starting current and thus the required rating of the converter. The disadvantage of such a scheme is that it may take longer to start the equipment (e.g. the case with induction motors). The resulting reduction in voltage may affect the performance of other equipment.

Internal and External Faults

The design of the system during internal and external faults is somewhat different than at the first two levels. Faults are rare events so that it is in some cases acceptable that

the operation of the end-use equipment is disrupted by the fault. This will lead to an interruption of the industrial process. An important design criterion is the frequency with which such process interruptions occur. To prevent process interruptions, some kind of redundancy is needed in the supply.

But whereas process interruptions are to some extent acceptable, damage to end-use equipment or to system component should not occur, not even during faults. Also should the impact on end-use equipment (thus on the industrial process) be as small as possible. It is the role of the power-system protection to take care of this.

Faults are associated with high currents and low voltages. High currents in the industrial system only occur for internal faults; low voltages occur both for internal and for external faults. In pure ac power systems, damage to equipment is prevented by limiting the fault-clearing time to a value less than the time the equipment can tolerate the fault current. But for power-electronic components this time is so short that the classical protection cannot clear the fault fast enough to prevent damage. Therefore active current limitation is needed, as discussed in one of the chapters of this licentiate thesis. The setting of the current limit of the converters is at least equal to the current rating as determined in level 1 and level 2 of the design process.

The disadvantage of current limitation (thus of a low rating) is that typically the voltage during an internal or external fault will be lower than without current limitation. The adverse effects on the production process will be less for a higher setting of the current limitation (thus for a higher rating of the components). This trade-off is part of the third design level. It requires detailed knowledge of how acceptable or unacceptable a process interruption is.

In pure ac systems the number of process interruptions is reduced by introducing redundancy in the components. This is successful against internal faults but not against external faults (better known as voltage dips). Some pure ac solutions are possible against external faults but in general power-electronics has to be introduced here.

In VSC systems redundancy may help to prevent interruptions, but against voltage dips the rating of the converters needs to be increased, as shown in the earlier chapters. A stochastics-based study is needed to find an optimal rating.

8.2 Future Work

As described before, VSC distribution and transmission have some disadvantages, which include potentially high losses and costs, but the technology continues to evolve. To further assess the potential and limitation of VSC distribution and transmission for industrial power systems, a number of possible applications and advancements in the VSC technology are required.

- Control system.

  Due to the second harmonics on the dc voltage if unbalanced faults occur, the control system should be improved to reduce or eliminate the harmonics. The frequency control also should be evaluated.

- On-site generation.

Connecting on-site generation downstream of the dc network can increase the fault level and thus solve some of the protection problems. On the other hand, it may introduce other problems, like difficulties with voltage and frequency control. Control algorithms and design methods should be developed to allow the combination of VSC-HVDC with on-site generation.

- Faults and protection.

  Faults in the dc system and faults in the downstream ac islands remain a serious concern. One of the problems is that the fault current in the downstream ac system is limited by the converters. This may make it different to use existing protection strategies. Differential or distance protection are probably able to solve this problem, but at higher costs than the traditional overcurrent protection. Protection of the dc network is very strongly related to the reliability of that network. Fast and reliable dc breakers are a possible solution.

- System design.

  The main substations are the place where the ac connections come together. The reliability of the supply is very strongly related to the position of circuit breakers and other switchgear. Also in the dc version a substation-like structure is needed. The dc substation will have to be designed based on the availability of suitable switchgear.

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Denotations

C_{dc}	Dc-link capacitor
U_{dcN}	Nominal dc voltage
U_{dc}	Actual dc voltage
S_N	Nominal apparent power of the converter
τ	Time constant of dc-link capacitor
V_{2i}, u_v	Ac voltage at the inverter side
i_{vi}, i_v	Ac current at the inverter side
V_{1i},u_L	Ac voltage at the transformer secondary side
i_{Ti}, i_{Li}	Ac current at the transformer secondary side
f_c	Carrier frequency
f_1	Fundamental frequency
m_f	Frequency modulation ratio
M	Modulation index
ω	Fundamental angular frequency
φ	Phase angle shift
X_v L_v	Phase reactor
R_v	Phase resistor
P	Active power
Q	Reactive power
ΔV	Voltage drop
u_{La}, u_{Lb}, u_{Lc}	Phase voltages of the transformer secondary side
i_{La}, i_{Lb}, i_{Lb}	Phase currents which flow into the transformer
i_{va}, i_{vb}, i_{vb}	Phase currents which flow into the VSC
u_{Lap}, u_{Lbp}, u_{Lcp}	Positive sequence voltage of transformer side
u_{Lan}, u_{Lbn}, u_{Lcn}	Negative sequence voltage of transformer side
i_{vap}, i_{vbp}, i_{vcp}	Positive sequence current of transformer side
i_{van}, i_{vbn}, i_{vcn}	Negative sequence currents of transformer side
u_{vap}, u_{vbp}, u_{vcp}	Positive sequence voltage of VSC side
u_{van}, u_{vbn}, u_{vcn}	Negative sequence voltages of VSC side
x_a, x_b, x_c	Three phase quantities
$\bar{x}_{\alpha\beta}$	Space vector
x_α, x_β	Three phase quantities
$x_{\alpha p}, x_{\alpha n}, x_{\beta p}$,$x_{\beta n}$	Positive and negative sequence components in the $\alpha\beta$ axis
T	One cycle period of the network fundamental frequency

k	Time step
T_s	Sampling period of the control system
i_{vdp}	Positive-sequence reactive current
i_{vdn}	Negative-sequence reactive current
i_{vqp}	Positive-sequence active current
i_{vqn}	Negative-sequence active current
k_p	Proportional gain for ac current control
$P_{ac(abc)}$	Instantaneous active power
$Q_{ac(abc)}$	Instantaneous reactive power
P_{dc}	Power transmitted on the dc side of the VSC
U	Amplitude of the phase voltage
$P_{ac(dq)}$	Instantaneous active power in dq-frame
$Q_{ac(dq)}$	Instantaneous reactive power in dq-frame
ΔP	Power unbalance
Δf	Frequency drift
$\|u\|$	Amplitude of the line voltage
$\|u^*\|$	Reference value of the amplitude of the line voltage
S	Instantaneous apparent power
i^{dqp^*}, i^{dqn^*}	Complex conjugate of the positive and negative current vectors
D	Duty ratio
N_{tr}	Transformer ratio
$v^*_{vdp}(k)$	Reference values of the positive voltages
$v^*_{vdn}(k)$	Reference values of the negative voltages
$i^*_{vdp}(k)$	Reference values of the positive reactive current
$i^*_{vqn}(k)$	Reference values of the negative active current
$v^*_{vqp}(k)$	Reference values of the positive voltages
$v^*_{vqn}(k)$	Reference values of the negative voltages
$i^*_{vqp}(k)$	Reference values of the positive active current
$i^*_{vdn}(k)$	Reference values of the negative reactive current

Abbreviations

IGBTs	Insulated Gate Bipolar Transistors
PWM	Pulse Width Modulation
PCC	Point of common coupling
VSC	Voltage source converter
ac or AC	Alternative Current
dc or DC	Direct Current
HVDC	High voltage direct current
VSC-HVDC	Voltage source converter based High voltage direct current
CSC	Current source converter
CCC	Capacitor commutated converter
PLL	Phase locked loop

Appendix

Components for the ac supplied industrial system:

Induction motor 1 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1255kA

Based angular frequency: 314.159265rad/s

Induction motor 2 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.2510kA

Based angular frequency: 314.159265rad/s

Induction motor 3 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1255kA

Based angular frequency: 314.159265rad/s

Synchronous motor:

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1046kA

Based angular frequency: 314.159265rad/s

RL loads:

Rated RMS phase voltage: 7.967kV

R: 19.044Ω L: 0.06062H

3 phase 2 winding tranformer 1:

3 phase transformer MVA: 30MVA

Based operation frequency: 50Hz

Winding 1 type: Y

Winding 2 Type: Δ

Leakage inductance: 0.2 p.u.

Wind 1 line-to-line voltage (RMS): 33.0kV

Wind 2 line-to-line voltage (RMS): 13.8kV

3 phase 2 winding tranformer 2:

3 phase transformer MVA: 1MVA

Based operation frequency: 50Hz

Winding 1 type: Δ

Winding 2 Type: Y

Leakage inductance: 0.2 p.u.

Wind 1 line-to-line voltage (RMS): 13.8kV

Wind 2 line-to-line voltage (RMS): 4.16kV

3 phase 2 winding tranformer 3:

3 phase transformer MVA: 60MVA

Based operation frequency: 50Hz

Winding 1 type: Y

Winding 2 Type: Δ

Leakage inductance: 0.2 p.u.

Wind 1 line-to-line voltage (RMS): 150kV

Wind 2 line-to-line voltage (RMS): 33kV

Cable:

Steady state frequency: 50Hz

Length of cable: 10km

Overhead line:

Steady state frequency: 50Hz

Length of cable: 25km

Components for the dc supplied industrial system:

Single phase tranformer 1:

Transformer MVA: 20MVA

Based operation frequency: 50Hz

Leakage inductance: 0.0267 p.u.

Resistance: 0.0019 p.u.

Wind 1 phase voltage (RMS): 19.05256kV

Wind 2 phase voltage (RMS): 45.322kV

Single phase tranformer 2:

Transformer MVA: 20MVA

Based operation frequency: 50Hz

Leakage inductance: 0.0267 p.u.

Resistance: 0.0019 p.u.

Wind 1 phase voltage (RMS): 86.603kV

Wind 2 phase voltage (RMS): 45.322kV

Induction motor 1 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1255kA

Based angular frequency: 314.159265rad/s

Induction motor 2 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.2510kA

Based angular frequency: 314.159265rad/s

Induction motor 3 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1255kA

Based angular frequency: 314.159265rad/s

Synchronous motor:

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.1046kA

Based angular frequency: 314.159265rad/s

RL loads:

Rated RMS phase voltage: 7.967kV

R: 19.044Ω L: 0.06062H

3 phase 2 winding tranformer 1:

3 phase transformer MVA: 30MVA

Based operation frequency: 50Hz

Winding 1 type: Y

Winding 2 Type: Δ

Leakage inductance: 0.2 p.u.

Wind 1 line-to-line voltage (RMS): 33.0kV

Wind 2 line-to-line voltage (RMS): 13.8kV

3 phase 2 winding tranformer 2:

3 phase transformer MVA: 1MVA

Based operation frequency: 50Hz

Winding 1 type: Δ

Winding 2 Type: Y

Leakage inductance: 0.2 p.u.

Wind 1 line-to-line voltage (RMS): 13.8kV

Wind 2 line-to-line voltage (RMS): 4.16kV

Cable:

Steady state frequency: 50Hz

Length of cable: 10km

Components for multi-level dc networks

Single phase tranformer 2:

Transformer MVA: 20MVA

Based operation frequency: 50Hz

Leakage inductance: 0.0267 p.u.

Resistance: 0.0019 p.u.

Wind 1 phase voltage (RMS): 86.603kV

Wind 2 phase voltage (RMS): 45.322kV

Induction motor 1 :

Rated RMS phase voltage: 7.967kV

Rated RMS phase current: 0.2510kA

Based angular frequency: 376.991118rad/s

Induction motor 2 :

Rated RMS phase voltage: 5.7737kV

Rated RMS phase current: 0.2887kA

Based angular frequency: 314.159265rad/s

Induction motor 3 :

Rated RMS phase voltage: 3.4642kV

Rated RMS phase current: 0.3849kA

Based angular frequency: 157.0796rad/s