Optimum barrier thickness study for the InGaAs/InAlAs/AlAs heterostructure barrier varactor diodes

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(Received 7 September 2006; accepted 4 December 2006; published online 3 January 2007)

This experimental study aims at finding the optimum barrier thickness in heterostructure barrier varactor (HBV) diodes to improve the diode efficiency especially for high-power frequency multiplier applications. The influence of barrier thickness on the destructive current leaking over and through the barrier is investigated for different biases and operating temperatures. The authors found that for an InP-based HBV, there is an optimum barrier thickness range between 10 to 14 nm which causes the lowest possible leakage current. © *2007 American Institute of Physics*.
[DOI: 10.1063/1.2430632]

There are many interesting applications possible with technologies operating within the millimeter and submillimeter wavelength bands, e.g., medical and biological, high-speed communication, surveillance systems, and imaging and sensing for security.[1] These applications have a common need for power sources at these frequencies. In one approach, sources are realized by multiplying a lower frequency using a nonlinear capacitance (varactor). Recent research on heterostructure barrier varactor (HBV) diodes has indicated that they are a very good candidate for use in varactor multipliers.[2] The HBV has a great advantage due to a symmetric capacitance-voltage characteristic allowing only odd harmonics to be created. The efficiency of the HBV device is determined by the capacitance swing and the losses in the diode.[3] In the HBV there is a high band gap material creating a barrier for electrons. Under biased conditions, electrons are accumulated at one side of the barrier and depleted at the other side. Thereby the capacitance decreases for increasing bias voltage. However, the magnitude of the bias voltage is limited due to a voltage dependent leakage current caused by electrons traveling over and through the barrier. In this letter we investigate how this leakage current can be limited by optimizing the design of the barrier.

We have fabricated high performance HBV diodes in a material system lattice matched to InP, see Table I. The high band gap semiconductor [InAlAs plus thin layer of AlAs (Ref. 4)] is sandwiched between moderately doped semiconductor layers with a lower band gap (InGaAs modulation layers). This layer sequence can be repeated *N* times to create an *N*-barrier HBV diode. The leakage current will decrease the multiplier efficiency and therefore the barrier thickness needs to be studied for a proper design and analysis of HBVs. A theoretical investigation of InAlAs/InGaAs/AlAs single barrier varactors has been published, showing that there is an optimum barrier thickness range minimizing the leakage current.[5] In this work, we experimentally verify these theoretical predictions. We present the leakage currents for different in-house InP molecular beam epitaxy (MBE) grown materials. The optimized barrier thickness range is deduced from an experimental temperature study at different bias voltages.

The leakage current is a function of the bias voltage across the barrier and the temperature in the device. This current is determined by the amount of tunneling through the barrier as well as thermionic emission over the barrier. The probability of both tunneling and thermionic emission depends on several parameters, such as barrier thickness, barrier height, temperature, and quality of the crystal and heterointerfaces. For a thin barrier and low bias voltage levels, the height of the barrier is sufficient to avoid thermionic emission and therefore the electron tunneling dominates over the thermionic leakage current contribution. For high bias voltage levels and thicker barriers, the thermionic emission dominates.[6] Since the effective barrier height decreases with increasing barrier thickness and bias voltage, there will be an optimum barrier thickness that depends on the voltage across the diode and the device temperature.

We have grown five materials, MBE1196–MBE1200, on semi-insulating InP using an EPI930 solid-source molecular beam epitaxy system. The growth rate was nominally set to 0.53 μm/h. The materials have the common structure of a two-barrier InP-based HBV diode but with varying total barrier thicknesses from 4 up to 21 nm, see Table I. Test diodes from the five MBE materials have been fabricated. Each di-

TABLE I. Two-barrier InP-based HBVs used in this study.

No.	Layer	Material	Thickness	Doping
10	Contact layer	$In_{0.53}Ga_{0.47}As$	260 nm	10^{19} cm^{-3}
9	Modulation	$In_{0.53}Ga_{0.47}As$	250 nm	10^{17} cm^{-3}
8	Spacer	$In_{0.53}Ga_{0.47}As$	5 nm	Undoped
7	Barrier	$In_{0.52}Al_{0.48}As$+AlAs+ $In_{0.52}Al_{0.48}As$	4, 10, 14, 17, and 21 nm[a]	Undoped
6	Spacer	$In_{0.53}Ga_{0.47}As$	5 nm	Undoped
5	Modulation	$In_{0.53}Ga_{0.47}As$	250 nm	10^{17} cm^{-3}
4	Spacer	$In_{0.53}Ga_{0.47}As$	5 nm	Undoped
3	Barrier	$In_{0.52}Al_{0.48}As$+AlAs+ $In_{0.52}Al_{0.48}As$	4, 10, 14, 17, and 21 nm	Undoped
2	Spacer	$In_{0.53}Ga_{0.47}As$	5 nm	Undoped
1	Modulation	$In_{0.53}Ga_{0.47}As$	250 nm	10^{17} cm^{-3}
0	Buffer	$In_{0.53}Ga_{0.47}As$	0.5 μm	10^{19} cm^{-3}
	Substrate	InP		SI

[a]Chalmers MBE1196, MBE1197, MBE1198, MBE1199, and MBE1200, respectively.

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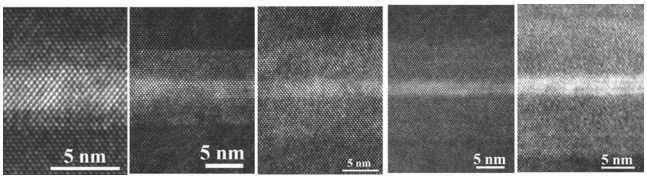

FIG. 1. High-resolution TEM images of the barrier structure of the materials MBE1196–MBE1200 from left to right.

ode has a mesa with a cross section of $58\times58\ \mu m^2$ where the surrounding epilayers have been removed by wet etching down to the buffer layer. Ohmic contacts were deposited both on top of the mesas and on the buffer layer. The barrier thickness for these materials, extracted from *C-V* measurements and corroborated by transmission electron microscopy (TEM) analysis, includes two undoped InAlAs layers with a 3 nm AlAs layer in the middle. We have verified lattice match condition and material quality by using an x-ray diffraction and cross-sectional TEM analysis. The detailed structure of the barriers for each material is clearly demonstrated by high-resolution TEM images, see Fig. 1. In these materials, no dislocations were found at the interface between InAlAs and InGaAs layers or at the interface between InAlAs and AlAs layers.

For the presented materials, we have measured *I-V* characteristics, maximum break through voltages, and the minimum differential conductances defined as

$$G_{\min} = \left.\frac{dI}{dV}\right|_{V=0}$$

from room temperature up to 170 °C with 15 °C interval.

Figure 2 shows the measured current density versus applied bias voltages at room temperature. The reproducibility between different diodes on the same chip was excellent. Devices with a 4 nm barrier show a very low breakdown voltage and relatively high leakage current, caused by a high tunneling probability.

Figure 3 shows the Arrhenius plot of the minimum differential conductance for different barrier thicknesses. It can be seen that the minimum differential conductance reaches a minimum for the diodes with the barrier thicker than 14 nm, i.e., when the thermionic field emission dominates. For even thicker layer, the effective barrier height decreases because the influence of the 3 nm AlAs layer becomes negligible.

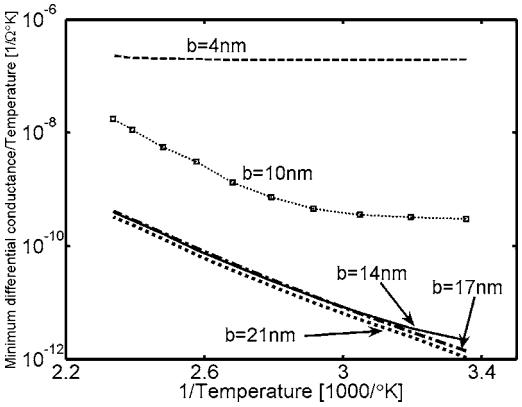

FIG. 3. Arrhenius plot of minimum differential conductance vs temperature (at $V_{bias}=0$ V).

The effective barrier height has been extracted from this plot for the three thickest barriers and is equal to 490 meV for flatband condition.

Figure 4 shows the current density as a function of the barrier thickness at four different temperatures. The solid lines represent low voltage (0.4 V) current densities. The dashed lines represent high voltage levels (7.0 V), which are below the device breakdown voltage in all cases except for MBE1196 (4 nm barrier thickness) at high temperature, 145 °C. From Fig. 4, it can be seen that by increasing the bias voltage across the device, the optimum barrier thickness with respect to the leakage current is reduced.

The influence of barrier thickness on the breakdown voltage is shown in Fig. 5; maximum voltage is here defined as the voltage resulting in a current density of $J=10$ A/cm^2. In Figs. 3 and 5, it is also shown that the device temperature does not affect the current density when the barrier is very thin, in agreement with that essentially temperature independent tunneling is the most dominating leakage mechanism.

In conclusion we have demonstrated experimentally that there is an optimum barrier thickness range between 10 to 14 nm that minimizes the leakage current through the device and thereby maximizes the breakdown voltage. The optimum thickness in this region depends on the applied bias voltage and device operating temperature. This experimental study shows the same behavior as was predicted in the theoretical investigation before.[4] Devices with thinner barrier layers suffer from higher leakage currents due to a higher

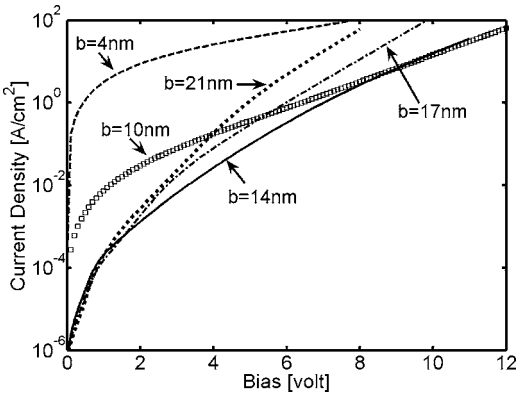

FIG. 2. Measured current density vs applied voltage for MBE1196–MBE1200 at room temperature.

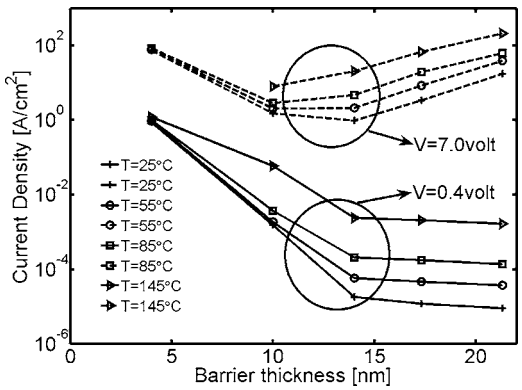

FIG. 4. Current density in two-barrier HBV diodes vs total barrier thickness at different temperatures and bias voltages.

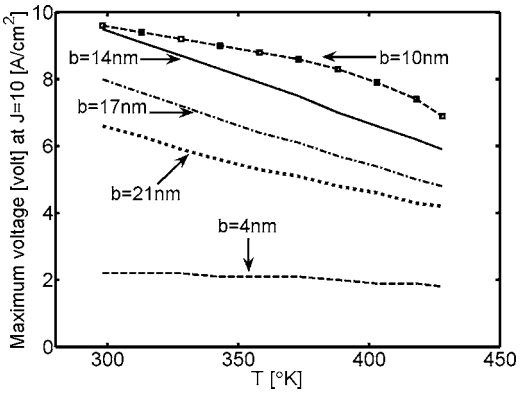

FIG. 5. Maximum voltage as a function of barrier thickness and temperature. Breakdown voltage is defined as the voltage resulting in a current density of 10 A/cm^2 through the diodes.

tunneling probability, while the effective barrier height decreases for thicker barriers because the pseudomorphic AlAs layer is not as effective anymore. This optimization needs to be taken into account especially for high-power applications.

The authors would like to thank Erik Kollberg for helpful suggestions, Gudjon Gudjonsson for help with the temperature measurements, and Jun Lu from Ångström Microstructure Laboratory for the TEM analysis. This work was supported by the Swedish Defence Research Agency, FOI, through the Nano Technology program, the Swedish Foundation for Strategic Research, SSF-HSEP, and the Swedish Micro and Nano Fabrication Network, μFab.

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