Ultra-low power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz

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***Abstract* — We present in this report an InGaAs/InAlAs/InP high electron mobility transistor (InP HEMT) with record noise temperature at very low DC power dissipation. By minimizing parasitic contact and sheet resistances, and the gate current, a 130 nm gate length InP HEMT was optimized for cryogenic low noise operation. When integrated in a 4–8 GHz three-stage hybrid low noise amplifier operating at 10 K, a noise temperature of 1.2 K ± 1.3 K at 5.2 GHz was measured. The gain of the amplifier across the entire band was 44 dB, consuming only 4.2 mW of DC power. The extracted minimum noise temperature of the InP HEMT was 1 K at 6 GHz.**

***Index Terms*—Cryogenic, InGaAs/InAlAs/InP high electron mobility transistor, InP HEMT, low noise, low power**

I. Introduction

THE best microwave noise performance is achieved with cryogenic low noise amplifiers (LNAs) based on InGaAs/InAlAs/InP high electron mobility transistors (InP HEMTs). However, reported progress in reducing noise has been slow the last decade. In [1], an average noise temperature of 1.8 K was reported for a 4-8 GHz LNA at 10 K. Such a low ambient temperature acts to strongly reduce the influence from noise sources in the InP HEMT, in particular channel noise and parasitic resistances. Normally, cryogenic LNAs are designed with InP HEMTs intended for room temperature operation. However, excellent noise performance at room temperature does not necessarily imply good noise performance at cryogenic temperature [2]. It would therefore be highly advantageous to tailor an InP HEMT technology for cryogenic operation.

In this letter we present InP HEMTs designed for cryogenic ultra-low-noise operation. The InP HEMTs have been integrated in a 4–8 GHz three-stage hybrid LNA operating at 10 K. The LNA demonstrated noise temperature and gain of 1.2 K and 44 dB, respectively, at an extremely low DC power dissipation of 4.2 mW. The average noise temperature was 1.6 K. The extracted minimum noise temperature T_{min} of the InP HEMT was 1 K at 6 GHz. To our knowledge, this represents state-of-the-art for low noise amplification at very low power dissipation.

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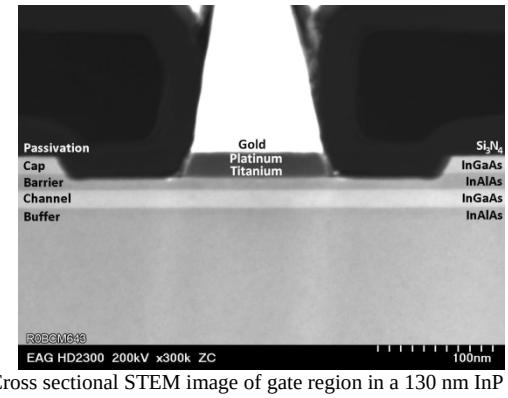

Fig. 1. Cross sectional STEM image of gate region in a 130 nm InP HEMT.

II. Device Fabrication

The epitaxial structure consisted from top to bottom of 20 nm $In_{0.53}Ga_{0.47}As$ cap layer doped to a Si concentration of $5x10^{19}$ cm^{-3}, 11 nm $In_{0.52}Al_{0.48}As$ barrier, $5x10^{12}$ cm^{-2} Si delta-doping, 3 nm $In_{0.52}Al_{0.48}As$ spacer, 15 nm $In_{0.65}Ga_{0.35}As$ channel and 250 nm $In_{0.52}Al_{0.48}As$ buffer. Hall measurements at room temperature of the structure with cap layer etched away demonstrated electron mobility and sheet carrier concentration of 11,400 cm^2/Vs and $2.8x10^{12}$ cm^{-2} respectively. The source-drain distance was 1.2 µm. A 300 nm wide gate recess was achieved with a succinic acid based solution. The gate length was 130 nm. PECVD passivation was performed at 270°C, resulting in a total Si_3N_4 thickness of 60 nm. A STEM image of the gate region, with marked epitaxial layers, is shown in Fig. 1. Compared to [3], the gate recess is relatively flat and wide.

Access resistances are key parameters in the optimization of low noise HEMTs [2]. Very low sheet resistance R_{sh} of 20 Ω/sq at 4 K and 60 Ω/sq at 300 K was obtained. Also very low ohmic contact resistance R_c, which was optimized using an annealed Au:Ge:Ni metal stack, only slightly increased from 0.03 Ω·mm at room temperature to 0.04 Ω·mm at 4 K. The resulting source and drain resistance R_s and R_d, respectively, was 0.13 Ω·mm and 0.14 Ω·mm at 4K, and 0.24 Ω·mm and 0.26 Ω·mm at 300 K. T-shaped gates enabled gate resistances of 130 Ω/mm at 4 K and 320 Ω/mm at 300 K.

III. Electrical characterization

DC and RF characterization was performed at 4 K and 300 K in a cryogenic probe station. Typical drain current I_d for 2x10 µm gate width devices are shown in Fig. 2. At 4 K, a kink is seen in the I–V characteristics at high I_d. Such behavior has been observed previously [4] when operating InP HEMTs

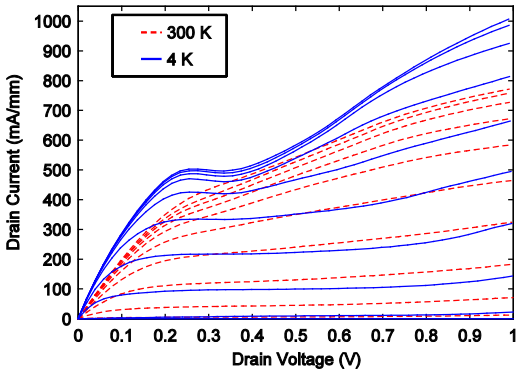

Fig. 2. Drain current of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (dashed) and 4 K (solid) ambient temperature. V_{gs} measured from -0.3 V to 0.6 V in steps of 0.1 V.

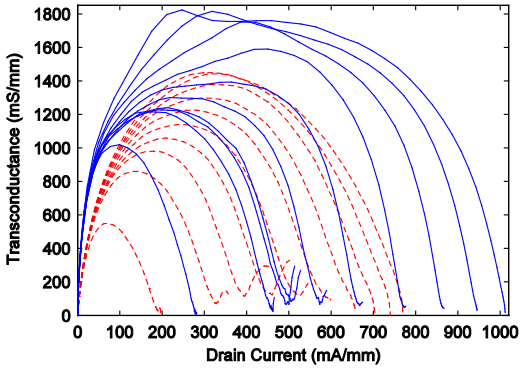

Fig. 3. Extrinsic g_m versus I_d of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (dashed) and 4 K (solid) ambient temperature. V_{ds} measured from 0.1 V to 1 V in steps of 0.1 V.

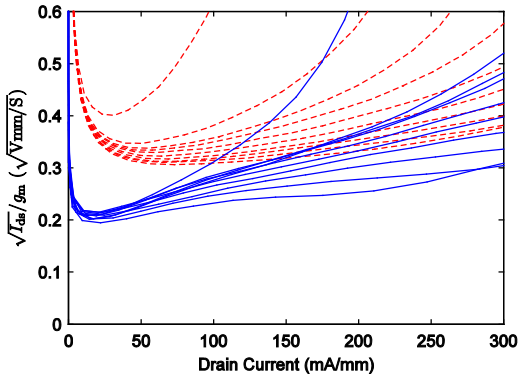

Fig. 4. $\sqrt{I_{ds}}/g_m$ versus I_d of a 2x10 µm gate width and 130-nm gate length InP HEMT at 300 K (dashed) and 4 K (solid) ambient temperature. V_{ds} measured from 0.1 V (upper curve) to 1 V (lower curve) in steps of 0.1 V.

at elevated drain currents under cryogenic conditions. Since the optimal bias of low-noise operation for the HEMT is for low I_d < 50 mA/mm, the kink phenomenon is far from the bias region of interest in this study. Maximum I_d at V_{ds} = 1 V of 1 A/mm at 4 K and 0.8 A/mm at 300 K was achieved.

A strong indicator for low noise performance in the InP HEMT is the response of DC transconductance g_m versus I_d [2]. This dependence is plotted in Fig. 3 which shows a very steep increase at low I_d. A g_m of more than 1 S/mm is observed for I_d of only 50 mA/mm at 4 K. Another way of highlighting the low-noise dependence of the InP HEMT is to plot $\sqrt{I_{ds}}/g_m$ versus I_d [2]. As seen in Fig. 4, the curves at 4 K exhibit a clear minimum which corresponds to the bias point I_d of 15 mA/mm. At this bias, the lowest noise temperature is obtained for the InP HEMT. The minimum in Fig. 4 is relatively insensitive to V_{ds} pointing to low power dissipation of the HEMT under low noise operation.

At optimum low noise bias, the InP HEMT exhibited a very low gate current density of 20 nA/mm at 4 K and 200 nA/mm at 300 K. The high breakdown voltage (off-state defined as gate-to-drain voltage at I_d = 1 mA/mm in common source), measured to 6.5 V, in combination with the very low gate current, shows that the HEMTs operate far from impact ionization.

Since the InP HEMTs display extremely low noise under cryogenic conditions, direct noise parameter measurements are very difficult and unreliable. Therefore an indirect method using an LNA was applied [1]. 4x50 µm InP HEMTs were integrated in a 3-stage hybrid 4-8 GHz LNA. The LNA was unconditionally stable at both 4 K and 300 K. Noise temperature for the LNA was measured at 10 K using a cold attenuator setup with a maximum uncertainty less than 1.3 K [5]. Repeatability of the measurement was better than 0.1 K.

The LNA noise temperature and gain as a function of frequency at 10 K for different bias points is shown in Fig. 5. At the optimum low noise bias (V_{DD} = 0.45 V, I_{DD} = 9.3 mA), a lowest noise temperature $T_{e,min}$ of 1.2 K was measured at 5.2 GHz. Across the 4-8 GHz band, the average noise temperature $T_{e,avg}$ was 1.6 K at the same bias point. Moreover, the average gain of the amplifier was 44 dB, with input and output return loss better than 15 dB, in the entire band. The total power consumption of the LNA at this bias was only 4.2 mW. When the LNA was biased for ultra-low power consumption of 0.33 mW (V_{DD} = 0.1 V, I_{DD} = 3.3 mA), the noise temperature and gain still exhibited numbers of 2.5-4.3 K and 27-34 dB, respectively. At room temperature, the measured LNA noise temperature was typically 25-30 K with a gain of 44 dB at a power consumption of 56 mW (V_{DD} = 1.25 V, I_{DD} = 45 mA). We present in Table I our results compared to previously published state-of-the art 4x50 µm InP HEMT LNAs operating at 10-15 K ambient temperature. The 4-8 GHz LNA using the InP HEMTs in this study exhibits a significantly lower $T_{e,min}$ and $T_{e,avg}$ than previously published results. Moreover, the gain per mW dissipated power is almost a factor of two higher than [6].

The uncertainty in the noise measurement is in the same range as the measured noise. To further validate the comparison, 100 nm gate length InP HEMTs with size 4x50 µm used in [1] were benchmarked against the InP HEMTs in this study using the same 4-8 GHz LNA and identical measurement procedure. The average noise temperature was in this case 2.2 K with an average gain of 39 dB at optimum low noise bias (V_{DD} = 0.6 V, I_{DD} = 10 mA). Hence 0.6±0.1 K better noise performance is obtained for the LNA based on the InP HEMTs in this study compared to the InP HEMTs used in [1].

To extract noise parameters of the InP HEMT, an equivalent small signal circuit of the transistor was made using measured S-parameters. By applying temperatures to all resistive elements in the transistor model [7], the noise temperature of the LNA could be simulated. By comparing these simulations with noise measurements in Fig. 5, an equivalent drain resistor temperature T_d = 450 K of the device was extracted.

TABLE I
DATA FOR STATE OF THE ART 4X50 μM INP HEMT LNAS AT 10-15 K

Ref.	Freq. (GHz)	$T_{e,min}$ (K)	$T_{e,avg}$ (K)	Gain/stage (dB)	Gain/power (dB/mW)
This work	4-8	1.2	1.6	14.7	10.5
[1]	4-8	1.4	1.8	13.5	2.5
[6]	4-8	3.1	3.5	13.5	6.8
[8]	4-12	3.3	4.5	11.3	-
[9]	4-12	2.7	3.5	13.7	1.7

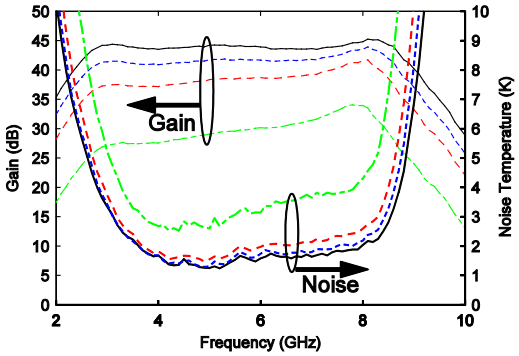

Fig. 5. Noise temperature and gain at 10 K of a three stage hybrid 4–8 GHz LNA. The 3-stage amplifier was biased at V_{DD} = 0.1 V, I_{DD} = 3.3 mA (green dash-dot); V_{DD} = 0.2 V, I_{DD} = 6 mA (red long dash); V_{DD} = 0.3 V, I_{DD} = 8 mA (blue short dash) and optimum bias V_{DD} = 0.45 V, I_{DD} = 9.3 mA (black solid).

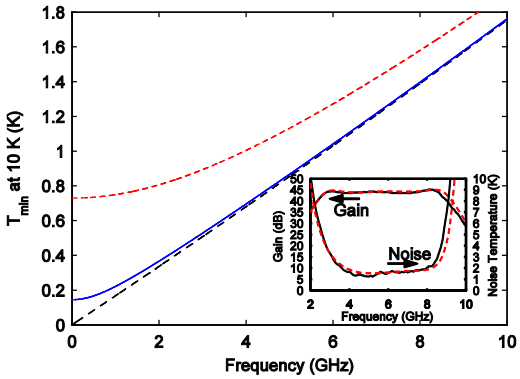

Fig. 6. Extracted T_{min} of a 4x50 μm InP HEMT exhibiting 20 nA/mm gate current at 10 K (blue solid) compared with the same device without gate current (black long dash) and with 0.5 μA/mm gate current (red short dash). The InP HEMT was biased at V_{ds} = 0.35 V and I_d = 3.1 mA. Inset shows a comparison between simulated (red dashed) and measured (black solid) noise temperature and gain of the 3-stage LNA in Fig. 5 using the extracted transistor model.

All other resistors were set to ambient temperature. The gate current was modeled with a shot noise current source using the measured DC gate current. From this model, all InP HEMT noise parameters were calculated. The extracted T_{min} at 10 K, shown in Fig. 6, was 1 K at 6 GHz.

The outstanding low noise performance of the InP HEMT is believed to be a result of the optimized gate recess resulting in both low gate current and high transconductance at low drain current. In Fig. 6 the importance of low gate current is emphasized by showing two modeled InP HEMTs either with zero gate current or with a representative gate current of 0.5 μA/mm.

IV. CONCLUSIONS

Ultra-low-noise InP HEMTs with 130 nm gate length have been designed and fabricated for cryogenic temperature operation. When integrated in a 4-8 GHz 3-stage hybrid IF LNA, a noise temperature of 1.2 K ± 1.3 K with an average gain of 44 dB and power dissipation of only 4.2 mW was measured at ambient temperature of 10 K. Extracted T_{min} of the InP HEMT was 1 K at 6 GHz.

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