# Electro-Thermal Model for Multi-Anode Schottky Diode Multipliers

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***Abstract*—We present a self-consistent electro-thermal model for multi-anode Schottky diode multiplier circuits. The thermal model is developed for an $n$-anode multiplier via a thermal resistance matrix approach. The non-linear temperature responses of the material are taken into consideration by using a linear temperature-dependent approximation for the thermal resistance. The electro-thermal model is capable of predicting the hot spot temperature, providing useful information for circuit reliability study as well as high power circuit design and optimization. Examples of the circuit analysis incorporating the electro-thermal model for a substrateless- and a membrane-based multiplier circuits, operating up to 200 GHz, are demonstrated. Compared to simulations without thermal model, the simulations with electro-thermal model agree better with the measurement results. For the substrateless multiplier, the error between the simulated and measured peak output power is reduced from ~ 13 % to ~ 4 % by including the thermal effect.**

***Index Terms*—Electro-thermal model, Gallium Arsenide, high power submillimeter-wave generation, self-heating, thermal analysis, frequency multiplier, Schottky diodes.**

## I. Introduction

PLANAR Schottky diode based frequency multipliers have been demonstrated to be promising compact and reliable sources for terahertz (THz) applications [1-3]. These terahertz applications include radio astronomy, astrophysics and earth observation applications [4-6], as well as imaging and general sensing applications [7-9]. To-date, the output power of Schottky diode based multiplier chains are in the micro-watt range for operating frequencies beyond 1 THz. For future THz science applications, this output power range is not sufficient. This generates a technological need to improve and optimize the current multiplier design towards delivering a higher output power.

At present, the initial stage of a THz multiplier chain is pumped with input power of a few hundred of milli-watts at W-band (75 GHz – 110 GHz) [5]. Intuitively, the goal of achieving a higher multiplier output power in the THz range can be realized by increasing the input power at the initial stage of the multiplier chain. Recent technological advancement in power amplifier developments has demonstrated the capability of providing power in the 1-Watt range at W-band [10]. This makes it possible to drive the initial multiplier stage at such high power. However, several phenomena that can reduce efficiency at high power, such as current saturation [11] and thermal effects [12], have been observed in varactor multipliers. Today, the major concern is the power handling capability of the multiplier chip, where the diodes degrade in performance or fail in operation due to excessive heat in the chip. This is particularly severe for multiplier chips based on Gallium Arsenide (GaAs), which has a relatively poor thermal conductivity. The chip heat sinking capability becomes worse at higher frequencies due to a smaller size of the chip geometry and the device area.

The thermal management issue has become an important aspect in the multiplier design for high power THz applications. A diode model incorporating the thermal effects on the electrical performance is needed during the circuit design stage. To-date, reports on thermal analysis and electro-thermal modeling of transistors [13-19] are abundant. Similar effort has also been performed on diodes, such as the hetero-structure barrier varactor (HBV) [20-22] and transferred electron devices (TED) [23].

For planar Schottky diodes, the electrical properties can be modeled via physics-based [24],[25] or equivalent circuit based [26],[27] approach. From the thermal perspective, a 2D heat flow model for a hybrid multiplier circuit [28] and a 'series-resistor' thermal model for the substrateless multiplier chip [12] have been presented. A systematic 3D thermal analysis on the Schottky diode based multipliers has also been reported recently [29]. However, these models are not coupled to the electrical model for self-consistent analysis. Thus, these models are limited to calculations of the junction temperatures by assuming a constant power dissipation level. In other words, a model which is capable of providing a

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quantitative estimate of the thermal effects on the electrical performance of the diode multiplier chip is not available.

The objective of this work is to develop a practical engineering approach to optimize high power THz diodes simultaneously from both the electrical and thermal perspectives. We propose a self-consistent electro-thermal diode model, for which temperature-dependent electrical parameters are updated as a function of dissipated power in each individual diode.

In this paper, layouts of the Schottky diode multiplier chips to be discussed are presented in Section II. The electro-thermal model for multipliers with $n$-number of anodes is then elaborated in Section III. In this model, the thermal resistance ($R_{th}$) network is mathematically presented as an $n \times n$ matrix. This thermal resistance matrix is extracted by solving the heat equation for a given multiplier geometry and material properties, using the 3-D finite element method (FEM). Finally, Section IV demonstrates the implementation of the electro-thermal model in circuit analysis, where harmonic-balance (HB) analyses are performed on both the substrateless- and membrane- based frequency doubler. Effects of the chip thermal characteristics on the electrical performance are discussed. The simulation result shows a better agreement with the measurement result when the thermal effects are included. This indicates the importance of implementing the self-consistent electro-thermal model for the circuit design and optimization.

## II. The Schottky Diode Chip Layout

To-date, two novel techniques for fabricating Schottky diode based multiplier chips used in the THz multiplier chain have been developed by the Jet Propulsion Laboratory (JPL), i.e. the substrateless and the monolithic membrane diode (MOMED) technologies [4],[5].

In this work, the electro-thermal model is built based on and verified by the JPL multiplier chips, as shown in Figure 1 and Figure 2. These multipliers are designed for frequency doubling operation up to 200 GHz, using a balanced architecture. The multiplier chips are seated in the waveguide channel by clamping the supporting beam leads to the waveguide wall. The input signal is coupled directly to the diodes, whereas the output signal from the diodes is coupled to the output waveguide, through the RF matching circuit and waveguide channel.

For the substrateless multiplier, the GaAs substrate underneath the RF matching circuit is removed, leaving a 50 μm thick GaAs frame for supporting the diodes. For the membrane multiplier chip, the GaAs substrate is remained under the diodes and matching circuit. However, the thickness of GaAs substrate is reduced to 5 μm for this chip. Thus, a comparison between the performances of both multipliers is essential to reveal the effect of excess heating on the electrical performance.

Although the electro-thermal model development is based on the 6-anode multiplier chip, the validity of this model is not restricted to this specific number of anodes on the multiplier chip. Similar methodology can be used to analyze general multiplier chips with a variable number of anodes as well as other chip layouts such as Schottky diode mixer chips and microstrip based monolithic microwave integrated circuits (MMICs).

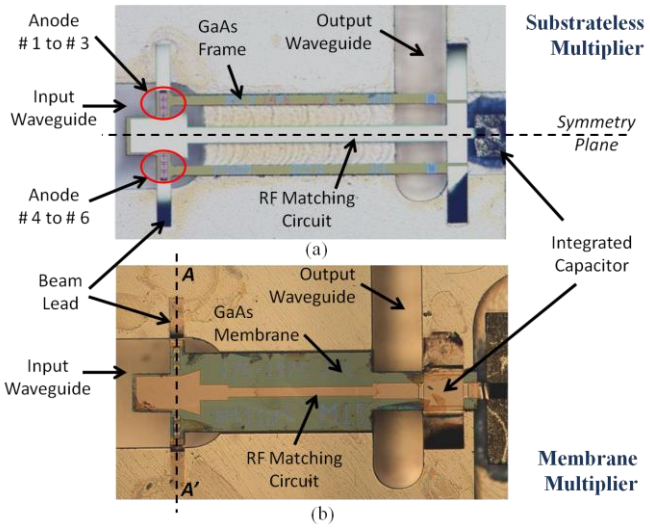


Figure 1 Top view of the multiplier chip mounted in a half-waveguide split block (a) substrateless multiplier; (b) membrane multiplier.

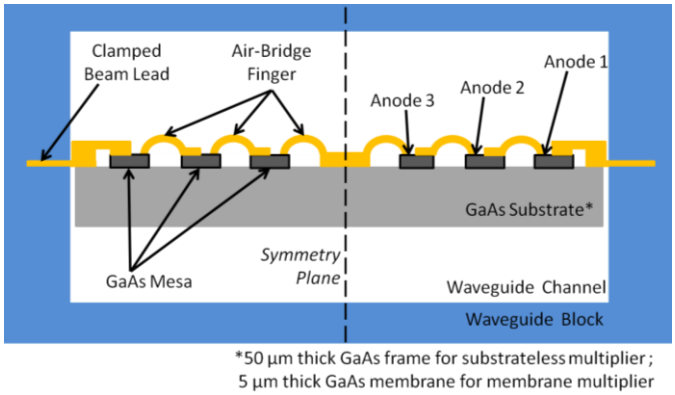


Figure 2 A schematic view of the A-A' cross section of the multiplier chip in a full waveguide block. NB! The drawing is not to scale.

## III. The Electro-Thermal Model

For frequency multiplication applications, the Schottky diodes are reverse-biased and operating as varactors [30]. Heat generation normally occurs within diode junction areas, elevating the local junction temperatures and thus modifying the temperature-dependent electrical parameters of the diode. The amount of generated heat is dynamic, depending on the high frequency input power, DC bias and current densities. The heat is then dissipated through various cooling mechanisms, such as conduction, convection and radiation.

The combined effectiveness of the cooling mechanisms is characterized by the local junction temperature elevation. In this work, only the conductive cooling mechanism is considered and the other cooling mechanisms are assumed to be negligible. Moreover, the potential uneven heat-flux distribution within the chip due to high frequency current-crowding phenomena, i.e. the skin and proximity effects [31], are not taken into account. This assumption is made considering that the electrical current conduction flows through a much smaller volume of material than the thermal

conduction. Thus, the heat flow path is determined by the physical geometry and material properties of the chip.

### A. The Single Diode Electro-Thermal Model

Figure 3 presents a self-consistent electro-thermal model for a single diode, showing the interaction between the electrical and thermal model. The electrical model provides the generated heat power to the thermal model in the form of instantaneous anode junction voltage and current ($V(t)$ and $I(t)$). The thermal model then calculates and updates the electrical model with the local junction temperature ($T^{anode}$).

In the electrical model, the diode is modeled with a current-source, $I_d$, a charge source, $Q_d$, and a series resistance, $R_s$. Temperature-dependent electrical parameters are entered to the model via analytical expressions. Using an electrical analogy approach in the thermal model, the instantaneous heat power to be dissipated ($P^{dis}$) is modeled as a current source, whereas the heat flow path is presented as a parallel connection of a thermal resistor ($R_{th}$) and a thermal capacitor ($C_{th}$).

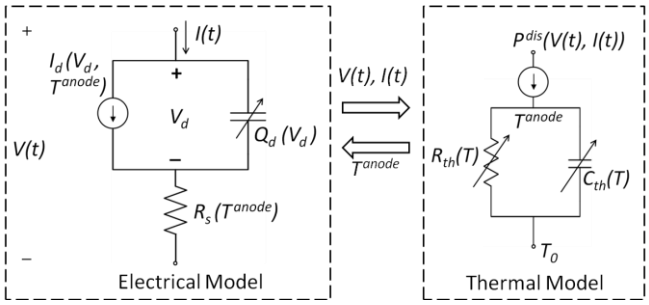


Figure 3 A self-consistent electro-thermal model for a single diode.

For multiplier applications at hundreds of gigahertz (GHz), the thermal time-constant ($\tau_{th}$) for the multiplier chip can be assumed to be much longer (i.e. in tens of milli-second range) than the period of diode operating frequency [29]. Thus, the temperatures can be assumed to be time-independent (steady-state) for a specific power dissipation level. The anode temperature is then calculated using (1), with the stationary dissipated power defined as a voltage-current multiplication.

$$T^{anode} - T_0 = R_{th}(T^{anode}) \times P^{dis} \tag{1}$$

Due to the non-linear material thermal conductivity, the thermal resistance is explicitly power dissipation level dependent. This non-linear system can be solved by approximating the thermal resistance, as a temperature-dependent function, using Taylor series. By performing a Taylor expansion around the ambient temperature ($T_0$) and only taking into consideration the linear term, the thermal resistance is approximated as (2). This approach of temperature-dependent thermal resistance treatment is proposed in the transistor electro-thermal model [14],[15].

$$R_{th}(T^{anode}) \approx R_{th}(T_0) + \frac{\partial R_{th}(T_0)}{\partial T^{anode}}\left(T^{anode} - T_0\right) \tag{2}$$

Based on this single diode electro-thermal model, the model is then further extended to the multi-anode case.

### B. The Multi-Anode Thermal Network

For the multi-anode thermal network, the thermal interactions between anodes must be considered. As shown in Figure 4, the thermal interactions between anodes are modeled as the thermal coupling network ($\mathbf{R_{th}}^{s}$) and the self-heating effects are modeled as the thermal resistances connected to the anodes ($\mathbf{R_{th}}^{anode}$). The heat sink or ambient temperature is modeled as $T_0^s$ and each anode temperature can be calculated using (3).

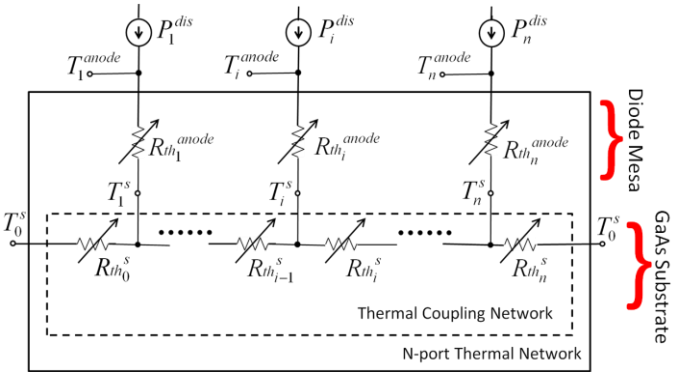


Figure 4 The thermal resistance network of an *n*-anode multiplier chip.

$$\Delta\mathbf{T} = \mathbf{T}^{\mathbf{anode}} - T_0^s = \mathbf{R_{th}}\left(\mathbf{T}^{\mathbf{anode}}\right) \times \mathbf{P}^{\mathbf{dis}} \tag{3}$$

where $\Delta\mathbf{T}$ and $\mathbf{P}^{\mathbf{dis}}$ are $n \times 1$ matrices, and $\mathbf{R_{th}}\left(\mathbf{T}^{\mathbf{anode}}\right)$ is a $n \times n$ matrix. The matrix representation of thermal resistance for junction temperature calculation is similar to that proposed for multi-finger transistors [14]. With the $n \times 1$ $\mathbf{P}^{\mathbf{dis}}$ matrix, the model is not limited to the case of equal heat power loading for all the anodes. Analysis of unequal heat power loading between anodes and potential thermal runaway cases are possible.

Analogously to the electrical circuit analysis, the *n*-port thermal network can be developed using the nodal analysis method. In this development, the thermal coupling network in the overall *n*-port thermal network is first formulated in the thermal coupling admittance matrix, $\mathbf{G_{th}}^{s}(\mathbf{T})$, written as (4). The thermal coupling resistance matrix, $\mathbf{R_{th}}^{s}(\mathbf{T})$, is then derived from the admittance matrix. Lastly, the self-heating thermal resistances are included in the final thermal resistance matrix, as in (6).

$$\mathbf{G_{th}}^{s}(\mathbf{T}) = \left[G_{th_{ij}}^{s}(\mathbf{T})\right] \tag{4}$$

$$\begin{aligned} G_{th_{ij}}^{s}(\mathbf{T}) &= G_{th_{i-1}}^{s}(\mathbf{T}) + G_{th_i}^{s}(\mathbf{T}) && \text{for } i = j \\ &= -G_{th_j}^{s}(\mathbf{T}) && = j+1 \\ &= -G_{th_i}^{s}(\mathbf{T}) && = j-1 \\ &= 0 && i < j-1;\ i > j+1 \end{aligned}$$

$$\mathbf{R_{th}}^{\mathbf{s}}(\mathbf{T}) = \left[R_{th_{ij}}^{s}(T)\right] = \left[G_{th_{ij}}^{s}(\mathbf{T})\right]^{-1} \quad (5)$$

$$R_{th_{ij}}(T) = \begin{cases} R_{th_i}^{anode}(T) + R_{th_{ij}}^{s}(T) & for\ i = j \\ R_{th_{ij}}^{s}(T) & i \neq j \end{cases} \quad (6)$$

In the multi-anode thermal model, the temperature dependency of the thermal resistance elements are addressed similar to the single anode thermal model, using the Taylor expansion approximation. By assuming negligible effects of the cross terms and high order terms in the Taylor series, the temperature dependency of the thermal resistance elements can be expressed as (7).

$$R_{th_{ij}}(T_i^{anode}) \approx R_{th_{ij}}(T_0) + \frac{\partial R_{th_{ij}}(T_0)}{\partial T_i^{anode}}\left(T_i^{anode} - T_0\right) \quad (7)$$

### C. The Thermal Resistance Matrix Extraction

In this work, the $n \times n$ thermal resistance matrix is extracted from FEM simulations using the Ansys Mechanical Simulation tool [32]. The multiplier chip 3-D layout is entered into the program and the heat flow equation is solved with appropriate thermal boundary conditions and material properties. By only considering the stationary state and conduction heat flow, the heat flow equation is simplified to the Fourier's heat law, as stated in (8).

$$\vec{q} = -\kappa(T)\overrightarrow{\nabla T} \quad (8)$$

where $\vec{q}$ is the heat flux, $\kappa(T)$ is the temperature-dependent thermal conductivity and $\overrightarrow{\nabla T}$ is the temperature gradient. The power dissipation in each anode is treated as a heat source and the thermal resistance elements are evaluated for an arbitrary chip layout and material properties.

For the GaAs-based multiplier chip analysis, the temperature-dependent GaAs thermal conductivity ($\kappa_{GaAs}$) given in equation (9) is used [33] for the temperature range in this paper.

$$\kappa_{GaAs}(T) = 50.6 \times \left(\frac{300}{T}\right)^{1.28} \quad W/m\,K \quad (9)$$

The thermal conductivity of gold is 310 W/mK, and brass is 109 W/mK. In this analysis, the effect of the passivation layer is assumed to be negligible and thus not included in the simulation. Further details on the FEM thermal simulation procedure are reported in [29]. With the above mentioned configurations, the following procedure is then performed:

i. Estimation of a reasonable power dissipation range, i.e. with the hot spot temperature kept below 500K, by applying an equal heat source on all of the anodes simultaneously in the 3D FEM simulations.
ii. Calculation of the thermal resistance elements, using (10), by performing a sequence of 3D FEM simulations for several heat source power levels.

$$R_{th_{ij}}(T_i^{anode}) = \frac{T_i^{anode} - T_0}{P_j^{dis}}\Big|_{P_k^{dis}=0, k \neq j} \quad (10)$$

iii. Extraction of the ambient temperature thermal resistance and temperature-dependent term, as defined in (7), through a series of curve-fitting procedures on the thermal resistance elements calculated from (ii).
iv. Calculation of the anode junction temperatures using (3) with the thermal resistance matrix extracted from (iii).
v. Comparison of the temperatures simulated from (i) and those calculated from (iv) for a range of specific power dissipation levels.

Examples of the formulation and implementation of the self-consistent electro-thermal model in circuit analysis are shown in Section IV.

## IV. Example Of Circuit Analysis Implementation

This section shows an example of a harmonic balance analysis of a 6-anode 200 GHz frequency doubler chip using the developed self-consistent electro-thermal model. In this example, the electro-thermal model is implemented using the symbolically defined device (SDD) component available in the Agilent Design System (ADS) microwave circuit simulator [34].

### A. The Schottky Diode Varactor Electrical Model

The electrical model of a Schottky diode varactor is shown in Figure 3. For the SDD component implementation, the voltage-dependent current source, voltage-dependent charge source and losses through the series resistance are specified similarly to those in the generic diode model in ADS [34]. The varactor diode electrical and device parameters for the frequency doubler chip are summarized in TABLE I.

TABLE I
DIODE ELECTRICAL AND DEVICE PARAMETERS AT 300 K

| Parameter | Symbol | Substrateless Multiplier | Membrane Multiplier |
|---|---|---|---|
| Thermal voltage (mV) | $V_T$ | 25.8 | 25.8 |
| Diode ideality factor | $\eta$ | 1.2 | 1.14 |
| Reverse saturation current (A) | $I_s$ | 6.7 x $10^{-14}$ | 1.6 x $10^{-13}$ |
| Zero-biased junction capacitance (fF) | $C_{j0}$ | 59 | 64 |
| Forward-biased depletion capacitance coefficient | $\alpha$ | 0.5 | 0.5 |
| Barrier height (eV) | $\emptyset_b$ | 0.85 | 0.85 |
| Series resistance ($\Omega$) | $R_s$ | 3.2 | 3.5 |
| Anode contact area ($\mu m^2$) | $A$ | 52.5 | 40.25 |
| Epilayer doping concentration ($cm^{-3}$) | $N_d$ | 1 x $10^{17}$ | 2 x $10^{17}$ |

In general, several electrical device parameters are dependent on the anode junction temperature. For the operating condition in this example, the analyzed temperature-dependent electrical parameters are limited to $V_T$, $I_s$ and $R_s$, as stated in (11) to (13). Other temperature-dependent electrical parameters can be entered to the model if required.

$$V_T(T) \propto T \tag{11}$$

$$I_s(T) \propto T^2 \times \exp\left(\frac{-\phi_b}{V_T}\right) \tag{12}$$

$$\begin{aligned} R_s(T) &= R_{epi}(T) + R_{spreading}(T) + R_{contact} + R_{finger} \\ &\approx \chi\, R_s(T) + (1-\chi) R_s \\ &\approx \chi\, R_s(T = 300\,K) \times \left(\frac{T}{300\,K}\right)^{0.89} + (1-\chi) R_s \end{aligned} \tag{13}$$

For the planar diode, the series resistance is comprised of several resistive components, as in (13). Among these components, the ohmic contact resistance ($R_{contact}$) and air-bridge finger resistance ($R_{finger}$) are assumed to be temperature independent. Only the epi-layer resistance ($R_{epi}$) and spreading resistance ($R_{spreading}$) are temperature-dependent. In this work, it is assumed that the temperature-dependent part of the epi-layer resistance is similar to that of the spreading resistance. The temperature-dependent resistance proportions, $\chi$, are approximately 40% and 30% of the total series resistance for the substrateless multiplier chip and membrane multiplier chip, respectively. The temperature-dependent empirical low-field mobility model developed by M. Sotoodeh [35] is used to scale the temperature-dependent series resistance. For a temperature range within 300 K to 500 K, which is generally a reasonable device operation range, the series resistance exhibits temperature dependency as in (13).

### *B. The Frequency Doubler Chip Thermal Model*

In order to extract the thermal resistance matrix, the procedure presented in Section III.C is performed. For a 6-anode multiplier chip, the order of the thermal resistance matrix required for analysis is six. For a thorough thermal investigation, including thermal run-away study, a 6 x 6 thermal resistance matrix is required. However, for a normal multiplier operation, the power dissipation and temperature at anode *i* is assumed to be the same as those at anode (*n*+1-*i*), due to the symmetry property of the balanced topology (see Figure 2). Thus, the thermal resistance matrix can be simplified to a 3 x 3 thermal resistance matrix.

#### *1) The Reasonable Operating Power Range*

The reasonable range of operating power levels for both multipliers are estimated by performing FEM simulations with equal power dissipation levels on all the anodes. Due to the chip symmetry property, it is sufficient to solve the 3D FEM heat equation in half of the chip domain. In this analysis, the maximum reasonable power dissipation level is estimated to be approximately 30 and 12 mW per anode for the substrateless multiplier chip and membrane multiplier chip, respectively.

#### *2) The Thermal Resistance Matrix Elements*

Upon identifying the power dissipation range, the thermal resistance elements are calculated from a sequence of single heat source FEM simulations, as described in step (ii), for several power levels. Due to the symmetry in the FEM simulations, the extracted thermal resistance elements represent the resistance as if the sources at anode *i* and anode (*n*+1-*i*) are turned-on at the same time.

The thermal resistance elements, calculated as a function of power dissipation level, are then analyzed as a function of anode temperature. The thermal resistances at ambient temperature and the temperature-dependent coefficients, as stated in (7), are then extracted through a linear curve-fitting procedure. Figure 5 shows the temperature dependencies of the diagonal thermal resistance elements for both multiplier chips as well as the corresponding fitted curves. The extractions show good agreements using the linear temperature-dependent thermal resistance approximations. The extracted thermal resistance matrices for the substrateless and membrane multiplier chip are written in (14) and (15), respectively.

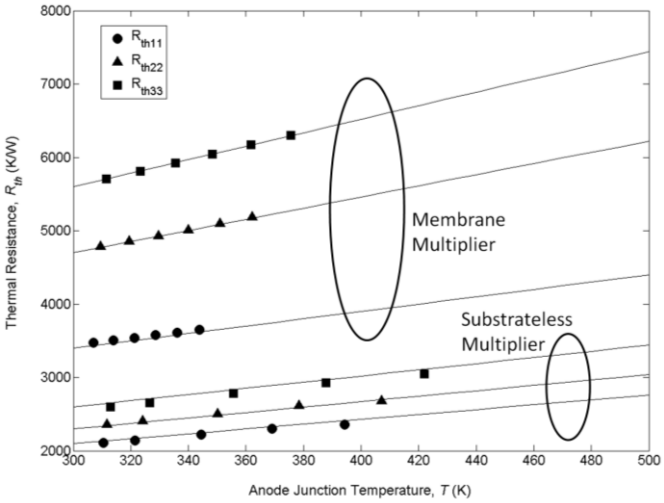


Figure 5 The temperature dependency of diagonal thermal resistance elements in the single heat source cases. The markers show the temperatures acquired from the FEM simulations at power level of 5, 10, 20, 30 and 40 mW for the substrateless multiplier, and 2, 4, 6, 8, 10 and 12 mW for the membrane multiplier. The solid lines show the corresponding fitted-curves.

$$\mathbf{R_{th}}\left(\mathbf{T^{anode}}\right) = \begin{bmatrix} 2100+3.3\left(T_1^{anode}-300\right) & 1100+1.6\left(T_1^{anode}-300\right) & 1100+1.4\left(T_1^{anode}-300\right) \\ 1000+1.4\left(T_2^{anode}-300\right) & 2300+3.7\left(T_2^{anode}-300\right) & 1300+2.1\left(T_2^{anode}-300\right) \\ 1000+1.4\left(T_3^{anode}-300\right) & 1300+2.0\left(T_3^{anode}-300\right) & 2600+4.2\left(T_3^{anode}-300\right) \end{bmatrix}$$

$\left[{}^{K}\!/_{W}\right]$ for substrateless multiplier chip (14)

$$\mathbf{R_{th}}\left(\mathbf{T^{anode}}\right) = \begin{bmatrix} 3400+5.0\left(T_1^{anode}-300\right) & 2500+3.3\left(T_1^{anode}-300\right) & 2400+3.0\left(T_1^{anode}-300\right) \\ 2400+2.9\left(T_2^{anode}-300\right) & 4700+7.6\left(T_2^{anode}-300\right) & 3600+5.7\left(T_2^{anode}-300\right) \\ 2300+2.6\left(T_3^{anode}-300\right) & 3500+5.6\left(T_3^{anode}-300\right) & 5600+9.2\left(T_3^{anode}-300\right) \end{bmatrix}$$

$\left[{}^{K}\!/_{W}\right]$ for membrane multiplier chip (15)

*3) The Thermal Model Verification*

For model verification, the anode junction temperatures with equal power, up to the maximum reasonable power dissipation level, on all the anodes are calculated using (3). These calculated temperatures are then compared to those acquired from FEM simulations. The result shows a good agreement of the anode temperatures acquired from both methods (see Figure 6). This indicates that the temperature-dependent thermal resistance, by only considering Taylor series expression up to first order term, is adequate in solving the non-linear problem for both multipliers.

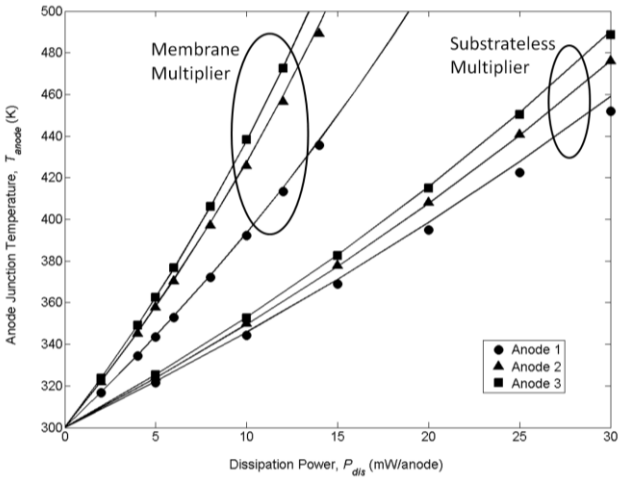


Figure 6 Comparisons of the anode temperatures calculated using the temperature-dependent thermal resistance matrix multiplication method and FEM simulation. The markers show the FEM simulated temperatures, whereas the solid lines show the corresponding calculated temperatures.

## C. The Harmonic Balance Simulation

For the harmonic balance simulation, the RF input power is swept from 0 mW to 180 mW at the pumping frequency of 99.5 GHz for the substrateless multiplier and 90 GHz for the membrane multiplier. The DC bias voltage is optimized for each RF power level in the electrical model. A similar optimized bias voltage is then applied in the electro-thermal simulation. Since the thermal time constant is much larger than one cycle of the input frequency, a thermal capacitance of 1 nW•s/K is added in parallel to all the thermal resistance elements in the model.

The analysis includes frequency harmonics up to the 8$^{th}$ order of the fundamental frequency. The input and output frequency matching circuits are implemented using scattering parameters (S-parameters), which are acquired from 3D FEM full wave simulations. Harmonics at higher frequencies are shorted to ground. For the substrateless multiplier, the input and output waveguide losses are 0.3 dB and 0.1 dB, respectively. On the other hand, both the input and output waveguides are simulated with losses of 0.1 dB for the membrane multiplier. Conductor losses for the matching circuits are taken into account in the 3D EM simulation.

Figure 7 shows the predicted temperatures of each anode as a function of RF input power for both multipliers, where the hot spots are identified to be at anode 3. Comparing with the substrateless multiplier, the rise in temperature is more significant for the membrane multiplier, as the consequence of a thinner GaAs substrate. For an RF input power of 100 mW, a temperature-rise of 43 K and 120 K is predicted for the substrateless and membrane multiplier, respectively.

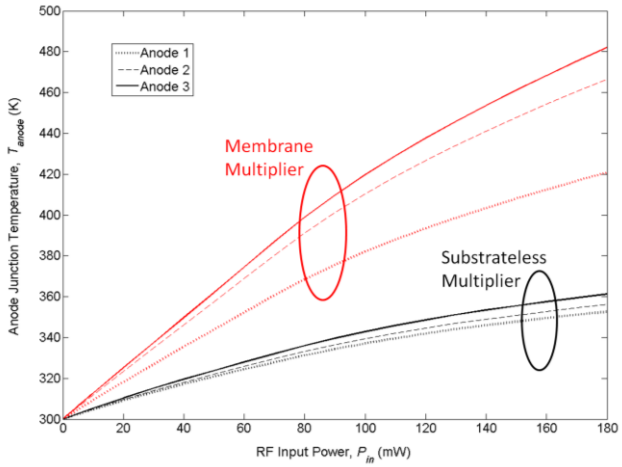


Figure 7 The estimated anode junction temperatures as a function of the RF input power.

A comparison of the circuit electrical performance, with and without thermal model, is shown in Figure 8. Benchmarking the simulation result with the measurement result shows that a better agreement is achieved by taking into consideration of the thermal effect. The result shows that the thermal effect is negligible for a lower input power range, e.g. 40 mW. There is no significant difference in the simulation results with and without the thermal model. For input power beyond 40 mW, the result shows that the electro-thermal model provides a better estimate of the multiplier performance.

For the substrateless multiplier, a very good agreement between the measurement and electro-thermal simulation result is achieved. For an input power of 150 mW, the measured output power is 34.5 mW. The error in output power estimation is ~ 4 % and ~ 13 % for the electro-thermal model and electrical model, respectively. Compared to the substrateless multiplier analysis, the membrane multiplier analysis shows more discrepancy between the simulated and measured circuit performance. For the electro-thermal model, the overestimation of the output power is ~ 17 % for the case of a 100 mW input power. This discrepancy can be attributed to the underestimated thermal resistance of the membrane multiplier.

Without considering the thermal effect, the electrical performance of the membrane multiplier is expected to be better than the substrateless multiplier. The maximum conversion efficiency is predicted to be 27% at an input power of 110 mW for the membrane multiplier, and 26% at an input power of 130 mW for the substrateless multiplier. However, due to a more significant thermal effect on the membrane multiplier, the maximum efficiency is reduced to 23% and the RF input power for peak efficiency is down-shifted to 90 mW.

Figure 8 (c) and (d) shows the instantaneous current-voltage ($I(t)$–$V(t)$) characteristic for the hottest diode, i.e. diode 3. The thermal effect on the current-voltage characteristic is also illustrated in this figure. For a RF input power of 150 mW, the diode currents in both multipliers

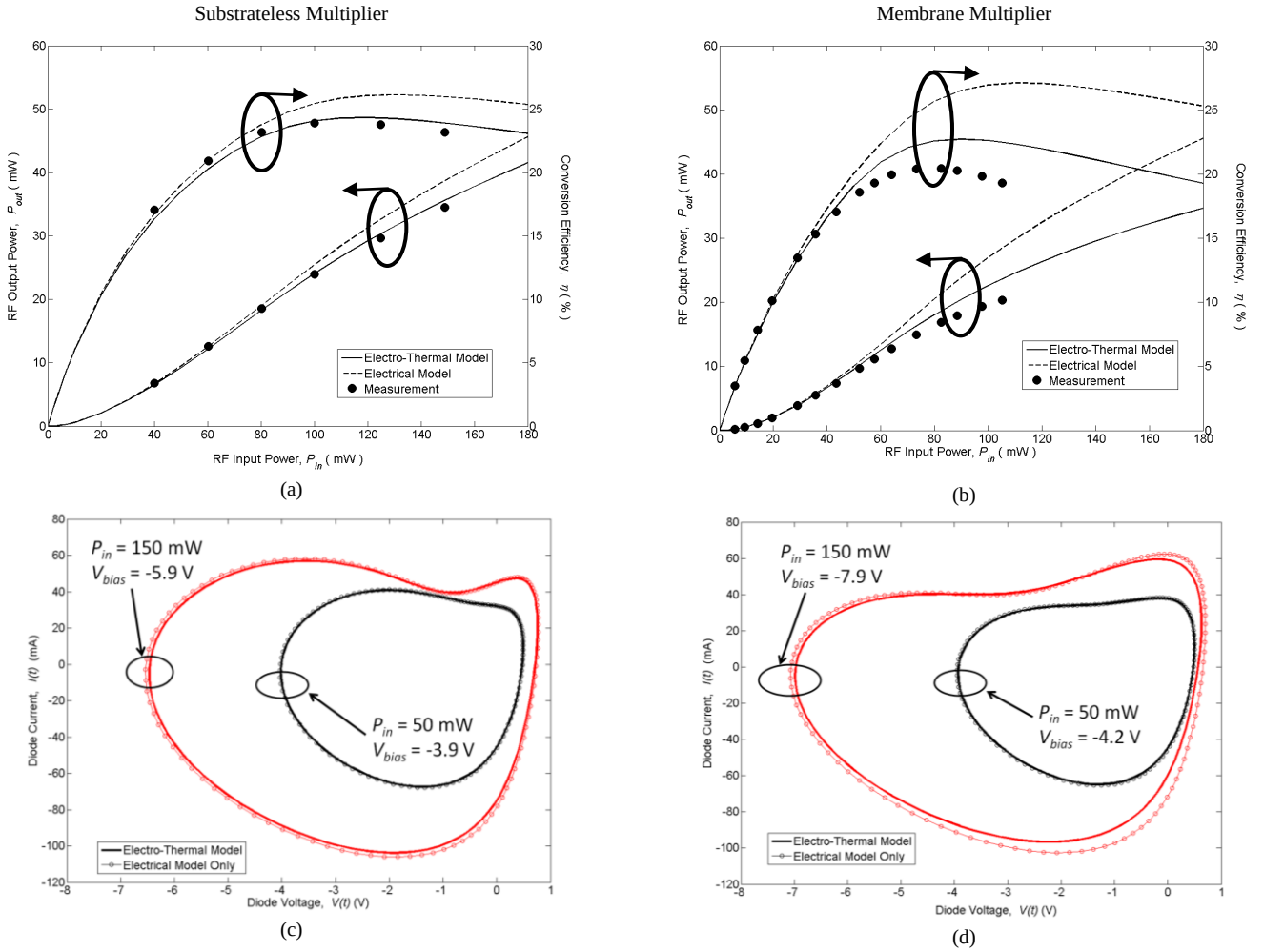


Figure 8 (a) and (b) A comparison of the RF output power and the flange-to-flange efficiency between simulation and measurement for both multiplier chips; (c) and (d) Thermal effect on the instantaneous current and voltage characteristics for diode 3.

are less than 120 mA. The current saturations due to electron velocity saturation effect [11] are calculated to be approximately 180 mA and 280 mA for the substrateless and membrane multiplier, respectively. The peak calculated current for the substrateless multiplier is 104 mA and the peak calculated velocity is ~ 12 x $10^6$ cm/s. Thus, it can be concluded that the multiplier performance is not limited by the current saturation effect up to the input power of 150 mW.

This analysis reveals the impact of the thermal management on the electrical performance for high power applications. Thus, the self-consistent electro-thermal model is an essential tool for circuit analysis towards optimizing the chip design from both electrical and thermal aspects.

## V. Conclusion

In this work, we have developed a self-consistent electro-thermal model for a multi-anode Schottky-based multiplier chip. The methodology and implementation of the model presented is straightforward and yet effective to incorporate the nontrivial thermal effects on the electrical performance. The incorporation of this model in the circuit analysis is beneficial for multiplier chip design and further design optimization.

Although the electro-thermal model is developed for the steady-state cases (i.e. continuous wave applications) of high frequency Schottky diode operations, the model can be further extended to pulsed-RF applications. For applications where the diode operating period is comparable to the thermal time-constant, a similar model can be implemented by incorporation of proper thermal capacitances in the thermal network. In addition, the model can also be extended to cover diode chip topologies required for array receivers.

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## References

[1] P. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, 2002, pp. 910-928.

[2] T. Crowe, W. Bishop, D. Porterfield, J. Hesler, and R. Weikle, "Opening the terahertz window with integrated diode circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, 2005, pp. 2104-

2110.
[3] G. Chattopadhyay, "Technology, Capabilities, and Performance of Low Power Terahertz Sources," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, 2011, pp. 33-53.
[4] S. Martin, B. Nakamura, A. Fung, P. Smith, J. Bruston, A. Maestrini, F. Maiwald, P. Siegel, E. Schlecht, and I. Mehdi, "Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes," *IEEE MTT-S International Microwave Symposium Digest, 20-25 May 2001*, Piscataway, NJ, USA: IEEE, 2001, pp. 1641-1644.
[5] G. Chattopadhyay, E. Schlecht, J. Ward, J. Gill, H. Javadi, F. Maiwald, and I. Mehdi, "An all-solid-state broad-band frequency multiplier chain at 1500 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, 2004, pp. 1538-1547.
[6] A. Maestrini, B. Thomas, H. Wang, C. Jung, J. Treuttel, Y. Jin, G. Chattopadhyay, I. Mehdi, and G. Beaudin, "Schottky diode-based terahertz frequency multipliers and mixers," *Comptes Rendus Physique*, vol. 11, Aug. 2010, pp. 480-495.
[7] D. Woolard, R. Brown, M. Pepper, and M. Kemp, "Terahertz Frequency Sensing and Imaging: A Time of Reckoning Future Applications?," *Proceedings of the IEEE*, vol. 93, 2005, pp. 1722-1743.
[8] D. L. Woolard, W. R. Loerop, and M. Shur, *Terahertz Sensing Technology:Emerging Scientific Applications & Novel Device Concepts*. Singapore: World Scientific, 2004.
[9] K. Cooper, R. Dengler, N. Llombart, T. Bryllert, G. Chattopadhyay, E. Schlecht, J. Gill, C. Lee, A. Skalare, I. Mehdi, and P. Siegel, "Penetrating 3-D Imaging at 4- and 25-m Range Using a Submillimeter-Wave Radar," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, 2008, pp. 2771-2778.
[10] M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, M. Hu, A. Corrion, A. Fung, R. Lin, L. Samoska, P. Kangaslahti, B. Lambrigtsen, P. Goldsmith, W. Wong, A. Schmitz, P. Hashimoto, P. Willadsen, and D. Chow, "W-Band GaN MMIC with 842 mW output power at 88 GHz," *IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2010, pp. 237-239.
[11] E. Kollberg, T. Tolmunen, M. Frerking, and J. East, "Current saturation in submillimeter-wave varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, 1992, pp. 831-838.
[12] E. Schlecht, G. Chattopadhyay, A. Maestrini, D. Pukala, J. Gill, S. Martin, F. Maiwald, and I. Mehdi, "A high-power wideband cryogenic 200 GHz Schottky 'substrateless' multiplier: Modeling, design and results," *Proceedings of the Ninth International Conference on Terahertz Electrons*, Charlottesville, VA, USA: 2001, pp. 485-494.
[13] P. Baureis, "Electrothermal modeling of multi-emitter heterojunction-bipolar-transistors (HBTs)," *Third International Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits*, 1994, pp. 145-148.
[14] C. Snowden, "Large-signal microwave characterization of AlGaAs/GaAs HBT's based on a physics-based electrothermal model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, 1997, pp. 58-71.
[15] D.J. Walkey, T.J. Smy, T. Macelwee, and M. Maliepaard, "Compact representation of temperature and power dependence of thermal resistance in Si, Inp and GaAs substrate devices using linear models," *Solid-State Electronics*, vol. 46, Jun. 2002, pp. 819-826.
[16] N. Nenadovic, S. Mijalkovic, L. Nanver, L. Vandamme, V. d'Alessandro, H. Schellevis, and J. Slotboom, "Extraction and modeling of self-heating and mutual thermal coupling impedance of bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol. 39, 2004, pp. 1764-1772.
[17] J. Higgins, "Thermal properties of power HBT's," *IEEE Transactions on Electron Devices*, vol. 40, 1993, pp. 2171-2177.
[18] J. Wilson and K. Decker, "GaAs MMIC thermal modeling for channel temperatures in accelerated life test fixtures and microwave modules," *Proceedings of IEEE/CPMT 10th Semiconductor Thermal Measurement and Management Symposium*, 1994, pp. 121-128.
[19] D. Dawson, "Thermal modeling, measurements and design considerations of GaAs microwave devices," *Technical Digest 16th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, 1994, pp. 285-290.
[20] J. Stake, L. Dillner, S. Jones, C. Mann, J. Thornton, J. Jones, W. Bishop, and E. Kollberg, "Effects of self-heating on planar heterostructure barrier varactor diodes," *IEEE Transactions on Electron Devices*, vol. 45, 1998, pp. 2298-2303.
[21] M. Ingvarson, J. Vukusic, A. Oistein Olsen, Arezoo Emadi T, and J. Stake, "An electro-thermal HBV model," *IEEE MTT-S International Microwave Symposium Digest*, 2005, p. 3.
[22] M. Ingvarson, B. Alderman, A. Olsen, J. Vukusic, and J. Stake, "Thermal constraints for heterostructure barrier varactors," *IEEE Electron Device Letters*, vol. 25, 2004, pp. 713-715.
[23] M. Zybura, S. Jones, G. Tait, and J. Duva, "Efficient computer aided design of GaAs and InP millimeter wave transferred electron devices including detailed thermal analysis," *Solid-State Electronics*, vol. 38, Apr. 1995, pp. 873-880.
[24] J. Grajal, V. Krozer, E. Gonzalez, F. Maldonado, and J. Gismero, "Modeling and design aspects of millimeter-wave and submillimeter-wave Schottky diode varactor frequency multipliers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, 2000, pp. 700-711.
[25] J. Siles and J. Grajal, "Physics-Based Design and Optimization of Schottky Diode Frequency Multipliers for Terahertz Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, 2010, pp. 1933-1942.
[26] J.L. Hesler, "Planar Schottky diodes in submillimeter-wavelength waveguide receivers," University of Virginia, 1996.
[27] T. Kiuru, J. Mallat, A. Raisanen, and T. Narhi, "Schottky Diode Series Resistance and Thermal Resistance Extraction From S - Parameter and Temperature Controlled I–V Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, 2011, pp. 2108-2116.
[28] D. Porterfield, "Millimeter-Wave Planar Varactor Frequency Doublers," University of Virginia, 1998.
[29] A.Y. Tang, E.T. Schlecht, G. Chattopadhyay, R.H. Lin, C. Lee, J. Gill, I. Mehdi, and J. Stake, "Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes," *Proc of 22nd International Symposium on Space Terahertz Technology*, Tucson, Arizon: 2011.
[30] A. Uhlir, "The Potential of Semiconductor Diodes in High-Frequency Communications," *Proceedings of the IRE*, vol. 46, 1958, pp. 1099-1115.
[31] A.Y. Tang and J. Stake, "Impact of Eddy Currents and Crowding Effects on High-Frequency Losses in Planar Schottky Diodes," *IEEE Transactions on Electron Devices*, vol. 58, 2011, pp. 3260-3269.
[32] *ANSYS Mechanical*, ANSYS Inc, Southpointe, 275 Technology Drive, Canonsburg, PA 15317, USA.
[33] S. Adachi, *Properties of group-IV, III-V and II-VI semiconductors*, John Wiley and Sons, 2005.
[34] *Advanced Design System 2009*, Agilent Technologies, 395, CA 94304 USA.
[35] M. Sotoodeh, A.H. Khalid, and A.A. Rezazadeh, "Empirical low-field mobility model for III–V compounds applicable in device simulation codes," *Journal of Applied Physics*, vol. 87, 2000, p. 2890.

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