A SiC Varactor with Large Effective Tuning Range for Microwave Power Applications

Christer M. Andersson, Niclas Ejebjörk, Anne Henry, Sven Andersson, Erik Janzén, Herbert Zirath *Fellow, IEEE*, and Niklas Rorsman, *Member, IEEE*

***Abstract*—SiC Schottky diode varactors have been fabricated for use in microwave power applications, specifically the dynamic load modulation (DLM) of power amplifiers (PAs). A custom doping profile has been employed to spread the C(V) over a large bias voltage range, thereby increasing the effective tuning range under large voltage swing conditions. The small-signal tuning range is approximately 6 and punch-through is reached at a bias voltage of -60 V, while the breakdown voltage is in the order of -160 V. An interdigitated layout is utilized together with a self-aligned Schottky anode etch process to improve the Q-factor at 2 GHz, which is 20 at zero bias and approximately 160 at punch-through.**

***Index Terms*—SiC, Schottky diodes, varactors, self-aligned, interdigitated, tuning range, power amplifiers, load modulation**

I. Introduction

THE future demand for high data rate wireless communication services pushes the development of novel power amplifier (PA) architectures. Dynamic load modulation (DLM) has for instance been demonstrated as a method to improve PA energy efficiency in the transmission of modern communication signals with high peak-to-average ratios [1]. Varactors are a central component in the realization of DLM architectures, but there is a lack of commercial varactor solutions specifically designed to support both high effective tuning range and high power operation.

We have previously reported on SiC Schottky diodes for use in microwave applications [2], [3]. SiC is a wide bandgap material that can withstand high electrical fields [4], and has a mobility suitable for high frequency devices. Special varactor design considerations are required to support applications featuring high power levels. The effective tuning range of varactor diodes decreases with the voltage swing, as the forward conduction and breakdown regions must be avoided [5]. In [3] the focus was specifically on fabricating varactors for use in the DLM of PAs. An effort was therefore made to linearize the C(V), improve the effective tuning range, and support a high breakdown voltage by a custom doping profile. Increasing the effective tuning range by a custom doping profile has also been reported in GaAs technology [6]. Recently a wide bandgap GaN varactor capable of handling high voltages was reported [7].

In this work further efforts have been made to improve the voltage handling of SiC varactors. Through improved doping profile design both the breakdown voltage and effective tuning range have been significantly improved compared to [3]. Fabricating the devices in a planar interdigitated self-aligned process has also contributed to a simultaneous improvement in Q-factor.

II. Epitaxial Design and Growth

Based on requirements for a specific DLM application the epitaxial doping profile was optimized by numerical methods with the goal of distributing the C(V) over a large bias range while simultaneously maintaining a high breakdown voltage and Q-factor. The nominal C(V) resulting from the optimization process was a cubic function, smoothly leveling out before punch-through to reduce higher order harmonic generation from a derivative discontinuity. Similar to [6] a low doped spacer layer was used as a design parameter. The breakdown voltage was however purposely designed, at the cost of higher series resistance, to be significantly larger than the punch-through voltage. In proper DLM network design the peak PA output power and largest varactor voltage swing occurs when the varactor is biased for minimum capacitance. The designed C(V) allows for large voltage swing operation in the saturated/linear C(V) region where the Q-factor is the highest and the power loss to harmonic generation is small.

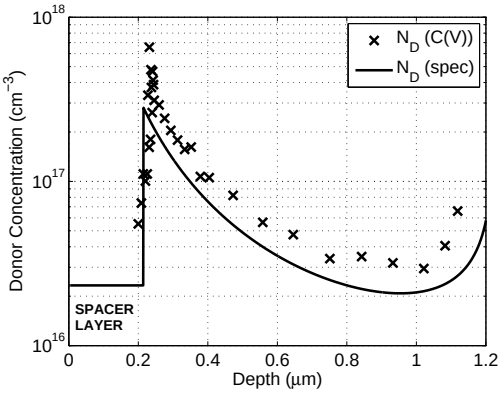

Fig. 1. Donor doping concentration (N_D) extracted from C(V) measurements, compared to the doping profile specification.

This research has been carried out in the Microwave Wide Bandgap Technology project financed by Swedish Governmental Agency of Innovation Systems (VINNOVA), Swedish Energy Agency (STEM), Chalmers University of Technology, Ericsson AB, Furuno Electric Co., Ltd., Infineon AG, Norse Semiconductor Laboratories AB, Norstel AB, NXP Semiconductors BV, and Saab AB.

C. M. Andersson, N. Ejebjörk, H. Zirath, and N. Rorsman are with the Microwave Electronics Laboratory at Chalmers University of Technology, SE-412 96 Göteborg, Sweden (e-mail: christer.m.andersson@chalmers.se).

A. Henry, S. Andersson, and E. Janzén are with the Department of Physics and Measurement Technology, Biology and Chemistry, Linköping University, 581 83 Linköping, Sweden.

Without the need to reduce the reverse bias to avoid breakdown at large voltage swing, the dynamic range of the DLM network remains constant. Linearity was not addressed in the C(V) design, as digital predistortion has successfully been shown capable of linearizing a highly nonlinear PA incorporating DLM [1].

The devices were fabricated in a planar process. The epitaxy was performed on a semi-insulating 4H-SiC Si-face 8° off c-axis substrate from Cree, Inc. Nitrogen was used for n-type doping and the doping profile specification is shown in Fig. 1. From bottom and up the nominal epitaxial structure consisted of a 1 μm highly doped ($\approx 1{\cdot}10^{19}$ cm^{-3}) access layer, a 1 μm graded depletion layer (from $2{\cdot}10^{16}$ to $3{\cdot}10^{17}$ cm^{-3}), and a 220 nm low doped spacer layer ($\approx 2{\cdot}10^{16}$ cm^{-3}). Correct choice of the spacer layer doping ensures complete depletion of the layer by the built-in junction voltage.

The epilayer growth was done in a horizontal hot-wall CVD reactor [8]. The growth temperature was 1560°C and the pressure 200 mbar. The Si and C sources were silane and propane with a mixture of hydrogen and argon as a carrier gas (4% of Ar in H_2). The epi-structure was grown in two steps. The highly doped layer was first grown with a C/Si ratio of 0.8 and a low growth rate of 2 μm/h. A baking of the susceptor followed to assure that the net background n-type level came down to the low 10^{14} cm^{-3} range. The graded depletion layer as well as the low doped spacer layer were grown during a second run with a C/Si ratio of 1 and a growth rate of 3 μm/h with a special schema for the flow of N_2 gas.

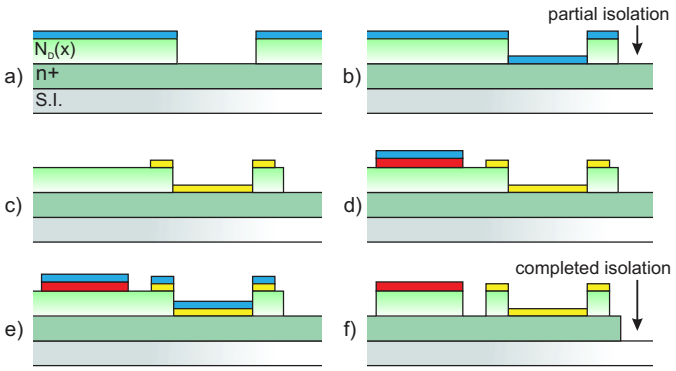

Fig. 2. Schematic fabrication process steps: a) ohmic contact recessing, b) partial device isolation, c) ohmic contact definition, d) Schottky contact definition, e) ohmic contact protection, f) self-aligned etching.

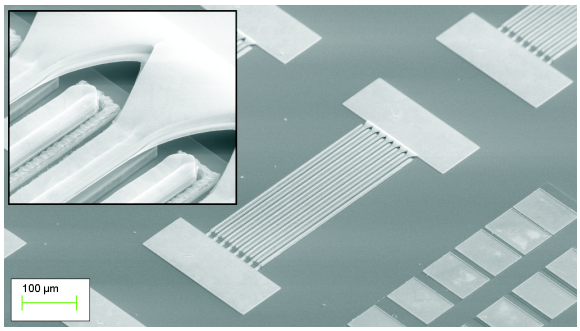

Fig. 3. SEM image of multi-finger devices featuring 7 anode fingers and a minimum capacitance of 1 pF, to be diced and mounted into hybrid circuits. The inset shows a close-up of the anode air-bridges.

III. Fabrication

Schematic illustrations of the main fabrication steps are shown in Fig. 2. Photolithography was used for all pattern transfer processes. Definition of the ohmic contact recesses was done by ICP etching using a Ni mask. A subsequent Ni masked etching step commenced the device isolation. Ohmic cathode contacts were defined by evaporation of Ni, followed by annealing at 1000°C for 5 min in an Ar atmosphere. TLM measurements yielded an ohmic contact resistance of 0.5 Ωmm. Schottky contacts (Ti/Pt/Au/Ni) were evaporated after removal of native oxide. A Ni layer was evaporated on top of the ohmic contacts as a protective etch mask. ICP etching of the entire chip produced self-aligned Schottky anode mesas, while simultaneously completing the device isolation. The pad and interconnect metallization was done by evaporation of Ti/Au. Electroplating of 3 μm gold defined electrodes and anode air-bridges. Finally, gold was sputtered on the backside of the chip.

The nominal layout for a single finger device consisted of a 5 μm wide and 400 μm long Schottky anode contact with two adjacent 10 μm wide ohmic cathode contacts at a contact spacing of 4 μm. A parallel connection of such single finger unit-cells, sharing adjacent ohmic contacts, were used to form larger multi-finger devices as shown in Fig. 3. To improve the area utilization coplanar ground planes, to facilitate on-wafer characterization, were only added to the single finger devices.

IV. Characterization

DC measurements (Keithley 4200) showed typical device breakdown voltages in the range of -150 to -170 V, corresponding to estimated peak electric fields of 2.1 to 2.3 MV/cm. This is comparable to the critical electric field in 4H-SiC (2.5 MV/cm at N_D=10^{16} cm^{-3}) [4]. For a few of the devices breakdown did not occur when biased to -200 V (estimated 2.5 MV/cm). For the best devices the leakage current at -100 V remained below 0.1 A/cm^2. In the forward direction the voltage-current slopes were close to 60 mV/decade, with a high DC on-resistance due to the low doped spacer layer. The I(V) for a single finger device is shown in Fig. 4.

To extract the single finger device characteristics a vector network analyzer (VNA, Agilent E8361A) was used to measure S-parameters from 0.1 to 40 GHz for bias voltages from 0 to -100 V. The resulting C(V) and Q-factors are shown in Fig. 5. At zero-bias and 2 GHz the capacitance is 0.92 pF (0.46 fF/μm^2) and the Q-factor 20 (Q_{min}). The small-signal tuning range is approximately 6 from 0 to -60 V, after which the C(V) saturates when punch-through is reached. The donor doping concentration extracted from C(V) measurements is shown in Fig. 1 and agrees well with the doping profile specification.

A performance comparison with published varactors is shown in Table I. This work does not represent the highest small-signal tuning range, but Table I shows that the tuning ratio of this work decreases more slowly with the bias volt-

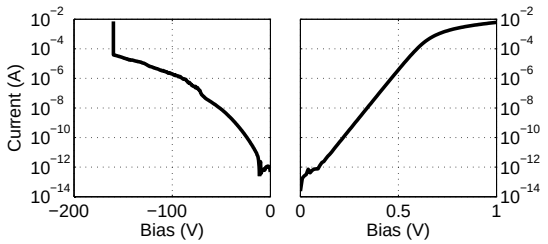

Fig. 4. I(V) for a single finger device with −160 V breakdown. The voltage-current slope is 62 mV/decade in the forward direction.

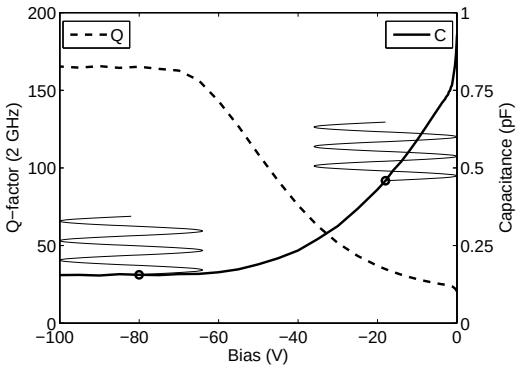

Fig. 5. C(V) and Q-factor at 2 GHz for a single finger device. Waveforms are inserted to illustrate how the C(V) supports an effective 3:1 tuning range at a voltage amplitude of 18 V (see 3:1 bias in Table I).

age. Fig. 6 shows how the effective tuning range decreases, from the small-signal tuning range, when superimposing an increasing voltage amplitude while simultaneously preventing forward conduction and reverse breakdown (see the waveforms in Fig. 5). It is seen that this work supports superior effective tuning range for voltage amplitudes larger than 5 V. The large bias range between punch-through and breakdown also allows for a voltage amplitude of more than 45 V at the peak Q-factor after punch-through (Q_{max}), making the devices suitable for DLM networks in high power PAs.

V. Discussion and Conclusions

The fabrication of SiC varactors with large effective tuning range suitable for microwave power applications, such as the DLM of PAs, has been demonstrated. This is accomplished by spreading the C(V) through the use of a custom designed doping profile. Making the C(V) non-abrupt has increased the

TABLE I
Comparison With Other Varactors

Technology	Tuning Range	4:1 / 3:1 / 2:1 Bias (V)[a]	Punch-thr. (V)	Break-dn. (V)	Q_{min}	Q_{max}
SiC [3] (2 GHz)	5.6:1	1 / 2 / 6	15	40	8	45
GaAs [6] (2 GHz)	9:1	5 / 7 / 9	15	28	22[b]	150[b]
GaN [7] (1 GHz)	5:1	2 / 3 / 9	N.A.	120	N.A.	> 35
This work (2 GHz)	6:1	8 / 18 / 30	60	>150	20	160

[a] bias voltage where the tuning ratio is 4:1 / 3:1 / 2:1
[b] assuming $Q_{parasitics} = 100$

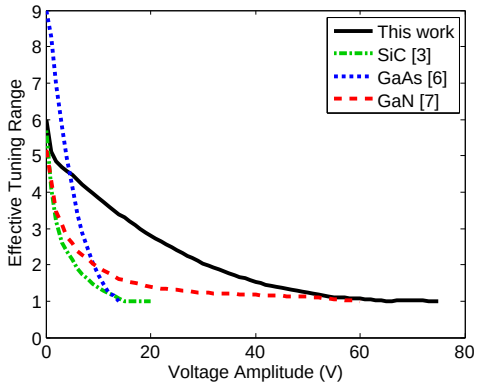

Fig. 6. Effective tuning range versus superimposed voltage amplitude, while avoiding forward conduction and reverse breakdown.

allowable voltage swing when the varactor is tuned. Device fabrication by a self-aligned interdigitated process enables the down-scaling of anode mesa dimensions and anode-cathode distance to reduce the parasitic series resistance. The breakdown voltage, effective tuning range, and Q-factor are all significantly improved compared to [3], and for specific applications trade-offs can be made through the epitaxial design. Supporting such a C(V), while simultaneously maintaining a high peak Q-factor by layout and processing, is exclusively enabled by the wide bandgap properties of SiC.

VI. Acknowledgement

The authors would like to thank Hossein M. Nemati (Chalmers), Christian Fager (Chalmers), Rik Jos (NXP Semiconductors BV), and Björn Almgren (Ericsson AB) for fruitful discussions concerning the varactor requirements for DLM architectures.

References

[1] H. M. Nemati, H. Cao, B. Almgren, T. Eriksson, and C. Fager, "Design of Highly Efficient Load Modulation Transmitter for Wideband Cellular Applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 11, pp. 2820–2828, Nov. 2010.

[2] J. Eriksson, N. Rorsman, and H. Zirath, "4H-silicon carbide Schottky barrier diodes for microwave applications," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 796–804, Mar. 2003.

[3] M. Sudow, H. M. Nemati, M. Thorsell, U. Gustavsson, K. Andersson, C. Fager, P.-Å. Nilsson, J. ul Hassan, A. Henry, E. Janzén, R. Jos, and N. Rorsman, "SiC Varactors for Dynamic Load Modulation of High Power Amplifiers," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 728–730, Jul. 2008.

[4] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H silicon carbide," *Applied Physics Letters*, vol. 71, no. 1, pp. 90–92, Jul. 1997.

[5] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of Varactor-Based Tunable Matching Networks for Dynamic Load Modulation of High Power Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1110–1118, May 2009.

[6] C. Huang, P. J. Zampardi, K. Buisman, C. Cismaru, M. Sun, K. Stevens, J. Fu, M. Marchetti, and L. C. N. de Vreede, "A GaAs Junction Varactor With a Continuously Tunable Range of 9:1 and an OIP_3 of 57 dBm," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 108–110, Feb. 2010.

[7] W. Lu, L. Wang, S. Gu, D. P. R. Aplin, D. M. Estrada, P. K. L. Yu, and P. M. Asbeck, "InGaN/GaN Schottky Diodes With Enhanced Voltage Handling Capability for Varactor Applications," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1119–1121, Oct. 2010.

[8] A. Henry, J. ul Hassan, J. Bergman, C. Hallin, and E. Janzén, "Thick Silicon Carbide Homoepitaxial Layers Grown by CVD Techniques," *Chem. Vap. Deposition*, vol. 12, no. 8-9, pp. 475–482, Sep. 2006.