Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes

Aik Yean Tang, Erich Schlecht, Goutam Chattopadhyay, Robert Lin, Choonsup Lee, John Gill, Imran Mehdi and Jan Stake

Abstract— **In this paper, we present the thermal analysis of high frequency planar Schottky diode based multiplier chips, for high power applications. In order to optimize the thermal characteristic of the multiplier chip, several chip layout and fabrication options are explored. Both the steady-state and transient thermal characteristic of a multiplier chip are analyzed by solving the heat equation via the 3D finite element method, taking into account the temperature-dependent material properties. The result shows that the multiplier chips exhibit thermal resistances in the order of 10^3 K/W and thermal time-constants in the order of milliseconds. The analysis also indicates that bonding agents with a better thermal conductivity is required in order to fully exploit benefits of the heat spreader. On the other hand, a GaN-on-Si-based multiplier chip demonstrates a better thermal handling capability compared to the GaAs-based chip. Experimental verification of the simulation result is performed using IR microscopy, showing a reasonable match of the measured and simulated result. The transient characteristic of the measured junction temperature is modeled by two time-constants, i.e. 11 and 3.3 ms.**

Index Terms—**Frequency multiplier, Gallium Arsenide, Gallium Nitride, heat spreader, high power submillimeter-wave generation, Schottky diodes, thermal conductivity, thermal analysis.**

I. Introduction

Advancement in terahertz applications, such as radio astronomy, astrophysics and earth observations, as well as imaging and sensing applications [1-5] has generated an increasing demand on the output power of terahertz sources. To date, planar Schottky diode based multiplier chains have been demonstrated to be promising, compact and reliable terahertz sources [6],[7]. Nevertheless, the output power of the multiplier chain is within the micro-watt range for operating frequencies beyond 1 THz. Therefore, continuous technology development of the multiplier chain is required toward delivering high power terahertz sources.

Recent progress in power amplifier technology has made it possible to construct W-band (75 – 110 GHz) sources capable of producing powers in the 1-Watt range [8]. These sources are required in order to build multiplier based local oscillator chains in the frequency range of 2-3 THz. However, it becomes imperative that the multipliers, in particular the initial stage multipliers, be able to withstand the large input power without degrading electrical performance or burning out. Therefore, the chip thermal management is nontrivial in optimizing the multiplier performance for high power applications.

To date, literature regarding thermal analysis and modeling of transistors [9-13], heterostructure barrier varactors [14],[15] and Gunn diodes [16-18] abound. For planar Schottky diode, the work on thermal analysis is limited. Thus far, a 1-D 'series-resistor' [19] and a 2-D heat flow model [20] have been reported. However, these models are not sufficiently flexible to be implemented to explore various chip layouts, as well as material systems in improving the thermal management of the multiplier chip.

In this paper, we present a 3D thermal analysis of the planar Schottky diode based multiplier chip. Both the steady-state and transient thermal characteristic of a multiplier chip are analyzed by solving the heat equation in a 3D calculation domain. The solution is acquired numerically via the finite element method (FEM). The objective of this work is to understand the thermal constraints of conventional multiplier chips and explore possible options to optimize the chip thermal characteristics. Various layout and fabrication options, such as thickness of the metal traces, substrate width and thickness, bonding to a heat spreader, are explored. In addition to the conventional Gallium Arsenide (GaAs)- based multiplier chip, the thermal characteristics of Gallium Nitride (GaN)-based diode on Silicon (Si) substrates are also studied.

The layout of the multiplier chip analyzed in this work and the thermal simulation setup are described in Section II. The experimental verification performed using infrared (IR) microscopy is explained in Section III. The steady-state and transient thermal analysis results are then discussed in Section IV. With this, an effective and flexible method to analyze the thermal behavior of the multiplier chip is demonstrated.

Manuscript received August 12, 2011. This work was carried out at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, under contract with National Aeronautics and Space Administration. The research has received funding from the VINNOVA, Security Link, Ericsson's Research Foundation, Solveig och Karl G Eliassons Minnesfond, and Chalmersska Forskningsfonden 2010.

A.Y. Tang and J. Stake are with the Department of Nanoscience and Microtechnology, Chalmers University of Technology, SE-42196, Göteborg, Sweden. (phone: +46 (0)31 772 1739; fax:+46 (0)31 164513; e-mail: aik-yean.tang@ chalmers.se).

E. Schlect, G. Chattopadhyay, R. Lin, C. Lee, J. Gill and I. Mehdi are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91125 USA.

II. The Multplier Chip Layout And Simulation Setup

The chip layout analyzed in this work is based on the 200 GHz substrate-less frequency doubler chip developed by the Jet Propulsion Laboratory (JPL). The multiplier chip is designed based on a balanced configuration, where 3 diodes are connected in series at each branch. The series connection of diodes in the design aims at improving the chip power handling capability. Details of the chip design are described in [21]. Fig 1 shows the top view and the cross section of the multiplier chip.

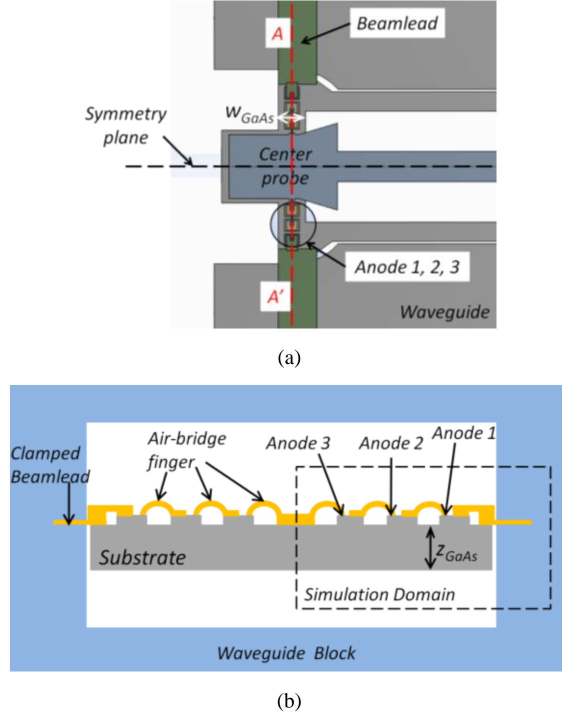

Fig. 1 Schematic of the substrateless multiplier chip (a) a top view of the chip mounted on a half waveguide split block; (b) the A-A' cross section of the multiplier chip in the full waveguide block. NB! The drawing is not to scale.

For the thermal analysis, the 3D FEM solution is acquired via the Ansys Mechanical [22] simulation tool. Due to the twofold symmetry of this chip, only half of the chip is simulated. The simulation domain is outlined in Fig. 1. The default chip layout and variation of layout parameters are summarized in TABLE I.

TABLE I
LAYOUT AND FABRICATION OPTIONS

Parameter	Symbol	Variable
Thickness of GaAs[a] or Si substrate	z_{GaAs}, z_{Si}	3[b], 5, 10, 25, 50[a] µm
Thickness of gold	z_{gold}	1[a], 2 µm
Width of substrate	w_{GaAs}	70[a], 120 µm
Thickness of CVD diamond	$z_{diamond}$	0[a], 10, 25 µm
Thickness of bonding agent	z_{bond}	0[a], 1 µm

[a] Default layout parameter of the multiplier chip analyzed in this paper.
[b] Only simulated for the GaAs-based multiplier.

In the FEM analysis, a similar heat load is applied directly beneath each of the anode contacts. All the non-contact surfaces of the waveguide block, except the facet facing toward the inner channel and the chip, are configured to be at the ambient temperature (T_{amb}), i.e. 300 K. The remaining surfaces are assumed to be adiabatic, i.e. assuming the effect of convection and radiation cooling mechanisms are negligible.

The temperature dependent thermal properties of the material are taken into account in this analysis. For simplicity, the thermal properties of the top junction layer and highly-doped buffer-layer are assumed to be similar. The material thermal properties used in this analysis are listed in TABLE II.

TABLE II
MATERIAL THERMAL PROPERTIES

Material	Thermal conductivity, $\kappa\left(W/mK\right)$	Thermal capacity, $c_p\left(J/kg\ K\right)$	Mass density, $\rho\left(kg/m^3\right)$
GaAs	$51\times\left(\frac{300}{T}\right)^{1.28}$	Tabulated data in [23]	5317
Gold	310	130	19320
Brass	109	377	8500
CVD diamond	1100	-	-
Bonding agent	0.52	-	-
GaN	$157\times\left(\frac{300}{T}\right)^{1.9}$	-	-
Si	$160\times\left(\frac{300}{T}\right)^{1.5}$	-	-

Upon setting up the proper simulation boundaries and material thermal properties, the conduction heat equation as stated in (1) is solved.

$$\rho\times c_p(T)\times\left(\frac{\partial T(x,y,z,t)}{\partial t}\right)=\left(\nabla\bullet(\kappa(T)\times\nabla T(x,y,z,t))\right)+g \qquad (1)$$

where ρ is the material mass density, $c_p(T)$ is the temperature-dependent thermal capacity, $T(x,y,z,t)$ is the time- and spatial-dependent temperature, $\kappa(T)$ is the temperature-dependent thermal conductivity and g is the heat generation rate per unit volume.

III. Experimental Verification

For the experimental characterization, a QFI [24] IR microscope (InfraScope^{TM}) with the capability of recording

the steady-state as well as the transient thermal characteristic was used. The 200 GHz multiplier chip is mounted on a waveguide split block, where the block is heated to an ambient temperature of 80 °C. The diodes are DC biased and the total power dissipation is estimated from the DC voltage and current.

A. *Steady-state Thermal Characterization*

In this measurement, the total DC power dissipation level is estimated to be 7.02 mW, i.e. 1.17 mW per anode. A similar power level is then applied to the anodes in the FEM simulations. For the steady-state thermal imaging, the spatial resolution is approximately 3 µm, allowing the temperature of each individual anode to be resolved. Fig. 2 shows the measured and simulated temperature distribution for the multiplier chip. A comparison of the measured and simulated anode temperatures is summarized in TABLE III.

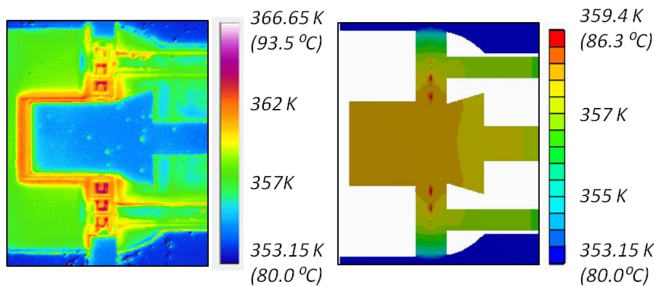

Fig. 2 Measured and simulated temperature distribution of the multiplier chip.

TABLE III
ANODE TEMPERATURE COMPARISON BETWEEN THE IR MEASUREMENT AND FEM SIMULATION

Anode #	IR Microscopy (°C)	Simulation (°C)	Max ΔT (°C)
1 / 6	87.0 / 88.0	85.0	3.0
2 / 5	88.0 / 89.0	86.0	3.0
3 / 4	89.0 / 89.5	86.0	3.5

By comparing the temperature at the anode area, the differences between measured and simulated temperatures are less than 3.5 °C. For a temperature rise of approximately 10 °C, the temperature difference contributes toward a maximum error of ~ 35%. The high error percentage is related to the relatively small temperature rise, due to a relatively low DC equivalent forward biased power dissipation in the chip. Nevertheless, the error is below 5 % in the absolute temperature scale (in °C).

For the ohmic contacts, the measured temperature is higher than the temperature at anode contacts. On the other hand, the measured temperature at center probe is lower compared to the simulation. The discrepancies between the measurement and simulation result are related to the geometrical anisotropic radiation and the lack of material spectral radiance correction. Thus, the dependency of material surface emissivity on temperature, emission angle and wavelength should be taken into consideration for further temperature characterization. Alternatively, the radiance correction problem could be circumvented by coating a thin layer of black paint as discussed in [11].

B. *Transient Thermal Characterization*

For transient thermal characterization, a single pixel, high-speed temperature detector is used in conjunction with the steady-state microscope. The multiplier is subjected to a 5 Hz square pulse, where the on-state equivalent power is estimated to be 9.2 mW, i.e. 1.53 mW per anode. Due to a lack of sufficient spatial resolution in this measurement setup, the recorded temperature is inherently an average temperature of the total imaging area. The imaging area and recorded temperature are shown in Fig. 3.

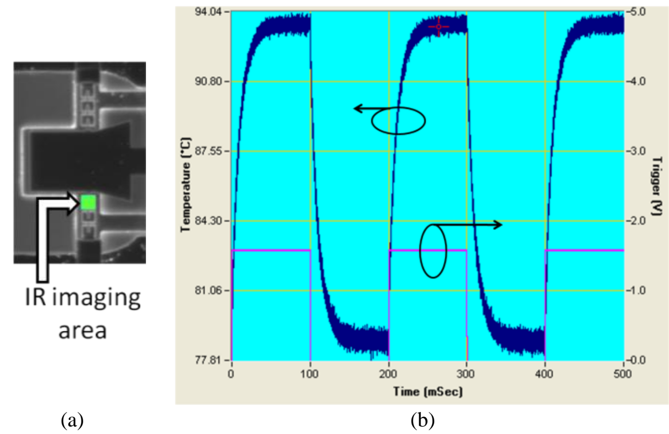

Fig. 3 (a) Imaging area of the chip during transient characterization; (b) The recorded average temperature and the measurement synchronization pulse during transient characterization.

Analysis of the measured temperature for the first on-state pulse, i.e. the first 100 ms, shows that modeling the transient characteristic of the temperature requires more one time-constant. The time-constants of the temperature transient characteristic are estimated by fitting (2) to the measured temperature. In this analysis, the temperature data below 1 ms is excluded. A plot of the measured temperature rise and the corresponding fitted curve for the period of 100 ms is shown in Fig. 4.

$$T(t) = T_1 + T_2 \times \left(1 - \exp\left(-t/\tau_1\right)\right) + T_3 \times \left(1 - \exp\left(-t/\tau_2\right)\right) \quad (2)$$

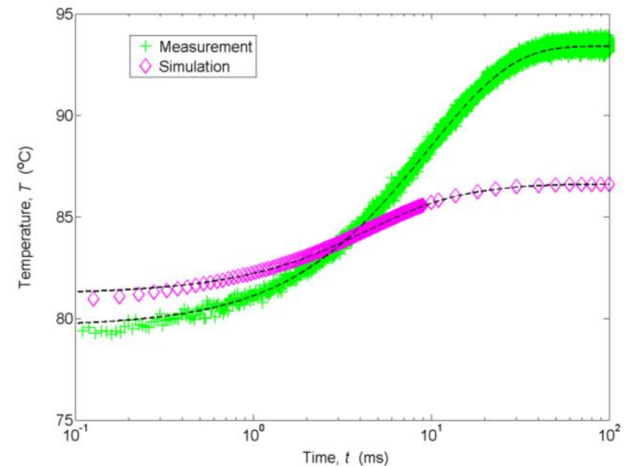

Fig. 4 A comparison of the measured and simulated transient temperature. The corresponding fitted curves are plotted in dashed lines. (Note: temperature data below 1ms is excluded from the curve-fit).

A transient simulation of the multiplier chip subjected to a similar heat pulse is performed. In order to compare with the measured temperature, a total of twelve temperature points within the imaging area are resolved. The average of these twelve temperatures is then used to estimate the coefficients of interest. The coefficients, estimated from the measurement and simulation, are compared in TABLE IV.

TABLE IV
COEFFICIENTS OF THE FITTED CURVE

Coefficient	IR Microscopy	Simulation
T_1 (°C)	79.6	81.2
T_2 (°C)	12.0	1.2
T_3 (°C)	1.8	4.2
τ_1 (ms)	11.0	14.0
τ_2(ms)	3.3	4.0

The result shows that the IR measured temperature settled at 94 °C whereas the simulated temperature settled at 87 °C. The estimated coefficient T_2 and T_3 are differing between the measured and simulated data. The discrepancy could be related to the lack of sufficient spatial resolution (~ 30 μm) as well as spectral radiance correction. The anomalously higher temperature at the ohmic contact, as discussed in Section III.A, is averaged into the measurement data, increasing the overall temperature. Thus, transient characterization with higher spatial resolution and more sophisticated spectral radiance correction is required. Nevertheless, there is a reasonable match for the estimated time-constants (i.e. τ_1 and τ_2) between the measurement and simulation.

IV. Result

For semiconductor device operation at room temperature, a junction temperature range between 300 K and 500 K is considered reasonable. Therefore, all of the thermal analysis performed in this work is limited to this temperature range. In this section, the result of the steady-state thermal analysis is first presented and discussed, followed by the transient thermal analysis.

A. Steady-state Thermal Analysis

1) The Hot Spot

Due to the temperature-dependent thermal conductivity of the GaAs, the temperature exhibits a non-linear behavior as a function of power dissipation. Thus, thermal resistance (R_{th}), as defined in (3), is explicitly power dissipation dependent.

$$R_{th_i} = \frac{T_{anode_i} - T_{amb}}{P_{dis_i}} \quad (3)$$

where i is the anode number.

Fig. 5 shows the steady-state anode junction temperatures for the multiplier chip with the default layout parameters. At a lower power dissipation level, such as 5 mW per anode, the temperatures of all the anodes are similar. However, it is observed that the temperature between anodes deviates as the power dissipation level is increased. The hot spot in the chip is located at the anode closest to the symmetry plane, i.e. anode 3. Thus, the analysis herein after is based on the thermal characteristic of anode 3.

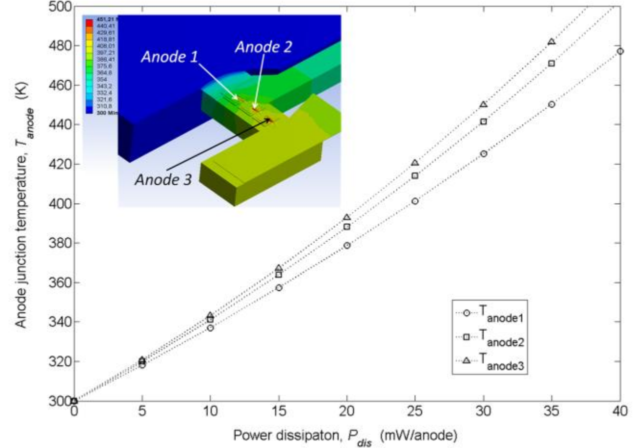

Fig. 5 A comparison of the anode temperatures in the multiplier chip as a function of power dissipation level. (Inset: A temperature distribution plot for the chip at power dissipation level of 30 mW per anode.)

2) Thermal Constraints

In order to optimize the chip layout, the thermal constraints for the chip have to be identified. Fig. 6 shows the temperature profile along the surface of a chip substrate. This figure indicates that the thermal bottleneck (i.e. high temperature gradient) is located at the transition area between the waveguide block to chip substrate, as well as the diode mesa areas close to the anode heat source.

By considering these constraints, the chip layout could be optimized by improving the heat path from the anode junction area to the substrate, and the beam lead connection from the substrate to the waveguide block. A better heat extraction from the top of the anode junction contributes to a reduced temperature gradient close to the junction area. This could be achieved by increasing the thickness of metal (i.e. gold) connection between the diodes, the center probe and the waveguide. On the other hand, a wider or thicker substrate would lower the overall thermal resistance of the chip. The suppression of the thermal gradient by increasing the thickness of gold and the width of the substrate is illustrated in Fig. 6.

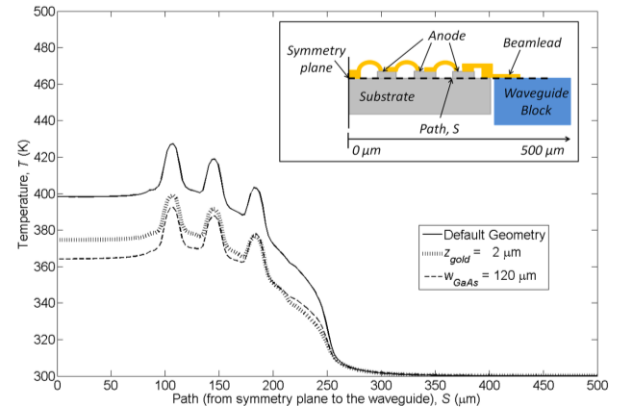

Fig. 6 A plot of the temperature profile along the surface of the substrate at a power dissipation level of 30 mW for each anode. (Inset: Schematic of the simulation domain indicating the physical location of the path, S. NB! The drawing is not to scale.)

3) Thermal Characteristic Optimization for a Thin Substrate

For high frequency electronic operation, a thinner substrate is favored in order to reduce dielectric loading losses. On the contrary, a thicker substrate is preferred to optimize the chip thermal conductance. A thinner substrate exhibits a larger thermal resistance. It is also subjected to a larger thermal coupling effect from adjacent diodes, which could be enhanced by the poor and temperature-dependent material thermal conductivity of the substrate material.

Intuitively, the larger thermal resistance for a thin substrate could be compensated by attaching a heat spreader at the bottom of the substrate. Thus, use of CVD diamond substrates, which possess approximately 30 times better thermal conductivity than GaAs, has been investigated. . A comparison of the effect of bonding the CVD diamond to the chip on the thermal behavior for several configurations is shown in Fig. 7. Considering a power dissipation level of 10 mW per anode, the thermal resistance for a 3 µm thick GaAs substrate is approximately four times larger than the resistance for a 50 µm thick substrate.

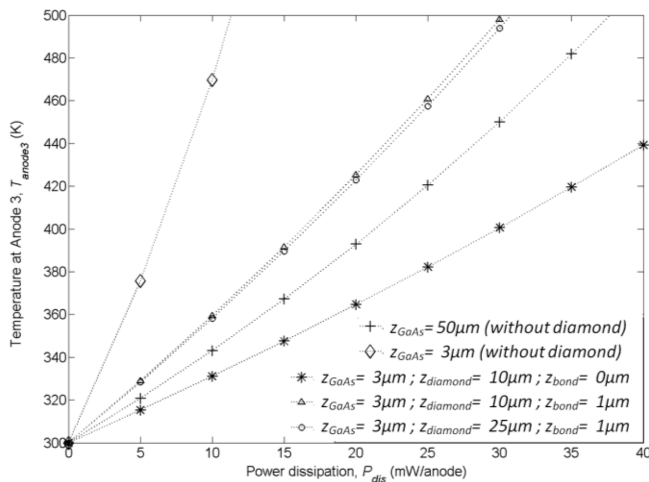

Fig. 7 A plot of the maximum junction temperature as a function of power dissipation.

Ideally, attachment of a 10 µm thick CVD diamond beneath the thin substrate results in a lower thermal resistance compared to the 50 µm thick substrate. For these two configurations, the thermal resistance is 3.4 x 10^3 K/W and 5 x 10^3 K/W, respectively, at a power dissipation level of 30 mW per anode. However, in practice, the CVD diamond is attached to the substrate via a thin layer of bonding agent. Due to the low thermal conductivity of the bonding agent, the thermal resistance is observed to be approximately two times higher compared to the values in the ideal case (without bonding agent). Moreover, with a layer of bonding agent, the effect of the CVD diamond layer thickness is minimal (see the plot for 10 and 25 µm thick CVD diamond layers in Fig. 7).

Fig. 8 illustrates the temperature profile from the top of anode to the bottom of substrate or heat spreader. The plot shows that the advantage of utilizing the CVD diamond is impeded by the bonding agent, which exhibits a high thermal resistance. Thus, it is concluded that the thermal behavior of the 3 µm thick substrate chip could be improved by bonding it to the CVD diamond. However, the thermal behavior of this configuration is not as optimal as a 50 µm thick substrate chip. In order to fully exploit the benefits of the heat spreader, a bonding agent with better thermal conductivity is required. One possibility is to load the bonding agent with diamond beads which helps to reduce the thermal resistance in the bonding layer. Alternatively, fabrication process incorporating ion-beam deposited CVD diamond layer on the semiconductor substrate could be considered.

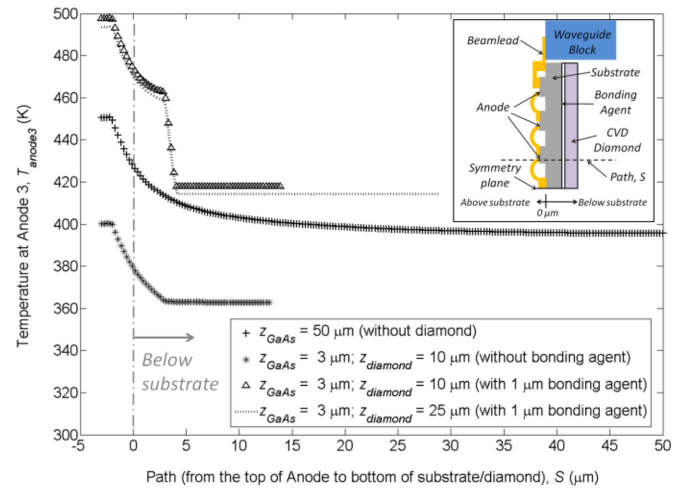

Fig. 8 Temperature gradient from the top of anode contact to the bottom of the chip (Inset: Schematic of the simulation domain indicating the physical location of the path, *S*. NB! The drawing is not to scale.).

From the material system point of view, progress in the Gallium Nitride (GaN) grown on Silicon (Si) substrate [25] has provided an opportunity to develop GaN-based diodes on Si-substrate. This material system possesses a better heat handling capability than GaAs, providing an alternative to GaAs for developing high power diode-based multipliers. Since the GaN layer is grown directly on the Si substrate, the thermal conductance of the substrate is not reduced by the bonding agent. Thus, the thermal behavior of this material system is also investigated.

Fig. 9 shows a comparison the thermal behavior of the GaAs and the GaN-on-Si- based multiplier chip. In this figure, a piecewice cubic hermite polynomial is used to interpolate the temperature as a function of substrate thickness for each power dissipation level (i.e. 0 to 40 mW at the interval of 5 mW). For both of these material systems, it is observed that the nonlinear temperature rise prevails for a thinner substrate, as a consequence of the non-linear temperature coupling effect. However, the result shows that the level of temperature elevation is lower for the GaN-on-Si based chip. For a 10 µm thick substrate, the temperature of the hot spot reached 500 K at the power level of 20 mW per anode for the GaAs-based multiplier, compared to the power level of 40 mW per anode for GaN-on-Si-based multiplier.

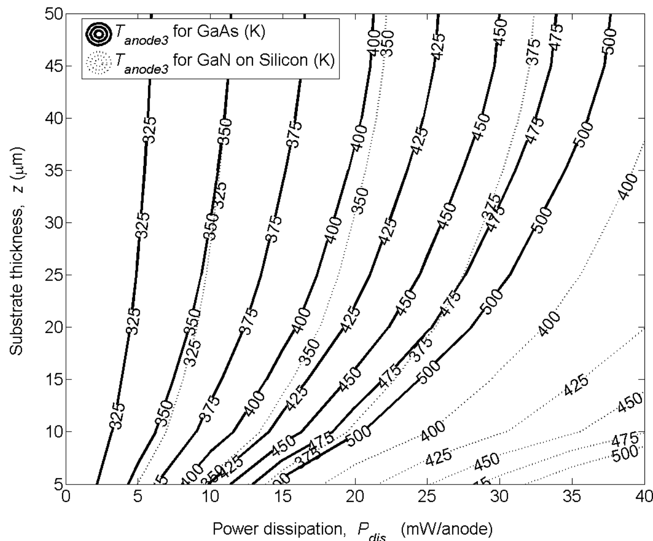

Fig. 9 A contour plot of the temperature of anode 3 as a function of substrate thickness and power dissipation for GaAs- and GaN-on-Si-based multiplier chip.

B. *Transient Thermal Analysis*

A transient thermal analysis is also performed on the multiplier chip with the default layout parameters for 2 power dissipation levels, i.e. 10 and 30 mW per anode. In order to compare the transient behavior of a thinner substrate, the multiplier chip with a 5 μm thick substrate is simulated. In these simulations, the temperatures at the anode junctions are monitored. Fig. 10 shows the simulation result for the transient characteristic of anode 3.

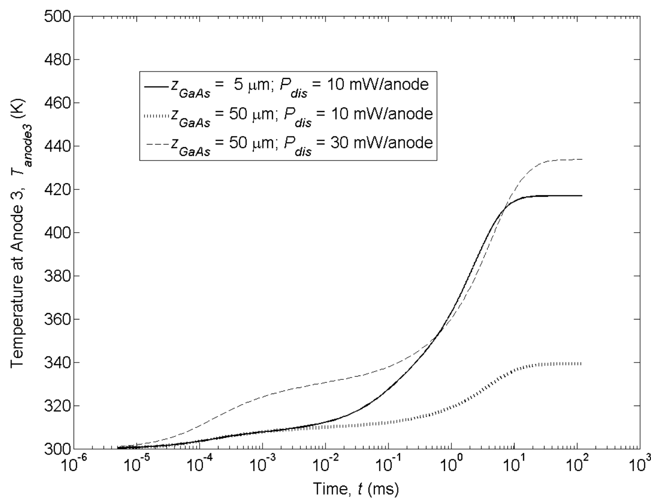

Fig. 10 Transient thermal characteristic of the multiplier chip.

At the diode junction, a sharp temperature rise occurs at the initial state. This is followed by a long slow rise to the steady-state. For a multiplier chip with a similar substrate thickness, the initial temperature rise differs for different power dissipation level. On the other hand, the initial temperature rises are similar for multiplier chips with different substrate thickness but subjected to a similar power dissipation level. This indicates that a similar thermal mass is experienced by the heat front at the instant when the power is dissipated. As time progresses, the heat front encountered a different thermal mass, due to the difference in the substrate thickness. In addition, the transient behavior for the multiplier chip could also be attributed to the thermal coupling effect, where the temperature rise is enhanced by the ambient heat from other anodes.

From the analysis, it is concluded there exists multi time-constants in the transient characteristics. The overall thermal time constant for the multiplier chip is large, exhibiting a settling time in the order of tens millisecond.

V. Conclusion

In this paper, a flexible and effective way of performing 3D thermal analysis of multiplier chips has been demonstrated using the FEM method. A 200 GHz frequency doubler chip is analyzed, taking into account the non-linear temperature response of the chip. The chip beamlead and the substrate thickness are identified as the two bottlenecks for thermal management. Optimization of the substrate thickness and material can result in better multiplier chip performance.

For the transient thermal analysis, the multiplier chip exhibits a slow and multi time-constants thermal response. This indicates that the temperature is almost constant for high frequency continuous wave (CW) application. However, further investigation on the transient behavior could be beneficial for applications where the multipliers are operated in pulse mode, such as radar imaging and sensing applications.

Acknowledgment

The authors would like to thank Dr. J. Vukusic (Chalmers University of Technology) for the useful feedback.

References

[1] P. Siegel, “Terahertz technology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, 2002, pp. 910-928.

[2] M. Shur, “Terahertz technology: devices and applications,” *Proceedings of 35th European Solid-State Device Research Conference*, 2005, pp. 13-21.

[3] A. Maestrini, B. Thomas, H. Wang, C. Jung, J. Treuttel, Y. Jin, G. Chattopadhyay, I. Mehdi, and G. Beaudin, “Schottky diode-based terahertz frequency multipliers and mixers,” *Comptes Rendus Physique*, vol. 11, Aug. 2010, pp. 480-495.

[4] D. Woolard, R. Brown, M. Pepper, and M. Kemp, “Terahertz Frequency Sensing and Imaging: A Time of Reckoning Future Applications?,” *Proceedings of the IEEE*, vol. 93, 2005, pp. 1722-1743.

[5] D.T. Hodges, E.E. Reber, F.B. Foote, and R.L. Schellenbaum, *Safeguards applications of far infrared radiometric techniques for the detection of contraband*, 1980.

[6] I. Mehdi, G. Chattopadhyay, E. Schlecht, J. Ward, J. Gill, F. Maiwald, and A. Maestrini, “Terahertz Multiplier Circuits,” *IEEE MTT-S International Microwave Symposium Digest*, 2006, pp. 341-344.

[7] G. Chattopadhyay, E. Schlecht, J. Ward, J. Gill, H. Javadi, F. Maiwald, and I. Mehdi, “An all-solid-state broad-band frequency multiplier chain at 1500 GHz,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, 2004, pp. 1538-1547.

[8] D. Ingram, Y. Chen, I. Stones, D. Yamauchi, B. Brunner, P. Huang, M. Biedenbender, J. Ellion, R. Lai, D. Streit, K. Lau, and H. Yen, “Compact W-band solid-state MMIC high power sources,” *Microwave Symposium Digest., 2000 IEEE MTT-S International*, 2000, pp. 955-

958 vol.2.

[9] D.J. Walkey, T.J. Smy, T. Macelwee, and M. Maliepaard, “Compact representation of temperature and power dependence of thermal resistance in Si, Inp and GaAs substrate devices using linear models,” *Solid-State Electronics*, vol. 46, Jun. 2002, pp. 819-826.

[10] P. Baureis, “Electrothermal modeling of multi-emitter heterojunction-bipolar-transistors (HBTs),” *Third International Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits*, 1994, pp. 145-148.

[11] J. Wilson and K. Decker, “GaAs MMIC thermal modeling for channel temperatures in accelerated life test fixtures and microwave modules,” *Proceedings of IEEE/CPMT 10th Semiconductor Thermal Measurement and Management Symposium*, 1994, pp. 121-128.

[12] C. Snowden, “Large-signal microwave characterization of AlGaAs/GaAs HBT's based on a physics-based electrothermal model,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, 1997, pp. 58-71.

[13] D. Dawson, “Thermal modeling, measurements and design considerations of GaAs microwave devices,” *Technical Digest 16th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, 1994, pp. 285-290.

[14] J. Stake, L. Dillner, S. Jones, C. Mann, J. Thornton, J. Jones, W. Bishop, and E. Kollberg, “Effects of self-heating on planar heterostructure barrier varactor diodes,” *IEEE Transactions on Electron Devices*, vol. 45, 1998, pp. 2298-2303.

[15] M. Ingvarson, B. Alderman, A. Olsen, J. Vukusic, and J. Stake, “Thermal constraints for heterostructure barrier varactors,” *IEEE Electron Device Letters*, vol. 25, 2004, pp. 713-715.

[16] X. Tang, M. Rousseau, C. Dalle, and J.C. De Jaeger, “Physical analysis of thermal effects on the optimization of GaN Gunn diodes,” *Applied Physics Letters*, vol. 95, 2009, p. 142102.

[17] F. Hasegawa and Y. Aono, “Thermal limitation for CW output power of a Gunn diode,” *Solid-State Electronics*, vol. 16, Mar. 1973, pp. 337-344.

[18] R.P. Joshi, S. Viswanadha, P. Shah, and R.D. del Rosario, “Monte Carlo analysis of GaN-based Gunn oscillators for microwave power generation,” *Journal of Applied Physics*, vol. 93, 2003, p. 4836.

[19] E. Schlecht, G. Chattopadhyay, A. Maestrini, D. Pukala, J. Gill, S. Martin, F. Maiwald, and I. Mehdi, “A high-power wideband cryogenic 200 GHz Schottky 'substrateless' multiplier: Modeling, design and results,” *Proceedings of the Ninth International Conference on Terahertz Electrons*, Charlottesville, VA, USA: 2001, pp. 485-494.

[20] D. Porterfield, “Millimeter-Wave Planar Varactor Frequency Doublers,” University of Virginia, 1998.

[21] J. Bruston, “Development of 200-GHz to 2.7-THz multiplier chains for submillimeter-wave heterodyne receivers,” *Proceedings of SPIE*, Munich, Germany: 2000, pp. 285-295.

[22] *ANSYS Mechanical*, ANSYS Inc, Southpointe, 275 Technology Drive, Canonsburg, PA 15317, USA.

[23] S. Adachi, *GaAs and related materials: bulk semiconducting and superlattice properties*, World Scientific, 1994.

[24] *Quantum Focus Instruments Corporation*, 2385 La Mirada Drive, Vista, CA 92081 USA.

[25] S. Pal and C. Jacob, “Silicon - A new substrate for GaN growth,” *Bulletin of Materials Science*, vol. 27, 2004, pp. 501-504.