Mobility improvement and microwave characterization of a graphene field effect transistor with silicon nitride gate dielectrics

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***Abstract*—We report on the influence of a silicon nitride gate dielectric in graphene based field-effect transistors. The silicon nitride is formed by a plasma-enhanced chemical vapor deposition method. The process is based on a low-density plasma at a high pressure (1 Torr), which results in a low degradation of the graphene lattice during the top-gate formation process. Microwave measurements of the graphene field-effect transistor show a cut-off frequency of 8.8 GHz for a gate length of 1.3 µm. A carrier mobility of 3800 cm^2/Vs at room temperature was extracted from the DC-characteristic.**

***Index Terms*—Graphene, FETs, Microwave transistors, dielectric.**

I. Introduction

Since the first production of graphene, a one-atom-thick planar sheet of carbon, in 2004 [1], a considerable effort has been performed to explore and make use of its unique properties. Much of the interest in graphene is due to a very high intrinsic carrier mobility [2], together with the ability to change its carrier density by the field-effect [3-7]. These properties make it a promising material for high speed analog devices such as transistors operating in the terahertz band (0.3-3 THz) [8]. One of the challenges in designing graphene Field Effect Transistors (G-FETs), is the degradation of the transport properties due to surrounding gate dielectric as well as influence from the carrier substrate. Also, in the process of creating the graphene-dielectric interface, defects are generated in the graphene lattice, which increases carrier scattering in the material and significantly decreases its intrinsic carrier mobility.

Several approaches have been investigated to overcome the problem. One approach is to use atomic layer deposition (ALD) of high-k oxides, which is performed at low temperature [9, 10]. However, a surface pretreatments is necessary to prohibit discontinuous film growth which can degrade the mobility [11]. Another approach is to utilize a polymer buffer layer between graphene and conventional gate dielectrics. Farmer et al. has shown that the buffer layer can preserve the carrier transport property in graphene [12]. From a technological point of view, however, it is preferred to avoid liquid processing needed for the polymer deposition and also the polymer has a problem of thermal stability. Recently, it has been demonstrated that nanowires can be exploited as a gate structure without degrading the transport properties in graphene, resulting in an intrinsic cut-off frequency (f_T) as high as 300 GHz [13]. However, the parasitic elements especially the high gate resistance, in the nanowire, reduces the extrinsic (f_T), to a few gigahertz [13]. Lately, it has been shown that silicon nitride can be directly deposited on graphene surface and the deposition process can be engineered in a way that the graphene substantially conserves its original transport properties. This is done by a plasma-enhanced chemical vapor deposition (PECVD) process at the pressure of 8 Torr [14]. Nevertheless, this high pressure level is hard to achieve in many common silicon nitride PECVD systems.

In this paper, we demonstrate a modified PECVD process in order to deposit silicon nitride films at a pressure of 1 Torr and it still preserves the transport properties of the graphene film. We achieve a carrier mobility as high as 3800 cm^2/Vs which is about twice higher than the earlier reported value using silicon nitride gate dielectric [14]. For the first time the RF performance of the G-FET is measured with silicon nitride gate dielectric. The RF results also corroborate retaining a high carrier mobility in the graphene sheet.

II. Device fabrication

The graphene samples were fabricated by micromechanical exfoliation of natural graphite on a 300 nm silicon oxide film, thermally grown on a high resistive (ρ>10K Ωcm) silicon substrate. The layer number was determined by measuring the changes in the reflectance of green light [15]. The source and drain pads were defined by electron beam lithography and consist of Ti(10 Å)/Pd(200 Å)/Au(500 Å) metal layer stack, deposited by electron beam evaporation. The silicon nitride gate was applied using a PECVD 6-inch chamber (STS). The process is performed at 350 ºC using SiH4, NH3 and N2 gases. A high frequency (13.56 MHz) RF source was used for the plasma generation. We optimized the process with the intent to reduce the damage on the graphene surface. This was achieved by increasing the chamber pressure as well as igniting the plasma with only 20 W. The gas flow rates for SiH4, NH3 and N2 were 40 sccm, 40 sccm and 4000 sccm respectively. We applied 2 different chamber pressures (0.4

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Torr and 1 Torr) in order to investigate the effect of the chamber pressure on the silicon nitride-graphene integration process. The layer structure of the device is demonstrated in Fig. 1. Two devices with the same size were fabricated with 40 nm silicon nitride on the graphene surface. The pressure of the silicon nitride PECVD process in the fabrication of the first and second device were 0.4 and 1 Torr respectively. The refractive index was measured to 2.1 for both films using an ellipsometer.

III. DC MEASUREMENT

The channel resistance versus back-gate voltage of the devices, prior the top-gate electrode formation, is depicted in Fig. 2a. As can be seen, the second device has a lower channel resistance which translates into less damage to the graphene lattice and a higher mobility. The higher chamber pressure decreases the mean free path of the radicals in the process, thereby disabling them from reacting with the exposed graphene surface.

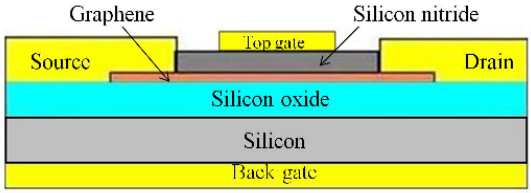

Fig. 1. The device layer structure (Si3N4/graphene/SiO2/Si). NB! Figure is not to scale.

In order to investigate the effect of the deposited silicon nitride on the transport property of the graphene quantitatively, we extracted the electron and hole mobilities of the second device by fitting the channel resistance to the equation [14]

$$R_{ds} = R_s + \frac{L}{Wq\mu\sqrt{n_0^2 + n^2}} \qquad (1)$$
$$n = C_{BG}(V_{BG} - V_{Dirac})/q$$

where L and W are the length and width of the graphene channel, q is the electron charge, C_{BG} is the back-gate capacitor, n_0 is residual carrier concentration, V_{Dirac} is the gate voltage at the Dirac point and R_s is the series resistance. Fig. 2b shows the channel resistance of the device versus the back gate voltage. It also depicts the fitted channel resistance profiles for both the electron carrier (n-channel $V>V_{Dirac}$) and the hole carrier (p-channel $V<V_{Dirac}$ }) and they are matched with the measurement results. The extracted carrier mobility for electron and hole are, *3800 cm^2/Vs* and *2300 cm^2/Vs*, respectively, series resistance $R_s=32\ \Omega$, gate voltage at the Dirac point V_{Dirac}= *-27V* and residual carrier concentration $n_0=2.2\times10^{11}cm^{-2}$. The obtained mobilities are comparable to the electron and hole mobilities of the devices whose gate dielectric is deposited by ALD [16]. The result suggests that the developed PECVD process highly preserves the carrier mobility in the graphene sheet. Also it should be noted that before silicon nitride deposition, the Dirac point was at a positive voltage (V_{Dirac}=*35-50V*) and carrier mobilities in the range of μ_e=*2500-3000 cm^2/Vs*, μ_h=*3500-4000 cm^2/Vs*. One possible reason for shifting of the Dirac point can be the reaction of the nitrogen atoms (NH_3) presented in the PECVD process with graphene [17] and also it is shown that in the presence of the NH_3 absorbent, graphene conductivity becomes higher when the channel is carried by electrons rather than holes [18].

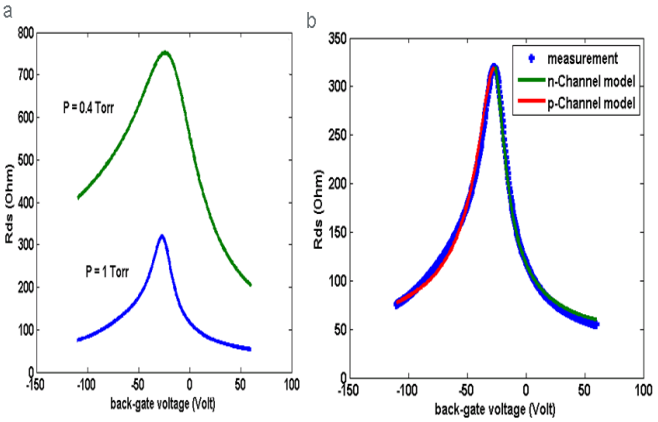

Fig. 2. (a) Channel resistance versus back-gate voltage of two graphene devices measured at RT. The silicon nitride is deposited at the pressure of 0.4 Torr for the first and 1 Torr for the second device (V_{ds} = 0.3V). (b) Channel resistance versus back-gate voltage measured at RT. The extracted mobilities are μ_e=*3800 cm^2/Vs* and μ_h=*2300 cm^2/Vs*. (*Vds = 0.3 V, W=15 μm, L =1.5 μm).*

IV. RF MEASUREMENT

For assessing the RF performance, a top-gate electrode consisting of Ti(10 Å)/Pd(200 Å)/Au(500 Å) was patterned by electron beam lithography (Fig. 3). The channel resistance of the device versus the top-gate voltage and the corresponding transconductance dI_{DS}/dV_{GS} and channel current of the device are measured at *Vds = 2.5V* and are depicted in Fig. 4. Leakage currents through the SiN top gate were < 1 pA μm^{-2}. The standard Through-Reflection-Line (TRL) calibration technique is utilized and the reference plane is located close to the G-FET. The measurement is performed from 1 GHz to 20 GHz with an Agilent PNA and on-wafer probe station. The s-parameters are measured at different Vgs values and changing gate voltage mainly affects S_{22} and S_{21} (Fig. 5a). The high frequency current gain (h_{21}), maximum stable gain (*MSG*) and Mason's unilateral gain (*U*) of the G-FET are shown in Fig. 5b which is measured in a 50-ohm coplanar waveguide environment. The device exhibits an extrinsic f_T of 8.8 GHz which is close to the intrinsic value of $g_m/2\pi C_g$ (14 GHz, C_g=*30 fF* is obtained from the S-parameters and g_m=*2.7 mS* from DC I-V). Due to the high contact resistances the device does not have power gain for f > 1GHz.

V. CONCLUSIONS

In summary, we developed a PECVD silicon nitride process with low density plasma which leads to a low degradation of the graphene surface. This allows for high mobilities to be retained in top-gate operation, qualifying the silicon nitride as a possible candidate for G-FET gate dielectric. The process

does not need any surface pretreatment and is performed by the common silicon nitride PECVD system.

We report a carrier mobility of 3800 cm^2/Vs which is the highest reported value using silicon nitride gate dielectric and this value is comparable to the values achieved by the ALD process [16, 19]. We achieve an extrinsic cut-off frequency of 8.8 GHz in a G-FET with silicon nitride as the gate dielectric for a relatively long gatelength (1.3 µm). The device works in the linear transport regime and therefore its cutoff frequency scales with the gate length as 1/L. By scaling the gate length down to the submicron region f_T can be extended into the millimeter wave region.

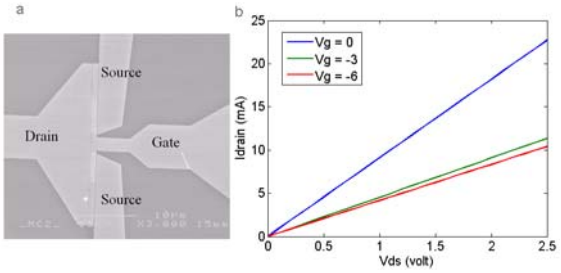

Fig. 3. (a) SEM image of the G-FET with 1.3 µm gatelength, 1.5 µm source-drain distance, 15 µm gatewidth and 40 nm thick silicon nitride layer. (b) Channel current versus drain voltage at different gate voltages.

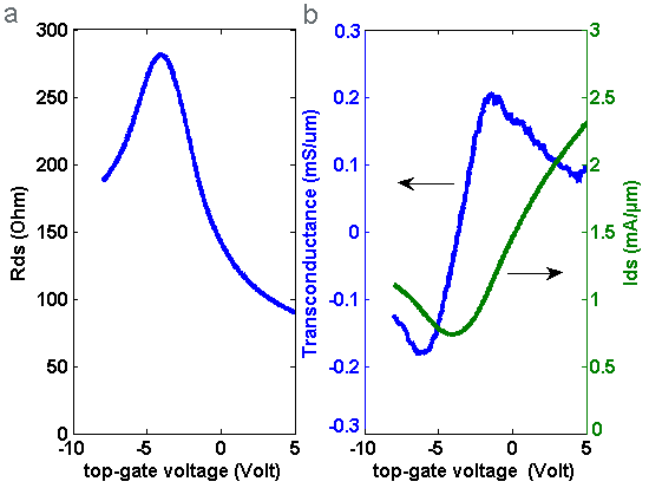

Fig. 4. (a) Measured channel resistance versus top-gate voltage at (RT). (b) transconductance and channel current of the G-FET at V_{ds} = 2.5 V.

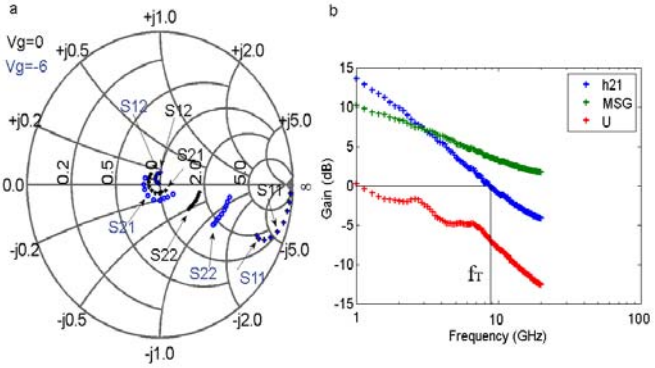

Fig. 5. (a) S-parameter for Vds = 2.5 V for Vgs = 0, -6 V, (b) Measured current gain (h_{21}), MSG and U-gain of a graphene transistor incorporating silicon nitride as the top-gate dielectric (RT). (b) The device shows aan extrinsic f_T of 8.8 GHz for which measurement is done with V_{ds} =2.5 V and V_{gs} = -6 V.

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