Fabrication and Characterization of Thin-Barrier $Al_{0.5}Ga_{0.5}N$/AlN/GaN HEMTs

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***Abstract*—The growth, fabrication, and performance of $Al_{0.5}Ga_{0.5}N$/AlN/GaN high-electron-mobility transistors (HEMTs) with a total barrier thickness of 7 nm are reported. An optimized surface passivation and an Ohmic recess etch yield HEMTs exhibiting 0.72 S/mm peak extrinsic DC transconductance at a current density of 0.47 A/mm. Devices with a gate length of 90 nm achieve 78 GHz unity-current-gain frequency and up to 166 GHz maximum frequency of oscillation. The minimum noise figure at 10 GHz is 0.52 dB with an associated gain of 9.5 dB.**

***Index Terms*—Aluminum gallium nitride, HEMTs, microwave noise, recessed Ohmic contacts, surface passivation.**

I. Introduction

THIN-BARRIER high-electron-mobility transistors (HEMTs) based on the III–nitride material system are an active area of research for millimeter-wave applications [1]. State of the art approaches involve relatively thick (> 200 Å), $x \sim 25\%$ $Al_xGa_{1-x}N$ barriers [2,3]; ultrathin (< 40 Å), binary AlN barriers [4,5]; thin $x = 40\%$ and ultrathin $x = 72\%$ $Al_xGa_{1-x}N$ barriers [6,7]; and lattice-matched $Al_xIn_{1-x}N$ barriers [8,9]. Within very high (70–100%) Al composition $Al_x(Ga,In)_{1-x}N$ barriers, a sharp electric field results from polarization-induced charge; this often necessitates an insulated-gate, or MISHFET, approach to ameliorate high gate leakage currents. Methods involving the growth of an $Al_xIn_{1-x}N$ barrier are limited to lower temperatures than $Al_xGa_{1-x}N$, resulting in inferior surface morphology.

In this letter, the traditional, uninsulated $Al_xGa_{1-x}N$ HEMT structure is investigated at an Al composition of 50%. The challenges presented by this thin-barrier material are twofold: (i) to effectively passivate the surface to mitigate surface depletion and transient trapping effects and (ii) to achieve a low-resistivity, alloyed Ohmic contact.

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II. Material Design and Characterization

In order to efficiently modulate the two-dimensional electron gas (2DEG) and minimize short-channel effects, the ratio of the gate length, L_G, to the distance, d, between the gate metal and the center of the 2DEG should be 10–15 [10]. In this work, d was scaled to 7 nm. The epitaxial III–nitride layers were grown by metalorganic chemical vapor deposition (MOCVD) on semi-insulating silicon carbide. These epitaxial layers consisted of, from the top down, a 20 Å GaN cap, 36 Å $Al_{0.5}Ga_{0.5}N$ barrier, 15 Å AlN interbarrier, and a 1.8 µm compensation-doped Fe:GaN buffer. Coupled one-dimensional Schrödinger–Poisson simulations [11] predict a 2DEG sheet density, n_{s0}, of 1.4×10^{13} cm^{-2}; the AlN interbarrier induces two-thirds of the 2DEG and improves hot-electron confinement, while the $Al_{0.5}Ga_{0.5}N$ barrier layer induces the remaining one-third of the sheet density. The tunneling probability compared to an AlN-only barrier is reduced by the inclusion of the $Al_{0.5}Ga_{0.5}N$ and GaN cap.

Lehighton measurements across the unpassivated 3" wafer revealed a sheet resistance of 405 ± 17 Ω/□. Fully-passivated van der Pauw test structures indicate a sheet resistance $R_{sh} = 334$ Ω/□, Hall mobility $\mu_H = 1245$ cm^2/V s, and 2DEG sheet density $n_{s0} = 1.5 \times 10^{13}$ cm^{-2}, demonstrating excellent agreement with the simulations. The realized reduction in sheet resistance is indicative of effective surface passivation.

III. Fabrication

After a standard wafer cleaning, the surface of the GaN cap layer was passivated with a ~70 nm LPCVD SiN_x film, which was grown using ammonia and dichlorosilane precursor gases at 820°C and 250 mTorr. The deposition temperature, pressure, and flow ratio were optimized to minimize the interface trap density as described in [12]. Under these growth conditions, the refractive index was measured as 2.3 at a wavelength of 632 nm, indicating a silicon-rich film. The passivation was etched in subsequent mesa isolation and contact deposition steps using an NF_3 inductively coupled plasma reactive ion etch (ICP RIE).

Next, mesa isolation was achieved via a Cl_2/Ar ICP RIE. Ohmic contacts were patterned with a self-aligned recess etch into the $Al_{0.5}Ga_{0.5}N$ barrier layer using a low-bias Cl_2/Ar ICP RIE [13]. The recess depth was characterized as a function of etch time and optimized for minimal Ohmic contact resistance, R_c, achieving $R_c < 0.5$ Ω mm across more than one wafer. A

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recessed, Ti/Al/Ni/Au metallization alloyed at 820°C yields $R_c = 0.48\ \Omega$ mm and $R_{sh} = 332\ \Omega/\square$. These values are tenable for mm-wave applications and an order of magnitude better than our non-recessed contacts ($R_c = 4.4\ \Omega$ mm).

Two-finger, U-shaped devices were fabricated. Electron-beam lithography was used to pattern gate openings in the SiN_x of 90 nm and 170 nm, as measured by SEM. A second electron-beam lithography step was used to define and lift-off Ni-based, gamma-shaped, field-plated gates.

IV. HEMT Characterization and Discussion

Characterization consisted of the following measurements: DC, S-parameter, pulsed utilizing a DiVA D225 using 200 ns pulses and a 1 ms period, noise parameters using an ATN NP5 system, and RF large signal using an active load-pull system using a Maury LSNA. The direct measurement of the magnitude and phase of incident and reflected waves at six harmonics permitted the reconstruction of a dynamic load line.

A. Steady-State DC, Small Signal, and Pulsed DC

The DC output characteristic of a representative 2×100 μm HEMT with a 170 nm gate footprint, 1 μm source-gate spacing, 2 μm gate-drain spacing, and a gate pitch of 50 μm (Fig. 1a) shows an on resistance of 2.1 Ω mm and reasonably low output conductance. The transfer characteristic for this device (Fig. 1b) exhibits good pinch-off at a threshold voltage of −0.6 V and a peak extrinsic transconductance of 662 mS/mm. For these DC curves, the gate bias is limited to $V_{GS} < +0.8$ V, beyond which the Schottky diode turns on. The breakdown voltage was characterized with a criterion of 1 mA/mm. The two-terminal breakdown was measured as $V_{DGbr} = 99\pm8$ V and the three-terminal breakdown was $V_{DSbr} = 88\pm8$ V using the drain-current injection technique [14]. The gate current, $|I_G|$, at pinch-off ($V_{GS} = -0.6$ V) under cold-FET conditions ($V_{DS} = 0$ V) is below 0.5 μA/mm.

This 2×100 μm device demonstrates a peak unity-current-gain frequency, f_T, of 50 GHz and simultaneous maximum frequency of oscillation, f_{max}, of 55 GHz at $V_{DS} = 5.5$ V. The latter increases to $f_{max} = 105$ GHz at $V_{DS} = 25$ V, while f_T drops to 40 GHz due primarily to thermal effects. At these respective biases, I_G is −2 μA/mm and −17 μA/mm.

The f_{max}/f_T ratio benefits from the reduced access resistance of a shorter source-gate spacing. A 2×50 μm HEMT with the

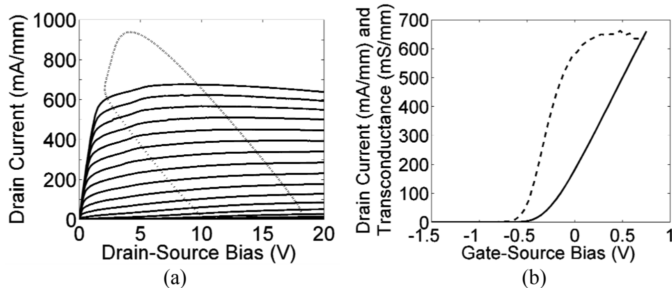

Fig. 1. DC characteristics of a 2×100×0.17 μm HEMT. (a) Output characteristic (solid); the maximum gate voltage is $V_{GS} = 0.7$ V and is depicted in steps of $\Delta V_{GS} = 0.1$ V. The dynamic load line (dotted) measured in saturation at 8 GHz CW biased class AB at $V_{DS} = 10$ V is superimposed. (b) Transfer characteristic (solid) at $V_{DS} = 4.5$ V; the extrinsic transconductance (dashed) peaks at 662 mS/mm at $V_{GS} = 0.5$ V.

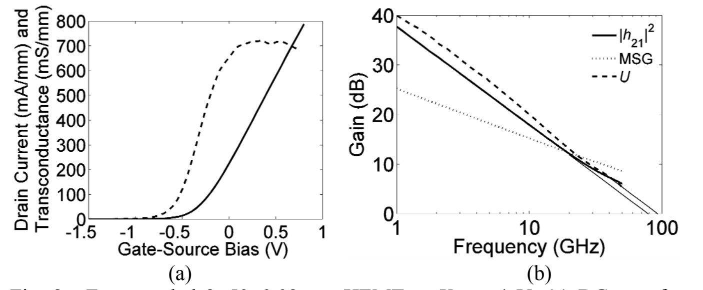

Fig. 2. For a scaled 2×50×0.09 μm HEMT at $V_{DS} = 4$ V, (a) DC transfer characteristic (solid); the extrinsic transconductance (dashed) peaks at 722 mS/mm at $V_{GS} = 0.35$ V. (b) Small-signal performance biased at peak g_m; $|h_{21}|^2$ (solid) and U (dashed) are extrapolated at an ideal −20 dB/decade to $f_T = 78$ GHz and $f_{max} = 93$ GHz, respectively.

gate footprint scaled to 90 nm and source-gate spacing halved to 0.5 μm exhibits a peak extrinsic transconductance of 722 mS/mm (Fig. 2a); at the same bias, $f_T = 78.5$ GHz and $f_{max} = 93$ GHz (Fig. 2b). After de-embedding the pad capacitances, $f_{T,int} = 91$ GHz. The maximum frequency of oscillation increases to $f_{max} = 166$ GHz with simultaneous $f_T = 57$ GHz at $V_{DS} = 20$ V. At these respective biases, the gate current, I_G, is −0.3 μA/mm and −4.0 μA/mm. The realized f_T and f_{max} are appropriate for mm-wave applications.

Pulsed I_D–V_{DS} characteristics measured from off-state ($V_{DSq} = V_{GSq} = 0$ V), gate-lag ($V_{DSq} = 0$ V, $V_{GSq} = -1.5$ V), and drain-lag ($V_{DSq} = 10$ V, $V_{GSq} = -1.5$ V) quiescent conditions reveal negligible gate lag and ~6% drain lag in the knee region. This predicts low DC-RF dispersion under large-signal operation, which is confirmed by the full swing of the dynamic load line, in that there is negligible increase of the dynamic on resistance at this bias (Fig. 1a) [15].

B. Noise Parameters

Noise parameter characterization of the same 2×100 μm HEMT with 170 nm gate footprint reveals a minimum noise figure $F_{min} < 1$ dB through the 14 GHz measurement range (Fig. 3). At 5 GHz $F_{min} = 0.36$ dB with an associated gain $G_A = 13.6$ dB; at 10 GHz, $F_{min} = 0.52$ dB with $G_A = 9.5$ dB. These noise parameter results are among the lowest noise figures published for short-gate III–nitride HEMTs [16]. The low F_{min}, low noise resistance, and high associated gain makes

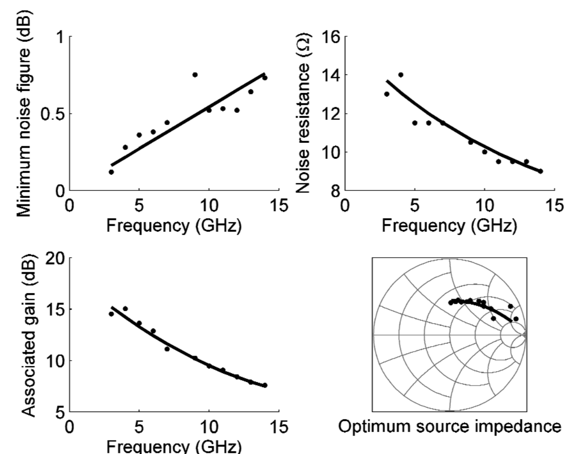

Fig. 3. Noise parameters of a 2×100×0.17 μm HEMT biased at $V_{GS} = -0.1$ V, $V_{DS} = 5$ V ($I_D = 177$ mA/mm, $I_G = -4$ μA/mm); best-fit curves guide the eye.

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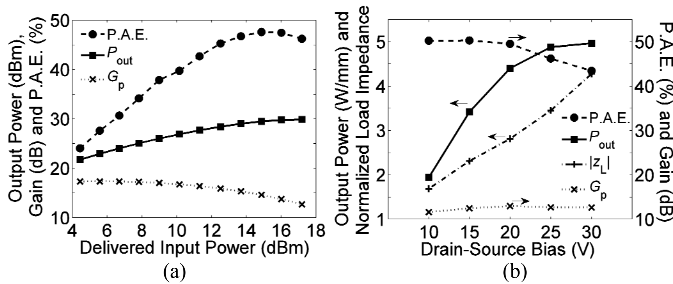

Fig. 4. Output power, gain, and power-added efficiency of a 2×100×0.17 μm HEMT operating in class AB at 8 GHz CW matched for output power (a) as a function of input power at V_{DS} = 25 V and (b) optimally matched and driven into saturation (~4 dB gain compression) as a function of drain-source bias.

this $Al_{0.5}Ga_{0.5}N$/AlN/GaN material structure an attractive platform for low-noise amplifier (LNA) monolithic microwave integrated circuit (MMIC) applications.

C. Large Signal

The 170 nm-gate-footprint HEMTs with 2×100 μm layout were characterized under power-matched, continuous-wave (CW) class AB operation at 8 GHz. At V_{DS} = 25 V when driven into compression, the device delivers 4.9 W/mm with 46% power-added efficiency (P.A.E.) (Fig. 4a). As a function of drain bias, the evolution of output power and P.A.E. when optimally matched for output power and driven into saturation is presented in Fig. 4b. The output power scales well with drain bias to 20 V, after which it is limited by a combination of self-heating, the small drain-lag, and output conductance.

V. Conclusion

High-Al content AlGaN/GaN HEMT structures with high sheet density and mobility are demonstrated. Devices were fabricated using a method compatible with Chalmers' in-house GaN MMIC process [17]. An LPCVD passivation mitigates the surface depletion effect induced by the thin barrier and results in low DC–RF dispersion; these findings are consistent with effective surface passivation. A recessed Ohmic contact achieves low contact resistivity. The HEMTs exhibit excellent noise performance and transconductance; the high g_m/I_D ratio allows high gain even at low current densities. The future inclusion of a nitride or oxide gate dielectric would permit further forward bias of the gate to drive the transistor into saturation. The DC, pulsed, small-signal, noise parameter, and large-signal results indicate that this thin-barrier $Al_{0.5}Ga_{0.5}N$/AlN/GaN epitaxial platform is promising for realizing high-power, high-efficiency microwave and millimeter-wave MMICs, including LNAs, switches, and wideband power amplifiers (PAs).

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