A 14 Gbps On-/Off- Keying Modulator in GaAs HBT Technology

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***Abstract*—A proof of concept on-/off- keying (OOK) modulator is designed and implemented in a commercial heterojunction bipolar transistors IC process. The modulator circuit consists of an amplifier/latch structure, which is used as an OOK modulator for the first time. One of its advantages is that the topology may be implemented in both field effect transistor and bipolar technology. The measurement results correspond well with simulation and show that the modulator is capable of handling carrier frequencies up to 28 GHz, and data rates up to 14 Gbps. The isolation of the modulator in the off-state is better than 27 dB over the whole frequency range.**

***Index Terms*—Emitter-coupled pair, GaAs heterojunction bipolar transistor (HBT), latch, MMIC, on-/off- keying (OOK) modulator, RF Switch, short switch transient time.**

I. Introduction

THE capacity requested for data traffic in communication networks is ever-increasing. Ultra-fast wireless technology is necessary to support the traffic. The trend is to allocate wide spectrum at high frequencies, thus low order modulation may be applied. Examples of such bands are the E-band (71–76 and 81–86 GHz), the 145 GHz and the 220 GHz bands. All of these are of interest for point-to-point links.

On-/off- keying (OOK) is a popular modulation used in applications where spectrum efficiency is not of highest priority. This is partly due to its simplicity and low implementation cost.

Several approaches have been used to implement OOK. The first is based on data-controlled impulse generation where the generated impulses pass through a bandpass filter of the desired carrier frequency [1]. The second approach uses a RF switch to turn on and off either an amplifier [2]–[7] or a local oscillator (LO) [8]. The advantage of directly switching a LO is that extremely high isolation is achievable [8]. The data rate, however, is limited due to the time it takes to start up an oscillation. The third type of OOK modulator is based on cancellation of two outputs from a differential amplifier [9]. Table I summarizes the results of previously reported OOK modulators, including present work.

Most OOK modulators are implemented in CMOS or HEMT technologies [1]–[9]. Bipolar transistors exhibit a less distinct switching behavior as compared to FET devices, and has therefore traditionally been considered less suitable for switch applications.

In this letter, we propose a new way to realize the switching function using a latch structure, which may be implemented in FET as well as in bipolar technology. Circuits based on latch structures have been widely used in comparators and static frequency dividers. To the best of the authors' knowledge, OOK modulators based on latch structure has not been reported so far.

It should be noted that this is a proof-of-concept demonstration and the design was not focused on performance optimization.

This letter is organized as follows: the basic concept of the latch structure is reviewed and its operation principle as an OOK modulator is described in Section II. The circuit topology is given in Section III. Measured results are shown in Section IV and are compared with simulation.

II. Operation Principle

The basic concept of the latch structure in a comparator application is given in [10]. Here we explain the operational principle of the proposed latch-based OOK modulator in similarity to [10].

A schematic diagram of a differential emitter coupled pair (ECP) latch is shown in Fig. 1. The operational waveforms of such a structure as latched comparator and OOK modulator are demonstrated in Fig. 2. In a latched comparator application, the tracking pair (Q3, Q4) comprise a differential amplifier, which pass the differential inputs (Dp, Dn) to the differential output nodes (Qp, Qn), when the clock (CK) is "high" (i.e. $\mathrm{CKp} = \mathrm{high}$ and $\mathrm{CKn} = \mathrm{low}$). In the latching phase (CK is "low"), the latching pair (Q5, Q6) emphasize the previous value of (Qp, Qn) by means of positive feedback and hold the comparison result until CK goes to 'high' in the next cycle. The maximum operation speed of the latch structure is determined by the delay of the recovery process in the tracking phase and regeneration process in the latching phase (Fig. 2) [10].

We propose an OOK modulator adopting a similar principle as mentioned above, by applying a carrier signal at the input and a data signal at the clock pair (Ckp, Ckn). When CK (or input data) is "high," the structure works in on-state (corresponding to the tracking phase) and the carrier passes to the output through

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TABLE I
COMPARISON OF PREVIOUSLY REPORTED RESULTS AND THIS WORK

Ref.	Tech.	Freq. (GHz)	Data-rate (Gbps)	ISO. (dB)	P_{DC} (mW)	Approach
[1]	0.1 μm InP HEMT	78-93	12.5	-	0.7	Impulse Generator
[2]	90 nm CMOS	60	2	28.5	14.4	Switching PA
[3]	90 nm CMOS	60	8	26.6	0	Distributed Switch
[4]	0.15 μm HJFET	DC-110	1	22.2	0	Traveling-wave Switch
[5]	0.1 μm InP HEMT	120	10	13	500**	Switching TWA
[6]	90 nm CMOS	60	2	19	26.3**	Switching PA
[7]	90 nm CMOS	60	2.5	-	183**	Switching Amplifier
[8]	0.13 μm CMOS	45-46	0.15	50	100 *	Switching LO
[9]	90 nm CMOS	60	3.5	-	5	Differential LO Cancellation
This work	1.4 μm GaAs HBT	DC - 28	14	>27	250	ECP latch

*:including LO,**:entire transmitter;

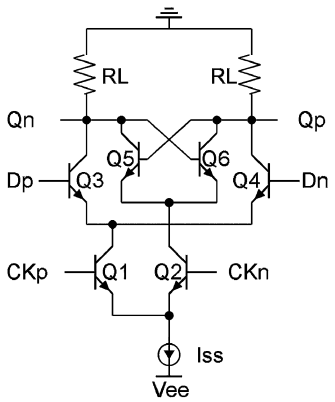

Fig. 1. Simplified diagram of a differential emitter-coupled pair (ECP) latch.

amplifier pair (Q3, Q4); when input data is 'low', the output is inter-locked by the latching pair (Q5, Q6), which is isolated from the input signal. In this way the carrier is turned on and off according to the input data.

III. CIRCUIT TOPOLOGY

Fig. 3 is the detailed schematic of the proposed OOK modulator. Q1–Q6 constitutes the core latch structure similar to what is shown in Fig. 1. Q7 and Q8 are emitter followers to provide proper bias to differential amplifier pair (Q3, Q4). So do Q9 and Q10 for the latch pair (Q5, Q6). The carrier signal is applied at port 1. The data signal applied at port 2 and via emitter followers Q11–Q14 is further fed to the ECP (Q1, Q2) which functions as a current switch controlled by the input data.

Fig. 4 is a photograph of the manufactured modulator chip. The chip dimension is 1.0 mm×0.8 mm including probe pads and on-chip decoupling capacitors. The core part of the circuit measures 0.4 mm×0.3 mm. The IC technology used in this work is a commercial GaAs HBT process with 1.4 μm emitter width [12]. The HBT device has a peak transient frequency f_t of 55 GHz and a maximum oscillation frequency f_{Max} of 63 GHz. All HBTs used in this design are single emitter device with 10 μm emitter length.

A single -5 volt dc supply is required for bias and the current is 50 mA, resulting in 250 mW of total dc power consumption.

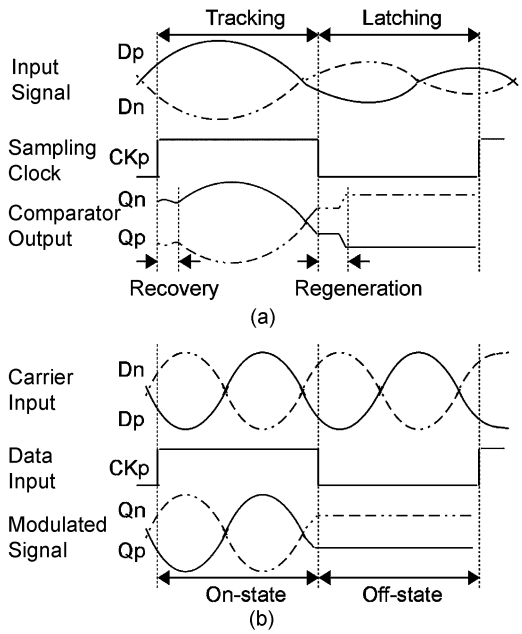

Fig. 2. Operational waveform of latch structure as: (a) latched comparator and (b) OOK modulator.

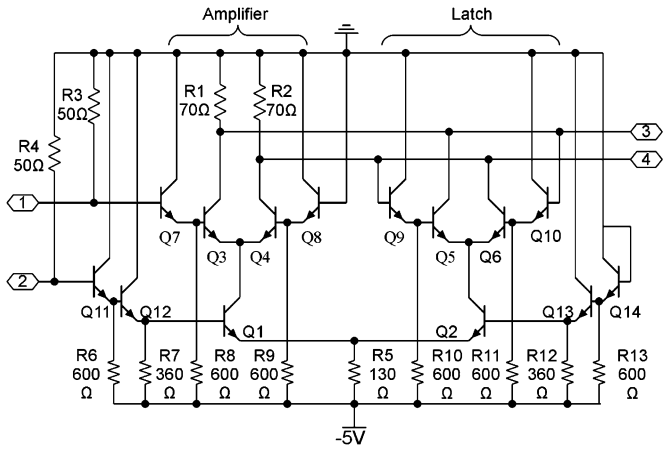

Fig. 3. Schematic of the proposed OOK modulator.

IV. MEASUREMENT RESULTS

Fig. 5 shows the measured and simulated insertion loss and isolation of the OOK modulator. A 0 dBm carrier is applied

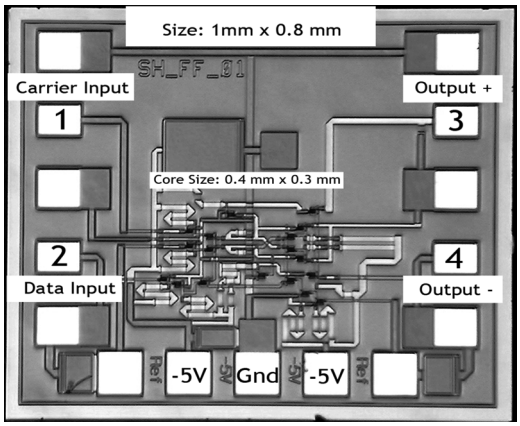

Fig. 4. Photograph of the GaAs HBT OOK modulator chip.

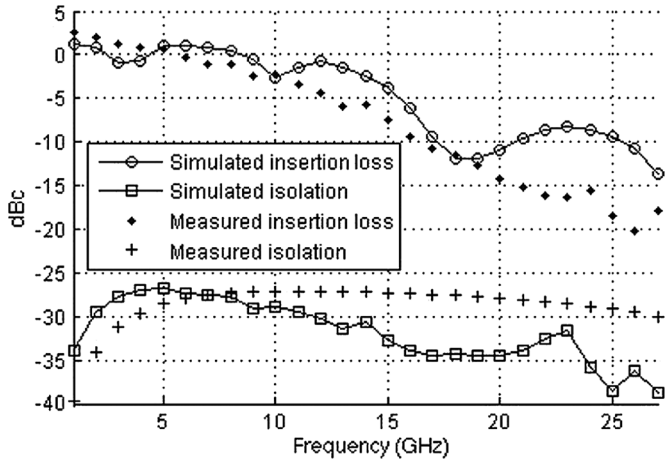

Fig. 5. Measured and simulated loss and isolation.

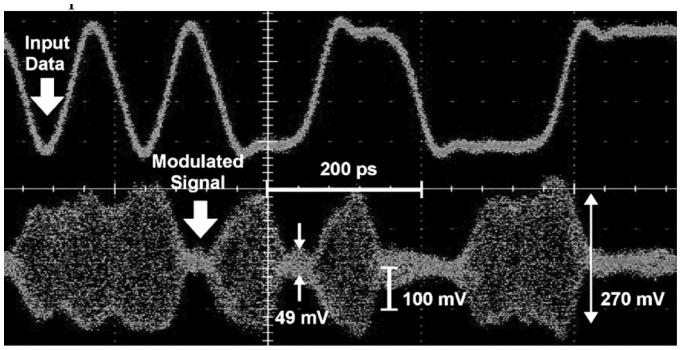

Fig. 6. Measured time domain waveform of a 14 Gbps data modulated on an 18 GHz carrier.

at port 1 and the power level at port 3 is measured when the data input is kept at either high (for insertion loss measurement) or low (for isolation measurement). The measured results show that the isolation is 27 dB or better for carrier frequencies up to 28 GHz (the maximum frequency measured). One advantage of applying the proposed latch structure is that the isolation does not become worse as carrier frequency increases. This is because that the latch block, due to the positive feedback [10], works in a stable saturation state [11]. Therefore, any leakage carrier signal from the amplifier stage will be attenuated through the latch.

The OOK modulator exhibits slight gain at low frequencies. The loss at higher frequencies is caused by the negative gain of the differential amplifier. Therefore, the output power of this modulator is limited.

Fig. 6 shows the modulator output when 14 Gbps data is modulated on an 18 GHz carrier. This is the highest data rate supported by the pattern generator we used. The results show that the switch transient time is short enough to support 14 Gbps data transmission.

V. Conclusion

An OOK modulator suitable for over 10 Gbps communication systems has been designed, fabricated and characterized. The modulator contains a latch structure, eliminating the need for RF switch, and therefore may be implemented either in FET or in bipolar process.

The measurement results show that this OOK modulator can operate over a wide carrier frequency range, from dc up to 20 GHz. Also, the modulator supports a data transmission up to 14 Gbps. The Off-state isolation is better than 27 dB over the operation frequency band.

References

[1] Y. Nakasha, "A 12.5-Gb/s pulse modulator with 6.5-ps FWHM using 0.1-μm inPHEMTs for ultra-wideband impulse radio communications," in *Proc. Compound Semicond. Integr. Circuit Symp. (CSICS'08)*, Oct. 2008, pp. 12–15.

[2] J. Lee, C. W. Byeon, K. C. Eun, I. Y. Oh, and C. S. Park, "Gbps 60 GHz CMOS OOK modulator and demodulator," in *Proc. Compound Semicond. Integr. Circuit Symp. (CSICS'10)*, Oct. 2010, pp. 3–6.

[3] A. Oncu, K. Takano, and M. Fujishima, "8 Gbps CMOS ASK modulator for 60 GHz wireless communication," in *Proc. Asian Solid-State Circuits Conf. (A-SSCC'08)*, Nov. 2008, pp. 125–128.

[4] H. Mizutani and Y. Takayama, "DC-110 GHz MMIC traveling-wave switch," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 5, pp. 840–845, May. 2000.

[5] T. Kosugi, M. Tokumitsu, T. Enoki, M. Muraguchi, A. Hirata, and T. Nagatsuma, "120 GHz Tx/Rx chipset for 10 Gbps wireless applications using 0.1 μm-gate InPHEMTs," in *Proc. Compound Semicond. Integr. Circuit Symp. (CSICS'04)*, Oct. 2004, pp. 171–174.

[6] F. Lin, J. Brinkhoff, D. D. Pham, and X. Yuan, "A low power 60 GHz OOK transceiver system in 90 nm CMOS with innovative on-chip AMC antenna," in *Proc. Asian Solid-State Circuits Conf. (A-SSCC 09)*, Nov. 2009, pp. 349–352.

[7] J. Lee *et al.*, "A low-power fully integrated 60 GHz transceiver system with OOK modulation and on-board antenna assembly," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2009, pp. 316–317.

[8] H.-Y. Chang, M.-F. Lei, C.-S. Lin, Y.-H. Cho, Z.-M. Tsai, and H. Wang, "A 46 GHz direct wide modulation bandwidth ASK modulator in 0.13-μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 9, pp. 691–693, Sep. 2007.

[9] E. Juntunen and M. C. H. Leung *et al.*, "A 60 GHz 38-pJ/bit 3.5-Gb/s 90 nm CMOS OOK digital radio," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 2, pp. 348–355, Feb. 2010.

[10] S. Kraus, I. Kallfass, R. E. Makon, R. Driad, and M. Moyal, "A 20 GHz bipolar latched comparator with improved sensitivity implemented in InP HBT technology," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 3, pp. 707–715, Mar. 2011.

[11] S. X. Shi, A. Ramaligam, D. Wang, and D. Z. Pan, "Latch modeling for statistical timing analysis," in *Proc. Design, Autom. Test Europe (DATE'08)*, Mar. 2008, pp. 1136–1141.

[12] WIN Semiconductor, H01U-00 GaAs 1 um HBT Model Handbook [Online]. Available: http://www.winfoundry.com