THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Optimization of Narrow Bandgap HEMTs for Low-Noise and Low-Power Applications

MIKAEL MALMKVIST

CHALMERS

Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
Göteborg, Sweden 2008

Optimization of Narrow Bandgap HEMTs for
Low-Noise and Low-Power Applications
MIKAEL MALMKVIST

ISBN 978-91-7385-059-9

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie nr 2740
ISSN 0346-718X

Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
SE-412 96 Göteborg, Sweden
Phone: + 46 (0) 31 772 1000

Technical Report MC2-111
ISSN 1652-0769

Cover: From left to right, a FIB-SEM cross-section image of a gate, a SEM image of a 4×50 μm gate-width HEMT, a DC yield map of a fabricated chip, an *I-V* output characteristic with f_T contours and a simplified HEMT small-signal model.

Printed by Chalmers Reproservice
Göteborg, Sweden 2008

Abstract

Owing to its semiconductor properties, such as the electron mobility and the peak velocity, the narrow bandgap high electron mobility transistor (HEMT) provides superior high-frequency and low-noise performance at a low DC power consumption. Successful fabrication of HEMTs requires careful optimization, due to the complex correlation between device design parameters and the DC, RF and noise performance. Even though the optimization is guided by fundamental equations, experimental verification is necessary.

This thesis deals with fabrication, small-signal modeling and optimization of narrow bandgap HEMT technologies based on either InGaAs/InAlAs or InAs/AlSb heterostructures grown on InP substrate. Integration of the InGaAs/InAlAs HEMT with passive components in a microstrip monolithic microwave integrated circuit (MMIC) process has been demonstrated.

The epitaxial layer design of 130 nm gate-length InGaAs/InAlAs HEMTs has been studied with respect to high-frequency and low-noise performance. The device DC, RF and noise performance was improved with increased In content in the channel. An optimum in δ-doping concentration and the Schottky layer thickness was found with respect to RF and noise performance. A too high δ or a too thin Schottky layer thickness degraded device performance significantly.

The electrical properties of InAs/AlSb HEMTs as a function of gate length L_g have been studied. When L_g was reduced from 335 nm to 225 nm, the extrinsic f_T exhibited a $1/L_g$ dependence. In order to account for the relatively high gate-leakage current I_G in the InAs/AlSb HEMT, the conventional field-effect transistor (FET) small-signal model (SSM) was extended. This resulted in an increased modeling accuracy. Moreover, the gate-recess technology of the InAs/AlSb HEMT was carefully investigated, showing either oxidized or non-oxidized gate recess depending on recess depth. By employing an insulated-gate instead of a standard Schottky-gate contact, I_G was reduced by two orders of magnitude, and extrinsic f_T and f_{max} improved by 60% and 50%, respectively.

To demonstrate the feasibility of the HEMT in an MMIC technology, two single-stage amplifiers based on InGaAs/InAlAs HEMTs were designed and fabricated. A broadband feedback amplifier operating at 0-42 GHz with an average noise figure of 3 dB and a W-band amplifier with a gain above 8 dB at 75-94 GHz were demonstrated.

Keywords: InGaAs/InAlAs, InAs/AlSb, heterostructure, high electron mobility transistor (HEMT), semiconductor device fabrication, optimization, noise, power consumption, small-signal modeling, MMIC.

List of Appended Papers

This thesis is based on the work contained in the following papers:

A. M. Malmkvist, S. Wang, and J. Grahn, "Epitaxial optimization of 130-nm gate-length InGaAs/InAlAs/InP HEMTs for high-frequency applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 268-275, 2008.

B. M. Malmkvist, S. Wang, and J. Grahn, "Epitaxial optimization of 130-nm gate-length InGaAs/InAlAs/InP HEMTs for low-noise applications," *submitted to IEEE Transactions on Electron Devices*, 2008.

C. M. Borg, E. Lefebvre, M. Malmkvist, L. Desplanque, X. Wallart, Y. Roelens, G. Dambrine, S. Bollaert, and J. Grahn, "Effect of gate length in InAs/AlSb HEMTs biased for low power or high gain," *accepted for publication in Solid State Electronics*.

D. M. Malmkvist, E. Lefebvre, M. Borg, L. Desplanque, X. Wallart, G. Dambrine, S. Bollaert, and J. Grahn, "Characterization of insulated-gate versus Schottky-gate InAs/AlSb HEMTs," in *Proc. European Microwave Integrated Circuit Conference*, 2007, pp. 24-27.

E. E. Lefebvre, M. Malmkvist, M. Borg, L. Desplanque, X. Wallart, G. Dambrine, S. Bollaert, and J. Grahn, "Gate-recess technology for InAs/AlSb HEMTs," *submitted to IEEE Transactions on Electron Devices*, 2007.

F. M. Malmkvist, E. Lefebvre, M. Borg, L. Desplanque, X. Wallart, G. Dambrine, S. Bollaert, and J. Grahn, "Electrical characterization and small-signal modeling of InAs/AlSb HEMTs for low-noise and high-frequency applications," *submitted to IEEE Transactions on Microwave Theory and Techniques*, 2007.

G. M. Malmkvist, A. Mellberg, N. Rorsman, H. Zirath, and J. Grahn, "Integration of components in a 50-nm pseudomorphic $In_{0.65}Ga_{0.35}As$-$In_{0.40}Al_{0.60}As$-InP HEMT MMIC technology," *Solid State Electronics*, vol. 50, no. 5, pp. 858-864, 2006.

H. M. Malmkvist, A. Mellberg, and J. Grahn, "A W-band MMIC amplifier using 70-nm gate length InP HEMT technology," in *Proc. European Microwave Conference (GAAS)*, 2005, pp. 165-168.

Papers not included due to overlap with the appended papers or being outside the scope of the thesis:

I. O. Engström, M. Malmkvist, Y. Fu, H. Ö. Olafsson, and E. Ö. Sveinbjörnsson, "Thermal emission of electrons from selected s-shell configurations in InAs/GaAs quantum dots," *Applied Physics Letters*, vol. 83, no. 17, pp. 3578-3580, 2003.

II. M. Malmkvist, A. Mellberg, J. Grahn, N. Rorsman and H. Zirath, "A 50-nm gate length InP pseudomorphic HEMT implemented in an MMIC broadband feedback amplifier," in *Proc. IEEE 16th International Conference on Indium Phosphide and Related Materials*, 2004, pp. 386-388.

III. A. Mellberg, M. Malmkvist, J. Grahn, N. Rorsman, and H. Zirath, "Integration of components in a 50 nm InGaAs-InAlAs-InP HEMT process with pseudomorphic $In_{0.65}Ga_{0.35}As$ channel," in *Proc. 34th European Microwave Conference (GAAS)*, 2004, pp. 171-174.

IV. O. Engström, M. Kaniewska, Y. Fu, J. Piscator, and M. Malmkvist, "Thermal emission of electrons from selected s-shell configurations in InAs/GaAs quantum dots," *Applied Physics Letters*, vol. 85, no. 14, pp. 2908-2910, 2004.

V. J. Grahn, P. Starski, M. Malmkvist, M. Fridman, A. Malmros, S. Wang, A. Mellberg, and H. Zirath, "InGaAs-InAlAs-InP HEMT technology for ultra-high frequency and ultra-low noise performance," in *Proc. IEEE 17th International Conference on Indium Phosphide and Related Materials*, 2005, pp. 124-128.

VI. M. Malmkvist, M. Borg, S. Wang, and J. Grahn, "Effect of Schottky layer thickness on DC, RF and noise of 70-nm gate length InP HEMTs," in *Proc. IEEE 18th International Conference on Indium Phosphide and Related Materials*, 2006, pp. 329-331.

VII. M. Borg, E. Lefebvre, M. Malmkvist, L. Desplanque, X. Wallart, Y. Roelens, G. Dambrine, A. Cappy, S. Bollaert, and J. Grahn, "DC and RF performance of 0.2-0.4 μm gate length InAs/AlSb HEMTs," in *Proc. IEEE 19th International Conference on Indium Phosphide and Related Materials*, 2007, pp. 67-70.

VIII. E. Lefebvre, M. Borg, M. Malmkvist, J. Grahn, L. Desplanque, X. Wallart, Y. Roelens, G. Dambrine, A. Cappy, and S. Bollaert, "(Cl_2:Ar) ICP/RIE dry etching of Al(Ga)Sb for AlSb/InAs HEMTs," in *Proc. IEEE 19th International Conference on Indium Phosphide and Related Materials*, 2007, pp. 125-128.

IX. S. Bollaert, L. Desplanque, X. Wallart, Y. Roelens, M. Malmkvist, M. Borg, E. Lefebvre, J. Grahn, D. Smith, and G. Dambrine, "Benchmarking of low band gap III-V based HEMTs and sub-100nm CMOS under low drain voltage regime," in *Proc. European Microwave Integrated Circuit Conference*, 2007, pp. 20-23.

CONTENTS

CHAPTER 1

Introduction

The first high electron mobility transistor (HEMT) was demonstrated in May 1980 by Mimura *et al.* [1]. Since then, the narrow bandgap HEMT has been established as an excellent microwave/mm-wave component, in particular with respect to maximum frequency of oscillation f_{max} and noise figure *NF*. This development of the HEMT has mainly been driven by applications in defense, space and communication.

The first generation HEMTs were based on GaAs/AlGaAs and InGaAs/AlGaAs heterostructures. While the second generation HEMTs are based on InGaAs/InAlAs heterostructures, the next generation may be based on InAs/AlSb and InSb/AlInSb heterostructures. Each generation provides higher channel mobility μ and peak velocity v_{peak}, as well as lower DC power consumption. These properties are essential for the design of a low-noise transistor. Narrow bandgap HEMTs provide superior f_{max} and *NF* performance of any three terminal device available today [2-6]. In particular, the InP-based InGaAs/InAlAs HEMT, with state-of-the-art f_{max} above 1 THz [2] and *NF* of 1.2-1.3 dB at 94 GHz [5, 6], are suitable for microwave and mm-wave low-noise and low-power applications. In parallel, the less expensive GaAs-based InGaAs/InAlAs metamorphic HEMT (MHEMT) technology has improved considerably, and is approaching similar device performance as the InP-based InGaAs/InAlAs HEMT [7, 8]. In demanding niche applications the InP-based InGaAs/InAlAs HEMT technology has become indispensable due to its superior noise performance. One example is ultra-low-noise cryogenic IF amplifiers for radio-astronomy receivers, where requirements on *NF*, gain and DC power consumption are of utmost importance.

Depending on the targeted application, the design and fabrication of the HEMT requires dissimilar approaches. A HEMT aimed for high output power has to be designed differently than a low-noise HEMT. To achieve an ultra-low noise HEMT, successful scaling of the HEMT is essential, since the noise

performance of a HEMT is closely connected to its RF performance. In contrast to the development of CMOS, the development of the HEMT has not been straightforward. Details on the epitaxial structure, the fabrication and the modeling are vital, nevertheless often omitted in reported publications. Optimizing the HEMT for current gain cut-off frequency f_T, f_{max}, low DC power consumption and minimum noise figure NF_{min} requires complex trade-offs in the HEMT design. Similar to other field-effect transistor (FET) technologies, the narrow bandgap HEMTs are improved by scaling of the gate length L_g. When aiming at high-frequency operation, both lateral and vertical optimization in the device architecture is simultaneously required. This will eventually lead to an elevated gate-leakage current I_G and consequently degraded noise performance. The device transport properties, μ and $v_{peak,}$ are other essential parameters to improve. This can be achieved through changes in the HEMT channel material. HEMTs based on pure InAs channel instead of the traditional InGaAs channel are such alternative. Both InAs/InAlAs HEMTs and InAs/AlSb HEMTs have shown promising results with respect to f_T, f_{max} and DC power consumption [9, 10]. Especially interesting is the new generation Sb-based HEMTs, such as the InAs/AlSb HEMT. Together with high μ and v_{peak}, this technology provides superior electron confinement, owing to its staggered type-II energy band alignment. This Sb-based HEMT technology introduces new challenges with respect to scaling, device design, fabrication, and modeling.

This thesis focuses on the InGaAs/InAlAs HEMT and the InAs/AlSb HEMT for low-noise and low-power applications. The aim is to provide a comprehensive picture on the optimization of the two narrow bandgap HEMT technologies with respect to high-frequency, low-noise and ultra-low DC power consumption. The thesis is comprised of nine chapters which are organized as follows: In Chapter 2, a background to the HEMT is provided, including its limitations with respect to frequency and noise performance, and its major applications. The results of the thesis are presented in Chapter 3-8. Chapter 3 is devoted to the narrow bandgap HEMT technology developed in this work, including detailed description of the HEMT epitaxial structures, and a comparison of the two narrow bandgap technologies with respect to fabrication and characterization. In Chapter 4, the small-signal modeling of the two investigated HEMT technologies is discussed. Lateral and vertical device optimization is considered in Chapter 5-6, focusing on the influence of L_g on the InAs/AlSb HEMT performance, and the influence of source-to-drain distance, In content in the channel, δ-doping concentration and Schottky layer thickness on the InGaAs/InAlAs HEMT performance. The importance of a controlled gate-recess technology, especially for InAs/AlSb HEMTs is treated in Chapter 7. In Chapter 8, two types of monolithic microwave integrated circuit (MMIC) demonstrators are presented. In Chapter 9, conclusions are given together with possible future research directions.

CHAPTER 2

Background

This chapter provides a brief background to the narrow bandgap HEMT. The basic HEMT principles are described. More detailed explanations are found in the literature [11-14]. The fundamental performance limitations with respect to high-frequency and low-noise operation are presented. Further details are found in [15-18].

2.1 Basic Principles

A HEMT is based on heterostructures. A heterostructure is formed when two semiconductor materials with different bandgaps and similar lattice constants

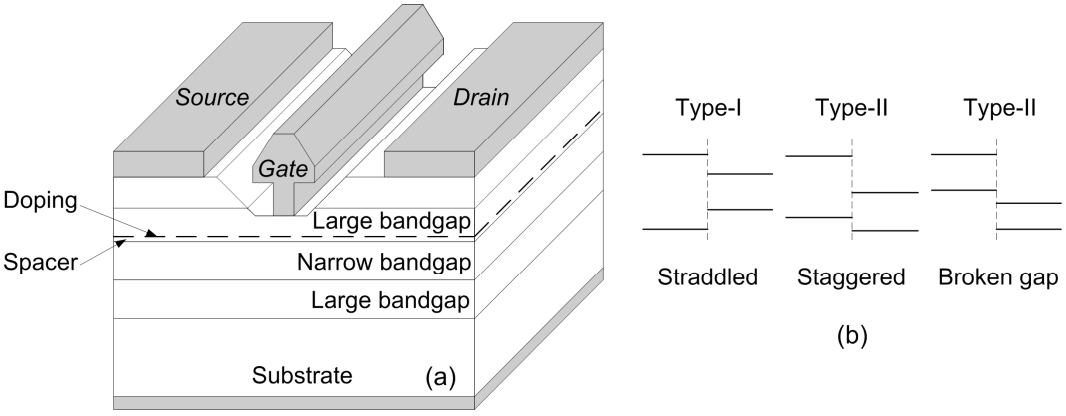

Figure 2.1 *Schematics of (a) the HEMT structure and (b) the different heterostructure energy band alignments: straddled (type-I), staggered and broken gap (type-II).*

are united. The interface between these two layers is called heterojunction.

A schematic of the HEMT is shown in Figure 2.1(a). The HEMT is based on one narrow bandgap channel material sandwiched between two larger bandgap materials. A quantum well (QW) is then formed. Depending on the semiconductor materials, different energy band alignment will occur. The most common one is straddled alignment (type-I), but also staggered alignment and broken-gap alignment exists (type-II), see Figure 2.1(b). The latter type implies either large conduction band- or valence band offset.

The HEMT (Figure 2.1(a)) is a three terminal controlled device. A drain and a source contact control the electric field $\mathcal{E}$, through the drain-to-source voltage V_{DS}. The drain-to-source current I_{DS} of a HEMT is hence governed by a drift current. By applying a voltage on a Schottky-gate contact, the sheet carrier concentration n_s is controlled. Furthermore, n_s depends on several epitaxial design parameters such as the spacer thickness, the doping concentration, the gate-to-channel distance and the conduction band offset.

To create an n-type HEMT, the large bandgap material is doped with donor atoms. Due to the lower conduction band energy of the QW (channel), electrons originating from the donors will transfer into the channel. This will create a two-dimensional electron gas (2DEG). Since the electrons are separated from there donor atoms, the ionized impurity scattering mechanism will decrease significantly compared to a bulk doped semiconductor transistor, e.g. a metal-semiconductor FET (MESFET). This is especially essential at cryogenic temperatures where ionized impurity scattering is the dominating scattering mechanism [19]. As a consequence, μ and v_{peak} will be exceptionally high in HEMTs (see Table 2.1).

2.2 Material Properties

An overview of the different III-V semiconductor compounds (omitting the nitrides) is shown in Figure 2.2 [11, 12, 14, 20]. The first generation HEMTs [1] were based on semiconductor materials with lattice constants around 5.65 Å with GaAs or InGaAs channel on GaAs substrate. By adding In to GaAs ($In_xGa_{1-x}As$), the energy gap and the electron effective mass m_e* are reduced. A direct consequence of the reduction in m_e* is an increased low-field electron mobility μ_e. Simultaneously, the separation between the Γ- and L-valleys in the conduction band increases [21], which is beneficial for v_{peak}. The increased In content in the channel, here defined as [In], will however induce strain due to lattice mismatch. This will eventually cause the material to relax, and severely degrade the channel transport properties. For the first generation HEMTs, the [In] was therefore only up to 20%.

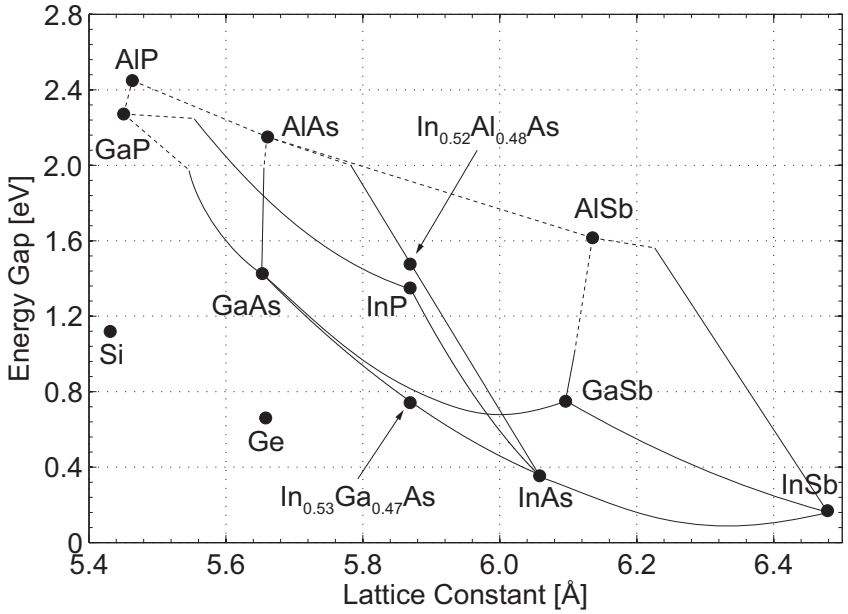

Figure 2.2 *Energy gap versus lattice constant at room temperature for the III-V semiconductors with various alloys (excluding the nitrides) [11, 12, 14, 20]. The dashed lines correspond to an indirect bandgap and the solid lines to a direct bandgap. Si and Ge are included as references.*

The second generation HEMTs are based on $In_xGa_{1-x}As$ channel, lattice-matched (x = 0.53) or pseudomorphic (x > 0.53) on InP substrate. As a result, higher [In] can be used compared to the first generation without material relaxation. Consequently, both higher μ_e and v_{peak} are achieved. In addition, v_{peak} is reached at lower electric fields providing lower DC power consumption. Similarly to the GaAs-based HEMTs, by increasing the [In] above 53%, μ_e and v_{peak} will improve until the channel finally relaxes. For the third generation HEMTs, based on 6.1 Å III-V compounds, both pure InAs and InSb channels are used. However, semi-insulating substrates do not exist. These HEMTs are therefore grown with a metamorphic buffer layer on either InP or GaAs substrate.

In Table 2.1, the crucial parameters for HEMTs with channels based on $In_xGa_{1-x}As$ are presented. The material data is for the channel material only, e.g. the μ_e in the HEMT will be lower than the presented values. In the literature, the values in Table 2.1 vary slightly. Nevertheless, the different trends are clear. The decrease in energy gap $E_{g,channel}$ and the increase in Γ- and L-valley separation $\Delta E_{\Gamma\text{-}L}$, μ_e, m_e* and v_{peak} with increased [In] is evident. It should be noted that the heterojunction conduction band offset ΔE_c is significantly increased when AlSb is used as barrier material (Schottky layer material) due to a staggered type-II energy band alignment.

Table 2.1 *$In_xGa_{1-x}As$ HEMT properties at room temperature [14, 20-22]*

	GaAs HEMT	$In_{0.53}Ga_{0.47}As$ HEMT	$In_{0.8}Ga_{0.2}As$ HEMT	InAs HEMT
Barrier material	$Al_{0.3}Ga_{0.7}As$	$In_{0.52}Al_{0.48}As$	$In_{0.4}Al_{0.6}As$	AlSb
$E_{g,\,channel}$ [eV]	1.42	0.75	0.50	0.36
ΔE_c [eV]	0.22	0.52	0.85	1.35
$\Delta E_{\Gamma\text{-}L}$ [eV]	0.29	0.44	0.60	0.73
μ_e [$cm^2/V{\cdot}s$]	8500	14000	20000	33000
m_e^*/m_0	0.064	0.041	0.027	0.022
v_{peak} [cm/s]	2.1×10^7	2.7×10^7	3.0×10^7	3.8×10^7

2.3 High-Frequency Limitations

The transit-time of a HEMT, decisive for the frequency performance, is improved with increased v_{peak}. High [In] in the channel should therefore provide superior device performance at a given L_g due to the elevated v_{peak} (see Table 2.1). However, increased scattering due to strain-induced defects may degrade the performance. Furthermore, the modulation efficiency, i.e. the ability to modulate I_{DS} without modulating immobile and low-velocity charge, needs to be considered as well [15]. When an extrinsic perspective is taken into account, parasitic (access) resistances and capacitances have to be considered. This will result in a total transit time t_T expressed by Nguyen *et al.* [23] as:

$$t_T = t_{pad} + t_{fringe} + t_i + t_{drain} = \frac{C_{pad}}{g_m W} + \frac{C_{fringe}}{g_{mi}} + \frac{C_{gs}}{g_{mi}} + t_{drain} = \frac{1}{2\pi f_T}, \tag{2.1}$$

where C_{pad} is the device pad capacitance, C_{fringe} the gate fringing capacitance, C_{gs} the gate-to-source capacitance, g_m and g_{mi} the transconductance and intrinsic transconductance, respectively, and W the gate width. t_{drain} introduces a delay time corresponding to the extension of the depletion region on the drain side of the gate.

The most straightforward method to increase f_T is through scaling by shrinking device geometries through a reduction of L_g, hence reducing C_{gs}, and by changing semiconductor material e.g. increased [In] (increased μ_e, v_{peak}). However, when L_g is reduced, second order effects, such as output conductance g_{ds} and source- and drain resistance R_s and R_d becomes significant. In addition, to maintain control of the carriers in the channel with reduced L_g, the gate-to-channel distance should be reduced correspondingly. An expression

for f_T, including the effects from access resistances and output conductance was reported by Tasker *et al.* [24]:

$$f_T = \frac{g_{mi}/(2\pi)}{(C_{gs}+C_{gd})\left[1+(R_s+R_d)\cdot g_{ds}\right]+C_{gd}g_{mi}(R_s+R_d)}, \tag{2.2}$$

where C_{gd} is the gate-to-drain capacitance. As long as the parasitic resistances are kept low, f_T is only governed by g_{mi}, C_{gs} and C_{gd}.

A crucial figure-of-merit for analog devices is f_{max}, which is the limiting frequency for a device to accomplish amplification. As reported by Das [25], f_{max} is closely related to f_T:

$$f_{max} = \frac{f_T}{\sqrt{4\frac{g_{ds}}{g_{mi}}\left[g_{mi}R_i + \frac{R_s+R_g}{1/g_{mi}+R_s}\right] + \frac{4C_{gd}}{5C_{gs}}\left[1+2.5\frac{C_{gd}}{C_{gs}}\right](1+g_{mi}R_s)^2}}. \tag{2.3}$$

The increased complexity of f_{max} compared to f_T is obvious. Consequently, it is not as straightforward to maximize f_{max} for a HEMT. In addition to maximizing f_T through high g_{mi} and low C_{gs} and C_{gd}, low g_{ds} and low gate resistance R_g are crucial. This will transform into a high voltage gain ($\sim g_{mi}/g_{ds}$). When L_g is reduced, several trade-offs are introduced, such as reduced L_g versus an increased R_g and increased C_{gd}/C_{gs} ratio [26].

Today's superior HEMT technology with respect to RF and noise performance is based on InGaAs/InAlAs HEMTs. The state-of-the-art intrinsic f_T (pad capacitances de-embedded) is 562 GHz (f_{max} = 330 GHz) reported by Yamashita *et al.* [3] with an L_g of 25 nm. An intrinsic f_{max} of 1.1 THz (f_T = 385 GHz) was recently reported by Lai *et al.* [2] with L_g = 35 nm. This is the highest f_{max} reported for any three terminal device. One method to compare f_T results of HEMTs with different L_g is to use the $f_T \times L_g$ product as a figure-of-merit [27, 28]. The $f_T \times L_g$ products for the above mentioned results were 14 GHz·µm and 13.5 GHz·µm, respectively. However, at L_g = 100 nm, an $f_T \times L_g$ product of 38 GHz·µm (f_T = 380 GHz) is typical for InGaAs/InAlAs HEMTs [4]. The large degradation in $f_T \times L_g$ product with reduced L_g, illustrates the scaling difficulties for ultra-short gate-length HEMTs.

The InAs/AlSb HEMT provides improved HEMT material properties (v_{peak}, μ_e, ΔE_c) compared to InGaAs/InAlAs HEMTs. In addition to the expected increased RF performance, one major benefit of the InAs/AlSb HEMT is the significantly reduced DC power consumption while maintaining a high f_T. The highest reported intrinsic f_T and f_{max} for InAs/AlSb HEMTs are 270 GHz and 280 GHz, respectively, with an L_g of 100 nm [29-31]. These values are lower than for 100 nm gate-length InGaAs/InAlAs HEMTs, mainly due to a relatively high I_G and g_{ds} which limits the device RF and noise performance. A

complete compilation of state-of-the-art f_T is shown in Paper C. To improve the RF performance of narrow bandgap HEMTs additionally, proper scaling and further technology assessment are necessary.

2.4 Noise Limitations

The physical origin of noise in HEMTs is related to random electric charge fluctuations such as irregular variations in current, voltage, resistance, etc [16, 18]. Thermal (Johnson) noise [32, 33] is generated in the source and drain contacts. Shot noise is generated when electrons cross the Schottky barrier from the gate to the channel, causing a gate-leakage current. Noise generated in the channel is caused by real-space transfer, intervalley scattering and impact ionization etc [16].

The HEMT figure-of-merit for noise is the noise figure *NF* or equivalent noise temperature T_e. *NF* is defined as the degradation in the signal-to-noise ratio as a signal passes through the device, with the source temperature T_0 = 290 K:

$$NF = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}/N_{in}}{S_{in}G_a/\left(N_a + N_{in}G_a\right)} = 1 + \frac{N_a}{N_{in}G_a} = 1 + \frac{T_e}{T_0}, \tag{2.4}$$

where S_{in}/N_{in} and S_{out}/N_{out} are the signal-to-noise power ratios at the input and output of the device, respectively. $N_{in} = kT_0B$, where k is Boltzmann's constant and B is the bandwidth. N_a is the noise generated in the device, G_a is the

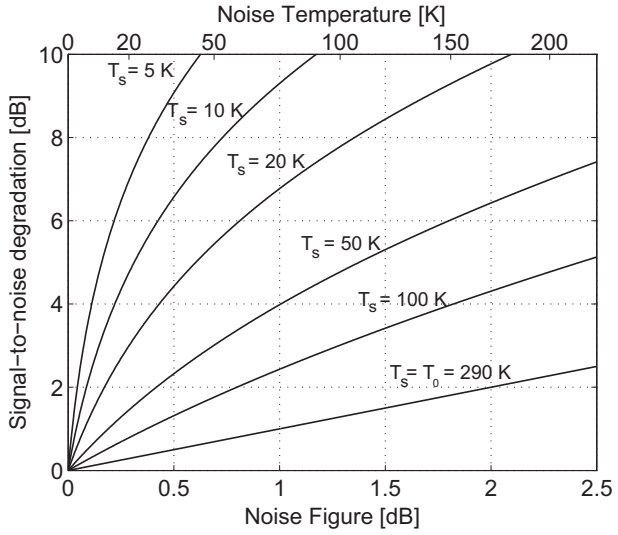

Figure 2.3 *Signal-to-noise degradation as a function of the device noise figure NF (and equivalent noise temperature T_e) with different source temperatures. T_s = 290 K corresponds to the definition of NF.*

associated gain and $N_a = kT_eG_aB$. If the source temperature is lower than T_0, the signal-to-noise degradation will be larger than the *NF* of the device, as shown in Figure 2.3. This clearly illustrates the importance of a low *NF* in applications where the noise source (e.g. antenna noise temperature) is lower than T_0.

Noise models are helpful for predicting device noise performance as well as for MMIC LNA design. Noise modeling of HEMTs with respect to small-signal parameters has been widely discussed in the literature [34-36]. A relatively simple empirical expression for $NF_{\min}$ was suggested by Fukui [34]:

$$NF_{\min} = 1 + 2\pi f K_f C_{gs} \sqrt{\frac{R_s + R_g}{g_{mi}}} \times 10^{-3}, \tag{2.5}$$

where K_f is a fitting factor and f is the frequency. It is clear from Eq. (2.5) that R_g, R_s and C_{gs} should be minimized and g_{mi} should be maximized to achieve as low $NF_{\min}$ as possible.

To describe the noise performance of a transistor completely, *NF* is not sufficient. One common set of noise parameters to describe noise of a device are minimum noise temperature $T_{\min}$ (= $(NF_{\min}-1)\times T_0$), noise resistance R_n, and optimal source impedance $Z_{opt} = R_{opt}+jX_{opt}$. Pospieszalski derived expressions of these parameters [35], with an approximated $T_{\min}$ according to:

$$T_{\min} = 2f \frac{2\pi C_{gs}}{g_{mi}} \sqrt{g_{ds} T_d R_i T_g}, \tag{2.6}$$

where T_g and T_d correspond to the equivalent noise temperatures of the Schottky series resistance R_i and R_{ds} (= $1/g_{ds}$), respectively. Eq. (2.6) can be further simplified through empirical parameter relations [37] by minimizing:

$$f(V_{DS}, V_{GS}) \cong \frac{\sqrt{I_{DS}}}{g_m}. \tag{2.7}$$

Thus, to achieve low microwave/mm-wave noise, a high g_m at a low I_{DS} should be obtained.

The InGaAs/InAlAs HEMT technology provides the lowest microwave/ mm-wave *NF* of any transistor, with $NF_{\min}$ as low as 1.3 dB and associated gain of 8 dB at 94 GHz [5]. For InAs/AlSb HEMT, only a few reports on device noise have been reported [38-40] with $NF_{\min}$ below 1 dB up to 25 GHz. Similar to the high-frequency limitations of the InAs/AlSb HEMT technology, the limiting factor for noise is the high I_G. The benefit of using InAs/AlSb

HEMTs compared to the InGaAs/InAlAs HEMT is that minimum *NF* is obtained at or below a V_{DS} of only 0.2 V. For the InGaAs/InAlAs HEMT, the corresponding value is 0.6-0.7 V. The InAs/AlSb HEMT technology is hence promising for low-noise applications where ultra-low DC power consumption is required.

2.5 Applications

The possibility to use devices at increasingly higher frequencies permits receivers with shorter integration time and smaller antenna size. Recent circuit records provide amplifiers above 300 GHz [41], with impressive 15 dB gain at 340 GHz [2]. The superior f_T, f_{max} and NF_{min} at microwave, mm- and sub-mm-wave frequencies of InGaAs/InAlAs HEMTs makes the technology attractive for applications such as radio-astronomy receivers, passive imaging and satellite-to-satellite or ground-to-satellite communication systems. These applications are mainly driven by performance rather than cost.

In radio astronomy, ultra-low signal levels are detected. The required integration time to reach a certain signal-to-noise ratio is proportional to the square of the receiver noise [42] and is significantly reduced with a small decrease in *NF*. This requires extremely low *NF* of the low-noise amplifier (LNA) in the receiver. The LNA is either positioned directly after the antenna, or as an IF amplifier subsequent to a mixer. The total receiver noise is essentially governed by the *NF* of the first-stage transistor of the LNA. An InGaAs/InAlAs HEMT is the preferred choice. In Figure 2.4, an image of an

Figure 2.4 *Atacama large millimeter/submillimeter array, located 5000 m above sea level on the Chajnantor site, Atacama, Chile. Courtesy: European organization for astronomical research in the southern hemisphere (ESO), produced for ALMA.*

array-based radio-astronomy receiver is shown, the Atacama large millimeter/submillimeter array (ALMA) (30-950 GHz). In ALMA, InGaAs/InAlAs HEMTs are used in the IF amplifier.

An important factor when selecting frequency band for a specific application is the atmospheric attenuation. Atmospheric attenuation minimum (atmospheric window) occurs at several microwave and mm-wave frequencies, for instance at 94, 140, and 220 GHz. These frequency bands are therefore suitable for passive imaging applications. A passive mm-wave image sensor detects mm-wave electromagnetic radiation from a specific object and visualizes it. This enables the detection of an object normally not possible to detect by visual light. One application is camera looking through fog [43], guiding airplanes when landing in difficult weather conditions. Another important application is camera for security precautions, where concealed weapons can be detected through e.g. clothes [44, 45]. Other interesting frequencies are 183 GHz and 184 GHz where water (H_2O) and ozone (O_3) absorption lines are present, respectively. At these frequencies, radiometers provide data for weather monitoring and global warming models [46]. Regarding low DC power consumption applications, the InAs/AlSb HEMT technology is of particular interest due to its excellent RF performance at low supply voltages of 0.1-0.2 V. For example, in phased-array radar systems such as space based radar where the numbers of sensing circuit elements can be in the range of 10^5-10^6 [47], it is of great interest to reduce the DC power consumption of each LNA due to power constrains, size and cost.

CHAPTER 3

Narrow Bandgap HEMT Technology

Two different narrow bandgap technologies have been investigated: the type-I InGaAs/InAlAs HEMT and the type-II InAs/AlSb HEMT. Both structures were grown by molecular beam epitaxy (MBE). A high yield InGaAs/InAlAs HEMT fabrication process has been developed. A modification of the process made fabrication of InAs/AlSb HEMTs possible. The two technologies have been compared with respect to epitaxial structure, fabrication and final device performance.

3.1 Epitaxial Structures

In Figure 3.1, technology computer aided design (TCAD) simulated energy-band diagrams at thermal equilibrium, of the two different technologies are

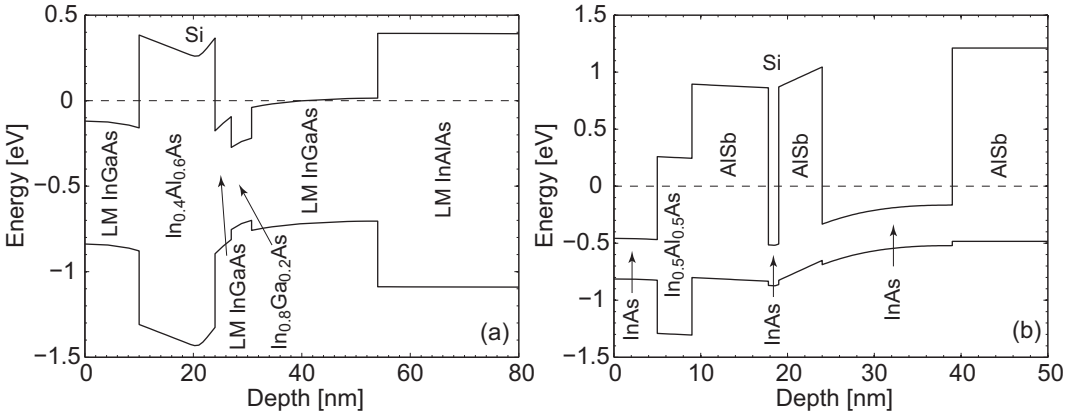

Figure 3.1 *TCAD simulated energy-band diagrams at thermal equilibrium and 300 K for (a) an InGaAs/InAlAs HEMT (LM = lattice-matched to InP) and (b) an InAs/AlSb HEMT.*

depicted (for the top epitaxial layers). The type-I and type-II energy band alignments are seen in Figure 3.1(a) and (b), respectively.

There are two essential differences between the epitaxial structures of the two studied HEMT technologies. First, the InGaAs/InAlAs HEMT has a type-I energy band alignment whereas the InAs/AlSb HEMT has a type-II energy band alignment. Second, the InGaAs/InAlAs HEMT was grown with a buffer layer lattice matched to an InP substrate, whereas the InAs/AlSb HEMT was grown with a metamorphic buffer on an InP substrate.

Two features desirable for high RF performance are large conduction band offset ΔE_c and high In content in the channel [In]. For the InGaAs/InAlAs HEMT, high Al content (60%) in the InAlAs Schottky layer was used to maximize ΔE_c. To maximize [In], a composite channel was utilized. This approach promotes high [In] while avoiding material relaxation. The composite channel included a short period of InAs/$In_{0.53}Ga_{0.47}As$ superlattice, sandwiched between two lattice matched (In = 53%) InGaAs layers. Note that the superlattice in Figure 3.1(a) is represented by a single 3.8 nm $In_{0.8}Ga_{0.2}As$ layer. For the InAs/AlSb HEMT, both the ΔE_c and the [In] are higher compared to the InGaAs/InAlAs HEMT. The InAs/AlSb material combination provides superior ΔE_c to any III-V semiconductor compound, due to the staggered type-II alignment with a ΔE_c = 1.35 eV. However, the type-II alignment makes it impossible to confine holes in the InAs channel.

A detailed overview of the InGaAs/InAlAs HEMT epitaxial structure (grown at Chalmers, Sweden) is provided in Table 3.1. The different nominal values with respect to Schottky layer thickness, δ-doping concentration, superlattice thickness and total channel thickness correspond to the epitaxial optimization explained in detail in Chapter 6.

Table 3.1 *InGaAs/InAlAs HEMT epitaxial structure*

Layer	Material	Thickness
Cap layer	$In_{0.53}Ga_{0.47}As$	10 nm
Schottky layer	$In_{0.4}Al_{0.6}As$	9-13 nm
δ-doping	Si	$3\text{-}7\times10^{12}$ cm^{-2}
Spacer	$In_{0.4}Al_{0.6}As$	3 nm
Channel	$In_{0.53}Ga_{0.47}As$	2 nm
Channel (superlattice)	InAs/$In_{0.53}Ga_{0.47}As$	3.8-9.5 nm
Channel	$In_{0.53}Ga_{0.47}As$	8.5-24.2 nm
Buffer layer	$In_{0.52}Al_{0.48}As$	500 nm
Substrate	S.I. InP	

The epitaxial structure of the InAs/AlSb HEMT (grown at IEMN, France) is summarized in Table 3.2. Three features had to be added to the InAs/AlSb HEMT epitaxial structure in comparison to the InGaAs/InAlAs HEMT. This was due to the fact that the AlSb suffers from strong oxidation when exposed to air [48], the difficulties to obtain n-type AlSb by using Si as a dopant, and the type-II staggered alignment. First, by growing an AlGaSb buffer layer on top of the AlSb buffer layer, a chemically stable shallow mesa floor can be achieved [49]. This layer is less reactive in air than the underlying AlSb and will prevent strong oxidation. Second, as Si would provide holes and not electrons if placed directly in the AlSb Schottky layer [49], a Si-doped InAs QW was placed in the Schottky layer to obtain an n-type device. The alignment of the InAs QW in the HEMT structure is illustrated in Figure 3.1(b). Te-doped AlSb Schottky layer is another common method used to obtain n-type InAs/AlSb HEMTs [50]. Finally, an $In_{0.5}Al_{0.5}As$ protection layer was placed between the AlSb Schottky layer and the InAs cap layer, see Figure 3.1(b). This protection layer should protect the AlSb Schottky layer from oxidizing during the gate-recess etch. Since no natural energy barrier for holes exists (type-II), this layer should also act as a hole blocking barrier to prevent a hole leakage current flowing from the channel to the gate.

Table 3.2 *InAs/AlSb HEMT epitaxial structure*

Layer	Material	Thickness
Cap layer	InAs	5 nm
Protection layer	$In_{0.5}Al_{0.5}As$	4 nm
Schottky layer	AlSb	10 nm
Doping layer	InAs	2 monolayers
δ-doping	Si	4.5×10^{12} cm^{-2}
Doping layer	InAs	2 monolayers
Spacer	AlSb	5 nm
Channel	InAs	15 nm
HEMT buffer	AlSb	50 nm
Metamorphic buffer	$Al_{0.8}Ga_{0.2}Sb$	250 nm
Metamorphic buffer	AlSb	750 nm
Smoothing layer	$In_{0.5}Al_{0.5}As$	100 nm
Substrate	S.I. InP	

3.2 Material Characterization

Prior to device fabrication the quality of the epitaxial structures was verified. Important material properties to monitor were interface quality, [In] (in the case of InGaAs/InAlAs HEMT) and carrier transport properties. The material quality was verified with X-ray diffraction (XRD) and Hall measurements at room temperature. XRD verified the layer structure and Hall measurements provided the basic HEMT properties μ_e and n_s.

In Figure 3.2, typical XRD results of the InGaAs/InAlAs HEMT and the InAs/AlSb HEMT are shown. The angles obtained from the XRD measurements were normalized to the InP substrate. Figure 3.2(a) reveals a slightly pseudomorphic buffer layer, good channel interface and a tensile strained Schottky layer. The relatively broad peak observed in Figure 3.2(b), corresponding to the AlSb buffer and the Schottky layer, is due to the metamorphic buffer.

When designing the HEMT epitaxial structure high μ_e and high n_s are highly desirable. However, a trade-off exists between μ_e and n_s. The Hall measurements in this thesis were performed without removing the cap layer. The measured μ_e and n_s is therefore a combination from both the channel and the cap layer. Generally, the InGaAs/InAlAs HEMTs had a μ_e slightly higher than 10,000 $cm^2/V{\cdot}s$ and an n_s around 4.0×10^{12} cm^{-2}. For the InAs/AlSb HEMT the corresponding numbers were 21,600 $cm^2/V{\cdot}s$ and 2.1×10^{12} cm^{-2}, respectively. These values compare well with reported numbers for similar narrow bandgap HEMT structures [14, 50].

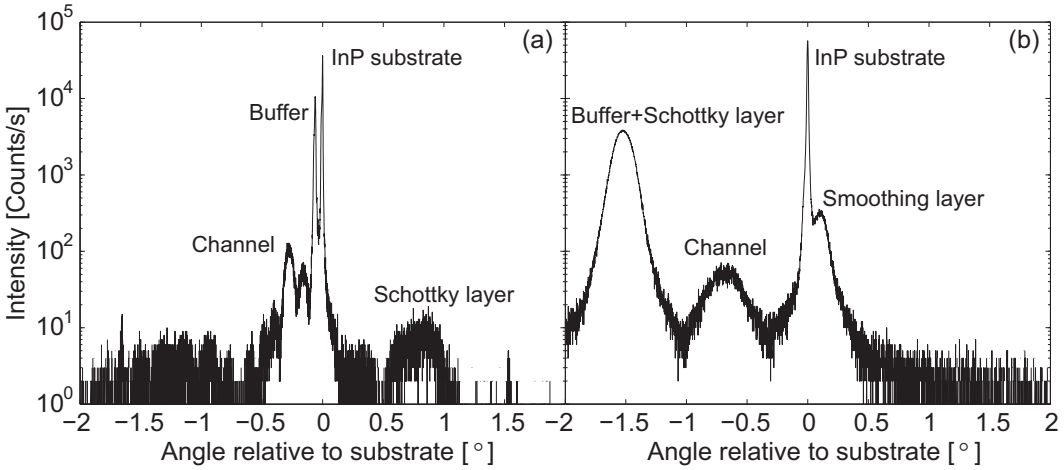

Figure 3.2 *X-ray diffraction measurement on the (004) plane of (a) an InGaAs/InAlAs HEMT and (b) an InAs/AlSb HEMT. Both measured results were normalized to the InP substrate.*

3.3 Device Fabrication

The fabrication process was similar for both InGaAs/InAlAs and InAs/AlSb HEMTs. Both optical- and electron-beam lithography (EBL) techniques were combined. The fabrication sequence included mesa isolation, ohmic contact formation, gate definition by EBL, gate-recess etch, Ti/Pt/Au gate metal deposition, Ti/Au contact pad sputtering or evaporation, reactively sputtered Si_3N_4 passivation and finally 3 µm thick Au plating. All metal depositions were finalized with a lift-off process. For the MMIC process, five additional steps were required: TaN thin-film resistors (TFRs) [51], a second metal layer, lapping, via-hole etching and backside Au plating. The complete fabrication-process sequence is illustrated in Figure 3.3. Details about the MMIC process are described in Paper G.

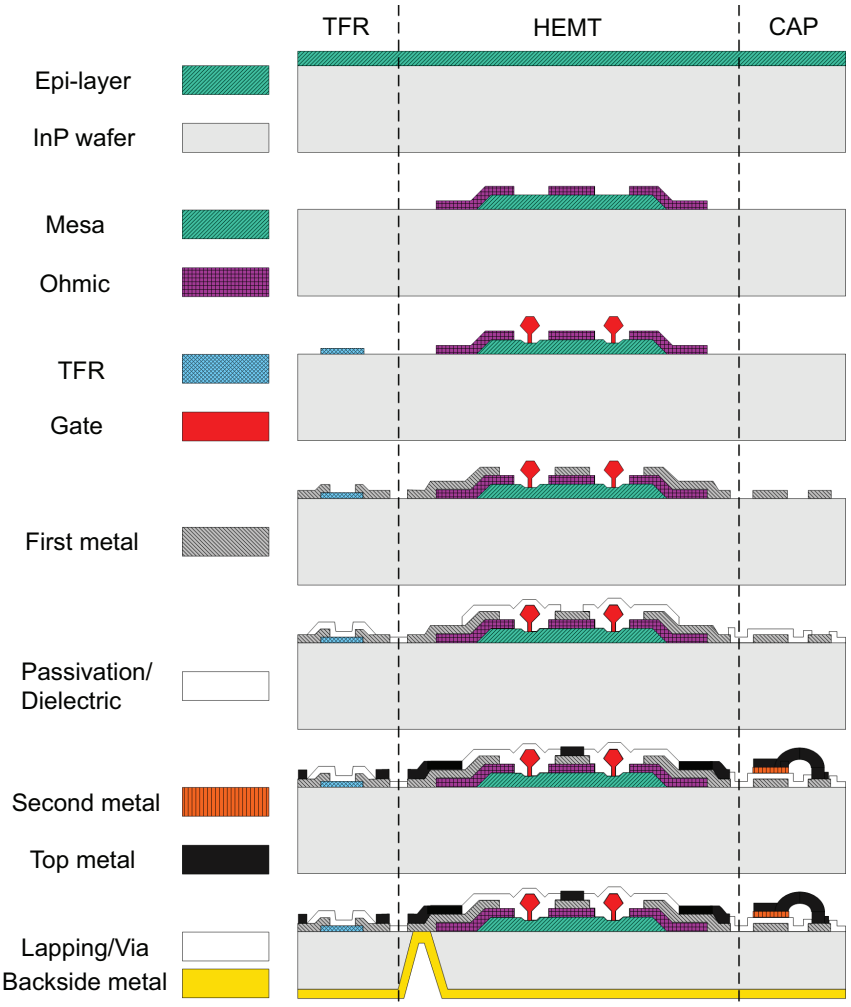

Figure 3.3 *MMIC process sequence for the investigated narrow bandgap technologies, including a HEMT, a thin-film resistor (TFR) and a capacitor (CAP).*

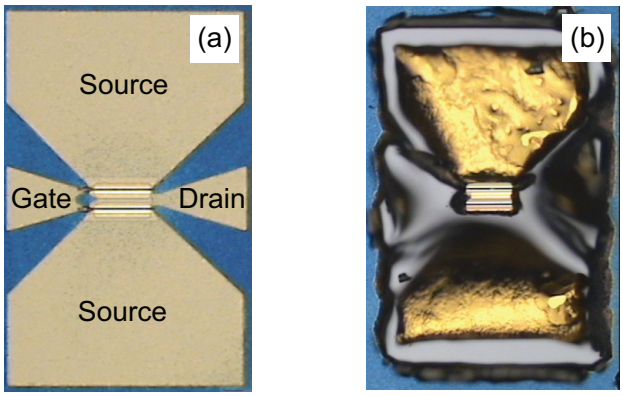

Figure 3.4 *Optical microscope pictures of an InAs/AlSb HEMT (a) with and (b) without AlSb oxidation, caused by different mesa-etch depths.*

A few but important modifications were required when fabricating InAs/AlSb HEMT in comparison to InGaAs/InAlAs HEMT. This was related to the severe oxidation of AlSb when exposed to air. First, the mesa isolation for the InAs/AlSb HEMTs had to be performed by utilizing a dry-etching technique, instead of the conventional wet etching. For this purpose, a Cl_2-based dry etch using inductively coupled plasma/reactive ion etch (ICP/RIE) was developed [52]. With this method, an unacceptably large lateral under-etching was avoided. To avoid AlSb oxidation, the dry etch had to stop in the more chemically stable $Al_{0.8}Ga_{0.2}Sb$ layer. An example of the InAs/AlSb HEMT with and without AlSb oxidation is shown in Figure 3.4. As observed in Figure 3.4(b), the contact pads were completely destroyed after a too deep mesa etch. This was due to oxidation of the AlSb under the contact pads, causing the pads to be lifted off. The second modification concerned the ohmic contacts. For the InGaAs/InAlAs HEMT, a Ni/Ge/Au metal stack was used whereas a Pd/Pt/Au metal stack was used for the InAs/AlSb HEMTs. This provides lower contact resistance as well as less in-diffusion of Au [53] for the InAs/AlSb HEMTs. Furthermore, the annealing temperature was lowered from 320°C to 275°C for the InAs/AlSb HEMT compared to the InGaAs/InAlAs HEMT. Generally, for both the InGaAs/InAlAs and the InAs/AlSb HEMT, the obtained contact resistance was < 0.2 Ω·mm and the sheet resistance was 140-160 Ω/sq. These values were obtained through the transmission line method (TLM).

The gate fabrication step, including EBL, gate-recess etch, gate-metal deposition and lift-off, was the most critical fabrication step. It both influenced the final device DC, RF and noise performance, but was also a considerable source of yield degradation. Both a bi-layer and a tri-layer resist stack were used for the gate definition. Either a bi-layer resist stack of PMMA (NANO950k PMMA 4% in anisole)/copolymer P(MMA-MAA) (NANO copolymer 10% in ethyllactate) was used, or a tri-layer resist stack with an

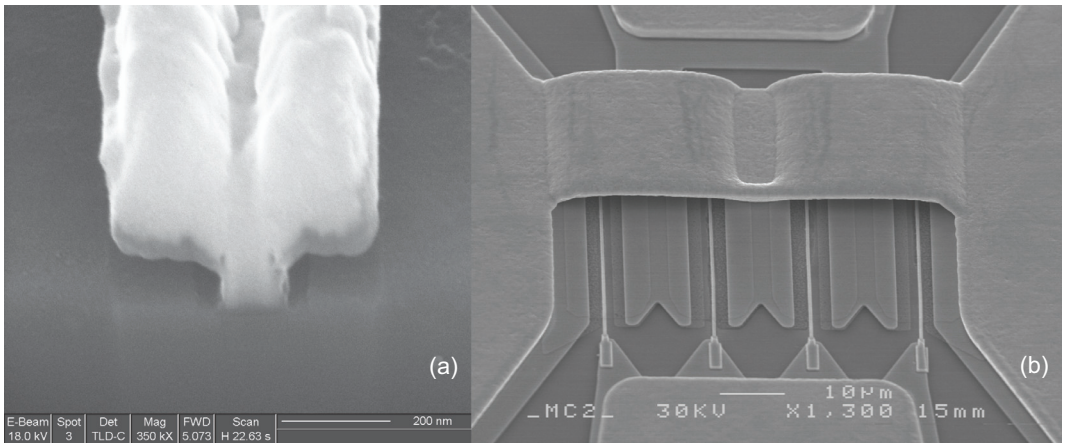

Figure 3.5 *(a) FIB-SEM cross-section image of a gate and (b) SEM image of an InGaAs/InAlAs HEMT.*

additional top layer of PMMA (NANO950k PMMA 2% in anisole). The tri-layer stack facilitates the subsequent lift-off procedure. The gate-recess width and depth are decisive for the final device DC, RF and noise performance. This is considered separately in Chapter 7.

The physical L_g of the fabricated HEMTs was measured by focused ion beam - scanning electron microscopy (FIB-SEM). A FIB-SEM cross-section image of a 130 nm gate is shown in Figure 3.5(a). In Figure 3.5(b), a SEM image of a finalized 4×50 µm InGaAs/InAlAs HEMT is shown, including Au plated air-bridges.

3.4 Device Characterization

The devices were mainly characterized by on-wafer DC and RF measurements at room temperature, but also in a cryogenic environment. This made it possible to analyze, optimize, model and finally integrate the components in an MMIC demonstrator.

3.4.1 Uniformity and Yield Analysis

To be able to select representative components for device analysis, wafer mapping was conducted to obtain an overview of the HEMT performance across the wafer.

On-wafer DC measurements of devices with gate widths ranging from 30 µm up to 100 µm, were performed by using a Cascade MicroTech automatic probe station and an HP4156B semiconductor parameter analyzer.

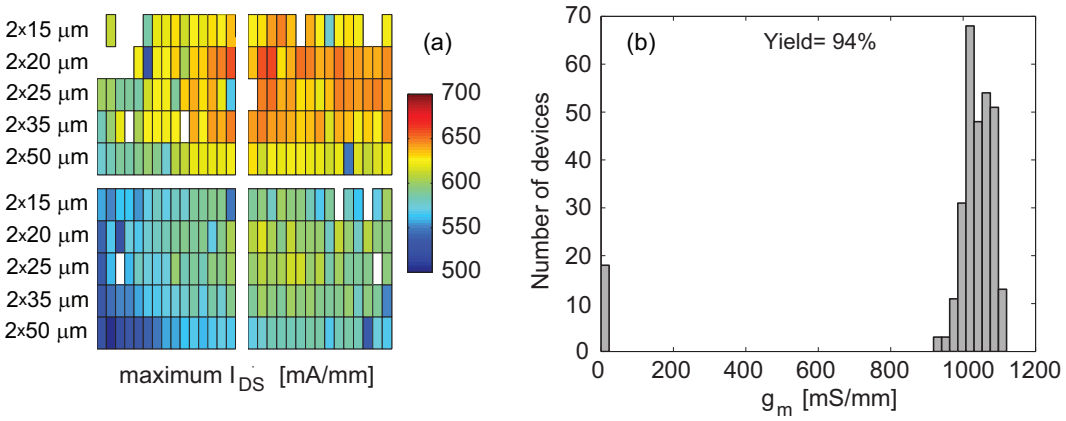

Figure 3.6 *DC wafer mapping of 300 InGaAs/InAlAs HEMTs at V_{DS} = 1.0 V showing (a) the maximum I_{DS} and (b) a statistical distribution of the corresponding g_m, revealing a device yield above 90%.*

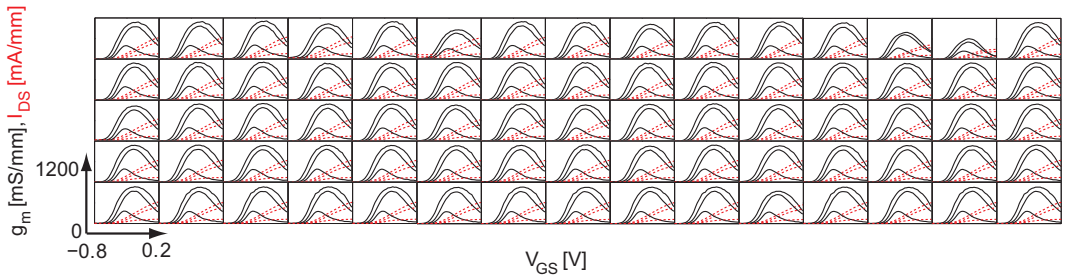

Figure 3.7 *$I_{DS}(V_{GS})$ and $g_m(V_{GS})$ at V_{DS} = 0.3, 0.7 and 1.0 V of 75 InGaAs/InAlAs HEMTs (from the upper right quarter of Figure 3.6(a)).*

DC wafer mapping of InGaAs/InAlAs HEMTs is shown in Figure 3.6. The criteria for a functional device were a minimum g_m of 800 mS/mm, an I_{DS} larger than 500 mA/mm, and a maximum pinch-off current of 1% of maximum I_{DS}. The defective devices are indicated as white squares in Figure 3.6(a). The devices with lowest maximum I_{DS} were found at the edge on the lower part of the chip, and most defective devices were found towards the top edge of the chip. The highest maximum I_{DS} achieved was 700 mA/mm, whereas the majority of the devices exhibited maximum I_{DS} in the range between 600 mA/mm and 650 mA/mm. In Figure 3.6(b), a statistical distribution of the measured peak g_m is shown (defective devices were assigned a g_m-value equal to zero). Most devices revealed a peak g_m in the range 1050 mS/mm to 1100 mS/mm, at a drain-to-source voltage V_{DS} of 1.0 V. A DC yield > 90% was obtained.

In Figure 3.7, an overview of the measured g_m and I_{DS} as a function of gate-to-drain voltage V_{GS} at V_{DS} = 0.3, 0.7 and 1.0 V is illustrated. This shows the uniformity of the devices corresponding to the upper right quarter of the wafer map in Figure 3.6(a). All devices assigned as working exhibited excellent uniformity with respect to g_m, I_{DS} and threshold voltage V_{TH} for all V_{DS}.

3.4.2 DC and RF Characterization

The DC characteristics give a first indication of the device frequency and noise performance. High g_m is beneficial for the high-frequency performance, whereas high I_G is negative for the noise performance.

In Figure 3.8, g_m and I_G as a function of V_{GS} for InGaAs/InAlAs HEMT and InAs/AlSb HEMT are compared. Note the difference in maximum V_{DS} in Figure 3.8(a), and the factor 1000 difference in y-scale in Figure 3.8(b). Maximum g_m of 1500 mS/mm at V_{DS} = 0.6 V and maximum g_m of 1200 mS/mm at V_{DS} = 1.0 V were obtained for the InAs/AlSb and InGaAs/InAlAs HEMT, respectively. In the literature, g_m as high as 3000 mS/mm at V_{DS} = 0.6 V with 60 nm gate-length InGaAs/InAlAs HEMTs, have been reported [54]. This was accomplished through lateral scaling, and a three-step recess etching for advanced vertical scaling. By using a double-gate HEMT on a transferred substrate, with L_g equal to 100 nm and 280 nm, Wichmann *et al.* [55] obtained a g_m = 2650 mS/mm. However, this required a complex fabrication process and also increased the gate capacitances, which limited the HEMT RF performance.

A significant difference in device DC characteristics is observed between the two investigated narrow bandgap HEMT technologies in Figure 3.8. Peak $g_m(V_{DS})$ for the InGaAs/InAlAs HEMT appears at approximately the same V_{GS} regardless of V_{DS}, whereas the peak $g_m(V_{DS})$ for the InAs/AlSb HEMT shifts towards more negative V_{GS} as V_{DS} is increased above 0.3 V, see Figure 3.8(a). This behavior is explained by the presence of an increased DC output

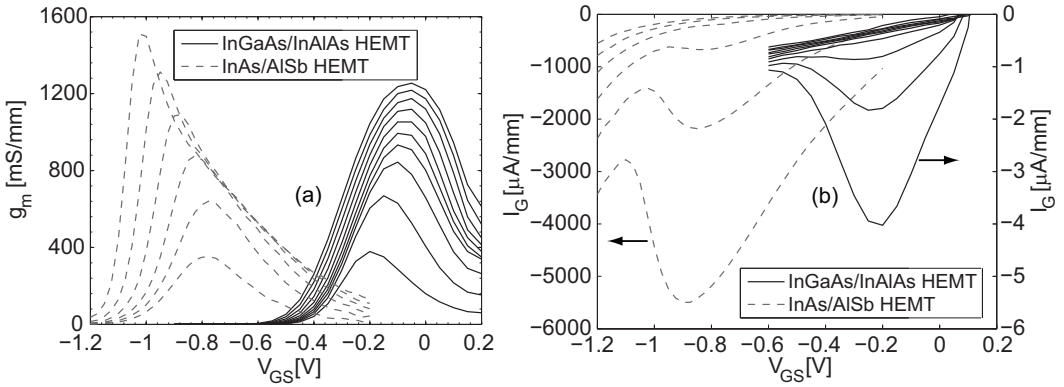

Figure 3.8 *DC characteristics of 225 nm gate-length InAs/AlSb HEMTs (dashed) at V_{DS}: 0.1 V to 0.6 V, and 130 nm gate-length InGaAs/InAlAs HEMTs (solid) at V_{DS}: 0.1 V to 1.0 V, in steps of 0.1 V. (a) $g_m(V_{GS})$ and (b) $I_G(V_{GS})$. Note the factor 1000 difference in the y-scale in (b).*

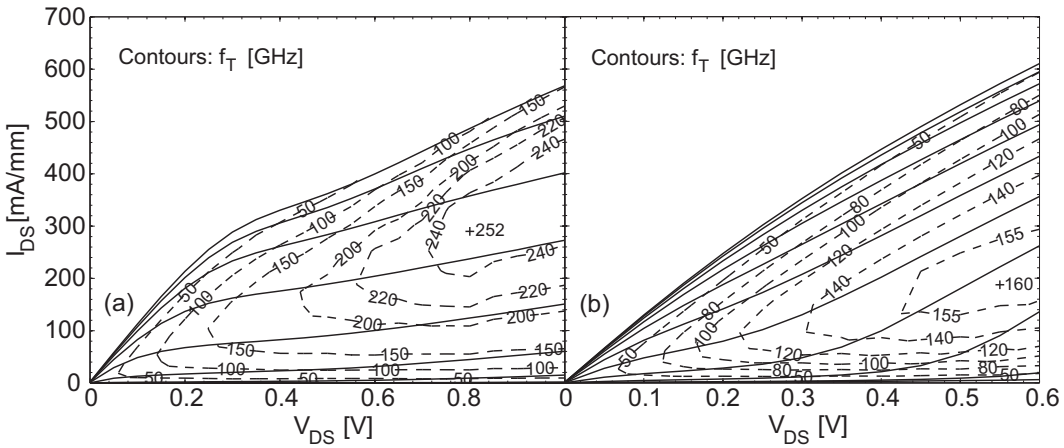

Figure 3.9 *I-V output characteristics with f_T contours for (a) 130 nm gate-length InGaAs/InAlAs HEMT with 1.0 µm source-to-drain distance and (b) 225 nm gate-length InAs/AlSb HEMT with 2.3 µm source-to-drain distance.*

conductance G_{DS}, caused by the severe impact ionization present in the InAs/AlSb HEMTs. As a result the increased g_m is mainly an artificial improvement. A high level of impact ionization will result in a deteriorated RF and noise performance. Several approaches have been considered to remove or minimize the amount of impact-ionization generated holes, either by using a back gate, a sub-channel or a thin channel (< 10 nm) [56-58]. However, the back gate increased the gate capacitance, and the μ_e was reduced in the thin channel. Both effects are negative for the RF performance.

In Figure 3.8(b), $I_G(V_{GS})$ is compared for the two technologies. The characteristic "bell-shape" is observed for both technologies. This indicates the presence of impact ionization [59]. However, the I_G values are approximately 1000 times higher for the InAs/AlSb HEMT. This is a typical level of I_G present in InAs/AlSb HEMTs [60].

In Figure 3.9, the *I-V* output characteristics, including contour plots of f_T, are shown for 130 nm gate-length InGaAs/InAlAs and 225 nm gate-length InAs/AlSb HEMTs with 2×50 µm gate-width (similar pad layout). The source-to-drain distance L_{SD} was 1.0 µm and 2.3 µm, respectively. Note that all extracted RF figures-of-merit in this work are extrinsic values (pad capacitances not de-embedded). Despite the longer L_g and L_{SD} for the InAs/AlSb HEMT, both technologies exhibited an f_T of approximately 120 GHz at a low V_{DS} of 0.2 V.

S-parameters were measured on-wafer up to 50 GHz with coplanar probes using an Anritsu 37397C vector network analyzer. f_T was obtained through extrapolation of the current gain $|h_{21}|^2$ with a -20 dB/decade slope. f_{max} was obtained from either modeled maximum available gain *MAG*, as shown in Figure 3.10, or by -20 dB/decade extrapolation of the unilateral power gain (Mason's gain) *U*.

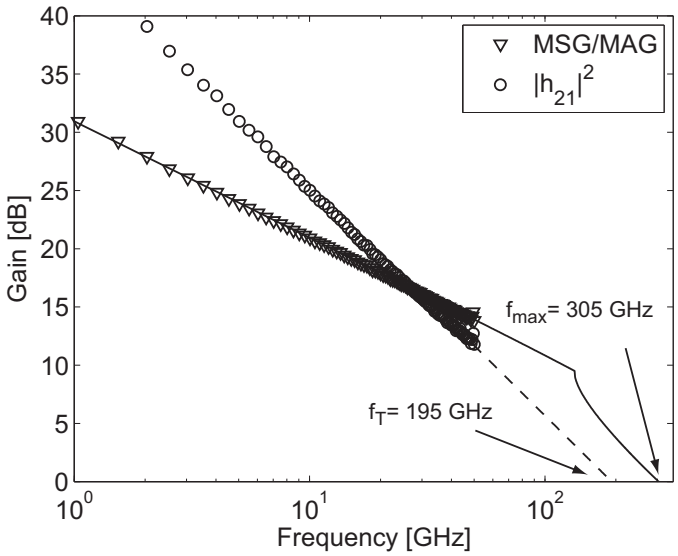

Figure 3.10 *Extraction of f_T and f_{max} for a 130 nm gate-length InGaAs/InAlAs HEMT through extrapolation from measured S-parameters.*

In Figure 3.11, f_T and $f_T \times L_g$ versus the DC power consumption are compared for the 130 nm gate-length InGaAs/InAlAs HEMT and the 225 nm gate-length InAs/AlSb HEMT. The InAs/AlSb HEMT exhibited similar DC power consumption for an f_T up to 100 GHz, see Figure 3.11(a). A more appropriate comparison is the $f_T \times L_g$ product, shown in Figure 3.11(b). This comparison clearly illustrates the advantage of using the InAs/AlSb HEMT technology for low DC power consumption.

The measured DC results can also be used as a first indication of the final noise performance of the HEMT. According to Eq. (2.7), NF_{min} should be achieved by minimizing the square root of I_{DS} over g_m. By using this expression, it should be possible to estimate the bias point where the lowest *NF* occurs. In Figure 3.12, contour plots of the square root of I_{DS} over g_m as a function of V_{DS} and V_{GS} are shown for an InGaAs/InAlAs HEMT. In the same figure, the bias point for measured minimum 50Ω noise figure $NF_{50\Omega}$ is highlighted for the same device. Indeed, lowest $NF_{50\Omega}$ was obtained where Eq. (2.7) had its minimum. This verified that minimizing Eq. (2.7) is a good approach to obtain low noise HEMTs. As a consequence, the HEMT with the lowest *NF* can (to first order) be selected on the basis of DC measurements.

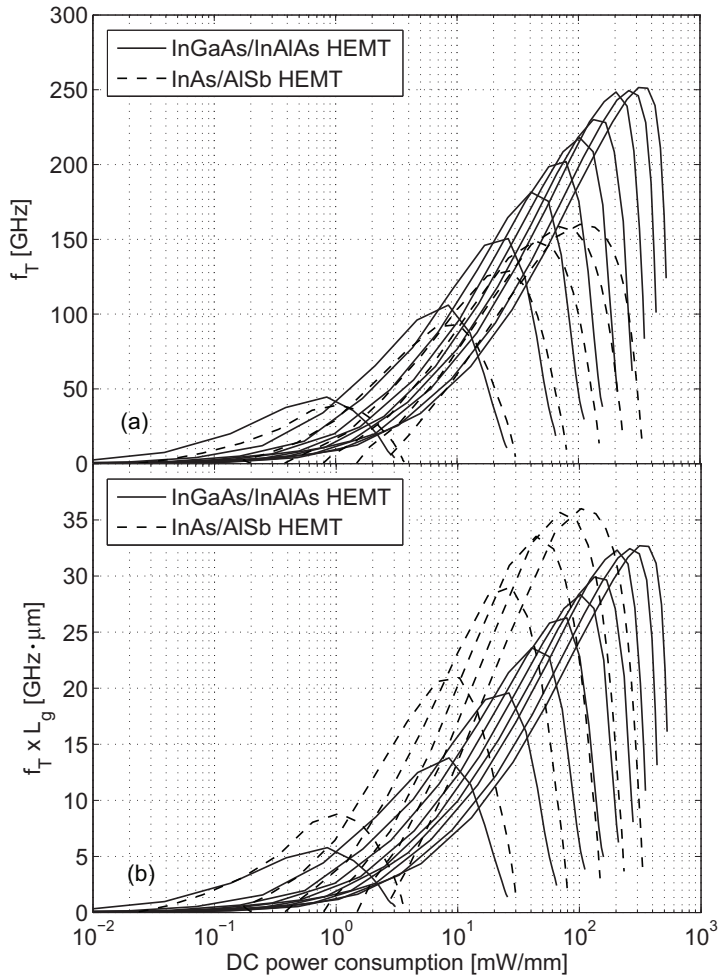

Figure 3.11 *Comparison of the (a) extrinsic f_T and (b) extrinsic $f_T \times L_g$ product versus DC power consumption for 130 nm gate-length InGaAs/InAlAs HEMTs and 225 nm gate-length InAs/AlSb HEMTs.*

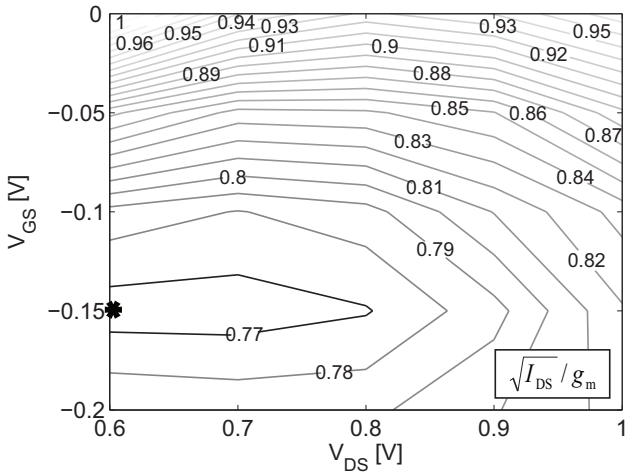

Figure 3.12 *Estimation of the bias point corresponding to minimum NF. The bias point corresponding to the measured $NF_{50\Omega}$ is marked with a star (*).*

3.4.3 Cryogenic Characterization

One essential feature of the HEMTs is the absence of carrier freeze-out at cryogenic temperatures. The electron energy levels in the channel are well below the donor level in the Schottky layer, and the ionization energy of the dopants is very low (a few meV) [61]. Therefore, sufficient n_s will sustain even at cryogenic temperatures. I_{DS} is thus limited by the saturation velocity v_{sat}. Therefore, even though μ_e is increasing with a factor 3-4 and n_s is approximately constant at cryogenic temperatures compared to room temperature [62], I_{DS} was only increased at low V_{DS}, see Figure 3.13(a). This is a bias corresponding to electron velocities below v_{sat}. Figure 3.13(b) shows an increased peak g_m of approximately 10% at 30 K compared to 300 K. This is a result of improved electron confinement as well as reduced access resistances. Another consequence of the improved carrier confinement with decreasing temperature was a shift in V_{TH} towards higher V_{GS}, see Figure 3.13(b).

The observed negative resistance for high V_{GS} and V_{DS} around 0.4 V in Figure 3.13(a) is often referred to as a kink effect. This effect is also seen at intermediate temperatures. Similar behavior has been reported by others [63, 64], also at room temperature [65]. It has been shown that this effect can be reduced or even removed by using an InP etch stop layer for the gate-recess etch [65]. This kink effect should not be mixed with increased I_{DS} at high V_{DS}, when the device is biased close to pinch-off (sometimes referred to as a kink effect as well [66]). The origin of the kink effect has been suggested to be related to trapping effects, both due to surface charge [65] and deep-level traps [63, 67]. The kink-effect observed in the *I-V* output characteristic is thus related to the material and/or the fabrication process.

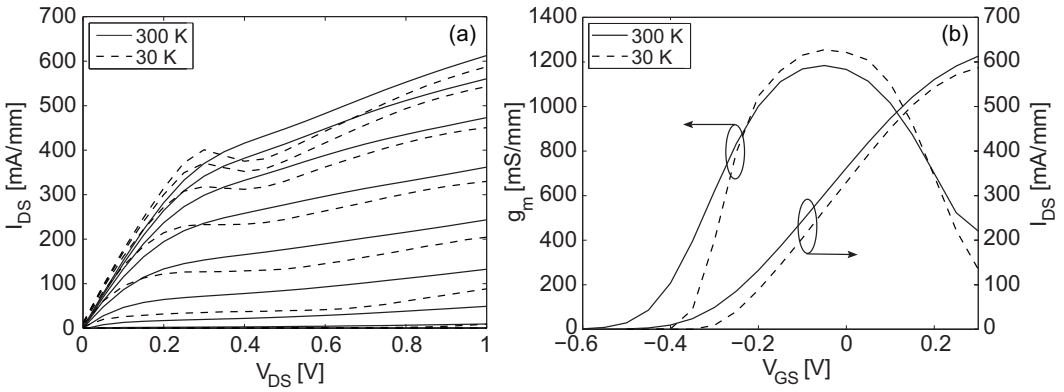

Figure 3.13 *InGaAs/InAlAs HEMT (a) I-V output characteristic at V_{GS}: -0.5 V to 0.3 V in steps of 0.1 V and (b) $g_m(V_{GS})$ and I-V transfer characteristics at V_{DS} = 1.0 V, at 300 K and 30 K.*

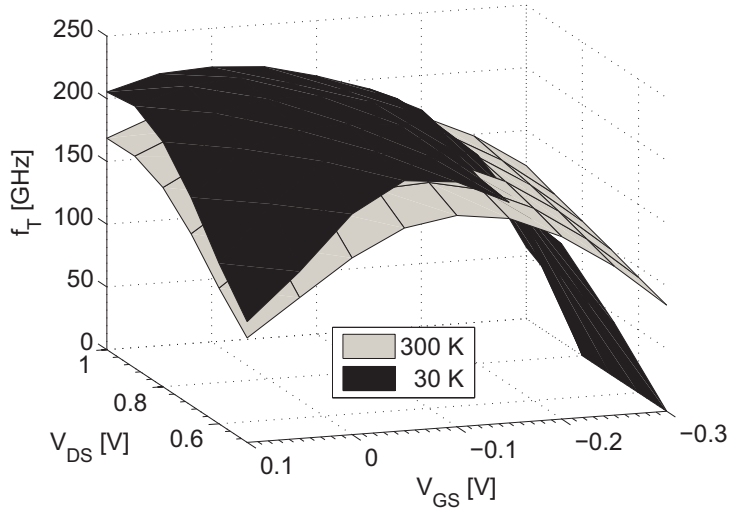

Figure 3.14 *Extrinsic $f_T(V_{GS}, V_{DS})$ at 300 K and 30 K for an InGaAs/InAlAs HEMT.*

In Figure 3.14, a comparison of f_T at 300 K and 30 K for an InGaAs/InAlAs HEMT is shown. Maximum f_T and f_{max} increased by 15% when the temperature was reduced from 300 K to 30 K. The trend in f_T as a function of bias is closely connected to the bias dependence of g_m. This is the reason for the lower f_T observed at 30 K for the lowest V_{GS}.

A more detailed investigation, comparing cryogenic and room temperature performance for 0.8 µm gate-length and 0.2 µm gate-length InGaAs/InAlAs HEMTs with varying [In], has been performed by Lai *et al.* [68]. In that study, f_T and f_{max} increased by 15-30% at 40 K compared to room temperature. The improvement with respect to high-frequency performance with reduced temperature was less significant for shorter L_g (0.2 µm) compared to longer L_g (0.8 µm). An improvement by 15% for L_g = 0.2 µm compares well with the results obtained for the 130 nm gate-length InGaAs/InAlAs HEMTs studied in this thesis.

CHAPTER 4

Device Modeling

In this chapter, small-signal modeling and noise modeling of narrow bandgap HEMTs are presented. In particular, the influence of I_G on the *S*-parameters and the noise performance is discussed.

4.1 Small-Signal Modeling

When optimizing devices or circuits, the small-signal model (SSM) is useful to understand and predict the device frequency limitations and noise behavior. Furthermore, the SSM is the basis for both noise modeling and large-signal modeling.

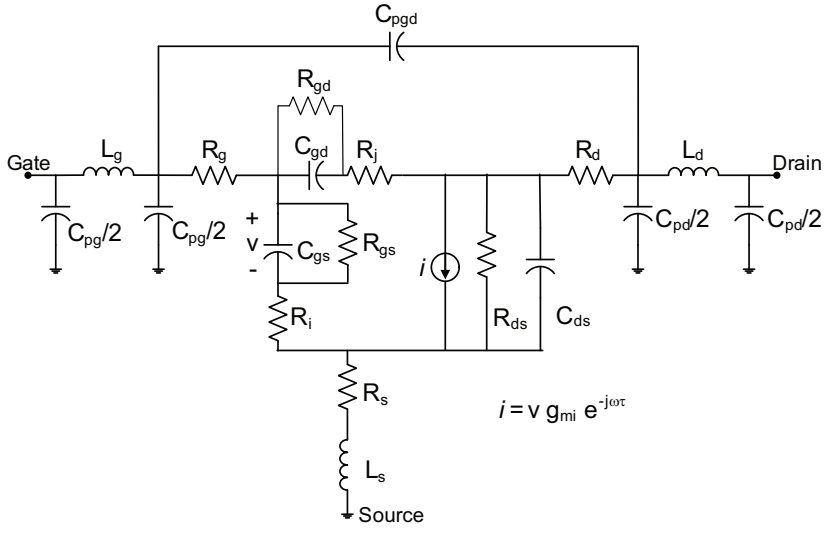

Figure 4.1 *Small-signal model of the narrow bandgap HEMT.*

In Figure 4.1, a SSM applicable to both the InGaAs/InAlAs HEMT and the InAs/AlSb HEMT is presented. In order to model both RF and noise behavior accurately, the relatively high I_G has to be considered in the SSM for the InAs/AlSb HEMTs. Therefore the SSM parameters R_{gs} and R_{gd} are required for this technology, in particular to improve the SSM accuracy for frequencies up to 10 GHz.

To correctly analyze the device behavior, an accurate model extraction technique is essential. For the extraction of the small-signal parameters in this thesis, a direct extraction method was used [69, 70] to obtain initial parameters for a subsequent optimization procedure [71]. The conventional SSM parameters were extracted as described in [70]. The additional parameters R_{gs} and R_{gd} were extracted from the *Y*-parameters at very low frequencies (10-100 MHz) after de-embedding the extrinsic parameters. More specifically, R_{gs} was extracted from the real part of $Y_{11}+Y_{12}$ and R_{gd} from the real part of $-Y_{12}$ [72]. However, direct extraction of R_{gd} and R_{gs} was not sufficient since the accuracy of the measured *S*-parameters at these low frequencies is relatively poor. Consequently, an optimization procedure involving an error function was required. The normalized error function was defined as:

$$\varepsilon = \frac{1}{4N}\sum_{j=1}^{2}\sum_{i=1}^{2}\frac{1}{\max\left|S_{ij}^{meas}\right|^2}\sum_{k=1}^{N}\left|S_{ij}^{meas}(k)-S_{ij}^{model}(k)\right|^2 \tag{4.1}$$

where N is the number of frequency points, k is the frequency index, and S_{ij}^{meas} and S_{ij}^{model} are the measured and the modeled *S*-parameters, respectively.

In Figure 4.2, the modeled and the measured *S*-parameters of a 2×50 µm gate-width InAs/AlSb HEMT are depicted for two different bias points. One bias point where the lowest $NF_{50\Omega}$ was measured, and one at the maximum geometric mean of f_T and f_{max}, here defined as $min(NF_{50\Omega})$ and $max(f_T, f_{max})$, respectively. The normalized error function ε as a function of V_{DS} and V_{GS} is shown in Figure 4.3 with the error at $min(NF_{50\Omega})$ and $max(f_T, f_{max})$ highlighted. The peculiar behavior in S_{21} and S_{22} at low frequencies for $max(f_T, f_{max})$ was due to the extensive impact ionization at V_{DS} = 0.5 V. This will appear as an inductive behavior in S_{22} and as a reduced S_{21} at low frequencies [73]. This effect was also observed in InGaAs/InAlAs HEMTs, but not as pronounced. As a consequence of the increased impact ionization at high V_{DS}, ε increases with V_{DS}, see Figure 4.3.

Two different approaches to model the impact ionization have been suggested in the literature, either by adding a voltage-controlled current source and an *RC*-cell in parallel with R_{ds} [73], or by adding an *LR*-series in parallel with R_{ds} in the SSM [74]. However, for the InAs/AlSb HEMTs an additional resistive behavior in S_{12} is observed for high V_{DS} at low frequencies, see Figure 4.2. To account for this behavior, a feedback resistance in addition to an *LR*-series in parallel with R_{ds} was used (Paper F).

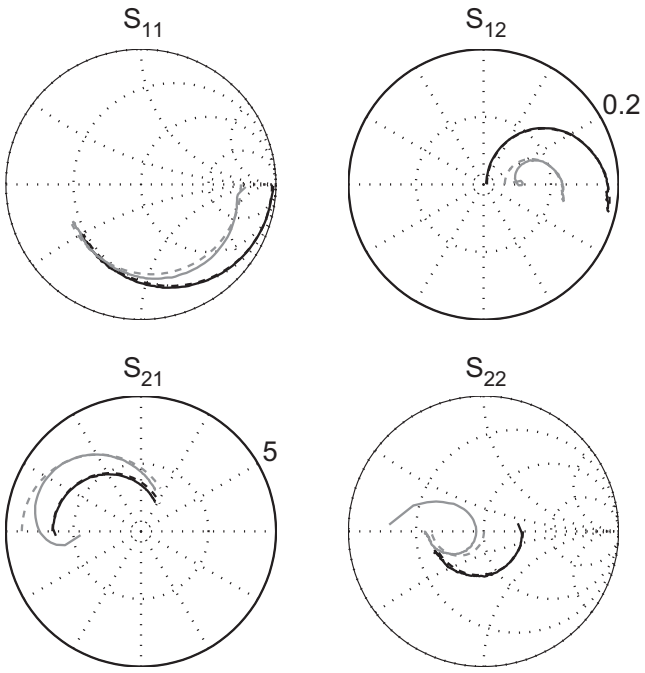

Figure 4.2 *Measured (solid) and modeled (dashed) S-parameters for a 2×50 μm gate-width InAs/AlSb HEMT biased for either low noise (black) or high frequency (grey) operation.*

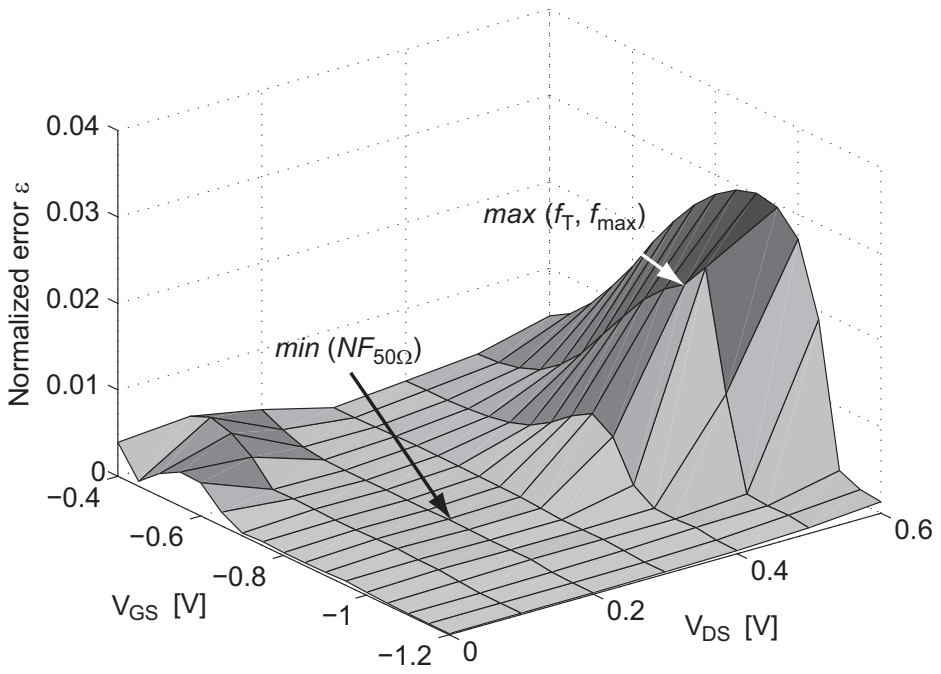

Figure 4.3 *Normalized error of the extracted S-parameters versus bias for a 2×50 μm gate-width InAs/AlSb HEMT. max(f_T, f_{max}) and min($NF_{50Ω}$) are the ε corresponding to the bias points in Figure 4.2.*

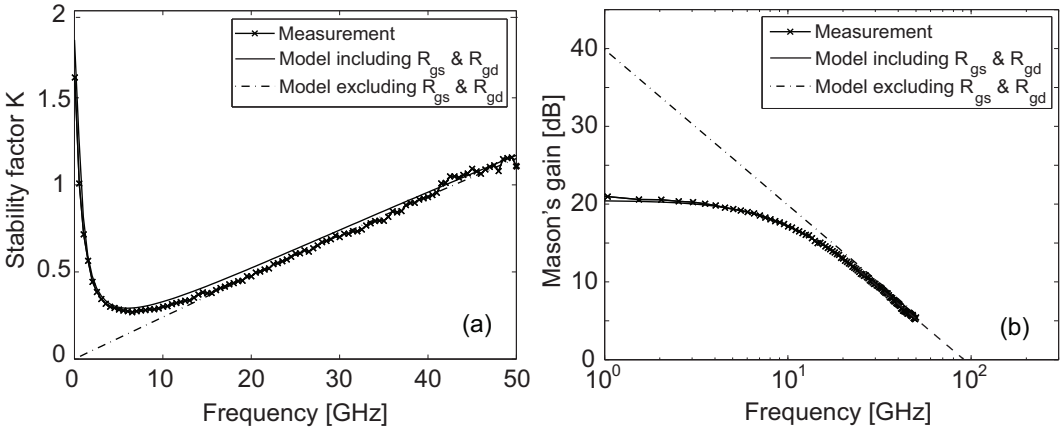

Figure 4.4 *Measured and modeled (a) K-factor and (b) Mason's gain for an InAs/AlSb HEMT.*

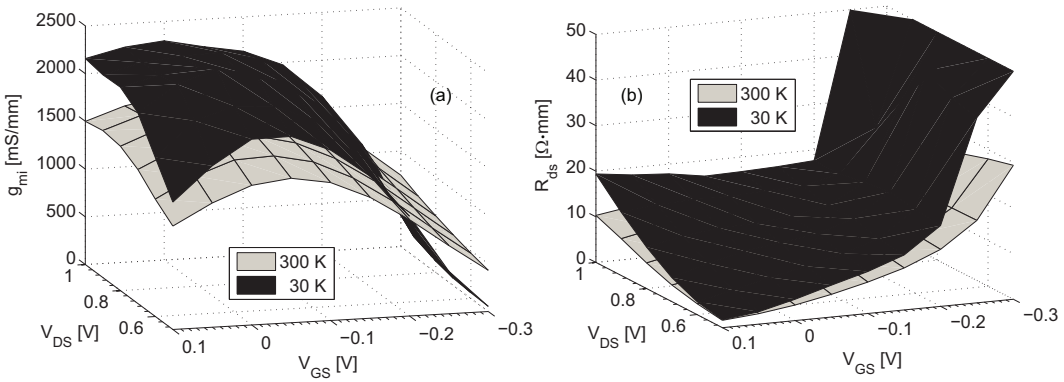

Figure 4.5 *(a) $g_{mi}(V_{GS}, V_{DS})$ and (b) $R_{ds}(V_{GS}, V_{DS})$ at 300 K and 30 K of an InGaAs/InAlAs HEMT.*

The SSM fitted excellent to measurements at a low-noise bias ($NF_{50\Omega}$) where impact ionization was of minor concern, see Figure 4.2. The importance of the additional SSM parameters R_{gs} and R_{gd} for the InAs/AlSb HEMT becomes clear when comparing the measured and modeled stability factor K and Mason's gain with or without these elements included in the SSM. This is illustrated in Figure 4.4. The discrepancy between the measured and modeled K and U is observed essentially at frequencies below 10 GHz. The observed deviation between measured and modeled U in Figure 4.4(b) was also present for the InGaAs/InAlAs HEMTs, however not to the same extent. Indeed, for the InAs/AlSb HEMTs, including R_{gs} and R_{gd} in the SSM provided a more accurate SSM, presented in Paper F. Earlier reported results have only used the conventional FET SSM [27, 75].

As already stated, HEMTs are especially suited for cryogenic applications. It is therefore interesting to compare the extracted small-signal parameters at room temperature and at cryogenic temperature. In Figure 4.5, the intrinsic

transconductance g_{mi} and R_{ds} as a function of V_{DS} and V_{GS} at 300 K and 30 K for an InGaAs/InAlAs HEMT are displayed. A significant increase in g_{mi} as well as an increased R_{ds} are observed when reducing the temperature from 300 K to 30 K. Both the increase and the change in shape of g_{mi} with reduced temperature correspond well with the observed f_T in Figure 3.14. Murti *et al.* [64] studied the temperature dependence on small-signal parameters of InGaAs/InAlAs HEMTs, showing similar trends with respect to g_{mi} and R_{ds} as observed in Figure 4.5.

4.2 Noise Modeling

The device noise performance in this thesis was modeled by utilizing the Pospieszalski model [35]. This model is based on the noise two-port representation developed by Rothe and Dahlke [76]. The Pospieszalski model is based on the SSM parameters, where R_i and R_{ds} are the noise sources. The noise is assumed to be of thermal origin only, and the noise generated by R_i and R_{ds} are represented by equivalent noise temperatures T_g and T_d, respectively.

$NF_{50\Omega}$ was measured on-wafer using an Agilent N8975A noise figure analyzer. For the investigated HEMTs, T_g was set to ambient temperature. T_d was obtained through a fitting of the measured $NF_{50\Omega}$ to the Pospieszalski model, using the Agilent's Design System (ADS) software.

The Pospieszalski model does not take into account I_G. This is however required for the InAs/AlSb HEMTs. Two different noise models exist which account for I_G in HEMTs and MESFETs: Either a model with an additional shot noise source [77] or a model with a resistor [78] added at the input, both

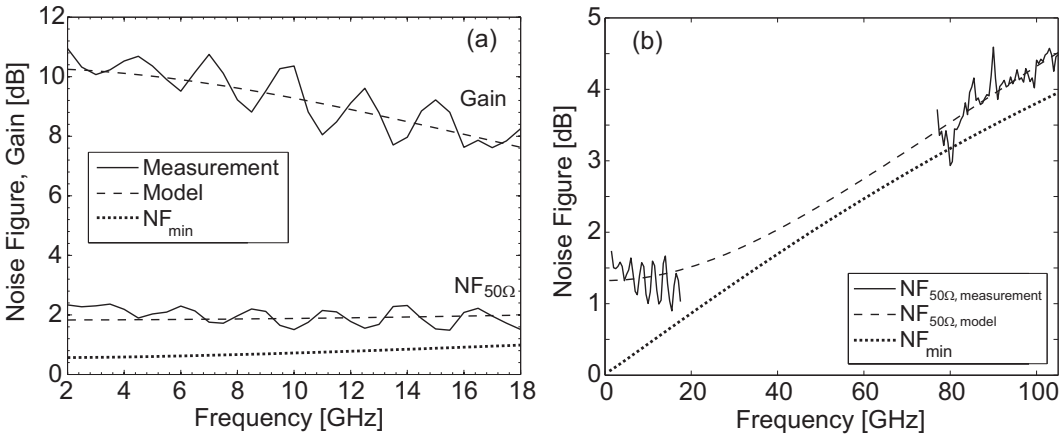

Figure 4.6 *Measured and modeled noise for 2×50 µm gate width (a) 225 nm gate-length InAs/AlSb HEMT and (b) 130 nm gate-length InGaAs/InAlAs HEMT.*

shunting R_i and C_{gs}. In this thesis, an adaption to the latter method has been applied. In the SSM shown in Figure 4.1, R_{gs} and R_{gd} models the noise contribution originating from I_G. The corresponding equivalent temperatures were set to the ambient temperature. In Figure 4.6(a), the measured and modeled $NF_{50\Omega}$ and associated gain are shown as well as NF_{min} for a 225 nm gate-length InAs/AlSb HEMT. Very good agreement between measured and modeled $NF_{50\Omega}$ was obtained with this modeling approach. An NF_{min} less than 1 dB was achieved between 2-18 GHz at V_{DS} = 0.2 V, meaning that both a relatively low NF_{min} and a low DC power consumption were achieved. These noise results are comparable to state-of-the-art for this technology [38, 39].

In Figure 4.6(b), measured and modeled $NF_{50\Omega}$ for a 130 nm gate-length InGaAs/InAlAs HEMT with a gate-width of 2×50 µm is shown. The $NF_{50\Omega}$ measurements were performed both at 2-18 GHz and at 75-110 GHz. The modeled $NF_{50\Omega}$ was only fitted to the measured $NF_{50\Omega}$ in the low-frequency region (2-18 GHz) by using a moving average of the measured $NF_{50\Omega}$. This was necessary due to presence of a standing-wave pattern caused by the 50Ω mismatch, see Figure 4.6. The final noise model was verified by extrapolating the model up to W-band, which revealed an excellent agreement with the measured data also in this frequency interval. NF_{min} was subsequently extracted by using ADS. At 94 GHz, NF_{min} was approximately 3.5 dB.

CHAPTER 5

Lateral Optimization

In this chapter, scaling of three main lateral design parameters, L_g, L_{SD} and gate width W is presented. L_g is the most fundamental lateral device parameter to scale for improving f_T and f_{max}. When L_g is reduced, access resistances should be reduced accordingly for proper scaling, for instance by reducing L_{SD}.

5.1 Gate-Length

For L_g above 2 µm, f_T increases as $1/L_g^2$ with reduced L_g [79]. When L_g is further reduced, f_T will only increase as $1/L_g$. Finally, when L_g becomes too short, f_T will roll-off from the $1/L_g$ slope. Such evolution is well-known for InGaAs/InAsAs HEMTs [26]. The f_T dependence on L_g for InAs/AlSb HEMTs has previously been mentioned in [9, 27, 56]. The difficulties to improve f_T with a $1/L_g$ slope were observed.

In Figure 5.1, the DC and RF dependence on L_g for InAs/AlSb HEMTs are shown, with L_g ranging from 225 nm to 335 nm. All devices had $W = 2\times50$ µm and a $L_{SD} = 2.3$ µm. Two different bias points are presented, one corresponding to the highest frequency performance and one to the lowest *NF*. In Figure 5.1(a), a shift in g_m towards more negative V_{GS} is observed for the shorter L_g, in particular at $V_{DS} = 0.5$ V. This behavior should mainly be attributed to an increased g_{ds} due to a higher field under the gate, but also a consequence of the reduced L_g over gate-to-channel distance. Furthermore, the observed constant peak g_m with reduced L_g suggests to reduce the gate-to-channel distance and L_{SD} for additional improvement in device performance. In Figure 5.1(b), it is observed that the slopes of f_T and f_{max} versus L_g are similar at $V_{DS} = 0.2$ V. However, at $V_{DS} = 0.5$ V, the slope of f_{max} was lower than the slope of f_T. This

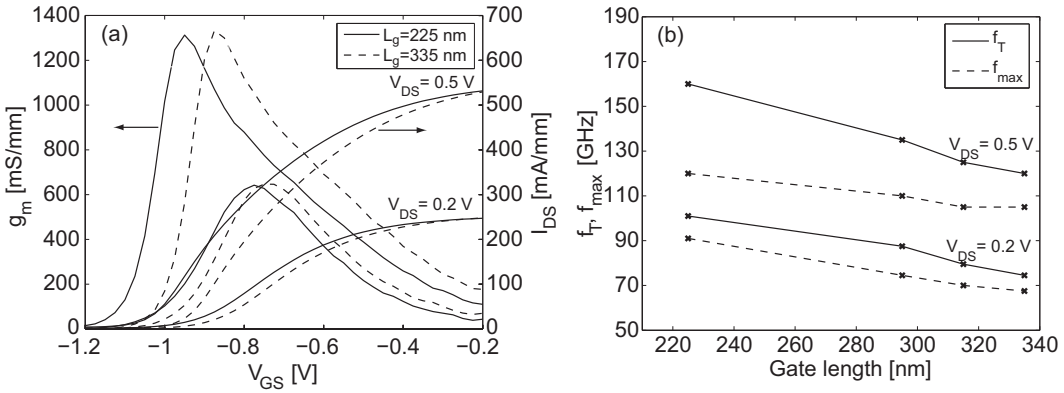

Figure 5.1 *Influence of L_g on (a) g_m and I_{DS} as a function of V_{GS} and (b) f_T and f_{max} for a 2×50 µm gate-width InAs/AlSb HEMT biased at V_{DS} = 0.2 V and V_{DS} = 0.5 V.*

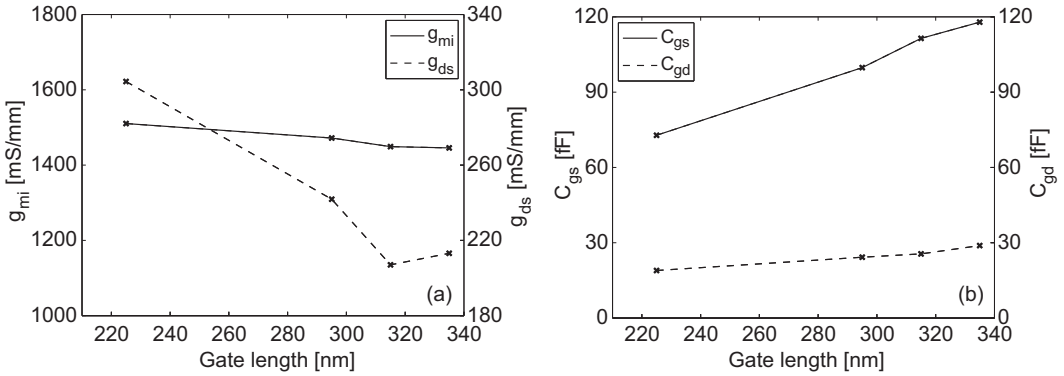

Figure 5.2 *Small-signal parameter (a) g_{mi} and g_{ds} (b) C_{gs} and C_{gd} dependence on L_g for a 2×50 µm gate-width InAs/AlSb HEMT biased at V_{DS} = 0.6 V.*

lower slope is consistent with the increased g_{ds} and almost constant intrinsic transconductance g_{mi} with reduced L_g shown in Figure 5.2(a).

In addition to a high g_{mi} and a low g_{ds}, the C_{gd} over C_{gs} ratio should be kept as low as possible to achieve a high f_{max} with reduced L_g. In Figure 5.2(b), C_{gs} and C_{gd} (including the extrinsic gate-to-drain capacitance C_{pgd}) are depicted as a function of L_g. A faster decrease in C_{gs} compared to C_{gd} is observed, i.e. the C_{gd}/C_{gs} ratio was increased with reduced L_g. One solution to maintain a low C_{gd}/C_{gs} ratio with reduced L_g is to utilize an asymmetric gate recess [80], which will reduce g_{ds} as well. Boos *et al.* [27] reported that the limiting factor for device improvement of their 200 nm gate-length InAs/AlSb HEMTs was a relatively large C_{gd} of 0.4-0.5 pF/mm. For the 225 nm gate-length InAs/AlSb HEMTs studied in this thesis, C_{gd} was almost 50% lower, 0.2-0.3 pF/mm, see Figure 5.2(b).

Within the investigated L_g interval, f_T exhibited a $1/L_g$ dependence, see Figure 5.1(b). When L_g was reduced from 335 nm to 225 nm, f_T increased with 40% to an f_T of 165 GHz. This is comparable to the best reported extrinsic f_T for InAs/AlSb HEMTs with similar L_g [60]. At an L_g of 100 nm there is a significant roll-off from the $1/L_g$ slope (Paper C). To minimize these effects, vertical scaling and reduction of access resistances are necessary. Furthermore, when L_g is reduced, the depletion region extending towards the drain contact ΔL will be a more significant part of the effective L_g (= L_g+ΔL). This will also contribute to the $1/L_g$ roll-off. One method to reduce the effective L_g is by utilizing a two-step gate recess etch combined with an InP etch-stop layer [81]. Another important factor to consider when reducing L_g is to minimize C_{fringe} (see Eq. (2.1)). C_{fringe} can be reduced by designing the T-gate for high aspect ratio between the gate-foot height and L_g. According to Wada *et al.* [82], this aspect ratio should be larger than two to minimize the effects of C_{fringe} for a conventional T-gate. However, using a double-decked-shaped (DDS) gate, the aspect ratio can be reduced to slightly above one [82].

5.2 Source-to-Drain Distance

When designing an analog HEMT for low *NF*, high f_T and high f_{max}, it is necessary to optimize R_s and R_d. For example, according to Eq. (2.2), $(R_s+R_d)\times g_{ds}$ should be much lower than one to achieve high f_T. Indeed, g_{ds} increased with reduced L_g (Figure 5.2(a)), and R_s+R_d must therefore be reduced accordingly. The most straightforward approach to reduce R_s and R_d is to reduce L_{SD}. Other approaches have been suggested to reduce R_s and R_d, such as optimizing the epitaxial structure of the cap layer [4].

130 nm gate-length InGaAs/InAlAs HEMTs with L_{SD} of 2.3 µm and 1.0 µm have been compared. The gate contact was aligned in the center of the ohmic

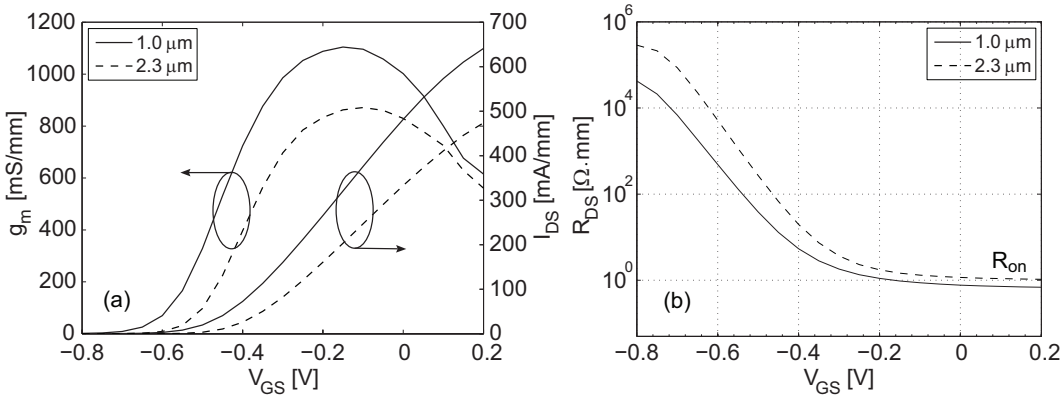

Figure 5.3 *Influence of source-to-drain distance L_{SD} on (a) $g_m(V_{GS})$, $I_{DS}(V_{GS})$ at V_{DS} = 1.0 V and (b) $R_{DS}(V_{GS})$ at V_{DS} = 50 mV for InGaAs/InAlAs HEMTs.*

contacts for the HEMT with L_{SD} = 1.0 µm. For the HEMT with L_{SD} = 2.3 µm, the gate contact was positioned with a gate-to-source distance of 0.5 µm. In Figure 5.3(a), $g_m(V_{GS})$ and $I_{DS}(V_{GS})$ are shown for L_{SD} = 1.0 µm and 2.3 µm. An improvement of 25% was achieved for g_m and I_{DS}. The on-resistance R_{on} was reduced from 1.1 Ω·mm to 0.7 Ω·mm, see Figure 5.3(b). As a result, f_T was improved by approximately 10%.

To further minimize access resistances required for ultra-short L_g of 50 nm, self-aligned ohmic contacts have been used [83, 84]. There is however a trade-off between gate-to-drain distance and breakdown voltage. Indeed, f_T increases by decreasing the gate-to-drain distance but the breakdown voltage will be reduced. For the presented InGaAs/InAlAs HEMTs with L_{SD} = 1.0 µm, the breakdown voltage was 2.5 V. This value was well above the supply voltage of 0.6-1.0 V.

5.3 Gate-Width

The influence from different gate widths on RF performance is interesting from several aspects. The choice of gate width W depends on the targeted frequency band. With increased frequency, a smaller W is required to facilitate impedance matching. A 4-8 GHz LNA utilize a W = 200 µm [62], whereas a 340 GHz LNA utilize a W = 20 µm [2]. A smaller W is also beneficial for R_g. Moreover, through the influence of W on SSM parameters, information about the intrinsic device behavior can be obtained.

In Figure 5.4(a), extrinsic f_T and f_{max} as a function of W are shown for 130 nm gate-length InGaAs/InAlAs HEMTs. No simultaneous optimum is observed for f_T and f_{max}. Since the gate pad capacitance C_{pg} is independent of W, the influence from C_{pg} will be more significant for small W. Extrinsic f_T is therefore continuously increasing with W. In contrast, f_{max} versus W reveals a maximum. When W is decreased, the gate resistance R_g is simultaneously

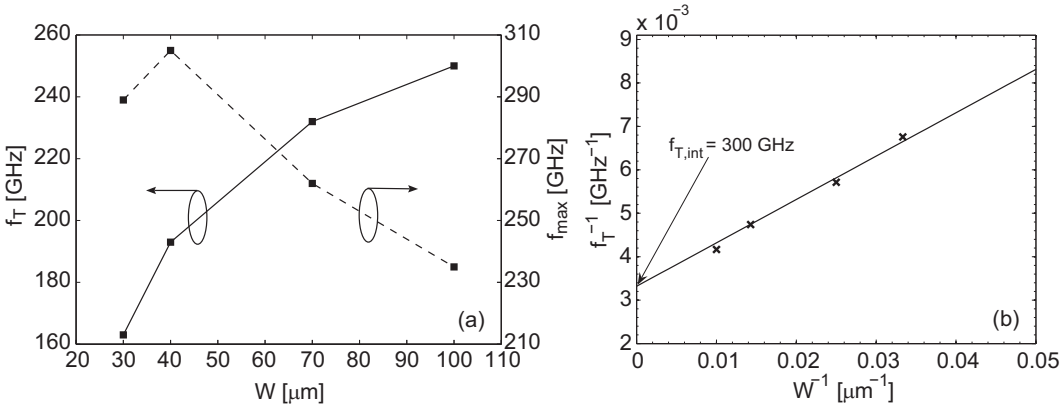

Figure 5.4 *Influence of the gate-width W on (a) extrinsic f_T and f_{max} and (b) the corresponding intrinsic f_T value extraction for InGaAs/InAlAs HEMTs.*

reduced, allowing f_{max} to increase. However, the influence of C_{pgd} on the total C_{gd} will also increase and eventually also the C_{gd}/C_{gs} ratio. As a result, a maximum in f_{max} was observed. This optimum in $f_{max}(W)$ has also been observed by Monte Carlo simulations [85]. One method to reduce C_{pgd} is reported in [86], where the layout of the gate and drain contacts are optimized.

In the literature, intrinsic f_T and f_{max} values are frequently presented. To extract an intrinsic f_T, the pad capacitances are often de-embedded from the measured *S*-parameters. This has to be done with great accuracy to avoid affecting C_{gs} and C_{gd}. Instead, by examining Eq. (2.1), it is clear that the intrinsic f_T can be obtained through $1/f_T$ versus $1/W$ plots by extrapolating f_T to a W equal to infinity. Using this method, the intrinsic f_T was estimated to be approximately 25% larger than the extrinsic value of a device with W = 2×50 µm, i.e. 300 GHz instead of 250 GHz, see Figure 5.4. The intrinsic f_{max} was estimated from the intrinsic SSM to be approximately 25% larger than the extrinsic values. For W = 40 µm, this resulted in an intrinsic f_{max} = 375 GHz.

In Table 5.1, the most essential SSM parameters are summarized. The SSM parameters were extracted for W = 30, 40, 70 and 100 µm by using the method described in Chapter 4. The majority of the parameters scaled well with W. The total gate-to-drain capacitance $C_{gd,tot}$ (= C_{gd}+C_{pgd}) did not scale with W. C_{pgd} was extracted by extrapolating a least-square fit of $C_{gd,tot}(W)$ towards W = 0 µm with the HEMT biased for pinched-off conditions. This resulted in a C_{pgd} = 3 fF. By comparing this value with C_{gd}, it was observed that C_{pgd} was as high as 50% of $C_{gd,tot}$ for small W. Reducing C_{pgd} is therefore essential for improved f_{max} in these HEMTs.

Table 5.1 *Small-signal model parameters for 130 nm gate-length InGaAs/InAlAs HEMTs as a function of gate width W*

SSM parameter		W = 30 µm	W = 40 µm	W = 70 µm	W = 100 µm
R_s	[Ω·mm]	0.22	0.23	0.22	0.21
C_{pgd}	[fF]	3	3	3	3
C_{gd}	[fF/mm]	93	80	74	79
C_{gs}	[fF/mm]	1100	1075	1029	1020
R_i	[Ω·mm]	0.40	0.50	0.76	1.0
g_{mi}	[mS/mm]	2043	2083	2114	2140
R_{ds}	[Ω·mm]	7.65	6.84	6.09	6.10

CHAPTER 6

Vertical Optimization

When L_g is reduced, the HEMT vertical structure must to be scaled. A rule-of-thumb is that the L_g over gate-to-channel distance aspect ratio should be larger than five to avoid short-channel effects (SCE) [87]. However, trade-offs between the vertical and lateral parameters in relation the DC, RF and noise performance of the HEMT makes the scaling complex. In this chapter, it is experimentally shown how the epitaxial structure is optimized for 130 nm gate-length InGaAs/InAlAs HEMTs, for either high frequency (Paper A) or low *NF* operation (Paper B).

6.1 Structure Definition

Three essential epitaxial parameters have been experimentally investigated: the In content in the channel ([In]: 53, 70 and 80%), the δ-doping concentration (δ: 3, 5 and 7×10^{12} cm^{-2}) and the Schottky layer thickness (d_{SL}: 9, 11 and 13 nm). The product of μ_e and n_s is known to increase with [In], which is highly desirable for RF performance. δ is a parameter that largely controls n_s and therefore I_{DS} and g_m. Variation of d_{SL} corresponds to altering the L_g over gate-to-channel distance aspect ratio. This will affect the charge control (modulation efficiency) which is closely connected to g_m. d_{SL} will also affect I_{DS} through surface charge effects, as well as I_G due to the change in gate-to-channel distance. The different investigated structures are summarized in Table 6.1. For this optimization, the in-house 130 nm gate-length InGaAs/InAlAs HEMT fabrication process with L_{SD} = 1.0 μm was used.

The reports on epitaxial optimization in the open literature are few and scattered, in particular with respect to noise performance. Nguyen *et al.* [83]

Table 6.1 *Investigated InGaAs/InAlAs HEMT epitaxial structures*

Series	δ [10^{12} cm^{-2}]	d_{SL} [nm]	[In] [%]
[In]	6.3	12	53 70 80
δ	3.0 5.0 7.0	12	80
d_{SL}	6.1	9 11 13	80

compared [In] = 53% with [In] = 80% for an L_g of 50 nm with respect to RF performance. Kim *et al.* [88] studied the effect of different L_g on different gate-to-channel distances and found different optimal gate-to-channel distances for different L_g with respect to f_T. For a longer L_g, a larger gate-to-channel distance was preferable. Takahashi *et al.* [89] recently reported on epitaxial optimization with respect to gate-to-channel distance. They suggested that it should be more important to improve g_m than reduce R_s to reduce *NF*. Through Monte Carlo simulations, Mateos *et al.* [90] suggested that lowest *NF* is achieved for lowest possible δ while maintaining sufficiently high I_{DS}. Generally, it is problematic to compare f_T, f_{max} and NF_{min} results in the literature due to different extrapolation techniques and reports both on intrinsic and extrinsic values. In the study reported in this thesis, important variables such as L_g, fabrication process, extraction and measuring methods have been kept constant. This provides an overall picture of the epitaxial scaling of 130 nm gate-length InGaAs/InAlAs HEMTs.

Different trade-offs exist when optimizing [In], δ and d_{SL}. Even though the transport properties should improve with [In] in an InGaAs material, it does not guarantee an improvement when incorporated in a HEMT structure. As [In] is increased, the compressive strain in the channel will increase due to the larger lattice constant compared to the surrounding materials lattice-matched to InP. Unless the channel thickness is less than the critical thickness, this will eventually result in material relaxation, strongly degrading the device performance. On the opposite, a too thin channel (<50-100 Å [91]) will decrease ΔE_c due to energy quantization. This will reduce the modulation efficiency through a reduced 2DEG density [15]. A composite channel (described in Chapter 3) is therefore used to obtain high [In].

With an increased δ-doping, larger I_{DS} and g_m are expected due to increased 2DEG density. To have a first indication of the influence from extreme δ, the energy-band diagram was studied for an InGaAs/InAlAs HEMT at thermal equilibrium by TCAD simulations. In Figure 6.1, simulated energy-

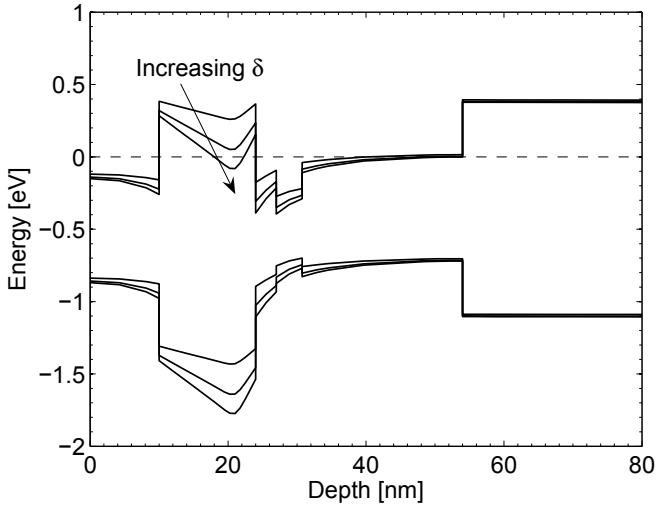

Figure 6.1 *TCAD simulated energy-band diagram with different δ-doping concentrations for an InGaAs/InAlAs HEMT at thermal equilibrium (for epitaxial layer details see Figure 3.1(a)).*

band diagrams with different δ-doping concentration are shown. It is observed that when δ was increased, the conduction band edge at the δ-doping plane approached the Fermi level. At a certain δ, the conduction band edge was even below the Fermi level. This indicated the presence of a parasitic channel at the δ-doping plane when δ exceeds a critical value. The absolute level where this phenomenon occurs needs to be validated through experimental data.

By reducing the gate-to-channel distance, the modulation efficiency and thereby g_m should increase. This can be done by reducing the Schottky layer thickness d_{SL}. However, the modulation efficiency is also closely connected to n_s [15]. For a thin d_{SL}, n_s will decrease due to an increased transfer of electrons to the cap layer. Furthermore, a HEMT with a too thin d_{SL} will suffer from an elevated I_G.

6.2 DC Optimization

In Figure 6.2, measured extrinsic $g_m(V_{GS})$ and $I_{DS}(V_{GS})$ are compared for [In], δ and d_{SL} at V_{DS} = 1.0 V. The d_{SL} parameter in this study was approximately equal to the gate-to-channel distance. AFM measurements revealed a total recess depth of approximately 13 nm. With a cap layer of 10 nm and a spacer thickness of 3 nm, the gate-to-channel distance equals d_{SL}. In Figure 6.2(a), an increased g_m and I_{DS} as a function of [In] is observed. This is mainly related to the increased conduction band offset leading to improved electron confinement.

In Figure 6.2(b), an increased g_m and I_{DS} versus δ is noticed. With a higher δ, more carriers will transfer into the channel. The higher 2DEG density resulted in an increased I_{DS} and g_m. At the same time, a more negative V_{GS} was required to pinch-off the devices, manifested as an increased V_{TH} as a function of δ. The observed trend in $I_{DS}(V_{GS})$ for different δ are in agreement with the results reported in [85, 92].

In Figure 6.2(c), it is observed that the shape and the position of the g_m-curves are directly dependent on the selection of d_{SL}. A maximum g_m was detected for the InGaAs/InAlAs HEMT with a d_{SL} = 11 nm. Using a small

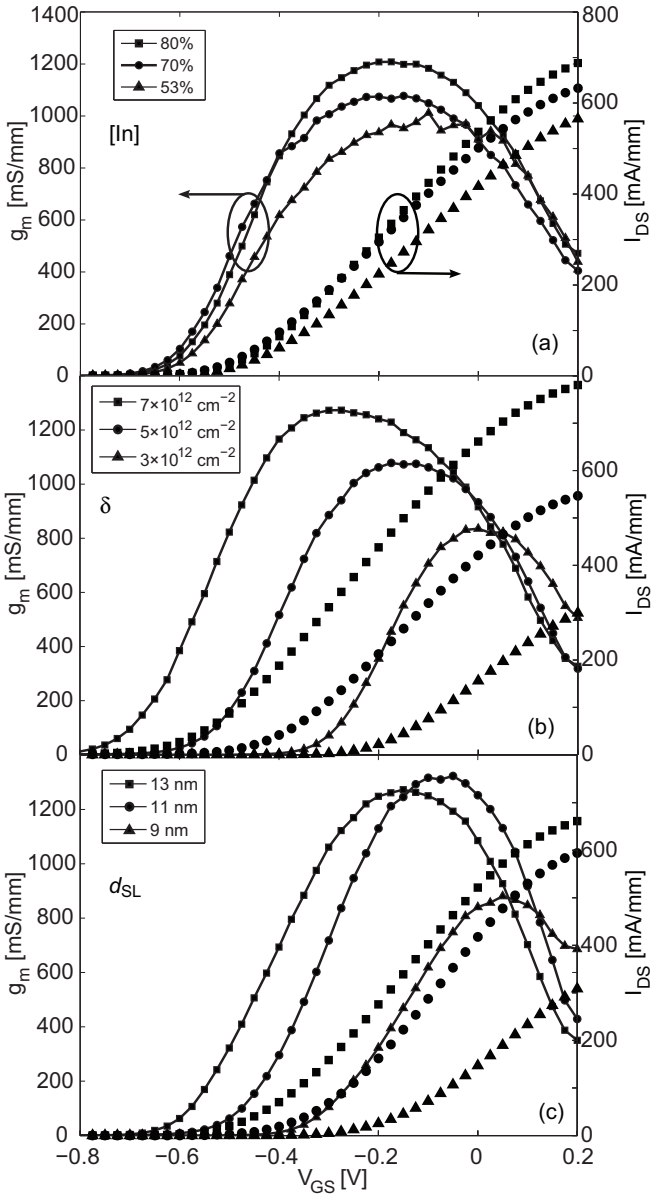

Figure 6.2 *Measured $g_m(V_{GS})$, $I_{DS}(V_{GS})$ versus (a) [In], (b) δ and (c) d_{SL} for 130 nm gate-length InGaAs/InAlAs HEMTs biased at V_{DS} = 1.0 V.*

gate-to-channel distance, an improvement in the modulation of the channel current is expected. However, when d_{SL} was reduced to 9 nm, the carriers in the channel become too few and g_m was strongly degraded. This was both due to a reduced 2DEG density as well as an increased R_s and R_d. Similar behavior has been observed in [88]. Since the d_{SL} parameter affects the amount of carriers in the channel, V_{TH} was changed in the same manner as for δ.

From this DC optimization, it appears that a trade-off does exist for the choice of d_{SL} but not for [In] and δ. Both [In] and δ should be maximized to achieve highest g_m.

6.3 RF and Noise Optimization

In Figure 6.3, f_T, f_{max} and NF_{min} are depicted for the different [In], δ and d_{SL}. f_T and f_{max} are presented for HEMTs biased both for minimum noise (V_{DS} = 0.6-0.7 V) and maximum RF performance (V_{DS} = 0.9-1.0 V). An interesting observation in Figure 6.3(a) is that the expected RF improvement with increasing [In] occurs mainly when the HEMT was biased for maximum RF performance, whereas only a minor improvement is observed when the HEMT was biased for minimum noise. The absence of improvement may appear anomalous. One explanation is that the composite channel approaches pinch-off, and it may therefore not be possible to take advantage of the high [In] superlattice. Instead, the electrons are mainly located in the lower part of the channel where [In] = 53%. A trade-off could be to utilize a homogenous pseudomorphic channel when designing the epitaxial structure for low-noise applications, for instance [In] = 65%.

In Figure 6.3(b), a large reduction in f_{max} is observed for $\delta = 7\times10^{12}$ cm^{-2}. As suggested by the TCAD simulations, this was most likely ascribed to a parasitic channel at the δ-doping plane. To avoid this phenomenon, it was estimated to use a δ below 6.3×10^{12} cm^{-2} (see Paper A). The HEMT with lowest δ suffered from a relatively poor RF performance, attributed to the low g_m, high R_s and high R_d. The best RF performance for the δ-series was therefore obtained at an optimum ($\delta = 5\times10^{12}$ cm^{-2}). For the d_{SL} parameter, an optimum at d_{SL} = 11 nm was achieved with respect to f_T and f_{max}, both when biased at minimum noise and at maximum RF performance, see Figure 6.3(c). This corresponds well with the observed DC performance.

NF_{min} was extracted through $NF_{50\Omega}$ measurements, as described in Chapter 4. A slight decrease in NF_{min} was observed with increasing [In], see Figure 6.3(d). This should mainly be ascribed to a reduced R_s and R_d. The parasitic channel present for $\delta = 7\times10^{12}$ cm^{-2} made it difficult to extract a trustworthy SSM and NF_{min} was therefore not possible to extract. However, the measured $NF_{50\Omega}$ indicated an NF_{min} significantly higher than for all the other investigated HEMTs. The lowest NF_{min} was obtained for $\delta = 5\times10^{12}$ cm^{-2}, see Figure 6.3(e).

With a δ equal to 3×10^{12} cm^{-2}, too few carriers appear in the channel to provide low resistance and high g_m, essential for low-noise HEMTs. In Figure 6.3(f), the influence of d_{SL} on noise performance is shown. For the thinnest d_{SL} = 9 nm, g_m was relatively low and I_G, R_s and R_d were all high. This resulted in a significant increase in NF_{min} compared to d_{SL} = 11 nm and 13 nm. An increased $NF_{50\Omega}$ as d_{SL} was reduced below a certain limit has previously been observed [93]. An optimal d_{SL} of 11 nm was observed in this study which is consistent with the observed maximum in g_m, f_T, and f_{max}.

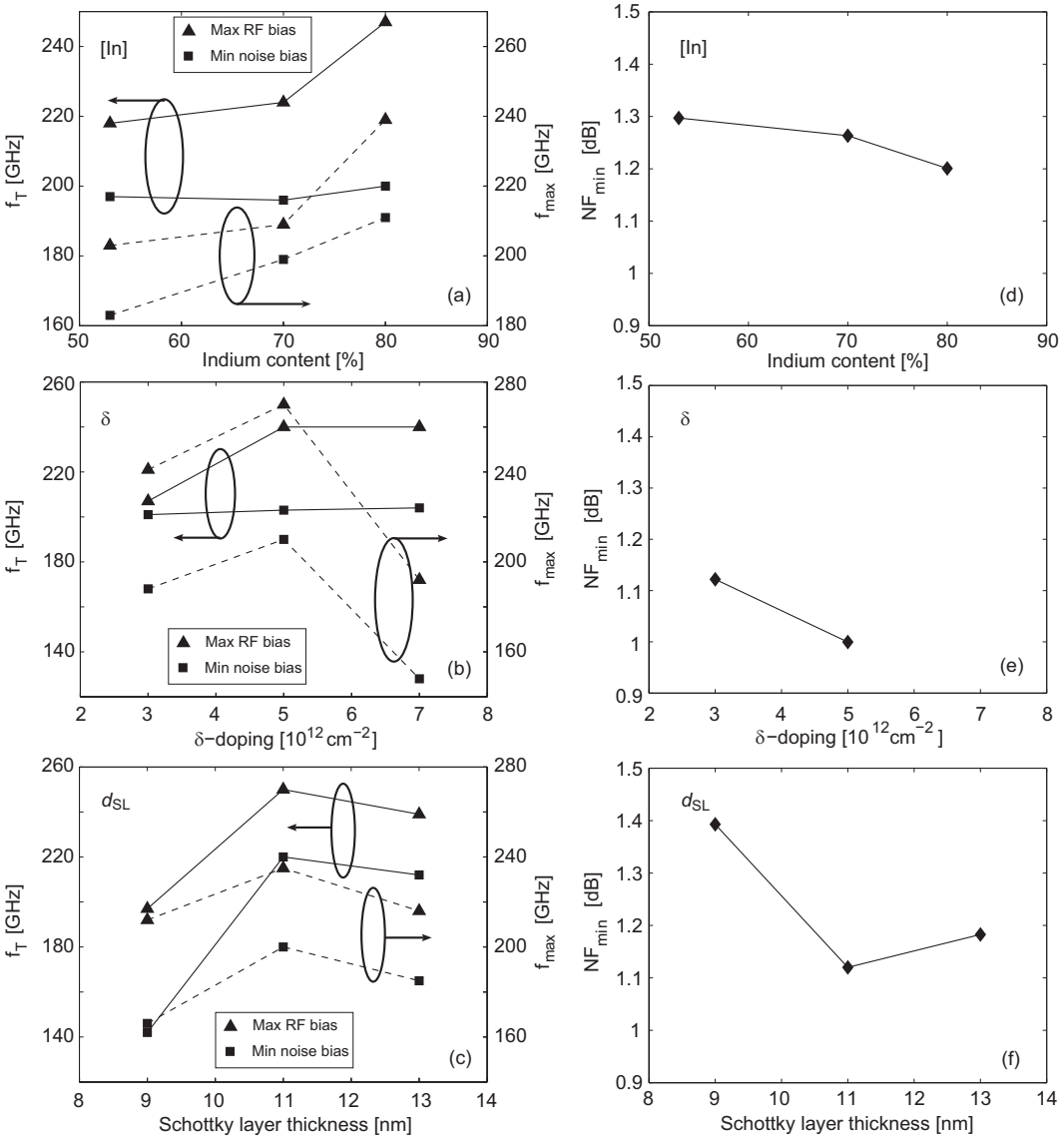

Figure 6.3 *Extrinsic f_T, f_{max} for maximum RF and lowest noise bias, and NF_{min} (@ 26 GHz) versus [In], δ and d_{SL}, for 130 nm gate-length InGaAs/InAlAs HEMTs.*

CHAPTER 7

Gate-Recess Technology

The impact of the gate-recess technology on the electrical properties for InAs/AlSb HEMTs and InGaAs/InAlAs HEMTs is described. The gate-recess fabrication step is crucial since it determines essential device parameters such as g_m, g_{ds}, V_{TH} and I_G. In other words, the gate recess is decisive for the RF and noise performance. In this chapter, significant differences will be shown in the electrical characteristics of the InAs/AlSb HEMT when employing different recess depths (Paper D and Paper E).

7.1 Recess Etch

For the InAs/AlSb HEMTs and InGaAs/InAlAs HEMTs in this work, a citric-acid based solution was used for the gate-recess etch. The recess depth and width were monitored by atomic force microscopy (AFM).

The citric-acid based solution etches InGaAs and should be selective to InAlAs [94]. In Figure 7.1, an AFM image of the gate recess of an InGaAs/InAlAs HEMT is shown after 30 s etching time. A recess depth of 13 nm was measured, suggesting that the InAlAs layer was etched approximately 3 nm (for details of the epitaxial structures see Chapter 3). This revealed a non-perfect InGaAs/InAlAs selectivity. For the InAs/AlSb HEMT, the recess-etch solution was selective to AlSb. However, since the AlSb Schottky layer can easily oxidize, control of the recess depth is especially crucial for this technology. Therefore, to reduce the etch rate, the gate-recess etch of the InAs/AlSb HEMTs was formed using a pH-adjusted solution (citric acid:NH_4OH:H_2O_2). By using a 20 s etching time and solutions with different pH values, different recess depths were obtained. This enabled to stop the recess etch in either the InAlAs protection layer or on the AlSb Schottky layer.

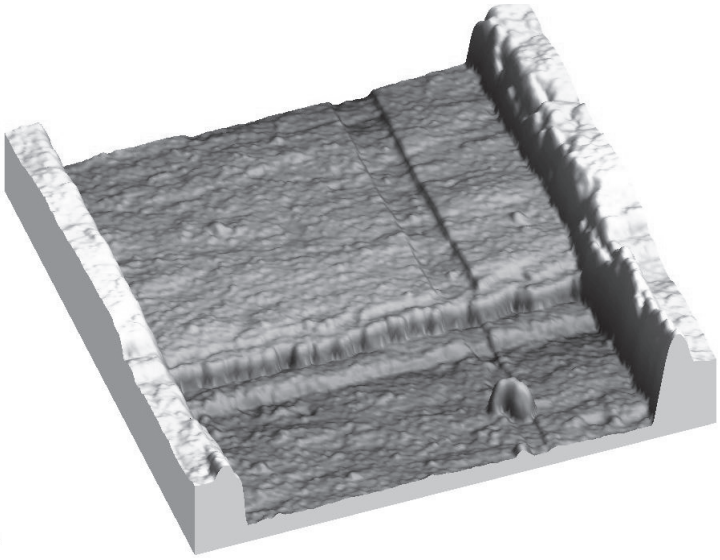

Figure 7.1 *AFM image of an InGaAs/InAlAs HEMT (before gate deposition) with a 2.3 µm source drain distance, including the mesa edge, the gate recess and part of the ohmic contacts.*

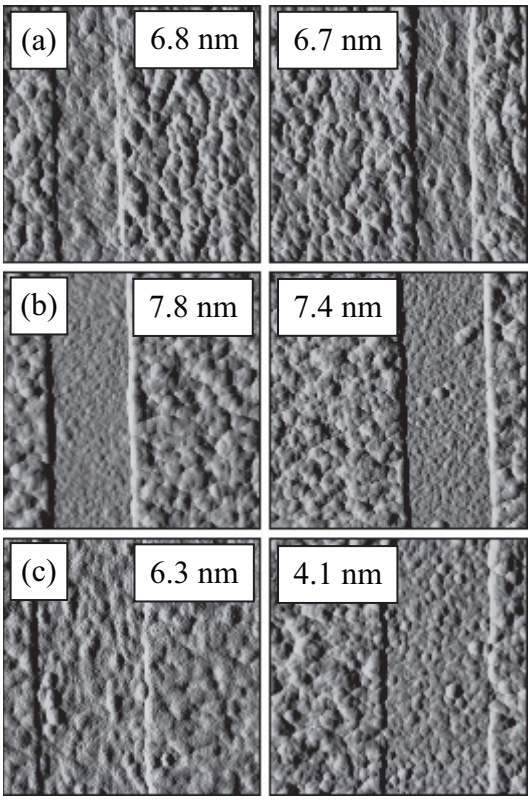

Figure 7.2 *1 µm × 1 µm AFM images of the gate recess evolution of InAs/AlSb HEMTs, two days (left column) and two weeks (right column) after the recess etch as a function of recess depth. Recess down to (a) 3D grown InAlAs, (b) 2D grown InAlAs and (c) AlSb Schottky layer.*

In Figure 7.2, AFM images of the gate recess of InAs/AlSb HEMTs are presented for three different recess depths. The images in the right and left column correspond to a recess depth measured two days and two weeks after the recess etch, respectively. The etchant with highest pH value is shown in Figure 7.2(a) and the lowest is shown in Figure 7.2(c). The AFM analysis revealed two characteristics for the gate recess of the InAs/AlSb HEMT. Depending on the recess depth, the gate recess evolved as a function of time, and a variation of the surface quality was observed. These behaviors were not present for the InGaAs/InAlAs HEMTs.

From Figure 7.2(a), it is clear that the gate recess did not evolve in time at a recess depth of 6.8 nm. The depth and the roughness suggested that the gate-recess etch was stopped in the three-dimensional (3D) grown upper part of the $In_{0.5}Al_{0.5}As$ protection layer (see Paper E for details). The gate recess was also stable in time at a recess depth of 7.8 nm, see Figure 7.2(b). Considering the stability and the depth of the recess, and its smoothness, it was concluded that this corresponded to the lower part of the $In_{0.5}Al_{0.5}As$ protection layer, where the $In_{0.5}Al_{0.5}As$ growth was still two-dimensional (2D). In Figure 7.2(c), it is observed that the gate-recess depth and roughness evolved with time. This evolution was due to the formation of an AlSb native oxide on the AlSb Schottky layer. Such fast formation of a native oxide on AlSb has been reported in detail by Shibata *et al.* [48]. For all the InAs/AlSb HEMTs, the gate-recess depth remained constant between two weeks and three months. It should be noted that the recess depth after two weeks, observed in Figure 7.2(c), was equal to the thickness of the InAs cap layer. A native oxide formed on the AlSb Schottky layer could therefore be incorrectly interpreted as a selective recess etch between InAs and InAlAs.

In the literature, the influence of the gate recess on HEMT performance has mainly been studied for InGaAs/InAlAs HEMTs [80, 81, 90, 95, 96]. For the InAs/AlSb HEMT, a selective citric acid-based etch between InAs and InAlAs has been mentioned, however with problems of InAlAs oxidation [9]. AFM images of the InAs/AlSb HEMT gate recess have previously only been shown by Boos *et al.* [53], but without any timing details. The results from the recess-etch study presented here show the importance of AFM measurements as a function of time for InAs/AlSb HEMTs.

7.2 Insulated-Gate versus Schottky-Gate HEMT

The InAs/AlSb HEMTs suffers from an elevated I_G. One common method to reduce I_G in InAs/AlSb HEMTs is to use an InAlAs protection layer, see Figure 3.1(b). However, this protection layer is not always sufficient (Paper E). An alternative idea to reduce I_G is to use the native oxide formed on the AlSb Schottky layer, as observed in Figure 7.2(c).

By fabricating two InAs/AlSb HEMTs with a slightly different recess-etch procedure, completely different device characteristic was achieved. For both HEMTs, the recess-etch depth was exactly as for the HEMT shown in Figure 7.2(c), i.e. the AlSb Schottky layer was reached. Before gate metal deposition an oxide removal step was performed on one HEMT, and omitted for the other HEMT. As a thin oxide forms relatively quickly on AlSb [48], the HEMT with the oxide removal step omitted prior to gate deposition should contain a native AlSb oxide between the gate contact and the Schottky layer.

In Figure 7.3, the DC characteristics of the two HEMTs are compared. The HEMT without an oxide was named Schottky-gate HEMT and the HEMT with an oxide between the gate contact and the Schottky layer was named insulated-gate HEMT. In Figure 7.3(a), it is observed that the insulated-gate HEMT exhibited slightly higher I_{DS} and higher G_{DS} compared to the Schottky-gate HEMT. In Figure 7.3(b), a very low I_G is observed for the insulated-gate HEMT under strong forward bias. This verifies the presence of an oxide under the gate. However, for the Schottky-gate HEMT, an I_G of almost two orders of magnitude higher is observed when forward biased at V_{GS} = 0.8 V. The higher G_{DS} of the insulated-gate HEMT observed in Figure 7.3(a), should be attributed to the oxide. The oxide will act as a blocking layer both for holes and electrons. Without the insulating layer, hole accumulation will be eliminated through a direct leakage to the gate due to the type-II energy band alignment. Elimination of hole accumulation has proven to suppress G_{DS} [57, 97]. Therefore, reduction of the hole accumulation can explain the lower G_{DS} for the Schottky-gate HEMT compared to the insulated-gate HEMT.

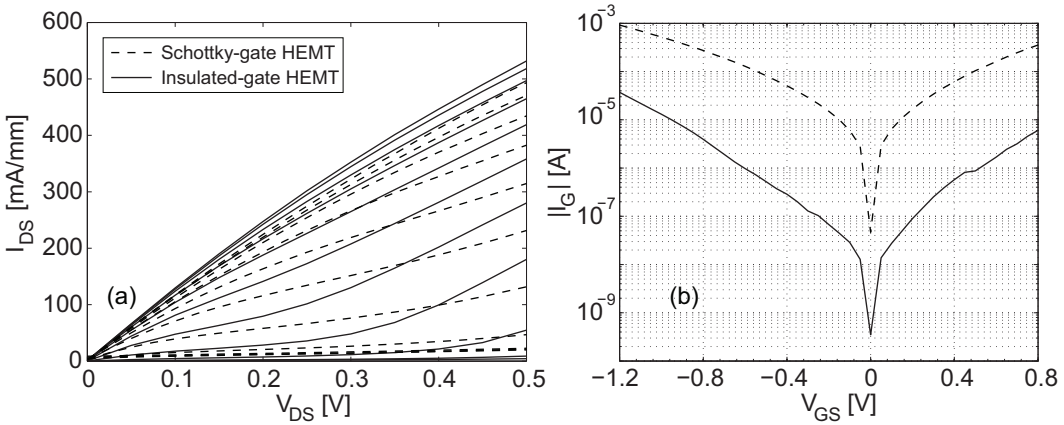

Figure 7.3 *DC performance of Schottky-gate InAs/AlSb HEMT versus insulated-gate InAs/AlSb HEMT. (a) I-V output characteristics at V_{GS}: -1.2 V to -0.2 V in steps of 0.1 V and (b) diode characteristics at V_{DS} = 0 V.*

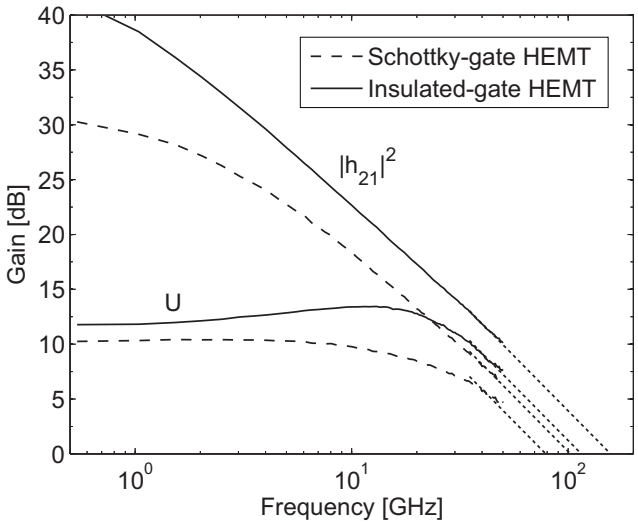

Figure 7.4 *RF performance of Schottky-gate InAs/AlSb HEMT versus insulated-gate InAs/AlSb HEMT.*

In Figure 7.4, the RF figures-of-merit of the Schottky-gate HEMT and the insulated-gate HEMT are compared. The Schottky-gate InAs/AlSb HEMT exhibited extrinsic f_T and f_{max} of 100 GHz and 80 GHz, respectively. For the insulated-gate InAs/AlSb HEMT, the extrinsic f_T and f_{max} increased to 160 GHz and 120 GHz, respectively. This is an improvement by 60% in f_T and 50% in f_{max}. This shows the possibility to reduce I_G in InAs/AlSb HEMTs by taking advantage of the native oxidation of the AlSb Schottky layer. A more conventional method to reduce I_G is to deposit a dielectric between the gate and the semiconductor. This method has been used to reduce I_G in InSb/InAlSb HEMTs [98] and InGaAs/InAlAs HEMTs [99] by employing a high-k dielectric deposited by atomic layer deposition (ALD) or MBE. This approach has so far not been considered for InAs/AlSb HEMTs.

CHAPTER 8

MMIC Technology

MMIC technology makes it possible to manufacture compact analog circuits operating in the microwave, mm-wave and even sub-mm-wave regions [41, 100, 101]. Recent results on MMICs based on the InGaAs/InAlAs HEMT technology have shown +300 GHz MMICs. Parasitics associated with bond wires connected to the active component become severe at these frequencies, and hybrid microwave integrated circuits are therefore normally avoided. At mm/sub-mm-wave frequencies, wafer thinning and via-hole etching are required for both microstrip and coplanar waveguide (CPW) technology in MMIC design [102, 103]. It is therefore not obvious which technology to choose when designing MMICs. In this thesis microstrip transmission lines have been selected.

In this chapter, the integration of 50 nm and 70 nm InGaAs/InAlAs HEMTs into MMICs is presented. To demonstrate the integration of active and passive components, two different MMICs have been designed and fabricated using InGaAs/InAlAs HEMTs with [In] = 65%.

8.1 Broadband Feedback Amplifier

A broadband feedback amplifier was designed to demonstrate the integration of metal-insulator-metal (MIM) capacitors and thin film resistors (TFRs) with a 50 nm gate-length InGaAs/InAlAs HEMT in a microstrip-based MMIC technology (Paper G).

The feedback approach provides a flat gain response through an improved control in the variation of the *S*-parameters. However, the feedback topology will also introduce higher *NF* and lower gain [104].

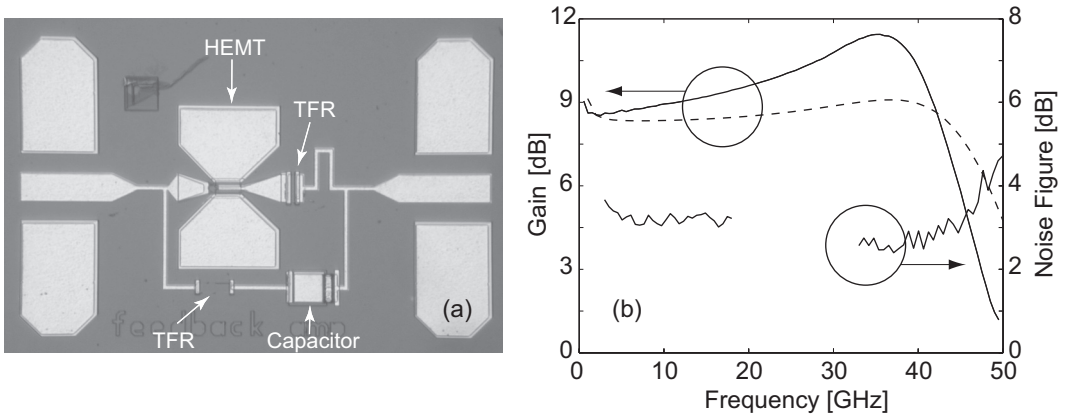

Figure 8.1 *A 0-42 GHz broadband MMIC amplifier based on a 50 nm gate-length InGaAs/InAlAs HEMT technology. (a) photograph of the amplifier with a chip size of 0.9 mm × 0.6 mm and (b) measured (solid) and modeled (dashed) gain, and measured noise figure (solid) for the amplifier at* V_{DS} *= 1.0 V and* V_{GS} *= -0.2 V.*

The single-stage amplifier in this study was designed using a 2×50 µm gate width HEMT loaded with a 10 Ω TFR at the output for stability reasons. In the feedback loop, a 1.2 pF MIM capacitor and a 250 Ω TFR and a 10 µm thin inductive line were utilized. The 50 nm gate-length InGaAs/InAlAs HEMT-based MMIC was fabricated using the in-house MMIC fabrication process using an L_{SD} = 2 µm. The 50 nm L_g was only verified by SEM at the edge of the gate. This introduces an increased error in the actual physical L_g, in comparison to an L_g measured by FIB-SEM.

In Figure 8.1(a), a photograph of the fabricated MMIC is shown highlighting the individual active and passive components. As TFR material, reactively sputtered TaN was used [51]. The resulting sheet resistance was 80-85 Ω/sq. TaN was selected since it is relatively chemically stable, and easy to fabricate with high reproducibility [105, 106]. Reactively sputtered Si_3N_4 with a nominal thickness of 2000 Å was used as dielectric for the MIM capacitors. Typically, the capacitors exhibited a capacitance of 300 pF/mm^2 and a breakdown voltage above 100 V. Such breakdown voltage compares well with Si_3N_4 capacitors fabricated using plasma enhanced chemical vapor deposition (PECVD) [107].

The *S*-parameters of the amplifier were measured on-wafer using coplanar probes with a HP8510C vector network analyzer. The *NF* of the amplifier was measured using an Agilent N8975A noise figure analyzer. As shown in Figure 8.1(b), the MMIC exhibited more than 8 dB gain and an average *NF* less than 3 dB over 0-42 GHz. The DC power consumption of the amplifier was 19 mW. A discrepancy is observed between measured and modeled gain, especially for the higher frequencies. Nonetheless, the results demonstrate the feasibility for MMIC integration for active and passive components in the in-house 50 nm InGaAs/InAlAs HEMT technology.

8.2 W-Band Amplifier

One interesting operating frequency for InGaAs/InAlAs HEMT MMICs is 94 GHz. At this frequency the atmospheric attenuation exhibits a minimum. This facilitates mm-wave applications such as long range sensing and imaging systems.

A single-stage amplifier based on a 70 nm gate-length InGaAs/InAlAs HEMT technology was designed and fabricated (Paper H). The design was based on a SSM extracted from *S*-parameter measurements up to 50 GHz. The SSM was extrapolated up to 110 GHz. The amplifier was measured using an HP8510C vector network analyzer with a W-band (75-110 GHz) test set. The setup was calibrated using an on-wafer transmission-reflection-line (TRL) structure.

A photograph of the fabricated W-band amplifier is depicted in Figure 8.2(a). The final chip area was 1.7 mm × 0.5 mm. The amplifier exhibited more than 8 dB gain between 75 GHz and 94 GHz, see Figure 8.2(b). This amplifier demonstrated the feasibility of a via-hole based process at W-band. Several design and fabrication parameters can be optimized to further improve the amplifier performance. This means to reduce the device access resistances, optimize the gate recess and improve the via-hole process.

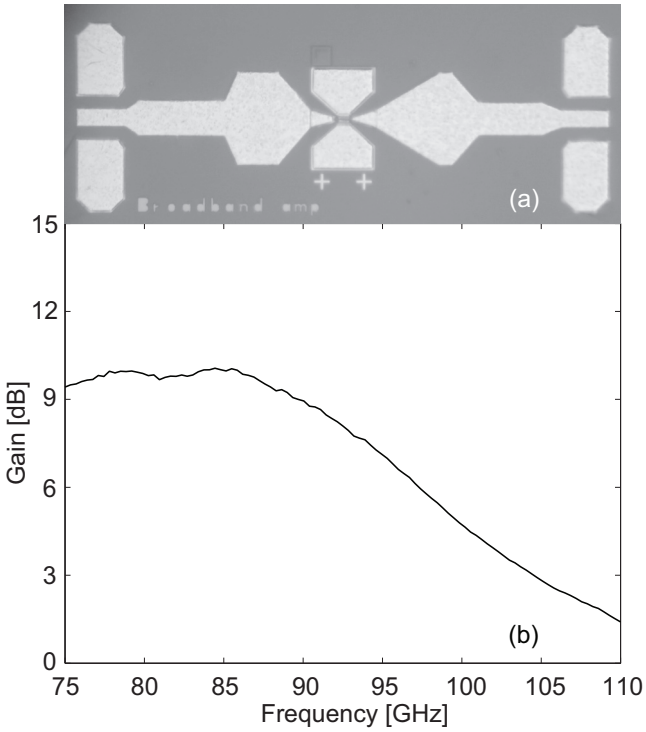

Figure 8.2 *(a) A photograph and (b) measured gain of a 94 GHz amplifier based on a 70 nm gate-length InGaAs/InAlAs HEMT technology. Chip size 1.7 mm × 0.5 mm.*

CHAPTER 9

Conclusions and Future Directions

This thesis has presented new results for narrow bandgap HEMTs targeting low-noise and low DC power applications. Device fabrication, modeling and optimization of two different narrow bandgap HEMT technologies have been conducted: the relatively established InGaAs/InAlAs HEMT, and the more immature InAs/AlSb HEMT technology. The significance of both lateral and vertical optimization, coupled to electrical device characterization has been discussed. Methods to solve the fabrication and modeling when dealing with the InAs/AlSb HEMT technology have been shown. Finally, the feasibility of integrating active and passive components into a microstrip InGaAs/InAlAs HEMT MMIC process was demonstrated.

A comprehensive experimental study on the optimization of the epitaxial structure of 130 nm gate-length InGaAs/InAlAs HEMTs has been performed, both with respect to f_T and f_{max}, as well as for NF_{min}. Three crucial parameters for the HEMT performance were optimized: the In content in the channel [In] ranging from 53% up to 80%, the δ-doping concentration in the range 3-7×10^{12} cm^{-2}, and the gate-to-channel distance through the Schottky layer thickness with values between 9 nm and 13 nm. It was verified that increasing [In] provides improved RF performance. When increasing In from 53% to 80%, f_T and f_{max} improved 14% and 21%, respectively. The δ-doping had a significant effect on DC and RF performance but in different ways. Both I_{DS} and g_m increased with δ, whereas f_{max} was strongly degraded at a δ = 7×10^{12} cm^{-2}. It was also shown that the gate-to-channel distance is a most sensitive parameter to DC, RF and noise device characteristics. A too short distance resulted in increased I_G and reduced RF performance. The best RF performance was found for an optimum structure with [In] of 80%, δ-doping concentration of 5-6×10^{12} cm^{-2} and Schottky layer thickness of 11 nm resulting in extrinsic f_T and f_{max} of 250 GHz and 300 GHz, respectively. Increasing [In] only provided a slight improvement in NF_{min}. In contrast, the RF performance

was much more improved with increased [In] (HEMT biased for high gain). It was also concluded that a δ-doping in the lower range of 5×10^{12} cm^{-2} was beneficial with respect to noise, with an NF_{min} of less than 1 dB at 26 GHz.

The DC and RF performance dependence on L_g of InAs/AlSb HEMTs were investigated in the range 225-335 nm, showing an f_T improvement with a $1/L_g$ dependence. Small-signal and noise modeling as well as characterization of InAs/AlSb HEMTs for ultra-low DC power consumption have been conducted. The conventional SSM had to be extended to model the elevated I_G. At a low V_{DS} of 0.2 V and a corresponding DC power consumption of 10 mW/mm, an NF_{min} less than 1 dB between 1-18 GHz was achieved. This demonstrates the potential of the InAs/AlSb HEMT technology for ultra-low DC power consumption in low-noise applications.

The gate-recess technology of InAs/AlSb HEMTs has been investigated by combining electrical measurements with AFM analysis. This showed the importance of measuring the recess depth as a function of time related to the rapid oxidation of AlSb. Depending on recess depth, completely different electrical characteristics were obtained for the InAs/AlSb HEMT. In particular, by etching down to the AlSb Schottky layer, formation of a native oxide in the gate recess had the effect that I_G was reduced by two orders of magnitude and the RF performance was considerably improved.

Two different single-stage MMIC amplifiers have been demonstrated based on 50 nm and 70 nm gate-length pseudomorphic InGaAs/InAlAs HEMTs, Si_3Ni_4 MIM-capacitors and TaN TFRs. A broadband feedback amplifier operating at 0-42 GHz with an average *NF* of 3 dB and a W-band amplifier with a gain above 8 dB at 75-94 GHz were modeled and fabricated.

Only a few years ago, a prediction of amplifiers at 1 THz was very distant. However, the recent breakthrough in state-of-the-art device RF performance, with an f_{max} above 1 THz, using 35 nm gate-length InGaAs/InAlAs HEMTs [2], points to MMIC amplifiers at 600-700 GHz employing that technology. One intriguing vision, through further device improvement, is MMIC amplifiers at 1 THz. This will introduce new challenges regarding fabrication, measurements and modeling.

InGaAs/InAlAs HEMT is an exclusive technology with niche applications requiring extremely low-noise receivers with high gain. The most well-known civil application is cryogenically cooled amplifiers in radio astronomy. Designing a HEMT for low noise at room temperature does not imply that a similar design will provide lowest noise at cryogenic temperatures. It would therefore be interesting to compare a HEMT optimized for NF_{min} at cryogenic temperature and with a HEMT optimization for room temperature operation. In particular, the origin and impact of the kink-effect, mainly observed at cryogenic temperatures, should attain more consideration.

The Sb-based HEMTs are particularly interesting due to the superior peak velocities at low DC power consumption. Interesting heterostructure combinations are InAs/AlSb, InSb/InAlSb and InGaSb/InAlSb. However,

HEMTs based on these materials have not been able to reach the RF and noise performance of InGaAs/InAlAs HEMTs, even though an intrinsic f_T above 300 GHz has been reported [98, 108] with an L_g of 85 nm. The main reason is the relatively high I_G and g_{ds} present in the Sb-based HEMTs. These issues have to be solved without compromising the RF performance. Another interesting research area is Sb-based HEMTs operating at cryogenic temperatures, where I_G can be kept sufficiently low without an insulated gate. This would potentially provide both lower noise and lower DC power consumption in cryogenic low-noise amplifiers.

Acknowledgement

For the completion of this work I am indebted to many people. First and foremost, I would like to acknowledge my supervisor Assoc. Prof. Jan Grahn for his guidance, commitment and encouragement throughout this work. My sincere thanks to my examiner Prof. Herbert Zirath for giving me the opportunity to do this work.

I am obliged to Dr. Anders Mellberg and Dr. Niklas Rorsman for providing such a good introduction to my Ph.D. studies, and whose knowledge and insight in various topics have been invaluable. Special mention should also be given to Prof. Einar Sveinbjörnsson for leading me into the world of semiconductors and for all fruitful discussions throughout these years.

I am grateful to my colleagues in the InP HEMT group for creating an inspiring working atmosphere. In particular Assoc. Prof. Shumin Wang for fruitful discussions and for providing epitaxial material, Dr. Eric Lefebvre and Malin Borg for all the effort they put into this work and for great collaboration.

Dr. Per-Åke Nilsson and Bengt Nilsson are acknowledged for their assistance on issues regarding electron-beam lithography. Without their help, the numerous hours spent in the clean room facility would have been even more. Many thanks to Dr. Christian Fager, Dr. Kristoffer Andersson and Assoc. Prof. Iltcho Angelov for fruitful discussions regarding modeling related issues. Martin Fagerlind is acknowledged for the help with TCAD simulations.

I would like to thank Assoc. Prof. Sylvain Bollaert, Prof. Alain Cappy, Prof. Gilles Dambrine, Dr. Ludovic Desplanque and Prof. Xavier Wallart at IEMN, University of Lille, France, for a great collaboration and for providing epitaxial material.

My appreciation to my friends Fredrik, Johan, Mattias and Martin cannot be overstated. Thank you for all your help and support whenever needed, both work and non-work related. This acknowledgement would not be complete without thanking my family for their endless support and for believing in me.

Finally, I want to express my gratitude to Maria for always being there.

This work was financially supported by the Swedish Research Council (VR), the Swedish Foundation for Strategic Research (SSF) through the Strategic Research Center for High-Speed Electronics and Photonics (HSEP) at Chalmers University of Technology, the Swedish Defense Research Agency (FOI) through the Swedish Defense Nanotechnology program, and the European Space Agency.

Göteborg, January 2008

Mikael Malmkvist

REFERENCES

[1] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A new field-effect transistor with selectively doped GaAs/n-$Al_xGa_{1-x}As$ heterojunctions," *Jpn. J. of Appl. Phys.*, vol. 19, no. 5, pp. 225-227, May 1980.

[2] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT device with Fmax greater than 1 THz," in *IEEE Int. Electron Devices Meet. Tech. Dig.*, 2007, pp. 609-611.

[3] Y. Yamashita, A. Endoh, K. Shinohara, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs with an ultrahigh f_T of 562 GHz," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 573-575, Oct. 2002.

[4] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547-GHz f_t $In_{0.7}Ga_{0.3}As$-$In_{0.52}Al_{0.48}As$ HEMTs with reduced source and drain resistance," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 241-243, May 2004.

[5] P. C. Chao, A. J. Tessmer, K-H. G. Duh, P. Ho, M-Y. Kao, P. M. Smith, J. M. Ballingall, S-M. J. Liu, and A. A. Jabra, "W-band low-noise InAlAs/InGaAs lattice-matched HEMTs," *IEEE Electron Device Lett.*, vol. 11, no. 1, pp. 59-62, Jan. 1990.

[6] K. L. Tan, D. C. Streit, P. D. Chow, R. M. Dia, A. C. Han, P. H. Liu, D. Garske, and R. Lai, "140 GHz 0.1 μm gate-length pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.60}Ga_{0.40}As$/InP HEMT," in *IEEE Int. Electron Devices Meet. Tech. Dig.*, 1991, pp. 239-242.

[7] K. Elgaid, H. McLelland, M. Holland, D. A. J. Moran, C. R. Stanley, and I. G. Thayne, "50-nm T-gate metamorphic GaAs HEMTs with f_T of 440 GHz and noise figure of 0.7 dB at 26 GHz," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 784-6, Nov. 2005.

[8] B. O. Lim, M. K. Lee, T. J. Baek, M. Han, S. C. Kim, and J. K. Rhee, "50-nm T-gate InAlAs/InGaAs metamorphic HEMTs with low noise and high f_T characteristics," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 546-548, July 2007.

[9] C. Kadow, M. Dahlstrom, J. U. Bae, H. K. Lin, A. C. Gossard, M. J. W. Rodwell, B. Brar, G. J. Sullivan, G. Nagy, and J. I. Bergman, "n^+-InAs-InAlAs recess gate technology for InAs-channel millimeter-wave HFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 151-158, Feb. 2005.

[10] A. Leuther, R. Weber, M. Dammann, M. Schlechtweg, M. Mikulla, M. Walther, and G. Weimann, "Metamorphic 50 nm InAs-channel HEMT," in *Proc. IEEE 17th Int. InP and Relat. Mater. Conf.*, 2005, pp. 129-132.

[11] O. Wada and H. Hasegawa, *InP-based materials and devices - physics and technology*, New York, USA: John Wiley and Sons, Inc., 1999.

[12] H. Morcoc, H. Unlu, and G. Ji, *Principles and technology of MODFETs* vol. 1, New York, USA: John Wiley and Sons, Inc., 1991.

[13] H. Morcoc, H. Unlu, and G. Ji, *Principles and technology of MODFETs* vol. 2, New York, USA: John Wiley and Sons, Inc., 1991.

[14] F. Schwierz and J. J. Liou, *Modern microwave transistors: Theory, design and performance*. New York, USA: John Wiley and Sons, Inc., 2003.

[15] M. C. Foisy, P. J. Tasker, B. Hughes, and L. F. Eastman, "The role of inefficient charge modulations in limiting the current-gain cutoff frequency of the MODFET," *IEEE Trans. Electron Devices*, vol. 35, no. 7, pp. 871-878, July 1988.

[16] H. L. Hartnagel, R. Katilius, and A. Matulionis, *Microwave noise in semiconductor devices*, New York, USA: John Wiley and Sons, Inc., 2001.

[17] L. D. Nguyen, L. E. Larson, and U. K. Mishra, "Ultra-high speed modulation-doped field-effect transistors: a tutorial review," *Proc. IEEE*, vol. 80, no. 4, pp. 494-518, Apr. 1992.

[18] A. van der Ziel, *Noise in solid state devices and circuits*, New York, USA: John Wiley and Sons, Inc., 1986.

[19] J. Singh, *Electronic and optoelectronic properties of semiconductor structures*, London, UK: Williams Clowes Limited, 2003.

[20] S. M. Sze, *High-speed semiconductor devices*, New York, USA: John Wiley and Sons, Inc., 1990.

[21] W. Porod and D. K. Ferry, "Modification of the virtual-crystal approximation for ternary III-V compounds," *Phys. Rev. B*, vol. 27, no. 4, pp. 2587-2589, Feb. 1983.

[22] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III-V compound semiconductors and their alloys," *J. Appl. Phys.*, vol. 89, no. 11, pp. 5815-5875, June 2001.

[23] L. D. Nguyen and P. J. Tasker, "Scaling issues for ultra-high-speed HEMTs," in *Proc. SPIE Int. Soc. Opt. Eng.*, 1990, pp. 251-257.

[24] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum f_T of millimeter-wave MODFETs," *IEEE Electron Device Lett.*, vol. 10, no. 7, pp. 291-293, July 1989.

[25] M. B. Das, "A high aspect ratio design approach to millimeter-wave HEMT structures," *IEEE Trans. Electron Devices*, vol. 32, no. 1, pp. 11-17, Jan. 1985.

[26] K. Shinohara, P. S. Chen, J. Bergman, H. Kazemi, B. Brar, I. Watanabe, T. Matsui, Y. Yamashita, A. Endoh, K. Hikosaka, T. Mimura, and S. Hiyamizu, "Ultra-high-speed low-noise InP-HEMT technology," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2006, pp. 337-340.

[27] J. B. Boos, W. Kruppa, B. R. Bennett, D. Park, S. W. Kirchoefer, R. Bass, and H. B. Dietrich, "AlSb/InAs HEMT's for low-voltage, high-speed applications," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1869-1875, Sep. 1998.

[28] C. R. Bolognesi and D. H. Chow, "InAs/AlSb dual-gate HFETs," *IEEE Electron Device Lett.*, vol. 17, no. 11, pp. 534-536, Nov. 1996.

[29] B. Y. Ma, J. Bergman, P. Chen, J. B. Hacker, G. Sullivan, G. Nagy, and B. Brar, "InAs/AlSb HEMT and its application to ultra-low-power wideband high-gain low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4448-4455, Dec. 2006.

[30] R. Tsai, M. Lange, L. J. Lee, P. Nam, C. Namba, P. H. Liu, R. Sandhu, R. Grundbacher, W. Deal, and A. Gutierrez, "260 GHz F_T, 280 GHz f_{MAX} AlSb/InAs HEMT technology," in *Proc. IEEE 63rd Device Res. Conf.*, 2005, pp. 257-258.

[31] R. Tsai, J. B. Boos, B. R. Bennett, M. Lange, R. Grundbacher, C. Namba, P. H. Liu, J. Lee, M. Barsky, and A. Gutierrez, "275 GHz f_{MAX}, 220 GHz f_T AlSb/InAs HEMT technology," in *Proc. IEEE 62nd Device Res. Conf.*, 2004, pp. 12-13.

[32] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 32, pp. 97-109, July 1928.

[33] H. Nyquist, "Thermal agitation of electric charge in conductors," *Phys. Rev.*, vol. 32, pp. 110-114, July 1928.

[34] H. Fukui, "Design of microwave GaAs MESFET's for broad-band low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 7, pp. 643-650, July 1979.

[35] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 9, pp. 1340-1350, Sep. 1989.

[36] R. A. Pucel, W. Struble, R. Hallgren, and U. L. Rohde, "A general noise de-embedding procedure for packaged two-port linear active devices," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 11, pp. 2013-2024, Nov. 1992.

[37] M. W. Pospieszalski, "Extremely low-noise amplification with cryogenic FETs and HFETs: 1970-2004," *IEEE Microw. Mag.*, vol. 6, no. 3, pp. 62-75, Sep. 2005.

[38] W. Kruppa, J. B. Boos, D. Park, B. R. Bennett, and R. Bass, "Microwave noise characteristics of AlSb/InAs HEMTs," *Electron. Lett.*, vol. 33, no. 12, pp. 1092-1093, June 1997.

[39] J. Bergman, G. Nagy, G. Sullivan, B. Brar, C. Kadow, H. K. Lin, A. Gossard, and M. Rodwell, "RF noise performance of low power InAs/AlSb HFETs," in *Proc. IEEE 61st Device Res. Conf.*, 2003, pp. 147-148.

[40] W. R. Deal, R. Tsai, M. D. Lange, J. B. Boos, B. R. Bennett, and A. Gutierrez, "A W-band InAs/AlSb low-noise/low-power amplifier," *IEEE Microw. Wirel. Compon. Lett.,* vol. 15, no. 4, pp. 208-210, Apr. 2005.

[41] X. B. Mei, W. Yoshida, W. R. Deal, P. H. Liu, J. Lee, J. Uyeda, L. Dang, J. Wang, W. Liu, D. Li, M. Barsky, Y. M. Kim, M. Lange, T. P. Chin, V. Radisic, T. Gaier, A. Fung, L. Samoska, and R. Lai, "35-nm InP HEMT SMMIC amplifier with 4.4-dB gain at 308 GHz," *IEEE Electron Device Lett.*, vol. 28, no. 6, pp. 470-472, June 2007.

[42] C. Risacher, "Low noise SIS mixers and cryogenic amplifiers for sub-millimeter astronomy." Ph.D. dissertation: Chalmers University of Technology, 2005.

[43] D. Streit, R. Lai, A. Oki, and A. Gutierrez-Aitken, "InP HEMT and HBT applications beyond 200 GHz," in *Proc. IEEE 14th Int. InP and Relat. Mater. Conf.*, 2002, pp. 11-14.

[44] H. Essen, A. Wahlen, R. Sommer, W. Johannes, R. Brauns, M. Schlechtweg, and A. Tessmann, "High-bandwidth 220 GHz experimental radar," *Electron. Lett.*, vol. 43, no. 20, pp. 1114-1116, Sep. 2007.

[45] A. Tessmann, "220-GHz metamorphic HEMT amplifier MMICs for high-resolution imaging applications," *IEEE J. Solid-State Circuit,* vol. 40, no. 10, pp. 2070-2076, Oct. 2005.

[46] R. Raja, M. Nishimoto, B. Osgood, M. Barsky, M. Sholley, R. Quon, G. Barber, P. Liu, R. Lai, F. Hinte, G. Haviland, and B. Vacek, "A 183 GHz low noise amplifier module with 5.5 dB noise figure for the conical-scanning microwave imager sounder (CMIS) program," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2001, pp. 1955-1958.

[47] W. R. Deal, R. Tsai, M. D. Lange, J. B. Boos, B. R. Bennett, and A. Gutierrez, "A low power/low noise MMIC amplifier for phased-array applications using InAs/AlSb HEMT," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2006, pp. 2051-2054.

[48] T. Shibata, J. Nakata, Y. Nanishi, and M. Fujimoto, "A Rutherford backscattering spectroscopic study of the aluminum antimonide oxidation process in air," *Jpn. J. Appl. Phys.*, vol. 33, pp. 1767-1772, Apr. 1994.

[49] C. R. Bolognesi, M. W. Dvorak, and D. H. Chow, "High-transconductance delta-doped InAs/AlSb HFETs with ultrathin silicon-doped InAs quantum well donor layer," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 83-85, Mar. 1998.

[50] B. R. Bennett, R. Magno, J. B. Boos, W. Kruppa, and M. G. Ancona, "Antimonide-based compound semiconductors for electronic devices: A review," *Solid-State Electron.*, vol. 49, no. 12, pp. 1875-1895, Dec. 2005.

[51] A. Mellberg, S. P. Nicols, N. Rorsman, and H. Zirath, "Fabrication and characterization of reactively sputtered TaN thin-film resistors for millimeter wave applications," *Electrochem. Solid State Lett.*, vol. 7, no. 11, pp. 261-263, Nov. 2004.

[52] E. Lefebvre, M. Borg, M. Malmkvist, J. Grahn, L. Desplanque, X. Wallart, Y. Roelens, G. Dambrine, A. Cappy, and S. Bollaert, "(Cl2:Ar) ICP/RIE dry etching of Al(Ga) Sb for AlSb/InAs HEMTs," in *Proc. IEEE 19th Int. InP and Relat. Mater. Conf.*, 2007, pp. 125-128.

[53] J. B. Boos, B. R. Bennett, W. Kruppa, D. Park, J. Mittereder, R. Bass, and M. E. Twigg, "Ohmic contacts in AlSb/InAs high electron mobility transistors for low-voltage operation," *J. Vac. Sci. Technol. B,* vol. 17, no. 3, pp. 1022-1027, May 1999.

[54] H. Matsuzaki, T. Maruyama, T. Enoki, and M. Tokumitsu, "3 S/mm extrinsic transconductance of InP-based high electron mobility transistor by vertical and lateral scale-down," *Electron. Lett.*, vol. 42, no. 15, pp. 67-68, July 2006.

[55] N. Wichmann, I. Duszynski, T. Parenty, S. Bollaert, J. Mateos, X. Wallart, and A. Cappy, "Double-gate HEMTs on transferred substrate," in *Proc. IEEE 15th Int. InP and Relat. Mater. Conf.*, 2003, pp. 118-121.

[56] C. R. Bolognesi, M. W. Dvorak, and D. H. Chow, "Impact ionization suppression by quantum confinement: Effects on the DC and microwave performance of narrow-gap channel InAs/AlSb HFET's," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 826-832, May 1999.

[57] B. Brar and H. Kroemer, "Influence of impact ionization on the drain conductance in InAs-AlSb quantum well heterostructure field-effect transistors," *IEEE Electron Device Lett.*, vol. 16, no. 12, pp. 548-550, Dec. 1995.

[58] J. B. Boos, M. J. Yang, B. R. Bennett, D. Park, W. Kruppa, C. H. Yang, and R. Bass, "0.1 μm AlSb/InAs HEMTs with InAs subchannel," *Electron. Lett.,* vol. 34, no. 15, pp. 1525-1526, July 1998.

[59] A. A. Moolji, S. R. Bahl, and J. A. del Alamo, "Impact ionization in InAlAs/InGaAs HFET's," *IEEE Electron Device Lett.*, vol. 15, no. 8, pp. 313-15, Aug. 1994.

[60] J. Bergman, G. Nagy, G. Sullivan, B. Brar, C. Kadow, H. K. Lin, A. Gossard, and M. Rodwell, "InAs/AlSb HFETs with f_τ and f_{max} above 150 GHz for low-power MMICs," in *Proc. IEEE 15th Int. InP and Relat. Mater. Conf.*, 2003, pp. 219-222.

[61] E. F. Schubert, *Doping in III-V semiconductors*, Cambridge, UK: University press, 1993.

[62] N. Wadefalk, A. Mellberg, I. Angelov, M. E. Barsky, S. Bui, E. Choumas, R. W. Grundbacher, E. L. Kollberg, R. Lai, N. Rorsman, P. Starski, J. Stenarson, D. C. Streit, and H. Zirath, "Cryogenic wide-band ultra-low-noise IF amplifiers operating at ultra-low DC power," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 6, pp. 1705-1711, June 2003.

[63] J. B. Kuang, P. J. Tasker, G. W. Wang, Y. K. Chen, L. F. Eastman, O. A. Aina, H. Hier, and A. Fathimulla, "Kink effect in submicrometer-gate MBE-grown InAlAs/InGaAs/InAlAs heterojunction MESFETs," *IEEE Electron Device Lett.*, vol. 9, no. 12, pp. 630-632, Dec. 1988.

[64] M. R. Murti, J. Laskar, S. Nuttinck, S. Yoo, A. Raghavan, J. I. Bergman, J. Bautista, R. Lai, R. Grundbacher, M. Barsky, P. Chin, and P. H. Liu, "Temperature-dependent small-signal and noise parameter measurements and modeling on InP HEMTs," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2579-2587, Dec. 2000.

[65] G. Meneghesso and E. Zanoni, "Failure modes and mechanisms of InP-based and metamorphic high electron mobility transistors," *Microelectron. Reliab.*, vol. 42, no. 4-5, pp. 685-708, Apr.-May2002.

[66] W. Kruppa, J. B. Boos, B. R. Bennett, and M. Goldenberg, "Traps and the kink effect in AlSb/InAs HEMTs," in *Proc. IEEE 8th Int. InP and Relat. Mater. Conf.*, 1996, pp. 458-461.

[67] B. Georgescu, M. A. Py, A. Souifi, G. Post, and G. Guillot, "New aspects and mechanism of kink effect in InAlAs/InGaAs/InP inverted HFETs," *IEEE Electron Device Lett.*, vol. 19, no. 5, pp. 154-156, May 1998.

[68] R. Lai, P. K. Bhattacharya, D. Yang, T. L. Brock, S. A. Alterovitz, and A. N. Downey, "Characteristics of 0.8- and 0.2-μm gate length $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As/InP$ ($0.53 \leq x \leq 0.70$) modulation-doped field-effect transistors at cryogenic temperatures," *IEEE Trans. Electron Devices*, vol. 39, no. 10, pp. 2206-2213, Oct. 1992.

[69] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151-1159, July 1988.

[70] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET`s for millimeter-wave applications," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 3, pp. 432-437, Mar. 1996.

[71] C. van Niekerk, P. Meyer, D. M. M. P. Schreurs, and P. B. Winson, "A robust integrated multibias parameter-extraction method for MESFET and HEMT models," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 5, pp. 777-786, May 2000.

[72] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to GaN devices," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 11, pp. 3440-3448, Nov. 2005.

[73] R. Reuter, M. Agethen, U. Auer, S. van Waasen, D. Peters, W. Brockerhoff, and F. J. Tegude, "Investigation and modeling of impact ionization with regard to the RF and noise behavior of HFET," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 6, pp. 977-983, June 1997.

[74] J. B. Boos, B. V. Shanabrook, D. Park, J. L. Davis, H. B. Dietrich, and W. Kruppa, "Impact ionisation in high-output-conductance region of 0.5 µm AlSb/InAs HEMTs," *Electron. Lett.,* vol. 29, no. 21, pp. 1888-1890, Oct. 1993.

[75] R. Tsai, N. Barsky, J. Lee, J. B. Boos, B. R. Bennett, R. Magno, C. Namba, P. H. Liu, A. Gutierrez, and R. Lai, "MMIC compatible AlSb/InAs HEMT with stable AlGaSb buffer layers," in *Proc. IEEE Lester Eastman Conf.*, 2002, pp. 276-280.

[76] H. Rothe and W. Dahlke, "Theory of noisy fourpoles," *Proc. IRE*, vol. 44, no. 6, pp. 811-818, June 1956.

[77] P. Heymann and H. Prinzler, "Improved noise model for MESFETs and HEMTs in lower gigahertz frequency range," *Electron. Lett.*, vol. 28, no. 7, pp. 611-612, Mar. 1992.

[78] R. Reuter, S. van Waasen, and F. J. Tegude, "A new noise model of HFET with special emphasis on gate-leakage," *IEEE Electron Device Lett.*, vol. 16, no. 2, pp. 74-76, Feb. 1995.

[79] T. Enoki, K. Arai, and Y. Ishii, "Delay time analysis for 0.4- to 5-µm-gate InAlAs-InGaAs HEMTs," *IEEE Electron Device Lett.*, vol. 11, no. 11, pp. 502-504, Nov. 1990.

[80] K. Shinohara, T. Matsui, T. Mimura, and S. Hiyamizu, "Novel asymmetric gate-recess engineering for sub-millimeter-wave InP-based HEMTs," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2001, pp. 2159-2162.

[81] T. Suemitsu, T. Enoki, H. Yokoyama, Y. Umeda, and Y. Ishii, "Impact of two-step-recessed gate structure on RF performance of InP-based HEMTs," *Electron. Lett.*, vol. 34, no. 2, pp. 220-222, Jan. 1998.

[82] S. Wada, J. Yamazaki, M. Ishikawa, and T. Maeda, "An 0.1-μm voidless double-deck-shaped (DDS) gate HJFET with reduced gate-fringing-capacitance," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 859-864, May 1999.

[83] L. D. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloian, "50-nm self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2007-2014, Sep. 1992.

[84] D. A. J. Moran, H. McLelland, K. Elgaid, G. Whyte, C. R. Stanley, and I. Thayne, "50-nm self-aligned and "standard" T-gate InP pHEMT comparison: the influence of parasitics on performance at the 50-nm node," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2920-2925, Dec. 2006.

[85] J. M. Lopez, T. Gonzalez, D. Pardo, S. Bollaert, T. Parenty, and A. Cappy, "Design optimization of AlInAs-GaInAs HEMTs for high-frequency applications," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 521-528, Apr. 2004.

[86] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Reduction of the feedback capacitance of HFETs by changing transistor layout and using via holes for source grounding," in *Proc. 24th Eur. Microw. Conf.*, 1994, pp. 764-769.

[87] Y. Awano, M. Kosugi, K. Kosemura, T. Mimura, and M. Abe, "Short-channel effects in subquarter-micrometer-gate HEMTs: simulation and experiment," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2260-2266, Oct. 1989.

[88] D.-H. Kim and J. A. del Alamo, "Scaling Behavior of In0.7Ga0.3As HEMTs for Logic," in *IEEE Int. Electron Devices Meet. Tech. Dig.*, 2006, pp. 837-840.

[89] T. Takahashi, M. Sato, K. Makiyama, T. Hirose, and N. Hara, "InAlAs/InGaAs HEMTs with Minimum Noise Figure of 1.0 dB AT 94 GHz," in *Proc. IEEE 19th Int. InP and Relat. Mater. Conf.*, 2007, pp. 55-58.

[90] J. Mateos, T. Gonzalez, D. Pardo, S. Bollaert, T. Parenty, and A. Cappy, "Design optimization of AlInAs-GalnAs HEMTs for low-noise applications," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1228-1233, Aug. 2004.

[91] L. D. Nguyen, D. C. Radulescu, M. C. Foisy, P. J. Tasker, and L. F. Eastman, "Influence of quantum-well width on device performance of Al0.30Ga0.70As/In0.25Ga0.75As (on GaAs) MODFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 5, pp. 833-838, May 1989.

[92] T. Parenty, S. Bollaert, J. Mateos, X. Wallart, and A. Cappy, "Design and realization of sub 100 nm gate length HEMTs," in *Proc. IEEE 13th Int. InP and Relat. Mater. Conf.*, 2001, pp. 626-629.

[93] M. Malmkvist, M. Borg, W. Shumin, and J. Grahn, "Effect of Schottky layer thickness on DC, RF and noise of 70-nm gate length InP HEMTs," in *Proc. IEEE 18th Int. InP and Relat. Mater. Conf.*, 2006, pp. 329-331.

[94] M. Tong, K. Nummila, A. Ketterson, I. Adesida, C. Caneau, and R. Bhat, "InAlAs/InGaAs/InP MODFET's with uniform threshold voltage obtained by selective wet gate recess," *IEEE Electron Device Lett.*, vol. 13, no. 10, pp. 525-527, Oct. 1992.

[95] K. Shinohara, Y. Yamashita, A. Endoh, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Importance of gate-recess structure to the cutoff frequency of ultra-high-speed InGaAs/InAlAs HEMTs," in *Proc. IEEE 14th Int. InP and Relat. Mater. Conf.*, 2002, pp. 451-454.

[96] Y. C. Chen, R. Lai, H. Wang, H. C. Yen, D. Streit, R. M. Dia, W. Jones, T. Block, P. H. Liu, T.-W. Huang, Y. C. Chou, and K. Stamper, "Optimization of InGaAs/InAlAs/InP HEMT gate recess process for high frequency and high power applications," in *Proc. IEEE 9th Int. InP and Relat. Mater. Conf.*, 1997, pp. 509-512.

[97] T. Arai, K. Sawada, N. Okamoto, K. Makiyama, T. Takahashi, and N. Hara, "Suppression of drain conductance in InP-based HEMTs by eliminating hole accumulation," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1189-1193, May 2003.

[98] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, "85nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications," in *IEEE Int. Electron Devices Meet. Tech. Dig.*, 2005, pp. 763-766.

[99] Y. Sun, E. W. Kiewra, S. J. Koester, N. Ruiz, A. Callegari, K. E. Fogel, D. K. Sadana, J. Fompeyrine, D. J. Webb, J. P. Locquet, M. Sousa, R. Germann, K. T. Shiu, and S. R. Forrest, "Enhancement-mode buried-channel $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ MOSFETs with high-κ gate dielectrics," *IEEE Electron Device Lett.*, vol. 28, no. 6, pp. 473-475, June 2007.

[100] W. R. Deal, S. Din, V. Radisic, J. Padilla, X. B. Mei, W. Yoshida, P. H. Liu, J. Uyeda, M. Barsky, T. Gaier, A. Fung, L. Samoska, and R. Lai, "Demonstration of a sub-millimeter wave integrated circuit (S-MMIC) using InP HEMT with a 35-nm Gate," in *Proc. IEEE Compon. Semiconduct. IC Symp.*, 2006, pp. 33-36.

[101] W. R. Deal, X. B. Mei, V. Radisic, W. Yoshida, P. H. Liu, J. Uyeda, M. Barsky, T. Gaier, A. Fung, L. Samoska, and R. Lai, "Demonstration of a 270-GHz MMIC amplifier using 35-nm InP HEMT technology," *IEEE Microw. Wirel. Compon. Lett.*, vol. 17, no. 5, pp. 391-393, May 2007.

[102] M. Riaziat, R. Majidi-Ahy, and I. J. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 3, pp. 245-251, Mar. 1990.

[103] S. Weinreb, R. Lai, N. Erickson, T. Gaier, and J. Wielgus, "W-band InP wideband MMIC LNA with 30 K noise temperature," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 1999, pp. 101-104.

[104] G. Gonzalez, *Microwave transistor amplifiers: Analysis and design*, 2 ed., New Jersey, USA: Prentice Hall, 1997.

[105] A. Katz, S. J. Pearton, S. Nakahara, F. A. Baiocchi, E. Lane, and J. Kovalchick, "Tantalum nitride films as resistors on chemical vapor deposited diamond substrates," *J. Appl. Phys.*, vol. 73, no. 10, pp. 5208-5212, May 1993.

[106] R. F. Kopf, R. Melendes, D. C. Jacobson, A. Tate, M. A. Melendes, R. R. Reyes, R. A. Hamm, Y. Yang, J. Franckoviak, N. G. Weimann, H. L. Maynard, and C. T. Liu, "Thin-film resistor fabrication for InP technology applications," *J. Vac. Sci. Technol. B*, vol. 20, no. 3, pp. 871-875, May 2002.

[107] J. Scarpulla, E. D. Ahlers, D. C. Eng, D. L. Leung, S. R. Olson, and C.-S. Wu, "Dielectric breakdown, defects and reliability in SiN MIMCAPs," in *Proc. GaAs Reliability Workshop*, 1998, pp. 92-105.

[108] T. Ashley, L. Buckle, S. Datta, M. T. Emeny, D. G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. J. Wallis, P. J. Wilding, and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," *Electron. Lett.*, vol. 43, no. 14, July 2007.