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Optimization of the PWM Switching Algorithm and the Output Filter of a Full Bridge Zero Voltage PWM Switching Converter.

Thesis for the Master of Sciences (MSc) degree

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Abstract

In this thesis work, optimization of a power supply is done. This is done by employing a variable switching frequency (VSF) algorithm to ensure the soft switching of a full bridge zero voltage PWM switched converter while keeping the output waveform quality. Also a reduction of the wire losses of the output filter inductor has been achieved by employing Litz wires.

It was found out that by using the VSF algorithm the switching losses were decreased. Moreover, by employing the VSF algorithm, the harmonic content of the output voltage of the full bridge has become more homogeneous throughout the frequency range.

In addition to these, it was found out that the use of the solid wires introduces high AC resistance in the inspected frequency range. Accordingly, by employing the Litz wire this AC resistance can be decreased and the RI^2 losses of the winding of the inductor can be reduced.

Preface

This work has been carried out for the Aibel AS, Oslo, Norway and registered as a thesis work for the MSc Degree in Electrical Power Engineer for the Division of Electric Power Engineering at Chalmers University of Technology, Goteborg.

The work has been carried out at the R&D laboratory of the Aibel AS, Oslo, Norway from June 2007 to November 2007.

I would like to thank my supervisor, Prof. Torbjörn Thiringer who has not only enlightened me with his courses at Chalmers University of Technology but also has supported in different areas to carry out this work. Further, I thank all the members of the Division of Electric Power Engineering at Chalmers University of Technology who has always supported me, and have shared their valuable knowledge. Especially I would like to thank Hakan Unal, Tonn Arro and SVEA for being there as friends and making it easier.

I would like to thank also Deborah Wood, my dear manager at Aibel AS, who made it possible for me to have this thesis work. Besides her, many thanks go to Svein Tryti, my great supervisor at Aibel AS, who has also supported me and enlightened me with his knowledge in electric power engineering. Also thanks for all my colleagues at the Department of R&D at Aibel AS, for making it easier for me during my thesis work.

Finally, all this would not have been possible without the generous support of my family. I can not thank enough for their unlimited patience and trust in me and what I am doing. They give reasons to me to be better, to make them proud.

For all your help I need to say:

Thank You.

Table of Content

List of Abbreviations

MSc : Master of Science
VIEC : Vessel Internal Electrostatic Coalescer.
DSP : Digital Signal Processor.
PWM : Pulse Width Modulation.
R&D : Research and Development.
PC : Personal Computer.
PLC : Programmable Logic Controller.
CPU : Central Processing Unit.
AC : Alternating Current.
DC : Direct Current.
ZVS : Zero Voltage Switching.
THD : Total Harmonic Distortion.
EMC : Electromagnetic Compatibility.
RMS : Root Main Square.
VSF : Variable Switching Frequency.
EMI : Electromagnetic Interference.
FSF: Fixed Switching Frequency.
OFIBO : Output Filter Inductor Before Optimization.
PT : Platinum.
RTD : Resistive Temperature Detector.
DAQ : Data Acquisition.

1. Introduction to the Thesis Work

1.1. Problem Background

Since 1999 Vetco Aibel has had an extensive R&D program focused on compact separation of the mixture of oil, water and gas. Part of the development has been about incorporating electrostatic coalescers into separation baffles. One result of the research is the increasingly known VIEC.

The VIEC uses an electrostatic field to create forces between the water droplets. The water droplets get drawn to each other and coalesce to become bigger droplets. It is stated by the Stokes' Theorem [13] that bigger droplets sink and separate faster than smaller droplets.

To create the magnetic field two metal plates in the VIEC block are charged with a voltage and frequency controlled power supply. Aibel with Kitron development has developed a power supply for powering various coalescer products, mainly the VIEC. The power supply was developed to deliver an AC output of up to 250 V, up to 200 W and up to 2 A. It is designed for frequency range from 0 Hz up to 10000 Hz. Because the power supply was intended to be used with various future products it was equipped with a DSP (TI TMS320F2810) that controls most parts of the power supply, including switching patterns, dead-time generation and coalescer control functionality, causing the power supply to be easily reprogrammable for new applications.

This thesis is hence about optimization of an existing full bridge zero voltage PWM switched mosfet converter. For the optimization of the converter it is important to consider typical coalescer loads. To limit the scope of the thesis the load considered shall be a typical VIEC load, which is a parallel resonant circuit with resistive losses. However, the power supply must also be usable with a resistive load.

1.2. Previous Work Done

Throughout the evolution of the VIEC power supply various design optimisations have been done. These optimisations are done by making both software and hardware changes.

When first designed, the full bridge inverter of the power supply was a hard switched, unipolar inverter using the PWM switching algorithm. S. Halasz, G. Csonka, A.A.M. Hassan and B.T. Huu [15] state that unipolar modulation technique - as opposed to the bipolar one - does not produce some of the harmonics bipolar one produce. Therefore unipolar PWM switching is an effective way for reducing harmonics but hard switching causes high turn on switching losses. As an earlier optimisation, the switching algorithm was changed to bipolar soft switching PWM algorithm with employing the power mosfets produced by Infeneon, named as the Coolmos.

The idea was to trigger the gate of the coolmos transistors when the current is freewheeling through the integral diode of the respective coolmos. After that the inverters have had losses occurring only at turn-off [1].

The problem with this kind of switching manner was that, the reverse recovery current of the integral diode causes high current peaks at the turn on of the mosfets thereby causing high switching losses. To overcome this problem a technique called active channel freewheeling was employed as the next optimisation.

The idea of the technique is to shunt freewheeling current away from the internal diode by decreasing the deadtime between the leg phases [2]. It is shown by Hongrae Kim, Thomas M. Jahns, and Giri Venkataramanan [2] that the peak turn on the current and the switching losses can be decreased drastically, especially at low current levels, by employing active channel freewheeling.

It is also shown in reference [2] that the turn-on switching losses are reduced more at higher loads. The objective of the active channel freewheeling technique is to use the mosfet's channel for current conduction during both forward conduction and freewheeling operation. Therefore the success of this technique depends on the ability of the channel to shunt as much device current as possible away from the body diode during reverse current conduction [2]. With less deadtime employed the peak current becomes lower at the turn on of the switch [2].

After increasing the output current from the full bridge inverter of the power supply by employing the active channel freewheeling, there was a need for redesigning the output filter inductors. To enable the windings to carry more current without having much loss,

the effective area of the conductors were increased. This was done by introducing two more parallel windings.

1.3. The Purpose of the Thesis Work

The power supply fulfils the design requirements mentioned in the section 1.1, but later measurements and operational experience has brought up a need for higher current and power output, lower losses, less generated EMI and higher harmonic quality for the output.

It is expected that these new demands to some extent can be fulfilled by optimizing the power supply design and by gaining better knowledge about the limitations in the design. It is not an option to re-design the board layout of the power supply at this time.

Moreover it is believed that the main focus should be on the optimisation of the switching algorithm and the output filter inductor winding.

1.4. The Outline of the Thesis Work

The work has several goals regarding the optimization of the converter:

- Reducing the switching losses, especially at high output currents
- Having higher output current and power from the full bridge
- Spreading harmonics by utilizing variable switching frequency
- Redesigning the output filter inductor in order to reduce the winding losses

Changes to the converter are limited to change of component values and software changes. Other types of changes are suggested for implementation in a later power supply re-design.

Therefore, the behaviour and the control of the major components is to be studied. There are, the full bridge zero voltage PWM switched mosfet converter, the DSP and the output filter.

The power supply is to be studied and also a literature survey about the soft switching converter topologies is to be done in order to classify the power supply type.

A setup experiment system is to be built in order to investigate maximum power delivered to load and maximum current of load with respect to output voltage, and output voltage frequency. Moreover the harmonic contents of output current and voltage, before and after output filter is to be studied for later comparisons.

A literature survey should be done in order to have an idea on possible improvements of the PWM switching algorithm. Variable switching frequency is to be evaluated.

The desired switching pattern should be implemented to the VIEC power supply converter. Lab tests must be carried out to verify the results.

Calculations for the output filter are to be done for desired output conditions. Possible solutions to avoid half turn in one output inductor are to be searched for.

The design of the related setup should be simulated and the results of the simulations should be evaluated.

After the simulations, the necessary changes should be implemented to the hardware, and lab tests should be carried in order to evaluate the results.

2. Introduction to the VIEC

2.1. The VIEC System Description

The VIEC is composed of coalescer elements, as shown in Figure 2.1, located in a supporting perforated wall in the vessel perpendicular to the fluid flow. The coalescer elements shall as a minimum cover the oil and emulsion layer. Each coalescer element is moulded in epoxy and consists of flat wide channels with low height stacked upon each other with electrode plates moulded in between each channel. The electrodes are attached to a high voltage transformer moulded inside the coalescer elements. All wires are connected with "subsea" connectors and further protected in 316 Stainless tubing conduits for added mechanical integrity.

Figure 2.1. VIEC element,

The coalescer elements are installed in a metal framework together with perforated plates, to ensure even distribution of flow throughout the cross section.

Figure 2.2 illustrate a typical location of the VIEC elements at the cross section. The VIEC elements are proposed installed to cover the area from Low Interface Level up to High Liquid Level.

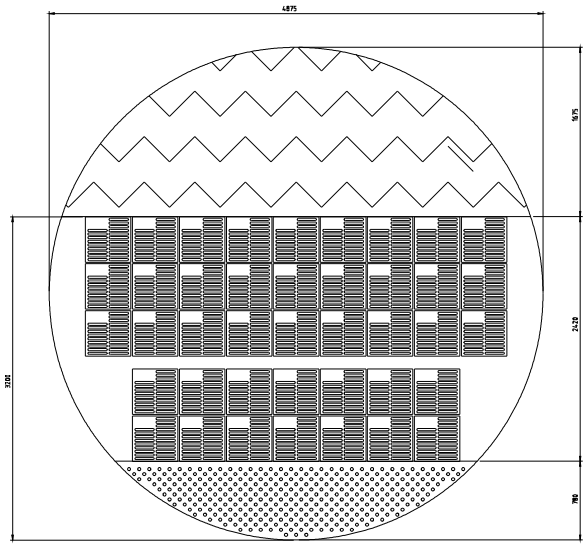

Figure 2.2. Typical locations of the VIEC elements in a cross section of a separator tank,

The VIEC elements are powered and controlled from the dedicated cabinets. Figure 2.3 shows a typical set of VIEC Control Cabinets.

Figure 2.3. VIEC Control Cabinets,

The VIEC elements are held in place with metal frame sections shown in Figure 2.4. The remaining cross sectional area will be filled with single perforated plates.

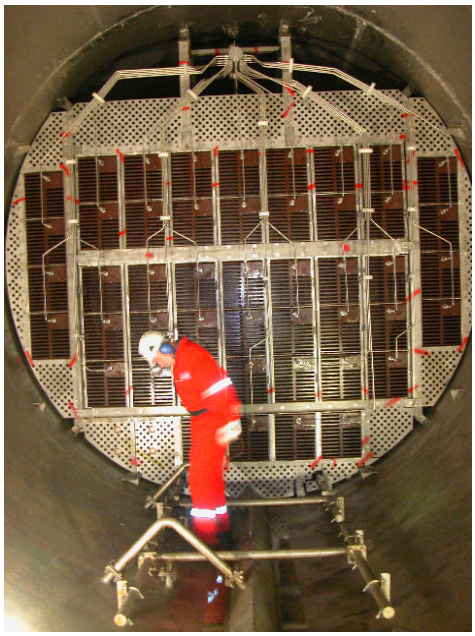

Figure 2.4. Assembled VIEC wall,

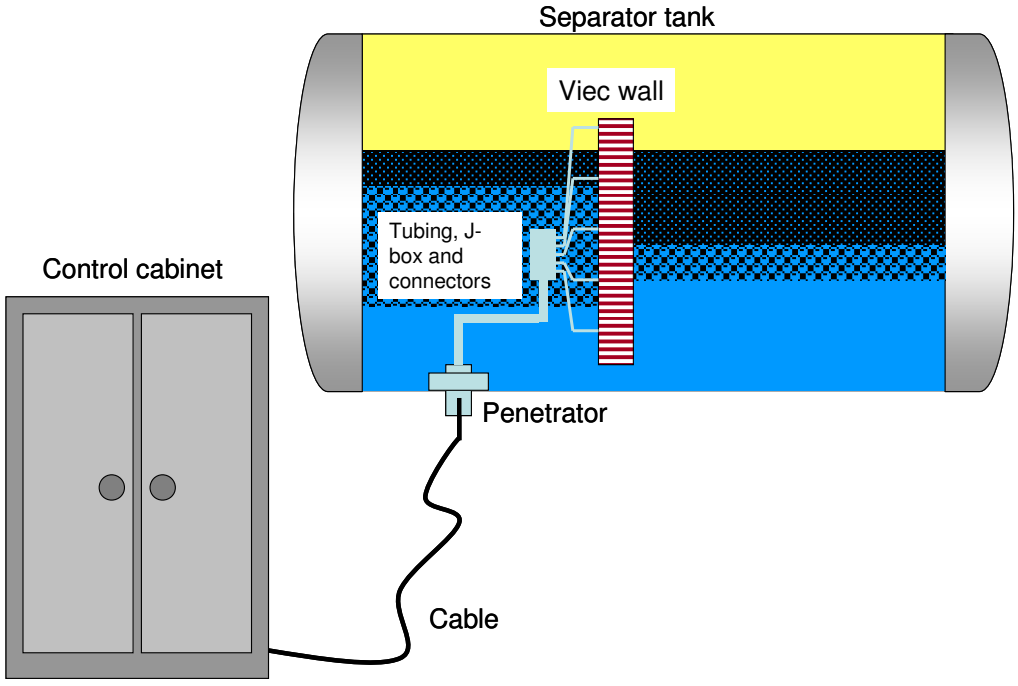

Figure 2.5. Complete VIEC system for a separator tank,

2.2. The Power Supply Control System

In this section the structure and the control of the power supply system, which feeds the VIEC blocks, will be analyzed. The parts in the system will be introduced.

The overall power supply and control system is shown below in Figure 2.6.

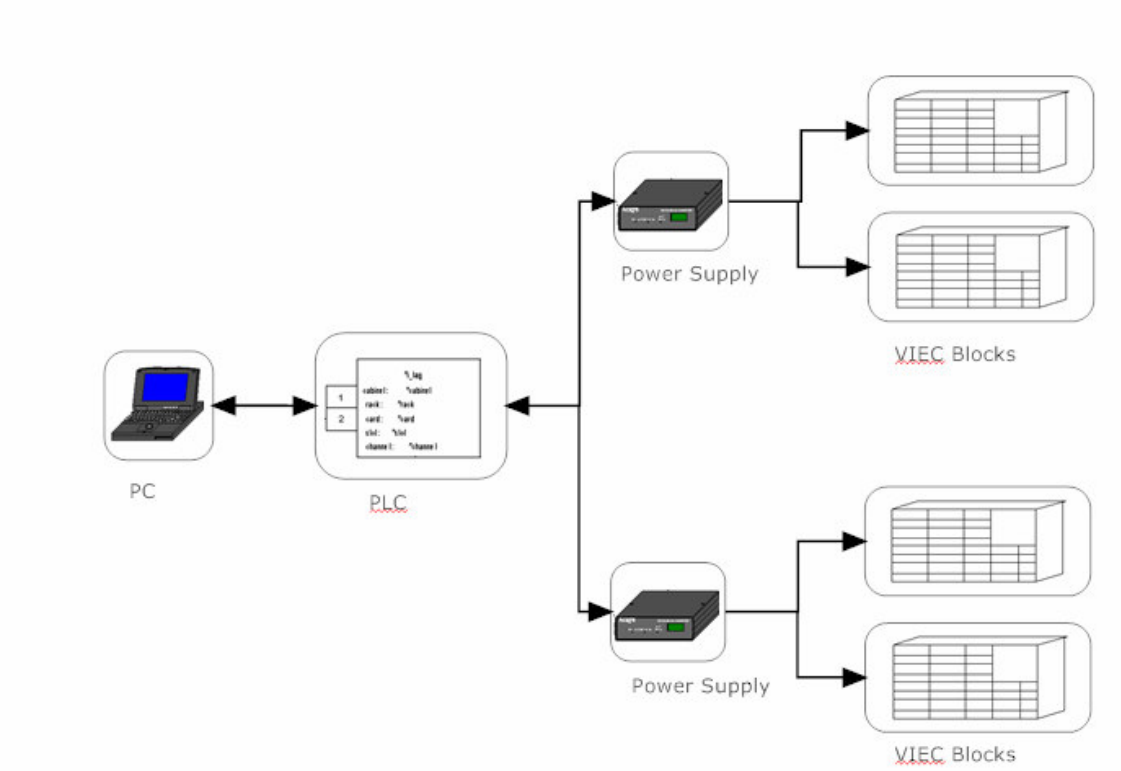

Figure 2.6. Control system of VIEC blocks,

As it is seen above, the whole system is modified, controlled or monitored over a PC. After the system is set up and uploaded by the software, the upper level control is done by the PLC and lower lever control is done by the DSP in the converter to supply the VIEC blocks with the voltage at desired magnitude and frequency. The PLC and the power supplies (converters) are placed in the control cabinet. The power and the signal cables from the converter are connected to VIEC blocks, with the help of the penetrators and the subsea tubing.

2.2.1. The PC

The PC is used as an interface between operators and the system. The interface is programmed in LabView ver 8.2.1. The standard PC is an "ELRACK-220GB-P4" rack mounted industrial PC from Elektronix AS.

The PC was changed into an industrial PC because the requirements to an industrial PC are stricter than a regular home PC, in order to have increased EMC [14].
The PC has a MOXA CP132-UL V2.0 card installed for RS485 communication. Also the PC screen is a "HP TFT7600 Rack mount keyboard and monitor".

2.2.2. The PLC

The PLC used in the control cabinet is an industrial OMRON PLC including the parts, listed in table 2.1, mounted from left to right as seen in Figure 2.7.

Figure 2.7. Standard Omron PLC,

Table 2.1. Standard Omron PLC parts

1 Power supply 230VAC. CJ1W-PA205R
1 CPU: Omron CJ1M-CPU12
4 RS-485 cards: CJ1W-SCU41-V2
1 Digital Input card, 16 channels: CJ1W-ID211
1 Digital Output card, 16 channels: CJ1W-OC211
1 Analogue Output card, 4 channels: CJ1W-DA041
1 Temperature measurement card for PT100 elements: CJ1W-TS562

The PLC is programmed with help of Omron CX Programmer and Omron CX Protocol.

2.2.3. The DSP

Power Supply uses TMS320C28x™ DSC, which is a highly integrated DSP with high-performance solutions for demanding control applications. The overall features of the DSP are given in table 2.2.

Table 2.2. Features of Texas Instruments DSP,

FEATURE		F2810	F2811	F2812	C2810	C2811	C2812
Instruction Cycle (at 150 MHz)		6.67 ns	6.67 ns	6.67 ns	6.67 ns	6.67 ns	6.67 ns
Single-Access RAM (SARAM) (16-bit word)		18K	18K	18K	18K	18K	18K
3.3-V On-Chip Flash (16-bit word)		64K	128K	128K	—	—	—
On-Chip ROM (16-bit word)		—	—	—	64K	128K	128K
Code Security for On-Chip Flash/SARAM/OTP/ROM		Yes	Yes	Yes	Yes	Yes	Yes
Boot ROM		Yes	Yes	Yes	Yes	Yes	Yes
OTP ROM (1K X 16)		Yes	Yes	Yes	Yes‡	Yes‡	Yes‡
External Memory Interface		—	—	Yes	—	—	Yes
Event Managers A and B (EVA and EVB)		EVA, EVB	EVA, EVB	EVA, EVB	EVA, EVB	EVA, EVB	EVA, EVB
• General-Purpose (GP) Timers		4	4	4	4	4	4
• Compare (CMP)/PWM		16	16	16	16	16	16
• Capture (CAP)/QEP Channels		6/2	6/2	6/2	6/2	6/2	6/2
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes
12-Bit ADC		Yes	Yes	Yes	Yes	Yes	Yes
• Channels		16	16	16	16	16	16
32-Bit CPU Timers		3	3	3	3	3	3
SPI		Yes	Yes	Yes	Yes	Yes	Yes
SCIA, SCIB		SCIA, SCIB	SCIA, SCIB	SCIA, SCIB	SCIA, SCIB	SCIA, SCIB	SCIA, SCIB
CAN		Yes	Yes	Yes	Yes	Yes	Yes
McBSP		Yes	Yes	Yes	Yes	Yes	Yes
Digital I/O Pins (Shared)		56	56	56	56	56	56
External Interrupts		3	3	3	3	3	3
Supply Voltage		1.8-V Core, (135 MHz) 1.9-V Core (150 MHz), 3.3-V I/O					
Packaging		128-pin PBK	128-pin PBK	179-ball GHH and ZHH 176-pin PGF	128-pin PBK	128-pin PBK	179-ball GHH and ZHH 176-pin PGF
Temperature Options	A: –40°C to 85°C	Yes	Yes	Yes	Yes	Yes	Yes
	S: –40°C to 125°C	Yes	Yes	Yes	Yes	Yes	Yes
	Q: –40°C to 125°C	Yes	Yes	PGF only	Yes	Yes	PGF only

† The *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors Silicon Errata* (literature number SPRZ193) has been posted on the Texas Instruments (TI) website. It will be updated as needed.
‡ On C281x devices, OTP is replaced by a 1K X 16 block of ROM.

2.3. The Power Supply

The power supply consists of three main parts. The power correction filter and the rectifier together can be called the input stage. The full bridge creates the required AC output by employing the PWM switching algorithm. Lastly there is an output filter stage in order to remove undesired harmonics at the output voltage. The input stage is not subject to the scope of this study. Moreover the DC link voltage is assumed to be pure

DC in most of the calculations throughout the paper. The overall block diagram of the system is shown in Figure 2.8.

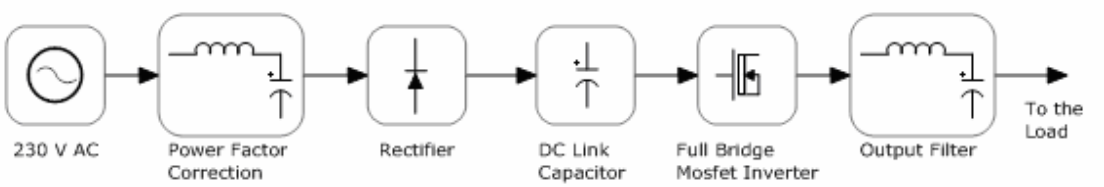

Figure 2.8. Block diagram of converter,

The Power Supply is controlled in a manner that magnitude and the frequency of the main component of the output voltage are controlled, with respective current, power and frequency limitations.

Also it can be noted that the main component of the output current follows the output frequency reference.

2.3.1. The Full Bridge Inverter

Full Bridge inverter consists of four Coolmos switches and their drive circuits. The simplified schematic of the full bridge inverter without the gate drive circuits is given in Figure 2.9.

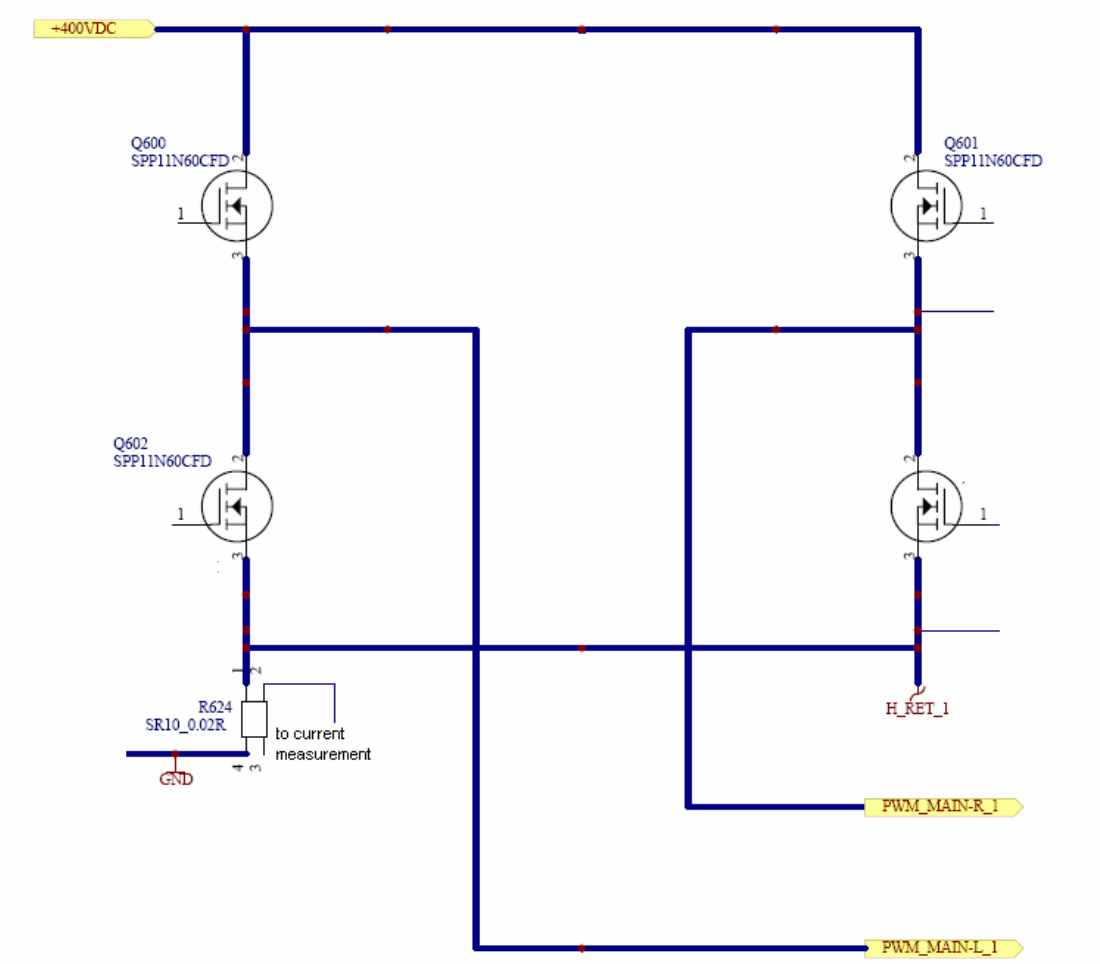

Figure 2.9. Simplified schematics of full bridge converter,

2.3.2. The Output Filter

The Output filter is a low pass filter with two parallel LC stages and a common mode filter. The output filter's simplified schematic is given below in Figure 2.10.

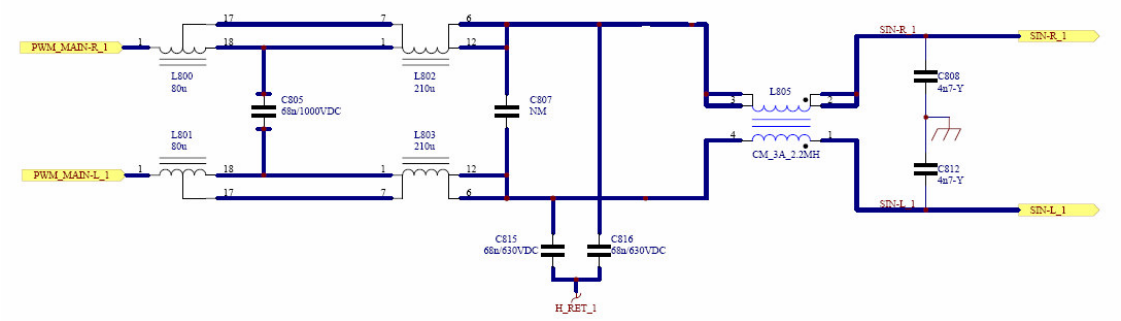

Figure 2.10. Simplified schematics of output filter,

A picture of the power supply is given below in Figure 2.11.

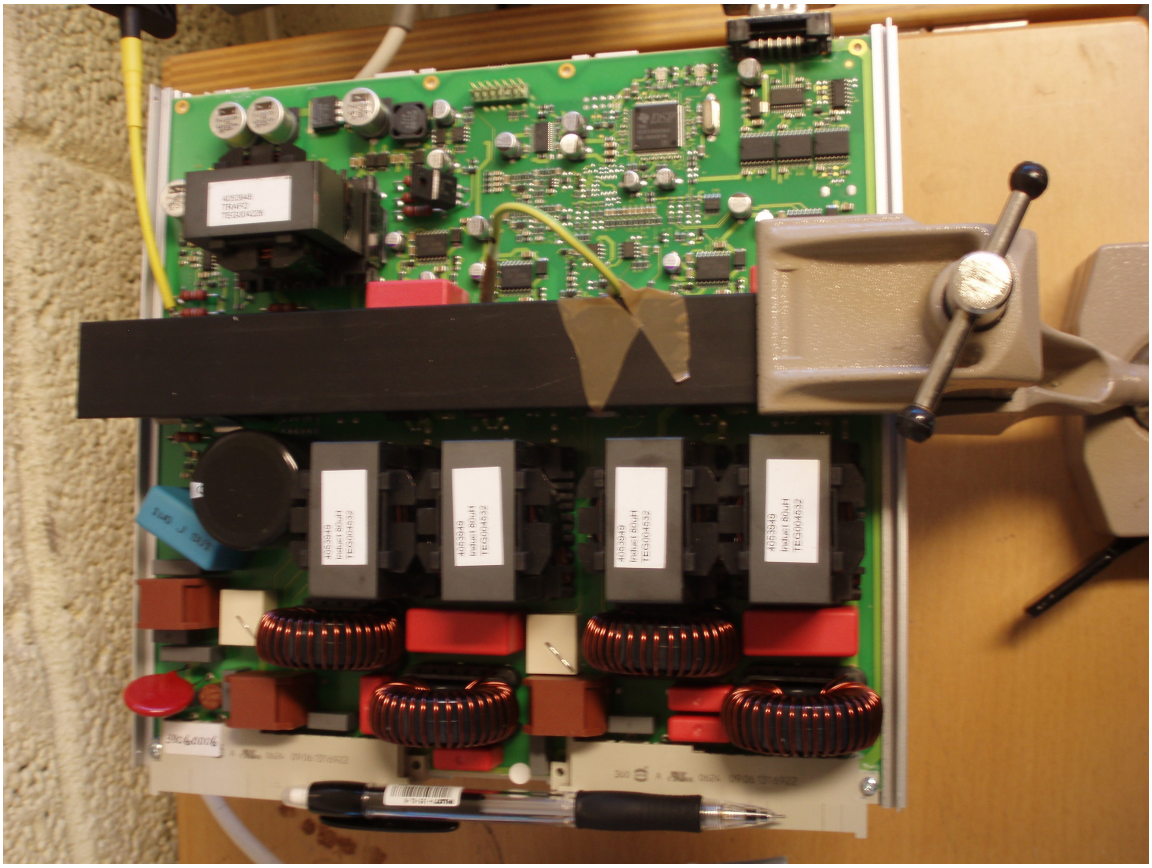

Figure 2.11. A picture of the power supply,

2.4. The Load

The load can be simplified as a parallel L-C resonance circuit with ohmic losses. The inductance part of the load is caused by the transformer of the VIEC block. The

transformers secondary winding has a rating for 4 kVA power, and 5 kHz frequency. Its primary winding is rated for 230 V RMS and 2 A RMS.

The capacitance part of the load is caused by the perforated plates of the VIEC block and the emulsion between.

3. The Effects on the Switching Losses of the power Supply

In this part of the work an experiment system is built in order to investigate possible effects on the switching losses of the power supply. Moreover the converter is going to be classified considering the layout and the switching.

After it is assured that the current is shunted as much away from the body diode of the Coolmos as possible during the reverse current conduction, the only control requirement left for ZVS is to assure that the current changes polarization in each switching cycle. This is due to the fact that the turn on of each Coolmos should occur during the time when the freewheeling current exists in the body diode of the respective Coolmos. Therefore the ripple of the current should be enough to assure this transition.

It has been mentioned in Section 2 of this thesis report that the load is a parallel resonance circuit with ohmic losses. Furthermore it can be added that the load seen from the output of the full bridge converter of the power supply behaves inductive in the operating frequency range. Below the equations for an inductance for transient and steady state are given,

$$V_L(t) = L\frac{di(t)}{dt} \tag{3.1}$$

$$V_L = L\frac{\Delta i}{\Delta t} \tag{3.2}$$

$$\Delta i = \frac{V_L \Delta t}{L} \tag{3.3}$$

Considering (3.3), it is seen that the ripple of the current, Δi, depends on; Δt which is dependent on duty cycle and switching frequency, V_L which is the DC link voltage and L which is the characteristic inductance of the load seen from full bridge (0.145 mH in our case). Since the DC link voltage and the characteristic inductance of the load seen from full bridge of the power supply can be considered as constants, it is appropriate to put focus on investigating the effects of the duty cycle and the switching frequency on the switching losses.

3.1. System Setup for the Experiments

To achieve the goals of this chapter, an experiment setup is built. The setup consists of an isolation transformer, an emergency button, the power supply, a load bank, an oscilloscope and a computer. The overall block diagram of the experiment system is given in Figure 3.1.

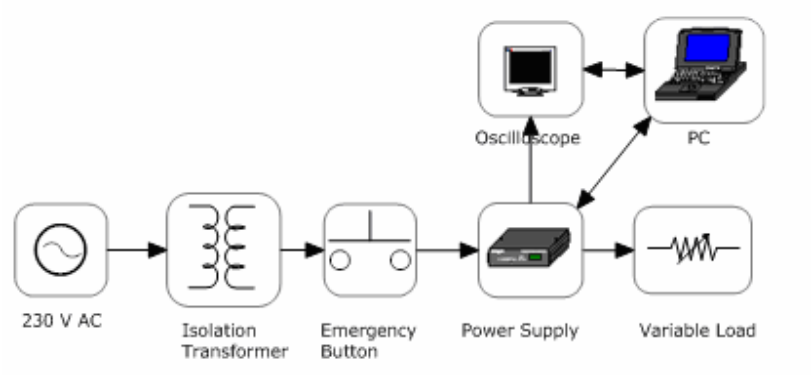

Figure 3.1. Experimental system block diagram,

The reason to use the isolation transformer is to provide galvanic isolation for the whole system. By decoupling the system electrically from the network, the grounding for measurements is safer and easier to make. The ratio for the transformer is 1:1 and the middle of the secondary winding is grounded.

The emergency button is for disconnecting the system from the network, in case of emergency situations such as failure of a component or a quick change of a decision for the setup. The button is a standard, two states emergency button and it can be locked if desired.

The power supply used is the one mentioned before in the report. It has an input slot with the input and output of power and another RS485 industrial communication port. The industrial communication port is used for the communication between the power supply and the PLC since there are more than one power supplies in a system. Therefore it is not used in this thesis work. On the other hand, the RS232 communication port, which is in the front panel of the power supply, is used for the computer based control of the power supply.

The oscilloscope is an Agilent DSO6034A, four channel standard oscilloscope. It has a LAN connection facility to the PC, via a VISA address. The manufacturer also supplies the software to capture data from the oscilloscope.

The computer is a laptop pc, which is used to control the frequency and the magnitude of the output voltage of the power supply online. Also it is used to capture the data from the oscilloscope and process the data with appropriate software, such as Matlab and MathCAD.

The load bank used in the experiments consists of 200W 230 VAC light bulbs. Although the load is purely resistive, because of the high inductances of the output filter of the power supply and the switching frequency range that is around 140 kHz, the load is seen as an inductance and resistance. For ease of calculations and low effect of resistance of the power supply load, the load from the full bridge output seen is taken as an inductance with a characteristic inductance of 0.145 mH.

A picture of the experiment system is given in Figure 3.2.

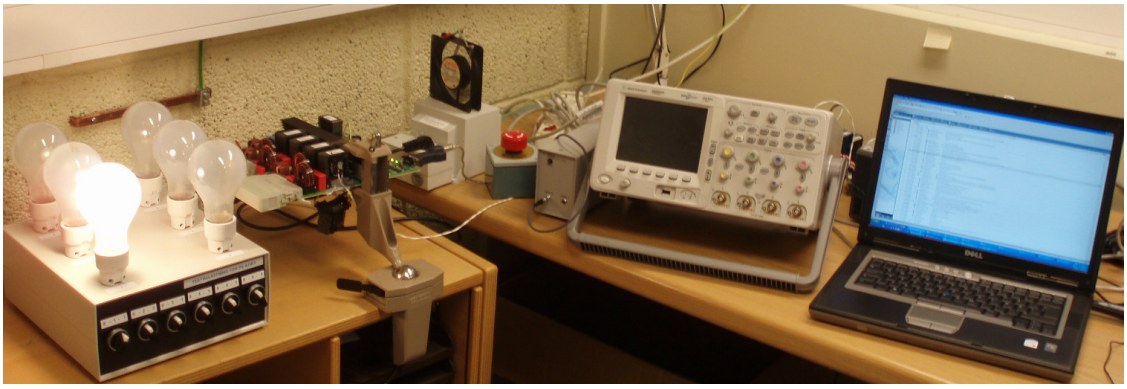

Figure 3.2. Experiment Setup,

The measurement points for the measurements of the turn on switching of the Coolmos are presented in Figure 3.3.

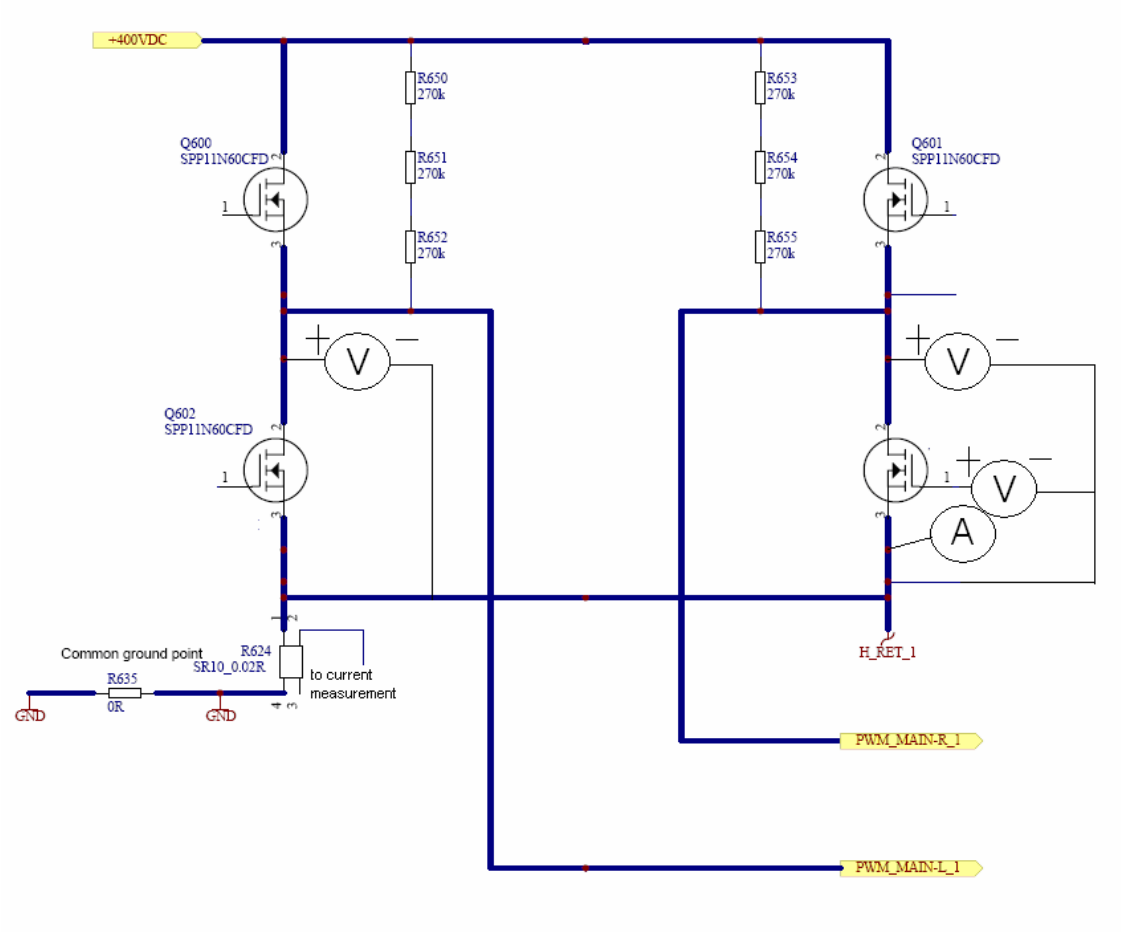

Figure 3.3. Measurement points for switching waveforms,

3.2. Results of the Experiments

3.2.1. Switching Without Load

The switching waveforms of the power supply are given below in Figure 3.4. It is seen that the peak current during turn-on of switching is so low that it can be neglected, which leads to lossless turn on of the Coolmos. That behaviour is verified also by the power dissipation graph of the switching. On the other hand there are turn off losses because of hard switching at turn off. These turn off losses are in the range of the safe operating area of the Coolmos, therefore they are not in the scope of this paper.

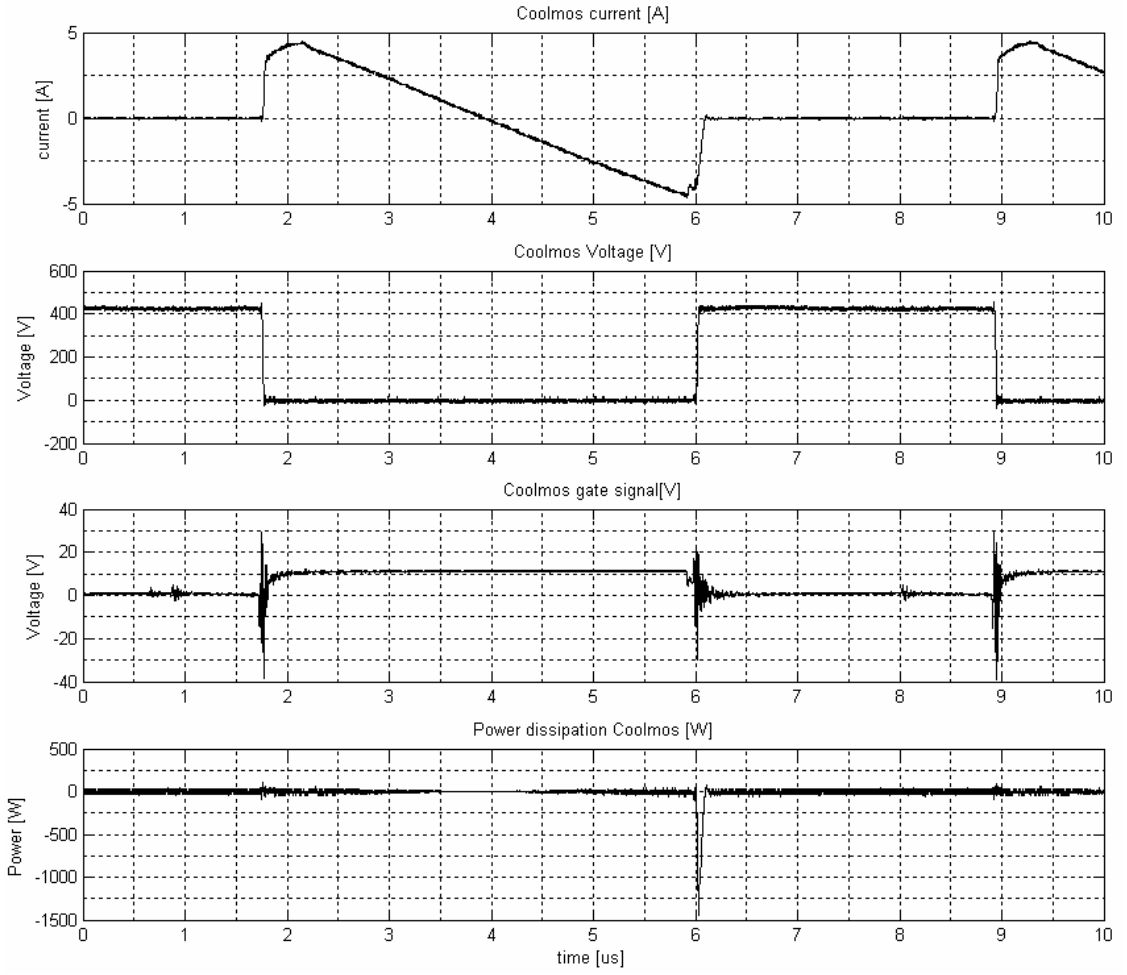

Figure 3.4. Measured coolmos switching waveforms vs. time, (V_{DC}=430V, IL=1A, V_{out}=200V, f_{out}=5 kHz, f_{switch}=140 kHz and no load).

3.2.2. Classification of the Converter

Even though the load is a parallel L-C bank with ohmic losses, after examining the switching algorithm and the full bridge converter waveforms, it can be said that this converter is not a resonance converter.

On the other hand it is using the inner body diode and the active channel freewheeling method to obtain soft switching. Therefore the converter can be classified as a zero voltage soft switched PWM converter.

3.2.3. The Effect of the Duty Cycle on the Switching Losses

In this experiment, the switching of the power supply is analyzed at different duty cycles. This is done by changing the output voltage level. This of course led to a change on the current drawn from the load, which is expected to be an effect on the switching losses.

In Figure 3.5, the effect of the current drawn on the switching losses can be seen. The measurements for this effect on the switching losses are synchronised by having the instances where the main output voltage is at the peak, therefore the voltage difference between the DC side and AC output is smallest. In these instances the current has the smallest ripple according to the basic inductance equations for the transient and steady state given in (3.1) and (3.2).

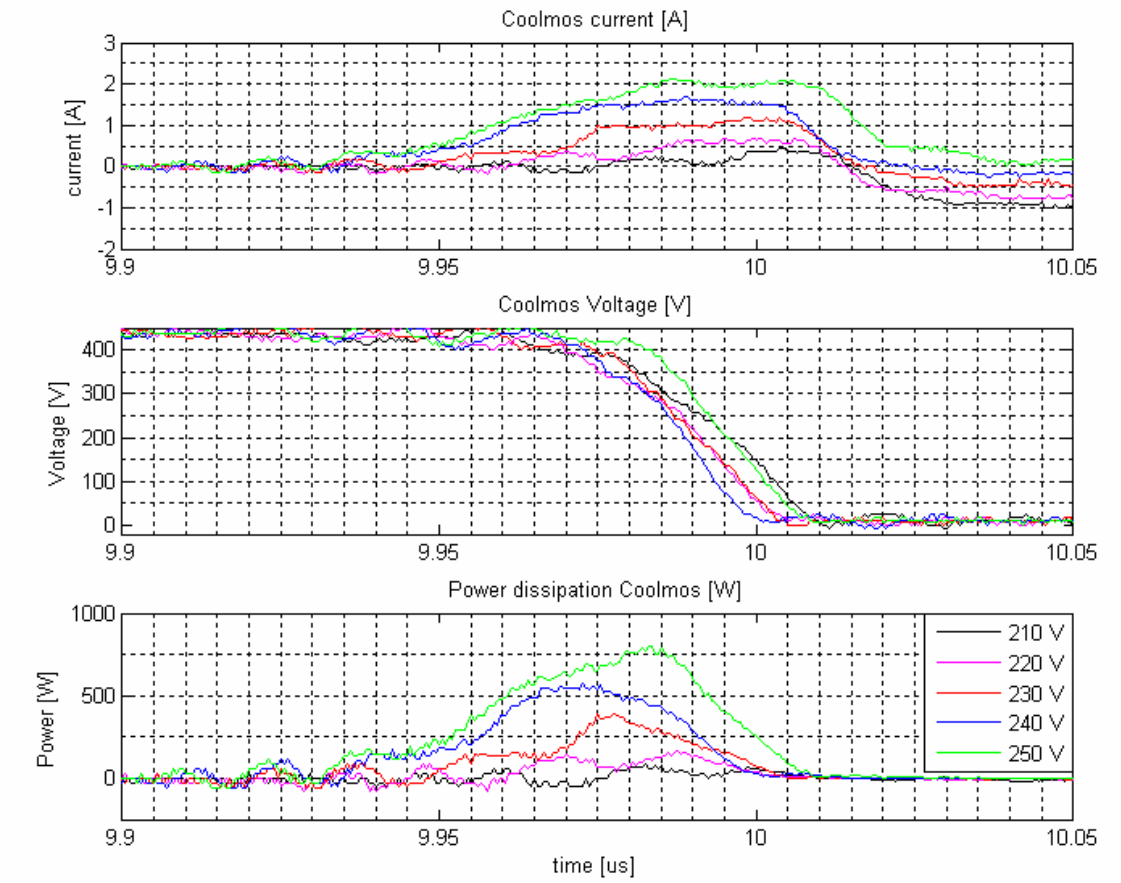

Figure 3.5. Effect of output current on turn on losses, (V_{DC}=430V, f_{out}=8 kHz, f_{switch}=140 kHz and 200W load),

3.2.4. The Effect of the Switching Frequency on the Switching Losses

In Figure 3.6 the effect of the switching frequency on the switching losses is given.

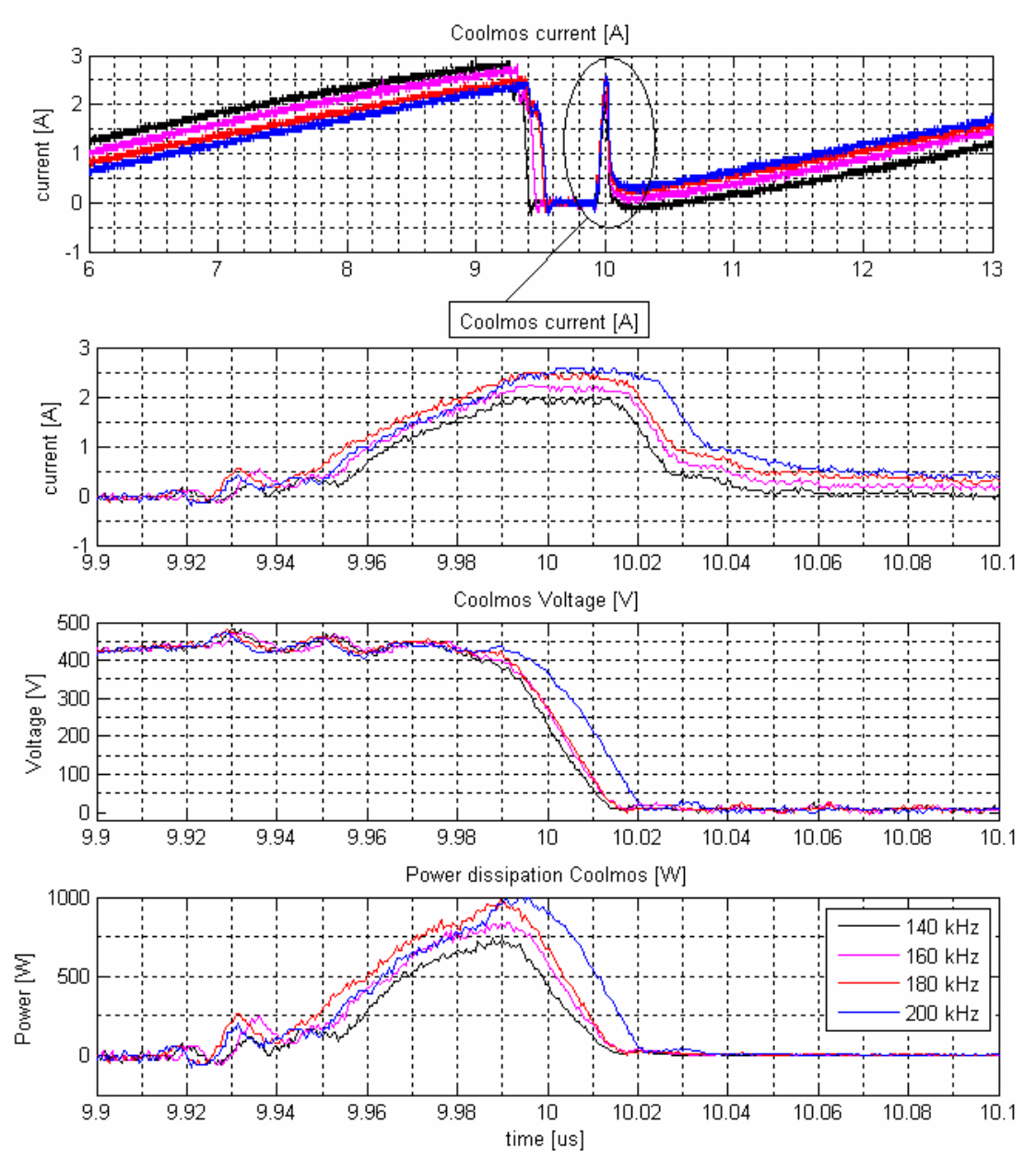

Figure 3.6. Effect of switching frequency on turn on losses, (V_{DC}=430V, V_{out}=220V, f_{out}=8 kHz and 200W load),

Once again the measurements for the effect of the switching frequency on the switching losses are synchronised by having the instances where the main output voltage is at the peak because of the reason mentioned earlier.

Considering that the ripple current gets lower when the switching frequency gets higher, and the current at the output of the full bridge is a perfect sinusoidal wave plus the ripple current, it is normal that the current does not cross zero at high loads and/or at high switching frequencies.

If the switching frequency is fixed, there is a trade off between the frequency and the magnitude of the output ripple, and the switching losses.

3.2.5. The Effect of the Output Frequency on the Switching Losses

Also an investigation of the switching losses dependency on the output main frequency is done. Keeping the load and the switching frequency constant, the main frequency of the output is changed. The results are given below in Figure 3.7.

As it is seen in Figure 3.7, there is not an effect from the output frequency on the turn on losses except for the losses that occur at 11.5 kHz output frequency. Since it is not an effect that can be generalized for the whole range of frequency change, it is decided not to include the effect.

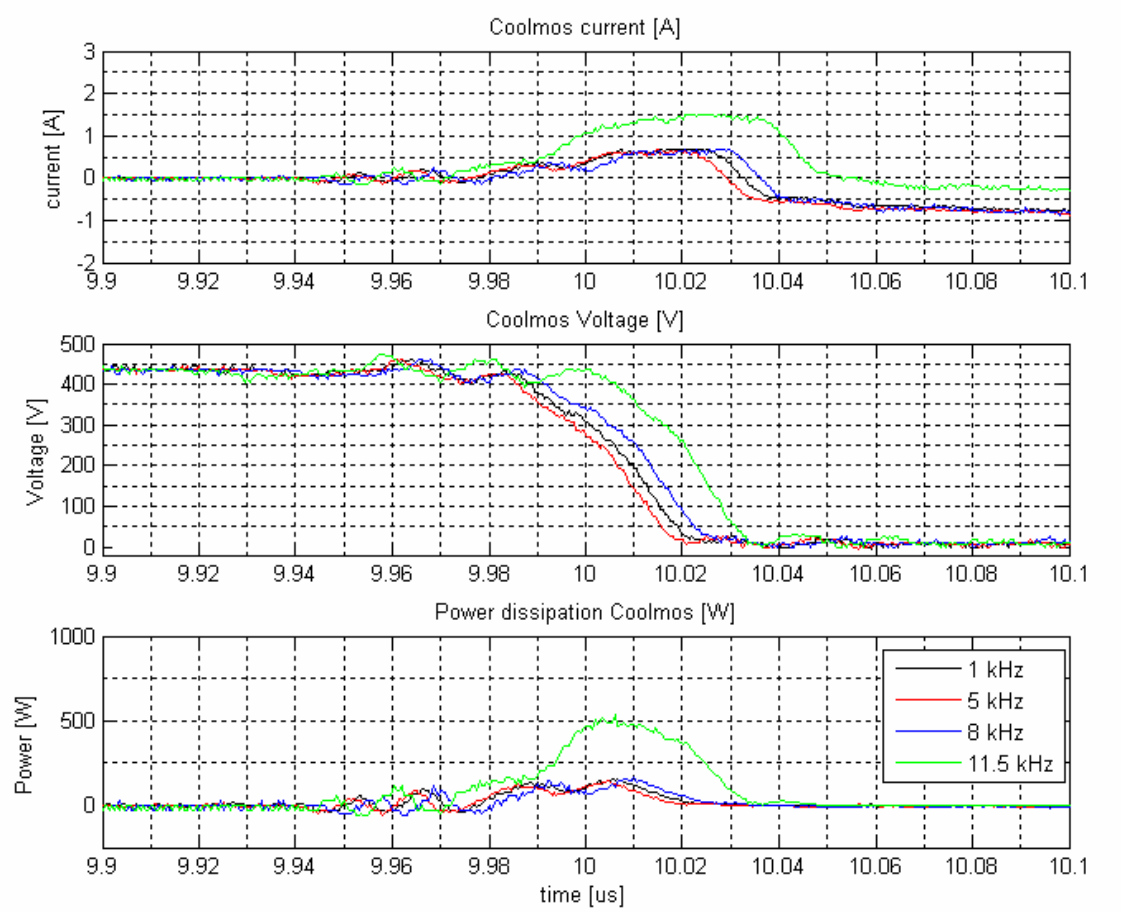

Figure 3.7. Effect of output frequency on switching losses, (V_{DC}=430V, V_{out}=220V, f_{switch}=140 kHz and 200W load),

3.3. Conclusion of the Experiments

After the measurements, it is seen that the switching losses depends on mainly the output current level (output voltage and load) and the switching frequency. Moreover no effect of the output frequency on the switching losses can be observed.

In balanced duty cycles around 0.5, where the load is supplied half of the period by positive and half of the period by negative voltage during the switching period, the magnitude of the ripple on the positive and the negative part are close to each other. Therefore there is a better margin for zero crossing of the current. This decreases the switching losses. If RMS of the main load current gets higher, it means that there would be an imbalance in duty cycles for the positive and the negative portion. If the load draws

higher current, the ripple of the current gets lower for the peaks of the output voltage. After a point the soft turn on switching would be lost.

Nevertheless duty cycle is controlled with respect to the output voltage. Also the output voltage is controlled due to the needs of the load. Therefore there is no room for optimization of output voltage level other than the limitations.

On the other hand the switching frequency can be set to optimize the trade off between the THD and losses. The high switching frequency is appropriate for improvement of THD and EMC. Nevertheless high switching frequency causes smaller ripples and the margin for zero crossing of the current is decreased. On the other hand low switching frequency gives better margin for the zero crossings of the current, but the THD of the output will be higher due to the fact that the low pass filter cuts more harmonic content as the frequency gets higher.

Therefore the VSF algorithm is proposed, in order to ensure zero crossings of the current when the margin for zero crossing is small and to ensure a reasonable THD when the margin for zero crossing is big.

4. The VSF Algorithm

As mentioned in Section 3 of this thesis report, the turn on losses depend on whether the current changes direction before each switching occurs. Since the output filter with the load behaves inductively, as seen from full bridge, the change in the current depends on the voltage applied to the filter, the characteristic inductance of the load and the period of the time that the voltage is applied.

The inductive behaviour depends on the output filter elements and the load. Therefore it cannot be controlled. On the other hand the voltage applied can be controlled but it is controlled due to the needs for the load, and not to assure the zero crossings. Therefore the only variable that can be manipulated is the period of time voltage applied by keeping the duty ratios as required by the load, in other words the switching frequency of the full bridge.

In this section, variable switching frequency (VSF) algorithm is proposed as a solution for the reduction of the turn on losses, especially at high loads. The algorithm and how it is implemented are explained.

4.1. The VSF

If the basic equation for inductance is considered for the power supply, the following results can be observed.

$$V_L(t) = L\frac{di(t)}{dt} \tag{4.1}$$

$$V_{DC}(t) - V_{FBout}(t) = L_{char}\frac{di_{FBout}(t)}{dt} \tag{4.2}$$

Assuming the output voltage to the load is a perfect sinusoidal,

$$V_{DC} - V_{RMS,FBout}\sqrt{2}\sin(2\pi ft) = L_{char}\frac{di_{FBout}(t)}{dt} \tag{4.3}$$

Where, V_{DC} is the DC voltage applied to the full bridge, $V_{FB,out}(t)$ is the output voltage of the full bridge, f is the frequency of the output voltage to the load and $i_{FB,out}(t)$ is the output current drawn from the full bridge.

To ensure a zero crossing in every switching, the peak to peak ripple of the current drawn must be at least two times of the average output current over a switching, which leads to,

$$V_L(t) = L\frac{\Delta i(t)}{\Delta t} \tag{4.4}$$

$$\Delta t = L\frac{\Delta i(t)}{V_L(t)} \tag{4.5}$$

$$\max(f) = \frac{V_L(t)}{L\Delta i(t)} = \frac{V_{DC} - abs(V_{out}(t))}{L_{char}\,2abs(i_{out}(t))} \tag{4.6}$$

Employing (4.4) to (4.6) in Matlab, the minimum switching frequencies needed in order to assure zero crossing for a period is calculated. The results are given below in Figure 4.1.

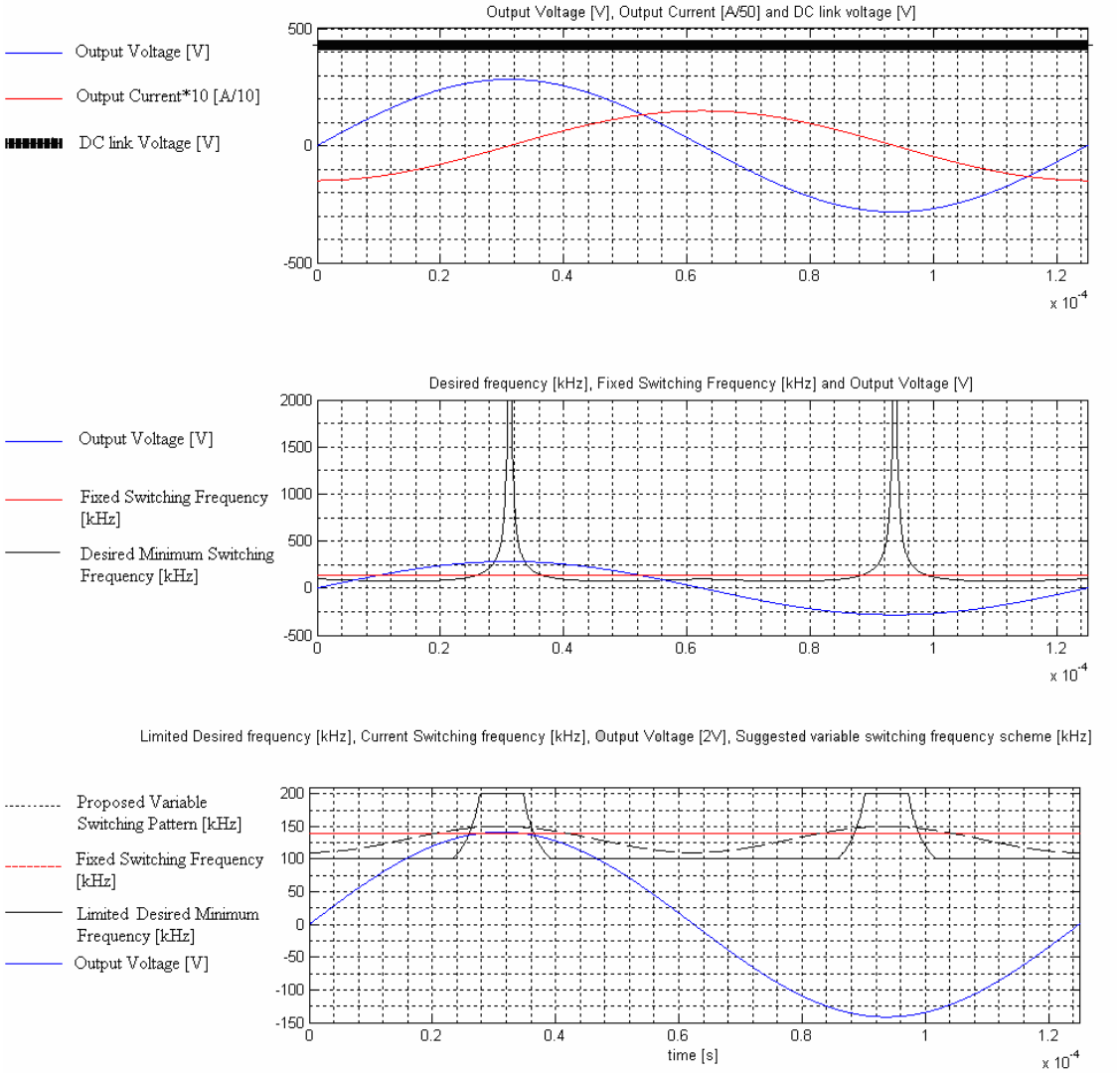

Figure 4.1. Calculation of the desired minimum switching frequency and proposed VSF algorithm, [Output frequency=8 kHz, Output load=19 Ω , Output voltage=200VAC]

In the first subplot of Figure 4.1, the estimated DC link voltage, the output voltage and the output current are given. As it is seen here and stated before, the load seen from the full bridge is considered to be a pure inductive load, L_{char}=0.145mH, whereas the main load is purely resistive R=19 Ω. Therefore the estimated current follows the output voltage by $\pi/2$ radians lagging.

Applying the minimum frequency formula stated before in (4.6), the maximum frequency needed is calculated and given in subplot 2 together with the fixed switching frequency.

Here the most important thing to observe is that the peaks of the maximum switching frequency are observed when the current is around zero. It is natural that the frequency can be higher (theoretically infinite) when the main component of the current is crossing zero. Also another thing that can be observed is that, when the main current is around its negative and positive peaks, the frequency should be decreased in order to assure the zero crossings.

Since there are limitations due to the switching losses and EMI regulations, the maximum frequency should be limited. Also considering the quality, the THD, of the output voltage and the efficiency of the output filter, the minimum frequency should be limited as well. On the third subplot of the Figure 4.1, the limitations are implemented. This waveform is the basic of the algorithm, that is implemented for VSF. For the first time implementation, instead of implementing a complex algorithm a sinusoidal change with a negative offset is proposed. The proposed change is given in subplot 3 of Figure 4.1 as well.

4.2. Implementation of the VSF Algorithm

The Power Supply DSP has a built in PWM interrupt with two main input variables the Duty Cycle and the Switching Period for each switching period. The comparator increases with CPU clock period, 1/150MHz, and creates output signal every switching period $(x \rightarrow lPWMDuty)$ with duration of duty cycle $(x \rightarrow uiTable[i])$. The creation and computation of the duty cycles, based on the sub oscillation method [17], is given in Figure 4.2 and (4.7).

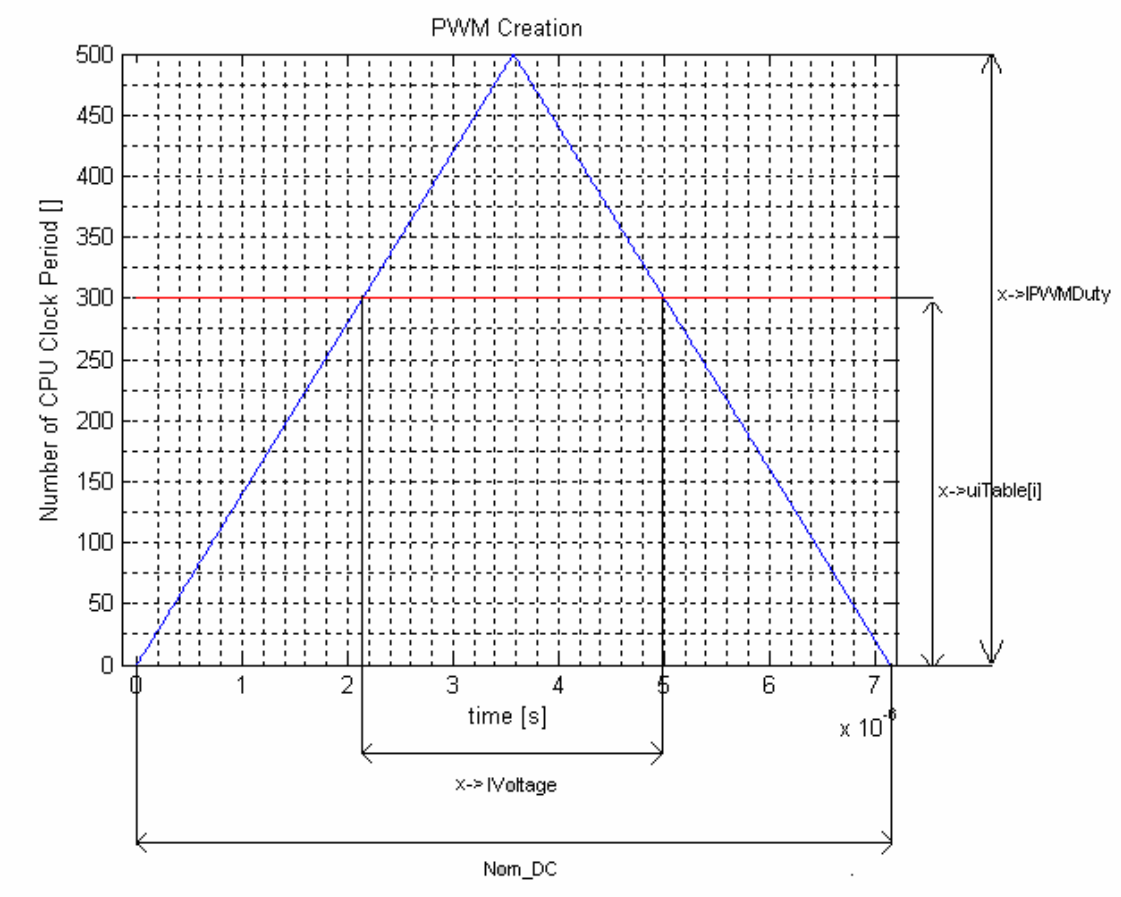

Figure 4.2. Creation of the PWM,

$$U = \frac{\sqrt{2}(x \to lVoltage)(x \to lPWMDuty)}{Nom\_DC} \tag{4.7}$$

Here $(x \to lPWMDuty)$ is the number of CPU Clocks for each switching period. *Nom_DC* is the nominal DC voltage, in our case nominal DC voltage is 430V. $(x \to lVoltage)$ is the reference voltage for the output.

Since the fixed switching frequency (FSF), which is around 140 kHz, is much higher than the output frequency, which is 4 kHz, the reference voltage for each switching cycle is modulated by the sinusoidal of the main as shown in Figure 4.3 and computed in (4.8).

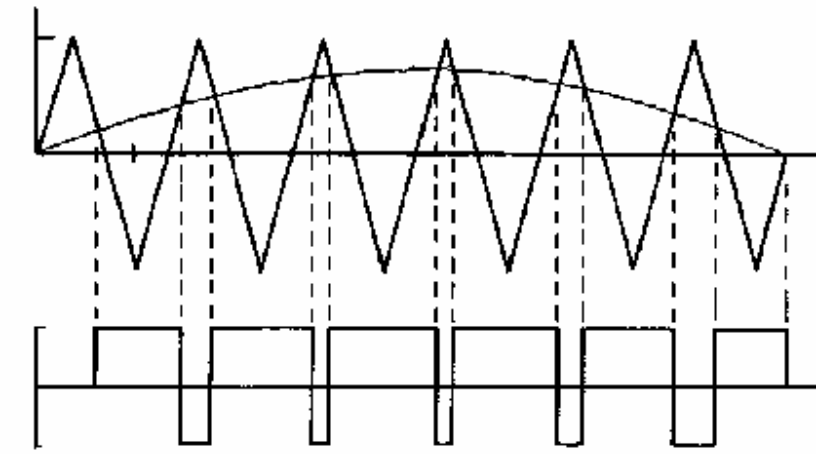

Figure 4.3. Creation of the PWM,

$$for \quad i = 0:1:x \rightarrow lSize$$

$$x \rightarrow uiTable[i] = \frac{U}{2}\sin(\frac{(2i-1)\pi}{x \rightarrow lSize}) \tag{4.8}$$

Here $(x \rightarrow lSize)$ is the number of the switching per output period, i replaces t in the discreet domain and U is the changing amplitude of the reference. Also $(x \rightarrow uiTable[i])$ is the table that has the number of CPU Clocks for the duty cycle of each switching period.

It must be observed that the information for the switching period, $(x \rightarrow lPWMDuty)$, is normally set as a constant as explained above. The proposed algorithm decreases the switching frequency, $(x \rightarrow lPWMDuty)$, with an offset in order to be within the limits of the maximum and the minimum frequency. Also this reduced switching frequency oscillates as a co sinusoidal with amplitude that is set as a parameter, which creates the VSF algorithm as explained before.

The oscillating cosines' frequency is chosen to be twice as fast as the output frequency. It is because the maximum peak switching frequency must occur twice in one output period, when the current crosses zero. Also the minimum peak switching frequency must occur twice in an output period, when the output voltage has its positive and negative peaks. This is to assure zero crossings in the problem phases seen in Figure 4.4 below. Therefore the $(x \rightarrow lPWMDuty)$ is changed to a frequency table and the duty cycle table is modified using this frequency table. Below the algorithms will be presented in (4.10)

and (4.11). Here $(x \to uiTableD[i])$ is the frequency table for one output period. A is the magnitude of the output frequency change, amplitude of the superimposed cosine function.

$$for \quad i = 0:1:x \to lSize$$

$$x \to uiTableD[i] = x \to lPWMDuty + A * \cos(\frac{(4i-1)*\pi}{x \to lSize})$$

$$U[i] = \frac{x \to lVoltage * \sqrt{2} * x \to uiTableD[i]}{Nom\_DC} \tag{4.10}$$

$$for \quad i = 0:1:x \to lSize$$

$$x \to uiTable[i] = \frac{U[i]}{2} * \sin(\frac{(2i-1)*\pi}{x \to lSize}) \tag{4.11}$$

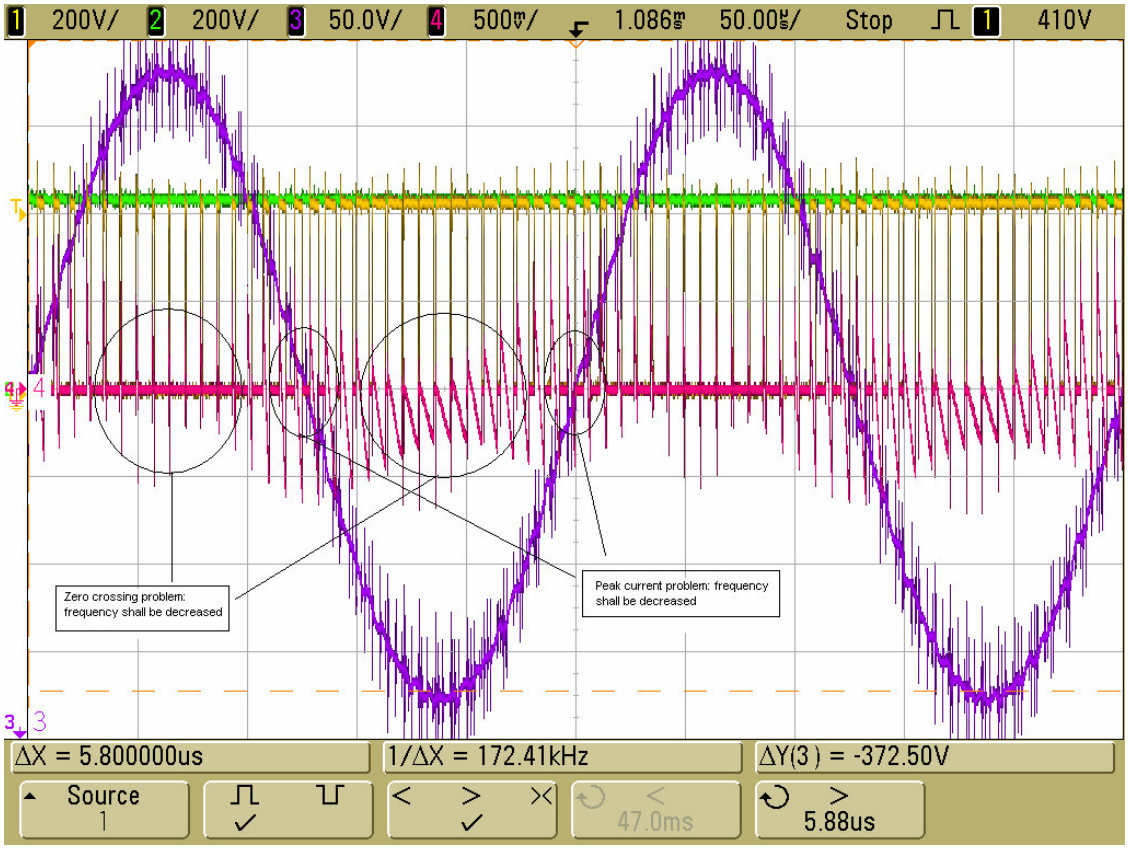

Figure 4.4. Problematic phases on which the VSF optimisation is needed to be implemented,

After implementing the VSF algorithm, the information about the VSF parameters are read from the DSP memory. The results are given below in Figures 4.5 and 4.6.

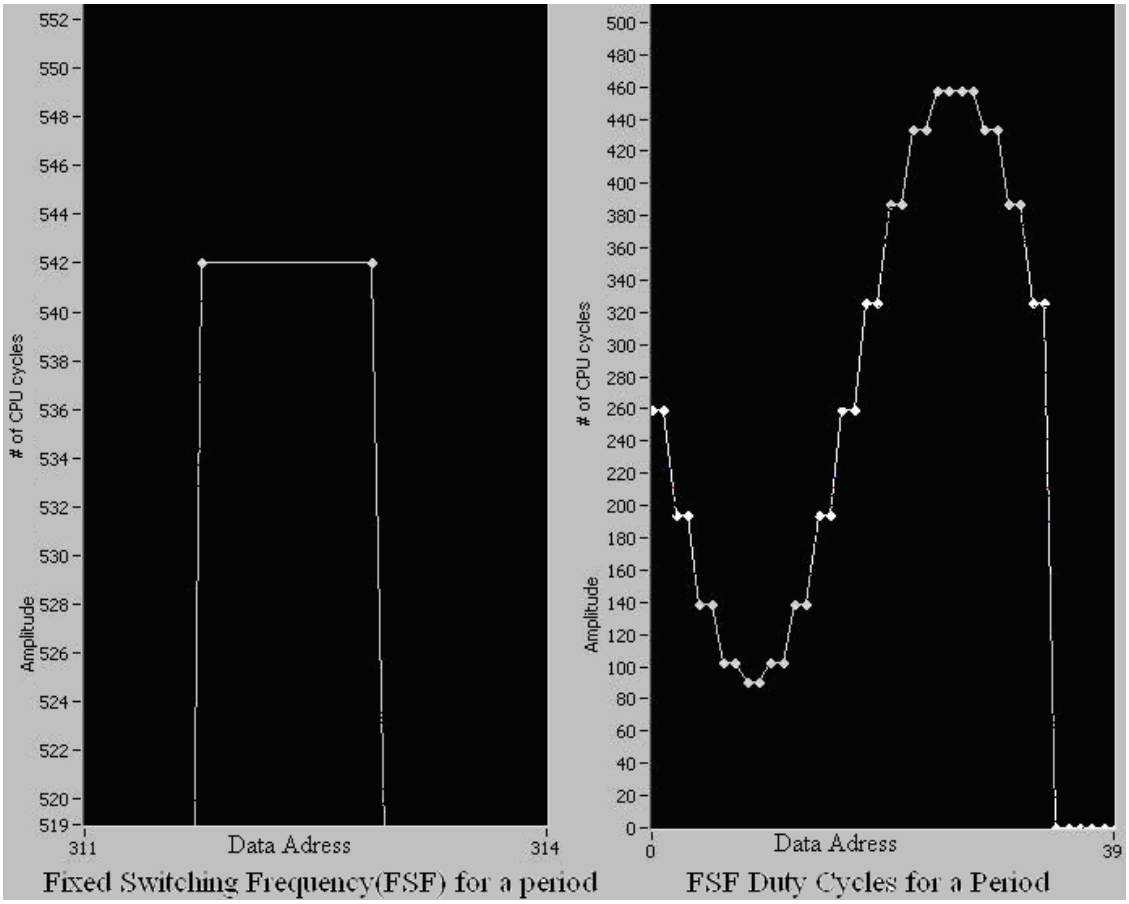

Figure 4.5. Content of parameters in DSP memory, related to PWM creation of the FSF Algorithm,

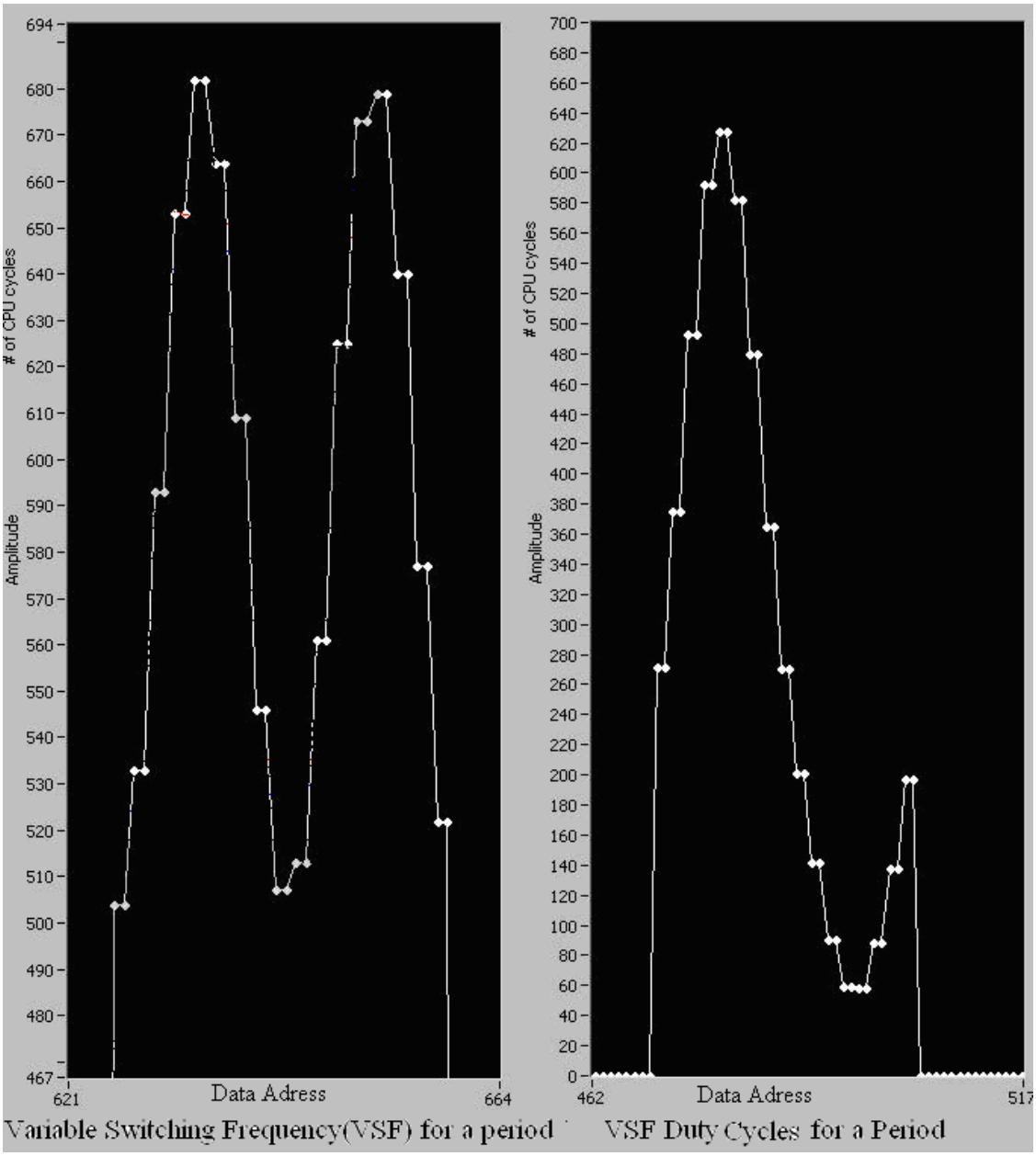

Figure 4.6. Content of the parameters in the DSP memory, related to the PWM creation of the VSF Algorithm,

Here it can be observed that, there is a difference between the peak switching frequency change in the negative and the positive half of the cosine. That's mainly because of the nonlinearity of the relation between switching frequency and the number of CPU cycles. (4.12) and (4.13) below show the relation between switching frequency and number of CPU cycles.

$$x \rightarrow uiTable[i] = \frac{CPU\_CLOCK}{Switching\_Frequency} \tag{4.12}$$

$$Switching\_Frequency = \frac{CPU\_CLOCK}{x \rightarrow uiTable[i]} \tag{4.13}$$

Here the variable that needs to be controlled is the *Switching Frequency* and it depends nonlinearly on $(x \rightarrow uiTable[i])$, which is the VSF parameter input. Nevertheless this won't create a problem; on the contrary the frequency content will be even more distributed. For later software changes, if needed, a more complex algorithm can be suggested to change that.

5. Results of the Measurements on the VSF Algorithm

5.1. Comparison of the switching algorithms

In this section, the measurement results from two different switching algorithms, FSF and VSF, are processed and compared in aspects of focus. The operating point is 130 VAC output voltages at 4 kHz frequency and the load is a 200W 230VAC light bulb which has a 19 Ω resistance. The oscilloscope outputs for two periods are shown below in Figure 5.1 and 5.2.

Here in the figures the magenta wave is the output voltage, the pink wave is the current from an upper switch on the full bridge inverter, the yellow wave is the source voltage of the respective switch and the green is the drain voltage of the respective switch.

If the figures are compared, it is seen that the zero crossings using the VSF algorithm are more assured. Also the distortion in the output voltage on the peaks are more frequent using the VSF algorithm, due to the decreased switching frequency which can be compensated for by modifying the output filter as a follow up work.

Because of the distribution of the switching frequency and the output voltage harmonic content, the EMI is expected to decrease according to Domingos S. L. et. al [3].

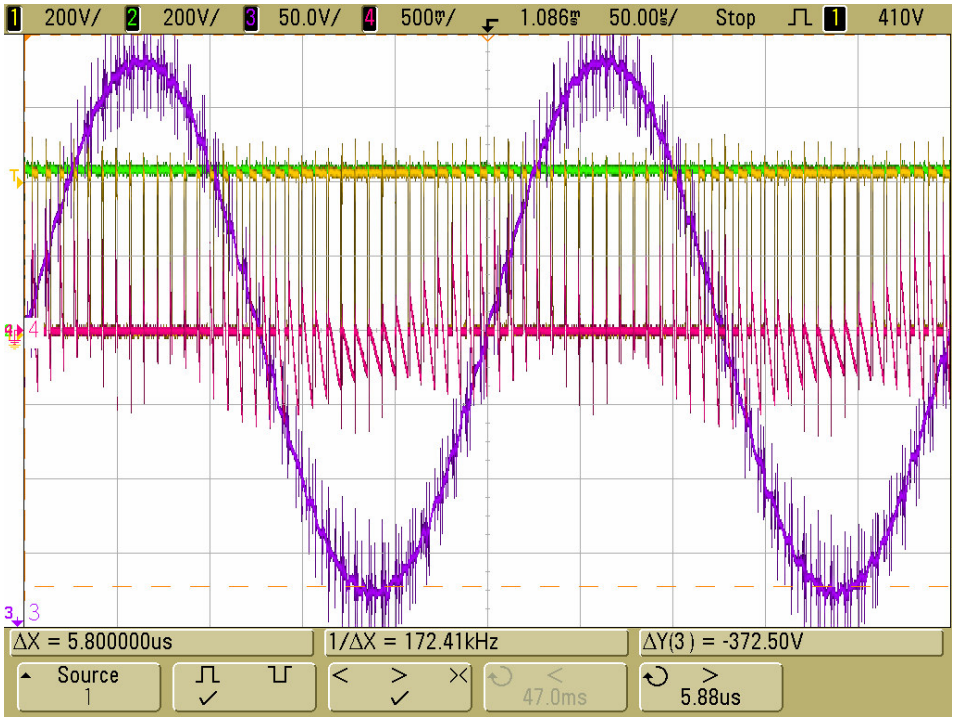

Figure 5.1. Oscilloscope outputs for FSF,

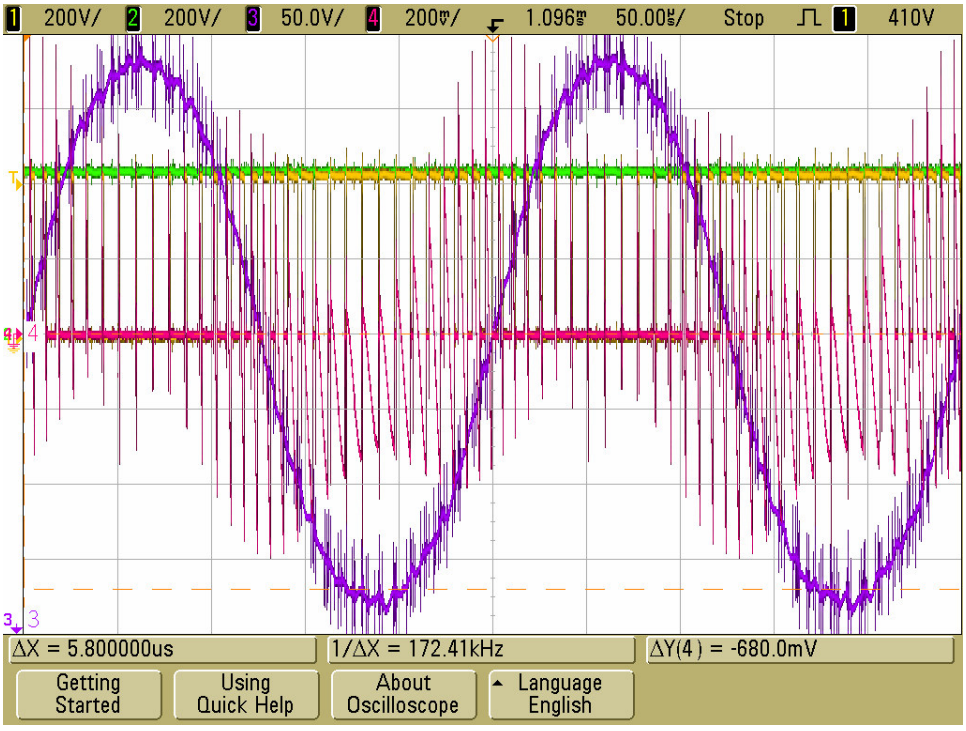

Figure 5.2. Oscilloscope outputs for VSF,

The comparison of the two algorithms at the turn on, which is the main focus of this work, is given below in Figure 5.3. Here it is clearly seen that the peak reverse current which is the main reason for turn on losses is lower if the VSF method is used. This results in decreased peak turn on power loss and total turn on power loss per switching. This will decrease the stress on the component when VSF is used. The output voltage is given to compare the operating points, which are the same in both algorithms' measurements, the lower peak of output voltage. Also the oscillations seem to be damped better with VSF.

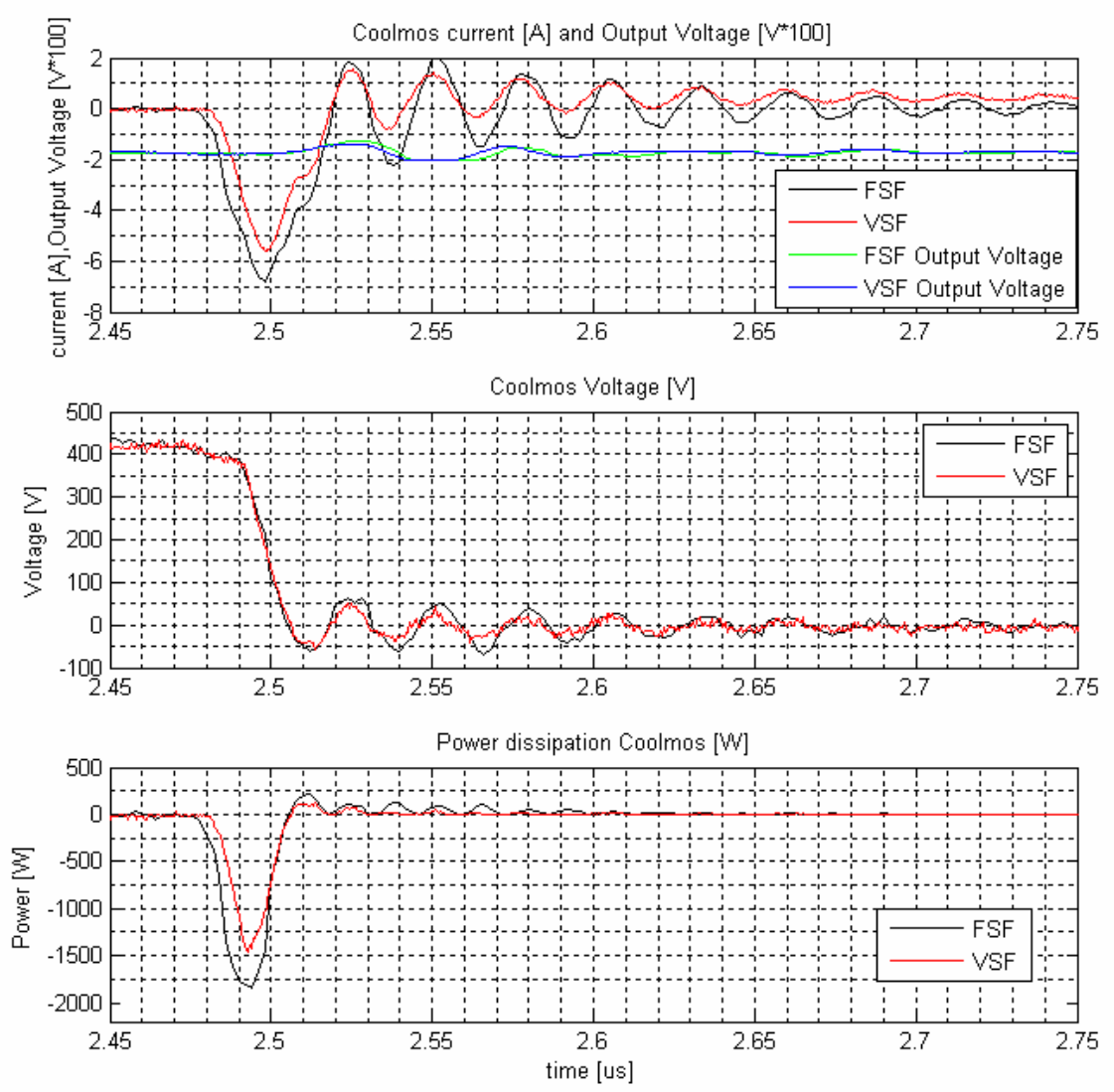

Figure 5.3. The comparison of turn on for FSF and VSF,

When it comes to numbers; the turn on loss per switching at the same operating point, where the highest turn-on loss occurs in the period, is 34.8 μWs with the FSF algorithm, whereas it is 21.0 μWs with the VSF. This means that either the rating of the equipment can be decreased or the life time of the equipment would be increased at the same operating conditions by using the VSF.

If a period of output voltage is taken into consideration, following Figure 5.4 is observed.

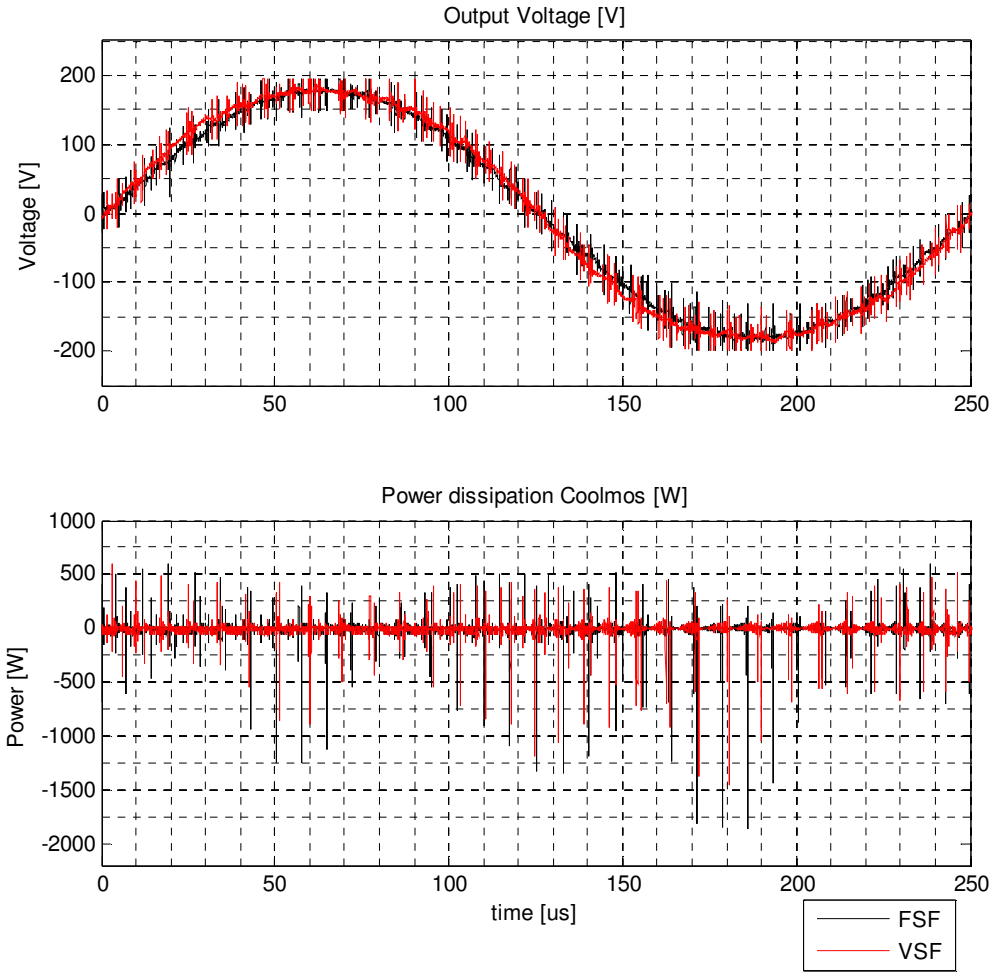

Figure 5.4: The comparison of switching losses with FSF and VSF for an output period,

In this figure it is observed that the peaks of the current drawn are lower, when the VSF algorithm is used, than when the FSF algorithm is used. This occurs even though the voltage level of the FSF is slightly higher. This will again end up with lower stress and

losses in the component. If the switching losses for a whole period are considered, it is seen that with the FSF method the losses are 4.3 mWs and with the VSF method the losses are 4.0 mWs.

The frequency content of the output voltage of the full bridge is given below in Figure 5.5.

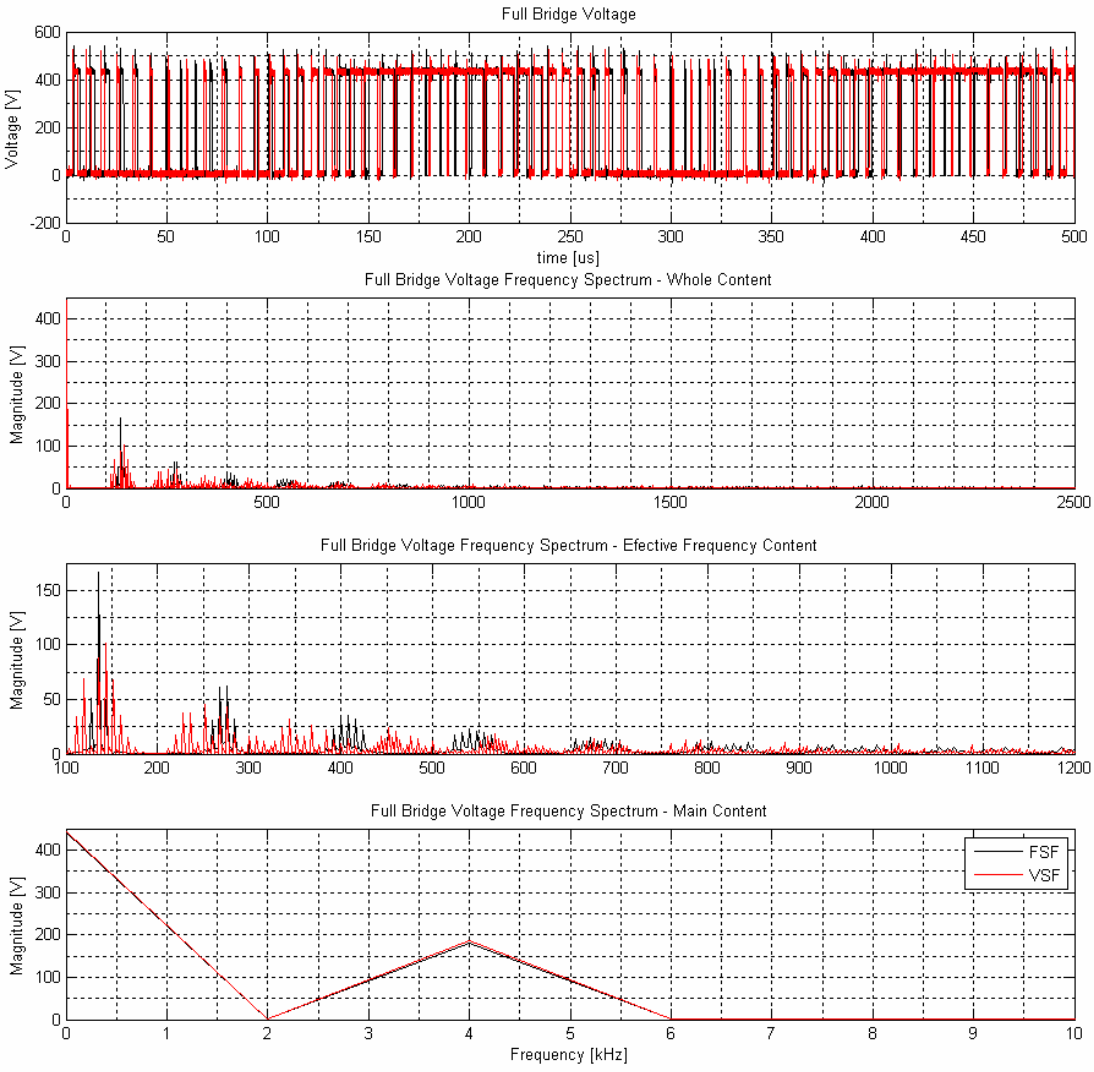

Figure 5.5: Frequency content of the fullbridge output voltage,

If the frequency content of the full bridge output voltage is analysed, it is seen that the frequency content around the multiples of switching frequency is decreased using the VFS method. Instead of having higher peaks at certain frequencies, the content of the

voltage that causes distortion is distributed. This would reduce EM noises caused by the power supply and make it easier to fit the EMI regulations.

It is also clearly seen in subplot 3 of Figure 5.5 that the main component is at 4 kHz, around 180V, which is the magnitude of the output voltage. Next it is observed that, the main component of the output voltage when the VSF algorithm is applied is slightly higher than the main component of the output voltage when the FSF algorithm is applied. Nevertheless the peaks of the harmonic content of the output voltage when the VSF algorithm is applied are lower than the ones when the FSF algorithm is applied.

5.2. Conclusion for the VSF Algorithm

It is clearly observed that with the VSF algorithm, the peak reverse current in the Coolmos on turn-ons can be decreased. This leads to a decrease at the turn on losses, especially at high loads.

This would result in several benefits such as;

-To decrease the rating of the Coolmos and related equipments,
-Capability to increase the output current, which would lead to increased output power at the same output voltage,
-Increasing the life time of the components by keeping the output power and components the same
-Match the EMI regulations better by distributing frequency content of the switching

6. Output Filter Inductor Optimisation

Another significant cause for the losses in the power supply is believed to be the output filter inductor, L800, seen in Figure 6.1. After changing from hard switching to soft switching, this inductor has been re-designed to increase the power output. This was done by increasing the diameter of the winding wire in order to carry more current.

After the re-design, it was observed that the inductor is getting hotter than its normal operating temperature. This has been occurring especially at the high current and frequency levels. Since the operating voltage band has not been changed and the temperature increase becomes significant at the high current and the high frequency levels, this temperature increase is believed to be caused by winding losses.

In this section of the thesis work, the design of the old output filter inductor has been analysed. Theoretical calculations have been compared with experimental results. A new design for the old inductor has been implemented. Finally, theoretical and experimental results for the old and the new designs have been compared.

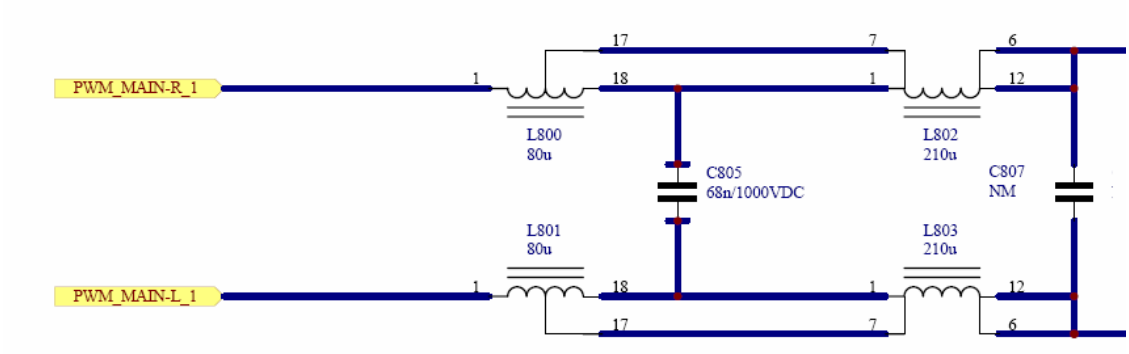

Figure 6.1: Low pass filter part of the Output stage of power supply,

6.1. Analysis of the Design of the Output Filter Inductor before Optimisation (OFIBO)

6.1.1. Design of the OFIBO

The inductor, L 800, is designed to be an 80 uH inductor. It has three main parts, which

are the core, the winding and the coil former.

The core of the inductor stores the recoverable energy by creating a medium to contain magnetic flux [12]. L800 core is constructed of two E-type, ungapped ferrite cores. The geometry of the core and the picture of the OFIBO are given in Figure 6.2. The supplier Siemens Matsushita also provides the following magnetic characteristics in Table 6.1 for a couple of cores;

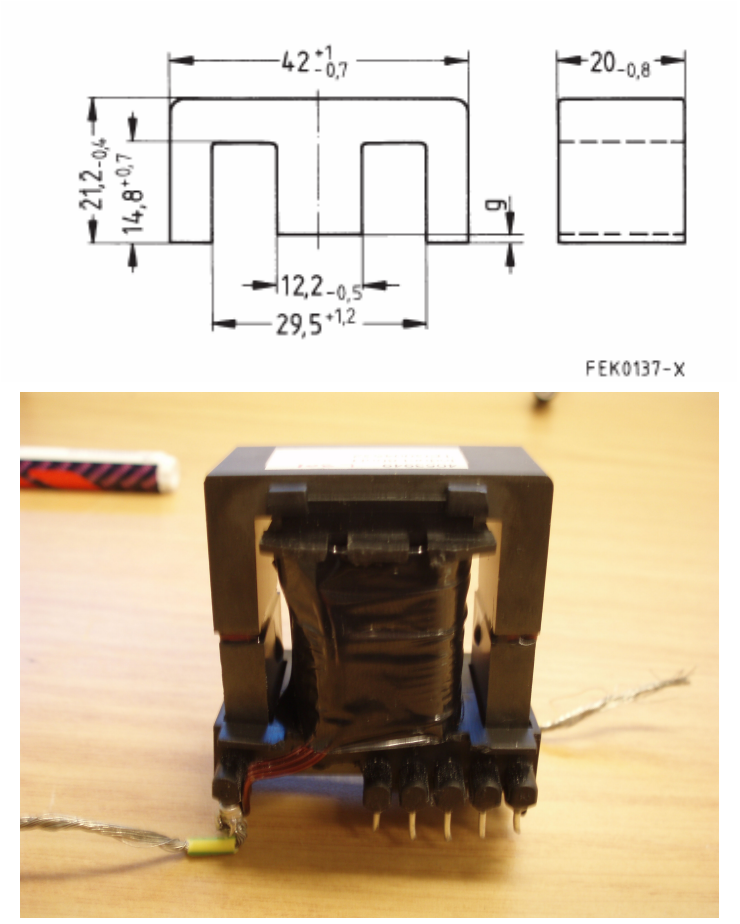

Figure 6.2. The geometry of the coreE/42/21/20, and inductor L800

The winding of the inductor is a bundle of wires that carries the current which creates the magnetic field that causes the magnetic flux in the core. These wires are also the mechanical connection to the circuit. L800 inductor is winded 20.5 turns with three parallel strand of round copper wire with 0.8 mm diameter.

Table 6.1. Magnetic characteristics of the core,

$\sum I / A = 0.41 mm^{-1}$
$A_e = 234 mm^2$
$A_{\min} = 239 mm^2$
$V_e = 22700 mm^3$
$I_e = 97 mm$

The coil former is the part that holds the winding and the cores. Also it creates the air gap needed. The coil former is the mechanical connection with the PCB board of the power supply and its geometry is given below in Figure 6.3.

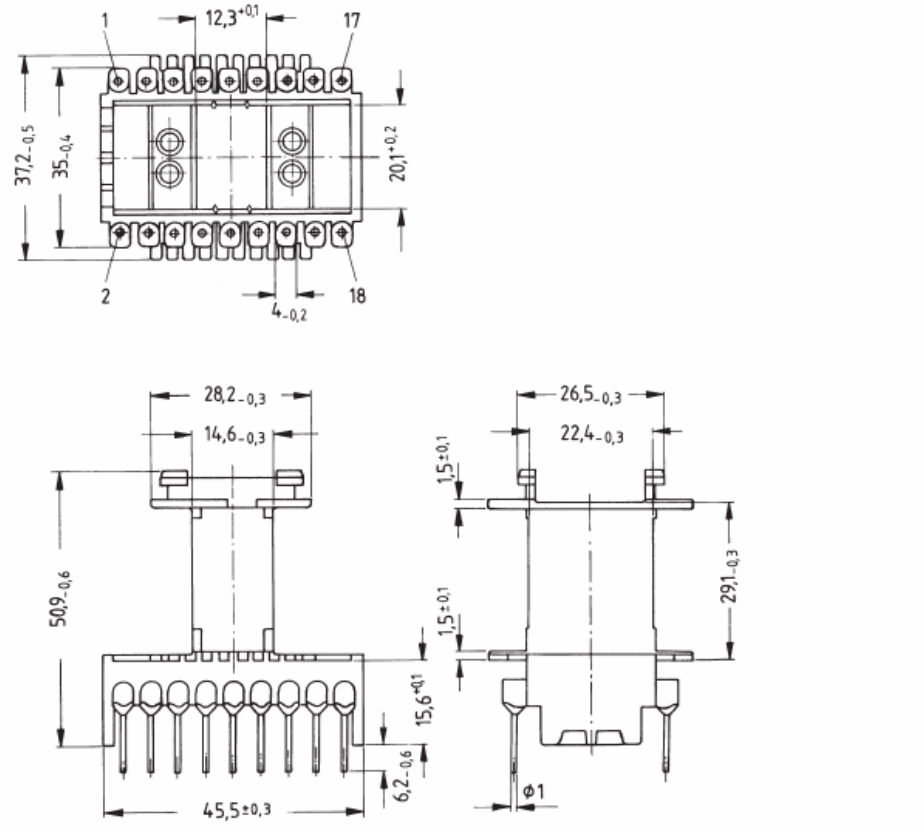

Figure 6.3. Coil former of the inductor,

The air gap of the inductor is approximately 1mm. If the linear case is taken into account, in a closed flux path, Ampere's law states that the magneto motive force (mmf) is

$$mmf = NI = \oint H(r)dl \tag{6.1}$$

In the inductor case, the flux passes the air gap; therefore it is possible to separate the magneto motive force terms into a core term and an air gap term,

$$mmf = NI = H_c l_c + H_a l_a \tag{6.2}$$

where N is the number of turns, I is the current flowing through the winding, H is the magnetic field intensity, l is the length of the flux path. The underscores, c and a, refer to the core and the air gap respectively. The relation between H and B, magnetic flux density and magnetic field intensity states that;

$$B(r) = \mu H(r) \tag{6.3}$$

where μ is the permeability. If this relation is employed in mmf equation;

$$mmf = NI = \frac{B}{\mu_c \mu_0} l_c + \frac{B}{\mu_0} l_a \tag{6.4}$$

where μ_0 is the permeability of the air and μ_c is the permeability of the core. Since μ_c is much bigger than μ_0, the first term, which refers to the magneto motive force in the core, will be insignificant. Therefore the first term on the right side of the (6.4) can be neglected. Then the mmf becomes

$$mmf = NI = \frac{B}{\mu_0} l_a \tag{6.5}$$

Combining (6.5) with the relation between B and H, the following expressions can be found;

$$H = \frac{NI}{l_a} \tag{6.6}$$

$$B = \frac{NI\mu_0}{l_a} \tag{6.7}$$

The energy stored in the inductor can be stated in two forms;

$$W = \frac{1}{2}\int_V BHdV = \frac{1}{2}BHAl_g \tag{6.8}$$

$$W = \frac{1}{2}LI^2 \tag{6.9}$$

where *V* is the volume of the effective mmf term, A is the area of the path where flux flows in the air gap, L is the inductance and W is the energy of the inductor. Finally if *B* and *H* terms are replaced and the (6.8) and (6.9) are solved for L, it is found;

$$L = \frac{N^2 A\mu_0}{l_g} \tag{6.10}$$

It is seen that the inductance depends on the number of turns and air gap size, in linear occasion. If the *L* is calculated for L800 case, it is seen to be approximately around 80uH.

6.1.2. DC loss in the Winding

There is a DC loss in the winding caused by the resistance of the wire. DC resistance of a wire depends on several properties of the wire and the environment, such as the material type, the conducting area, the length and the temperature. In general form, the resistivity and the resistance of a copper wire as a function of the temperature can be given as [4];

$$\rho_{cu} = 1{,}724\left[1 + 0.0042(T - 20)\right]10^{-6} \tag{6.11}$$

$$R_{cu} = \rho_{cu}\, l_{cu} \big/ A_{cu} \tag{6.12}$$

where ρ_{cu} is the bulk resistivity of copper, T is the temperature in degrees, R_{cu} is the resistance of the copper wire, l_{cu} is the length of the copper wire and A_{cu} is the cross section of the copper wire.

Inserting parameters of the wire used in L800 R_{cu} is calculated as $0.0169\,\Omega$.

6.1.3. The Skin Effect and the Proximity Effect

Figure 6.4 shows a high frequency model of a single wire [5]. *A* represents the surface of the wire, *B* is the centre. L_x represents the inductance per unit length external to the wire (what would be measured inductance of the wire). L_i is the inductance distributed within the wire, from surface to the centre. R_i is the distributed longitudinal resistance from the surface to the centre. Collectively R_i is the dc resistance of the wire. All values given are per unit length of wire.

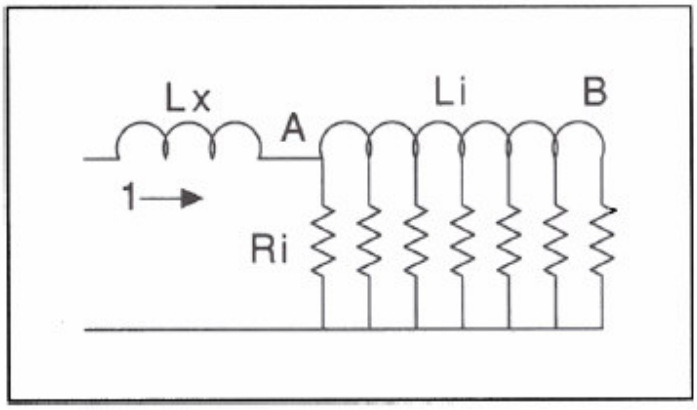

Figure 6.4. High frequency model of a single wire,

If the wire is analysed with respect to the circuit given above, it can be said that at high frequencies the resistance near the surface of the wire blocks the current to flow in the centre of the conductor. What physically happens is that, in the high frequencies the energy transfer to inductance L_i is significant with respect to Ri^2t. Then the current flow concentrates near the surface, even though the resistance is higher, in order to minimize energy transfer to L_i [5]. This causes an extra AC resistance for the wire, which is more significant at higher frequencies

Penetration depth (or skin depth), is defined as the distance from the conductor's surface to where current density (and the field, which terminates current flow) is 1/e times the surface current density [5].

$$D_{pen}=\sqrt{\frac{\rho_{cu}}{\pi\mu_0\mu_{cu}f}} \tag{6.13}$$

where ρ_{cu} is the bulk conductivity of the copper, μ_0 is the free magnetic air permeability, μ_{cu} is the relative permeability of copper and f is the frequency.

Also, when two conductors, thicker than D_{pen} are in proximity and carry opposing currents, the high frequency current components spread across the surfaces facing each other in order to minimize magnetic field energy transfer (minimizing inductance). This high frequency conduction pattern is shown in Figure 6.5.

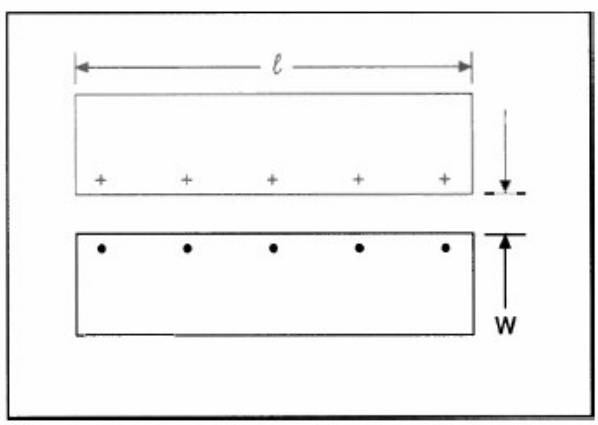

Figure 6.5. Proximity Effect,

To minimize inductance the current won't flow on any other surfaces, which will increase the AC resistance.

Several methods of calculating AC resistance have been published. One of them is published by Dowell [7]. The expression for the winding AC resistance given below in Equations 6.14 and 6.16 are determined by exploiting the one dimensional solution of the field in the winding space [7]. For a conductor with round cross sectional area;

$$A = \left(\frac{4}{\pi}\right)^{3/4} \frac{d^{3/2}}{Dpen * t^{1/2}} \tag{6.14}$$

$$R_{ac} = R_{dc} A \left[\frac{e^{2A} - e^{-2A} + 2\sin 2A}{e^{2A} - e^{-2A} - 2\cos 2A} + \frac{2}{3}(m^2 - 1) \frac{e^{2A} - e^{-2A} - 2\sin 2A}{e^{2A} + e^{-2A} + 2\cos 2A} \right] \tag{6.15}$$

where R_{dc} is DC winding resistance, m is number of layers in one winding portion, d is copper diameter of the conductor, t is distance between centres of two adjacent conductors and $Dpen$ is the skin depth.

It is assumed that the magnetic flux is parallel to winding layers, and this is not well satisfied for low values of d/t. The application of these expressions to solid round windings with high values of d/t (0.7<d/t<1) results in a good accuracy of R_{ac} [7]. In the inductor L800, it can be assumed $d=t$. On the other hand this expression cannot be used to represent the AC resistances of a bunched litz wire [7].

Another weakness of this expression is that the capacitive effect in the winding, which becomes significant in the higher frequencies, is ignored [7]. Therefore it can be expected that in the high frequencies the R_{ac} model may not match the experimental results.

After applying the equations for the frequency range between 1 kHz and 2 MHz at room temperature the results obtained are given in Figure 6.6.

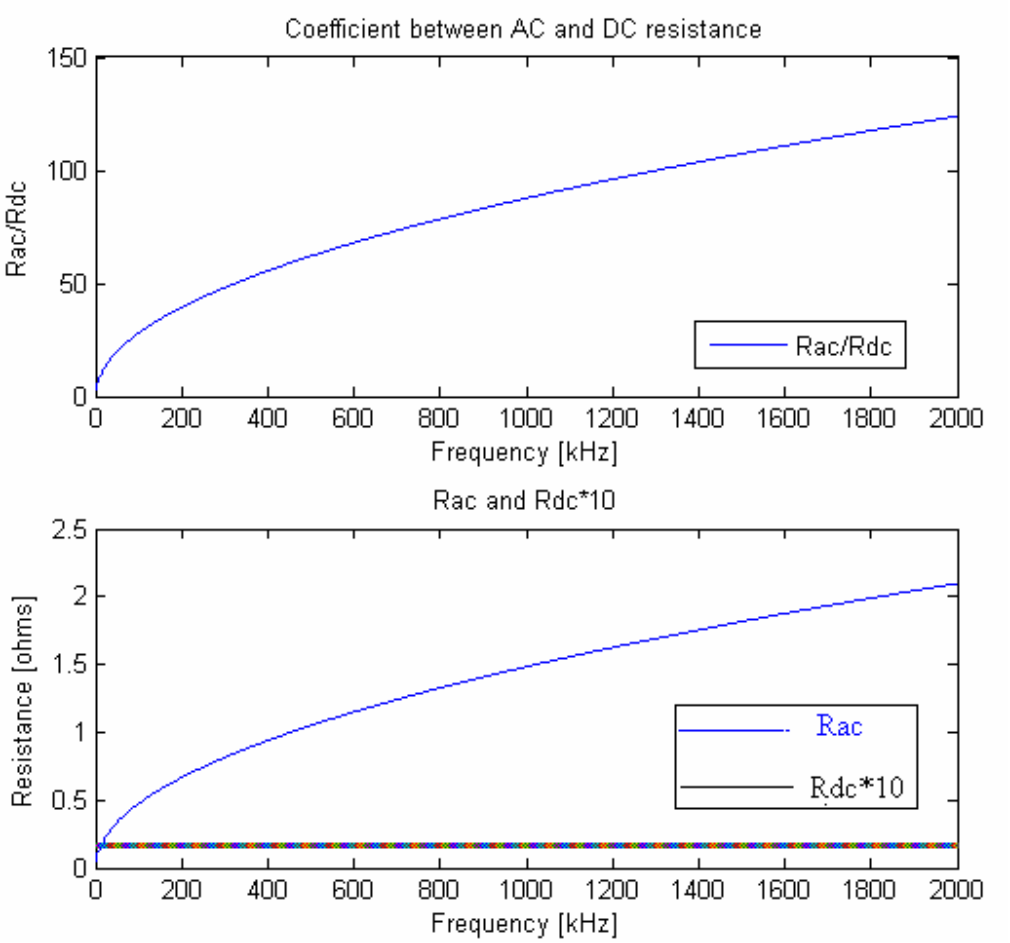

Figure 6.6. Rac and Rdc,

Here it is seen that the AC resistance can be over 30 times higher than the DC resistance around the switching frequency of the power supply, 140 kHz. This frequency range is important because, as it is seen in Figure 6.7, around the switching frequency, the frequency content of the inductor current is the same as the one in the main frequency. Therefore this will cause undesired losses.

The common coefficient between AC and DC resistance, taken into account by Texas Instruments at design is 1.7 [5]. This result briefly explains one of the reasons for why high losses may be because of the size of the conductor, theoretically. Therefore a practical measurement is proposed as a result of these calculations.

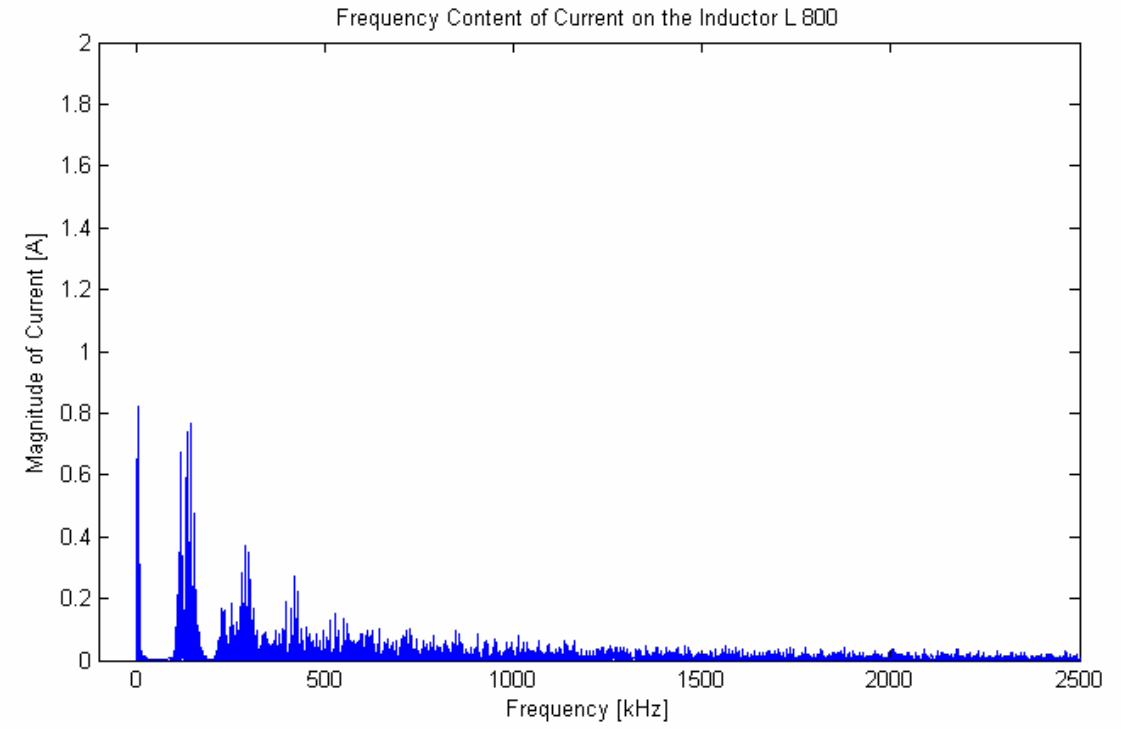

Figure 6.7. The frequency content of inductor current,

6.2. Measurements on the OFIBO

In this section, measurements on the inductor have been made in order to understand the behaviour of the inductor in a wide frequency range.

6.2.1. Experimental setup for measuring inductance and resistance of OFIBO

To verify the results obtained from the theoretical calculations of the AC resistance, the resistance and the inductance of the inductor are measured with a high precision LCR meter. For the measurements, an Agilent E 4980 E type LCR meter is used. This LCR meter is measuring the voltage drop over and the current through the inductor for different voltage levels and frequencies and processes the data obtained to give out parameters such as *L, R, C, Z, Q* etc.

The LCR meter works in the range of 20 Hz to 2 MHz. It gives 0.05% basic accuracy

with four digit precision throughout its range. The test signal can be adjusted up to 20V RMS and 40V DC bias.

The LCR meter also supports LAN, USB and GPIB PC connectivity. In the measurements subject to this thesis, it is controlled by a pc over an USB port. The interface for making a frequency sweep is programmed in Labview. The necessary drivers are taken from the producer. The range of the sweep is selected between 1 kHz and 2 MHz. The lower limit is selected to be the lower limit of the power supply frequency and the higher limit is chosen to be the highest limit of the LCR meter. The amplitude of the test signals is chosen to be 15V.

The LCR meter is connected to the inductor via coaxial cables. When connecting the coaxial cables 4 terminal pair (4TP) configuration is selected due to the frequency range and for disturbance rejection purposes. The four-terminal pair (4TP) configuration solves the mutual coupling problem because it uses the coaxial cable to isolate the voltage sensing cables from the signal current path [8]. Since the return current flows through the outer conductor of the coaxial cable, the magnetic flux generated by the inner conductor is cancelled by that of the outer conductor (shield) [8]. The measurement range for this configuration can be improved to below 1 Ω.

The impedance measurement range realizable for this configuration depends on the measurement instrument and on how well the 4TP configuration is strictly adhered to up to the connection point of the measured component. The 4TP connection is given below in Figure 6.8. If the cables are not connected properly, the measurement range will be limited, or in some cases, measurement cannot be made. Figure 6.8 also shows an example of incorrect configuration.

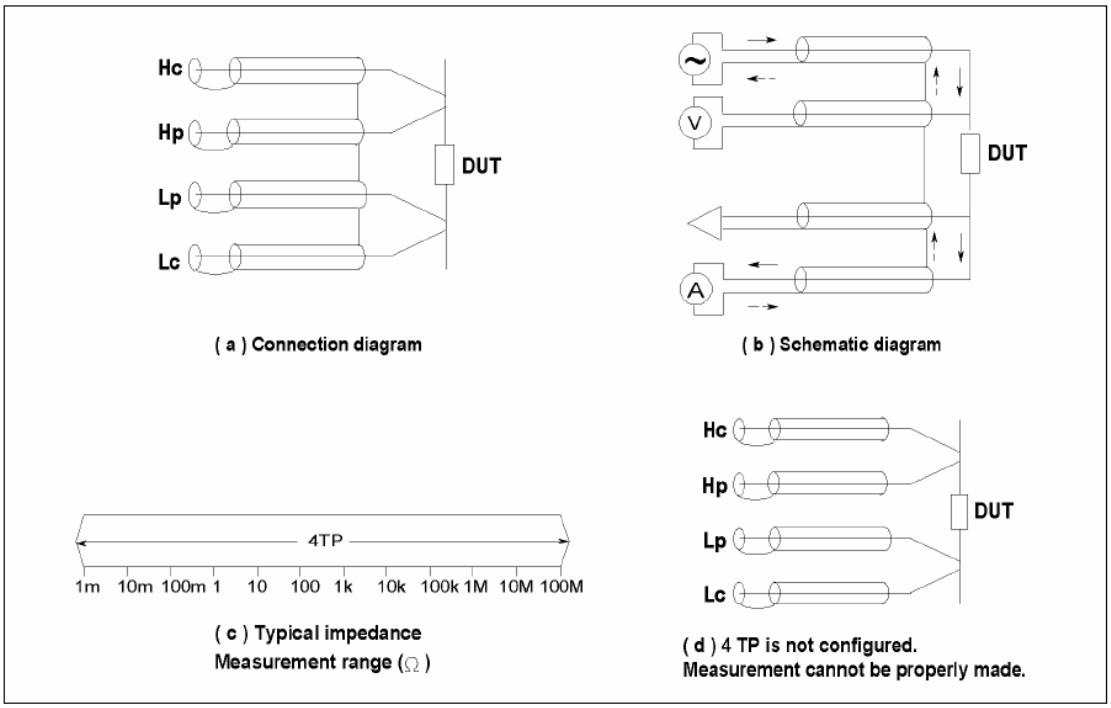

Figure 6.8. 4TP Connection,

6.2.2. Results of the Measurements on the OFIBO

After programming the Labview interface and connecting the inductor with 4TP configuration a frequency sweep between 1 kHz and 2 MHz is done. The experimental result and comparison with the theoretical result is given below in Figure 6.9.

It is clearly seen in the figure that for DC resistance the theoretical and experimental results are almost the same. Theoretical DC resistance is $0.0169\,\Omega$ and measurement result is 0.0165. On the other hand for the AC resistance the theoretical results do not match the experimental results at all. For the lower frequencies the match is not bad, but the error is increasing with frequency.

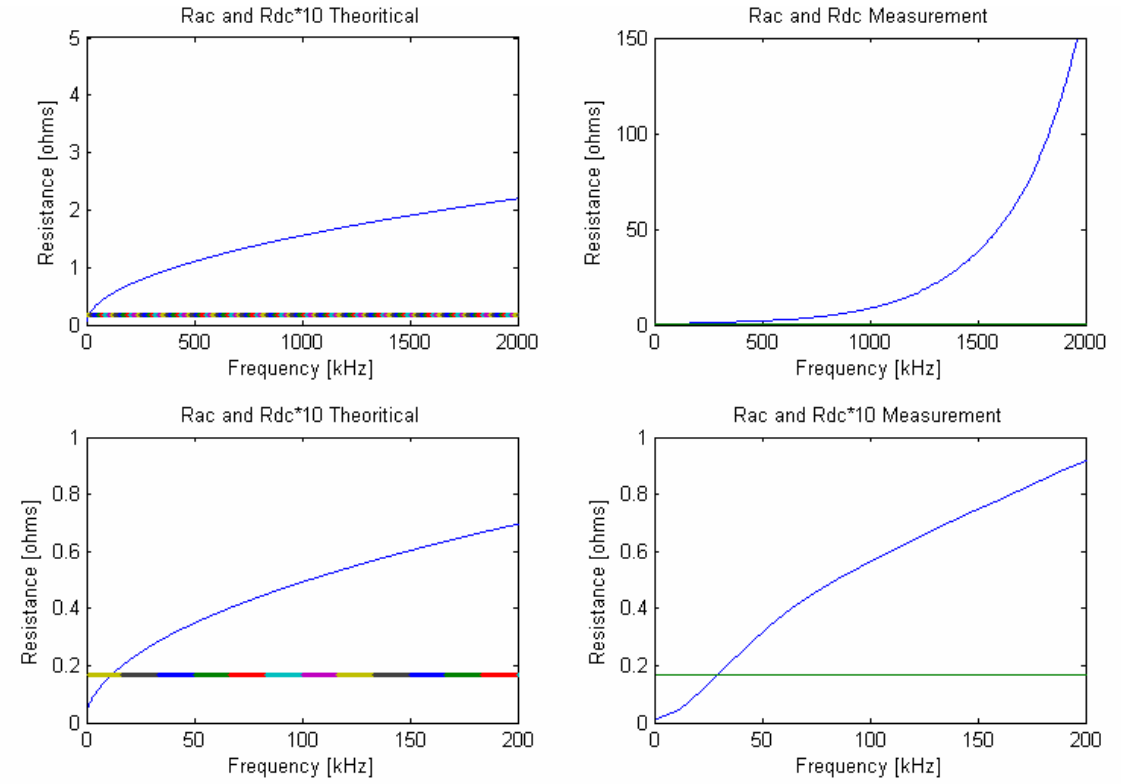

Figure 6.9. Comparison of theoretical Rac and Rdc with experimental results,

After some discussion on what may be the reason for this difference, it is assumed to be because of the capacitive effect between the windings. It is stated in [9] that at high frequencies, the impedance of an inductor ceases to be ideal and is dominated by parasitic capacitances. The cumulative effect of these capacitances is commonly described as a 'stray' capacitance, *Cs*. Of particular interest is the frequency at which the capacitive and inductive impedances match, giving rise to a self-resonance, and providing an upper-frequency bound to operation as an inductor.

The magnitude of the stray capacitance is strongly dependent on the winding geometry and the proximity of any conducting surfaces [9]. Since there are 20 windings in 3 layers, L 800 stray capacitances can be expected due to proximity effect. Therefore a new model for L-800 including stray capacitance has to be derived.

6.2.3. Re-modelling of the OFIBO

All circuit components are neither purely resistive nor purely reactive; they are a combination of these impedance elements. The result is; all real-world devices have parasitics - unwanted inductance in resistors, unwanted resistance in capacitors, unwanted capacitance in inductors, etc. Of course, different materials and manufacturing technologies produce varying amounts of parasitics, affecting both a component's usefulness and the accuracy with which you can determine its resistance, capacitance, or inductance. A real-world component contains many parasitics. With the combination of a component's primary element and parasitics, a component will be like a complex circuit.

For an inductor; resistance of the windings, and resistance of the core due to the permeability of the core, imply that the stray capacitances between the windings are the main parasitic effects. In the L800 inductor case the core losses are neglected since the core has high permeability. The main parasitic effects of the L800 are considered to be resistance of the wires and stray capacitance. Considering these effects, a model for the inductor seen in Figure 6.10 is proposed.

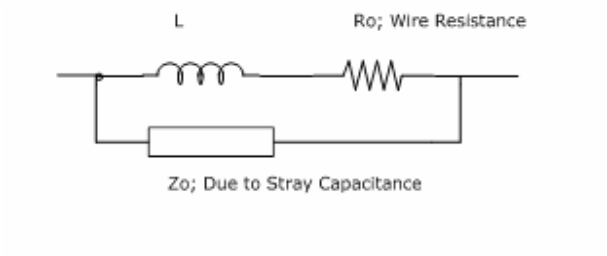

Figure 6.10. Proposed inductor model,

As it is seen in the model, the impedance is proposed parallel to the inductor with winding resistance. Impedance is proposed instead of pure capacitance because it wasn't known from the first place if a pure capacitance would be enough for modelling.

If the equations are derived using basic circuit theory, the following expressions can be obtained for the impedance.

$$Z_{inductor} = \frac{Z_o(R_o + j\omega L)}{Z_o + (R_o + j\omega L)} \tag{6.16}$$

$$Z_o = \frac{Z_{inductor}(R_o + j\omega L)}{Z_{inductor} - (R_o + j\omega L)} \tag{6.17}$$

Here R_o represents the AC resistance of the inductor, L is the pure inductor, $Z_{inductor}$ is the measured impedance of the inductor and Z_o is the impedance caused by stray capacitance effect.

The equations were applied and the following result in Figure 6.11 for Z_o were obtained.

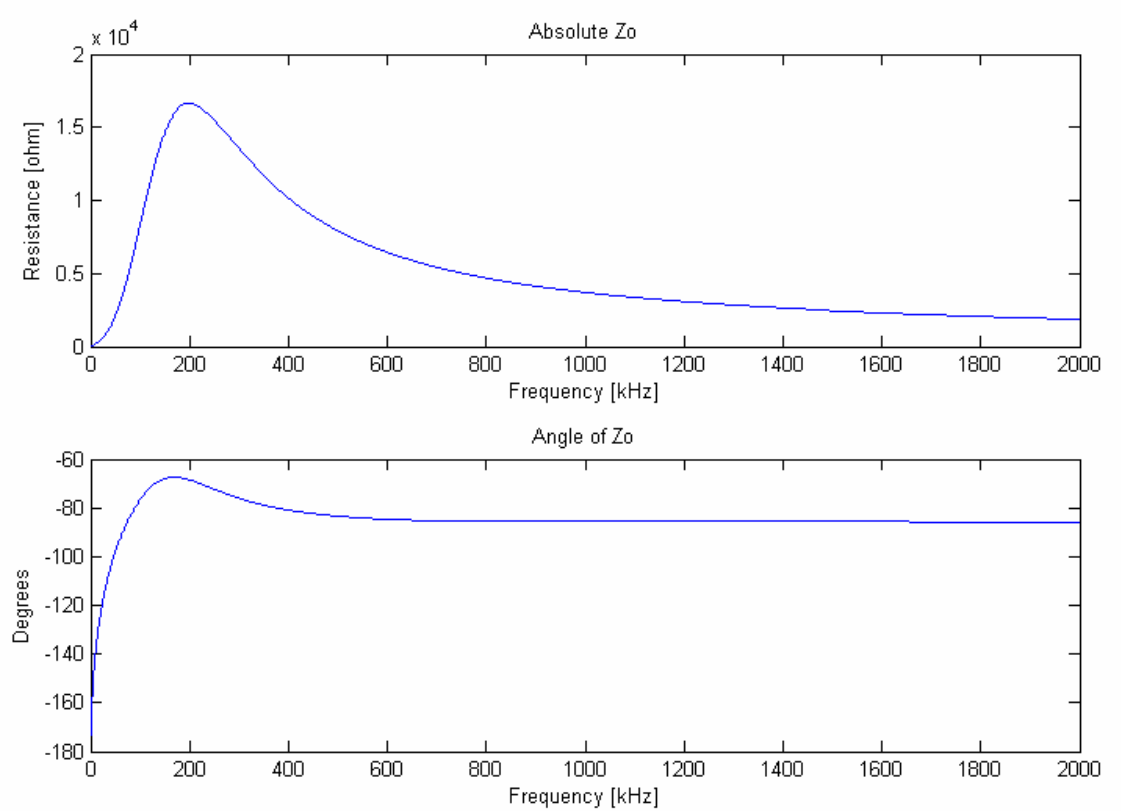

Figure 6.11: Magnitude and Angle of Zo,

Here it is seen that the impedance caused by stray capacitance is not purely capacitive because the angle is not stable at -90 degrees. Also there is a parasitic effect in the lower frequencies. Therefore a resistance in series with a capacitance is also added to model, and the model became as in Figure 6.12.

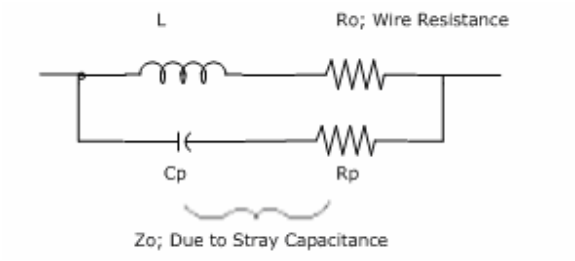

Figure 6.12. Proposed inductor model with components,

Here R_p is the resistive part and C_p is the capacitive part of the parallel impedance caused by stray capacitances in the model.

It must be noted that if this model won't be satisfactory enough, there is always a way to increase the complexity of the model until its behaviour is satisfactory. The extra equations to separate the capacitive and resistive part of the parallel impedance caused by stray capacitances are given below through the following expressions.

$$Z_o = \frac{1}{j\omega C_p} + R_p = R_p - \frac{j\omega}{C_p \omega^2} \tag{6.18}$$

$$R_p = real(Z_o) \tag{6.19}$$

$$C_p = \frac{-1}{img(Z_o)\omega} \tag{6.20}$$

The equations applied and the following result in Figure 6.13 for C_p and R_p were obtained.

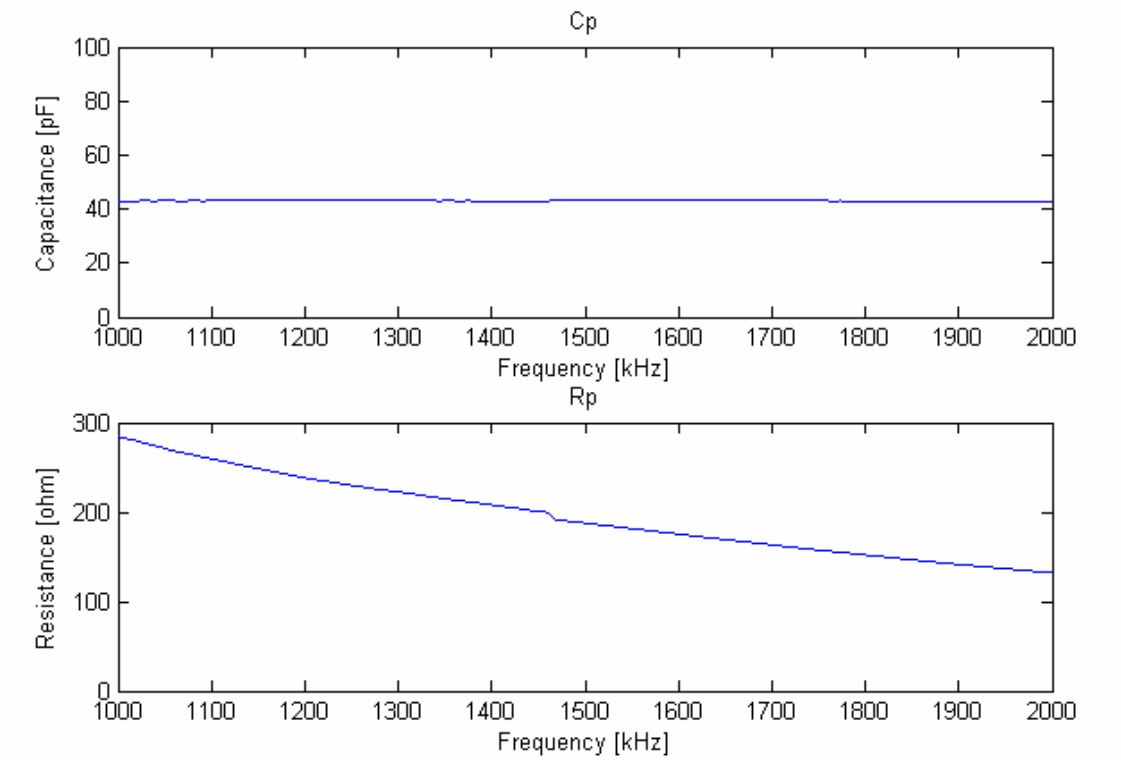

Figure 6.13: C_p and R_p,

First of all here the frequency range is chosen to be between 1MHz and 2 MHz to avoid the transient part in the lower frequencies. Also the capacitive effect becomes more and more significant in the higher frequency range. Looking at the results of the calculations C_p is chosen to be 42.98 pF and R_p is chosen to be 150 Ω and the theoretical results are compared with experimental results once more. The results are given below in Figure 6.14.

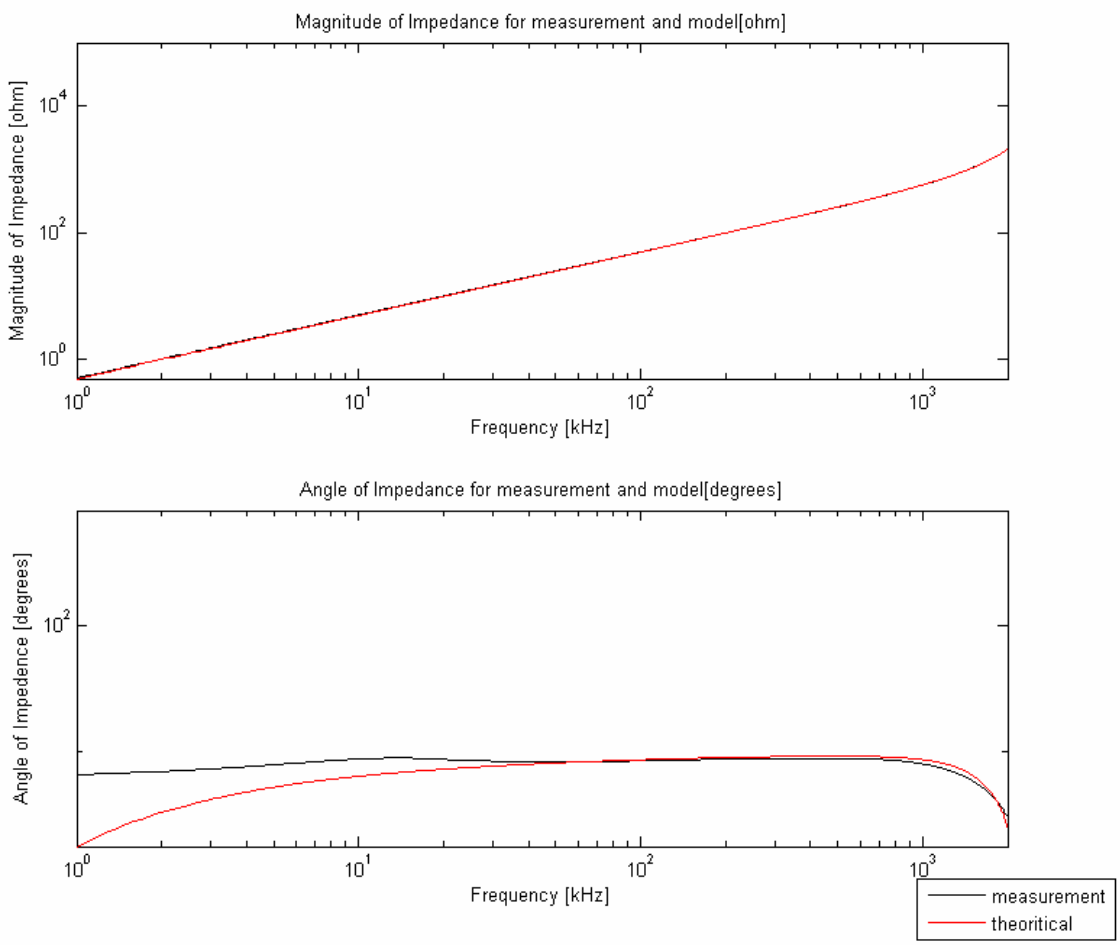

Figure 6.14: Comparison of theoretical model with experimental one,

Here it is seen that the theoretical model matches the experimental results with small errors in lower frequencies. This is maybe due to the interpolation error caused when interpolating the experimental results below 1 kHz, where no measurement is actually done.

This model can be used for later studies or modifications on the inductor, if a solid round conductor is decided to be used after comparison.

6.3. Optimisation of the Output Inductor Windings

In this section, a solution has been proposed to optimise the output inductor in order to decrease winding losses.

6.3.1. The Litz Wire

Litz wire is a special type of wire used in electronics. It consists of many thin wires, individually coated with an insulating film and twisted together; following a carefully prescribed pattern often involving several levels (groups of twisted wires are twisted together, etc.). The combined conductor has a greater surface area than a solid conductor and, because of the twist pattern the magnetic fields generated by current flowing in the strands are in directions such that they have a reduced tendency to generate an opposing e.m.f. in the other strands [11]. Hence, for the wire as a whole, the skin effect and associated power losses when used in high-frequency applications are reduced.

It was stated in some of the previous sections of this thesis that the skin effect is significant in the L 800 inductor. Therefore the Litz wire is proposed to reduce the losses in the inductor. This type of wire is used to wind the inductors and the transformers, especially for the high frequency applications where the skin effect is more pronounced, and the proximity effect can even pose more severe problem. The Litz wire is one kind of stranded wire, but, in this case, the reason for its use is not the usual one of avoiding complete wire breakage due to material fatigue. An example of a Litz wire is given below in Figure 6.15.

Figure 6.15. Typical Litz wire,

If the equations for the AC resistance are taken into consideration, it is seen that the AC resistance depends on the diameter, the skin depth, the number of layers in one winding portion and the DC resistance of the wire. If the wire diameter is decreased the coefficient between the AC and the DC resistance gets lower but on the other hand the DC resistance gets higher. Therefore having parallel windings with small diameters would reduce the AC resistance. On the other hand having parallel windings would cause unwanted

capacitive effects; therefore these windings must be winded in order to minimize these effects. For these reasons the use of Litz wire is proposed.

Unfortunately Dawson's approach for calculating the AC resistance for solid round windings cannot be applied to the Litz wires [7]. Also the geometry and winding of a Litz wire is patented for the manufacturer and most of the time information about that is not avaible. If this information were provided a finite element analysis of the Litz wire can be done to estimate the AC resistance as a future follow up work.

6.3.2. The Solid Wire and the Litz Wire AC Resistance Comparison

In this section the AC resistance of two different type of wires, the solid wire and the Litz wire are measured in a frequency sweep. The wires are not winded to a core but to lower the capacitive effect they are twisted. The result of the measurements is given below in Figure 6.16.

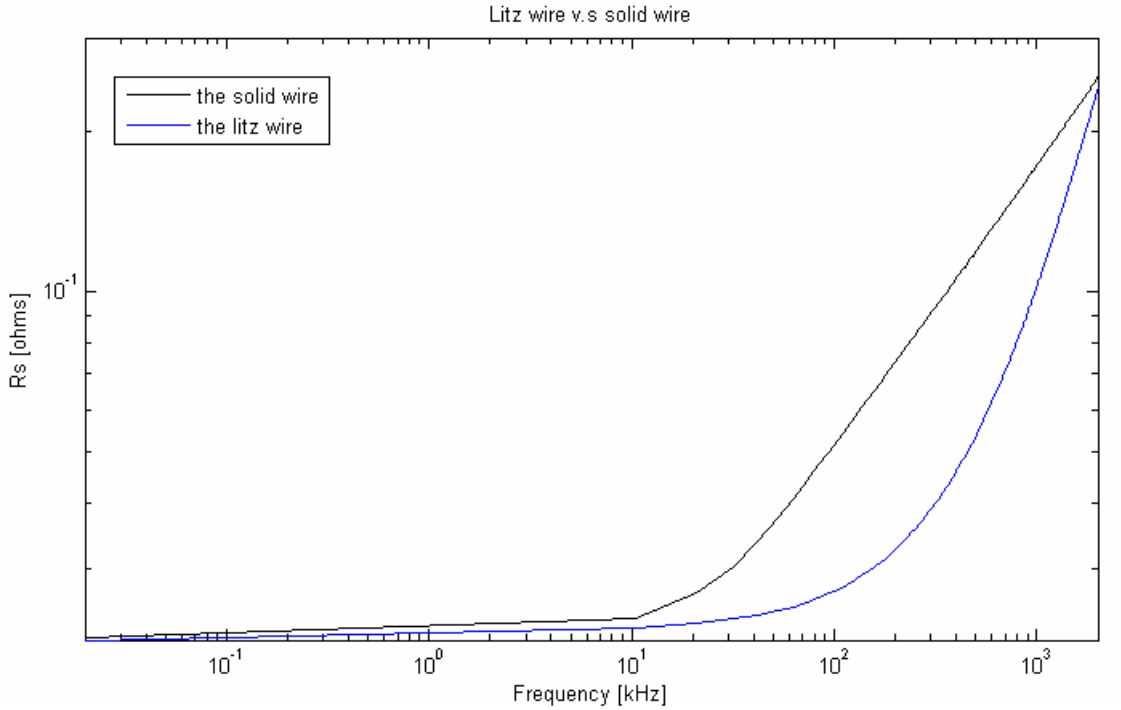

Figure 6.16. AC Resistances of the Litz wire and the Solid Wire,

The DC resistance of the wires are taken to be the same to see the effect of frequency on the resistance of these two types of wires.

Here the most important thing is that, even though the DC resistances of the two wires are the same; the Litz wire has lower AC resistance throughout the frequency sweep range. Moreover, if the AC resistance difference between the two wires increases up to a certain frequency around 300 kHz. After that the resistance difference decreases.

Unfortunately the limitation of the measurement device prevented measurements to include frequencies over 2 MHz. If the measurement range could be increased, it is expected that the AC resistance of the Litz wire would exceed the AC resistance of the solid wire. This is also stated by Alberto Reatti and Francesco Grasso [16]. Nevertheless if Figure 6.7 is recalled, the most important frequency range for the harmonics of the inductor current is between 100 kHz and 500 kHz. Therefore it is appropriate to use the litz wire as an optimisation.

7. Results of the Output Filter Optimisation

To compare the inductors winded with solid wire and the Litz wire, a new inductor with L 800 core is winded with the Litz wire to give approximately 80 uH inductance around the main output frequency level of the power supply. The inductor is seen in Figure 7.1.

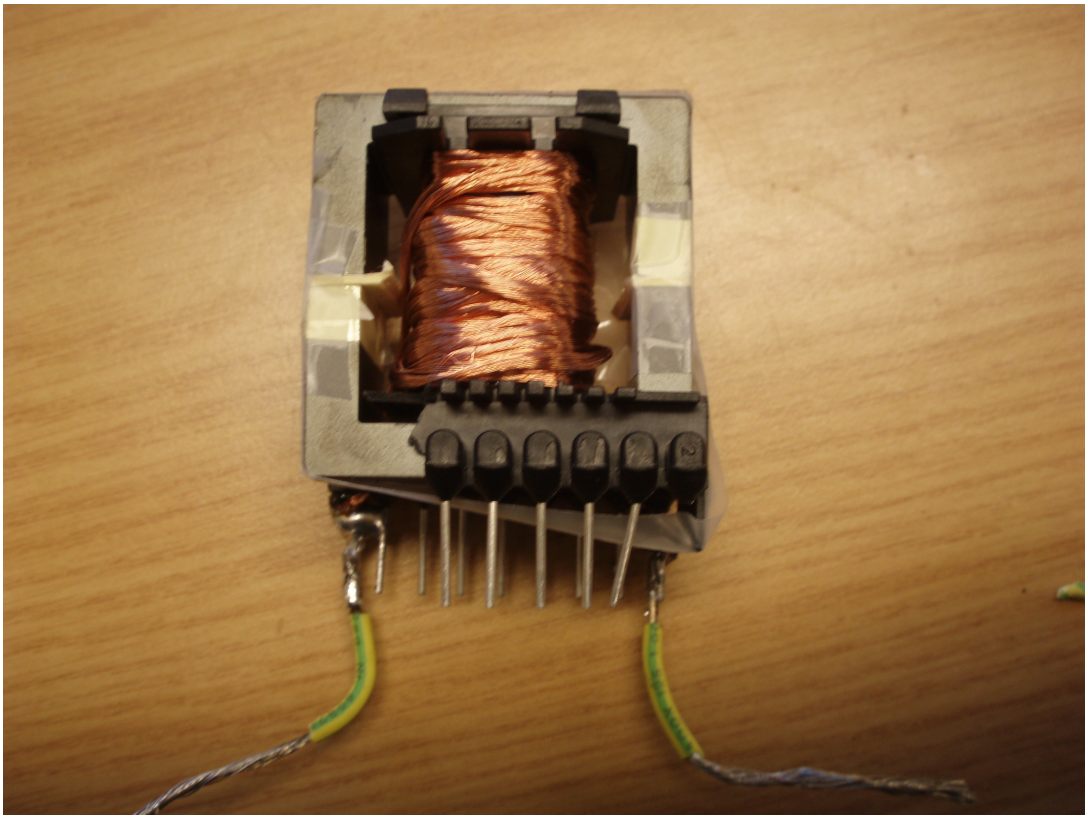

Figure 7.1. Inductor which is winded with the Litz wires.

The Litz wire used to wind the inductor has 120 copper Litz elements with 0.1 mm diameter each. The total effective area of the conductor is around 0.94 mm^2 [10]. The effective area of the solid conductor is 1.508 mm^2 more than 1.5 times that of the litz wire. As expected the DC resistance of the Litz wire is higher than the solid conductor wire, $0.0339\,\Omega$.

Firstly a frequency sweep on both inductors has been done with the LCR meter. The results obtained in the measurements of two inductors are given below in Figure 7.2.

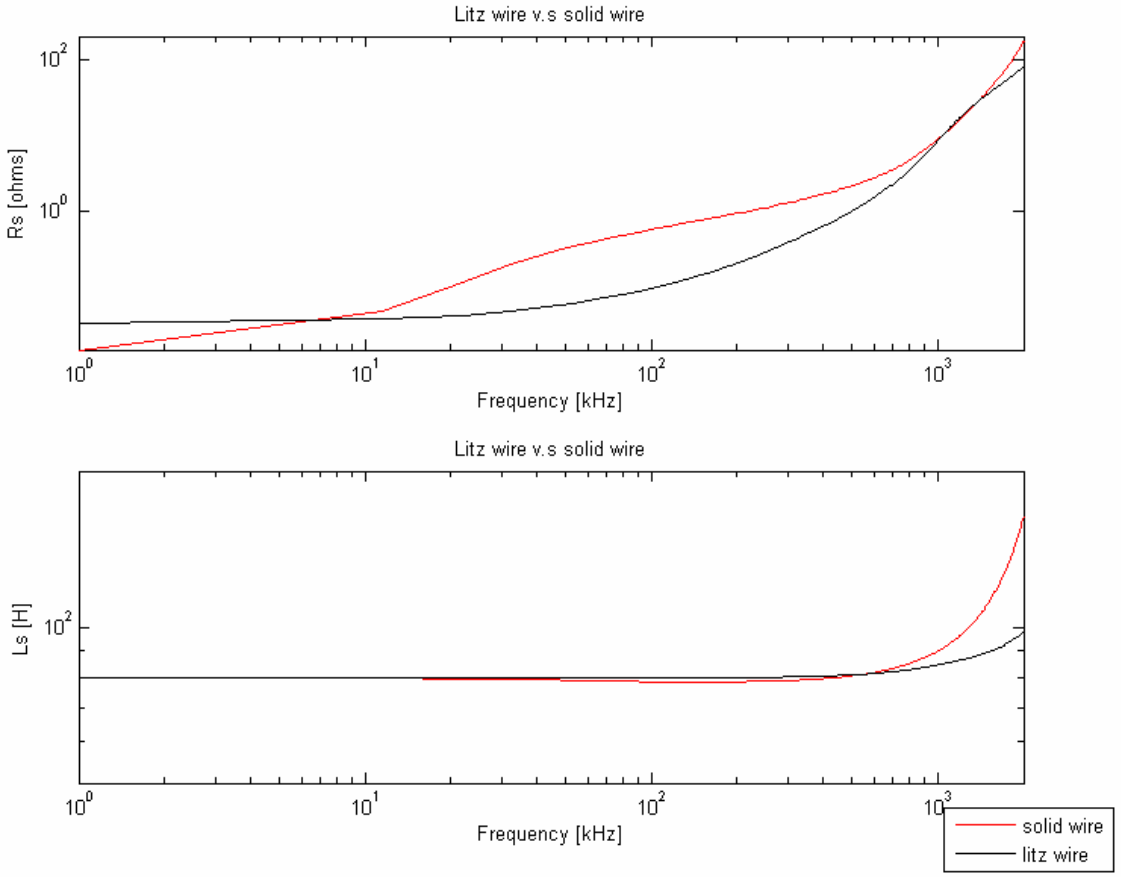

Figure 7.2. Comparison of measurements on two inductors,

Figure 7.2 shows that the inductance part of the inductor with the Litz wire is more stable than the one with the solid wire. This means that the inductance with the Litz wire is more resistant to parasitic effect caused by high frequency. Also at high frequencies it can be clearly seen that the Litz wire winded inductor had less losses, even though it has higher DC resistance. The AC resistance of the Litz wire winded inductor is lower, not just at high frequencies but also in low frequencies as well. Below in Figure 7.3 is the zoomed portion of the graphs for low frequencies, in which the harmonic content of the current is high.

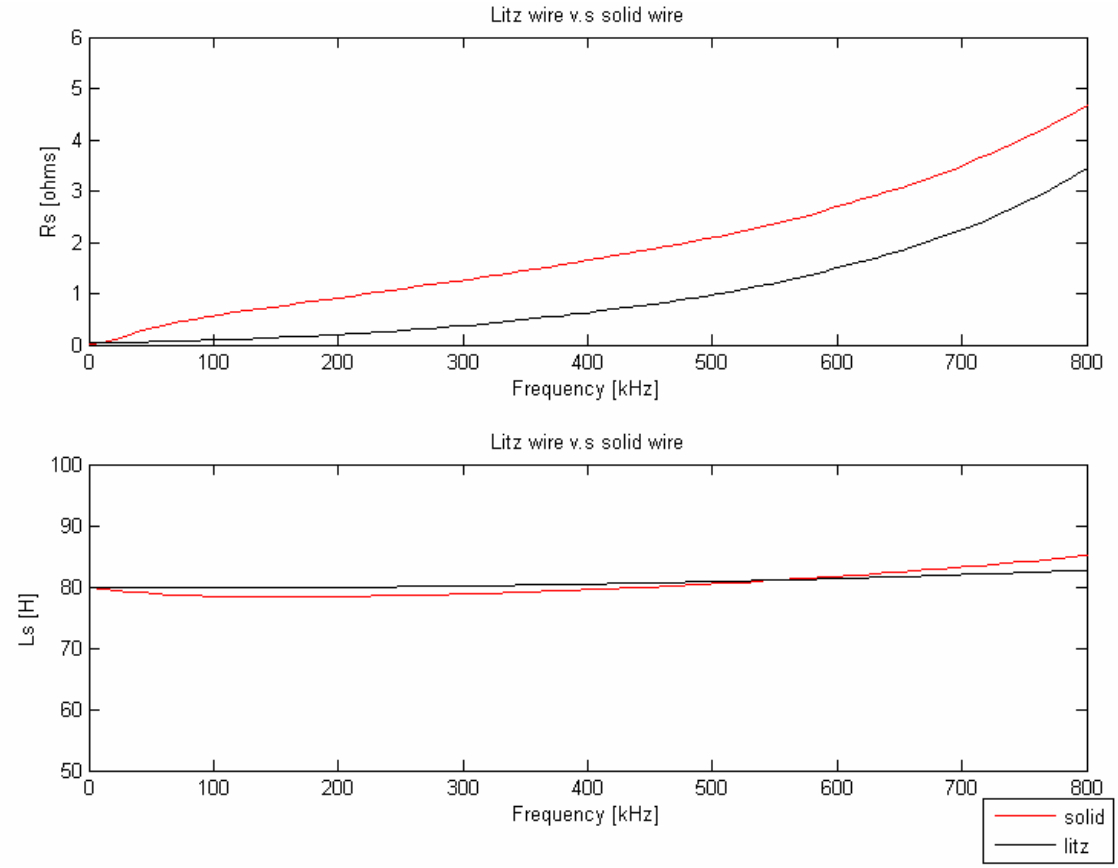

Figure 7.3: Comparison of two inductors,

Nevertheless there is a portion between 1050 kHz and 1380 kHz where the AC resistance of the Litz wire exceeds that of the solid wire.

If the effective area of the Litz wire is selected to be the same as the solid wire, the AC resistance of the Litz wire would drop more, probably to levels below the AC resistance of the solid wire throughout the whole frequency range.

Secondly a temperature measurement has been made on the two types of inductors. The temperature measurement has been made with a surface PT (platinum) RTD (resistive temperature detector) element, pt 100, which has been placed on the windings.

The temperature of both winding has been measured with respect to time, in order to get dynamical response. To isolate the measurement from disturbances, some precautions such as not using cooling and isolating the RTD, were taken. Both inductors have been

placed at the same location, and the power supply has been operated at the same conditions to supply the same load.

The power supply has been operated at 4 kHz with 140 kHz switching frequency in order to supply the light bulb, which was used earlier in the thesis work, with a voltage of 200V. After processing the data to align the starting points, the results are presented in Figure 7.4.

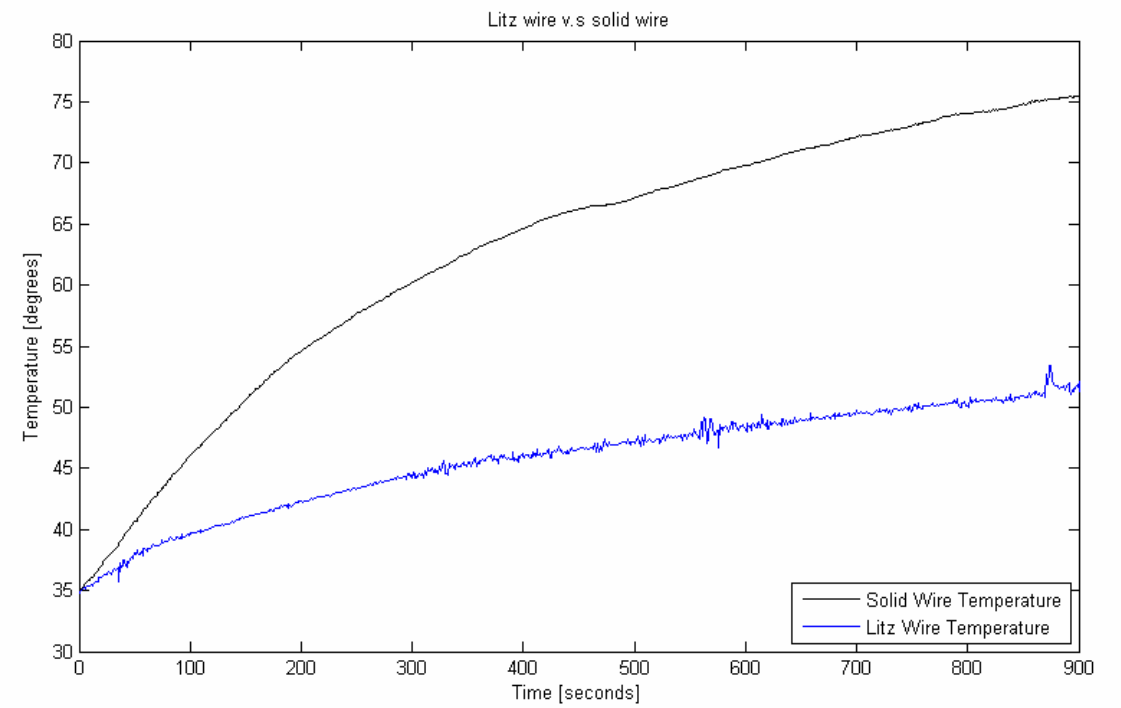

Figure 7.4. Temperature comparison between the two types of inductors,

It is clearly seen in the Figure 7.4 that the winding of the inductor with the solid wire gets hot faster than the winding of the inductor with the Litz wire. The temperature increase of the windings depends on the losses in the windings, which are related to resistance of the windings and the current that flows through them. Considering that the output voltage and frequency are the same in both cases if we assume that the load changes similarly in both cases, the current flow is the same as well. Therefore the only effect is that of the resistance. This shows that the resistance of the solid winding, which is mainly AC resistance at the operating frequency, is higher than the resistance of the Litz winding.

8. Conclusions

In this thesis possible optimizations for a variable frequency and voltage power supply has been investigated. The problems and their causes were analyzed in order propose the optimizations. Two main solutions have been proposed and implemented, as software and hardware optimizations respectively.

Firstly the VSF is implemented as a software optimization, in order to reduce losses. It is observed that with the VSF algorithm, the peak reverse current in the Coolmos on the turn ons can be decreased. This leads to a decrease of the turn on losses especially at high loads.

Also it is observed that the harmonic content of the output voltage of the full bridge is more distributed and does not have a high peak in switching frequency. Since EM noises are caused by high voltage changes, it is believed that the main EM noise source in the power supply is the full bridge. By distributing the frequency content and reducing the peaks the EMI regulations can be matched with a better margin.

Secondly the AC resistance of the output filter inductor, L 800, has been reduced, especially at normal operating conditions, by changing the solid wire windings to the litz wire windings. The measurements show that the losses caused by AC resistance are reduced by using the Litz wire.

Further work can be done as an optimization, in order to enhance the performance of the power supply. For example, more sophisticated control of the frequency of the VSF, the re-design of the output filter to match the VSF, and analytical or FEM modelling of the Litz windings are the first proposed follow up works.

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