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DC voltage control in stacked converters at low pulse numbers

Master of Science Thesis

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Göteborg, Sweden, 2007
Report No. xxxx

Abstract

The increased demand of power from renewably energy sources has driven the development of wind power offshore forward. The power ratio has increased and problems with HVAC cable systems have led the industry to look at other options. One way to handle the increased amount of power is to use HVDC transmission. However the HVDC technique based on thyristors can not be used since it requires a stiff alternating current source at both ends. Instead VSC based HVDC is a possible solution. The VSC based HVDC used today has never been optimised regarding volume which is needed since offshore platforms are very costly. Therefore a new solution has been developed which builds on the idea of connecting a certain number of VSCs in series. In this way harmonic elimination by using phase shifting can be used. This technique leads to lower demand for filter capacity, which saves volume. In this case the phase reactors have been removed and the needed control inductance is obtained from the transformer.

In this thesis two different control models for the series connected VSCs has been developed and tested. The first one, control model A, works by seeing the series connected VSCs as a single large VSC. Therefore only one current vector controller and one DC-link voltage controller is needed. The other model is control model B and it uses a current vector controller and a DC-link voltage controller for each VSC.

The results from the tests show that control model A works as thought but further tests are needed. This is due to problems with the distribution of the DC voltages for the VSC. Control model B on the other hand does not work as thought. The current vector controllers have substantial problems with step response and the DC-link voltage controllers can not perform a start. This model does also require further tests.

Keywords: Voltage Source Converter (VSC), Pulse Width Modulation (PWM), High Voltage Direct Current (HVDC), Control strategies, Series connected VSCs, current vector control

Acknowledgements

This work has been carried out at ABB Corporate Research, Västerås.

I would to special thank my supervisor Dr. Frans Dijkhuizen at ABB Corporate Research for his support and encourage during this work.

I would like to thank my family for their love and support during my studies.

Mikael Holm
January 25, 2007

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1 Introduction

1.1 Background

The demand for renewable energy is rapidly increasing, which is a tendency that is going on since the past decades. Offshore wind farms have earlier been relatively small and delivered small amounts of power. However the increased demand of power has driven the development forward and this yield for wind power offshore a power ratio of up to 160 MW. The method for interconnecting offshore wind farms with onshore utility systems is done through alternating current (AC) submarine cable systems, usually at 33 kV. This is not a good enough solution when higher power levels are in the picture and then a higher wind farm transmission voltage is required, High Voltage Alternating Current (HVAC). This requires a substation platform containing step-up transformers.

The first wind farm with this technique is the 160 MW Horns Rev wind farm, which was taken in to use in 2002 outside the west coast of Denmark. One of the problems with HVAC cable is the capacitive charging current which sets a limit on the length of the cable. The industry has realised the problem and has started to look at another solution, using Direct Current (DC) cable systems when long distances are required. High Voltage Direct Current (HVDC) system also demands an offshore platform, which contains a converter station. Classic HVDC, with phase commutated thyristors, requires a stiff alternating current source at both ends. When there is little or no wind at all the only way to maintain a stiff current source is through standby generators. Another disadvantage is the size of the converter station. An alternative to classic HVDC is Voltage Source Converter (VSC) based HVDC, since its stations are much smaller, though their size have never been optimized.

The losses in the HVDC cable is much lower compared with HVAC, on the other hand the losses in the VSC are 3.2% for both ends. Therefore the VSC based HVDC is interesting when the losses for HVAC cable exceeds that value, which happens at long distances. Furthermore, the VSC HVDC has not yet been used commercial for offshore wind farms and does not have yet a track record. Consequently there are some unique requirements for HVDC offshore, low volume and low losses, and in this way reduce the cost of the system.

Today's HVDC Light® platform consist of 6 pulse bridge converts up to voltages of ±300 kV and it has IGBTs (Insulated Gate Bipolar Transistor) as switching elements. An alternative to offshore is to connect several 6 pulse bridge converters in series and connect them directly with a transformer and by doing so the converter phase reactor can be omitted. Further, at the AC output a multilevel voltage pattern can be obtained with minimum filter requirements. In this way space and volume can be saved on the offshore platform. This topology is called compact HVDC Light® by ABB.

Up to now little work has been done on how the converter control should be done. At the moment the converters are used at low pulse number, which has consequences for the control dynamics and for the dc bus ripple voltage.

1.2 Aim

The aim for this thesis work is to investigate control methods for compact HVDC Light® and particularly at low pulse numbers. Control methods for both HVDC Light® and compact HVDC Light® are considered in this thesis. The intent for the control methods is to maintain a stable and low ripple DC voltage at low converter pulse numbers

1.3 Structure

This thesis has the following structure.

Chapter 2 briefly introduces HVDC as transmission technique, presents its history and also describes the different techniques that are used today.

Chapter 3 describes how the voltage source converter works and presents a couple of different Pulse Width Modulation (PWM) strategies. This chapter also includes derivation of two control systems, current vector controller and DC-link voltage controller. Finally some simulation results are presented in this chapter.

Chapter 4 presents a circuit that is a further development of the voltage source converter presented in Chapter 3. This chapter also includes two different control models for DC-link voltage control.

Chapter 5 shows the simulations results from the testing of two control models.

Appendix A describes how the transformation between three-phase system and αβ-frame is done and how the transformation between αβ-frame and dq-frame is done.

Appendix B, C and D presents how the simulation model used in Chapter 3 and 5 works.

2 High Voltage Direct Current

This chapter describes what High Voltage Direct Current (HVDC) is, what is used for, why it is used and how it works. The brief historical story of HVDC will be told and the different techniques that are used today will be described. The chapter ends with a brief presentation of a new technique, which can be a reality within a couple of years.

2.1 Introduction

Electric energy is produced by power stations in form of AC voltage and current. This energy should be transferred from the power station to the location where the load is. Usually this transfer of energy is done by using AC system. However, in some cases other techniques are attractive, such as DC transmission.

DC transmission becomes economically interesting when large amount of energy should be transmitted over a long distance. Common breakeven distance for profitability for HVDC overhead transmission lines is in the range of 300 - 400 km and for underwater cables the breakeven distance is much smaller [1]. The HVDC becomes interesting at longer distances since AC lines, especially cables, have high capacitance, which limits the lines length. That means that the losses increase when the length of the AC line increases which happens more slowly for DC lines. Already at short distances under water DC becomes a better choice.

There are also other benefits with using DC transmission as you get improved transient stability and dynamic damping of the electrical system oscillations [1]. This gives increased stability in the grid. HVDC also gives the possibility to interconnect two different AC systems, which has different frequencies and is not synchronised. For example it is possible to interconnect the Swedish and the German electrical grid, despite that they are not synchronised. This is due to the fact that the two stations can have phase differences.

Health aspects need to be taken into account for when choosing transmission technique. There is no power frequency magnetic field from DC cables, such as the AC cables have. There is only a static magnetic field and it is similar to the magnetic field of the earth. The recommended values for static magnetic field strength are much higher than for power frequency magnetic fields, because there is no induction effect [2]. At the converter stations the electromagnetic field is kept low due to the fact that the stations are enclosed in buildings and designed to be very efficient shielded. The shield is needed due to that the converter stations are sensitive to radio interference and they also create radio interference for other equipments.

In highly populated areas today it can be extremely difficult to get permission to build a new AC transmission overhead line, both of health reasons and space reasons. The overhead lines occupy larger area but DC transmission needs fewer lines and together with benefits of lower electromagnetic fields it can be easier to get permission for an HVDC overhead transmission line.

There are not only advantages with HVDC and drawbacks are that the converter stations are very expensive and have constant losses. That makes it in some cases less expensive with common AC transmission.

During the last years new markets for HVDC has start to grow. The number of offshore wind farms is rising and it is opening the possibility to use HVDC for transmission of the energy to mainland. Another trend is that oil platforms are being connected with the mainland via HVDC. The electricity that the oil platform needs to work is normal created by steam turbines. The stream is created by burning natural gas. Instead, if the electricity is supplied via HVDC the emission of carbon dioxide is reduced.

2.2 History of HVDC transmission

ASEA started as early as in end of the nineteen twenties to develop products for HVDC transmission. At that time a young man with the name of Uno Lamm, later known as the Father of HVDC, started

working at ASEA and with HVDC. The component that ASEA worked with was mercury arc valves but it had some problems. The biggest problem was with arc-backs and Uno Lamm worked a lot to solve that problem. However it would take some time before the first HVDC transmission line was used in normal service. The Swedish utility company Vattenfall and the Swedish government decided in 1950 that a DC line between the island of Gotland and the Swedish mainland should be built. In this way the local grid on Gotland would be connected to the Swedish grid. A system with capacity of 20 MW and with transmission voltage of 100 kV has been ordered. However, still there were some problems with the HVDC technology and first in 1954 the line could be taken into service. The breakthrough for HVDC came in the nineteen sixties when ASEA received four international contracts which they worked on in parallel. The largest system that was built with mercury arc valves was at Nelson River in Canada and system was built for 150 kV and 2 kA [3].

With HVDC mercury arc valves ASEA was the only manufacture but the competitors wanted a piece of the HVDC market. The competitors discover that there chance was the new component thyristor. The thyristor had the advantage that it did not age and if it failed, it had fail safe, i.e. the thyristor would lose its semi-conductor properties but retain its current carrying capability. ASEA was forced to start working with the thyristor to keep its strong market position and researching started in the middle of the nineteen sixties. In 1970 the first plant with thyristors was taken into service. The thyristors operated in series with two mercury arc valves in Gotland. At the same time the mercury arc valves started to vanish and in 1971 the research was cancelled but still in 2004 nine systems was in service, and total amount of delivered systems were 17 [3]. The development of the thyristors continued and ASEA/ABB came to be world leader in this field. Today they can offer HVDC up to 1500 MW [4].

A further step in the development of the HVDC was taken in 1997 when ABB introduced voltage source converter based HVDC, the HVDC Light®. It is the third generation of HVDC with IGBT (Insulated Gate Bipolar Transistor) valves. The first new system was taken into service was in 1999 and it was a line on Gotland between a wind farm and the local grid. The system was designed for 50 MW and with voltage at ±80 kV. The latest system was taken into service in 2006 and it is a line between Estonia and Finland. The system has a capacity of 350 MW and ±150 kV.

2.3 HVDC Classic

A typical single-line diagram of a HVDC Classic transmission system, which interconnects two AC systems, is shown in Fig 2.1. Both systems can have independent loads and local generation. It is also possible to have power flow in both directions of the HVDC system.

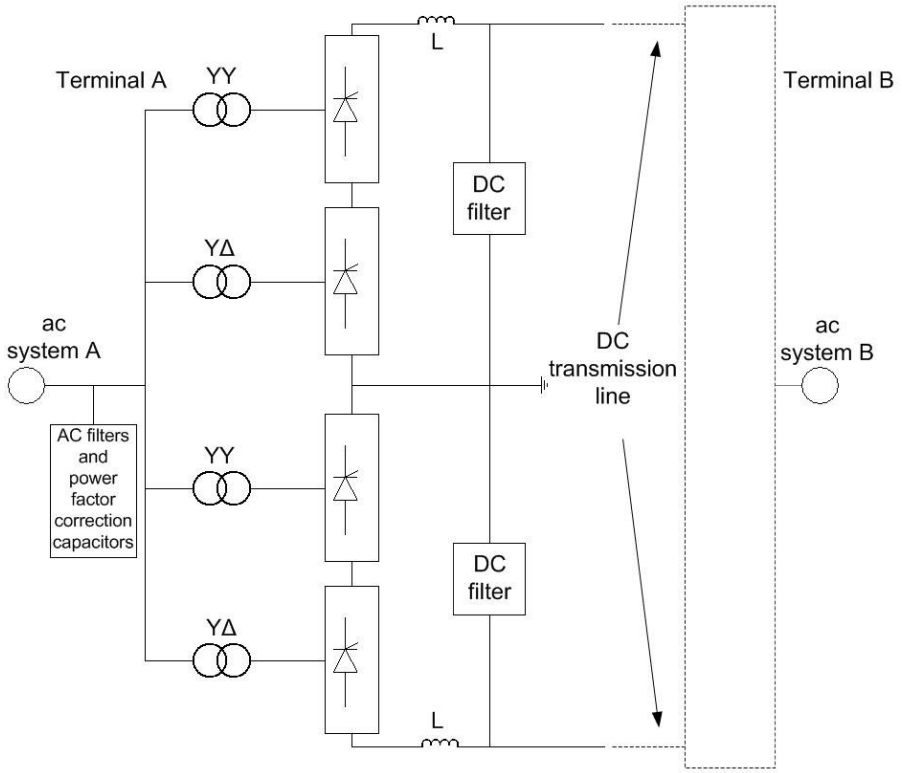

Fig 2.1 A typical HVDC Classic system

Assume that the power flow is from station A to station B. Then the system works in the following way, first the grid voltage for system A is transformed up to the transmission level. The converters at station A rectify the voltage and apply it to the HVDC transmission line. At station B the voltage is inverted by the converters and the voltage is transformed down at the transformers, to match system B's grid voltage. It should be remembered that HVDC Classic is a current stiff system.

Each converter terminal consists of a positive and negative pole. Each pole consists of two 6-pulse line-frequency bridge converters. These two are connected through a y-Y and a y-Δ transformer and in this way a 12-pulse setup is given.

At each terminal there is an AC filter and its function is to minimise the current harmonics which are generated by the converters from reaching the grid. At the AC filter there are also power factor correction capacitors, which supply the converters with the reactive power that they need. At the DC side there are two DC filters and two smoothing inductors, L. Their function is to minimise the ripple in the HVDC transmission line [1].

2.3.1 Area of use

HVDC Classic is used generally when very large amount of power needs to be transmitted over a long or very long distance. The losses from an AC system increases with the distance and HVDC Classic becomes economically possible when the AC system losses are larger than the losses from the HVDC Classic system.

2.4 HVDC Light®

HVDC Light® uses IGBT valves instead of thyristors valves, which HVDC Classic is using. A major difference between HVDC Light® and HVDC Classic is that the Classic works as a current source while the Light works as a voltage source. In other words, the power transmission for HVDC Classic is determined from current while for HVDC Light it determined from voltage.

In Fig 2.2 a single-line diagram over a HVDC Light® terminal is shown. At the end of the DC cable an exact same type of terminal can be found. The terminal consists of a power transformer, which

transform up the voltage to the transmission level. The voltage is rectified with help from the voltage source converter. The VSC works both as a rectifier and inverter, depending of the active power flow direction. The VSC consists of six valves and it will later be discussed in detail. After that the voltage has been rectified it is connected to the DC cable. At terminal B the voltage is inverted and transformed down to the grid voltage level.

HVDC Light® needs filter to work as thought. There is a Harmonic filter and its purpose is to limit the amount of harmonics that can reach the grid. There is one phase reactor per phase, between the power transformer and the VSC. The phase reactor works as a series filter. The phase reactor reduces the amount of current harmonics that reach the utility grid. By using the phase reactor an almost perfect sinusoidal current reaches the grid. At the DC side there is also a filter and it consist of capacitors. They keep the voltage at the DC cable as constant as possible [2].

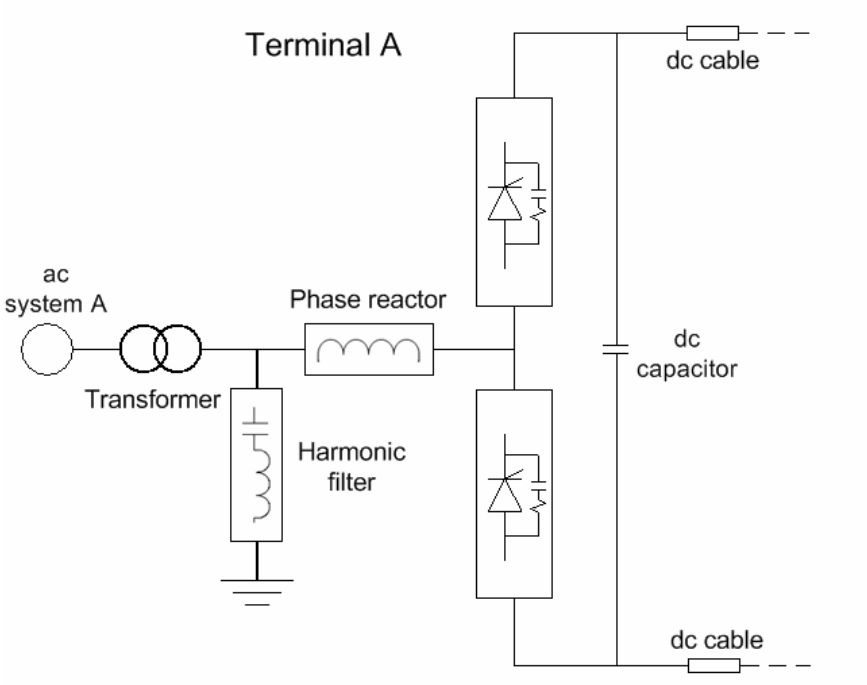

Fig 2.2 Simplified single-line diagram for HVDC Light

2.4.1 Advantages of the HVDC Light®

- Active and reactive power can be controlled independently and rapidly [2].
- Black start possible [2]
- Stabilize the AC grid [2]
- Possibility to change from full power in one direction to full power in reverse [2]
- No minimum power is required, can operate down to zero power [2]
- No need for additional reactive shunt compensation [2]
- Can work as a STATCOM (Static Synchronous Compensator) even when the DC line is disconnected [2]
- No electromagnetic fields [2]
- Reduce risk of flashover, due to indoor design [2]

2.4.2 Differences between HVDC Light® and HVDC Classic

HVDC Light®

- Each terminal is a HVDC converter and a SVC (Static VAr Compensator) [2]
- Suitable both for submarine and land cable connections [2]

- Less area needed [2]
- Forced commutation up to 2000 Hz [2]
- Power range 50 – 1100 MW [2]
- IGBT valves

HVDC Classic

- Power range up to 3000 MW [2]
- Most cost effective in the higher power range [2]
- Thyristor valves
- Can not be turn off with a control signal
- Line commutated, 50 / 60 Hz

2.4.3 Area of use

Today HVDC Light® can not handle the same power levels as the HVDC Classic can. Therefore HVDC Light® is used when smaller amount of power should be transmitted. HVDC Light® is used where it would be too expensive to build the transmission line with HVDC Classic. In this way a new market for HVDC has been created. For instance HVDC Light® can be used to supply oil platforms with power and it can also be used to connect wind farms with the grid. The small size of the terminals and the possibility to use cables has made HVDC Light® a reasonable alternative in the transmission grid. HVDC Classic demands too high power levels and too long distance to be an economically alternative. These obstacles have now diminished with HVDC Light®.

2.5 Compact HVDC Light

Compact HVDC Light is based on HVDC Light® but it also includes some improvements. HVDC Light® is not optimized regarding size. Additionally, with the Compact HVDC Light efforts has been spent on trying to reduce the losses.

An important improvement is the reduction of the filter size and it has been made by decreasing the amount of harmonics in the system. The reduction has been possible by connecting eight voltage source converters in series. In this way each voltage source converter can run with a lower pulse number, switching frequency divided by the fundamental frequency. These techniques make the switching losses of transistors lower. To be able to reduce the harmonics the carrier waves for the eight converters are evenly displaced. By using this technique it is possible to remove the phase reactors and the only inductances in the circuit are the leakage inductance of the transformer. When the amount of harmonics is diminished the harmonic filter and the DC capacitors can be made smaller. The phase reactors, the harmonic filter and the DC capacitors occupies more than half of the total volume for a normal HVDC station and the phase reactor part is approximately a third of that. Therefore it is easy to understand how much volume that it is saved when the phase reactors are removed. The reduction of the volume gives lower construction costs, especially when it is used for offshore wind farms.

2.5.1 Research issues

Compact HVDC Light is not a commercial product and more research is planned. There are some technical problems that need to be solved to reach a final product. One problem is whether the windings of transformers can handle the stress that arises now that voltage is square-waves, because the phase reactors are removed. Also the converter control needs be investigated, since little effort has been put into it. The question is if it is possible to have a stable system and at the same time preserve the low amount of harmonics. In addition also the capacitors size needs to be investigated more.

3 Three-phase Voltage Source Converter

In this chapter the basics of a Voltage Source Converter (VSC) for High Voltage Direct Current (HVDC) will be discussed, control issues are addressed as well. In the first part the operation of VSC will be discussed. After that a shorter discussion about different PWM techniques will follow. Then the current vector controller is studied, which includes information about how it works and how it is designed. The DC voltage controller is then described and finally the chapter ends with a summary.

3.1 Voltage Source Converter scheme

VSC is a forced-commutated converter that converts AC voltage into DC voltage or vice versa. The VSC has the ability to let the power flow in both direction and can change the power direction in a very short time. It can be seen as a controllable voltage source. VSC is for example used in high power applications, such as HVDC Light.

In Fig 3.1 a drawing of a standard VSC is shown. It is a six-pulse forced-commutated converter and it consist of six power semiconductors and six anti-parallel connected diodes. The semiconductors are in this case of the type Insulated Gate Bipolar Transistor (IGBT). Some alternatives are Gate-Turn-Off Thyristors (GTO) and Gate-Controlled Thyristors (GCT).

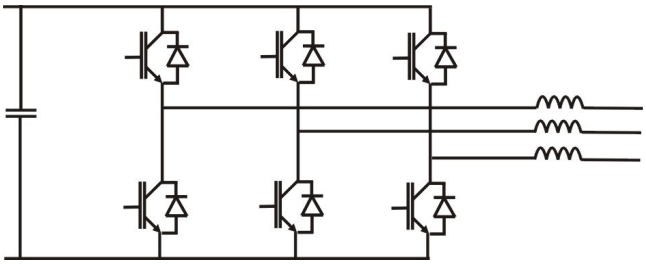

Fig 3.1 Drawing of a VSC

The output voltages of the converter can be controlled by modulation techniques and in this thesis Pulse-Width Modulation (PWM) will be used.

3.2 Pulse Width Modulation

Pulse-Width Modulation (PWM) is used to create a desired signal and in this case a sinusoidal wave with determined amplitude and frequency. There are several different modulation methods but they all have two objectives. The first is to calculate the on time for the switches and the desired fundamental output voltage is obtained. The second objective is to arrange the switching process to minimize the harmonic distortion, switching losses or other specified criterion. Three different techniques, natural-sampled PWM, regular-sampled PWM and optimized PWM, for creating the wanted signal will be briefly discussed.

3.2.1 Natural-sampled PWM

Natural-sampled PWM, also called sinusoidal PWM, works by comparing a low frequency sinusoidal wave with a determined frequency, reference wave, to a high frequent triangular wave, carrier wave. The switching instant is determined when the reference signal and the carrier wave intercept with each other. In this way, a switching pattern is obtained. If the reference signal has a larger value than the carrier wave, the switch signal becomes high and it becomes low when the reference signal has a smaller value. The switching frequency for the system is determined by the carrier wave's frequency and the created signal's fundamental amplitude is determined according to the following expression [1].

$$V_p = m \cdot \frac{V_d}{2 \cdot \sqrt{2}} \tag{3.1}$$

where V_d is the DC-link voltage and m is the modulation index.

The modulation index is usually within the range of zero and one. However, it can have higher value than one and then the converter works in overmodulation. Overmodulation creates more harmonics comparing to when the modulation index is in the interval of zero and one. The modulation index is calculated in the following way [1].

$$m = \frac{V_{control}}{V_{tri}} \tag{3.2}$$

where $V_{control}$ is the peak-value for the reference signal and V_{tri} is the peak-value for the carrier wave.

An advantage with natural-sampled PWM is that it is easy to implement with analogue techniques. A simple circuit contains a comparator which detects the intersections between the carrier wave and the reference wave [5].

3.2.2 Regular-sampled PWM

Regular-sampled PWM is used with microprocessors or Digital Signal Processors (DSP). It works in the following way, samples of the reference signal is taken at regularly spaced intervals, coinciding with the carrier wave's peaks. This happens either once or twice in each carrier cycle. If it is done one time per cycle it is called symmetric regular-sampled PWM and the sampling frequency is the same as the switching frequency (carrier wave frequency). On the other hand, if it is done twice per cycle it is called asymmetric regular-sampled PWM and the sampling frequency is the double switching frequency. This gives that the sampled signal has constant amplitude during each sampling interval. The width of the pulse is proportional to the amplitude of the reference signal at uniformly spaced sampling times. After that the sampled signal is compared to the triangular wave and the switching pattern is determined. The benefit of using asymmetric regular-sampled PWM is that the sampled signal contains more information about the reference signal than what the sampled signal does when symmetric regular-sampled PWM is used.

3.2.3 Optimized PWM

It is possible to improve the performance for the PWM with help from different sorts of techniques, i.e. maximize the output voltage amplitude. One technique is Third Harmonic Injection PWM technique. It works by injecting third harmonic component to the reference signal, the sinusoidal wave. This can give a performance boost of about 15 % in the gain. But it also leads to third harmonics in the line-to-neutral, if not a balanced load with floating neutral point is used [6]. The optimised PWM technique is not taken under consideration.

3.3 Current vector controller

The current vector controller's task is to control the currents floating in the grid so that they are equal to the reference value. The quantities with a star are reference signals. The controller consists mainly of three different parts, current vector controller, transformation blocks and PWM. The transformation blocks transform the three-phase quantities to DC quantities and in this way the currents can be controlled easier. The block diagram of the controller is presented in Fig 3.2.

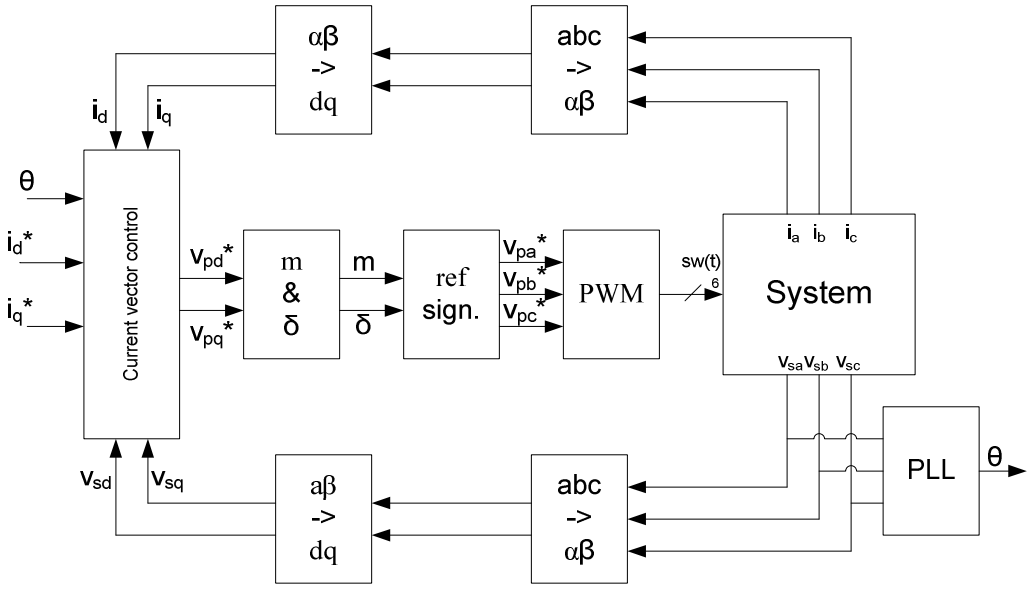

Fig 3.2 Block diagram of the current vector controller

The inputs to the current vector controller are the filtered grid voltages and grid currents. They are transformed to the αβ-frame, and then transformed to the rotating dq-frame. The equations used in the transformations of the currents and the voltages are shown in Appendix A. Usually, the transform uses a generator magnetic flux vector as reference for the synchronisation of the dq-frame, i.e. dq-frame rotates. It makes the voltages and the currents to becoming constant vectors in the dq-frame, when steady state is attained. In this thesis however the grid flux is used and also the q axis is set to follow the grid voltage vector. In this way the grid voltage vector only consists of a q-component, the d-component is zero. The reason is that then the q-component of the current is the active part and d-component is the reactive part. By doing this the power factor is one when the d-component of the current is zero.

The DC quantities are then used as inputs for the PI controller, which task is to control and reduce the steady state error. Out from the PI controller comes two voltages, d and q-component of the VSC reference voltage. These are then used to calculate the modulation index, m, and the load angle, δ. The modulation index and the load angle are used to get three-phase voltages, which are used as reference voltages for the PWM. Out of the PWM the transistors gate signals are obtained, i.e. the switching patterns. The theta block calculates the grids flux angle, which is used in the αβ to dq transformation.

3.3.1 A Simplified model

Before a controller can be designed a model of the system needs to be derived. In Fig 3.3 a simplified model of a grid-connected VSC is shown. The grid and the VSC are modelled as two three-phase voltage sources and one RL-filter at each phase. The VSC consist of six IGBTs, six diodes and two capacitors.

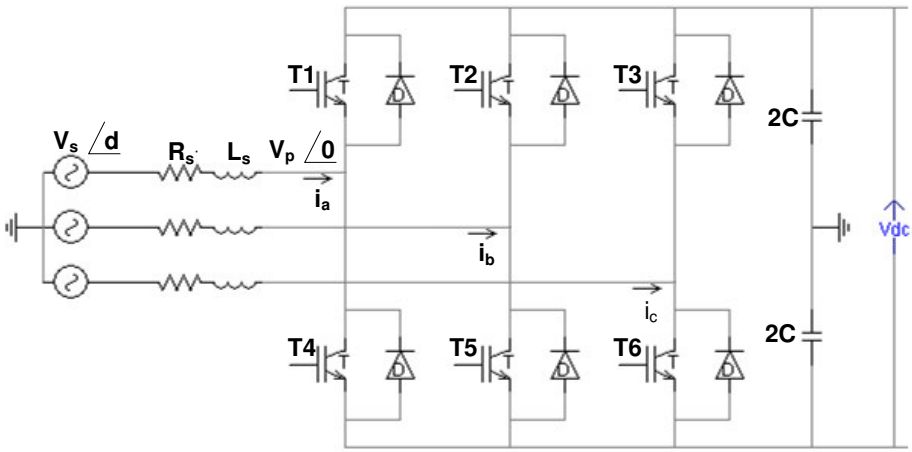

Fig 3.3 A basic model of a VSC

If the resistor R is neglected the active power P and reactive power Q can be expressed as in Equations (3.3) and (3.4).

$$P = \frac{V_s \cdot V_p}{X_s} \cdot \sin\delta \tag{3.3}$$

$$Q = \frac{V_s \cdot \left(V_s - V_p \cdot \cos\delta\right)}{X_s} \tag{3.4}$$

where V_s denotes the fundamental component of the AC grid voltage, V_p denotes the VSC fundamental voltage, δ denotes the phase-angle difference between V_s and V_p and X_s denotes the reactance of converter.

The circuit in Fig 3.3can according to Kirchhoff's voltage law be mathematically modelled as

$$v_{p1}(t) = -R_s \cdot i_1(t) - L_s \cdot \frac{d\,i_1(t)}{dt} + v_{s1}(t) \tag{3.5}$$

$$v_{p2}(t) = -R_s \cdot i_2(t) - L_s \cdot \frac{d\,i_2(t)}{dt} + v_{s2}(t) \tag{3.6}$$

$$v_{p3}(t) = -R_s \cdot i_3(t) - L_s \cdot \frac{d\,i_3(t)}{dt} + v_{s3}(t) \tag{3.7}$$

where $v_{P1}(t)$, $v_{P2}(t)$ and $v_{P3}(t)$ are VSC output voltages, $v_{S1}(t)$, $v_{S2}(t)$ and $v_{S3}(t)$ are the grid voltages, $i_1(t)$, $i_2(t)$ and $i_3(t)$ are the grid currents .The reference direction of the current is from the grid to the VSC.

The grid voltages can be expressed as

$$v_{s1}(t) = V\cos(\omega \cdot t) \tag{3.8}$$

$$v_{s2}(t) = V\cos\left(\omega \cdot t - \frac{2\pi}{3}\right) \tag{3.9}$$

$$v_{s3}(t) = V\cos\left(\omega \cdot t + \frac{2\pi}{3}\right) \tag{3.10}$$

Equations (3.5)-(3.7) transformed to the αβ-frame, with amplitude invariant transformation, becomes

$$\underline{v}_{p\alpha\beta}(t) = -R_s \cdot \underline{i}_{\alpha\beta}(t) - L_s \cdot \frac{d\,\underline{i}_{\alpha\beta}(t)}{dt} + \underline{v}_{s\alpha\beta}(t) \tag{3.11}$$

where

$$\underline{v}_{p\alpha\beta}(t) = v_{p\alpha}(t) + jv_{p\beta}(t) \tag{3.12}$$

$$\underline{v}_{s\alpha\beta}(t) = v_{s\alpha}(t) + jv_{s\beta}(t) \tag{3.13}$$

$$\underline{i}_{\alpha\beta}(t) = i_{\alpha}(t) + ji_{\beta}(t) \tag{3.14}$$

Equation (3.11) can be transferred into the dq-frame by using the αβ to dq transformation, where the q axis is synchronised with the grid voltage vector. In this way all the quantities becomes DC quantities and it simplifies the design of the controller.

$$\underline{v}_{pdq}(t) = -R_s \cdot \underline{i}_{dq}(t) - L_s \cdot \frac{d\,\underline{i}_{dq}(t)}{dt} - j\omega L\underline{i}_{dq}(t) + \underline{v}_{sdq}(t) \tag{3.15}$$

where

$$\underline{v}_{pdq}(t) = e^{-j\theta(t)} \cdot \underline{v}_{p\alpha\beta}(t) = v_{pd}(t) + jv_{pq}(t) \tag{3.16}$$

$$\underline{v}_{sdq}(t) = e^{-j\theta(t)} \cdot \underline{v}_{sdq}(t) = v_{sd}(t) + jv_{sq}(t) = jv_{sq} \tag{3.17}$$

$$\underline{i}_{dq}(t) = e^{-j\theta(t)} \cdot \underline{i}_{p\alpha\beta}(t) = i_d(t) + ji_q(t) \tag{3.18}$$

$$\theta(t) = \arctan\left(\frac{v_{s\beta}}{v_{s\alpha}}\right) - \frac{\pi}{2} \tag{3.19}$$

Equation (3.15) is split into two equations, representing the d and q-components respectively.

$$v_{pd}(t) = -R_s \cdot i_d(t) - L_s \cdot \frac{d\,i_d(t)}{dt} - \omega L_s i_q(t) + v_{sd}(t) \tag{3.20}$$

$$v_{pq}(t) = -R_s \cdot i_q(t) - L_s \cdot \frac{d\,i_q(t)}{dt} + \omega L_s i_d(t) + v_{sq}(t) \tag{3.21}$$

The grid voltages in Equations (3.8) to (3.10) transformed into dq-frame

$$\underline{v}_{sdq}(t) = v_{sd}(t) + jv_{sq}(t) = jV \tag{3.22}$$

The active and reactive power can also be calculated as

$$P = \frac{3}{2}v_{sq}(t) \cdot i_q(t) + \frac{3}{2}v_{sd}(t) \cdot i_d(t) = \frac{3}{2}v_{sq}(t) \cdot i_q(t) \tag{3.23}$$

$$Q = \frac{3}{2}v_{sq}(t) \cdot i_d(t) - \frac{3}{2}v_{sd}(t) \cdot i_q(t) = \frac{3}{2}v_{sq}(t) \cdot i_d(t) \tag{3.24}$$

From Equations (3.23) and (3.24) it is obvious that the active and reactive power can be independently controlled by controlling the q and d-component of the current.

3.3.2 Derivation of the PI controller

Equation (3.20) and (3.21) describes the VSC system in the rotating dq-frame. Alternative to the simplified circuit a block diagram can be made, seen in Fig 3.4.

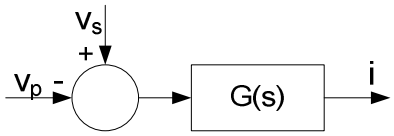

Fig 3.4 Block diagram for the VSC model

The input signal is v_p, output signal is the current vector and v_s is modelled as a load disturbance. By applying the Laplace transform to Equation (3.15) the transfer function G(s) is given.

$$G(s) = \frac{1}{(s + j\omega)L + R} \tag{3.25}$$

The term $j\omega L$ in Equation (3.25) is the reason for existence of the cross-coupling between Equations (3.20) and (3.21). The cross-coupling is described with the term $\omega L_s i_q$ in Equation (3.20) and with the term $\omega L_s i_d$ in Equation (3.21). In Equation (3.15) the term $j\omega L_s \underline{i}_{dq}$ is the cross-coupling term, since multiplication with j makes the d-axis end up on the q-axis and vice versa.

The first step is cancelling the cross-coupling. It can easily be done by adding a decoupler, $j\omega L_s \underline{i}_{dq}$. It is assumed that L is known with rather high accuracy. In Fig 3.5 the complete control system is presented as a block scheme. The input signal v_p is selected as

$$\underline{v}_{pdq}(t) = \underline{v}'_{pdq}(t) - j\omega L_s \underline{i}_{dq}(t) \tag{3.26}$$

By doing this Equation (3.15) can now be written as

$$\underline{v}'_{pdq}(t) = -R_s \cdot \underline{i}_{dq}(t) - L_s \cdot \frac{d\,\underline{i}_{dq}(t)}{dt} + \underline{v}_{sdq}(t) \tag{3.27}$$

This equation does not have any complex valued coefficients and therefore the cross-coupling is removed.

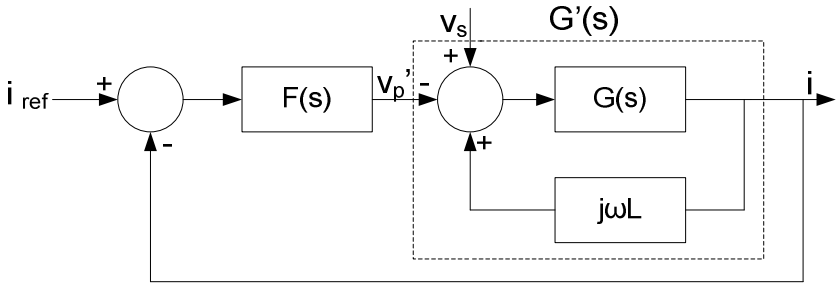

Fig 3.5 Block diagram of the current control with decoupling loop

The system function for the decoupled system is

$$G'(s) = \frac{1}{sL + R} \tag{3.28}$$

An ordinary PI controller is sufficient since the system is a first-order complex valued system.

$$F(s) = k_p + \frac{k_i}{s} = k_p\left(1 + \frac{1}{T_i \cdot s}\right) \tag{3.29}$$

The expressions for the constants can be seen in Equation (3.30) to (3.32), in [7] the derivation is presented. Equation (3.32) is used when the software for implementing of the PI controller require the proportional gain and the integral time constant.

$$k_p = \alpha \cdot L \tag{3.30}$$

$$k_i = \alpha \cdot R \tag{3.31}$$

$$T_i = \frac{k_p}{k_i} = \frac{\alpha \cdot L}{\alpha \cdot R} = \frac{L}{R} \tag{3.32}$$

where α is the closed-loop system bandwidth, k_p is the proportional gain of the controller, k_i is the integral constant and T_i is the integral time constant.

Fig 3.6 shows how the block diagram in Fig 3.5 can be implemented.

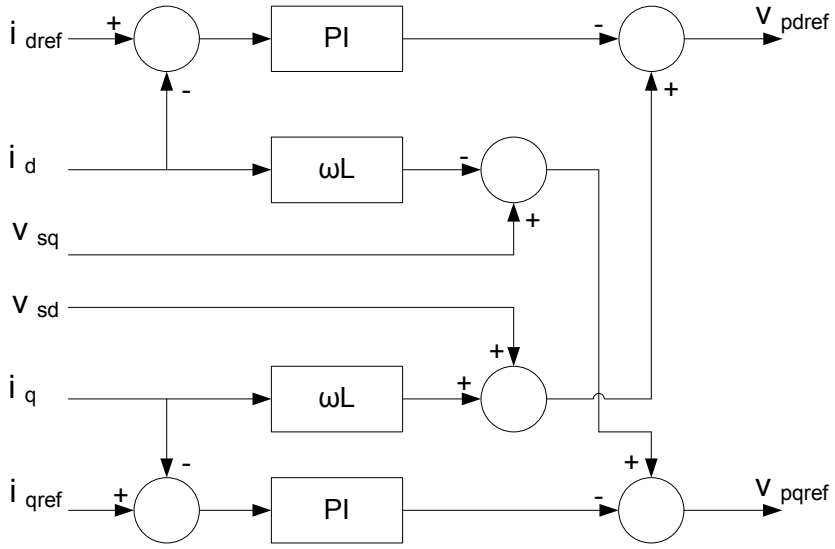

Fig 3.6 Current control and decoupling network

3.4 DC-link voltage controller

The DC-link voltage controller has only one purpose and it is to make sure that the DC-link voltage has the correct value. The output from the controller becomes the reference active current $i_{q,ref}$.

The block diagram of the DC-link voltage controller is presented in Fig 3.7. The principle of the whole control system is that the DC-link voltage controller works as outer control loop and the current vector controller works as inner control loop. The bandwidth for the current vector controller is much faster than the DC-link voltage controller, usually 10 times higher [7]. The DC-link voltage controller method of operation is to take the measured DC-link voltage V_{dc} and compare it to the reference voltage, $V_{dc,ref}$. The difference, the error, is the input to a PI controller. The output from the PI controller is a reference signal, in this case a current reference. The controller looks a bit different depending if feed-forwarding of the load current is used or not. When feed-forwarding is used the load current i_{load}, see Fig 3.8, is added together with the output signal from the PI controller. I_{load} is measured at the DC side of the VSC and is scaled and added together with the PI controller's output. The new signal becomes the output signal from the DC-link voltage controller, active current reference $i_{q,ref}$. This signal is fed to the current vector controller.

When feed-forwarding is not used the output signal from the PI controller becomes the active current reference $i_{q,ref}$ and it is fed as input to the current vector controller.

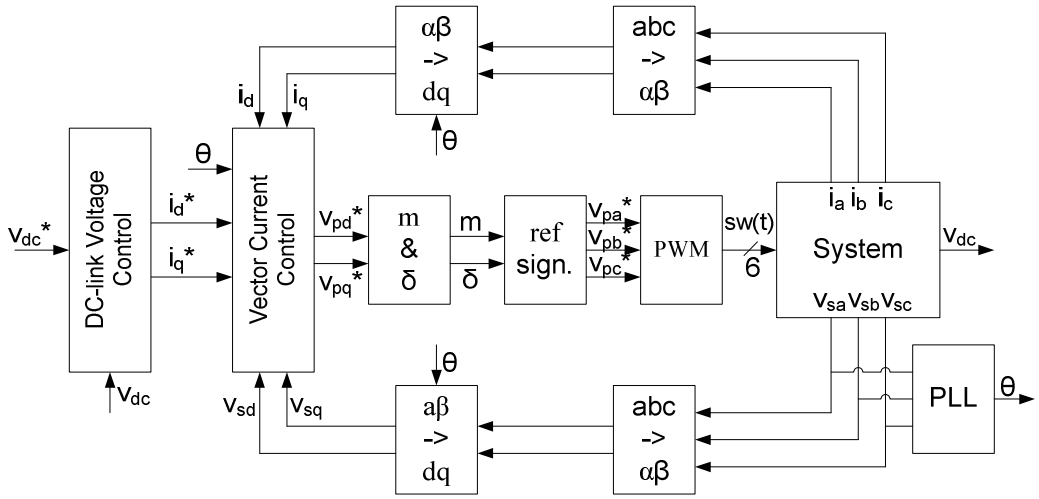

Fig 3.7 Block diagram of the whole control system

Fig 3.8 shows a block scheme over the DC controller and how the controller is build.

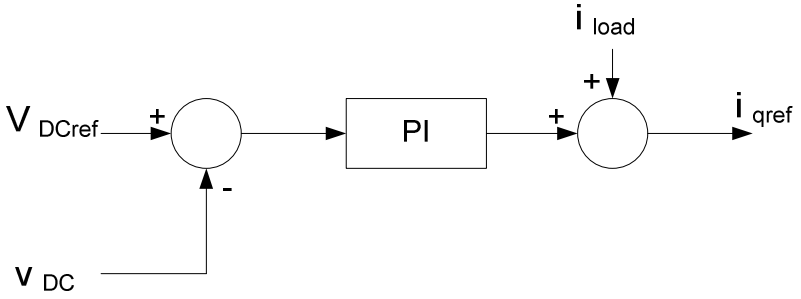

Fig 3.8 Block diagram of the DC-link voltage controller

It is possible to explain what happens at the DC side of the VSC in a mathematical way and following expressions describes this. In Section 3.3.1 the VSC is described and the expressions for both active and reactive power were derived. Those expressions are written here again to make it easier for the following calculations.

$$P_{ac} = \frac{3}{2} \cdot v_{sq}(t) \cdot i_q(t) \tag{3.33}$$

$$Q_{ac} = \frac{3}{2} \cdot v_{sq}(t) \cdot i_d(t) \tag{3.34}$$

The power on the DC side of system can be written as

$$P_{dc} = v_{DC}(t) \cdot i_{DC}(t) \tag{3.35}$$

If the losses in the converter and the RL-filter are neglected and that same amount of power is transmitted at both side of the converter it is possible with help from Equations (3.33) and (3.35) to write following

$$P_{dc} = v_{DC}(t) \cdot i_{DC}(t) = P_{ac} = \frac{3}{2} \cdot v_{sq}(t) \cdot i_q(t) \tag{3.36}$$

With help from Kirchhoff's current law the following expression can be written about the currents at the DC side.

$$i_{dc}(t) = i_C(t) + i_{load}(t) \tag{3.37}$$

We also know that the capacitors current can be written as

$$i_C(t) = C \cdot \frac{d}{dt} v_{DC}(t) \tag{3.38}$$

By inserting Equation (3.38) into Equation (3.37) the following equation is given

$$i_{DC}(t) = C \cdot \frac{d}{dt} v_{DC}(t) + i_{load}(t) \tag{3.39}$$

Equation (3.39) is inserted into Equation (3.36) and that gives

$$v_{DC}(t) \cdot \left(C \cdot \frac{d}{dt} v_{DC}(t) + i_{load}(t) \right) = \frac{3}{2} \cdot v_{sq}(t) \cdot i_q(t) \tag{3.40}$$

It can be rewritten as

$$\frac{d}{dt} v_{DC}(t) = \frac{3}{2} \cdot \frac{v_{sq}(t) \cdot i_q(t)}{v_{DC}(t) \cdot C} + \frac{i_{load}(t)}{C} \tag{3.41}$$

Equation (3.41) describes the DC voltage variations.

The current vector controller is much faster than the DC voltage controller and therefore can it be assumed that the currents i_d and i_q are equal to its reference values.

$$i_q(t) = i_{q,ref}(t) \tag{3.42}$$

By rewriting Equation 3.41, the reference active current $i_{q,ref}$ can be calculate as

$$i_{q,ref}(t) = \frac{2}{3} \cdot \frac{v_{DC}(t)}{v_{sq}(t)} \cdot \left(C \cdot \frac{d}{dt} v_{DC}(t) + i_{load}(t) \right) \tag{3.43}$$

3.5 Simulation

In this section the results concerning controllers' performance will be presented. To verify the controllers' performance the simulation program PSCAD/EMTDC was used. In Appendix B the simulation models are described together with pictures. The purpose of the simulations was to test the controllers' dynamics and it was done by exposing them with step response test.

3.5.1 Current vector controller

In this section the results for the current vector controller, which is described in Section 3.3, is presented. The parameters of the system and the control parameters that were used in the simulation can be seen in Table 3.1 and Table 3.2.

Table 3.1 System parameters used in the simulation model

Source Voltage (line-to-line RMS)	V_s	41.3 kV
DC-link Voltage	V_{dc}	75 kV
Filter Resistance	R_s	2 mΩ
Filter Inductance	L_s	0.02 H
Capacitance	C	500 μF
Grid frequency	f	50 Hz
Switching frequency	f_{sw}	2 kHz

Table 3.2 Parameters of the current vector controller used in step response simulation

Proportional gain	K_{pi}	15
Integral time constant	T_i	0.002 s

A step pulse, the amplitude varies between 0 A and 1 kA and the step length is 0.2 s, is given to the active current reference $i_{q,ref}$ while the reactive current reference $i_{d,ref}$ is kept constant at 0 A. The response of the active and reactive currents, i_q and i_d, are shown in Fig 3.9.

Another step pulse, with amplitude varying between 0 A and 1 kA and with step length of 0.2 s, is given to the reactive current reference $i_{d,ref}$ while the active current reference $i_{q,ref}$ is kept constant at zero A. The response of the active and reactive currents, i_q and i_d, is shown in Fig 3.10.

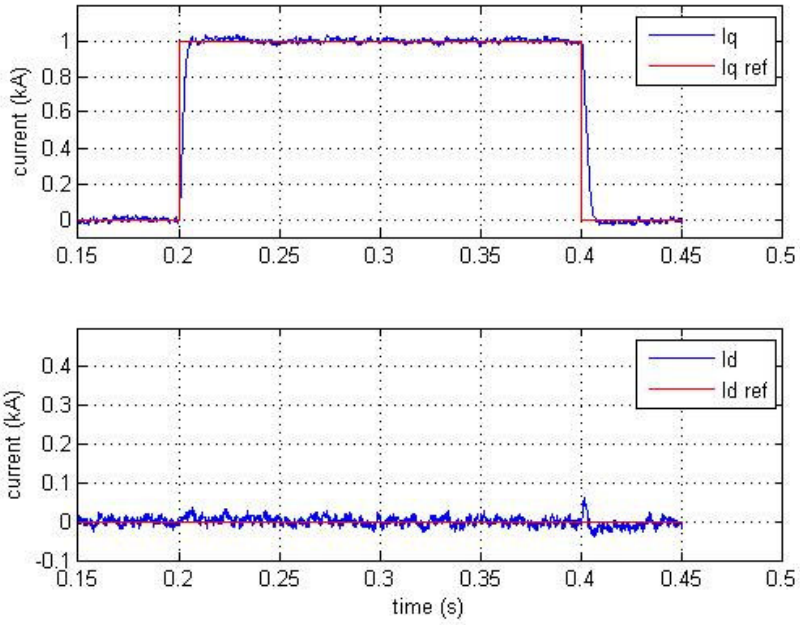

Fig 3.9 Responses of the real and reactive current, i_d and i_q, with a step pulse given to active current reference i_q^*. The magnitude varies between 0 and 1 kA and the pulse width is 0.2 s, while the reactive current reference i_d^* is kept at 0 A.

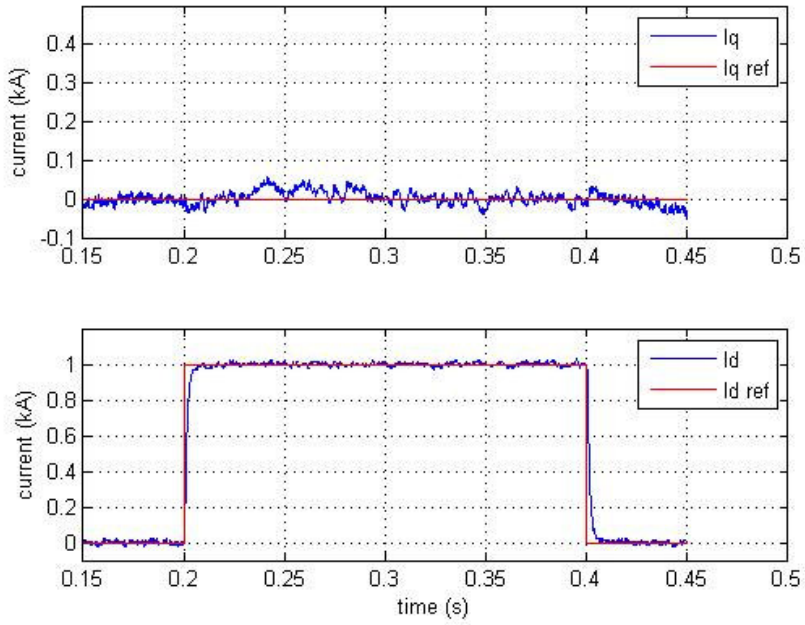

Fig 3.10 Responses of the real and reactive current, i_d and i_q, with a step pulse given to reactive current reference i_d^*. The magnitude varies between 0 and 1 kA and the pulse width is 0.2 s, while the reactive current reference i_q^* is kept at 0 A.

As shown in Fig 3.9 and Fig 3.10 the current vector controller works as expected. In both cases the current reach the reference values within reasonable time. A small cross-coupling can be seen and also some oscillations, which is a consequence of the switch devices. The harmonics lie around the switching frequency and can be reduced with an ac filter. However, there will always be a small amount of harmonics in the signals.

3.5.2 DC voltage controller

In this section the results for the DC-link voltage controller, which was derived in Section 3.4, is presented. In this simulation a DC current source is used instead of the two voltage sources, which was used in the simulation in Section 3.5.1. The current source is used to simulate the load current and by changing its value a load disturbance is received. The system parameters and the control parameters were used in the simulation can be found in Table 3.3 and Table 3.4.

Table 3.3 System parameters used in the simulation model

Source Voltage (line-to-line RMS)	V_s	41.3 kV
DC-link Reference Voltage	$V_{dc\ ref}$	75 kV
Filter Resistance	R_s	2 mΩ
Filter Inductance	L_s	0.02 H
Capacitance	C	500 μF
Grid frequency	f	50 Hz
Switching frequency	f_{sw}	2 kHz

Table 3.4 Parameters of the Current Vector Controller (CVC) and DC-link controller used in step response simulation

Proportional gain, CVC	K_{pi}	15
Integral time constant, CVC	T_i	0.002 s
Proportional gain, DC-link	K_{pdc}	0.1
Integral time constant, DC-link	T_{idc}	0.1 s

The simulation was done by changing the current value from 0.1 kA to 0.5 kA when t=0.3. In this way a load change was simulated and this tested if the controller's dynamic could handle it. The simulation was done in two different ways, the first simulation had no feed-forwarding of the load current and the second simulation feed-forwarding of the load current was used. In Fig 3.11 the DC-link voltage is shown, when no feed-forwarding is used and Fig 3.12 shows the DC-link voltage then feed-forwarding is used.

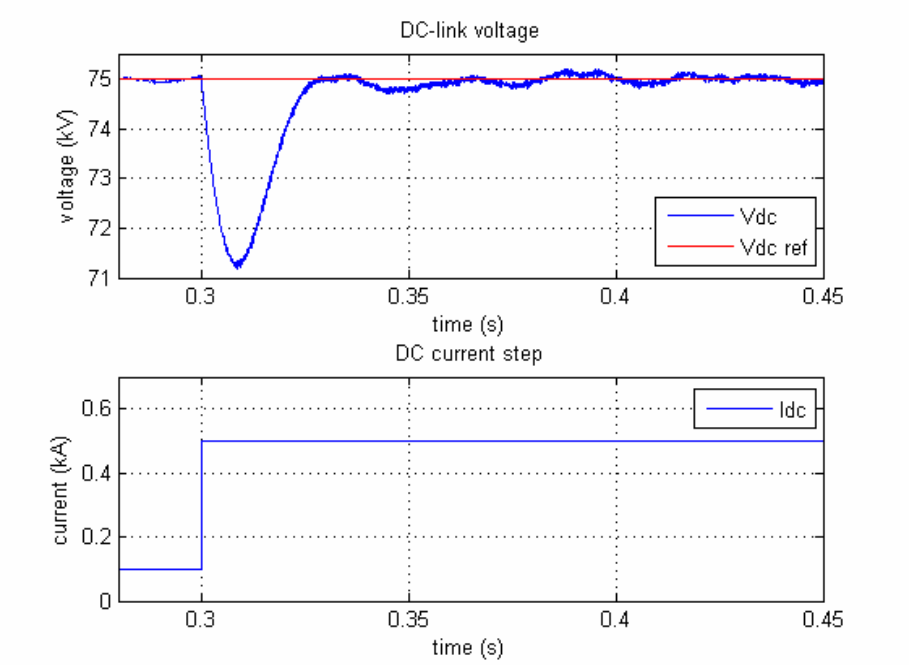

Fig 3.11 Dynamic response of the DC-link voltage controller at load current step from 0.1 kA to 0.5 kA, without feed-forwarding.

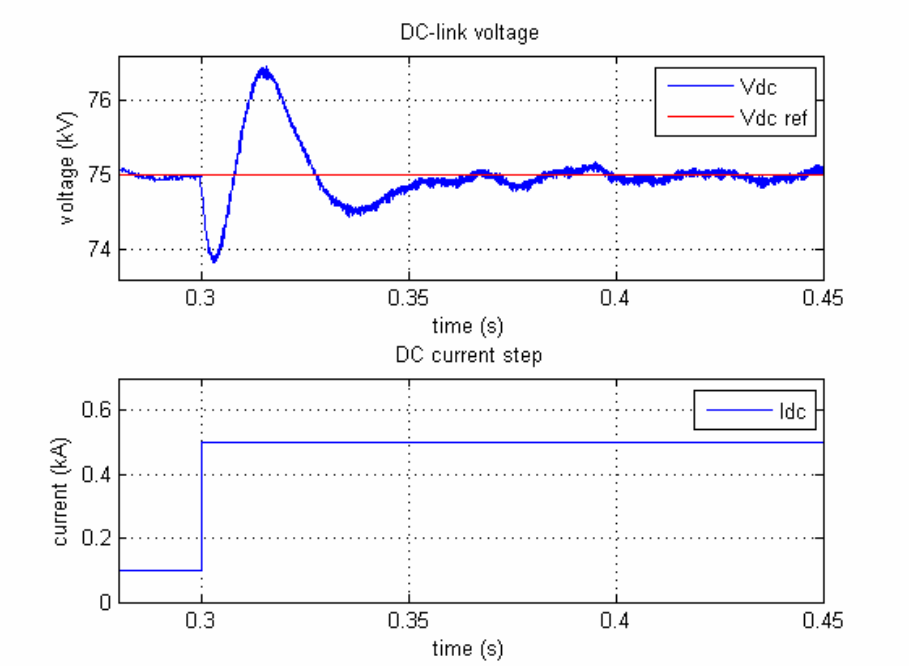

Fig 3.12 Dynamic response of the DC-link voltage controller at load current step from 0.1 kA to 0.5 kA, with feed-forwarding.

In Fig 3.11 and Fig 3.12 it can be seen that there is a difference whether feed-forwarding of the load current is used or not. Without feed-forwarding, Fig 3.11, a deeper dip is given and it reaches down to approximately 71.5 kV. When feed-forwarding, Fig 3.12, is used the dip reaches to approximately 76.5 kV but now there is also an overshoot in the DC-link voltage. The demand of the system decides what variant should be used. If an overshoot can be acceptable perhaps feed-forwarding of the load current would be a good choice. It will result in a smaller dip but with larger oscillations in the voltage. The most likely choice is without feed-forwarding, due to the fact that oscillations in the DC-link voltage are not wanted. The voltage dip in this case is also relative small.

3.6 Summary

In this chapter a three-phase voltage source converter has been discussed. This has included information about how it works and control issues have been addressed. Furthermore a current vector controller and a DC-link voltage controller have been derived and these systems have then been tested with simulations in PSCAD/EMTDC.

The performance for the control system has been tested by studying the step response for the current vector controller. It was shown that the current vector control functioned as expected. The vector DC-link voltage controller's dynamic was tested through shifting the load current and studying the voltage variations. This test was done with two different control systems, with and without feed-forwarding of the load current. It was shown that the result was better without feed-forwarding, since with feed-forwarding the DC-link voltage had both a dip and an overshoot.

4 Four voltage source converters connected in series

4.1 Introduction

In Chapter 3 one voltage source converter was presented that could be used for transfer of power. It consisted of six transistors interconnected together with three series RL filters, see Fig 3.1. This setup works very well when the demand regarding volume is small but in some cases volume cost a lot of money. If it is possible to decrease the volume new market will be open.

In this chapter a different technique which is a further development of the VSC in Chapter 3 is presented. Instead of having a single VSC per terminal now N_m numbers of converters are connected in series. In this thesis N_m is equal to four. In Fig 4.1 such a circuit can be seen and in Fig 4.2 the VSC that is used can be seen. The transformer is series connected on the grid side and that creates a multilevel voltage waveform. The multilevel voltage waveform gives the benefit that filter rating can be kept low and it saves volume. Furthermore the converters are directly interconnected with the transformer, which can be seen in Fig 4.2. In this way the phase reactor has been eliminated and it saves space and footprint. The drawbacks of this connection are: 1) Square Voltage waveforms, 2) Transformer stresses, 3) DC-link voltage balance.

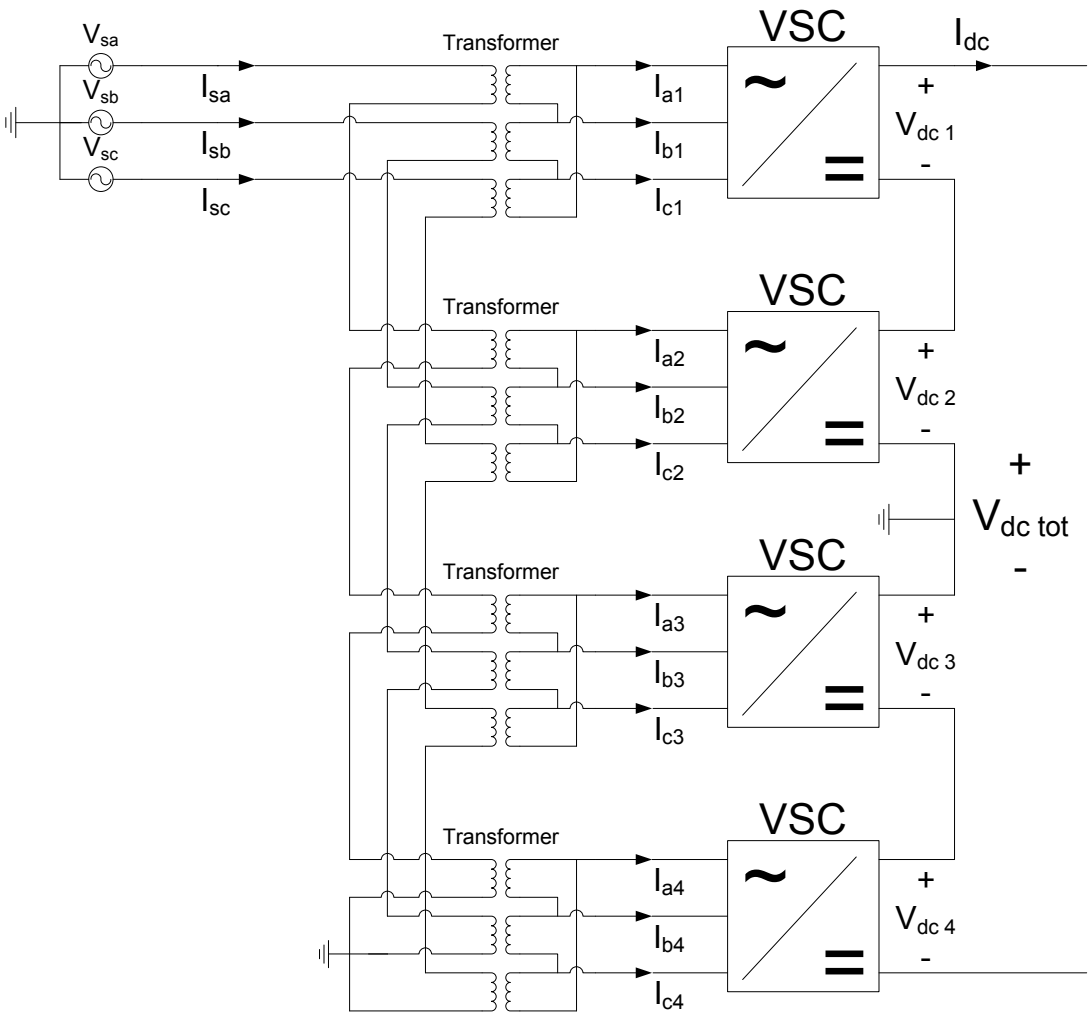

Fig 4.1 Circuit with four VSC connected in series together with transformers and grid source

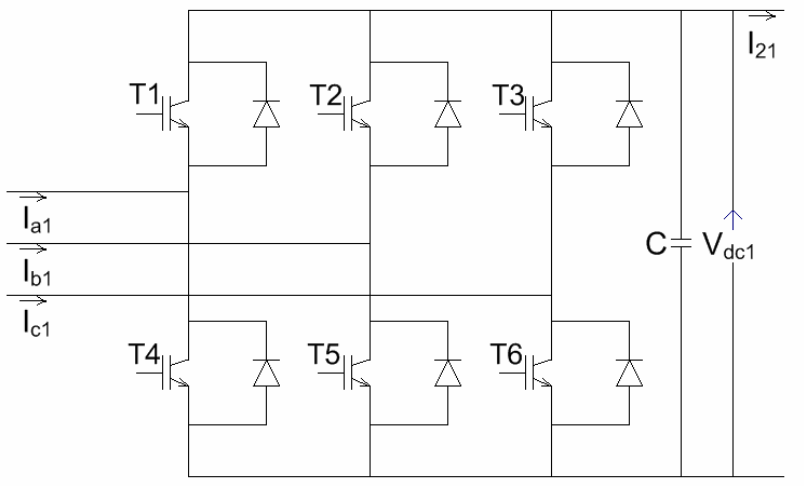

Fig 4.2 Voltage source converter which is used in the circuit

By connecting the VSC in series harmonic elimination by phase shifting can be used. With phase shifting means that the carrier wave for the PWM's is evenly phase shifted. This lead to less THD (Total Harmonic Distortion) for the system and it saves filter rating. There are also other advantages with this series connection. The PWM technique has always been associated with high switching frequency causing higher switching losses. This connection makes it possible to reduce the switching frequency for each converter since the equivalent carrier wave frequency for the whole system is equal to $N_m \cdot K_c$, where K_c is the carrier wave frequency for the converters [9]. For example, if an equivalent carrier wave frequency of 2 kHz for the whole system is wanted and the number of converters is four, then the carrier wave frequency for each converter is equal to 0.5 kHz. This results to a significant reduction of the switching losses and it is possible to increase the number of converters, N_m, and decrease the converters carrier wave frequency, K_c, even more.

Fig 4.3 shows one of the grid currents when four VSC connected in series and a single VSC are used respectively.

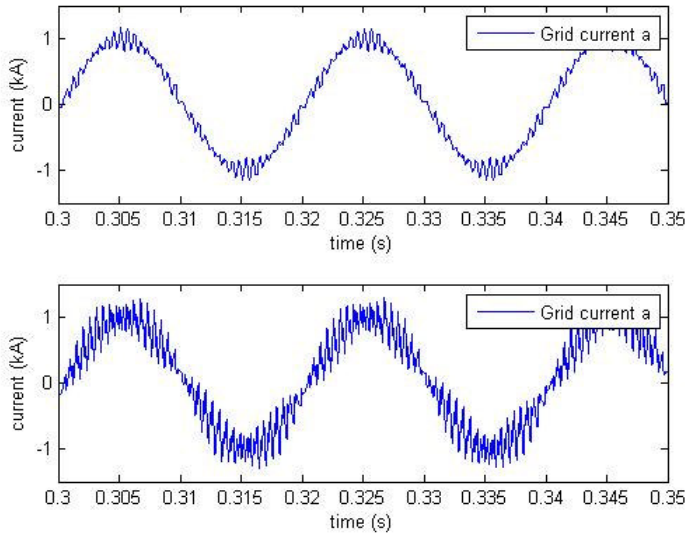

Fig 4.3 Grid currents
Upper figure: Grid current for four VSC connected in series
Lower figure: Grid current for a single VSC

In both simulations the same phase reactor value has been used and the reduction of THD is easily seen in fig x. The current seen in the lower figure contains more oscillations than the current in the upper figure.

4.2 Circuit

The circuit in Fig 4.1 has some similarities with the circuit that is used in Chapter 3. Each voltage source converter looks the same except from the phase reactor. The needed inductance for the circuit is supplied by the leakage inductance of the transformer and the mathematical expressions are the same. A distinction can be seen on the DC side of the circuit. The voltage source converters are connected in series resulting to a bit different expressions for the DC quantities. The total DC-link voltage can be expressed as

$$V_{dc\,tot} = \sum_{n=1}^{N_m} V_{dc\,n} \tag{4.1}$$

where V_{dcn} is the DC voltage across the capacitor of the converter.

Applying Kirchhoff's Current law results

$$C_n \cdot \frac{d}{dt} V_{dc\,n} = i_{1n} - i_{2n} \tag{4.2}$$

where i_{1n} is the current through the transistors and i_{2n} is the current output from each VSC.

The output current i_{2n} is common through each unit [8].

$$i_{2n} = i_{dc} \ , \quad n = 1, 2, ..., N_m \tag{4.3}$$

The power from the DC side is calculated as

$$P_{dc} = i_{dc} \cdot \sum_{n=1}^{N_m} V_{dc\,n} \tag{4.4}$$

4.2.1 PWM

In this circuit Sinusoidal PWM (SPWM) is used and it is described in Section 3.2. In this case there are four converters, i.e. 24 transistors. This can be seen as twelve transistor pairs and these should be controlled with PWM technique. Each transistor pair needs a PWM module to determine the switching pattern for the two transistors. As mentioned in paragraph 4.1 a technique called phase shifted carriers are used. This technique works by phase shifting the carrier wave for each converter. For converter 1 the phase shifting is zero, converter 2 has a phase shifting of 90 degrees, converter 3 has a phase shifting of 180 degrees and converter 4 has a phase shifting of 270 degrees. Fig 4.4 shows how the four carrier waves for one of the phases and the phase shift can easily be seen.

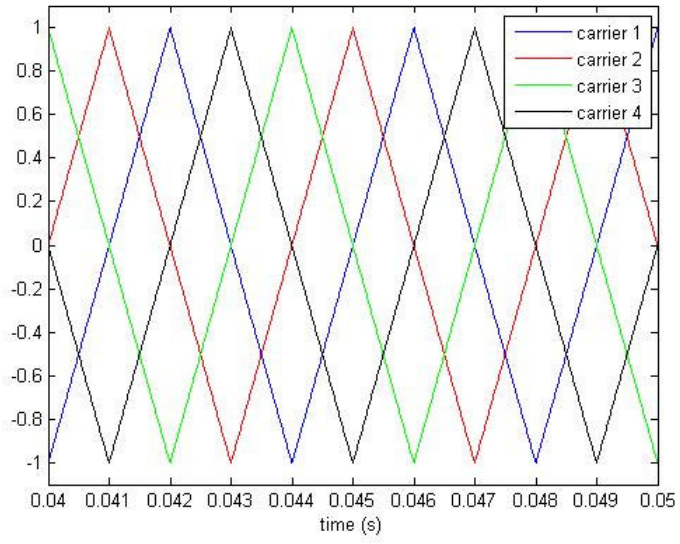

Fig 4.4 Phase shifted carrier waves for harmonic elimination

This phase shifting can be described mathematically as

$$\theta_i = \frac{360}{N_m} \cdot (i-1) \ , i = 1,2,...,N_m \tag{4.5}$$

where N_m is the total number of converters.

To get the most out of this PWM technique a low as possible K_c value should be chosen, reducing the switching losses. Thus the ratio K_c/K_m, there K_m is the fundamental sinus wave, should be as low as possible.

Comparably low value creates lower sideband harmonics that can appear in the DC voltage [9]. In [9] a bench marking between the different K_c/K_m ratios is presented and the merits of the demerits of the different ratios are stated. High K_c/K_m ratio will lead to filter reduction but to keep the advantages with switching losses the ratio must be kept to a minimum. A lot of factors are necessary to take in to account when choosing switching frequency, for instance how many converters Nm should be used, the equivalent switching frequency for the whole system, K_c/K_m ratio, switching losses.

To each PWM module a reference signal is compared with Kc. In Fig 4.5 it can be seen how the switching pattern is determined. It is possible to increase the performance of the PWM by adding third harmonic content, if the three-phase system is with floating neutral. Since zero sequence components in the output voltage of a converter do not result in corresponding currents. This can give an increase of 15 percent in performance but is not used in this thesis.

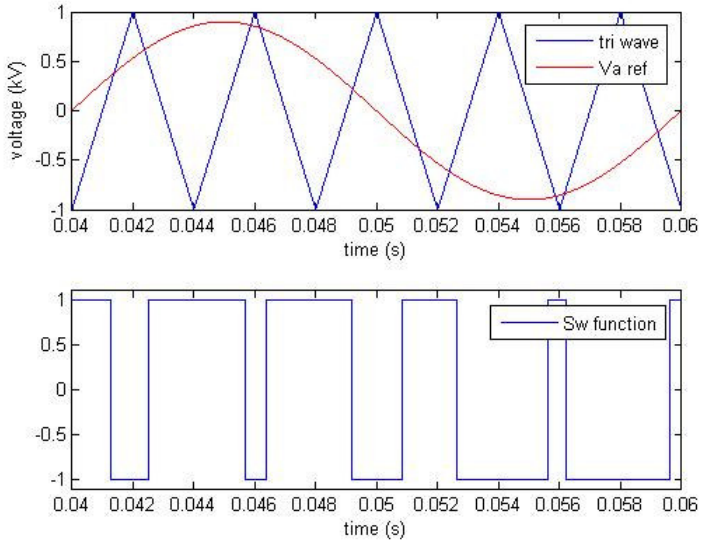

Fig 4.5 SPWM control of a phase and nth converter.
Upper figure: Carrier wave and modulation signal.
Lower figure: Switching function

4.3 Control systems

The purpose of the control system is to control the DC-link voltage and it is done by controlling the transistors, as mentioned in Chapter 3. The control system should have an inner control loop that controls the d and q-component of currents and an outer control loop which controls the DC-link voltage. There is a difference with control system used now compared to the system described in Chapter 3. There are 24 transistors and also the connections are different and this makes the control system more complex. Two different control systems will be discussed, control model A and control model B. Control model A is build in way that only one controller for the currents and one for the DC voltages is needed. Control model B on other hand consist of four controllers for the currents and four for the DC voltages, i.e. the converters are controlled individually.

4.3.1 Control model A

Control model A consists of a single control system for the whole converter circuit. It works in such a way that the four converters are seen as a single large converter. The only thing that is of interest for the control system is the inputs and the outputs from the converter circuit, i.e. grid voltage, grid currents and DC-link voltage. The control system described in Chapter 3 is used in this model but the series connected transformer must be considered. There are 24 transistors that need to be controlled and it is done by comparing all PWM modules with the same reference voltage. The carrier waves for the PWM modules are of course still evenly distributed, see Section 4.2.2. With only one controller the complexity of the control system is reduced and only two currents, I_{sd} and I_{sq}, and one DC-link voltage, V_{dc_tot}, should be controlled. A drawback of this control model is that is not possible to control the DC voltage for each converter. This can lead to unbalance at the DC side of the circuit. The DC-link voltage may be following the reference value but is not uniformly distributed over the four converters. The DC voltage for one converter may increase and another decrease with the same amount. It is possible that the unbalance affects the whole circuit and its performance needs further investigation. The control model consists of two parts, a current vector controller and a DC-link voltage controller, as shown in Fig 4.6.

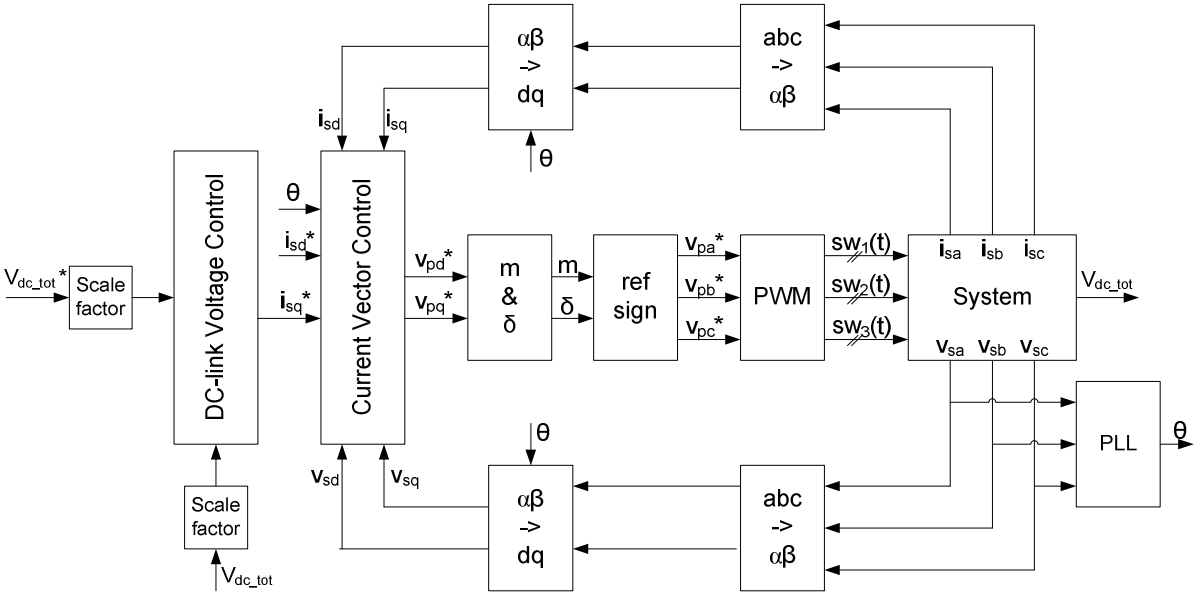

Fig 4.6 Block scheme over control model A

Inputs to the current vector controller are the filtered grid voltages, grid current and reference currents I_{sd}^* and I_{sq}^*. The grid currents and the grid voltages go through two processes before becoming inputs to the current vector controller. First they are transformed to the αβ-frame and after that they are transformed to the rotating dq-frame. The filtered grid voltages are also inputs to the Phase-Locked Loop (PLL) and can determine the vector which is used for the synchronisation of the dq-frame. In this case the synchronisation is done in such a way that the grid voltage vector follows the q-axis. The grid voltage vector consists of only the q-component. The q-component of the current is the active part and the d-component is the reactive part.

The outputs from the current vector controller are two signals, V_{pd}^* and V_{pq}^*. It is the d and q-component of the VSC reference voltage. They are inputs to the block which calculates the modulation index, m, and the load angle, δ. The modulation index and the load angle are used in the calculation of the reference three-phase voltages that is used to determine the switching pattern. The reference voltages compared to the PWM block and transistors gate signals are created.

The second part of the control system is the DC-link voltage controller and its inputs are the reference DC-link voltage and the actual DC-link voltage. The signals are scaled and fed to the controller due to the transformer which is used in the circuit. Both the grid voltages and the grid currents are measured

at the grid side of the transformer. The DC-link voltage is measured at the converter side of the transformer and therefore needs to be scaled. The scaling factor consists of two parts, the transformer ratio and a connection factor. The connection factor depends on how the transformer is connected. If the converter side of the transformer is connected in a delta connection the connection factor becomes $\sqrt{3}$.

The output from the DC-link voltage controller is the reference grid current I_{sq}^{*}.

The blocks in Fig 4.6 exist in only one copy beside the blocks that calculates the three-phase voltages reference and the PWM block. These two blocks exist in four copies, since every VSC needs an individual PWM module.

Current vector control

The task for the current vector controller is to control the grid currents so that they follow the reference values. Fig 4.7 shows the block diagram for the current vector controller, which has a decoupling term. There is no difference with this controller compared to the one described in Section 3.3.

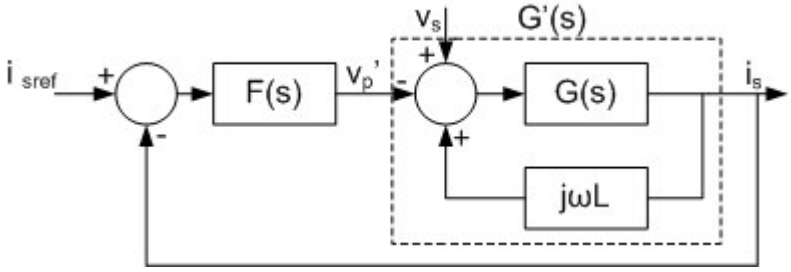

Fig 4.7 Block diagram for the current vector controller used in control model A

The two inputs to the current vector controller are compared and the difference is fed to the PI controller. A decoupling term and the grid voltage are then added to the PI controller's output. The new signal is the current vector controller's output.

The implementation of the current vector controller in this case is presented in Fig 4.8.

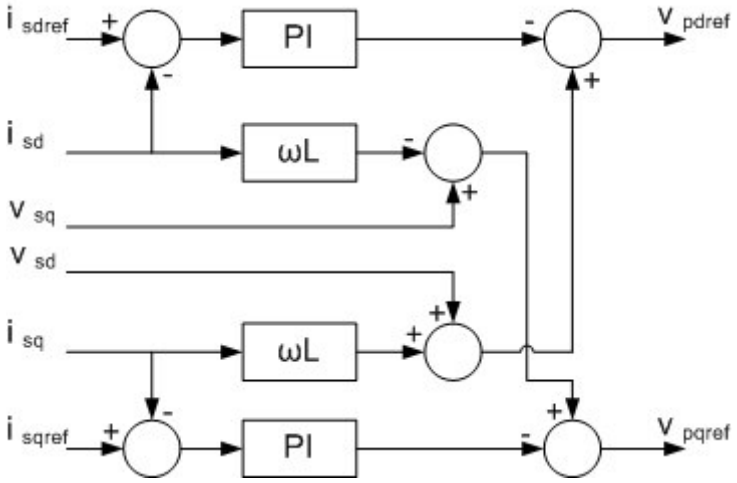

Fig 4.8 Implementation of the current vector controller used in control model A

DC-link voltage control

The DC-link voltage controller's purpose is to control the DC-link voltage so that the reference value is reached. Fig 4.9 shows the block diagram for the DC-link voltage controller and it does not differ from the DC-link voltage controller which was presented in Section 3.4.

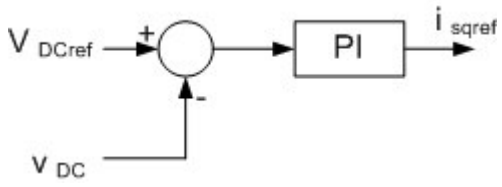

Fig 4.9 Block diagram for the DC-link voltage controller used in control model A

The DC-link voltage controller output is the reference grid active current I_{sq}^{*}, which is the input to the current vector controller. The controller's input is the reference DC-link voltage and the measured DC-link voltage.

4.3.2 Control model B

Control model B is slightly different from the control model A. This gives a more complex system and everything should in this case be done four times. In the control model A the four converters was seen a single converter but not here. This makes it possible to control the DC voltage for each converter individually and avoiding the unbalance that can arise in the control model A. However the grid currents are not controlled directly since the converter currents are controlled.

This model has similarities with the model in Chapter 3 but now four of those models are used. Fig 4.10 shows the block scheme for the control model B.

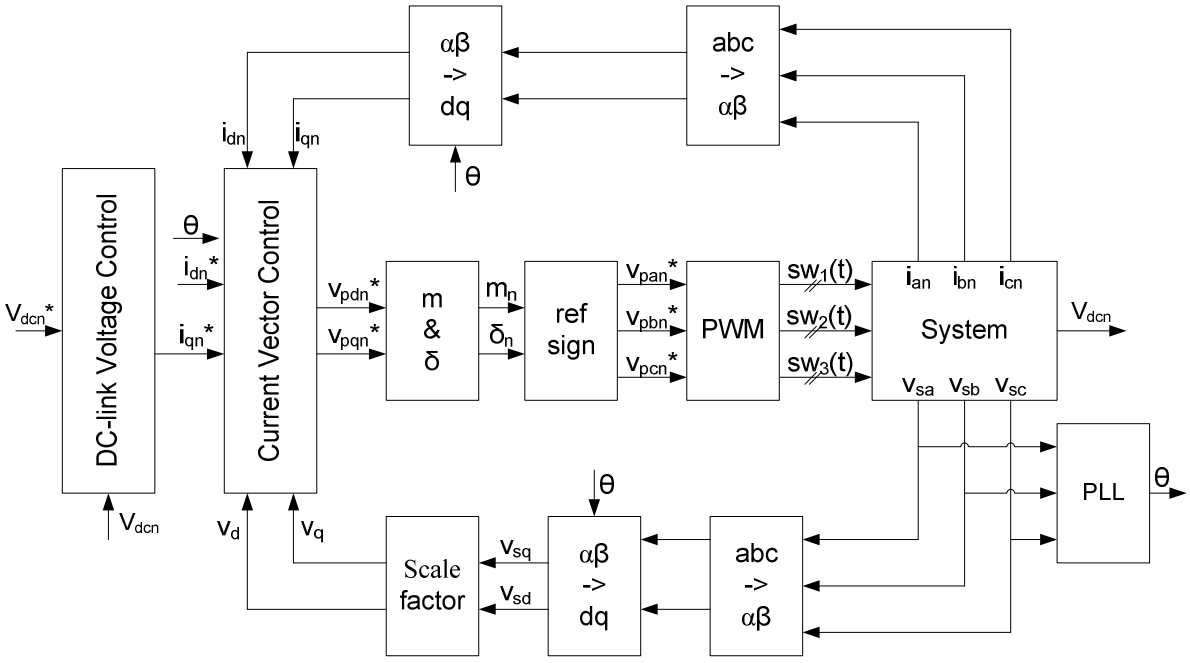

Fig 4.10 Block scheme for control model B

As can be seen in Fig 4.10 there are some similarities between control model A and B. Still the filtered grid voltages are inputs to the PLL, which calculates the synchronisation vector that is used in the dq transformation. The synchronisation is done so that the grid voltage vector follows the q-axis and therefore consists of the q-component. The inputs to the current vector controller are the converter currents, the filtered grid voltages and the reference converter currents. Both the converter currents and the grid voltages are transformed twice, first to the αβ-frame and secondly transformed to the dq-frame.

The outputs of the current vector controller are the d and q-components reference voltage. Those are inputs to the block where the modulation index, m, and the load angle, δ, are calculated. They are then inputs to calculation of the three-phase voltages that are inputs to the PWM module. From the PWM module the gate signals are calculated and the switching pattern of the system is determined.

The second part of the control system is the DC-link voltage controller and its inputs are the reference voltage and the measured DC voltage. The output from the controller is the active converter current reference.

The majority of the blocks in Fig 4.10 are needed for each converter and exist in this case in four copies. The only blocks that are needed in one copy are the grid voltage blocks and it is the PLL-block and the blocks where the calculation of the DC quantities of the grid voltages is done.

Current vector controller

The purpose of the current vector controller is to control the converter currents so that the reference value is always kept. In Fig 4.11 the block diagram for the current vector controller can be seen and it has a decoupling part. This current vector controller has no difference with the controller presented in Chapter 3.3.

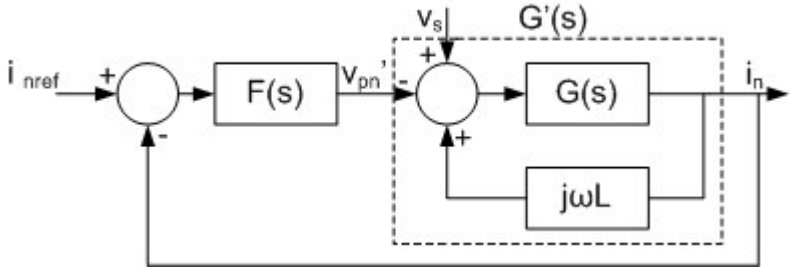

Fig 4.11 Block diagram for the current vector controller used in control model B

The input to the PI controller is the current error and to the output from the PI controller a decoupling term and the gird voltage are added. The implementation of the current vector controller is this case can be seen in Fig 4.12.

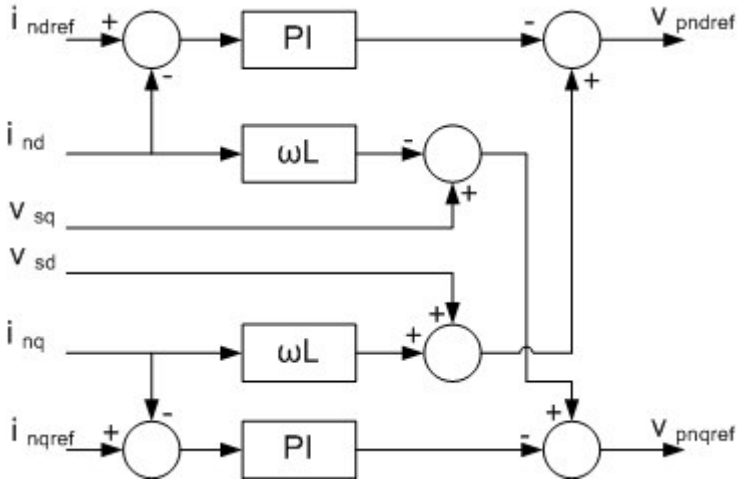

Fig 4.12 Implementation of the current vector controller used in control model B

DC-link voltage controller

The purpose for the DC-link voltage controller is to control the DC voltage for the converter so that the reference value is reached. A block diagram of the DC-link voltage controller can be seen in Fig 4.13 and is explained in Chapter 3.4.

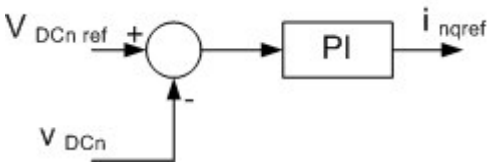

Fig 4.13 Block diagram for the DC-link voltage controller used in control model B

The input signal to the DC-link voltage controller is the reference DC voltage and the measured DC voltage of the converter. The difference between them is the input to the PI controller and out from the PI controller comes the reference active current of the converter. That is also the output from the DC-link voltage controller.

4.4 Summary

In this chapter a further development of the VSC from Chapter 3 has been presented. Instead of have only one single VSC per terminal there is now a number of VSCs connected in series. This gives the possibility to minimise the volume of the system since the required filter capacity is minimised. In this case the volume is reduced when no phase reactors are used. The PWM technique that is used was also described. Finally two different control methods were presented. The first control model disregards the fact that there are several converters connected in series and instead the whole circuit is treated as a big VSC. In this way the control system only consist of one current vector controller and one DC-link voltage controller. The second control model uses a current vector controller and a DC-link voltage controller for each VSC.

5 Simulation and testing of the different control models

In Chapter 4 a circuit with four VSCs connected in series and two control models were presented. The response of the two control systems are tested by using the simulation program PSCAD/EMTDC. The test is divided in two parts: First test of the current vector controller and, 2) test of the DC-link voltage controller. The current vector controller must work as thought otherwise the DC-link voltage controller will not work. The current vector controller is the inner controller. The simulation models can be seen in Appendix C, control model A, and Appendix D, control model B. The system parameters used in the simulations are presented in Table 5.1.

Table 5.1 System parameters used in the simulation

Source Voltage (line-to-line RMS)	V_s	16.48 kV
DC-link Voltage	V_{dc}	300 kV
Winding number 1	N_1	5
Winding number 2	N_2	86.76
Filter Inductance	L_s	0.0001 H
Converter capacitance	C_n	100 μF
Grid frequency	f	50 Hz
Converter Switching frequency	f_{sw}	450 Hz

5.1 Current vector control test

The idea with this test is to see if the controller can handle step pulses. It is interest to see how quickly the reference values is reached and also if there are some problems with overshoot and oscillations. Step pulses will be applied to both i_d^* and i_q^* to study the response of the control system works.

5.1.1 Control model A

Table 5.2 shows the parameters used in the current vector controller in these step response simulations.

Table 5.2 Parameters of the current vector controller used in step response simulation

Proportional gain	K_{pi}	5
Integral time constant	T_i	0.003 s

The first test is a step pulse added to the active current reference and the magnitude is 1 kA and the pulse length is 0.1 s. The reactive current reference is kept constant at zero during the simulation. The response of the active and reactive current is shown in Fig 5.1 and the grid currents are shown in Fig 5.2.

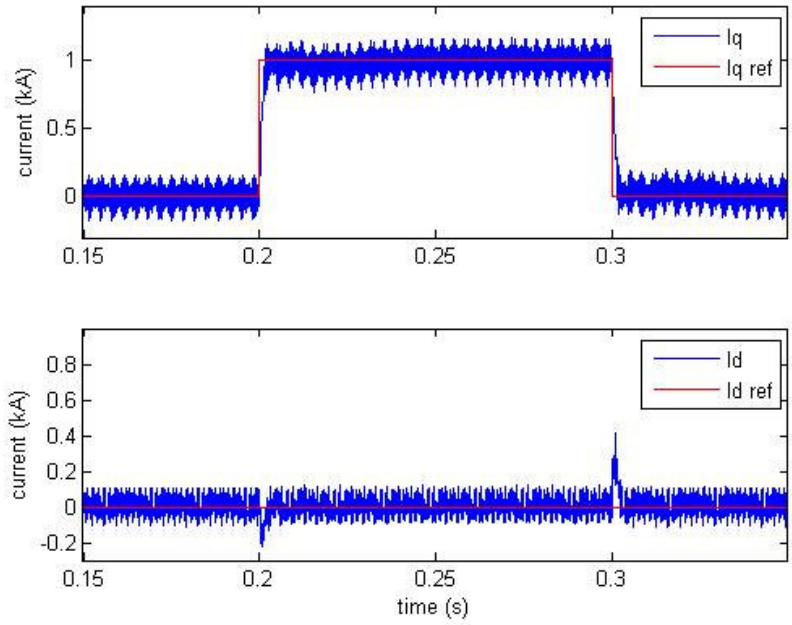

Fig 5.1 Responses of the real and reactive current, i_d and i_q, with a step pulse given to active current reference i_q^*. The magnitude varies between 0 and 1 kA and the pulse width is 0.1 s, while the reactive current reference i_d^* is kept at 0 A.

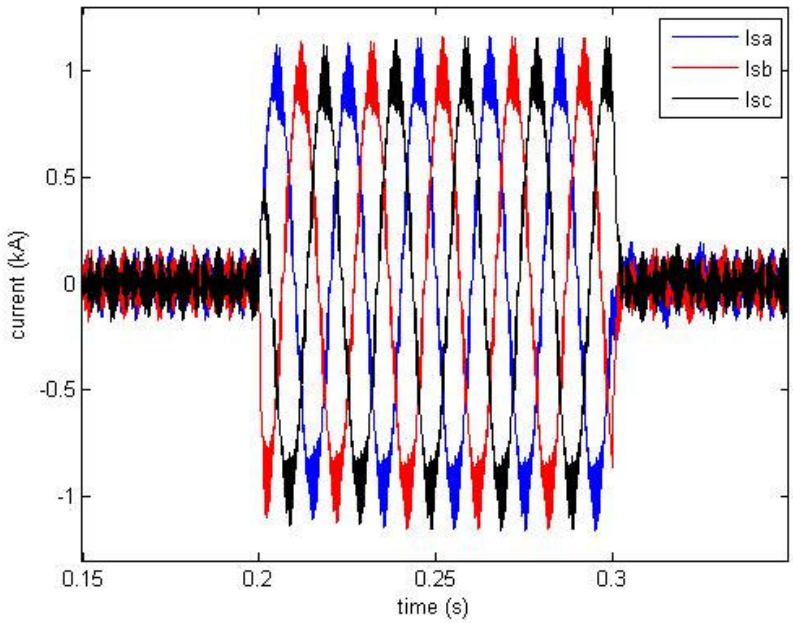

Fig 5.2 Currents I_{sa}, I_{sb}, I_{sc} during a step pulse given to active current reference i_q^*

The current vector controller works and the reference value is reached within reasonable time. Some cross-coupling can be seen in Fig 5.1 but it is rather small.

Another step pulse is given to the active current reference but now the magnitude is larger. The reactive current reference is still kept constant at zero during the simulation. In Fig 5.3 the response of the active and reactive current is shown and in Fig 5.4 the corresponding grid currents are presented.

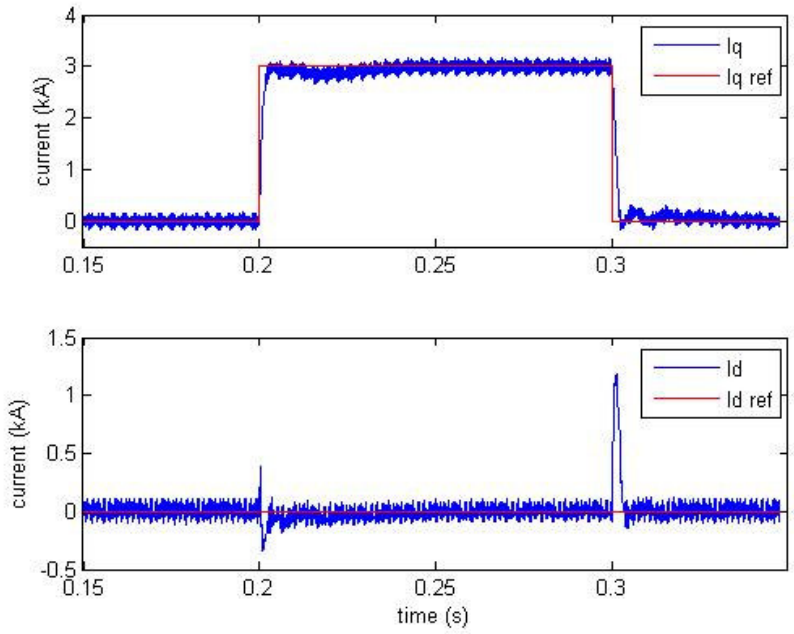

Fig 5.3 Responses of the real and reactive current, i_d and i_q, with a step pulse given to active current reference i_q^*. The magnitude varies between 0 and 3 kA and the pulse width is 0.1 s, while the reactive current reference i_d^* is kept at 0 A.

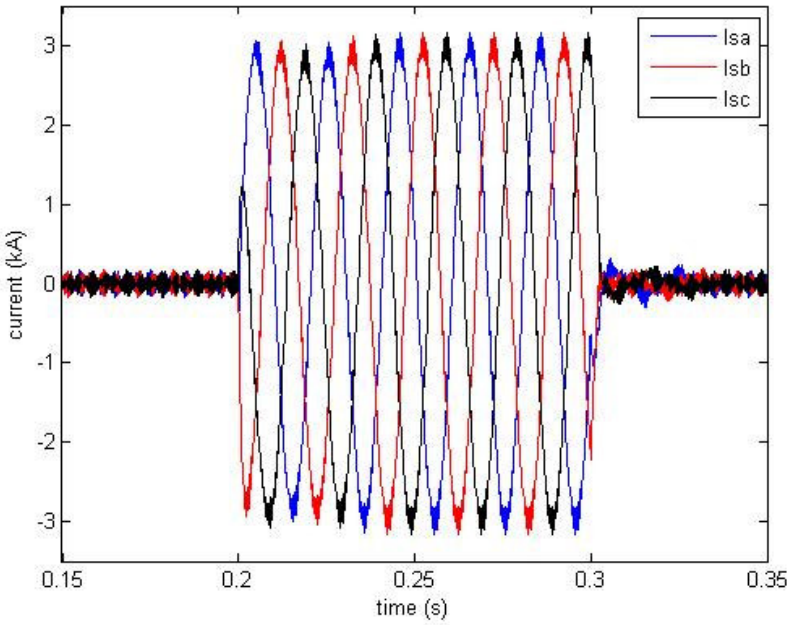

Fig 5.4 Currents I_{sa}, I_{sb}, I_{sc} during a step pulse given to active current reference i_q^*

The current vector controller works and the reference values are reached. Since the step is now higher the cross-coupling becomes larger, especially when the active current goes from 3 kA to 0 kA. At that time the reactive current is higher than 1 kA, which is a large amount reactive power.

The step response for the reactive current should now be tested. The first test is a step pulse with magnitude of 1 kA and pulse length of 0.1 s. Fig 5.5 shows the active and reactive current response and Fig 5.6 shows the grid currents during the step pulse.

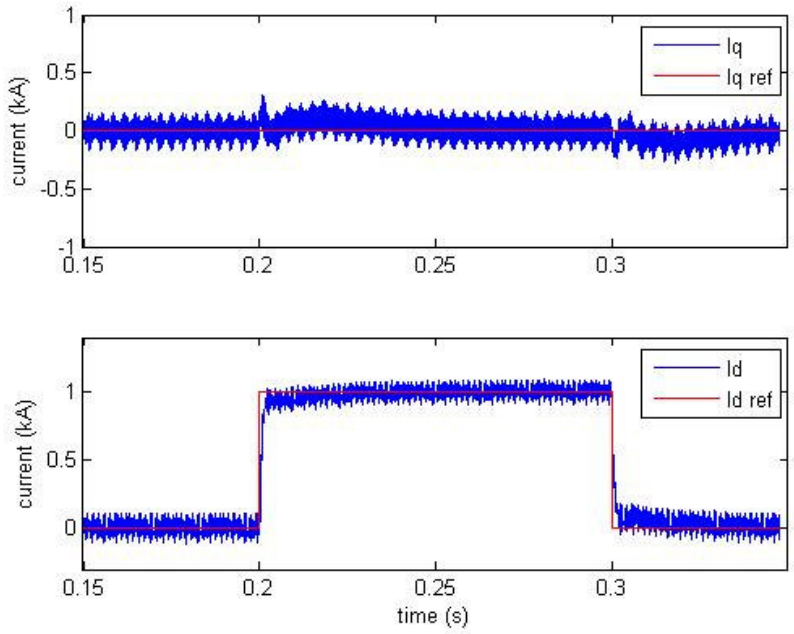

Fig 5.5 Responses of the real and reactive current, i_d and i_q, with a step pulse given to reactive current reference i_d^*. The magnitude varies between 0 and 1 kA and the pulse width is 0.1 s, while the active current reference i_q^* is kept at 0 A.

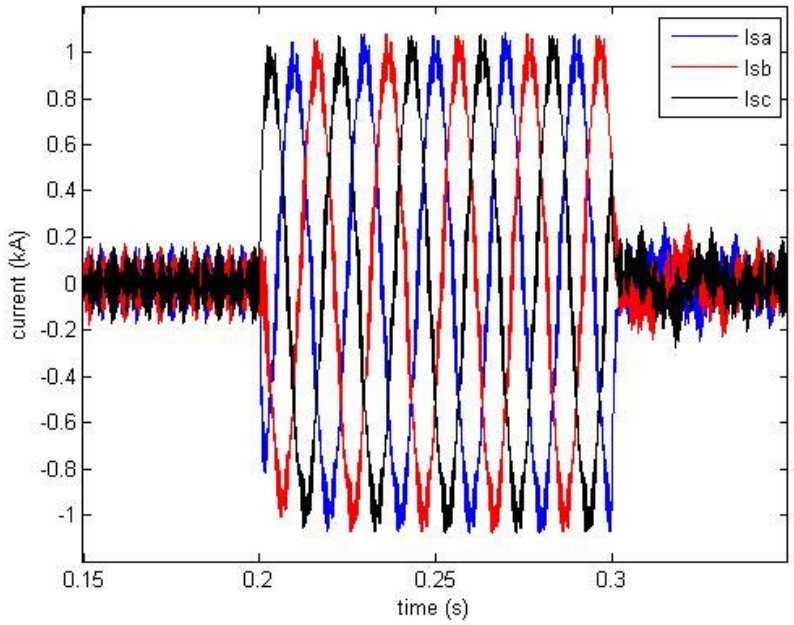

Fig 5.6 Currents I_{sa}, I_{sb}, I_{sc} during a step pulse given to reactive current reference i_d^*

The current vector controller handles also reactive current step as expected. Almost no cross-coupling can be seen and the reference value is reached in reasonably time.

The next test is to increase the reference reactive current step and the magnitude is now 3 kA. The response of the active and reactive current is shown in Fig 5.7 and the grid phase currents are shown in Fig 5.8.

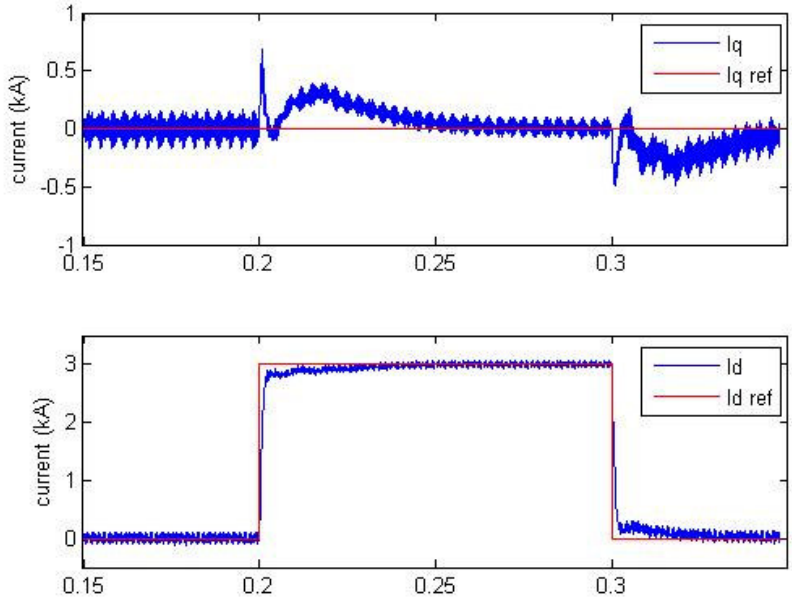

Fig 5.7 Responses of the real and reactive current, i_d and i_q, with a step pulse given to reactive current reference i_d^*. The magnitude varies between 0 and 3 kA and the pulse width is 0.1 s, while the active current reference i_q^* is kept at 0 A.

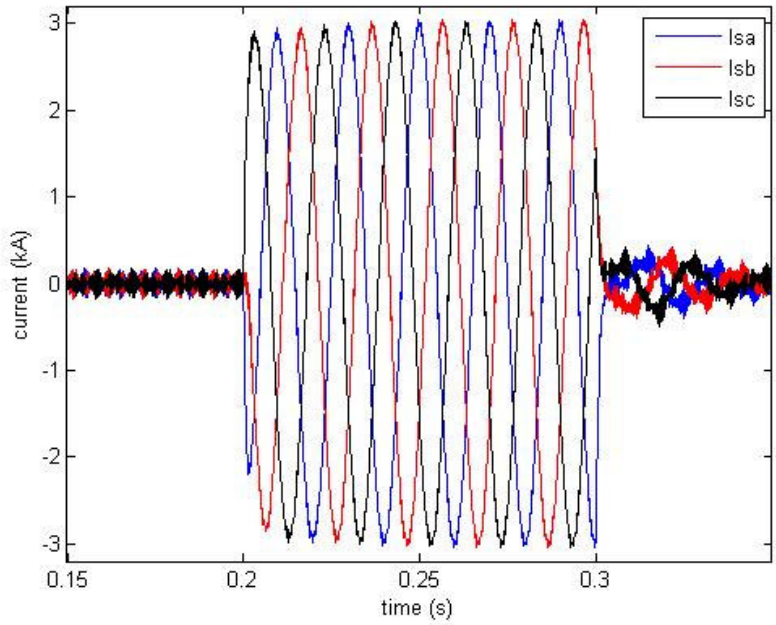

Fig 5.8 Currents I_{sa}, I_{sb}, I_{sc} during a step pulse given to reactive current reference i_d^*

The current vector controller has for the first time problems. The reference value is reached after some time and the cross-coupling is the reason for that. In Fig 5.7 it can be seen that the active current changes more than expected. These problems are still small and the performance is satisfactory.

The last test of the current vector controller is more advanced. Both reference currents will have steps and this simulates a normal usage of circuit, because both active and reactive power is changed and that is expected in normal operation. The reference active current makes a step from 0 to 1 kA at t equal to 0.2 s. It stays at that value until t equals 0.35 s, then it changes to -1, simulates power reversal. The reference reactive current makes a step pulse at t equals 0.25, magnitude is 1 kA and pulse length 0.05 s. The active and reactive current can be seen in Fig 5.9 and the grid phase currents can be seen in Fig 5.10.

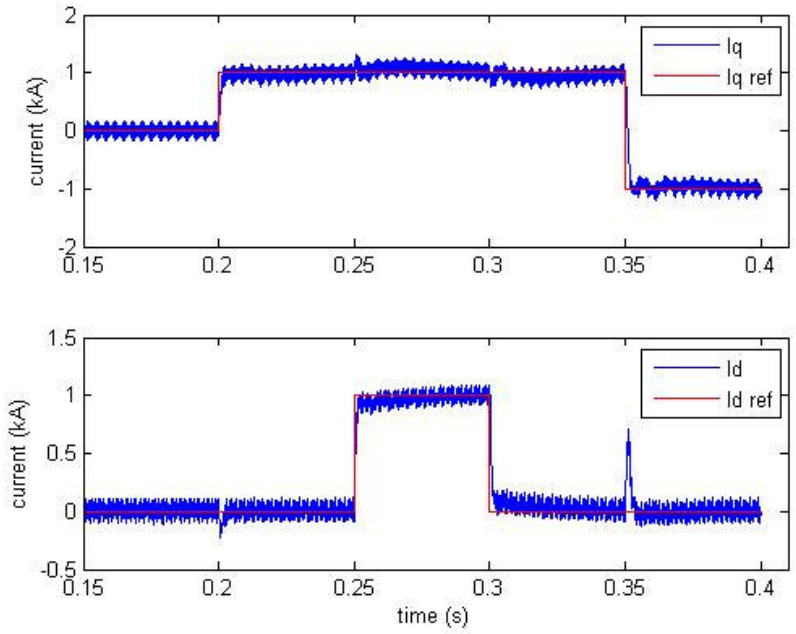

Fig 5.9 Responses of the real and reactive current, i_d and i_q, with a step pulse given to active current reference i_q^*. The magnitude varies between 1 and -1 kA and the pulse width is 0.15 s. A step pulse is also given to the reactive current reference i_d^*. The magnitude varies between 0 and 1 kA and the pulse width is 0.05 s.

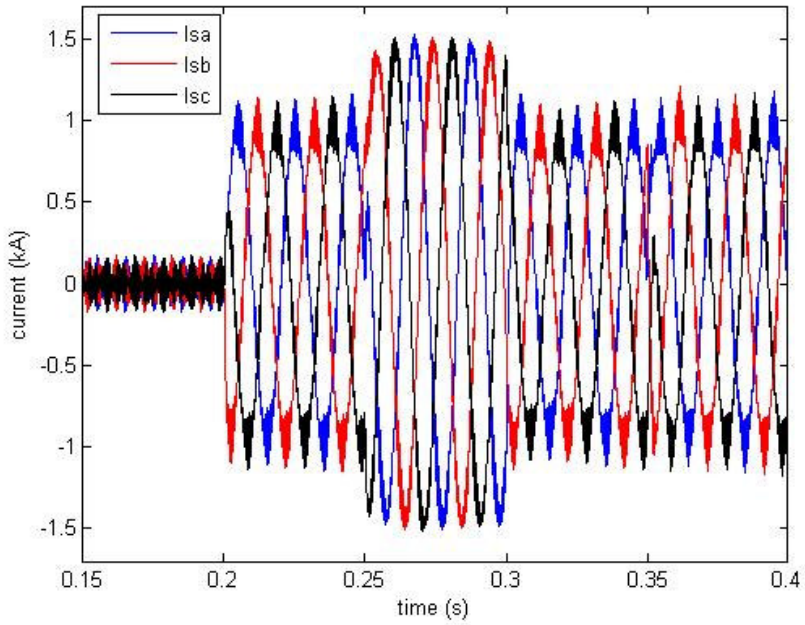

Fig 5.10 Currents I_{sa}, I_{sb}, I_{sc} during steps in active current reference i_q^* and reactive current reference i_d^*

The step response is good and the controller works as expected. Problem with cross-coupling occur at t equals 0.35 when step in reference active current is made. Otherwise the cross-coupling is small and can almost not be seen. The three-phase currents look also as expected with some harmonic content.

5.1.2 Control model B

Table 5.3 shows the parameters used in the current vector controller used in these step response simulations.

Table 5.3 Parameters of the current vector controller used in step response simulation

Proportional gain	K_{pi}	25
Integral time constant	T_i	0.0001 s

A step pulse, magnitude 0.1 kA and pulse length 0.1 s, is given to the active current reference while the reactive current reference is kept constant at zero. In Fig 5.11 the response of the active and reactive currents are shown. In Fig 5.12 the grid phase currents and currents of the converter 1 can be seen.

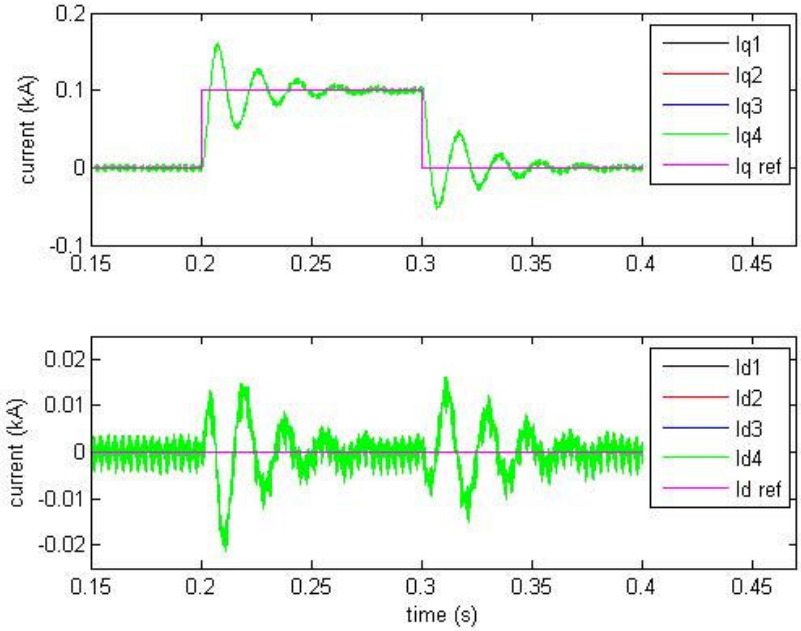

Fig 5.11 Responses of the real and reactive currents, i_{dn} and i_{qn}, with a step pulse given to active current reference i_q^*. The magnitude varies between 0 and 0.1 kA and the pulse width is 0.1 s, while the reactive current reference i_d^* is kept at 0 A.

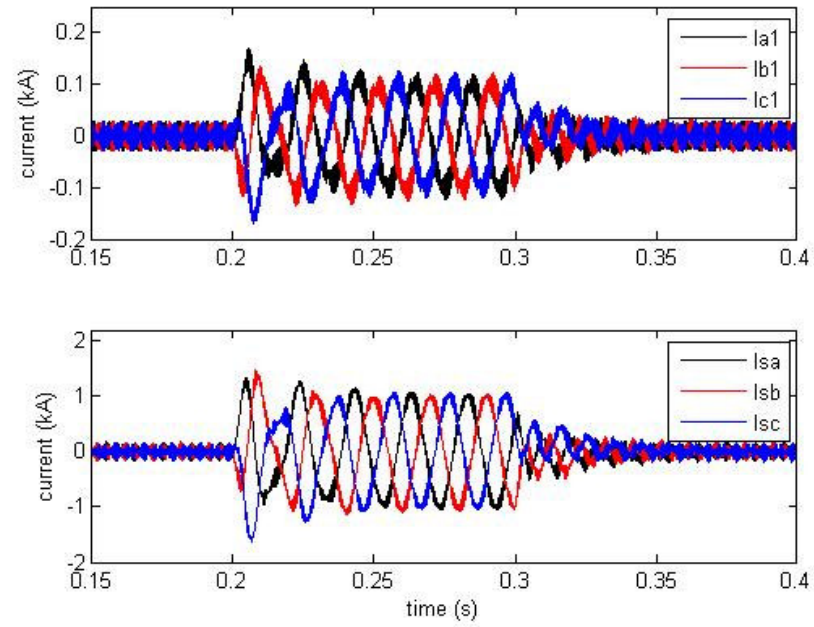

Fig 5.12 Currents I_{a1}, I_{b1}, I_{c1} and currents I_{sa}, I_{sb} and I_{sc} during step in active current reference i_q^*

As seen in Fig 5.11 the step response is not as good as in Fig 5.1, control model A. There is more oscillations and cross-coupling with this control model. The result is also seen in Fig 5.12 as the currents are not completely sinusoidal. The amplitude for the different phases is also different.

Another step pulse, with amplitude varying between 0 and 0.3 kA and step length of 0.1, is given to the active current reference. During the simulation the reactive current reference is kept constant at zero. The response of the active and reactive currents is presented in Fig 5.13. The converter current for converter 1 and the grid currents are presented in Fig 5.14

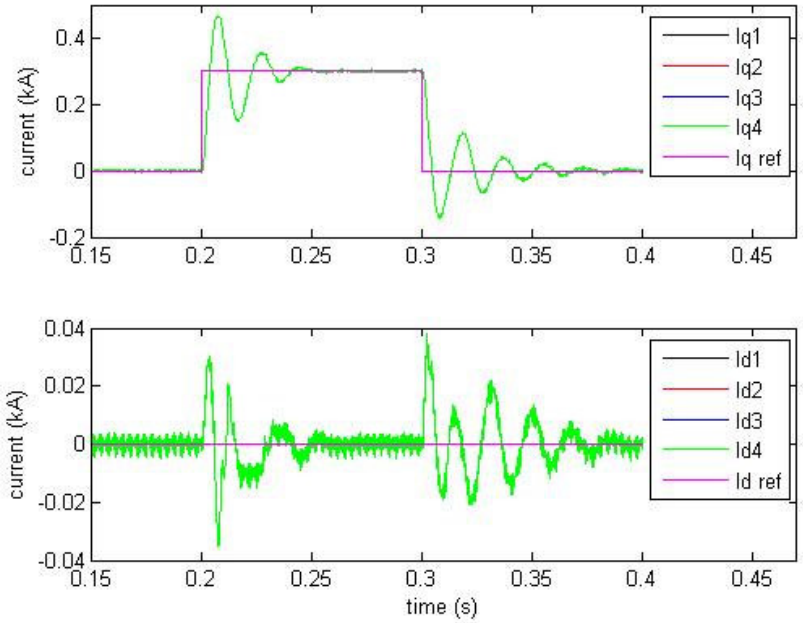

Fig 5.13 Responses of the real and reactive currents, i_{dn} and i_{qn}, with a step pulse given to active current reference i_q^*. The magnitude varies between 0 and 0.3 kA and the pulse width is 0.1 s, while the reactive current reference i_d^* is kept at 0 A.

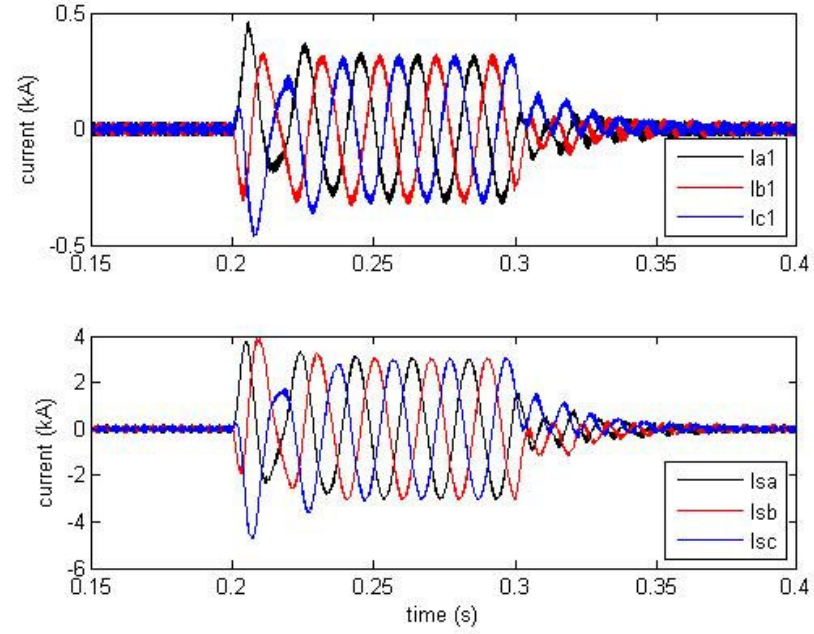

Fig 5.14 Currents I_{a1}, I_{b1}, I_{c1} and currents I_{sa}, I_{sb} and I_{sc} during step in active current reference i_q^*

Also for this step pulse the response is not as good as the respective test for control model A. Oscillations occur in both active and reactive current and the cross-coupling can easily be seen. The converter currents and the grid currents also here have problems with different amplitude for the phases.

A step pulse is given to the reactive current reference and its magnitude is 0.1 kA and pulse length of 0.1 s. The active current reference is in this case kept constant at zero. In Fig 5.15 the response of the active and reactive currents are shown. In Fig 5.16 the converter currents for converter 1 and the grid currents is shown.

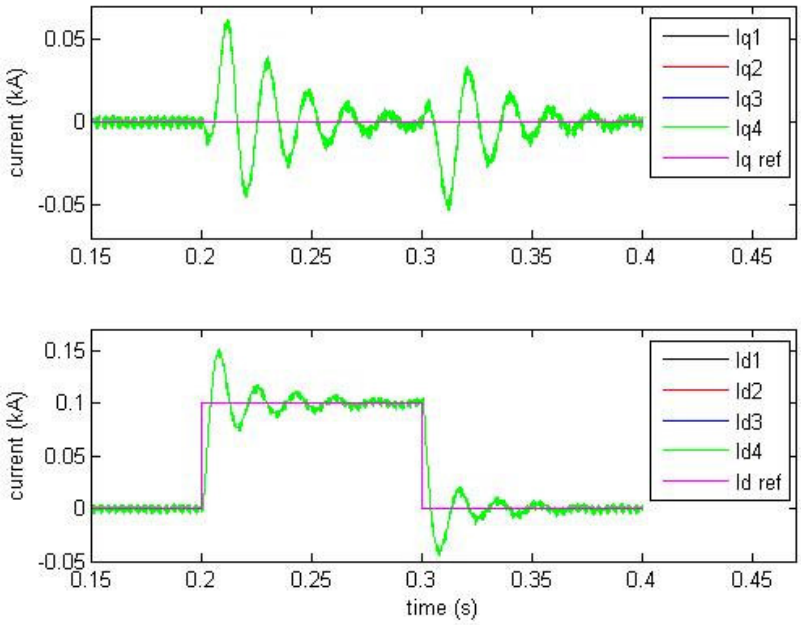

Fig 5.15 Responses of the real and reactive currents, i_{dn} and i_{qn}, with a step pulse given to reactive current reference i_d^*. The magnitude varies between 0 and 0.1 kA and the pulse width is 0.1 s, while the active current reference i_q^* is kept at 0 A.

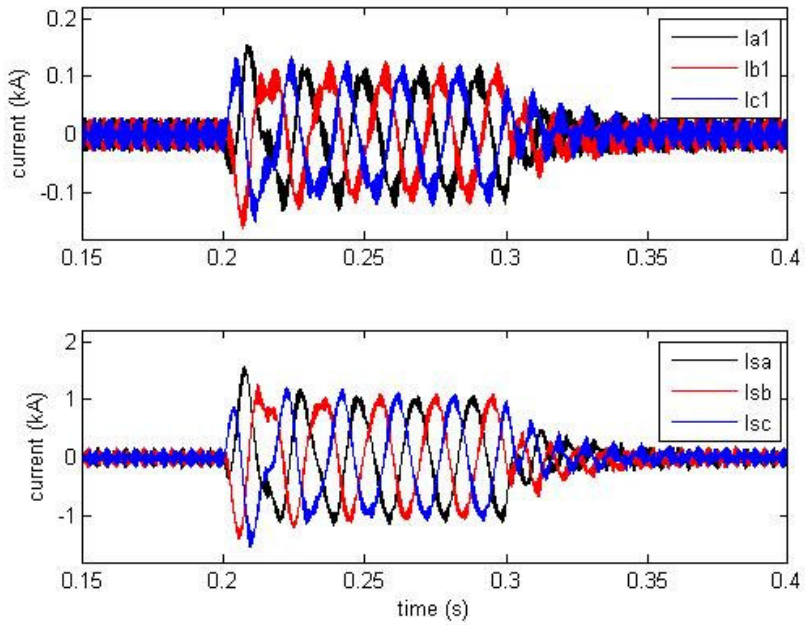

Fig 5.16 Currents I_{a1}, I_{b1}, I_{c1} and currents I_{sa}, I_{sb} and I_{sc} during step in reactive current reference i_d^*

The step in reactive current reference does also lead to worse results than when control model A is used. There is noticeable overshoot for the reactive current together with oscillations. In the active current can cross-coupling be seen, which lead to oscillations in active current. These oscillations are seen in Fig 5.16 as the amplitudes for the different phases can easily be seen.

Another step pulse is given to the reactive current reference, the magnitude is now 0.3 kA and the pulse length is kept at 0.1 s. The active current reference is still kept constant at zero. The response of the active and reactive currents can be seen in Fig 5.17. The converter currents for converter 1 and the grid currents can be seen in Fig 5.18.

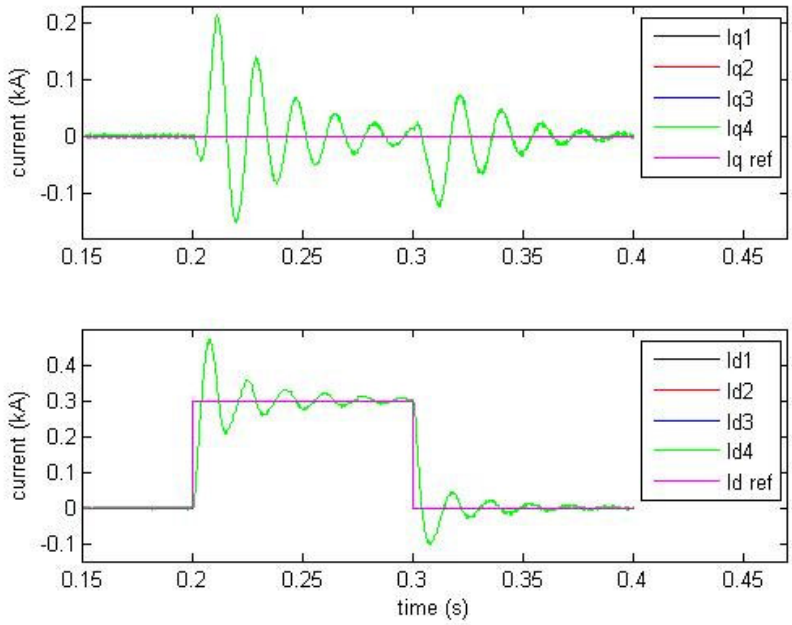

Fig 5.17 Responses of the real and reactive currents, i_{dn} and i_{qn}, with a step pulse given to reactive current reference i_d^*. The magnitude varies between 0 and 0.3 kA and the pulse width is 0.1 s, while the active current reference i_q^* is kept at 0 A.

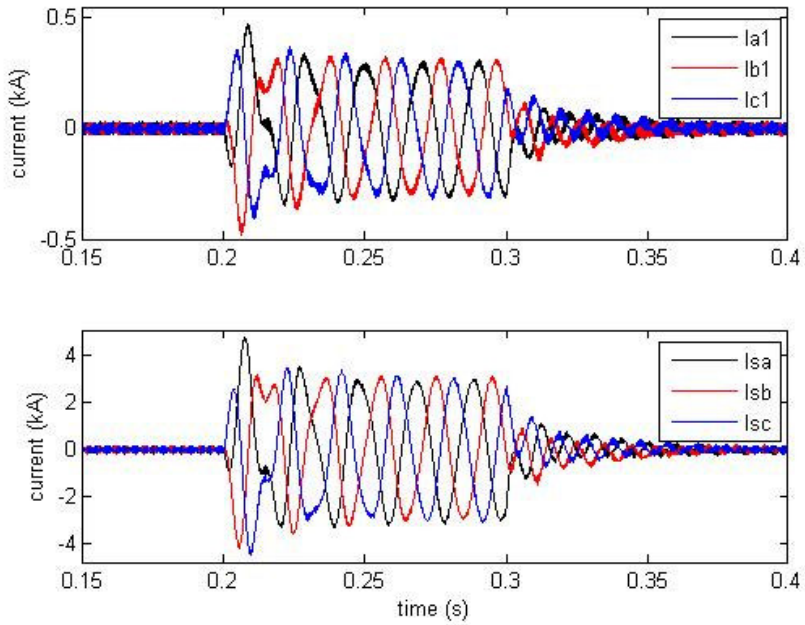

Fig 5.18 Currents I_{a1}, I_{b1}, I_{c1} and currents I_{sa}, I_{sb} and I_{sc} during step in reactive current reference i_d^*

The result of the step pulse given to the reactive current reference is remarkable. The peak value for the active current is over 0.2 kA but it should be zero. Also the overshoot for the reactive current is high, is peaks around 0.5 kA. Oscillations are seen both the reactive and active current and there amplitude varies rather much. These problems are easily seen in Fig 5.18 as the currents in the beginning of the step do not look like sinusoidal waves. There are also problems with amplitude difference between the phases.

The last step test for the control model B is a little bit advanced than other tests. In this case both reference currents will have steps. The first step is for the active current reference, which at t=0.2 makes a step from zero to 0.1 kA. It stays at 0.1 kA until t=0.35 and then it makes a step to -0.1 kA. The reactive current reference is kept at zero until t=0.25 and then a step pulse is given. The magnitude for the pulse is 0.1 kA and the pulse length is 0.05 s. These steps simulate changes in both the active and reactive power. During normal operation the controller must be able to handle steps in both currents. In Fig 5.19 the response of the active and reactive currents is shown. In Fig 5.20 the converter currents for converter 1 and the grid currents are shown.

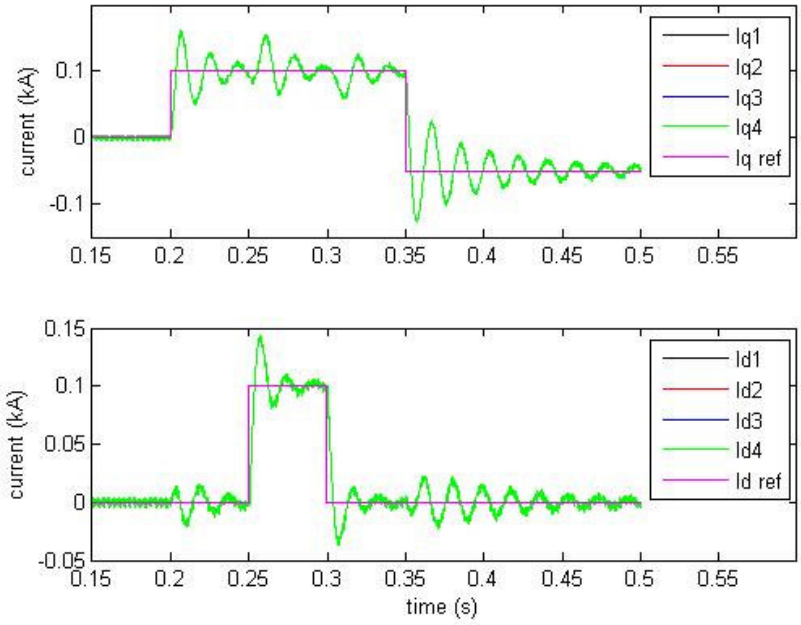

Fig 5.19 Responses of the real and reactive current, i_d and i_q, with a step pulse given to active current reference i_q^*. The magnitude varies between 0.1 and -0.1 kA and the pulse width is 0.15 s. A step pulse is also given to the reactive current reference i_d^*. The magnitude varies between 0 and 0.1 kA and the pulse width is 0.05 s.

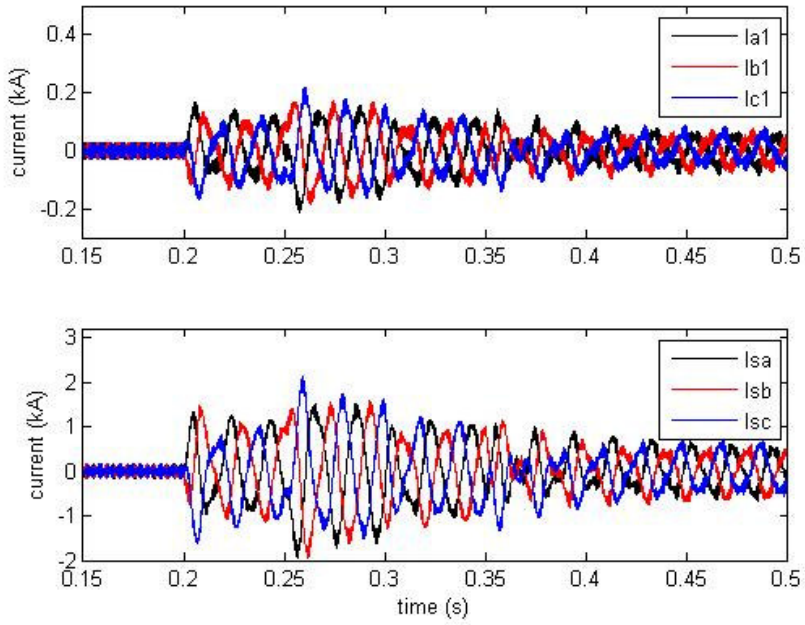

Fig 5.20 Current I_{a1}, I_{b1} and I_{c1} and currents I_{sa}, I_{sb}, I_{sc} during steps in reference active current i_q^* and reference reactive current i_d^*

Fig 5.20 shows the problems that now occur. The currents are not smooth sinusoidal waves and the amplitude for the phases also differs. The reason for these is the oscillations that occur in the active and reactive currents. The active and reactive current oscillates all the time during the steps and that is due to cross-coupling. The overshoot for the currents are also high which leads to too high power.

5.1.3 Conclusions

From the simulation results of the current vector controller conclusions can be made. By comparing the results from the test with control model A and B it is seen that the current vector controller for control model A works better. Still the current vector controller is not perfect but the cross-coupling for control model A is compared to those in control model B are insignificant. The oscillations seen in the step responses for control model B are not seen in responses for control model A. The difference between the two models is best seen in the last test when both active reference and reactive current reference exposed to steps. Control model A handles it very well and only once of cross-coupling term can be seen. Control model B can not handle the steps and both reactive and active current oscillates. The resulting three-phase currents are not sinusoidal waves as when control model A is used. From this test it can be concluded that the current vector controller in model B does not work properly. It is maybe possible to do some changes to it to get it to work better. The result from model A is satisfactory. Model B seems to be the worst alternative.

For both control models more tests are needed. These tests have been run but further tests are needed. The control parameters need some more investigation and it most likely that the performance for both control models can be increased when adjusting the control parameters.

5.2 DC-link voltage control test

This test is used to test the control models to see if they can control the DC-link voltage. The test is performed by simulating a load current at the DC side of the converters. The control dynamics are tested by changing the load current. Additionally, a step has been added to the reactive current reference and the response of the system has been studied. The results are divided in two parts, one part for results from the control model A and another part for results from the control model B.

5.2.1 Control model A

Table 5.4 shows the control parameters used in the current vector controller and the DC-link voltage controller in these simulations.

Table 5.4 Parameters of the Current Vector Controller (CVC) and DC-link controller used in the simulations

Proportional gain, CVC	K_{pi}	5
Integral time constant, CVC	T_i	0.003 s
Proportional gain, DC-link	K_{pdc}	1
Integral time constant, DC-link	T_{idc}	0.01 s

The first test is done by changing the load current, I_{dc}, and at t=0.3 it changes from 0.05 kA to 0.2 kA. This simulates an increase of active power transmission and in Fig 5.21 the resulting DC-link voltage and the load current are shown. In Fig 5.21 the DC voltage for the converters is shown and in Fig 5.22 the active current reference and the response of active current are shown.

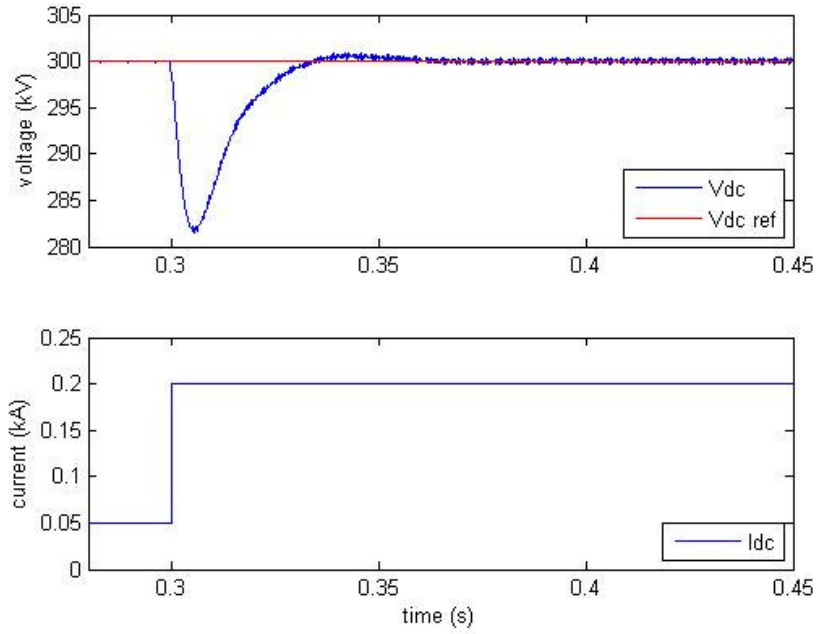

Fig 5.21 DC-link voltage V_{dc} and current I_{dc} during step in load current, from 0.05 kA to 0.2 kA

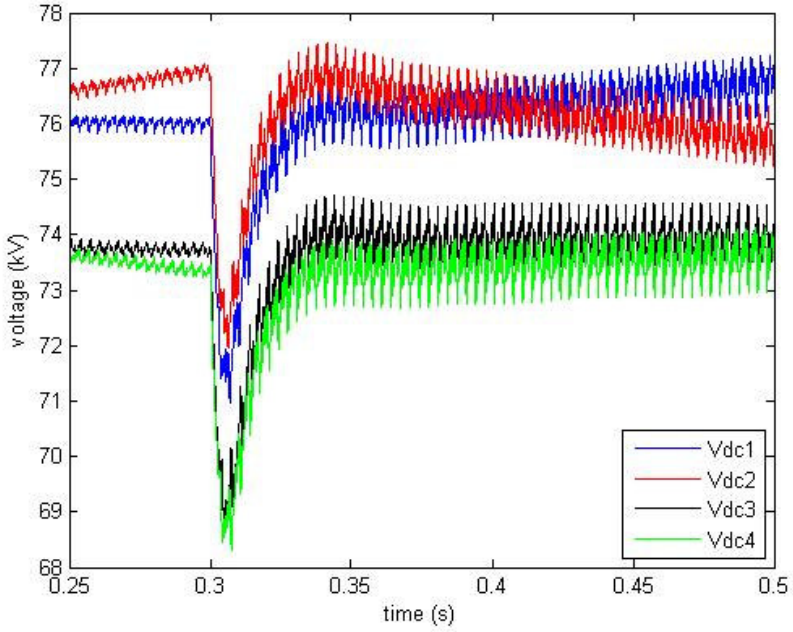

Fig 5.22 Voltages V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} during step in load current, from 0.05 kA to 0.2 kA

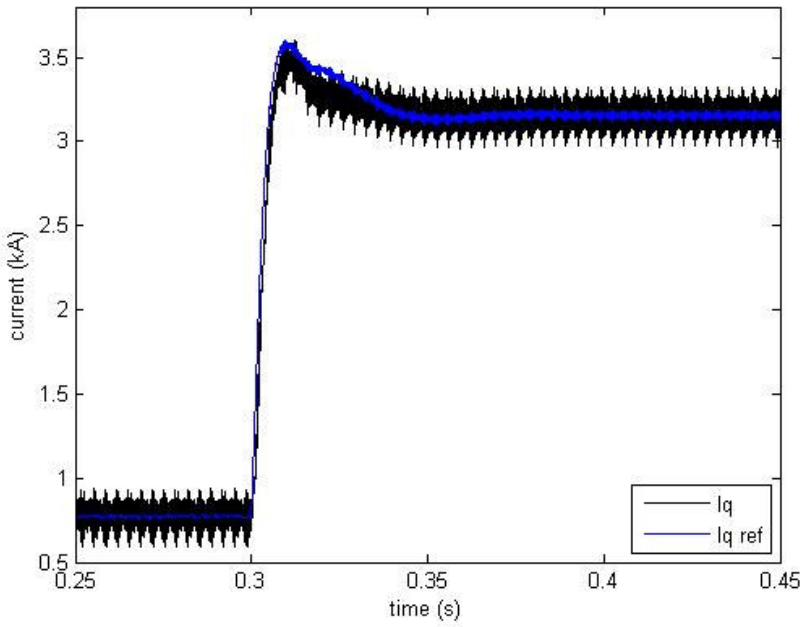

Fig 5.23 Current I_q and active current reference i_q^* during step in load current, from 0.05 kA to 0.2 kA

The result shows that the DC-link voltage controller works and the reference DC voltage are reached after the step in the load current is made. The DC voltage dips at approximate 280 kV and that can be seen as a rather big dip. The DC voltage does not have an overshoot when it tries to reach the reference value. The DC voltages for the converters show on the other hand some problems. The DC-link voltage is not distributed uniformly on the DC voltages for the converters. They are also not constant and increasing and decreasing respectively. The step response for the active current does show some good results. The active current is able to follow the active current reference which means that the control system can provide the circuit with the amount of active power that it needs.

The next test involves power reversal since the load current is changed from 0.2 kA to -0.2 kA at t=0.35. The resulting DC-link voltage and the DC load current are presented in Fig 5.24. The DC voltages for the converters are presented in Fig 5.25 and in Fig 5.26 the reference active current and the response of the active current are presented.

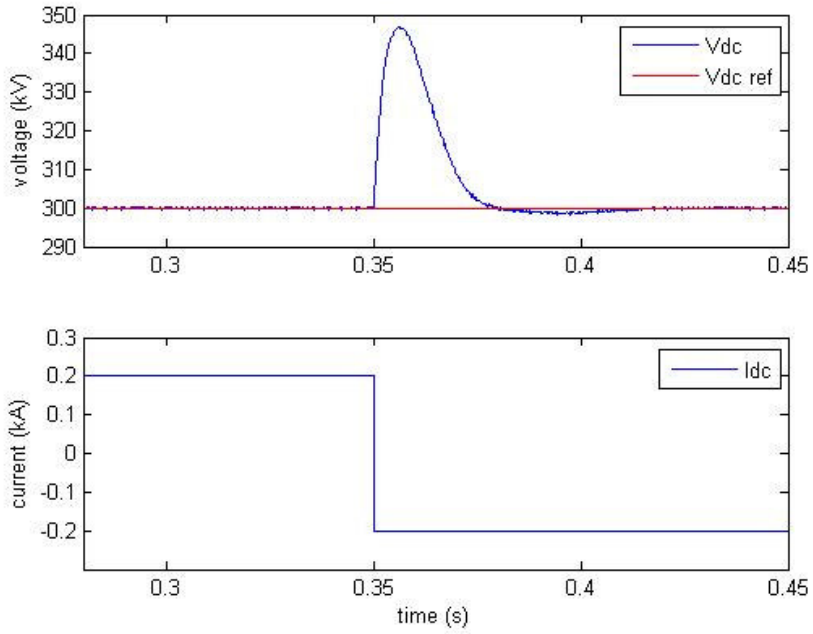

Fig 5.24 DC-link voltage V_{dc} and current I_{dc} during step in load current, from 0.2 kA to -0.2 kA

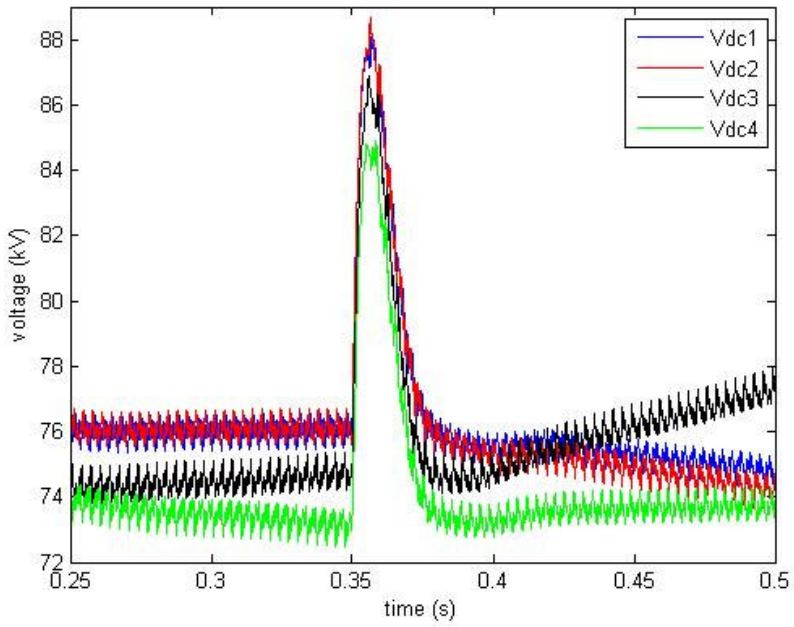

Fig 5.25 Voltages V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} during step in load current, from 0.2 kA to -0.2 kA

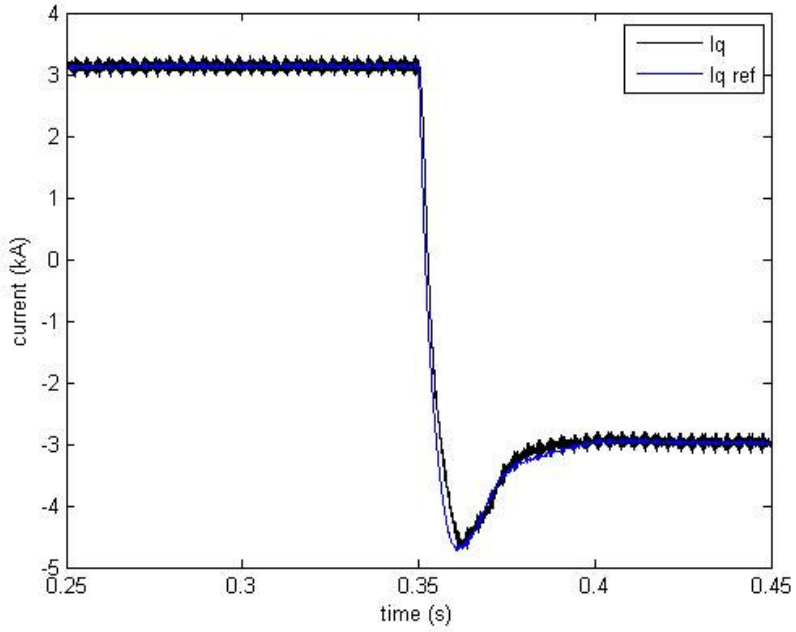

Fig 5.26 Current I_q and active current reference i_q^* during step in load current, from 0.2 kA to -0.2 kA

The result shows that the DC-link voltage controller can control the DC-link voltage during a power reversal. The DC-link voltage peaks at approximate 345 kV but after that it returns to the reference value. The individual DC voltages for converters shows some unbalance and the voltages are not kept constant. While the current response is working well and the reference value is followed by the active current.

The last test of the DC-link voltage performance is to make a step in the reference reactive current before a power reversal. The reference reactive current makes a step at t=0.3 and the amplitude changes from 0 kA to 1 kA. At t=0.35 the DC load current changes polarity, from 0.2 kA to -0.2 kA. In Fig 5.27 the DC-link voltage is shown together with the DC load current. The DC voltages for the converters are shown in Fig 5.28 and in Fig 5.29 the response of the active and reactive current is shown.

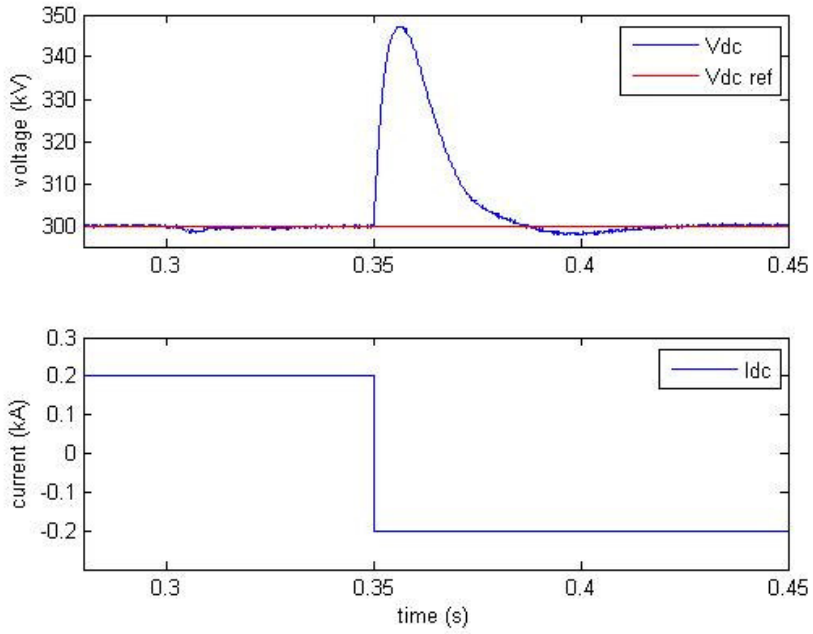

Fig 5.27 DC-link voltage V_{dc} and current I_{dc} during step in load current, from 0.2 kA to -0.2 kA, and step in reactive current reference i_d^*

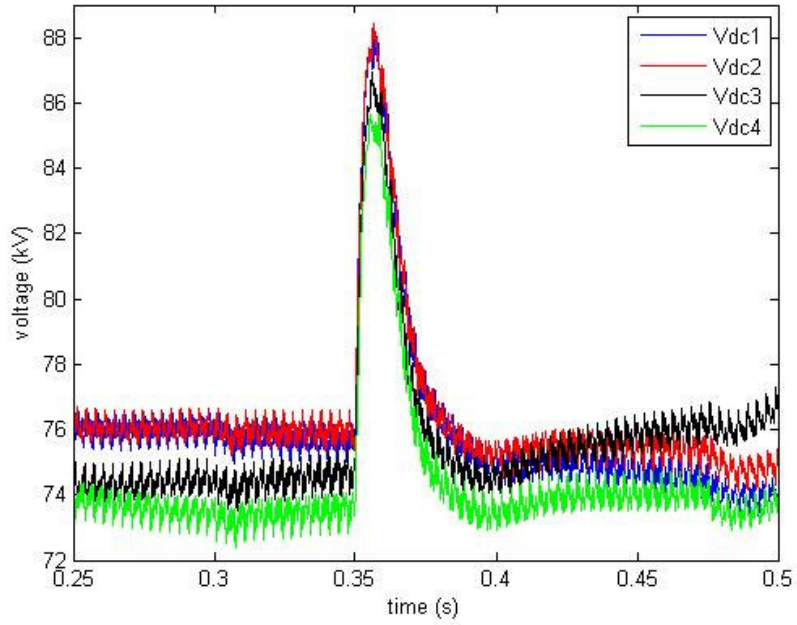

Fig 5.28 Voltages V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} during step in load current, from 0.2 kA to -0.2 kA, and step in reactive current reference i_d^*

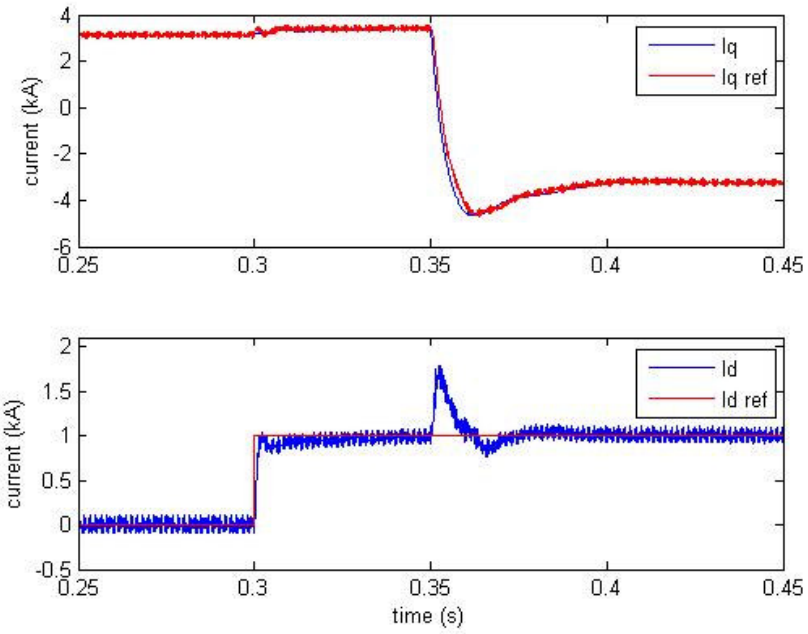

Fig 5.29 Current I_q and I_d and reference active current i_q^* and reactive current reference i_d^* during step in load current, from 0.2 kA to -0.2 kA, and step in reactive current reference i_d^*

The DC-link voltage controller works as expected and the DC-link voltage is almost none affected by the step in the reactive current reference. The change of polarity of the DC load current leads to a peak in the DC-link voltage. It peaks is at approximate 348 kV and after it goes back to the reference value. The DC voltages for the converters are also here unbalanced and the same phenomena with increasing respectively deceasing voltages are also seen. The step response for the active and the reactive current is looking good. The only problem is a peak at t=0.35 for the reactive current, probably some sort of cross-coupling happening there.

5.2.2 Control model B

Table 5.5 shows the control parameters used in the current vector controller and the DC-link voltage controller in these simulations.

Table 5.5 Parameters of the Current Vector Controller (CVC) and DC-link controller used in the simulations

Proportional gain, CVC	K_{pi}	25
Integral time constant, CVC	T_i	0.0001 s
Proportional gain, DC-link	K_{pdc}	0.001
Integral time constant, DC-link	T_{idc}	1 s

Problems occur during start of the DC-link voltage controller in control model B. Therefore it is not possible to run the tests which were used for control model A. In Fig 2.1 the four active converter currents are shown and it is during the start of the DC-link voltage controller. In Fig 5.31 the DC-link voltage and the DC voltages for the converters are shown and it is also during the start up.

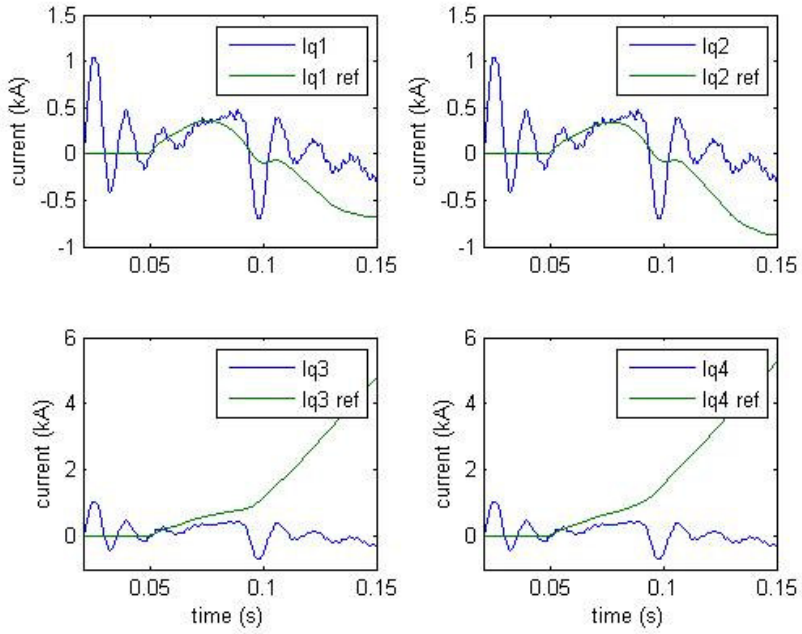

Fig 5.30 Currents I_{q1}, I_{q2}, I_{q3} and I_{q4} and active currents reference i_{q1}^*, i_{q2}^*, i_{q3}^* and i_{q4}^* during start up of DC-link voltage controller

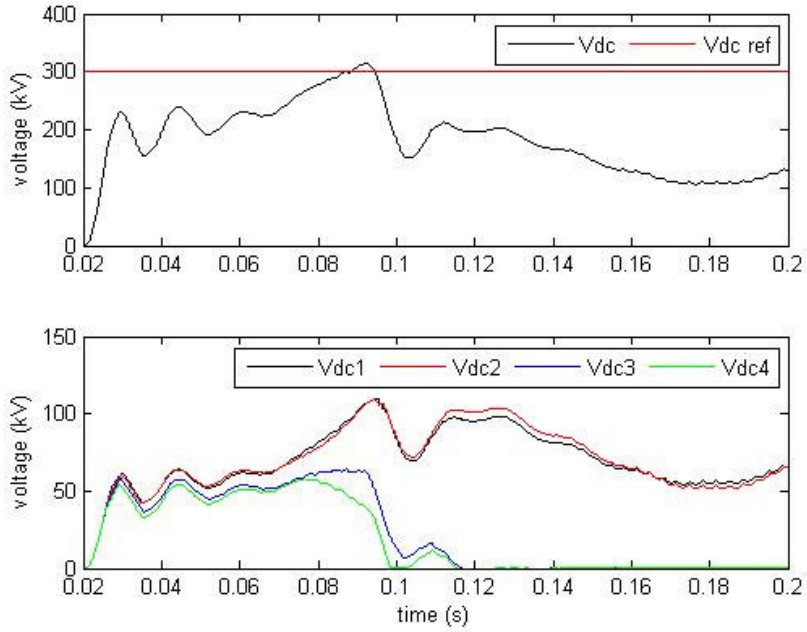

Fig 5.31 DC-link voltage V_{dc} and converter DC voltages V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} during start of DC-link voltage controller

The problem that can be seen is that the active converter currents are not able to follow the reference active currents, which are fed from the DC-link voltage controller. Two of the currents increase rapidly while the other two decreases. This results in problems for the DC voltages. As can be seen in Fig 5.31 the DC-link voltage reaches the reference value once but is not able stay at the value. Instead it decrease and varies a lot. The DC voltage for the converters shows some differences. Two of the voltages become zero after some time and the other two varies a lot. This variation in the DC voltages makes it impossible to simulate DC load current changes. This result also demonstrates how important the current vector controller is for the DC-link voltage controller.

5.2.3 Conclusions

From the results of the DC-link voltage control test some conclusions can be made. The first thing is that the DC-link voltage control in control model B is not working at all. It is able to reach the reference value but it is not able to keep the DC-link voltage at the reference value. The reason for this is probably the connection of the transformer. The transformer is series connected on the grid side and therefore the same current is floating all the windings. The current controller can not control the converter currents individually which is seen in Fig 5.30. The reference currents are different but the active currents for the converters are the same. The idea with DC-link voltage control in model B is to control DC voltage for each converter and then the active currents reference should and are not the same. Therefore control B is not working and probably it is not possible to get to work.

The DC-link voltage control in control model A on the other hand work very well. Maybe the peaks and the dips are a bit large but still the control brings the voltage back to the reference value. However, it is not working without problems. The unbalance of the DC voltage for the converters may cause some problems with instability. The constant increase and decrease of the voltage may also be a problem. To be able to say that control model A is working correctly more tests need to be done. Especially long time tests were the unbalance in the DC voltage for the converters are investigated. Perhaps it is possible to make some changes to the control model so the unbalance can be limited.

The control parameters for the control models need more investigation. Very little time has been spent on adjusting the parameters and it is very likely that performance can be increased with changes made to the control parameters.

5.3 Summary

The simulations presented here have tested the two control models that were described in Chapter 4. The first part of simulations was test of the current vector controller for the two models. It has been shown that the current vector controller for the control model A could handle the step responses better than the current vector controller for control model B. The step response for control model A did not include as much oscillations as the step response for control model B. Almost no cross-coupling was seen in the response for model A but was easily seen in the response for model B. It was concluded that the current vector controller in model A was working much better.

The second part of the simulations was to test the DC-link voltage control for the control models. Rather quickly it was seen that the DC-link voltage control in control model B was not working at all. It was assumed that the cause for this was the transformer connection on the grid side. The connection makes it impossible to individually control the different converter currents.

The DC-link voltage control in control model A on the other hand worked well and was able to control the DC-link voltage. It could also keep the DC-link voltage during load current disturbances. It was concluded that only one of the control models was able to fulfil the objective of the thesis. The control model A did also have some problems. The DC voltage for each converter was not evenly distributed and that may lead to instability in the whole system. More tests are needed before it is possible to say that the control model A works in all cases. These simulations have had short durations, none of them exceeded 0.5 seconds. Therefore long time tests are required before it can be said that the models work correctly.

6 Conclusions and future work

In this thesis the voltage source converter was discussed. The background and the aim of the thesis were briefly discussed. HVDC was presented in Chapter 2 and it contained information what it is, how it works and also its history. Different kinds of HVDC technologies were discussed and theirs differences, advantages and disadvantages were also discussed.

The next part of the thesis was a presentation of the voltage source converter in detail. First the circuit was discussed and how it can be used to get the signal that is wanted. This is done by using pulse width modulation and three different PWM techniques were presented. A control system for a voltage source converter was derived. It was divided into two parts, one current controller and one DC-link voltage controller. For the current controller a simplified model of the voltage source converter was derived and it was used for the derivation of the PI controller. For the DC-link voltage controller expressions for the DC quantities were derived. A control system for the DC-link voltage control was derived and the chapter ended with simulation test of the two control parts. The first simulation test was to check if the current controller could handle step pulses and see how the system performed. It was seen that the control system had no problems with the step pulses and the control system performed as thought. The other simulation test was a test of the DC-link voltage controller and it was performed on two different controllers, one without feed-forwarding of the load current and one with feed-forwarding of the load current. Both control systems were exposed to load disturbances and they were able to control the DC-link voltage.

Chapter 4 contained a further development of the voltage source converter that was presented in Chapter 3. Instead of having one voltage source converter the circuit contained four voltage source converter connected in series. Between the grid and the converters a transformer was connected and the transformer was connected in series on the grid side. The reason for the connection was that a multilevel grid voltage waveform was created. In this way the filter rating can be reduced. The series connection of the converters gave the possibility to use harmonic elimination by phase shifting. It is a technique that works by phase shifting the carrier waves for the converters PWM modules. This leads to less harmonic content and the filter capacity can be reduced. That was done when the phase reactor from Chapter 3 was removed from the circuit. The used PWM technique was briefly discussed and two different control models were derived. Their aim was to control the active current, the reactive current and the DC-link voltage. Control model A worked by seeing the four converters as one large converter and the same reference signals are fed to the converters. In this way only one current controller and one DC-link voltage controller was needed. The control system from Chapter 3 was used. Control model B on the other hand worked by controlling each converter independent. That gave four current controllers and four DC-link voltage controllers, which made the system more complex but also makes it possible to control the DC voltages for the converters.

In Chapter 5 simulations were performed for both control models. The tests were divided into two parts, step response test and DC-link voltage test. The step response test was performed first and it was shown that control model A worked better than control model B. The DC-link voltage test was performed on both control models but here unexpected result was obtained. Control model B was not able to control the DC-link voltage and the reason for that is transformer connection on the grid side. It is impossible to control the converter currents individually since the current is flowing through the transformer windings is the same. But control model A was able to control the DC-link voltage and worked as thought. The conclusion after the simulation tests was that more testes are needed to draw the conclusion that control model A works in all cases.

6.1 Conclusions

First of all control model A works as thought during the tests that have been performed. The step response for the currents is good and a small amount of cross-coupling could be seen. Probably is it possible to get even better performance out from the current controller if further time is spent on choosing the control parameters. To be able to say that the current controller can handle all kind of steps further tests must be performed, especially for high step values.

Secondly, the DC-link voltage control in control model A manages the task but questions regarding the unbalance of the DC voltages for the converter were emerged. This unbalance and the increase and the decrease of the voltages may lead to stability problems for the controller. Therefore it is not possible to say that the DC-link voltage controller works as thought. Further test and especially long time tests of the DC-link voltage controller need to be performed. The capacitance value for the converters can maybe diminish these problems.

Control model B works not satisfactory. The step response for the current controller is not as good as when control model A is used. Problems with cross-coupling occur and both signals have problems with oscillations. Perhaps it is possible to make some changes and in that way make the current controller to work better. The limit of time has made it impossible in this thesis to look at it.

The DC-link voltage controller in control model B does not work at all. It was seen it could not even make a start. The control system was designed to control the DC voltage for each converter individually. However it is impossible to control the converter currents independently. The series connection of the transformer leads to that the same currents floats in the transformer windings. Therefore the converter currents for the converters are all the same. Converter current A for converter 1 is the same as the converter current A for converter 2, 3 and 4. This makes the whole idea of the control system to fail. The thought was that the converter currents for the converters should be different and in this way control the DC voltages for the converters. Perhaps a change to circuit can make the control system work but at this time it seems unlikely.

Finally, another problem with control model B needs to be addressed. The transformer makes that there is a phase difference between the grid currents and the converter currents. This is not so important for control model A but for control model B it is. When looking at the active and reactive currents for the converters and comparing these to the active and reactive current of grid currents, the phase difference is seen. The current controller in control model B does what it is supposed to do and both currents are equal to the reference value. Then the active and reactive current of the grid current are not having the same load angle. The control system is supposed to control the system so that only active current is transmitted. Since load angle difference will result to a different load angle for the grid currents are not the same as the load angle for the converter currents. In reality the system delivers both active and reactive current.

6.2 Future work

Due to the limited time of the thesis work some parts have not been investigated. The most important thing needs to be looked at is the unbalance of the DC voltages for the converters when control model A is used. It was seen that the DC-link voltage was not uniformly distributed over the converter capacitances. This should be looked at to see if this lead to stability problems for the control system and if it is possible to diminish the unbalance. Maybe the capacitor value can be changed so that the unbalance becomes less.

Secondly, the control parameters have not been optimised and perhaps it is possible to increase the controllers performance is this way. Feed-forwarding of the load current should be tested in the DC-link voltage controller to see if this also leads to better performance.

In all simulation tests SPWM has been used and the optimised PWM has not been tested. This should also be tested to see if the control performance can be improved.

A further look at control model B should be done to verify if it is possible to increase the performance. Perhaps some changes to the circuit can optimise the control system. At the moment it is too early to disregard it, just based on this first, initial investigation.

The control models need to be tested for eight converters connected in series.

References

[1] N. Mohan, T. Undeland, and W. P. Robbins, *Power Electronics; Converters, Applications and Design*, 3rd ed. Hoboken, NJ: Wiley, 2003.

[2] *It's time to connect*, 2006, rev 2. [Online]. Available: http://search.abb.com/library/ABBLibrary.asp?DocumentID=1JNL100105-122&LanguageCode=en&DocumentPartID=&Action=Launch

[3] L. Haglöf, *History of HVDC Part 1: The mercury arc valve era*, May 2004. [Online]. Available: http://www.abb.se/cawp/gad02181/5950ab82df908d0cc1256e89002f3e6f.aspx

[4] P. Danfors, *History of HVDC Part 2: ASEA's HVDC Thyristor Introduction 1965 – 1980*, May 2004. [Online]. Available: http://www.abb.se/cawp/gad02181/6d34ebf7b22e5cd5c1256e930030703e.aspx

[5] F. Stergiopoulos, *Analysis and Control Design of The Three-Phase Voltage-Source AC/DC PWM Converter*, Ph.D thesis, The University of Birmingham, Birmingham, UK, 1998.

[6] V. G. Agelidis, *Optimum Pulse Width Modulation Techniques for Three Phase Inverters*, Ph.D thesis, Curtin University of Technology, Perth, Australia, 1997.

[7] L. Harnefors, *Control of Variable-Speed Drives*, Department of Electronics, Mälardalens University, Västerås, 2002.

[8] J. W. Dixon and B. T. Ooi, *Series and Parallel Operation of Hysteresis Current Controlled PWM Rectifiers*, IEEE Transactions on Industry Applications, Vol.25, No.4, July/August 1988, pp. 644-651.

[9] B. T. Ooi and J. Kuang, *Series Connected Voltage-Source Converter Modules For Force-Commutated SVC and DC-Transmission*, IEEE Transactions on Power Delivery, Vol.9 No.2, April 1994, pp.977-983.

Appendix A

Transformation for Three-phase systems

This appendix describes how the voltages and the currents are transformed between a three-phase system and a αβ-frame, and between a αβ-frame and a dq-frame. This is an important tool that is used in the controller. The dc quantities that are obtained are easier to control.

A.1 Transformation between three-phase system and αβ-frame

The three-phase quantities $x_a(t)$, $x_b(t)$ and $x_c(t)$ can be transformed into a vector $\underline{x}_{\alpha\beta}$ in the fixed two-axis coordinate system, called αβ-frame. The vector is defined as

$$\underline{x}_{\alpha\beta}(t) = x_\alpha(t) + jx_\beta(t) = K\left(x_a(t) + x_b(t)\cdot e^{j\frac{2}{3}\pi} + x_c(t)\cdot e^{j\frac{4}{3}\pi} \right) \tag{A.1}$$

where K is a scaling constant and in this thesis its equal to 2 divided by 3.

The transformation is described in a matrix form in Equation A.2.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{A.2}$$

The inverse transformation matrix is described in Equation A.3.

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{A.3}$$

The active power is calculated be using Equation A.4.

$$P = \frac{3}{2}\left(u_\alpha \cdot i_\alpha + u_\beta \cdot i_\beta\right) \tag{A.4}$$

A.2 Transformation between αβ-frame and dq-frame

Vector $\underline{x}_{\alpha\beta}$ rotates in the αβ-frame with the angular frequency ω(t) in the positive direction, anticlockwise. A dq-frame is placed in the αβ-frame and synchronised with a vector that is rotating with the same angular frequency as the vector $\underline{x}_{\alpha\beta}$. In this way the vector $\underline{x}_{\alpha\beta}$ will appear as fixed vector in that frame. The components of $\underline{x}_{\alpha\beta}$ in the dq-frame are given by the projection of the vector on the synchronisation vector and the orthogonal projection, seen in Fig A.1.

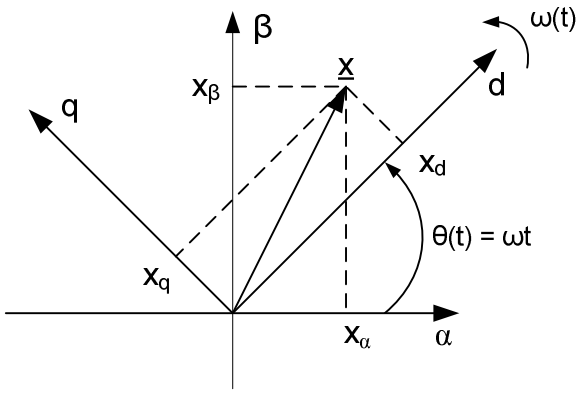

Fig A.1 Relation between αβ-frame and dq-frame

The transformation written in vector form

$$\underline{x}_{dq} = e^{-j(\theta)} \cdot \underline{x}_{\alpha\beta} \tag{A.5}$$

where the angle θ(t) is given by

$$\theta = \int \omega dt \tag{A.6}$$

The inverse transformation from dq-frame to αβ-frame is given by

$$\underline{x}_{\alpha\beta} = e^{j(\theta)} \cdot \underline{x}_{dq} \tag{A.7}$$

The transformation from αβ-frame to dq-frame matrix is written as

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{A.8}$$

And the inverse matrix is

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{A.9}$$

Appendix B

Implementation of a VSC in PSCAD/EMTDC

The objective of this chapter is to describe how a control system for a VSC has been implemented in PSCAD/EMTDC. The different parts in the simulation model are described one by one.

B.1 System

Figure below shows how the simulation model looks like, the model consist of a grid, a RL filter and a VSC. This model is used in simulation of the current vector controller.

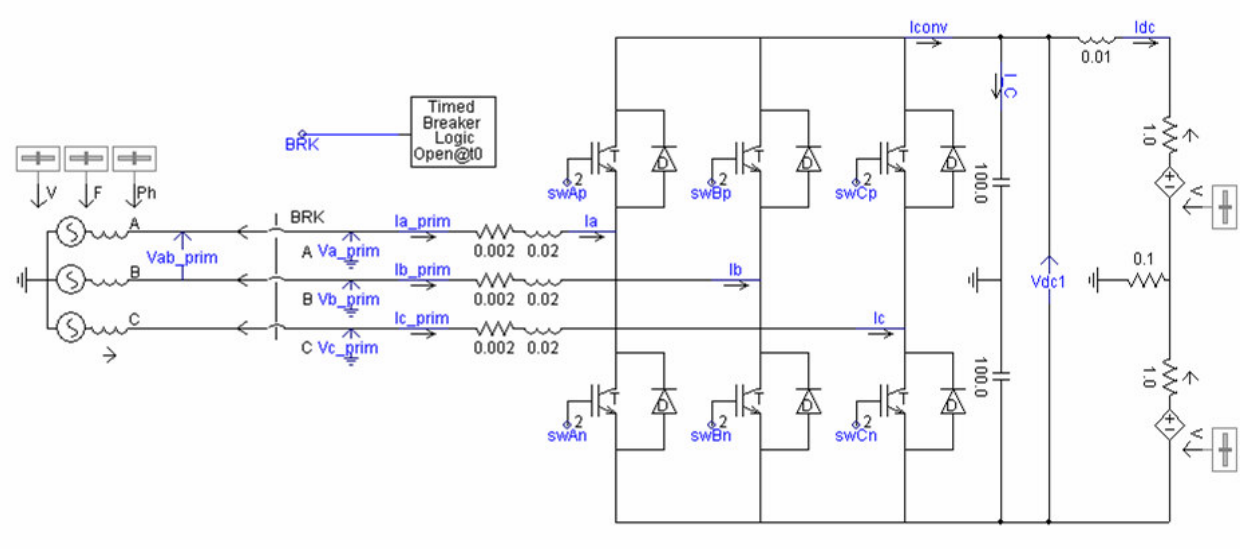

Fig B.1 The simulation model used for the simulation.

For the simulation of the DC-link voltage controller the VSC below, Fig B.2, is used. The difference compared to Fig B.1 is that the two voltage sources are replaced with a current source.

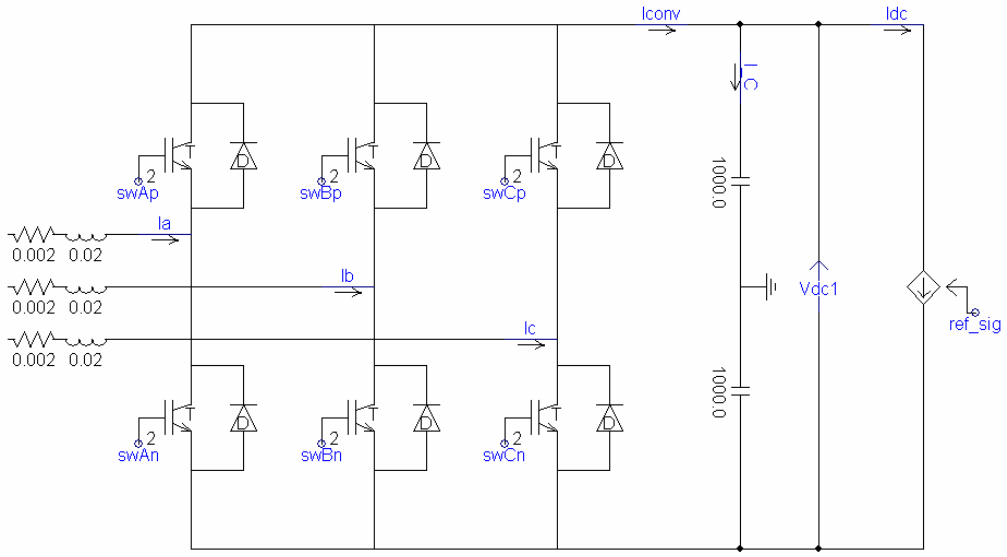

Fig B.2 The VSC used for the simulation of the DC-link voltage controller.

B.2 Implementation of current controller in PSCAD/EMTDC

The simulation model which is shown in Fig B.1 has been used and the controller that was presented in Chapter 3 has been built. Fig 3.2 shows an overview of the current controller and below the implementation of the different blocks is presented.

B.2.1 Transformation from three-phase system to dq-frame

The transformation of the three-phase quantities into the dq-frame is done in two steps. The first step is to transform the quantities to the αβ-frame and then from the αβ-frame to the dq-frame. The phase voltages and the currents in Fig B.1 are transformed to the dq-frame. That is done be implementing Equations (A.2) and (A.8). Fig B.3 shows how the d-component of the phase voltages have been calculated and Fig B.4 shows how the q-component was calculated. The transformation of the currents is done in the same way. The only thing that is done is that the voltages in the figures are changed to respective current.

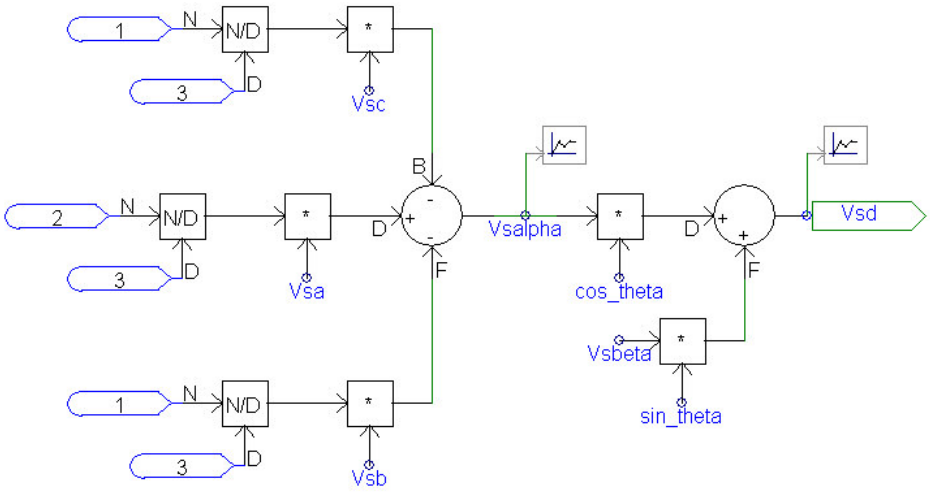

Fig B.3 Creation of d-component

The transformation is made as can seen in the figures in two steps. First an amplitude invariant transformation from the three-phase system to the αβ-frame, it creates the quantities $V_{s\alpha}$ and $V_{s\beta}$. That is then followed by a transformation from αβ-frame to dq-frame. In figures that is the change from $V_{s\alpha}$ and $V_{s\beta}$ to V_{sd} and V_{sq}.

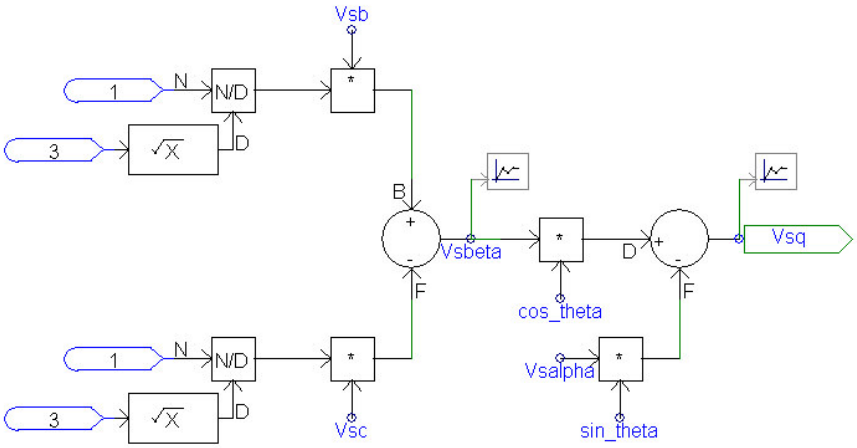

Fig B.4 Creation of q-component

In Section B.2.2 the calculation of the transformation angle is described.

B.2.2 Calculation of transformation angle

The transformation angle is very important in the controller and its object is to make the synchronisation with the grid correct. It is used when the transformation from αβ-frame to the dq-frame is done and in that way the dq-frame is synchronised with the grid. In this simulation the voltage vector $V_{\alpha\beta}$ is defined to be parallel with the q axis in the dq-frame and the transformation angle is defined as

$$\sin\theta = -\frac{V_{s\alpha}}{|V_{s\alpha\beta}|} \tag{B.1}$$

$$\cos\theta = \frac{V_{s\beta}}{|V_{s\alpha\beta}|} \tag{B.2}$$

How the implementation in PSCAD/EMTDC is done can be seen in Fig B.5. $V_{s\alpha}$ and $V_{s\beta}$ are the phase voltages which have been transformed to the αβ-frame.

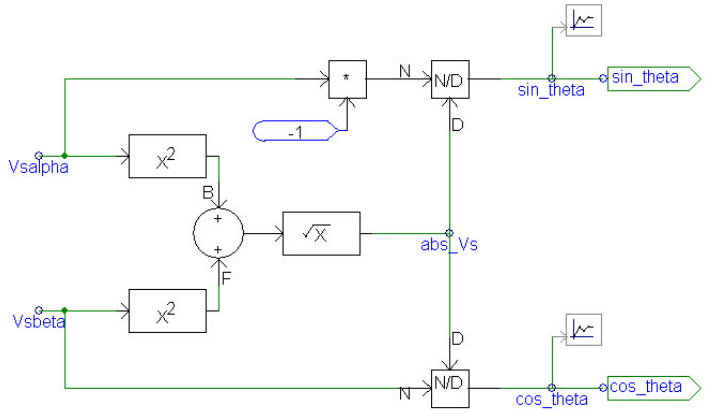

Fig B.5 Implementation of calculation of transformation angle in PSCAD/EMTDC

B.2.3 Current vector controller

The heart in the whole current controller is the current vector controller with PI controller, decoupling and feed-forwarding of the voltage. It is presented in Fig B.6 and it is divided into two parts, one for the d-component and one for the q-component.

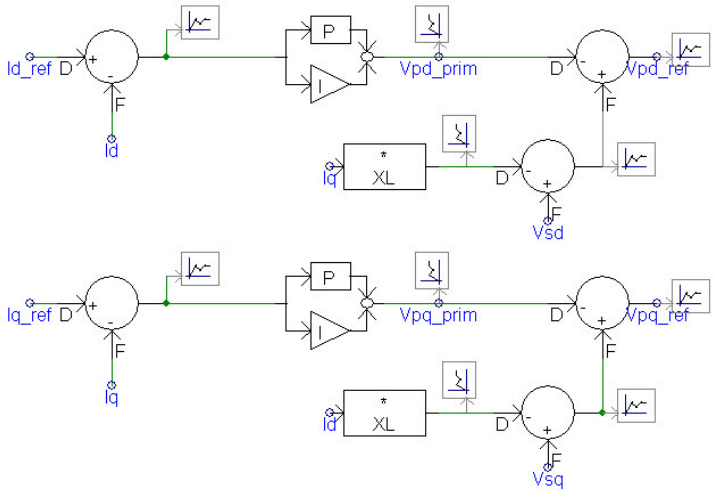

Fig B.6 The current vector controllers, the upper is the controller for the current I_d and lower is the controller for the current I_q.

I_{d_ref} and I_{q_ref} are reference currents that the controller is thought to follow. The decoupling terms are the signals that are received when the currents are multiplied with reactance X_L, the grids reactance. The feed-forwarding is simply done by adding V_{sq} and V_{sd} to respective output signal. The output signal consists of two voltages. They represent the phase voltages at the AC side of the VSC in the dq-frame. These goes then into the modulation index and load angle block.

B.2.4 Calculation of modulation index and load angle

The signals that are received from the vector controller, voltages in the dq-frame, must be transformed to three-phase signals. In this simulation this is done in two steps, first the modulation index and the load angle are calculated and after that the three-phase reference voltages are created. This is presented in Fig B.7 and Fig B.8. The other part is presented in Section B.2.5.

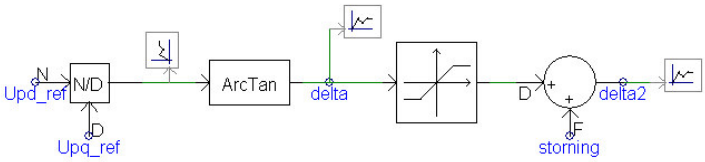

Fig B.7 Calculation of the load angle is implemented

Fig B.7 shows how the load angle is calculated and the mathematical expression is

$$\delta = \tan^{-1}\left(\frac{U_{pdref}}{U_{pqref}}\right) \tag{B.3}$$

Besides calculating the load angle there is a hard-limit avoiding high angle values. Through this way the possibility to transfer a high amount of power is limited, which could otherwise damage the circuit.

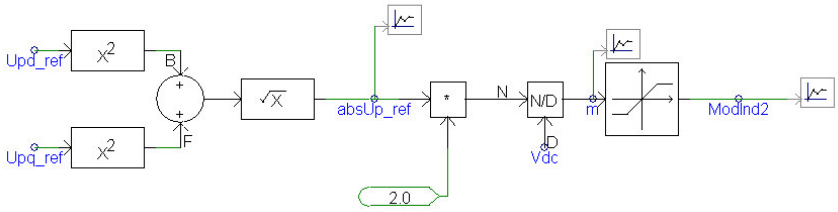

Fig B.8 Calculation of modulation index

Fig B.8 shows how the calculation of the modulation index is implemented in PSCAD/EMTDC and below is the equation that is used in the implementation.

$$m = 2 \cdot \frac{\sqrt{U_{pdref}^2 + U_{pqref}^2}}{V_{dc}} \tag{B.4}$$

Also for the modulation index there is a hard-limit and its purpose is to avoid a to high and low modulation index. If the modulation index would have a value higher than one then overmodulation is reached and a too low value leads to more harmonic contents. The goal is to have the modulation index within a span and in that way have a good operation of the system. Both the modulation index and the load angle are then input signals to the block which creates the three-phase reference voltages.

B.2.5 Creation of reference signals

To be able to create signals to the transistors some reference signals to the PWM is required. These are created from the modulation index and the load angle, and the calculations can be seen in Section B.2.4. In Fig B.9 the creation of the reference signals are presented.

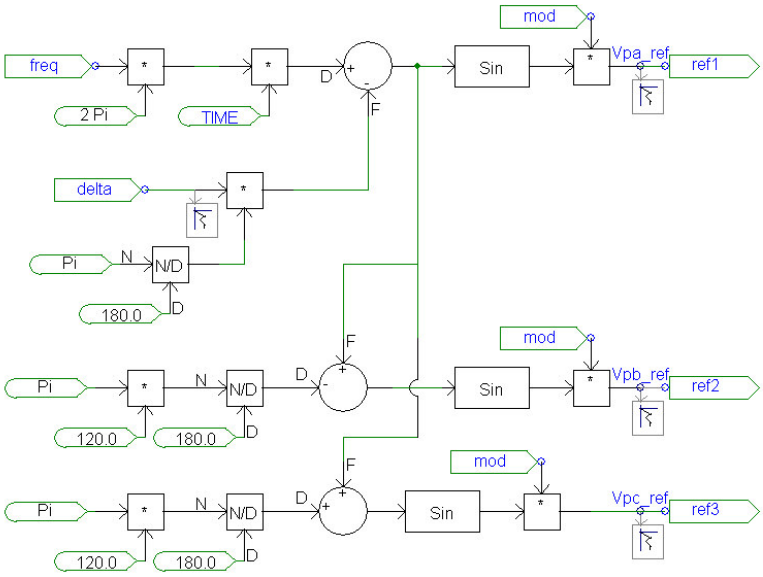

Fig B.9 Creation of three-phase reference voltages

Input signal to the block are modulation index m and load angle δ and out from the block comes three reference signals with peak value of one. The three signals represent the fundamental phase voltages at the AC side of the VSC. Thus there is a phase difference of 120 degrees between them and the output signal then goes to the PWM block.

B.2.6 Creation of gate pulses to the switches

The creation of gate pulses is done in a following way, each reference signal is compared to a triangular wave. The triangular wave has a predetermined frequency, which also determines the switching frequency for the transistors. If the reference signal has a higher value than the triangular wave then the output is high. Instead if the reference signal has a lower value than triangular wave the output is low. When the output is high this means that the output signal has a value of one and with low is means that the output signal is zero. In this way a pulse train is created and it decides if the transistor should be on or off. In Fig B.10 it is shown how the implementation in PSCAD/EMTDC is done and there are three of these blocks, one for each phase. The output signal pwmA is taken to a block which creates the digital signals that the IGBTs use.

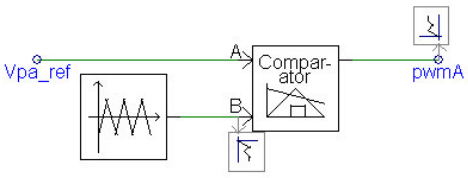

Fig B.10 The creation of the gate pulses

B.3 Implementation of DC-link voltage controller in PSCAD/EMTDC

As mentioned earlier, in this part the VSC in Fig B.1 has been changed to the VSC shown in Fig B.2. The controller is described in detail in Chapter 3.4 and an overview of the controller can be seen in Fig 3.7. Below the different parts of the controllers are presented.

B.3.1 DC-link voltage controller without feed-forwarding of the load current

The DC-link voltage controller in this case consists of only a PI controller and it is shown in Fig B.11.

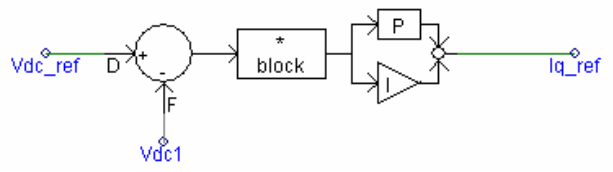

Fig B.11 Without feed-forwarding of the load current

V_{dc_ref} is the DC reference voltage that the controller is supposed to track and it is compared to the measured voltage V_{dc}. The output signal from the controller is the reference current I_{q_ref} and it is then fed into the active current I_q's controller, which can be seen in Fig B.5. The block which is in between the PI controller and the subtraction is used during start of the controller. During a short time the parameter block has the value zero and at that time the output from the controller is also zero. After that the parameter has the value one and does not affect the behaviour of the controller.

B.3.2 DC-link voltage controller with feed-forwarding of the load current

This controller is used when feed-forwarding of the load current is desired and differs on one point from the controller in B.3.1. That is I_{load} is added together with the output signal from the PI controller. In Fig B.12 the controller can be seen.

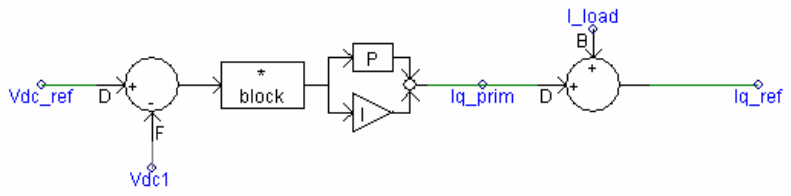

Fig B.12 With feed-forwarding of the load current

V_{dc_ref} is the DC reference voltage that the controller is supposed to follow and it is compared to the measured voltage V_{dc}. The output from the PI controller is add together with the signal I_{load} and the sum of these signals becomes the output from the controller, the reference current I_{q_ref}. It is then fed to the active current I_q's current vector controller, which can be seen in Fig B.5. In Section B.3.3 the calculation of I_{load} is described. The block which is in between the PI controller and the subtraction is used during start of the controller. During a short time the parameter block has the value zero and at that time the output from the controller is also zero. After that the parameter has the value one and does not affect the behaviour of the controller.

B.3.3 Scaling of the load current

Equation (B.5) and (B.6) express the active power at respective side of the VSC. If it is assumed that the power transmitted on the ac and dc side is the same and those losses in the converter and the filters are neglected.

$$P_{ac} = \frac{3}{2} \cdot v_{sq}(t) \cdot i_q(t) \tag{B.5}$$

$$P_{dc} = v_{dc}(t) \cdot i_{dc}(t) \tag{B.6}$$

$$\frac{3}{2} \cdot v_{sq}(t) \cdot i_q(t) = v_{dc}(t) \cdot i_{dc}(t) \tag{B.7}$$

The load on the DC side is only an active power load and therefore i_q is written as

$$i_q(t) = i_{load}(t) \tag{B.8}$$

Inserting (B.8) into (B.7) and after some rewriting following expression is given

$$i_{load}(t) = \frac{2}{3} \cdot \frac{v_{dc}(t)}{v_{sq}(t)} \cdot i_{dc}(t) \qquad \text{(B.9)}$$

The implementation of Equation (B.9) is shown in Fig B.13.

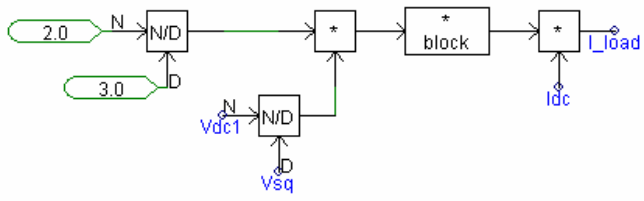

Fig B.13 The scaling of the load current

V_{dc1} is the measured DC-link voltage, V_{sq} is the q-component of the grid voltage and I_{dc} is the current measured at the DC side of the VSC.

Appendix C

Implementation of control model A in PSCAD/EMTDC

The objective of this chapter is to describe how the control system for control model A, described in Chapter 4, have been implemented in PSCAD/EMTDC. The different parts in the simulation model are described one by one.

C.1 System

In Fig C.1 the circuit that is used for the simulation test of the current vector controller is shown. For the simulation test of the DC-link voltage control the circuit differs on one point. The two voltage sources on the DC-link are removed and instead there is a current source. The current source is used to simulate load disturbances.

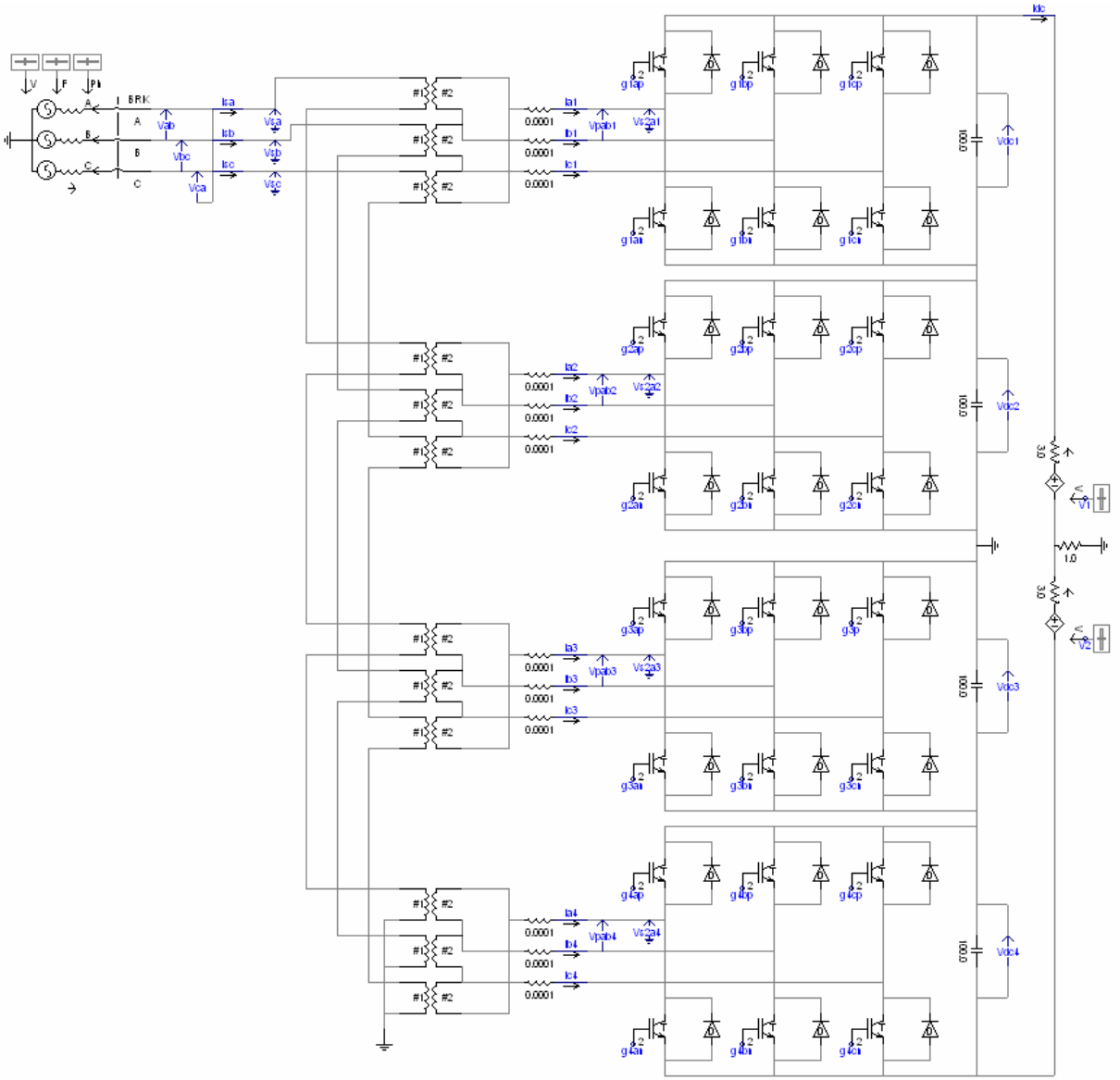

Fig C.1 Simulation circuit used when testing control model A

C.2 Implementation of current controller in PSCAD/EMTDC

The simulation model which is shown in Fig C.1 has been used and the controller that was presented in Chapter 4 has been built. Fig 4.6 shows an overview of the current controller and below the implementation of the different blocks is presented.

C.2.1 Transformation from three-phase system to dq-frame

The transformation of the three-phase quantities into the dq-frame is done in two steps. The first step is to transform the quantities to the αβ-frame and then from the αβ-frame to the dq-frame. The phase voltages and the currents in Fig C.1 are transformed to the dq-frame. That is done be implementing Equations (A.2) and (A.8). Fig C.2shows how the d-component of the phase voltages have been calculated and Fig C.3shows how the q-component was calculated. The transformation of the currents is done in the same way. The only thing that is done is that the voltages in the figures are changed to respective current.

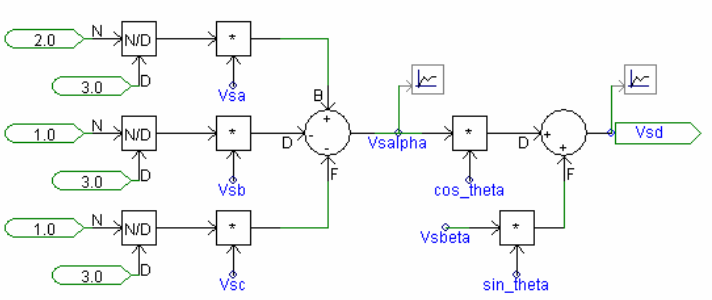

Fig C.2 Creation of d-component

The transformation is made as can be seen in the figures in two steps. First an amplitude invariant transformation from the three-phase system to the αβ-frame, it creates the quantities $V_{s\alpha}$ and $V_{s\beta}$. That is then followed by a transformation from αβ-frame to dq-frame. In figures that is the change from $V_{s\alpha}$ and $V_{s\beta}$ to V_{sd} and V_{sq}.

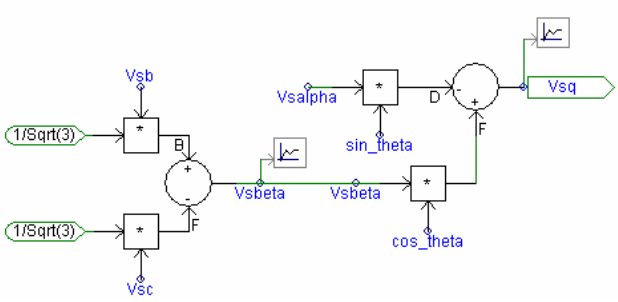

Fig C.3 Creation of q-component

In Section C.2.2 the calculation of the transformation angle is described.

C.2.2 Calculation of transformation angle

The transformation angle is very important in the controller and its object is to make the synchronisation with the grid correct. It is used when the transformation from αβ-frame to the dq-frame is done and in that way the dq-frame is synchronised with the grid. I this simulation the voltage vector $V_{\alpha\beta}$ is defined to be parallel with the q axis in the dq-frame and the transformation angle is defined as

$$\sin\theta = -\frac{V_{s\alpha}}{\left|V_{s\alpha\beta}\right|} \tag{C.1}$$

$$\cos\theta = \frac{V_{s\beta}}{|V_{s\alpha\beta}|} \tag{C.2}$$

How the implementation in PSCAD/EMTDC is done can be seen in Fig C.4. $V_{s\alpha}$ and $V_{s\beta}$ are the phase voltages which have been transformed to the αβ-frame.

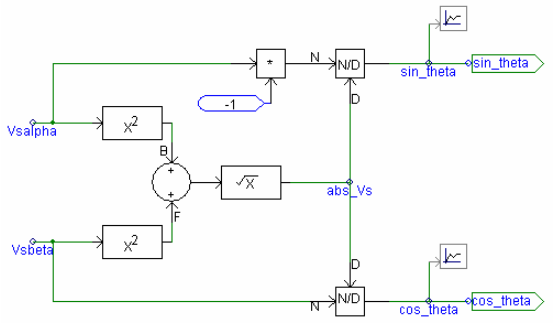

Fig C.4 Implementation of calculation of transformation angle in PSCAD/EMTDC

C.2.3 Current vector controller

The heart in the whole current controller is the current vector controller with PI controller, decoupling and feed-forwarding of the voltage. It is presented in Fig C.5 and it is divided into two parts, one for the d-component and one for the q-component.

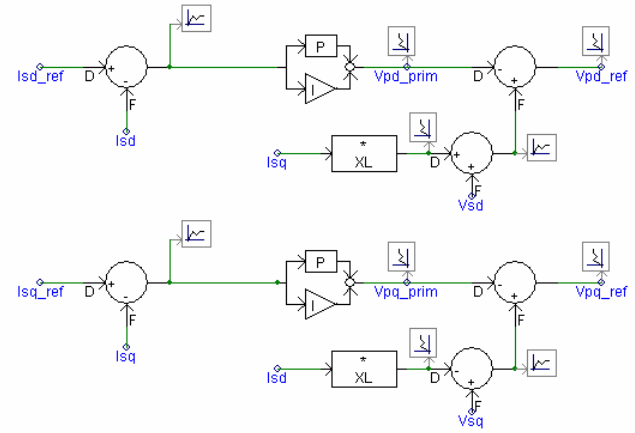

Fig C.5 The current vector controllers, the upper is the controller for the current I_d and the lower is the controller for the current I_q

I_{d_ref} and I_{q_ref} are reference currents that the controller is thought to follow. The decoupling terms are the signals that are received when the currents are multiplied with X_L, the grids reactance. The feed-forwarding is simply done by adding V_{sq} and V_{sd} to respective output signal. The output signal consists of two voltages. They represent the phase voltages reference for the VSC in the dq-frame. These two are then fed into the modulation index and load angle block.

C.2.4 Calculation of modulation index and load angle

The signals that are received from the vector controller, voltages in the dq-frame, must be transformed to three-phase signals. In this simulation this is done in two steps, first the modulation index and the load angle are calculated and after that the three-phase reference voltages are created. This is presented in Fig C.6 and Fig C.7. The other part is presented in Section C.2.5.

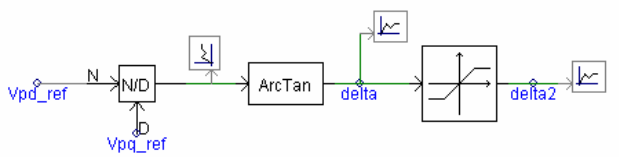

Fig C.6 Calculation of the load angle is implemented

Fig C.6 shows how the load angle is calculated and the mathematical expression is

$$\delta = \tan^{-1}\left(\frac{U_{pdref}}{U_{pqref}}\right) \tag{C.3}$$

Besides calculating the load angle there is a hard-limit, avoiding high angle values. Through this way the possibility to transfer a high amount of power is limited, which could otherwise damage the circuit.

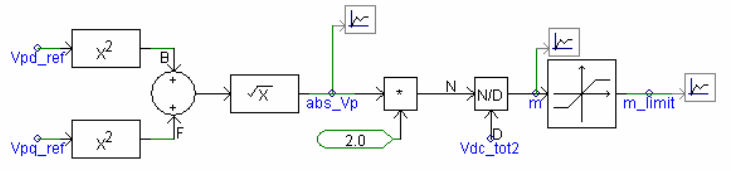

Fig C.7 Calculation of modulation index

Fig C.7 shows how the calculation of the modulation index is implemented in PSCAD/EMTDC and below is the equation that is used in the implementation.

$$m = 2 \cdot \frac{\sqrt{U_{pdref}^2 + U_{pqref}^2}}{V_{dc}} \tag{C.4}$$

Also for the modulation index there is a hard-limit and its purpose is to avoid a to high and low modulation index. If the modulation index would have a value higher than one then overmodulation is reached and a too low value leads to more harmonic contents. The goal is to have the modulation index within a span and in that way have a good operation of the system. Both the modulation index and the load angle are then input signals to the block which creates the three-phase reference voltages.

C.2.5 Creation of reference signals

To be able to create signals to the transistors some reference signals to the PWM is required. These are created from the modulation index and the load angle and the calculations can be seen in Section C.2.4. In Fig C.8 the creation of the reference signals are presented.

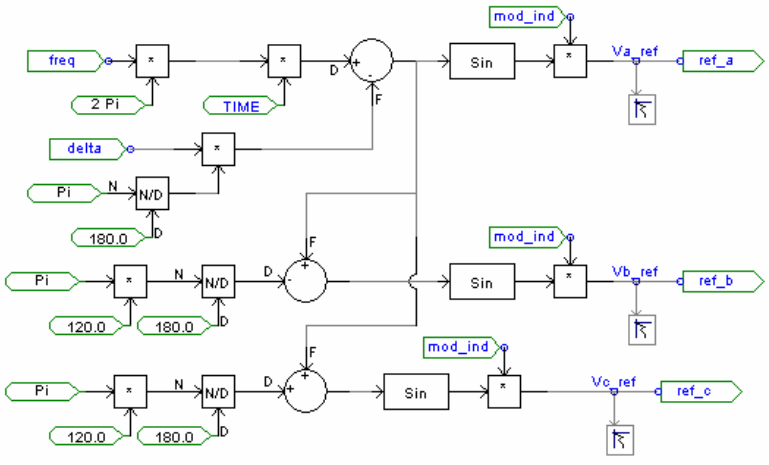

Fig C.8 Creation of three-phase voltages

Input signal to the block are modulation index m and load angle δ and out from the block comes three reference signals with peak value of one. The three signals represent the fundamental phase voltages at the AC side of the VSC. Thus there is a phase difference of 120 degrees between them and the output signal then goes to the PWM block.

C.2.6 Creation of gate pulses to the transistors

The creation of gate pulses is done in a following way, each reference signal is compared to a triangular wave. The triangular wave has a predetermined frequency, which also determines the switching frequency for the transistors. If the reference signal has a higher value than the triangular wave then the output is high. Instead if the reference signal has a lower value than triangular wave the output is low. When the output is high this means that the output signal has a value of one and with low is means that the output signal is zero. In this way a pulse train is created and it decides if the transistor should be on or off. In Fig C.9 it is shown how the implementation in PSCAD/EMTDC is done and there are three of these blocks, one for each phase. The output signal pwmA is taken to a block which creates the digital signals that the IGBTs use.

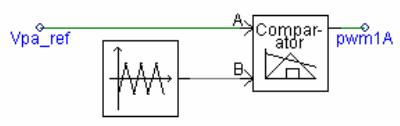

Fig C.9 The creation of the gate pulses

C.3 Implementation of DC-link Voltage Controller in PSCAD/EMTDC

As mentioned earlier, in this part the circuit in Fig C.1 has been changed. The controller is described in detail in Chapter 4 and an overview of the controller can be seen in Fig 4.6. Below the different parts of the controllers are presented.

C.3.1 Scaling of DC-link voltage

The scaling of the reference DC-link voltage and the measured DC-link voltage can be seen in Fig C.10.

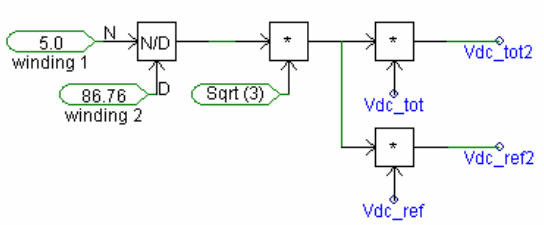

Fig C.10 Calculation of scale factor and vector scaling

The scaling is need since the DC-link voltage is measured on the converter side of the transformer. The scaling factor is

$$K = \frac{Winding\,1}{Winding\,2} \cdot \sqrt{3} \tag{C.5}$$

C.3.2 DC-link voltage controller

The DC-link voltage controller in this case consists of a PI controller and it is shown in Fig C.11.

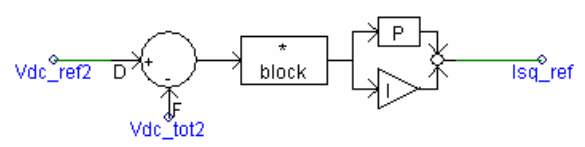

Fig C.11 DC-link voltage controller

V_{dc_ref} is the DC reference voltage that the controller is supposed to track and it is compared to the measured voltage V_{dc}. The output signal from the controller is the reference current I_{q_ref} and it is then fed into the active current I_q's controller, which can be seen in Fig C.5. The block which is in between the PI controller and the subtraction is used during start of the controller. During a short time the parameter block has the value zero and at that time the output from the controller is also zero. After that the parameter has the value one and does not affect the behaviour of the controller.

Appendix D

Implementation of control model B in PSCAD/EMTDC

The objective of this chapter is to describe how the control system for control model B, described in Chapter 4, have been implemented in PSCAD/EMTDC. The different parts in the simulation model are described one by one.

D.1 System

In Fig D.1Fig C.1 the circuit that is used for the simulation test of the current vector controller is shown. For the simulation test of the DC-link voltage control the circuit differs on one point. The two voltage sources on the DC-link are removed and instead there is a current source. The current source is used to simulate load disturbances.

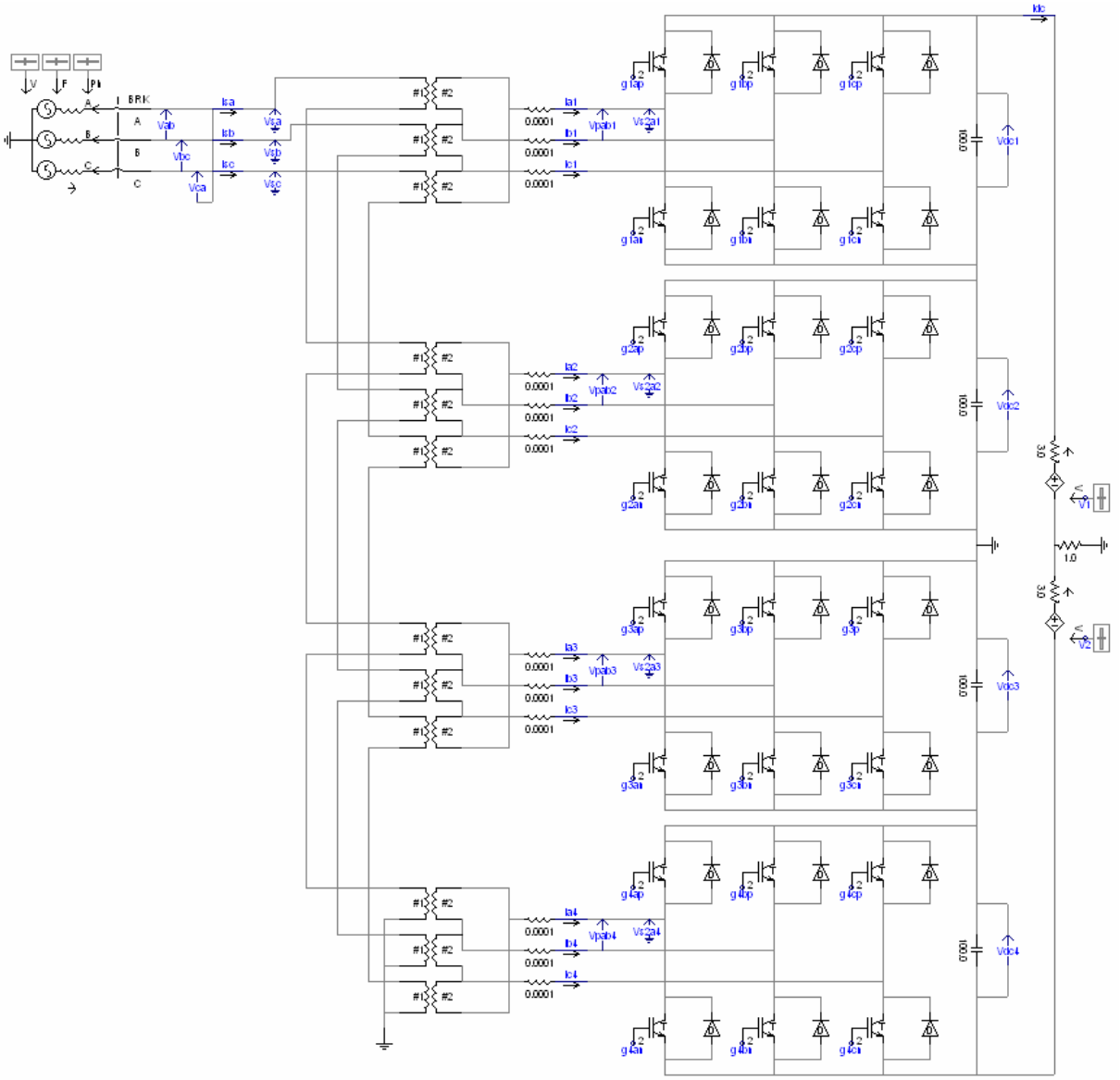

Fig D.1 Simulation circuit used during test on control model B

D.2 Implementation of current controller in PSCAD/EMTDC

The simulation model which is shown in Fig D.1 has been used and the controller that was presented in Chapter 4 has been built. Fig 4.10 shows an overview of the current controller and below the implementation of the different blocks is presented.

D.2.1 Transformation from three-phase system to dq-frame

The transformation of the three-phase quantities into the dq-frame is done in two steps. The first step is to transform the quantities to the αβ-frame and then from the αβ-frame to the dq-frame. The phase voltages and the currents in Fig D.1 are transformed to the dq-frame. That is done be implementing Equations (A.2) and (A.8). Fig D.2 shows how the d-component of the phase voltages have been calculated and Fig D.3 shows how the q-component was calculated. The transformation of the currents is done in the same way. The only thing that is done is that the voltages in the figures are changed to respective current.

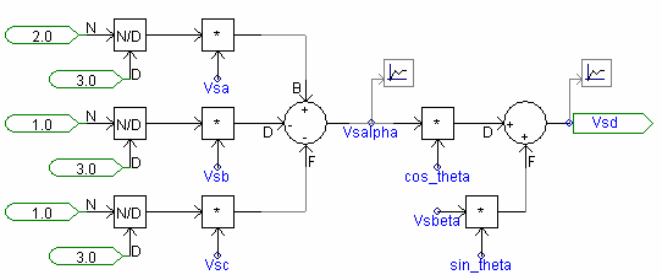

Fig D.2 Creation of d-component

The transformation is made as can seen in the figures in two steps. First an amplitude invariant transformation from the three-phase system to the αβ-frame, it creates the quantities $V_{s\alpha}$ and $V_{s\beta}$. That is then followed by a transformation from αβ-frame to dq-frame. In figures that is the change from $V_{s\alpha}$ and $V_{s\beta}$ to V_{sd} and V_{sq}.

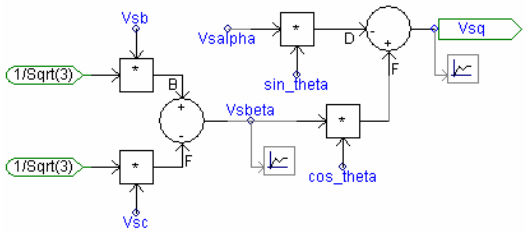

Fig D.3 Creation of q-component

In Section D.2.2 the calculation of the transformation angle is described.

D.2.2 Calculation of transformation angle

The transformation angle is very important in the controller and its object is to make the synchronisation with the grid correct. It is used when the transformation from αβ-frame to the dq-frame is done and in that way the dq-frame is synchronised with the grid. In this simulation the voltage vector $V_{\alpha\beta}$ is defined to be parallel with the q axis in the dq-frame and the transformation angle is defined as

$$\sin\theta = -\frac{V_{s\alpha}}{\left|V_{s\alpha\beta}\right|} \tag{D.1}$$

$$\cos\theta = \frac{V_{s\beta}}{|V_{s\alpha\beta}|} \tag{D.2}$$

How the implementation in PSCAD/EMTDC is done can be seen in Fig D.4Fig B.5. $V_{s\alpha}$ and $V_{s\beta}$ are the phase voltages which have been transformed to the αβ-frame.

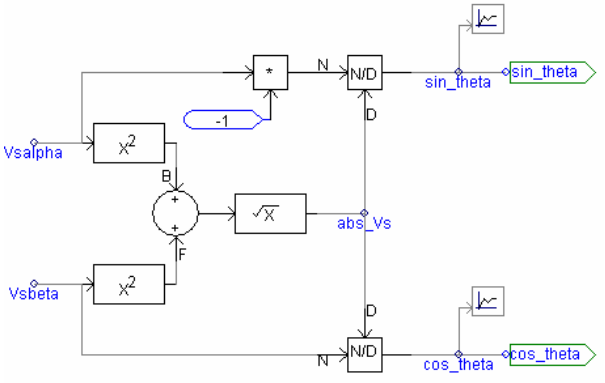

Fig D.4 Implementation of calculation of transformation angle in PSCAD/EMTDC

D.2.3 Current vector controller

The heart in the whole current controller is the current vector controller with PI controller, decoupling and feed-forwarding of the voltage. It is presented in Fig D.5, the d-component, and Fig D.6, the q-component.

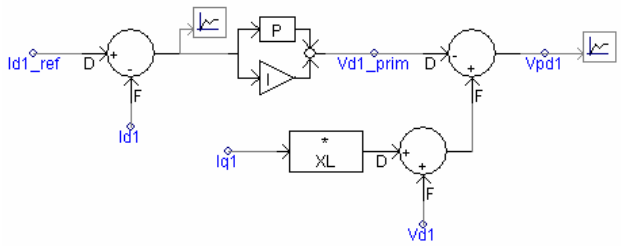

Fig D.5 The current vector controller for the current I_d

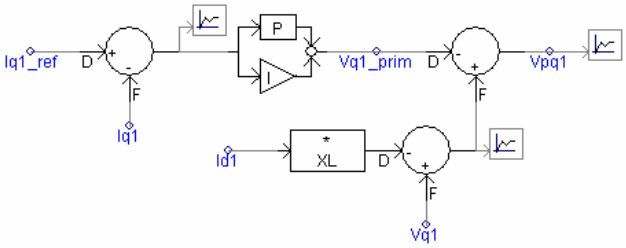

Fig D.6 The current vector controller for the current I_q

I_{d_ref} and I_{q_ref} are reference currents that the controller is thought to follow. The decoupling terms are the signals that are received when the currents are multiplied with X_L, the grids reactance. The feed-forwarding is simply done by adding V_{sq} and V_{sd} to respective output signal. The output signal consists of two voltages. The represent the phase voltages at the AC side of the VSC in the dq-frame. These goes then into the modulation index and load angle block.

D.2.4 Calculation of modulation index and load angle

The signals that are received from the vector controller, voltages in the dq-frame, must be transformed to three-phase signals. In this simulation this is done in two steps, first the modulation index and the load angle are calculated and after that the three-phase reference voltages are created. This is presented in Fig D.7 and Fig D.8. The other part is presented in Section D.2.5.

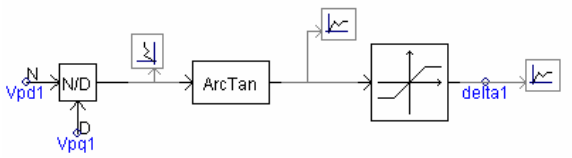

Fig D.7 Calculation of load angle

Fig D.7 shows how the load angle is calculated and the mathematical expression is

$$\delta = \tan^{-1}\left(\frac{U_{pdref}}{U_{pqref}}\right) \tag{D.3}$$

Besides calculating the load angle there is a hard-limit avoiding angle values. Through this way the possibility to transfer a high amount of power is limited, which could otherwise damage the circuit.

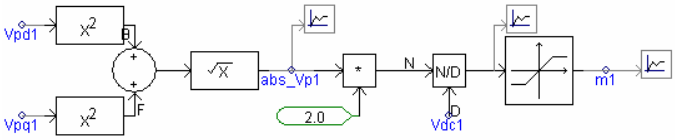

Fig D.8 Calculation of modulation index

Fig D.8 shows how the calculation of the modulation index is implemented in PSCAD/EMTDC and below is the equation that is used in the implementation.

$$m = 2 \cdot \frac{\sqrt{U_{pdref}^2 + U_{pqref}^2}}{V_{dc}} \tag{D.4}$$

Also for the modulation index there is a hard-limit and its purpose is to avoid a to high and low modulation index. If the modulation index would have a value higher than one then overmodulation is reached and a too low value leads to more harmonic contents. The goal is to have the modulation index within a span and in that way have a good operation of the system. Both the modulation index and the load angle are then input signals to the block which creates the three-phase reference voltages.

D.2.5 Creation of reference signals

To be able to create signals to the transistors some reference signals to the PWM is required. These are created from the modulation index and the load angle and the calculations can be seen in Section D.2.4. In Fig D.9 the creation of the reference signals are presented.

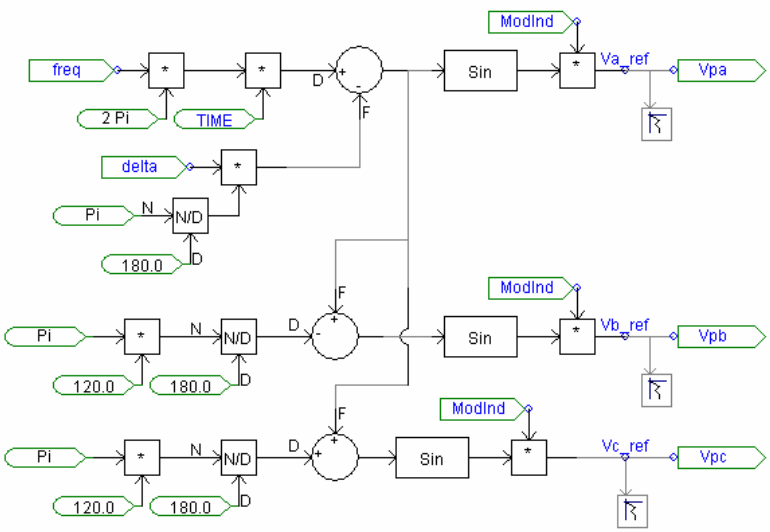

Fig D.9 Creation of three-phase reference voltages

Input signal to the block are modulation index m and load angle δ and out from the block comes three reference signals with peak value of one. The three signals represent the fundamental phase voltages at the AC side of the VSC. Thus there is a phase difference of 120 degrees between them and the output signal then goes to the PWM block.

D.2.6 Creation of gate pulses to the transistors

The creation of gate pulses is done in a following way, each reference signal is compared to a triangular wave. The triangular wave has a predetermined frequency, which also determines the switching frequency for the transistors. If the reference signal has a higher value than the triangular wave then the output is high. Instead if the reference signal has a lower value than triangular wave the output is low. When the output is high this means that the output signal has a value of one and with low is means that the output signal is zero. In this way a pulse train is created and it decides if the transistor should be on or off. In Fig D.10Fig B.10 it is shown how the implementation in PSCAD/EMTDC is done and there are three of these blocks, one for each phase. The output signal pwmA is taken to a block which creates the digital signals that the IGBTs use.

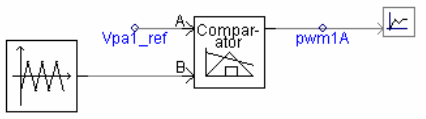

Fig D.10 The creation of the gate pulses

D.2.7 Scaling of grid voltages

The scaling of the grid voltages can be seen in Fig D.11.

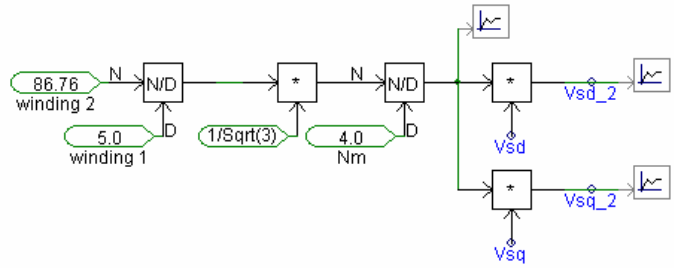

Fig D.11 Calculation of scale factor and vector scaling

The scaling is done because the grid voltages are measured on the grid side of the transformer while the other quantities are measured on the converter side of the transformer.

The scaling factor is

$$Y = \frac{Winding\ 2}{Winding\ 1} \cdot \frac{1}{N_m \cdot \sqrt{3}} \tag{D.5}$$

D.3 Implementation of DC-link Voltage Controller in PSCAD/EMTDC

As mentioned earlier, in this part the circuit in Fig D.1 has been changed. The controller is described in detail in Chapter 4 and an overview of the controller can be seen in Fig 4.10. Below the part of the controller is presented.

D.3.1 DC-link voltage controller

The DC-link voltage controller in this case consists of a PI controller and it is shown in Fig D.12.

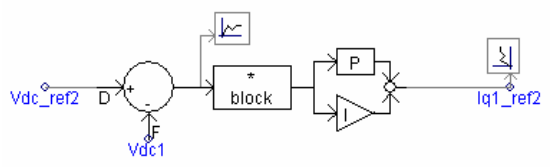

Fig D.12 DC-link voltage controller

V_{dc_ref} is the DC reference voltage that the controller is supposed to track and it is compared to the measured voltage V_{dc}. The output signal from the controller is the reference current I_{q_ref} and it is then fed into the active current I_q's controller, which can be seen in Fig D.6. The block which is in between the PI controller and the subtraction is used during start of the controller. During a short time the parameter block has the value zero and at that time the output from the controller is also zero. After that the parameter has the value one and does not affect the behaviour of the controller.