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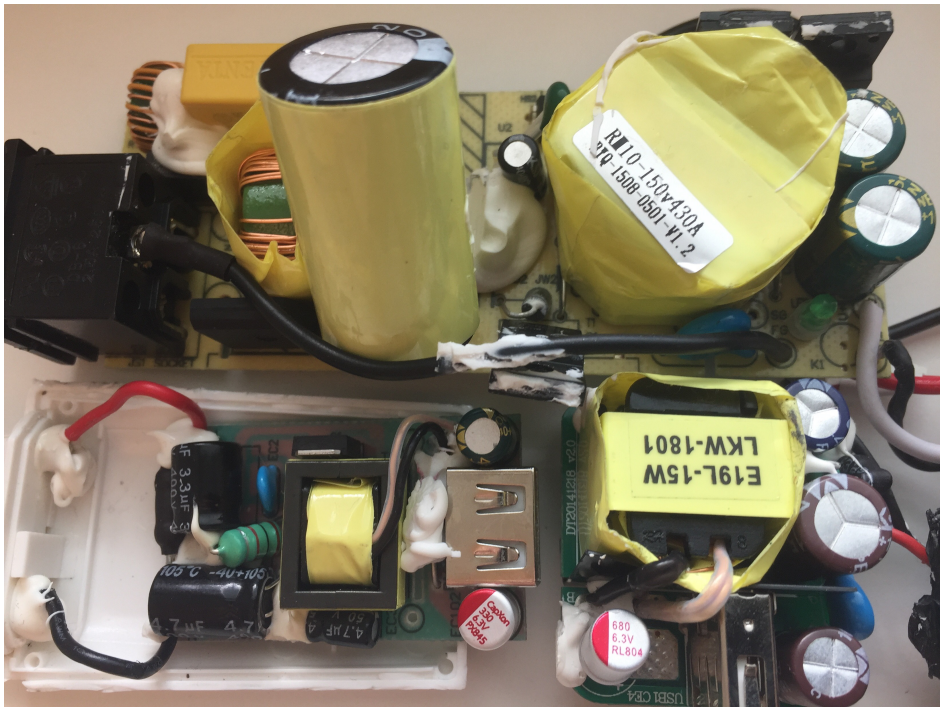

Efficiency Study of Isolated DC-DC Converters

– Through Simulation and Measurements

Master's Thesis in Electric Power Engineering

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Department of Electrical Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden, 2019

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Cover: Phone and laptop chargers of flyback topology.

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Abstract

Technological advancements of new devices put higher demands on power supplies to increase their power delivering capabilities. Simultaneously, to reach emission requirements, harder regulations are instated on the energy efficiency of power converters. Currently, the lowest efficiencies are seen for low power DC-DC converters, were the market is dominated by converters of flyback topology. To keep up with the demand for higher power and efficiency, ways of improving the flyback's efficiency as well as the possibility of using other converter topologies are investigated. A criterium for the converter topologies in this study was the need for galvanic isolation, thus the flyback, forward and LLC bridge converter were chosen for further investigation. The converters were designed and then implemented for evaluation in the electronic circuit simulation software LTspice. As a validation of the simulations, electrical measurements on similar converters from phone and laptop chargers were performed. The results from the measured and simulated efficiency curves both showed similar drops in efficiency at partial loading below 20% of the rated load. From the simulations the converter with the highest attainable efficiency over the entire operating region were the LLC bridge converter followed by the forward and lastly the flyback. The largest losses in the converters were caused by the diode and transformer, however the exact loss distribution depends on component choice. The efficiency could be further increased by implementation of synchronous rectification, for which the losses in the LLC converter were reduced by 64.1% and the peak efficiency reached 97.3%.

Keywords: DC-DC converter topology, flyback, forward, LLC, partial loading, synchronous rectifier.

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Rasmus Karlsson & Vetle Huse Syversen, Gothenburg, June 2019

Contents

1
Introduction

1.1 Background

The demand for energy is constantly increasing due to rising populations and higher living standards around the world [1]. At the same time the energy consumption needs to decrease if our society is to be able to lessen the effects of climate change. Thus energy efficiency is becoming more important and higher demands are put on applications to follow these ever stricter standards. In the field of power transmission, research is currently going into transitioning from the now dominant alternating current (AC) power grid into direct current (DC). In electrical devices, the conversion from the AC grid voltage to DC voltage is handled by a rectifier circuit followed by a DC-DC converter. Thus, if the power grid was DC, the AC-DC rectification would no longer be needed and the efficiency of the device could be increased. It also makes it more convenient to implement renewable technologies like solar photovoltaic which would move the power generation directly to the consumer [2, 3].

Both the AC-DC rectifier and the DC-DC converter contributes to total losses, however most comes from the DC-DC converter. A number of DC-DC converters had their efficiencies measured at Chalmers. The tested converters were of flyback topology and had an average measured efficiency in the range of $67-81\%$ depending on the loading [3]. By conducting a study of why these losses take place and how they could be reduced, the possibilities for higher efficiency DC-DC converters can be examined. The lowest efficiency is generally seen for low power converters as small voltage drops can have a major impact on the overall efficiency. Thus, by comparing different low power converter topologies, methods for optimizing efficiency can be evaluated.

1.2 Aim & Scope

The aim of this thesis is to identify and compare different DC-DC converter topologies for low power applications in the range of $5 - 15W$, to establish their efficiency at rated power and behaviour during partial loading. Possibilities to further increase the efficiency of each converter topology is also going to be investigated. The converter efficiency study is going to be conducted through simulation, using the electronic circuit simulator LTspice. To evaluate the simulation results and establish the current state of commercial converters, electrical efficiency measurements will be performed on purchased converters having similar power levels.

1.3 Thesis Outline

- **2. Theory**
  The flyback, forward and LLC converter topology and operation is investigated. A review of the key components within the converters are conducted and possibilities for further efficiency improvement are discussed. The EMI, error propagation and present value analysis are also covered briefly.
- **3. Method**
  The purchased DC-DC converters are introduced and the methodology for performing electrical measurements are summarized. Then the design procedure for the flyback, forward and LLC converter in LTspice is explained and the component choice is justified.
- **4. Results**
  The flyback, forward and LLC converter implemented into LTspice are evaluated in terms of power dissipation to compare their relative efficiency for partial loading. As well as which components are the major contributors to lowering efficiency. A short look at the effects of leakage inductance, the impact of transformer winding choice and an economical evaluation of SR are also conducted.
- **5. Discussion**
  The results obtained from the simulations and electrical measurements are discussed and compared.
- **6. Future Work**
  Description and possibilities of providing more reliable design models and implementation of further efficiency improvement topologies for future work.

2
Theory

2.1 DC/DC Converters

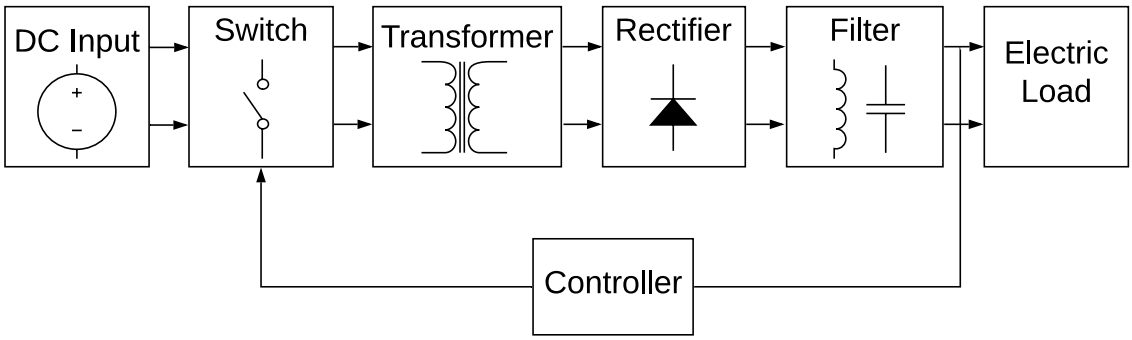


Figure 2.1: Isolated DC/DC converter block diagram

Almost every appliance and device in today's household operates on DC voltage and thus require some type of voltage conversion going from the conventional (230) AC electrical outlet. Especially challenging is the DC-DC conversion for devices containing digital circuits and LED-drivers because they generally require low voltages. Thus, even a small voltage drop can have a large impact on the total efficiency which limits the power density of the device. A general isolated DC-DC converter is shown in Fig. 2.1, with the transformer providing electrical isolation. Due to safety requirements and high voltage conversion ratios, an isolation transformer within the converter is often a requirement [4]. The transformer provides electrical isolation and thus prevents current ground loops as well as providing the freedom to step up or step-down voltages [4]. There is also the benefit of preventing high voltage and current transients from reaching the output of the converter. As the converters in this study are designed with low output voltages, low power levels as well as galvanic isolation, the converter topologies in Table 2.1 have been selected. Typical power levels for each topology is shown to indicate when they are most commonly used. More about the topology and operation of the three DC/DC converters will be further explained in the chapters below.

Table 2.1: common power range for the given topologies [5]

Topology	Flyback Converter	Forward Converter	Half-Bridge LLC
Typical Power Range [W]	0 - 150	50 - 500	100 - 1000

2.2 Flyback Converter

The most commonly used low power converter topology that provides galvanic insulation today is the flyback converter, as it can be produced at low cost due to the small component count [6]. The flyback converter, which can be seen in Fig. 2.2, is derived from the buck-boost converter with the addition of a transformer operating as a coupled inductor. Another difference from the buck-boost converter is that the flyback output voltage is the same polarity as the input. This because the polarity of the secondary transformer winding is inverted to provide a positive output voltage during the discharge cycle. The transformer is used as energy storage during switching cycles as well as providing galvanic insulation and voltage regulation.

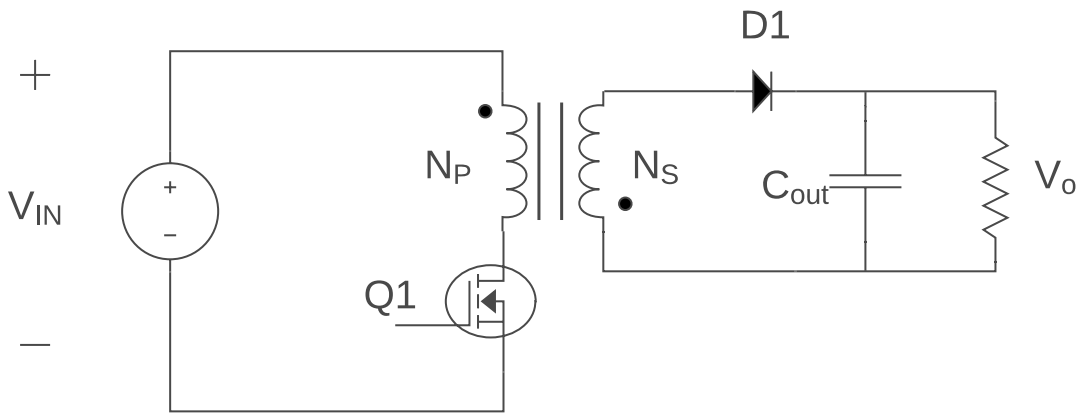


Figure 2.2: A Flyback converter circuit model

The voltage and current path during switch on and switch off are presented in Fig. 2.3. When the switch is on as shown in Fig. 2.3 (a), the primary current flows through the primary winding and charges the transformer. Due to the arrangement of the winding, a negative voltage will be induced across the secondary winding thus reverse biasing the rectifying diode, preventing the core from discharging over the load. As the primary switch turns off as shown in Fig. 2.3 (b), the polarity on the secondary winding is reversed, causing the diode to be forward biased. The flyback transformer can then freely discharge the stored energy onto the load [6, 7].

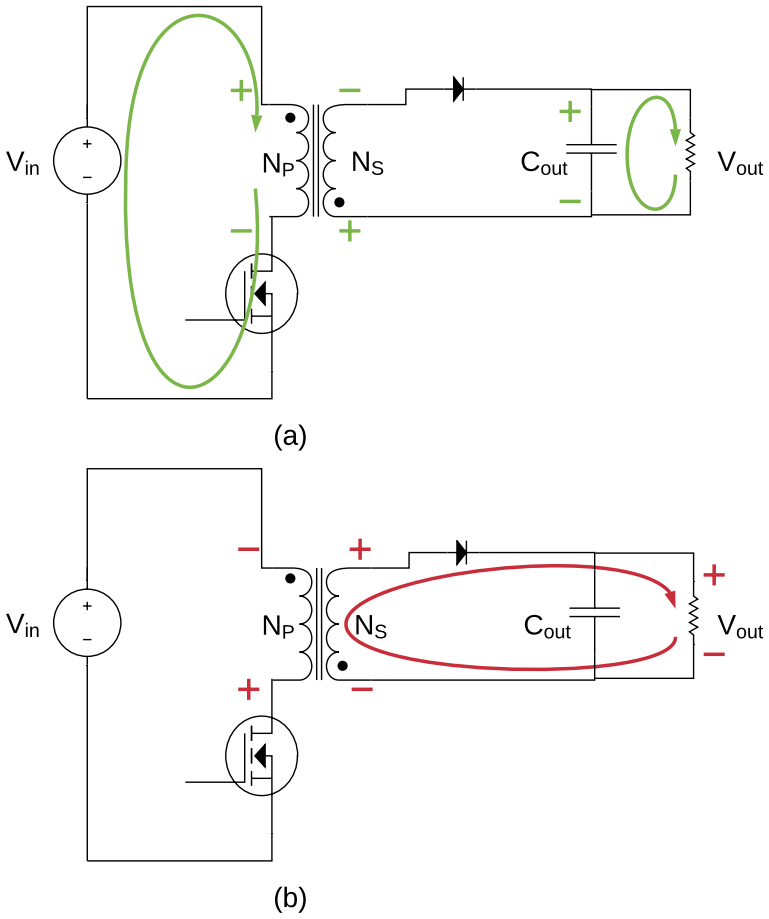


Figure 2.3: Conduction mode for a flyback converter; (a) the switch is turned on and (b) the switch is turned off.

2.2.1 Discontinuous Conduction Mode

The behaviour of the current through the flyback can be defined based on two different operating modes, discontinuous conduction mode (DCM) and continues conduction mode (CCM). In this section, DCM is presented. A converter operating in DCM discharges the transformer core fully each switching cycle. The relation between input and output voltage for a flyback converter operating in DCM is

$$\frac{V_o}{V_{in}} = D\sqrt{\frac{RT_s}{2L_m}} \tag{2.1}$$

where V_o and V_{in} are the output and input voltage respectively. D is the duty cycle and T_s is the switching period, L_m is the transformer magnetizing inductance and R is the load resistance.

The voltage across the switch and the transformer currents for a flyback operating in DCM can be seen in Fig. 2.4, where the switch is conducting during the time t_{on} and blocking during time t_{off}. During t_{on}, current increases linearly through the magnetizing inductance and builds up magnetic flux in the transformer until the switch turns off.

As the switch is turned off the voltage across the secondary winding reverses and forward biases the diode. The secondary current I_{SEC} starts flowing and demagnetizes the core fully over the time period t_{Demag}. The demagnetization time may vary, depending on the load. During the switch off-time t_{off}, the voltage across the switch is the sum of input voltage and reflected output voltage. During switching a voltage ripple may appear, marked by the first red circle in Fig. 2.4, caused by resonant between switch node capacitance and leakage inductance. This voltage ripple can be reduced by implementing a snubber or active clamp circuit and is an important factor when deciding what transistor to use in the circuit [6, 7].

The time period noted t_{DEAD} in Fig. 2.4 describes the time were I_{SEC} has reached zero. During this time there is resonant ringing between the transformer primary winding inductance and the switch capacitance, indicated by the second red circle. By utilizing valley switching, the switching losses can be reduced drastically by turning on the switch when the ringing voltage is at its lowest point [6].

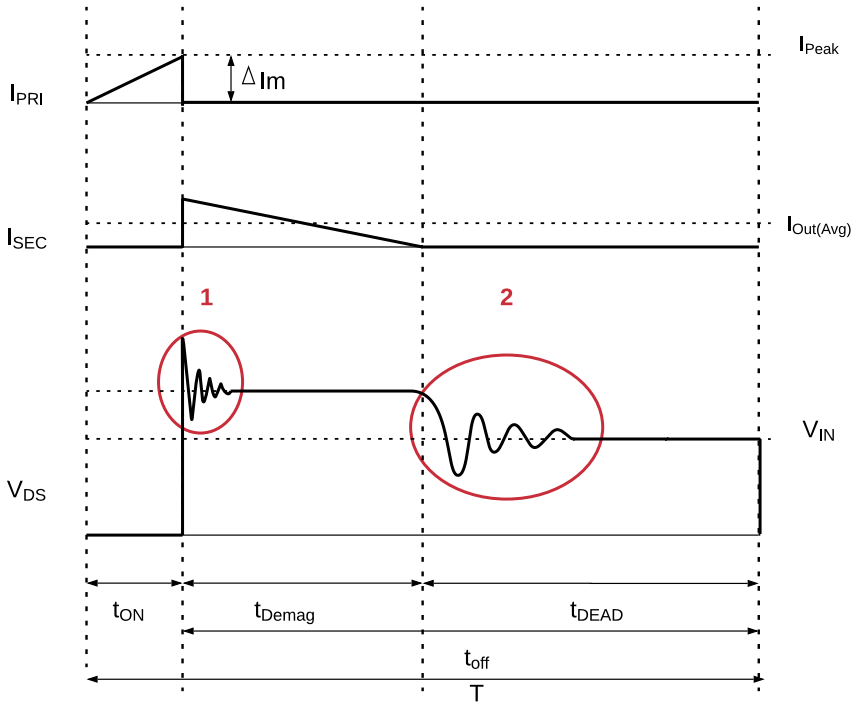


Figure 2.4: Current and voltage behaviour of a flyback operating in DCM.

One of the advantages with DCM operation, is the absence of reverse recovery current from the diode. This is due to that the secondary current through the diode is allowed to go to zero, which does not occur for CCM. Another advantage is that the flyback requires a smaller inductance due to higher current di/dt which reduces the size of the magnetic components. However, the large ripple currents in DCM leads to high rms currents and increases the conduction losses in the circuit [6].

When designing a flyback converter, a design parameter called the ripple factor, K_{RF}, is introduced [8]. This parameter allows the designer to chose a desired current ripple for the converter. The ripple factor is defined as

$$K_{RF} = \frac{\Delta I}{2I_m} \tag{2.2}$$

where K_{RF} is the ratio between the peak to peak current ripple ΔI and the average current through the magnetizing inductance I_m. The ripple current and magnetizing inductance can be calculated from

$$\Delta I = \frac{V_{in}D}{L_m f_s} \tag{2.3}$$

$$I_m = \frac{P_{in}}{V_{in}D} \tag{2.4}$$

where f_s is the switching frequency and P_{in} is the input power [9]. For a converter made to operate in DCM, $K_{RF} = 1$ and thus there is no DC component to the current. This can be seen in Fig. 2.4 where $2I_{Out(Avg)} = \Delta I$.

By combining (2.2) – (2.4), the magnetizing inductance of the transformer can be written as

$$L_m = \frac{(V_{in,min}D_{max})^2}{2P_{in}f_s K_{RF}} \tag{2.5}$$

The peak and rms current through the switch are then calculated as

$$I_{m,peak} = I_m + \frac{\Delta I}{2} \tag{2.6}$$

$$I_{m,rms} = \sqrt{\frac{D}{3}\left[3(I_m)^2 + \left(\frac{\Delta I}{2}\right)^2\right]} \tag{2.7}$$

To get an even output voltage, a filter capacitor needs to be implemented to the output. The output capacitor is thus calculated as

$$C_{Out} = \frac{\Delta I_o}{8f_s \Delta V_{Out}} \tag{2.8}$$

where ΔV_{Out} is the maximum allowed output voltage ripple [7].

2.2.2 Continuous Conduction Mode

The second conduction mode is continuous conduction mode (CCM) where the converter transfer function is expressed by

$$\frac{V_o}{V_{in}} = \frac{1}{n}\frac{D}{1-D} \tag{2.9}$$

In this mode the output voltage only depends on the duty cycle D and the winding ratio n, which is

$$n = \frac{N_p}{N_s} \tag{2.10}$$

where N_p is the number of primary side windings and N_s is the number of secondary side windings [6]. The voltage across the switch and current through the transformer of a flyback in CCM is presented in Fig. 2.5.

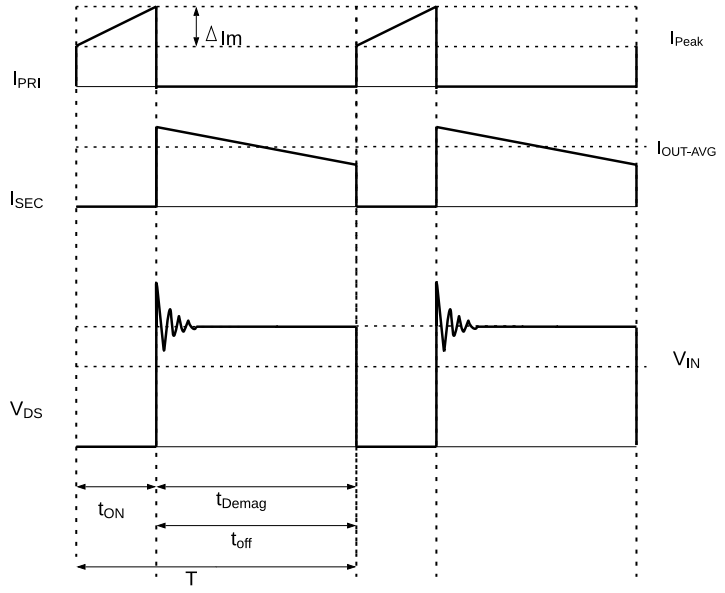


Figure 2.5: Current and voltage behaviour of a flyback operating in CCM.

In this mode there is always a current flowing through one of the transformer windings, thus there is no dead time and the current ripple and rms value is kept lower than for DCM. This also gets rid of the ringing usually occurring during the dead time making valley switching impossible. Due to lower rms current, CCM operation is generally preferred for higher loads although it is inevitable to enter DCM when the loading decreases far enough. Thus, converters designed for CCM normal operation also features a controller made to handle DCM operation.

The design steps for a flyback converter for CCM operation is similar to one for DCM operation, however now the ripple factor should be $K_{RF} < 1$. This can be seen in Fig. 2.5 where $2I_{OUT-AVG} > \Delta I$ as there is a DC component to the current. A common value for the ripple factor is $K_{RF} = 0.4-0.8$ for European appliances [8].

2.3 Forward Converter

The forward converter share many similarities with the flyback converter, however energy is not stored in the transformer, but directly transferred to an output inductor. This means smaller ripple currents to the output which reduces the size of the output capacitor [10]. The Forward converter is derived from the buck converter, but is implemented with a transformer, providing galvanic isolation and the possibility to step the voltage. The circuit topology of a forward converter can be seen in Fig 2.6.

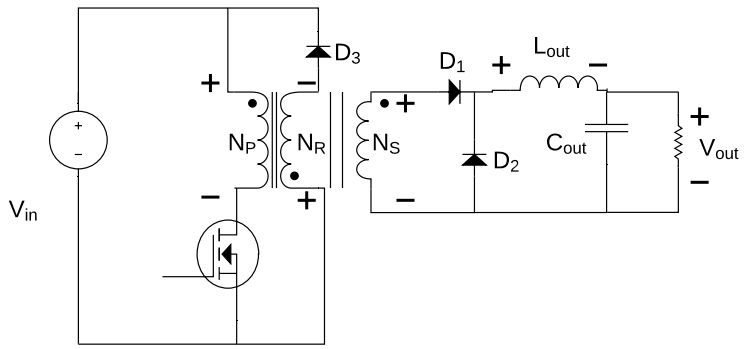


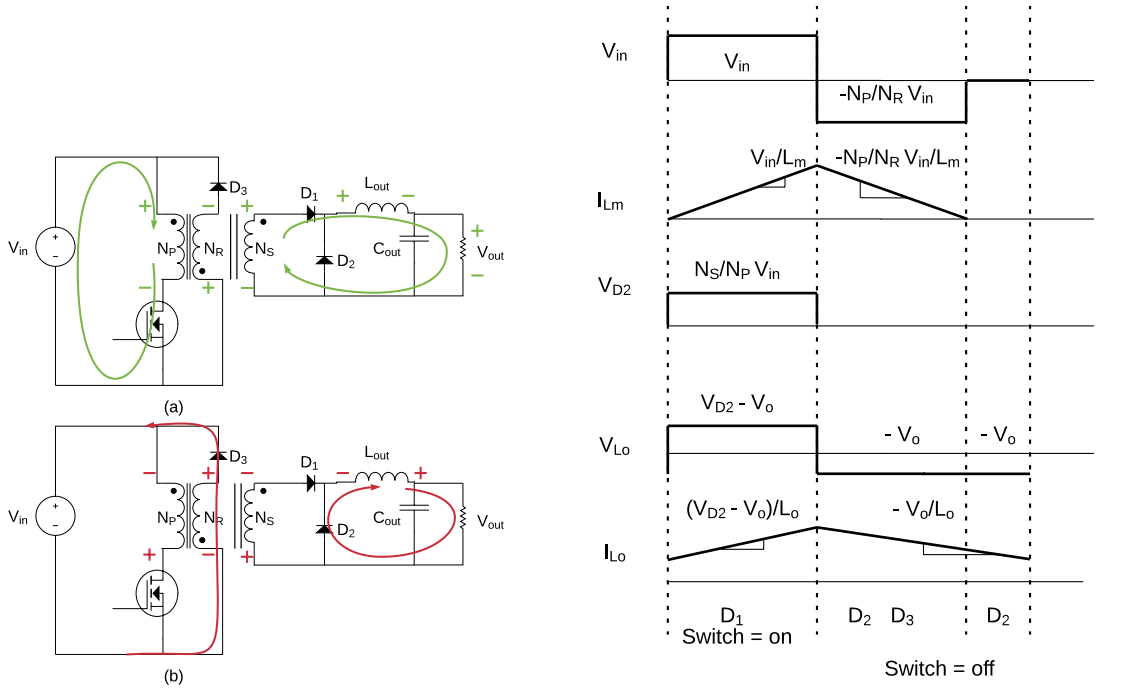
Figure 2.6: Forward converter circuit model

Because the forward converter is derived from a buck converter, their transfer functions share some similarities, the only difference is the inclusion of the transformer turns ratio [11]. The transfer function is therefore given as

$$\frac{V_o}{V_{in}} = D\frac{N_s}{N_p} \tag{2.11}$$

where the relationship between the number of primary and secondary windings provides flexibility for the voltage conversion.

Due to the immediate energy transfer between primary and secondary, the stored energy caused by the magnetizing current in the transformer is not discharged by the output voltage. This introduces the need of a third winding, called reset winding which prevents the magnetizing current to increase for every switching cycle. The discharge behaviour of the voltage and current caused by the reset winding can be seen in Fig. 2.7, where Fig. 2.7 (a) shows the current path and voltage polarity during turn on and turn off and Fig. 2.7 (b) shows the current and voltage waveforms. [10, 11].



(a) Current path and voltage polarities of the forward converter during on and off

(b) Current and voltage waveforms of the forward converter during on and off.

Figure 2.7: Current and voltage behaviour of forward converter during turn on and turn off.

During conduction mode input voltage V_{in} reverse biases diode D3. The voltage reflected to the secondary side forward biases diode $D1$, thus voltage across the inductor can be expressed by [4, 10, 11]

$$V_{Lout} = \frac{N_s}{N_p} V_{in} - V_o \tag{2.12}$$

The inductor voltage behavior during turn on can be seen in Fig. 2.7 (b) which increases linearly with

$$\frac{di}{dt} = \frac{V_{Lout}}{L_{out}}. \tag{2.13}$$

When the switch turns off, energy stored in L_{out} begins to discharge onto the load. The voltage over the primary winding will change polarity connecting the primary inductor in series with the input voltage causing high voltages over the switch [11]. The switch voltage V_S can be calculated as

$$V_S = V_{in} + \frac{N_p}{N_r} V_{in}. \tag{2.14}$$

where N_r is the number of windings to the reset winding. Simultaneously, the reflected voltage forward biases $D3$, providing a current path for the magnetizing current and thereby resetting the magnetic field in the transformer. On the secondary side during turn-off, the voltage over the output inductor is clamped by the freewheeling diode $D2$ and discharges the output inductor onto the load. [4, 10, 11]

2.4 LLC Resonant Bridge Converter

A resonant bridge converter is a type of bridge converter that utilizes a network of inductors and capacitors, called a resonant tank, to regulate gain as well as to achieve lower losses through zero voltage switching (ZVS). By changing the configuration of the elements within the resonant tank, different converter characteristics around a resonant switching frequency can be obtained. The topology for an LLC half-bridge converter with full wave rectification can be seen in Fig. 2.8. The resonant tank is located in between the switching bridge and rectifier stage. The bridge LLC converter requires a high number of components compared to the other topologies but is naturally able to achieve ZVS [12]. The converter is also able to operate for a wide load and still maintain high efficiency [12].

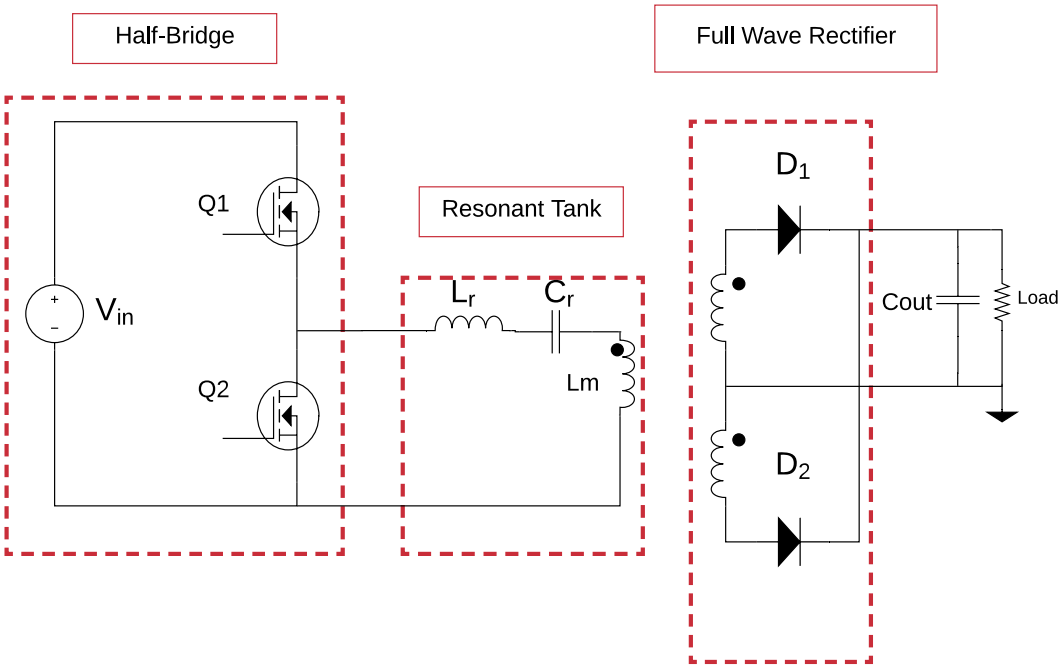


Figure 2.8: A LLC half-bridge converter with a full-wave rectifier.

As indicated by its name, the resonant tank of the LLC bridge converter consists of two inductors L_r, L_m and one capacitor C_r, where L_m is the magnetizing inductance of the transformer. Because the LLC has two inductors, the circuit has two resonant frequencies and is thus also known as a multi-resonant converter.

The switching bridge can either be implemented with four switches to form a full bridge, or with two to form a half bridge. The half bridge topology outputs half the voltage of a full bridge, thus the transformer require half the amount of windings. However, this has the implication that the primary current through the half bridge switches and transformer winding will be twice as high as that of the full bridge, leading to higher conduction loss. A comparison between half bridge and full bridge converters can be seen in Table 2.2.

Table 2.2: Switching bridge: Half bridge compared to full bridge

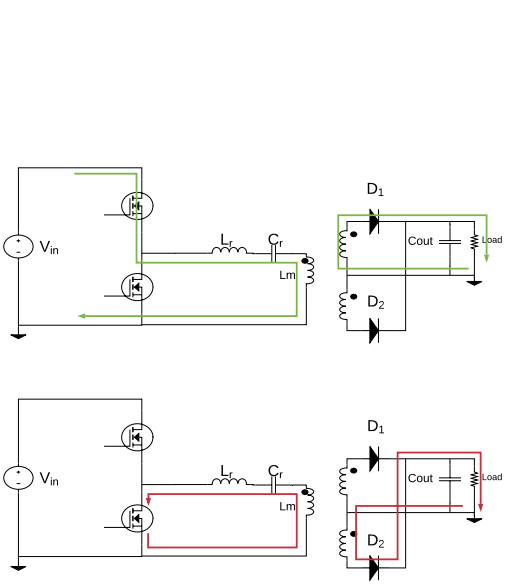
I_{rms}	Number of Switches	Primary windings	Total conduction loss for switches	Transformer primary copper loss
$\times$ 2	$\div$ 2	$\div$ 2	$\times$ 2	$\times$ 2

As for the output rectifier, it can either be implemented as a full bridge rectifier or a full wave rectifier. The difference is that the full wave rectifier uses two diodes instead of four, and two secondary side winding coils instead of one. Thus, the full wave rectifier has twice the winding losses, but half the diode losses compared to the full bridge rectifier. The voltage rating of the diodes also needs to be two times larger for the full wave rectifier. A comparison between full wave and full bridge rectifiers can be seen in Table 2.3 [13].

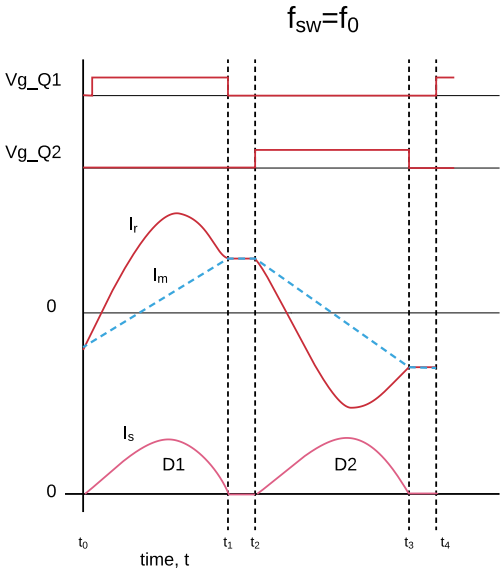
Table 2.3: Rectifier: Full wave compared to full bridge

Diode voltage rating	Number of diodes	Total diode conduction losses	Number of secondary windings	Transformer secondary copper loss
$\times$ 2	$\div$ 2	$\div$ 2	$\times$ 2	$\times$ 2

The operation of the LLC converter from input to output starts with the switch bridge circuit which generates a square wave voltage, with a switching frequency close to the resonant frequency of the resonant tank elements. The resonant tank acts as a filter to create a sinusoidal current and a bipolar square wave voltage, with a gain depending on the switching frequency of the switch bridge. The voltage gets scaled by the transformer ratio, rectified by the full wave rectifier and smoothed by the output capacitor. The conduction cycles can be seen in Fig. 2.9 (a) and current and voltage waveforms can be seen in Fig. 2.9 (b) [13]. It is during the dead time between t_1 and t_2 that the condition for ZVS occurs.



(a) Current path of the LLC converter during turn on and turn off



(b) Current and voltage waveforms of the LLC during switch on and off.

Figure 2.9: Current and voltage behaviour of half bridge LLC converter during turn on and turn off.

The LLC bridge converter resonant tank enables the possibility to step up and step down voltages while attaining low switching losses. During normal operation the gain of the resonant tank is in unity as this is the preferable operation mode that causes the converter to operate at maximum efficiency [12]. Depending on the application of the converter and on expected input and output voltage fluctuations, the minimum gain $M_{g(min)}$ and maximum gain $M_{g(max)}$ needed can be specified according to

$$M_{g(min)} = \frac{n \cdot V_{o(min)}}{V_{in(max)}} \tag{2.15}$$

$$M_{g(max)} = \frac{n \cdot V_{o(max)}}{V_{in(min)}} \tag{2.16}$$

As previously stated, the resonant tank, is multi-resonant and its gain varies with the switching frequency. Thus, there is no duty cycle control for the bridge switches but instead the duty cycle is kept at 50% and only the switching frequency is varied. The gain of the resonant tank can be obtained from an equivalent AC circuit seen in Fig. 2.10, derived using the first harmonic approximation (FHA). Using FHA means to approximate the input square wave voltage with its first harmonic component, due to the filtering of the resonant tank. The magnitude of the fundamental voltage component from a half bridge is

$$V_{FHA} = \frac{2}{\pi} V_{DC} \tag{2.17}$$

The voltage across the transformer, before the rectifier, is a bipolar square wave voltage that has the fundamental component

$$V_{ac(out)} = \frac{4 \cdot n \cdot V_o}{\pi} \tag{2.18}$$

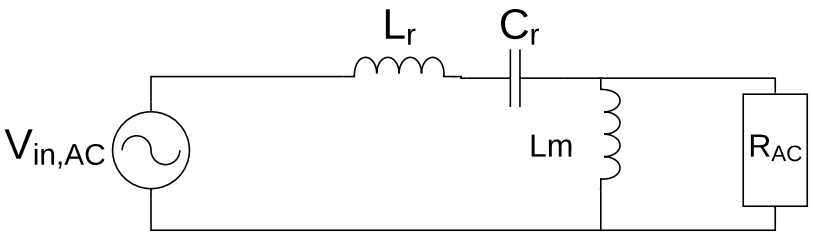


Figure 2.10: The equivalent AC model of the LLC converter.

The input power P_{in} to the AC model in terms of the AC current I_{ac} and the load R_{ac} from (2.21) is

$$P_{in} = I_{ac,rms}^2 \cdot R_{ac} = \frac{I_{ac,peak}}{\sqrt{2}} R_{ac} = \frac{I_{ac,peak}^2}{2} R_{ac} \tag{2.19}$$

The output power to the actual load R_{out} depends on the DC current $I_{out,DC}$ through the load as

$$P_{out} = I_{out,dc}^2 \cdot R_{load} = (\frac{2}{\pi} I_{ac,peak})^2 R_{load} = \frac{4R_{load}}{\pi^2} I_{ac,peak}^2 \tag{2.20}$$

By equating the efficiency of the converter to 100%, so that $P_{in} = P_{out}$, the input power corresponds to the output power and thus the equivalent AC resistance equals

$$R_{ac} = \frac{8n^2}{\pi^2} R_{out} \tag{2.21}$$

where n is the turns ratio of the transformer and R_{out} is the actual output resistance. From the equivalent LLC circuit in Fig. 2.10, it is apparent that as the AC resistance R_{ac} changes, so does the equivalent circuit. Thus, the influence of L_r and L_m will vary with the load. Two extreme cases can be used to illustrate this. First when the loading is high, R_{ac} has a much lower value than the magnetizing inductance $R_{ac} << L_m$, thus L_m can be neglected. Secondly when the loading is zero the opposite is true, so $R_{AC} >> L_m$ and the resistor can be neglected. Both equivalent LC circuit will have different resonance frequencies, the first one being

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.22}$$

where f_{r1} is the resonance frequency for $R_{ac} << L_m$, for which the output voltage gain is one or lower [14]. The second resonance frequency is then given as

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2.23}$$

for $R_{AC} >> L_m$, for which the output voltage gain is larger than one. The ratio between L_r and L_m,

$$m = \frac{L_m}{L_r} \tag{2.24}$$

can be used to describe the influence of the f_{r2} gain on the f_{r1} gain. For $m = 0$ the magnetizing inductance is zero and thus it wont influence the F_{r1} gain. Similarly if m is very high f_{r2} will be too far away from f_{r1} to have any real impact on its gain. To be able to have a gain above and below one the ratio should be within $0 < m < \infty$.

Another useful factor to describe the resonant gain is the quality factor Q, defined as

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{AC}} \tag{2.25}$$

Which can also be written as

$$Q = \frac{L_r \omega_r}{R_{AC}} \tag{2.26}$$

where ω_r is the resonant frequency of the LC circuit with elements L_r and C_r [14]. The value of Q describes how fast the voltage gain drops when deviating from f_{r1}. For a larger Q the gain will drop faster around the resonant point and thus the influence of the gain from f_{r2} will be lessened. By performing an AC analysis on the equivalent circuit model from Fig. 2.10, the converter gain due to different choices of quality factors is visualized in Fig. 2.11 for $m = 4$. Thus for low values of Q, which is for low loads, high gains are attainable.

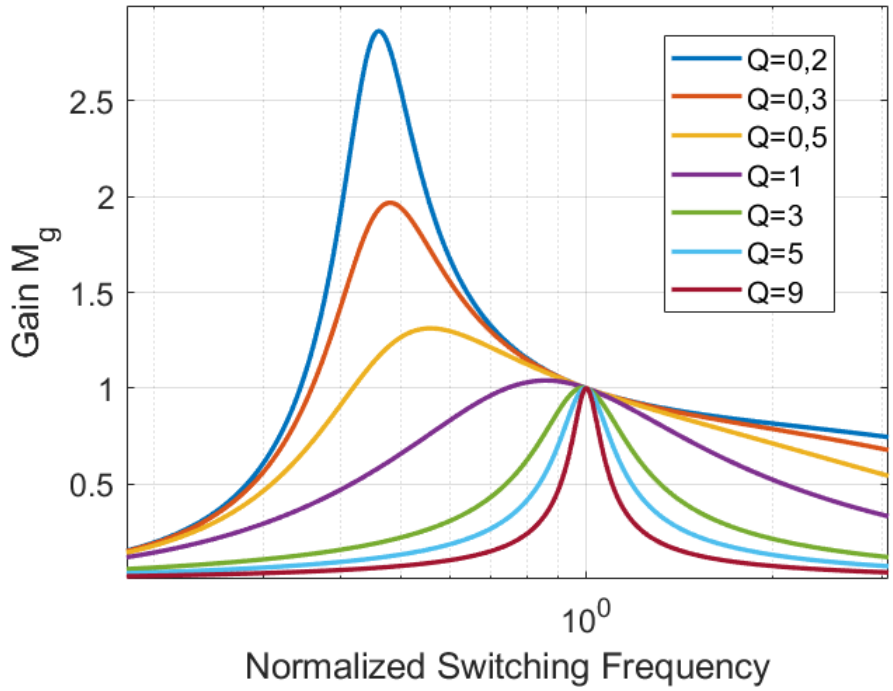


Figure 2.11: Voltage gain for $m = 4$ with curves plotted for different quality factors.

To achieve ZVS the current is allowed to flow through the MOSFET body diode, thus discharging the drain to source capacitance and causing the voltage across the MOSFET to go to zero. When this condition is met the gate signal can be applied to turn on the MOSFET with, in theory, no switching loss. Any operating point in Fig. 2.11 is not possible, because to achieve ZVS the converter must operate with inductive impedance. The gain plot can be divided into three areas to show the operating regions which can be seen in Fig. 2.12. Region one provides lower gain while region two provides higher gain and they are both causing inductive operation. Region three however is the capacitive region and it is avoided as ZVS no longer is possible.

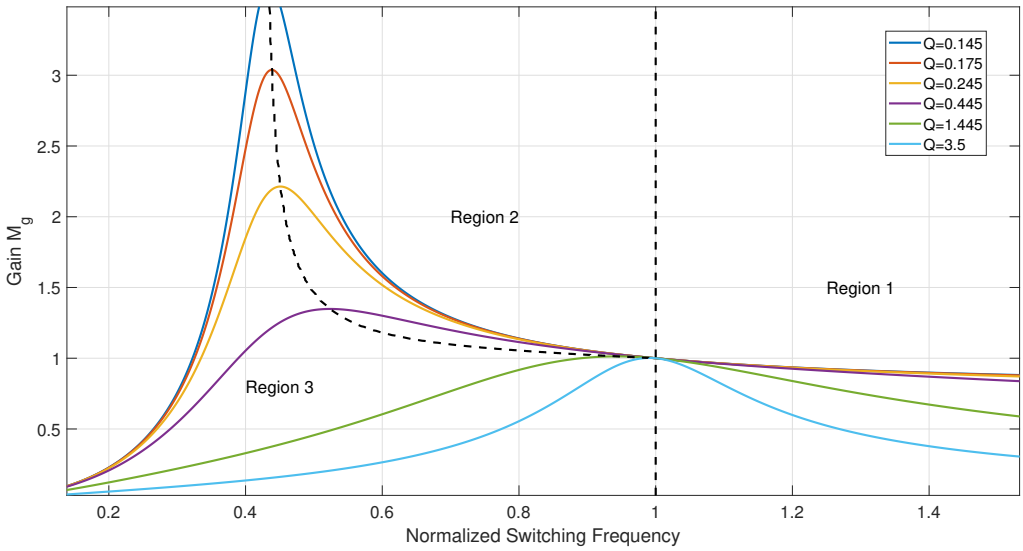


Figure 2.12: Attainable gain for different quality factors with $m = 4.5$. **Region 1:** Inductive operation & less than unity gain. **Region 2:** Inductive operation & higher than unity gain. **Region 3:** Capacitive operation & loss of ZVS.

Because the maximum attainable gain reduces with higher loading, the converter must be designed to be able to reach the gain required at the highest load condition. To help choose a Q and m for a required gain, a plot of the maximum attainable gain for different Q and m values is plotted in Fig. 2.13

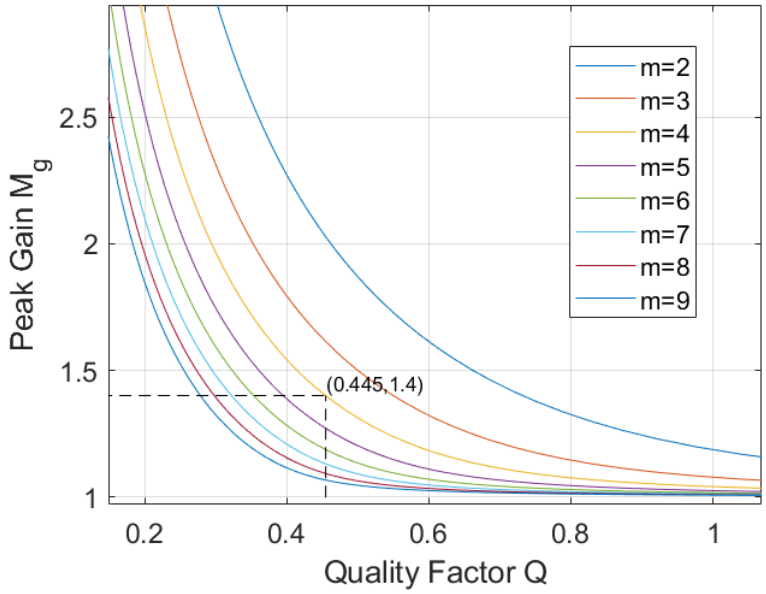


Figure 2.13: Maximum attainable gain for different Q and m values.

2.5 Diode

A diode is a passive component that allows current to flow from anode to cathode if enough bias is applied to the terminals. The voltage applied over anode and cathode must exceed the potential barrier and is typical in the range of $0.4 - 0.7V$ for a common p-n diode. For applications which require a low voltage barrier potential, what is known as a Schottky diode can be used as the voltage drop is typically $0.3V$ [7]. Hence, together with its low conduction loss and high switching capabilities, the Schottky diode has been the preferable diode choice for low power applications [7]. The forward voltage drop and low on resistance affects the conduction loss, which is given by

$$P_{cond} = V_f I_{F(Avg)} + R_d I^2_{F(rms)} \tag{2.27}$$

where V_f and R_d are the forward voltage drop and on-resistance respectively. The rms current $I_{F(rms)}$ and average current $I_{F(Avg)}$ are currents flowing from anode to cathode [15].

When negative biased is applied to the diode, a small current will flow through the device. This current occurs due to minority carriers and is often negligible [7]. If the negative bias across the diode reaches the breakdown voltage rating of the diode, minority carries will contribute to the forming of an electron avalanche. This results in a large conducting current and together with the high voltage may cause destruction of the device [7].

2.6 MOSFET

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a voltage controlled transistor used for high frequency switching and low power applications. The MOSFET structure can be seen in Fig. 2.14 with the connecting terminals of drain, source and gate.

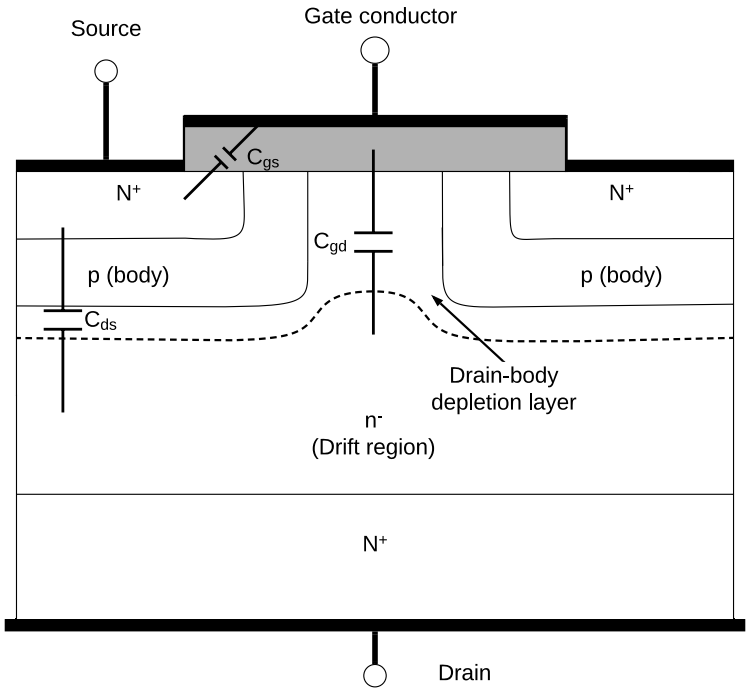


Figure 2.14: N-channel MOSFET with its parasitic capacitances

By applying a positive voltage at the gate, positive charges are accumulated close to the gate and the insulating layer. These charges attracts electrons in body region of the MOSFET due to the field effect, thus creating a conducting channel called an N-channel. This allows electrons to flow from source to drain and therefore current from drain to source. The current through the MOSFET causes conduction losses and is considered to be one of the major power dissipation that occurs in a MOSFET [7]. The conduction losses can be described by

$$P_{on} = I_{0,rms}^2 \cdot r_{DS(on)} \tag{2.28}$$

where I_0 is the output current flowing through the MOSFET, and $r_{DS(on)}$ is the sum of several resistances within the MOSFET [7].

In addition to conduction losses, there is also losses that occurs during turn off and turn on. They are called switching losses and are more prominent at high switching frequencies. The turn on characteristics for a MOSFET can be seen in Fig. 2.15 and is divided into three different time periods. The first period describes the voltage rise of V_{GS} provided by an external drive circuit. When the voltage reaches the threshold value $V_{GS(th)}$, a conducting channel is created and current starts to flow

through drain and source. As V_{GS} continues to increase the current i_D starts to rise and settles at I_0 with a total rise time of t_{ri} [7].

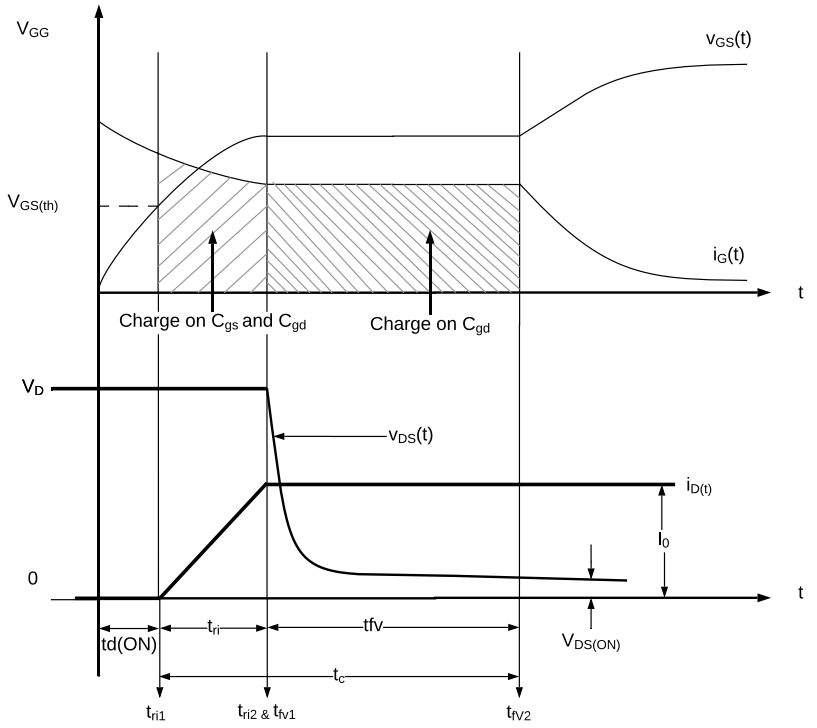


Figure 2.15: Voltage and current behaviour during turn on of a MOSFET. The upper waveforms shows the gate to source voltage and gate current. The lower shows current and voltage relationship between drain and source.

When $i_D = I_0$, voltage over drain and source will start to decrease over a time period t_{fv} and finally stabilize at a voltage of

$$V_{DS(on))} = I_0 \cdot r_{DS_{(on)}} \tag{2.29}$$

The time period consisting of t_{ri} and t_{fv} is combined to one time period called crossover time t_C described in Fig. 2.15. The overlap between the voltage and the current during t_C determines the turn on switching loss which can be described by

$$P_{sw(on)} = f_{sw} \int_{t_{ri1}}^{t_{fv2}} v_{DS(t)} i_{d(t)} dt \tag{2.30}$$

The same formula can be applied during turn off, but the time constraints will be the rise of voltage $t_r v1$ and fall of current $t_f i2$.This can be shown by

$$P_{sw(off)} = f_{sw} \int_{t_{rv1}}^{t_{fi2}} v_{DS(t)} i_{d(t)} dt \tag{2.31}$$

By adding (2.30) and (2.31), the total switching losses can be described as

$$P_{sw} = P_{sw(on)} + P_{sw(off)} = f_{sw} \int_{t_{ri}}^{t_{fv}} v_{DS(t)} i_{d(t)} dt + f_{sw} \int_{t_{rv}}^{t_{fi}} v_{DS(t)} i_{d(t)} dt \tag{2.32}$$

As the significance of switching losses is determined by the amount of voltage and currents overlap. By shifting either the voltage or current to minimize the overlapping area opens the possibility to reduce switching losses. Such methods can allow the MOSFET to operate with either ZVS or zero current switching (ZCS) [7].

At every switching period there will also be losses associated with the gate current. This is due to the charging and discharging of the gate capacitor at every switching cycle, as accumulation of charges determines the conducting behaviour of the MOSFET [10]. The accumulated gate charge Q_g together with the drive voltage V_{dr} causes losses that can be described by

$$P_{dr} = V_{dr} Q_g f_s \tag{2.33}$$

2.7 High Electron Mobility Transistor (HEMT)

The HEMT is a power switch that provides low $r_{ds(on)}$, small gate- and output capacitance and complete absence of reverse recover current. This opens the possibility to operate at higher switching frequencies together with low conduction losses. The structure of a generic HEMT can be seen in Fig. 2.16. It uses substrate made of silicon or silicon carbide, depending on cost and thermal conductivity requirements. A thin layer of insulation material is used to separate the transistor from the substrate. The Galium Nitride (GaN) has high breakdown voltage capabilities and with the combination of the AlGaN can form a highly conducting channel. The source, gate and drain are separated with a dielectric [16, 17].

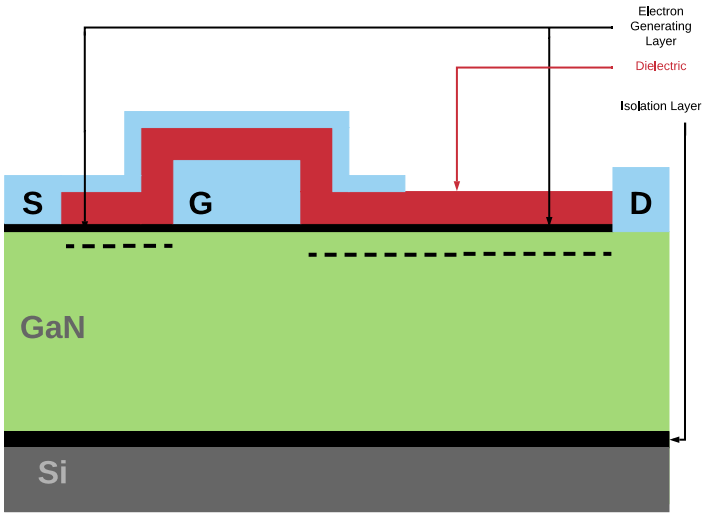


Figure 2.16: Cross section of a generic GaN transistor

The GaN HEMT utilizes a new mode of operation compared to other transistors. Instead of being based on a semiconductor homojunction it uses a heterojunction to obtain high electron mobility as well as high electron concentration. The bending of the electric bands caused at the interface of the GaN and AiGaN causes a region where the conduction band will fall below the fermi-level. In this intersection a

"pool" of a highly conductive two-dimensional electron gas (2DEG) will be created. The resistance in this intersection is very low since the electrons are "pooled" and not dependent on movement between lattices, thus providing low conduction losses. The advantage of the 2DEG is that both the on-state resistance and the gate charge can be kept low relative to traditional MOSFET topologies even when designed with high voltage tolerance [16–18].

2.8 Transformer

Transformers are used in isolated DC/DC converters to provide electrical isolation as well as to step up or step down voltage. The transformer consists of at least two sets of windings wound around a core, used to transmit the magnetic field from the primary to secondary set of windings. The voltage induced across the N number of windings due to the changing magnetic flux ϕ passing through the transformer core is

$$V(t) = N\frac{d\phi}{dt} \tag{2.34}$$

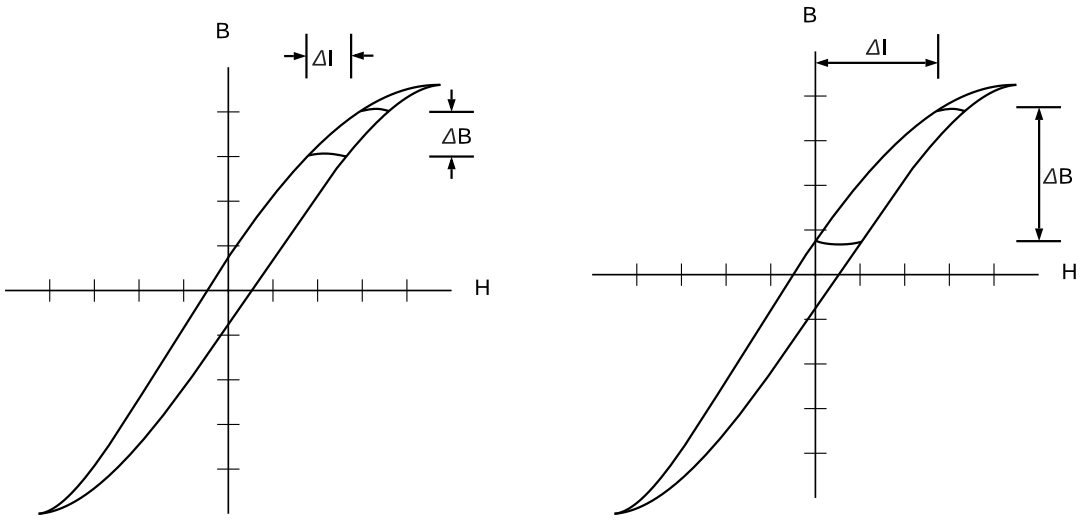
The magnetic flux depends on the effective magnetic cross section of the transformer core A_e and the magnetic flux density B as follows

$$\phi = B \cdot A_e \tag{2.35}$$

To calculate the magnetic flux density, (2.34) and (2.35) are used together and integrated over the converter conduction interval $T_s \cdot D$ [7]. This can be written as

$$B = \frac{1}{N \cdot A_e}\int_0^{DT_s} V dt = \frac{V \cdot DT_s}{N \cdot A_e} \tag{2.36}$$

There are mainly two kinds of losses in a transformer, the core losses and winding losses. The core losses are composed of eddy current losses and hysteresis losses, but their significance will differ depending on the core material. For smaller power ranges and high frequency applications ferrite is the most commonly used material for a number of reasons [7]. Advantages with ferrite is high electrical resistance and low magnetic coercivity. However, the magnetic saturation level is low, typically around $0.3T$ [7]. Due to its high electrical resistance and low coercivity, the significance of eddy current loss and hysteresis loss is low. Thus enabling the transformer to operate at high frequencies. The hysteresis losses depends on the B-H curve of the particular ferrite material which can be seen in Fig. 2.17. The B-H curve can be obtained by applying a magnetic field until the material saturates and then reversing the magnetic field. The area within this curve are related to the losses, due to the polarization of the core material. These losses increases at higher frequencies due to more frequent reversal of the magnetic field.



(a) Hysteresis losses in CCM **(b)** Hysteresis losses in DCM

Figure 2.17: B-H curve and hysteresis loss when operating in the two separate conduction modes

The loss can be represented as power loss per unit volume by Steinmetz's equation

$$P_{hys} = k f_s^a B^b \tag{2.37}$$

where B is the magnetic flux density peak and k, a and b are material constants empirically found by curve fitting [19]. Such loss curves are provided by manufacturers of magnetic material, often showing curves for different frequencies and at different temperatures. The loss curve for the material $N87$ is shown in Fig. 2.18 [20]. A line equation can then be fitted to Fig. 2.18 and the loss per volume for different magnetic flux densities can be calculated from it.

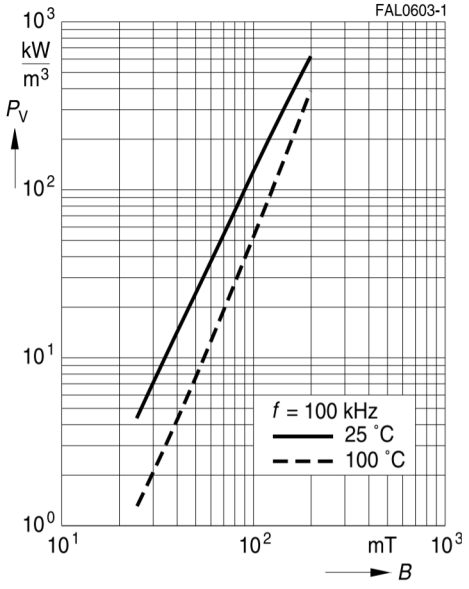


Figure 2.18: Power loss in kW/m^3 as a function of B, at 25°C and 100°C.

The winding losses occur due to the DC resistance in the transformer and is thus dependent on the cross section of the wires. The total winding losses includes the current flowing in the primary and secondary windings which can be described by

$$P_c = I_{P(rms)}^2 R_P + I_{S(rms)}^2 R_S \tag{2.38}$$

Where R_P and R_S is the DC resistance of the primary and secondary winding which are

$$R_P = \frac{N_P \rho l_N}{A_{C,prim}} \tag{2.39}$$

and

$$R_S = \frac{N_S \rho l_N}{A_{C,sec}} \tag{2.40}$$

where $A_{C,prim}/A_{C,sec}$ is the primary and secondary side winding cross section area, l_N is the average length of one wire turn and ρ is the electrical resistivity of copper. When choosing the winding cross section a rule of thumb is to limit the current per square millimeter to below $5A/mm^2$ [8].

The design of the DC-DC converter transformer can be one of the most challenging parts of the design process, due to the sheer number of parameters that can be optimized in various ways. After the system specifications are established, a core and core material should be chosen. Choosing a core is a non-trivial process that often involves going back and fourth between different models [19]. The core geometry and core material selection process in the scope of this thesis is based on the manufacturers recommendation for approximate power level for different cores. After a core suitable for the power level is chosen, the minimum number of primary windings is calculated from (2.36)

$$N_{p,min} = \frac{L_m I_{peak}}{B_{sat} A_e} \tag{2.41}$$

where I_{peak} is the peak-current through the mosfet, B_{sat} is the magnetic flux at saturation and A_e is the effective magnetic cross section. If the transformer is used for energy storage as it is in a flyback converter, an air-gap is required to not saturate the core. The air-gap reduces the equivalent permeability of the core and thus increases the magnetic field that can be applied before saturation, the B-H curve for this case can be seen in Fig. 2.17. The air-gap is calculated from

$$G = 4\pi A_e \left(\frac{N_p^2}{1000 L_m} - \frac{1}{A_L} \right) \cdot 10^{-7} \tag{2.42}$$

where A_L is the inductance factor of the core [8]. To verify that the windings fit inside the transformer, the total winding cross section A_{wr} needs to be less than the available winding area in the transformer A_w. The winding cross section area is calculated as

$$A_{wr} = \frac{A_c}{k_F} \tag{2.43}$$

where A_c is the area of the primary and secondary side copper windings and k_F is the fill factor to account for the gaps in between the windings. A typical fill factor is $0.2 < k_F < 0.25$ [8]. If the condition $A_{wr} < A_w$ is met the design can be considered to be satisfactory.

An important factor in the transformer which affects the rest of the circuit is its leakage inductance. This inductance arises from non-perfect linking of the flux from the first to the second set of windings. The leakage inductance can be minimized by winding techniques and different core shapes. However, a general formula for a rectangular core is

$$L_{leak} = \frac{\mu_0 N_p^2 l_N b_w}{3h_w} \tag{2.44}$$

where μ_0 is the permeability in vacuum, b_w is the width of wire coil and h_w is the height of the wire coil [7].

2.9 Synchronous Rectifier

For converters made for low voltage applications the forward voltage drop of the diode can have a significant impact on the overall efficiency. In order to reduce the voltage drop and increase the efficiency it is possible to replace the passive diode with a transistor, creating a synchronous rectifier (SR). This makes it possible to exploit the transistor's low on-resistance $R_{ds(on)}$ and avoid the diode forward voltage drop [21]. The SR MOSFET with its internal body diode can be seen in red, mounted on the negative output leg in Fig. 2.19.

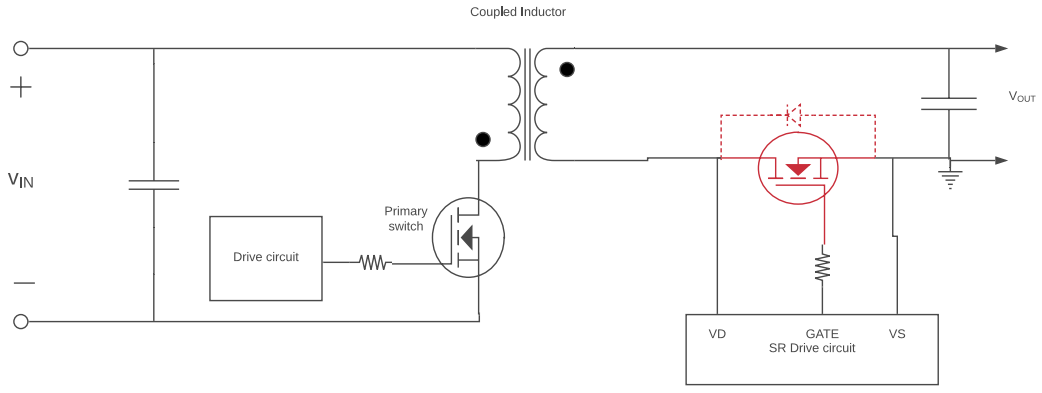


Figure 2.19: Flyback with SR implemented on the secondary side.

Because a transistor is an active component as oppose to the diode, it will be necessary to also implement a controller. Possible control strategies available differ in complexity and implementation and they all have advantages and disadvantages.

Self-driven SR control: The implementation of this SR control can bee seen in Fig. 2.20 and uses the winding polarity in the transformer itself to control the transistor. It is done by connecting the transistor gate to either the positive or negative output leg so that the transistor will turn on as the output windings changes polarity. Thus, any extra control integrated circuit won't be needed for this case of SR [21].

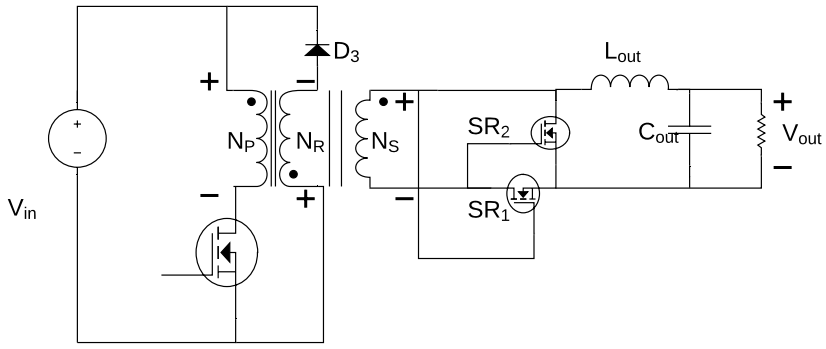


Figure 2.20: Forward converter with self driven SR control method.

V_{ds} **Sensing:** This SR control method works by choosing two voltage reference levels, V_{THON} and V_{THOFF} in Fig. 2.21, and then comparing them with the transistor drain voltage to decide whether to turn the transistor on or off. The turn on voltage reference is placed so that during the transformer discharge cycle, when the transistor body diode starts to conduct, the resulting diode voltage drop triggers the turn on of the transistor [21].

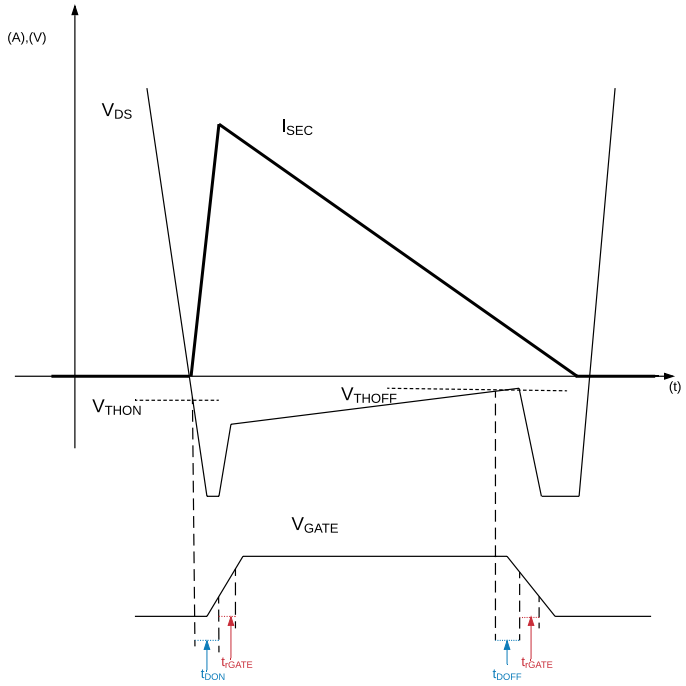


Figure 2.21: Behaviour of the Drain-to-source voltage sensing controller

As seen in Fig. 2.21 there is a turn on delay t_{on} after the turn on threshold V_{on} due to gate driver and comparator delays. As the transistor is conducting, the voltage drop across its on-state resistor directly represents the secondary side current. Thus, the turn off voltage can be set to $V_{THOFF} = V_{ds} = 0$ which is the moment when the current turns zero. Due to tolerance requirements and operating delay the turn off voltage is placed a bit before zero. After the transistor has turned off the last part of the current is transmitted through the body diode. Then the transistor blocks until the next transformer discharge cycle [21].

A challenge with this design is for the sensing circuit to simultaneously be able to handle high voltages and measure very low voltages. The threshold voltages V_{on} and V_{off} should be kept as low as possible, often just a few mV. The SD also needs to operate close to the body diode which puts tough requirements on the timings and accuracy of the voltage-sense circuit [21].

2.10 Snubbers

A snubber is a circuit added to a component within the DC-DC converter to relieve stresses and thus reduce its required voltage rating. The choice to add a snubber is therefore a trade-off between the cost of a higher rated component and the increase in complexity [7].

The working principle and composition of a snubber circuit differs for each area of use. Such uses are to:

- Limit the voltage magnitude as well as rate of change $\frac{dV}{dt}$ across a device during turn off.
- Limit the current magnitude as well as rate of change $\frac{dI}{dt}$ through a device during turn on.
- Modify the switching trajectory of a switching device.

In DC-DC converters of flyback topology, snubbers are most commonly used on the power transistor, output rectification diode and on the transformer primary windings [7].

To mitigate overvoltages caused by resonance between the leakage inductance of the transformer and the drain-source capacitance of the switching transistor a RCD snubber can be added. Like the name implies an RCD snubber consists of a resistor, a capacitor and a diode, connected in parallel with the transformer primary windings. To decide the size of the resistor and capacitor, the largest allowable resonance voltage overshoot V_{os} should be defined. The greater the allowed overshoot, the less energy is needed to be dissipated by the snubber [7]. The voltage overshoot depends on the breakdown voltage of the power transistor V_{ds}, for which it is customary to include a 10% safety margin $V_{ds} = V_{ds} \cdot 0.9$ [22]. The overshoot is written as

$$V_{os} = V_{ds} - V_{in} - V_{ro} \tag{2.45}$$

where V_{in} is the converter input voltage and V_{ro} is the output voltage reflected to the primary side. The peak current through the clamping circuit is then defined as

$$I_{sn}^{peak} = \sqrt{I_{ds}^{peak} - \frac{C_{oss}}{L_{leak}} V_{os}^2} \tag{2.46}$$

where I_{ds}^{peak} is the peak current through the transistor, C_{oss} is the output capacitance of the transistor and L_{leak} is the leakage inductance. The snubber current and switching frequency f_s is then used to calculate the power dissipation in the snubber with the formula

$$P_{snub} = \frac{1}{2} f_s L_{leak} (I_{sn}^{peak})^2 \cdot \frac{V_{ro} + V_{os}}{V_{os}} \tag{2.47}$$

The size of the resistor needed to dissipate this power is

$$R_{snub} = \frac{(V_{ro} + V_{os})^2}{P_{snub}} \tag{2.48}$$

Finally the capacitor is picked based on the allowed voltage ripple across the capacitor ΔV_{snub}. The snubber capacitor is thus

$$C_{snubb} > \frac{V_{ro} + V_{os}}{\Delta V_{snub} R_{snub} f_s} \tag{2.49}$$

2.11 Active Clamp

An active clamp can be used to reduce overvoltages due to leakage inductance instead of an RCD snubber and can be seen in Fig 2.22. The active clamp contains a capacitor and a transistor which are used to store and recycle energy to the load from the transformer leakage inductance. This configuration also provides ZVS similar to the turn-off snubber, thus increases the general efficiency and allows for higher switching-frequencies. The possibility to operate at higher switching frequencies occurs as energy no longer i dissipated over the resistor but recycled back to the load and allows ZVS operation. In addition to this, higher switching frequency could also reduce the size of the transformer and thus make it possible to obtain a higher power density. This is a technology in development as DC-DC converters with multiple transistors will have non-linear capacitive effects on the circuit which are not yet well understood [23].

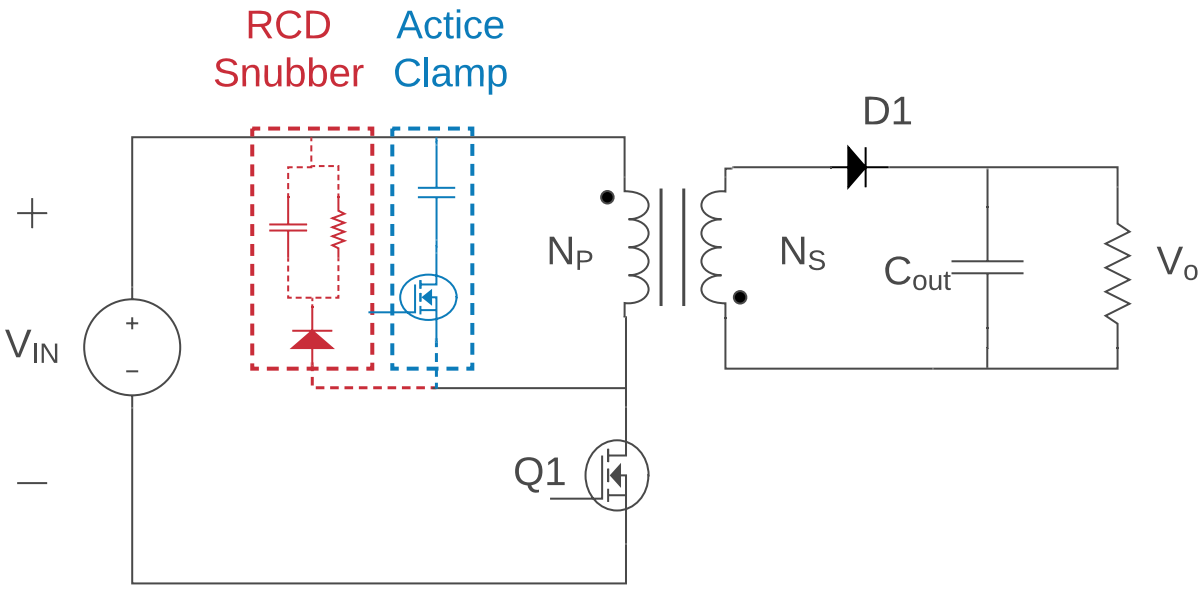


Figure 2.22: Flyback converter with Active clamp and RCD snubber

2.11.1 EMI

Electromagnetic interference (EMI) is a disturbance or noise caused by some external source and affecting an electric component [7]. EMI should be kept within certain boundaries following the standards set for different regions of the world as well as the component applications. The term EMI encompasses disturbances with different frequency dependent modes of transfer. These are, conducted noise, coupled noise and radiated noise. Conducted noise is low frequent and travels through the conductor, while the coupled noise occurs at higher frequencies due to capacitive and magnetic coupling. At very high frequencies, wires and leads may act like antennas and radiate noise as electromagnetic waves.

DC-DC converters can cause a lot of EMI due to the high power, high $\frac{di}{dt}$, parasitic elements and fast switching involved in their operation [7]. This noise may then interfere with the system itself or other systems. To deal with this, EMI filters, snubbers and component shielding can be used to reduce the cause of noise and keep the noise from disturbing sensitive equipment. Dithering is another method for reducing the intensity of the switching noise. This is done by varying the switching frequency back and forth so that the emission will be spread to a wider frequency band. The PCB layout can also be designed to avoid EMI by minimizing high $\frac{di}{dt}$ loop area (bypass capacitors) as well as placing sensitive components far away from potential noise sources. Another design choice that affects the noise performance of the converter is the placement of the synchronous rectifier. By placing it on the positive output leg the noise from the switch through the transformer parasitic capacitor is reduced.

2.12 Electrical Measurement

Efficiency measurements are going to be performed on a number of converters, which will be used as a comparison with the simulated circuits. To measure the efficiency, a setup consisting of variable resistors, a DC-supply and various electric measuring equipment is used. The input and output power from the converters are calculated by measuring the current and voltage and using

$$P = v_{DC} \cdot i_{DC} \tag{2.50}$$

Then, by computing the input and output power, the efficiency is

$$\eta_{conv} = \frac{P_{out}}{P_{in}} \tag{2.51}$$

2.12.1 Measurement Uncertainty

When performing real life measurements, instrument errors or uncertainty must always be considered. The uncertainty is a combination of accuracy and precision, specific to the instrument in question. When using the measured quantities in calculation, the uncertainties must be propagated correctly. If some generic measured quantities are a, b and c and their uncertainties are δa, δb and δc. Then for addition and subtraction between these quantities, the uncertainty is [24]

$$Q = a + b - c \tag{2.52}$$

and

$$\delta Q = \sqrt{\delta a^2 + \delta b^2 + \delta c^2} \tag{2.53}$$

The reason the total uncertainty δQ is not just the addition of each contribution is because the uncertainty of an instrument follows a normal distribution and is thus probabilistic in nature [24]. The uncertainty is ± 1 standard deviation from the mean of the distribution and thus there is a 68% chance the measured value falls within $a \pm \delta a$. This because there are no certain bounds for the errors that (2.53) is used. For multiplication and division the equation is simplified by writing the uncertainties as percentages $\delta a\% = \frac{\delta a}{a}$, then

$$Q = \frac{a \cdot b}{c} \tag{2.54}$$

and

$$\delta Q\% = \sqrt{\delta a\%^2 + \delta b\%^2 + \delta c\%^2} \tag{2.55}$$

2.13 Present Value Analysis

By increasing the converter efficiency, by for instance implementing synchronous rectification, the price of the product is going to get affected. This means that the end user is most likely going to have to pay more for the product, to later save money on the electrical bill. To analyze the benefits of investing in a converter with increased efficiency and reduced losses, the present value method is used [25]. The present value method is used as a way of relating the future savings on the power bill to the present day investment required to implement the SR. The present value (PV) is thus the present value of future profits and can be calculated as

$$PV = \sum_{i=1}^{n} \frac{a_i}{(1+p)^i} \tag{2.56}$$

were n is the life time of the converter counted in years, a_i is the profit due to the power saved each year and p is the discount rate.

The profit a_i depends on the amount of saved kilowatt hours kWh from using SR and the energy price per kilowatt hour the years its in use. The discount rate p is the expected return on a investment of similar risk and is used as a way of translating future earnings to present earnings [25]. If the profit a_i is equally large each year (2.56) can be rewritten as

$$PV = a\Big(\frac{1}{p} - \frac{1}{p(1+p)^n}\Big) \tag{2.57}$$

3
Method

3.1 Review of Phone and Laptop Chargers

To investigate what efficiency can be expected from low power DC-DC converters and perform measurements of efficiency curves for comparison with simulations, three flyback converters are procured. Two where phone chargers and one a laptop charger. Their respective power, voltage and current levels are presented in Table 3.1. To analyze how the rated power level of the converter affects its performance, converters with three different rated output power levels $5W$, $12W$ and $45W$ were chosen.

Table 3.1: Power and voltage rating for phone chargers from Clas Ohlson and Sandstrøm as well as a laptop charger from Blueparts

Converter Model	Rated Power	Input Voltage AC	Output Voltage, DC	Output Current
Sandstrøm Model No.:S6TRLC14	5 W	100-240 V	5 V	1 A
Clas Ohlson Model No.:38-7211	12 W	100-240 V	5 V	2.4 A
Blueparts Model No.:LAS045HCO	45 W	100-240 V	19 V	2.37 A

3.1.1 Sandstrøm Model No.:S6TRLC14

This is quite a small charger with low output power. The contacts from the wall socket connects through a fuse to a diode bridge rectifier and filter capacitor on the PCB. The converter is of flyback topology and contains a transformer, a MOSFET on the primary side, as well as a diode and filter capacitor on secondary side. There is no connection between the primary and secondary side of the converter, indicating that the control method does not require direct measurement of the output voltage. The labeling on the MOSFET and diode is hard to read and is therefore hard to obtain data specification.

3.1.2 Clas Ohlson Model No.:38-7211

For this charger, the rectification step is the same as for the Sandstrøm model. The size of the components are however considerably larger due to the higher rated power. The converter primary side does not show any visible MOSFET and it can be concluded to be integrated into the control circuit. The primary and secondary side have a capacitor connected in between to reduce the EMI generated from the transformer parasitic capacitance between the primary and secondary windings [26]. The capacitor is of Y-class to ensure there is no risk for ground currents at fault.

The secondary side rectifying diode is of Schottky type, which has a lower forward voltage drop than a standard PN diode.

3.1.3 Blueparts Model No.:LAS045HCO

The laptop charger is of flyback topology and shares some similarities to the phone chargers. However, the size of the components are increased due to its higher rated power level. The two components that occupies the most space on the PCB board are the transformer and input capacitor. To reduce losses, two Shottky diodes are connected in parallel for the output rectifier as a way of reducing the r_{on}, while obtaining the same forward voltage drop. The two output capacitors are also connected in parallel to obtain the required capacitance and reduce the ESR.

3.2 Phone and Laptop Charger Efficiency

3.2.1 Electrical Measurement Equipment

The electrical equipment used to measure the efficiency of the procured converters is presented in Table 3.2. The current shunt was used together with the Siemens function meter.

Table 3.2: List of the electrical equipment, Measurement Accuracy: ± (reading + added to final value)

Component NR	Component	Producer	Model	Function	Accuracy
1	Power Supply	Power Supply	SM300-20	DC V Supply	0.5% + 2 digit
2	True-rms Digital Multimeter	Fluke	175	DC Volts	0.15% + 2 digit
3	Function Meter	Siemens	B1080	(DC + AC) Volts	0.5% +0.1%
4	Multimeter	HP	3468A	Input Current	0.17% + 6 digit
5	Current Shunt	Siemens		Output Current	
6	Variable Resistance			Ω	

3.2.2 Electrical Measurement

The electrical measurement setup is shown in Fig. 3.1, with indicators referring to the equipment listed in Table 3.2.

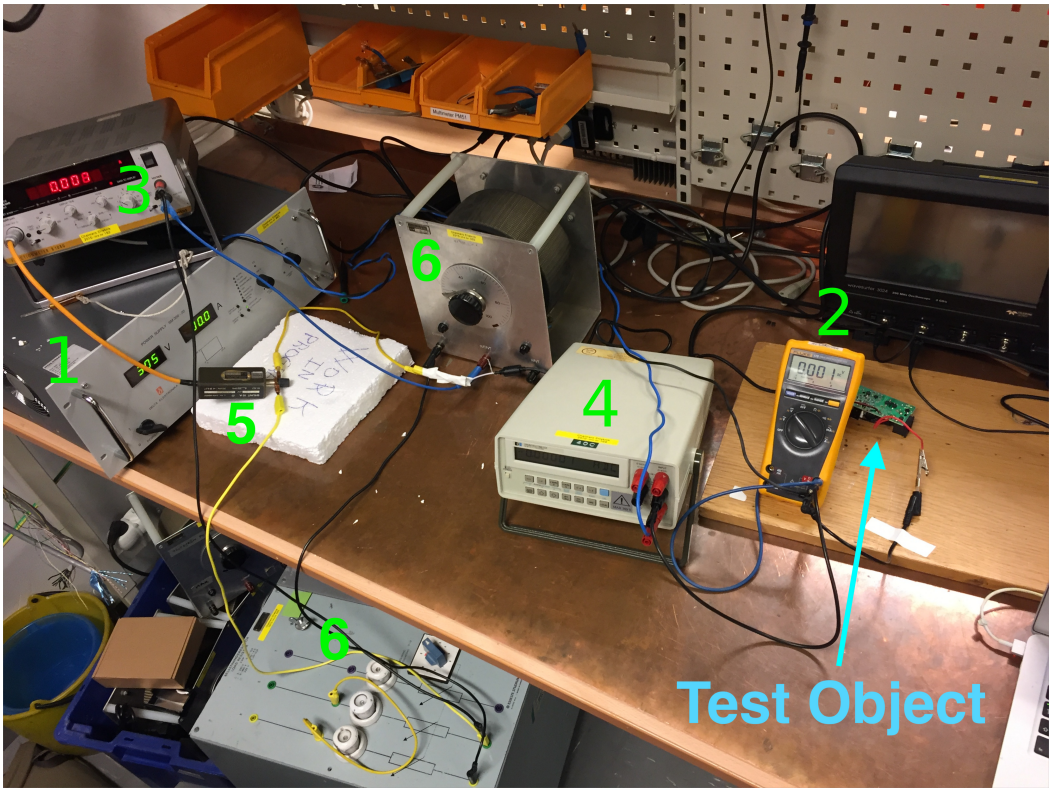


Figure 3.1: Setup of the electrical measurements, with numbers indicating the equipment in Table 3.2

To measure the losses of the DC-DC converter, the internal diode rectifier of the charger is bypassed. For a European voltage level of 230V AC a rectified DC voltage of 325V DC should be supplied. However, due to equipment limitations a SM300-20 is used which can supply a DC voltage of 305.4V. An additional Fluke 175 is connected to the input together with HP 3468A, providing high resolution measurements of voltage and current to establish the supplied power.

To obtain the output power directly, the function meter B10880 together with a 10A shunt were found suitable. In addition to power measurement, B10880 also enables the possibility to measure the output voltage and current. The setup with the function meter can be seen in Fig. 3.1 connected to the terminals of the variable resistor.

The measurement was conducted by gradually increasing the resistances from the lowest possible value that gives a stable output voltage and upward. Notations of input and output voltage and current were taken to calculate the efficiency. The resistance was increased to the point where the measurements became too uncertain to continue due to the low currents and the experiment were stopped. As the load rose above that of rated operation, current and generated heat became too high and the test was terminated to not damage the converters.

3.3 Converter Design Setup

The three converters that are to be implemented in LTspice are based on the specifications in Table 3.3. The input voltage in Table 3.3 is set to be $325V$ DC as it is the rectified AC input of $230V$ AC. The design is made to resemble a phone charger and thus the output voltage is set to $5V$ DC. The acquired phone chargers have a power level of $5W$ and $12W$, for this design a slightly higher power level of $15W$ is chosen. This was done to get a similar case to the two phone chargers. A frequency of $100kHz$ is used compared to the phone chargers which had a switching frequency of about $35kHz$. There is a strong incentive to increase the switching frequency as this means that the size of components can be reduced as well as power to reduce charge time.

Table 3.3: LTSpice design specifications

V_{in}	P_{Out}	V_{Out}	Ripple Voltage	Switching Frequency
$V_{in(Nominal)}$	Nominal	Nominal	Nominal	Nominal
325 ± 25 V DC	15 W	5 V	50mV	100 kHz

3.4 Flyback Converter

The first decision when designing a flyback converter is to choose whether to operate in CCM or DCM. Because DCM has higher rms current and thus higher losses, the operating mode for the converter in Table 3.3 is chosen to operate in CCM. The rest of the design process can be summarized with the flow chart seen in Fig. 3.2.

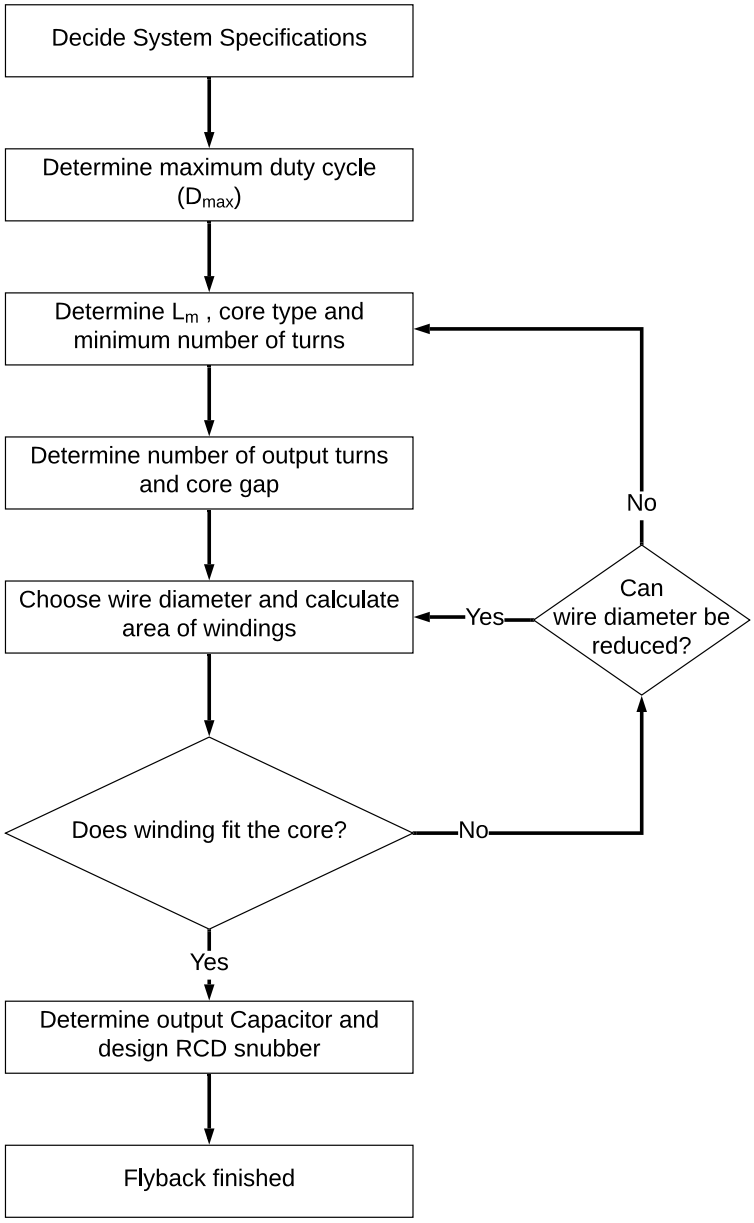


Figure 3.2: Flyback converter design flow chart.

When determining the maximum duty ratio D_{max} it is favorable to keep D high to lower the voltage stress on the secondary side diode. In CCM operation however,

the effects of sub harmonic oscillations keep the maximum duty ratio limited to $D < 0.5$ for most controllers. To avoid going above $D = 0.5$, the maximum duty cycle is set to $D_{max} = 0.45$.

In order to determine the transformer magnetizing inductance L_m, the ripple factor K_{RF} must be established. Choosing a ripple factor comes down to balancing the benefit of low conduction losses for low K_{RF} and reducing transformer size by using a high K_{RF}. For European input voltages a range of $K_{RF} = 0.4 - 0.8$ is recommended [8]. In this design the ripple factor is set to $K_{RF} = 0.5$. When K_{RF} has been decided, the magnetizing inductance L_m is calculated according to (2.5) as

$$L_m = \frac{(V_{in,min} \cdot D_{max})^2}{2P_{in} f_s K_{RF}} = 12.118mH \tag{3.1}$$

and the ripple current ΔI and the average current through the magnetizing inductance I_m are calculated according to (2.3) and (2.4) as

$$\Delta I = \frac{V_{in} D}{L_m f_s} = 0.1207A \tag{3.2}$$

$$I_m = \frac{P_{in}}{V_{in} D} = 0.1207A \tag{3.3}$$

For the calculated magnetizing inductance, the peak current and rms current are

$$I_{m,peak} = I_m + \frac{\Delta I}{2} = 0.1811A \tag{3.4}$$

$$I_{m,rms} = \sqrt{\frac{D}{3}\left[3(I_m)^2 + \left(\frac{\Delta I}{2}\right)^2\right]} = 84.27mA \tag{3.5}$$

The next step is to select the core shape and core material. The E core $EFD25$ is selected as it fits the transfer power demand in Table 3.3 [27]. Due to the switching frequency, the material for the $EFD25$ is taken as $N87$ provided by the data sheet [28]. The worst-case operating condition is considered when the temperature of the core is $100°C$, for which $N87$ has a saturation flux density of $390mT$. To ensure operation below magnetic saturation for $N87$, the minimum number of primary winding turns is calculated according to (2.41) as

$$N_{p,min} = \frac{L_m I_{m,peak}}{B_{sat} A_e} = 97.02 \tag{3.6}$$

The turns ratio can then be obtained from the CCM transfer function (2.9), which has been slightly modified to include an estimate the diode voltage drop which is set to $V_{diode} = 0.3V$. Thus, the turns ratio is

$$n = \frac{V_{in}}{V_o + V_{diode}} \frac{D_{max}}{1 - D_{max}} = 50.17 \tag{3.7}$$

The turns ratio gives $N_s = 1.934$ which is then rounded up to a complete integer and is thus $N_s = 2$. Recalculating the number of primary turns N_p, turns ratio and duty cycle for this N_s results in $n = 50$, $N_p = 100$ and $D = 0.435$. In order

to maintain the magnetizing inductance value with the new windings, a gap in the core is required. The required gap length from (2.42) is then

$$G = 4\pi A_e\left(\frac{N_p^2}{L_m} - \frac{1}{A_L}\right) \cdot 10^{-7} = 0.0365mm \tag{3.8}$$

At this point the wire diameters for the primary and secondary windings should be decided and compared with the available core space to see if they fit. If they don't, the number of winding turns must be changed as shown in the flowchart of Fig. 3.2. The wire diameter for the primary and secondary side is chosen as $d_{N1} = 0.25mm$ and $d_{N2} = 1.5mm$ respectively. This results in current densities of $Id_{N1} = 1.7167A/mm^2$ and $Id_{N2} = 2.4868A/mm^2$ which both are below $5A/mm^2$ and therefore fulfills the requirements. The resulting winding area A_{wr} should be smaller than the winding slot area $A_w = 40.7mm^2$. The copper area is $A_c = 8.4430mm^2$, using (2.43) with a fill factor of $k_F = 0.21$ the winding area is

$$A_{wr} = \frac{A_c}{k_F} = 40.20mm^2 \tag{3.9}$$

which is sufficient. The winding resistances are then calculated by (2.39) and (2.40) to

$$R_P = \frac{N_P \rho l_N}{A_{C,prim}} = 1.711\Omega \tag{3.10}$$

and

$$R_S = \frac{N_S \rho l_N}{A_{C,sec}} = 0.951m\Omega \tag{3.11}$$

The leakage inductance due to the number of windings and the geometry of the core is then calculated with (2.44) as

$$L_{leak} = \frac{\mu_0 N_p^2 l_N b_w}{3h_w} = 75.99\mu H \tag{3.12}$$

where the width of the coil slot is $b_W = 5.95mm$ and the height of the coil slot is $h_W = 16.4mm$. The output capacitor is then selected to maintain a output voltage ripple below $V_{Out} = 50mV$, from (2.8) the required capacitance is

$$C_{out} = \frac{\Delta I_o}{8 f_s \Delta V_{Out}} = 150\mu F \tag{3.13}$$

Lastly the RCD snubber is calculated for the primary switch IPN80R2K0P7 which has a breakdown voltage of $800V$. Thus, from (2.45) the allowed overshoot is

$$V_{os} = V_{ds} - V_{in} - V_{ro} = 145V \tag{3.14}$$

and the snubber current from (2.46) is

$$I_{sn}^{peak} = \sqrt{I_{ds}^{peak} - \frac{C_{oss}}{L_{leak}} V_{os}^2} = 0.178A \tag{3.15}$$

The power dissipated by the snubber to reduce the voltage overshoot is then calculated from (2.47) to

$$P_{snub} = \frac{1}{2} f_s L_{leak} (I_{sn}^{peak})^2 \cdot \frac{V_{ro} + V_{os}}{V_{os}} = 0.328W \tag{3.16}$$

then the value of the snubber resistor and capacitor from (2.48) and (2.49) is

$$R_{snub} = \frac{(V_{ro} + V_{os})^2}{P_{snub}} = 475.8k\Omega \tag{3.17}$$

$$C_{snubb} > \frac{V_{ro} + V_{os}}{\Delta V_{snub} R_{snub} f_s} = 207.6pF \tag{3.18}$$

All calculated parameters from the flyback design are summarized in Table 3.4.

Table 3.4: Calculated parameters flyback

Components	Calculated
D_{max}	0.45
K_{RF}	0.5
L_m	12.118mH
$I_{m,peak}$	0.1811A
$I_{m,rms}$	84.27mA
N_p	100 turns
N_s	2 turns
G	0.0365mm
A_{wr}	$40.20mm^2$
L_{leak}	75.99μH
C_{Out}	300μF
R_{snub}	475.8kΩ
C_{snubb}	207.6pF

3.4.1 Flyback Component Selection

When choosing components for the flyback converter, the parameters from Table 3.4 are used as a basis. The used components are presented with their required rating in Table 3.5.

Table 3.5: Selected components for flyback converter where Vbd is the breakdown voltage of the device

Component	Model	Vbd [V]	$R_{on}[\Omega]$	Gate Charge [C]
Output Capacitor	T520D337M006ATE018		18m	
Diode	B520C, Schottky	20	1.1	
SR switch	FDC8884	30	19m	5.3n
Primary Switch	IPN80R2K0P7	800	2	9n
Transformer	EF(D) 25, N87			

3.5 Forward Converter

The design procedure of the forward converter will be executed in the following order; transformer selection, output inductor and capacitor, MOSFET and diode consideration, implementation of SR and component selection.

3.5.1 Transformer Selection

One of the first values that must be established is the transformer ratio between primary and reset windings, and between primary and secondary windings. The ratio between N_r and N_p is set to 1 for simplicity, giving a duty cycle of 0.5 to ensure proper demagnetization [10]. The primary and secondary ratio is computed by using (2.11), thus winding ratio is calculated as

$$\frac{N_p}{N_s} = n = \frac{V_{in}D}{V_O} = 27 \tag{3.19}$$

V_O is set to $6V$ to account for voltage drop over the diode and output inductor [10]. The selected transformer core is selected based on core recommendation for power levels given in Table 3.3, which gives the transformer core EF(D)25 with ferrite material N87 [27]. Thus, the minimum number of turns to prevent saturation obtain from (2.41) can therefore be calculated to be

$$N1 > \frac{V_{in}D\frac{1}{f_s}}{B_{sat}A_e} = 71.84 \tag{3.20}$$

With V_{in} = 325 V, D=0.5, B_{sat} = 0.39T and A_e=58mm^2. To fulfill the saturation criteria and transformer ratio, primary and secondary is set to 81 and 3 respectively. As the number of winding's has been established, next process is to verify that the winding area is able to fit the core window. The primary/reset and secondary conductor diameter is estimated to be 0.25mm and 0.5mm respectively due to the large current deviation between primary and secondary side. The total conductor area can therefore be calculated as

$$A_{cu} = 2\pi(\frac{d_P}{2})^2 N_P + \pi(\frac{d_S}{2})^2 N_S = 8.737mm^2 \tag{3.21}$$

Factor of K_{cu}=0.25 is included to account for insulation tape and geometric shape of the conductor. Therefore, the total winding area can be recalculated from (2.43) to be

$$A_{Wr} = \frac{A_{Cu}}{K_{cu}} = 34.948mm^2 \tag{3.22}$$

Since $A_W = 40.7\ mm^2 > A_{Wr} = 34.948\ mm^2$ the core criteria is fulfilled, so no further iteration is needed. As the number of windings and dimension has been established, resistance of the primary, reset winding can be calculated with (2.39) and the secondary winding resistance with (2.40). The primary and reset winding have the same number of turns and their respective resistances can therefore be calculated as

$$R_P = R_R = \frac{N_P \rho l_N}{A_{C,prim}} = 1.42\Omega \tag{3.23}$$

The secondary winding resistance is calculated as

$$R_S = \frac{N_S \rho l_N}{A_{C,Sec}} = 12.834m\Omega \tag{3.24}$$

The transformer non-idealities caused by leakage inductance in the core is then calculated with (2.44) to

$$L_{leak} = \frac{\mu_0 N_p^2 l_N b_w}{3h_w} = 52.35\mu H \tag{3.25}$$

The final process of the transformer design is determination of the transformer inductance. The selected core material is N87 and primary and secondary inductance can be calculated using the inductance factor AL, giving

$$L_P = L_R = A_L N_P^2 = 13.122mH \tag{3.26}$$

$$L_S = A_L N_S^2 = 18\mu H \tag{3.27}$$

Another case was created with priority of reducing the core losses. This was done by increasing the primary and secondary windings while maintaining the ratio of 27. The selected turns for primary and reset windings is therefore 135 turns, which gives secondary winding 5 turns. The diameter of the secondary winding is kept the same while primary and reset windings are reduced to 0.2 mm assuming current density below $5A/mm^2$.

3.5.2 Output Inductor and Capacitor

Since the converter is to be simulated at partial loading, a minimum ripple must be established to ensure that the output inductor is large enough to operate in CCM [10]. A reduction of 5% of the nominal load will be chosen resulting in a current of

$$I_{O(min)} = 5\%I_O = 0.15A \tag{3.28}$$

To ensure CCM in the given operation mode, ripple current has to be less than twice of $I_{0(min)}$ as stated in 3.30. This will then give a maximum ripple limit of

$$\Delta I_O \leq 0.3A \tag{3.29}$$

As the ripple boundary has been established, the next step will be to implement the voltage across the inductor (2.14) in to (2.13) to solve for L_{out}.

$$L_O > (\frac{N_s}{N_P}V_{in} - V_O)\frac{1}{\Delta I_O}t_{on} \tag{3.30}$$

The output inductor is located on the secondary side and gain given by t_{on} from (2.11) gives

$$t_{on} = \frac{V_O}{V_{in}}\frac{N_P}{N_S}\frac{1}{f_s} \tag{3.31}$$

By substituting (3.31) into (3.30), the minimum inductor requirement can be calculated as

$$L_O > (1 - \frac{1}{V_{in}}\frac{N_P}{N_S}V_O)\frac{1}{\Delta I_O}V_O\frac{1}{f_s} \Rightarrow L_O > 97.44\mu H \tag{3.32}$$

To reduce the output voltage ripple, a satisfying output capacitor must be established [6]. The output ripple is given in Table 3.3 and the capacitor is calculated to be

$$C_{Out} = \frac{\Delta I_O}{8f_s\Delta V_{Out}} = 7.5\mu F \tag{3.33}$$

The transformer, output inductor and capacitor has been selected and the component values for both designs are presented in Table 3.6.

Table 3.6: Calculated main components for both the forward converter cases

Component	Case 1	Case 2
Duty Cycle	0.5	0.5
n	27	27
L_{out}	97.44μH	97.44μH
C_{out}	7.5μF	7.5μF
$N_p = N_r$	83	135
N_s	3	5
A_{Wr}	34.948mm^2	37.856mm^2
$R_p = R_r$	1.42Ω	3.61Ω
R_s	12.834mΩ	21.39mΩ
$L_p = L_r$	13.122mH	36.45mH
L_s	18μH	50μH
L_{leak}	52.35μH	138.48μH

3.5.3 MOSFET and Diode Consideration

The MOSFET is selected by considering the maximum voltage, gate charge and $R_{DS(on)}$. The MOSFET experiences its maximum voltage during turn off and is described by (2.14), which gives

$$V_{DS} = 325V + \frac{1}{1}325V = 650V \tag{3.34}$$

Additional design correction including derating of 20% is added to make sure the MOSFET can withstand voltages above normal operations.

The remaining component values that must be implemented with respect to the design parameters are the three diodes. The justification of the diodes on the secondary will be considered first. The two diodes, $D1$ and $D2$, will experience a reverse voltage (V_r) reflected by the primary side that can be calculated as

$$V_r > (V_{in}\frac{N_S}{N_P}) = 12.04V \tag{3.35}$$

In addition to the reverse voltage criteria, the diodes must be able to conduct rms currents experienced at maximum load. The last diode of consideration is $D3$ located on the primary side. The diode will experience a reflected voltage of $325V$DC reflected by transformer ratio 1:1 between primary and reset. The diode will operate with rms current caused by demagnetization of the transformer.

3.5.4 Implementation of Synchronized Rectifier (SR)

In order to improve the efficiency further SR is implemented, thus the output diodes are replaced with switches. The components in Table 3.6 are kept the same and voltage tolerance described in (3.35) is still valid. In addition to voltage rating, tradeoffs between conduction losses and switching losses must be considered. The

MOSFET implementation is conducted according to the self-driven SR control seen in Fig. 2.20 where $D1$ and $D2$ are replaced with SR1 and SR2 respectively.

3.5.5 Component Selection

The minimal value for the output inductor presented with partial loading tolerance described in 3.32 was determined to be 97.44 μH. Including some uncertainties, the inductance model PCV-1-104-05 with 100μH is found to be the suitable output inductance. The same procedure is considered in determination of the output capacitor and the suitable model is selected as A700V106M006ATE055 which has a capacitance of 10 μF.

The diodes located on the secondary side must withstand the voltage given in (3.35) and a rms current of approximately 3 A is selected due to design specifications in Table3.3. An added voltage and current tolerances are considered to ensure system robustness. Therefore, Schottky diode B520C is selected with the ability of low forward voltage and fast switching. The demagnetization diode $D3$ is to operate at $325V$, but derating of 20% is added to preserve secure operation. The available Schottky diode in LTSpice library that fulfills the voltage tolerance criteria is UPSC600. The demagnetizing current is assumed to be very small and UPSC600 provides safe operation up to $1A$.

The remaining components that have to be selected are the three switches starting with the primary switch, then $SR1$ and $SR2$. The primary switch will experience high voltage of $650V$ and a derating of 20% is added to the final voltage tolerance to prohibit possibilities of breakdown. The IPN80R2K0P7 is chosen as the primary switch with a current rating of $3A$.

The $SR1$ and $SR2$ are selected to operate with a minimum voltage tolerance of 14.5 V including derating of 20%. In addition, the MOSFET must be able to a conduct current of $3A$. To utilize the implementation of SR, the choice of MOSFET will be prioritized with low $r_{ds(on)}$ and $Q_(g)$. One model that fulfill these specifications is FDC8884 provided by Onsemi and is presented together with the other components in Table 3.7.

Table 3.7: Selected components for forward converter

Component	Model	Vbd [V]	$R_{on}[\Omega]$	Gate Charge [C]
Output Inductor	PCV-1-104-05		47.3m	
Output Capacitor	A700V106M006ATE055		55m	
Diode 1	B520C, Schottky	20	1.1	
Diode 2	B520C, Schottky	20	1.1	
SR switch 1	FDC8884	30	19m	5.3n
SR switch 2	FDC8884	30	19m	5.3n
Primary Switch	IPN80R2K0P7	800	2	9n
Transformer	EF(D) 25, N87			

3.6 LLC Half Bridge Converter Design

Before designing the resonant tank, the topology for the switching bridge and output rectifier should to be decided. From Table 2.2 the half bridge is the best choice due to the low rated power and high input voltage of this application. Using the half bridge reduces the number of switches and due to the low primary side current the increase in conduction losses this brings with it is low. The output rectifier is decided by looking at Table 2.3, for a low output voltage the full wave rectifier is favorable due to its lower amount of diodes and thereby lower diode power loss. The design process for the resonant tank of an LLC bridge converter is an iterative process which can be divided as shown in Fig. 3.3.

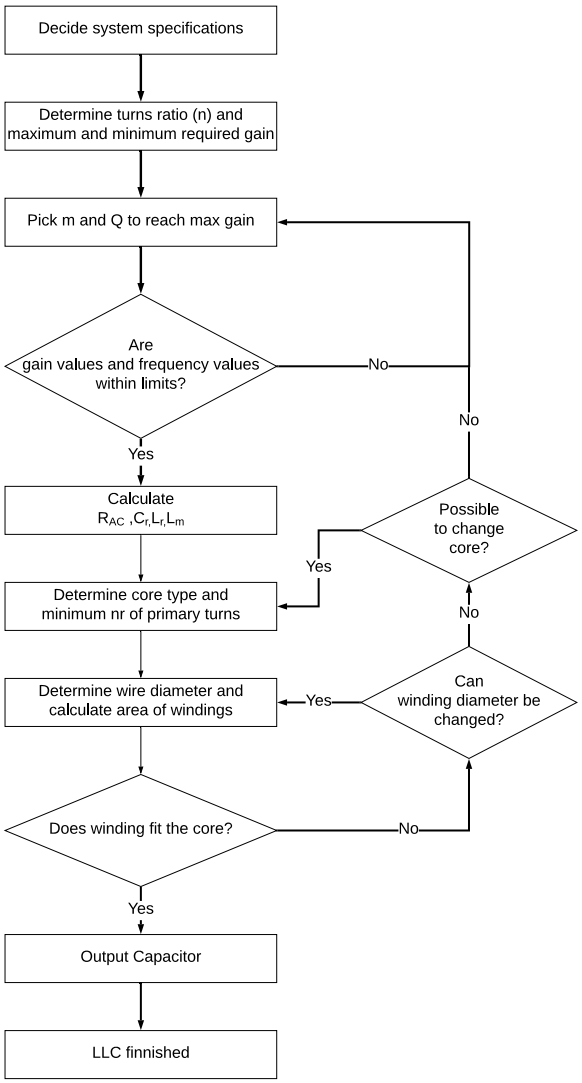


Figure 3.3: LLC half bridge design flow chart.

Because the LLC converter at normal operation has a resonant tank gain of $M_g = 1$ and the half bridge voltage is $V_{hb} = \frac{V_{in}}{2}$, the transformer turns ratio is

$$n = \frac{V_{in}}{2V_o} = 32.5 \tag{3.36}$$

The required minimum resonant tank gain is calculated according to the specifications in Table 3.3 and (2.16). The expected diode voltage drop with a value of $V_{diode} = 0.3V$ is added to the output voltage, the minimum gain is thus

$$M_{g\_min} = \frac{2n \cdot (V_{o\_min} + V_{diode})}{V_{in\_max}} = 0.975 \tag{3.37}$$

The maximal gain calculation includes the diode voltage drop $V_{diode} = 0.3V$, and also the expected loss V_{loss} due to an expected operating efficiency of 90%. From (2.15) the maximum gain is

$$V_{loss} = \frac{\frac{P_{out}}{90\%} \cdot 10\%}{I_{out}} = 0.556V \tag{3.38}$$

$$M_{g\_max} = \frac{2n \cdot (V_{o\_max} + V_{diode} + V_{loss})}{V_{in\_min}} = 1.28 \tag{3.39}$$

To safely reach the gain $M_g = 1.28$ the maximum gain for the design is set to be able to handle 110% overloading, in this case $M_{g\_max} = 1.4$. Figure 2.13 is used to choose possible combinations of Q and m for $M_{g\_max} = 1.4$, in this case $Q = 0.445$ and $m = 4$ are chosen

The equivalent AC resistance for rated operation $R_{AC,min}$ is calculated from (2.21) to

$$R_{AC,min} = \frac{8N^2}{\pi^2}\frac{V_o^2}{P_{o,max}} = 1426.94\Omega \tag{3.40}$$

The resonant inductor L_r is then calculated according to (2.26) as

$$L_r = \frac{R_{AC}Q}{\omega_r} = 1.011mH \tag{3.41}$$

Then from the resonant frequency equation (2.22), the resonant capacitor C_r is

$$C_r = \frac{1}{(2\pi F_{r1})^2 L_s} = 2.506nF \tag{3.42}$$

Finally, the magnetizing inductance calculated according to (2.24) is

$$L_m = m \cdot L_r = 4.044mH \tag{3.43}$$

In order to choose a transformer, the current through the magnetizing inductance needs to be established. It can be calculated by dividing (2.18) by the magnetizing reactance ωL_m as follows

$$I_{m\_peak} = \frac{V_{ACout}}{\omega L_m} = \frac{4 \cdot n \cdot V_o}{\pi \cdot \omega L_m} = 81.5mA \tag{3.44}$$

The core shape and material are primarily taken as $EFD25$ as it fits the transfer power demand in Table 3.3 and with material $N87$ ferrite [27]. For a core temperature of $100°C$ the $N87$ ferrite has a saturation flux density of $390mT$. Using the peak current through the magnetizing inductance the minimum number of primary side winding turns $N_{p,min}$ are calculated with (2.41) to

$$N_{p,min} = \frac{L_m I_{m,peak}}{B_{sat} A_e} = 14.56 turns \tag{3.45}$$

Because the turns ratio is $n = 32.5$ there is no danger of saturation. Thus, the primary turns can be taken as $N_p = 65$ and the secondary turns as $N_s = 2$. The required gap length to reach the magnetizing inductance from (2.42) is then

$$G = 4\pi A_e \left(\frac{N_p^2}{L_m} - \frac{1}{A_L} \right) \cdot 10^{-7} = 0.0397mm \tag{3.46}$$

The wire diameter for the primary side is chosen as $d_{N1} = 0.35mm$ and $d_{N2} = 1mm$. This results in current densities of $Id_{N1} = 1.222A/mm^2$ and $Id_{N2} = 3.005A/mm^2$ which both are below $5A/mm^2$ and therefore fulfills the design requirements. The resulting winding area A_{wr} should be smaller than the winding slot area $A_w = 40.7mm^2$. The copper area is $A_c = 9.395mm^2$, using (2.43) with a fill factor of $k_F = 0.24$ the winding area is

$$A_{wr} = \frac{A_c}{k_F} = 39.15mm^2 \tag{3.47}$$

which is sufficient. The winding resistances are then calculated by (2.39) and (2.40) to

$$R_P = \frac{N_P \rho l_N}{A_{C,prim}} = 0.5675\Omega \tag{3.48}$$

and

$$R_S = \frac{N_S \rho l_N}{A_{C,sec}} = 2.139m\Omega \tag{3.49}$$

In LLC converters it is common to utilize the transformer leakage inductance as part of the resonant tank inductor. Due to this, the leakage inductance is neglected and is assumed to be a part of the resonant inductor L_r.

The output capacitor is calculated according to (2.8) as

$$C_{Out} = \frac{\Delta I_o}{8 f_s \Delta V_{Out}} = 58.9\mu F \tag{3.50}$$

All calculated parameters from the LLC converter design are summarized in Table 3.8.

Table 3.8: Calculated parameters for the LLC half-bridge converter.

Components	Calculated
n	32.5
M_{g_min}	0.975
M_{g_max}	1.28
L_r	1.011mH
L_m	4.044mH
C_r	2.506nF
I_{m_peak}	81.5mA
N_p	65 turns
N_s	2 turns
G	0.0397mm
A_{wr}	40.7mm^2
R_p	0.5675Ω
R_p	2.139Ω
C_{Out}	58.9μF

3.6.1 LLC Component Selection

When choosing components for the LLC converter, the parameters from Table 3.8 are used as a basis. The used components are presented with their required rating in Table 3.9.

Table 3.9: Selected components for LLC converter.

Component	Model	Vbd [V]	R_{on}[Ω]	Gate Charge [C]
Output Capacitor	A700V566M006AT		28m	
Diode	B520C, Schottky	20	1.1	
SR switch	FDC8884	30	19m	5.3n
Primary Switch	IPN80R2K0P7	800	2	9n
Transformer	EF(D) 25, N87			

4

Results

4.1 Electrical Measurements

In this section the efficiency at partial loading of existing DC-DC converters are evaluated. The efficiency curve for three flyback converters of different power levels can be seen in Fig. 4.1.

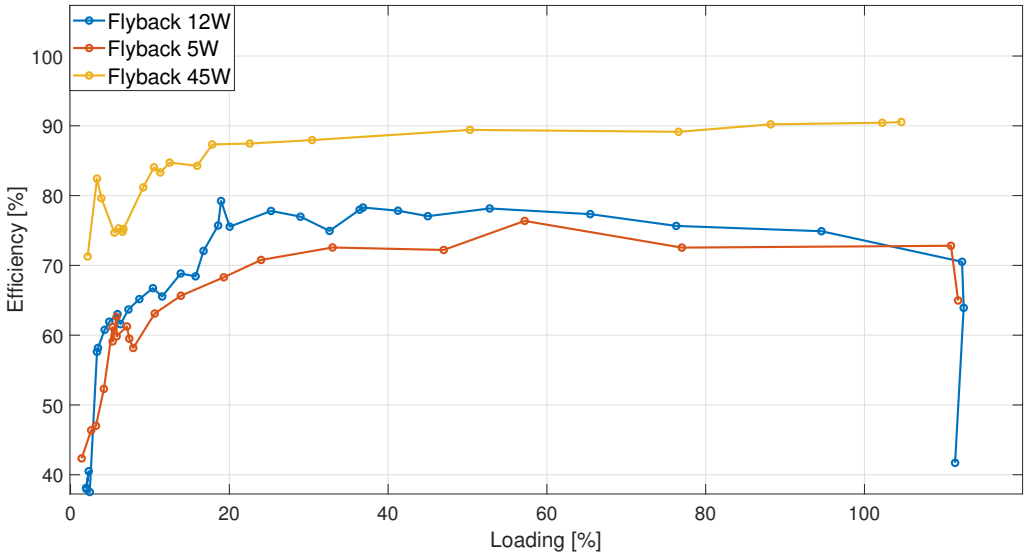


Figure 4.1: Efficiency curve from electrical measurements on three different flyback converters.

The converter curves in Fig. 4.1 show similar behaviour and provide a fairly consistent efficiency from 20% to rated loading. As the load drops below 20% the converters experience severe drops in efficiency. The data points from operation below 20% of load current shows some variation from point to point. This may be partly due to the measurement equipment error shown in Table A.1-A.3 and also due to the low current drawn at these loads. Thus, a small current variation can have a noticeable impact on the calculated efficiency. Above rated load the $5W$ and $12W$ converter efficiency drops which may damage the converter. The $45W$ converter has some kind of overcurrent protection and shuts down for loads drawing more than approximately 105% of rated current.

4.2 Partial Loading

In this section the efficiency of the flyback, forward and LLC converter operating at partial loading are modelled. The efficiency curves for each converter, with and without hysteresis losses are plotted together in Fig. 4.2 and Fig. 4.3 respectively. Because the converter models lack a controller, the duty cycle and switching frequency is controlled manually. This process is iterative and performed until the output voltage $V_o = 5V \pm 0.1V$.

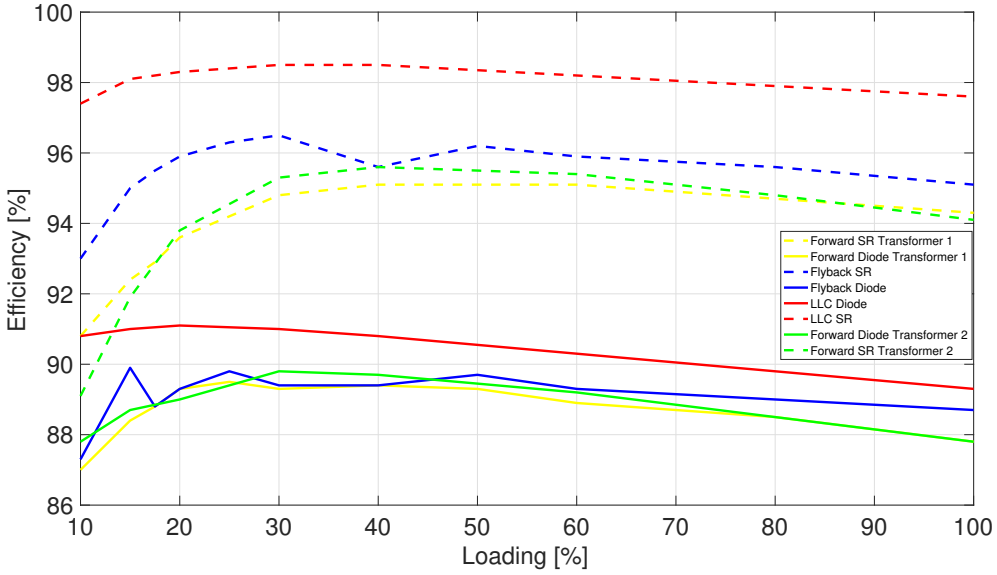


Figure 4.2: Topologies experiencing partial loading without hysteresis losses.

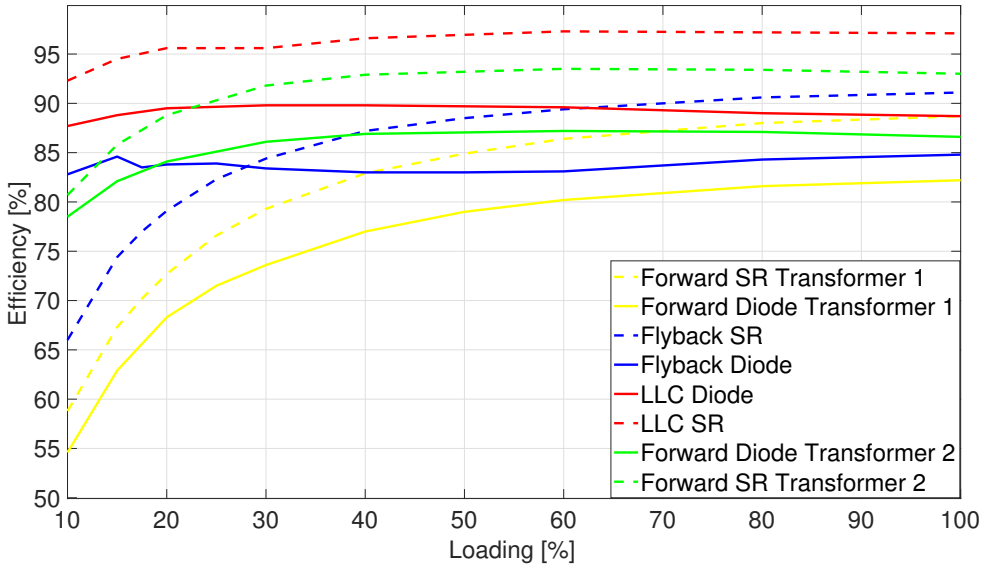


Figure 4.3: Topologies experiencing partial loading with hysteresis losses.

The result show that the LLC with SR, is operating with the highest overall efficiency with and without hysteresis losses. All curves follow a similar behaviour except the one for flyback with diode rectifier. For low loads it has a slight oscillation and less of an efficiency reduction. In Fig. 4.2, without hysteresis loss, the flyback and the two forward converters with diode rectifiers have roughly the same efficiency and with SR the flyback becomes the most efficient. With the hysteresis loss however, the forward converter with transformer 2 becomes more efficient than the other forward and flyback converters. This shows the advantage of the forward converter being able to have a greater magnetizing inductance than the flyback.

The power dissipation throughout partial loading for the forward converter with diode rectifier for transformer design 1 can be seen in Fig. 4.4. It shows the danger of operating above rated load as although the efficiency is increasing the total losses are also increasing non linearly.

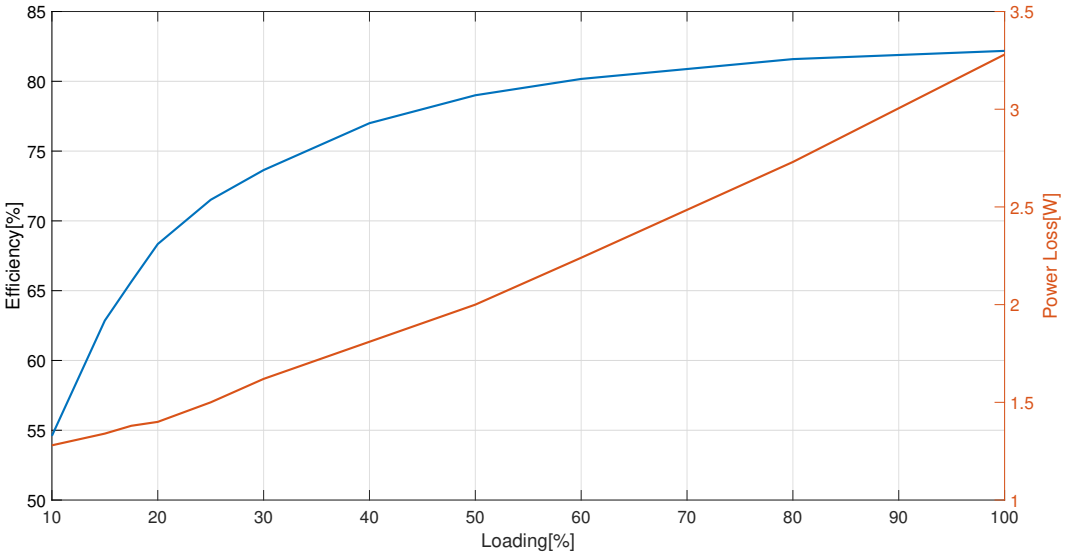


Figure 4.4: Efficiency and power loss comparison of Forward converter with diode rectifier and transformer design 1

The power dissipation caused by each component during partial loading in the flyback converter is presented in Fig. 4.5. The results show that the components that has the largest contribution to the converter efficiency are the diode and transformer. Thus, by reducing the losses in the diode by investing in a diode with lower forward voltage drop and r_{on} or in SR the efficiency can be increased significantly. The transformer loss is almost constant from $60 - 100\%$ due to the flyback entering CCM and thus the magnetizing current remain constant. The primary switch losses increases only slightly as the loading increases, which suggests that the major cause of losses are switching loss due to the low currents. The results also shows how the percentage of the loss decreases significantly as the converter enters CCM between 60-100% loading.

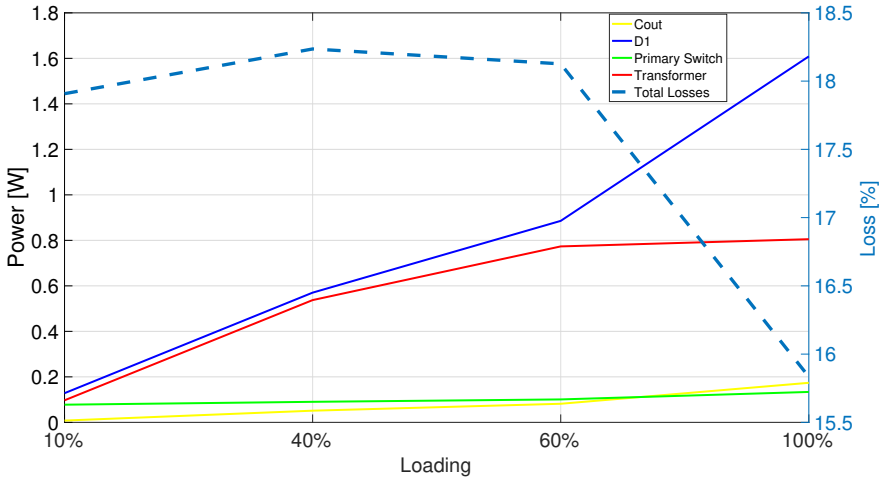


Figure 4.5: Component losses during partial loading of Flyback Converter

The power dissipation caused by the components during partial loading in the forward converter with transformer design 2 is presented in Fig. 4.6. Here, the power loss in the two diodes together with output inductor increases at 60% loading while the transformer remains at a fairly stable consumption due to its high magnetizing inductance. At 10% loading the power consumption caused by the primary switch and diodes are mainly caused by the switching losses and the high forward voltage drop due to the low current. The results also indicates that even though the power consumption of the components increases towards rated power, the percentage of the total loss decreases.

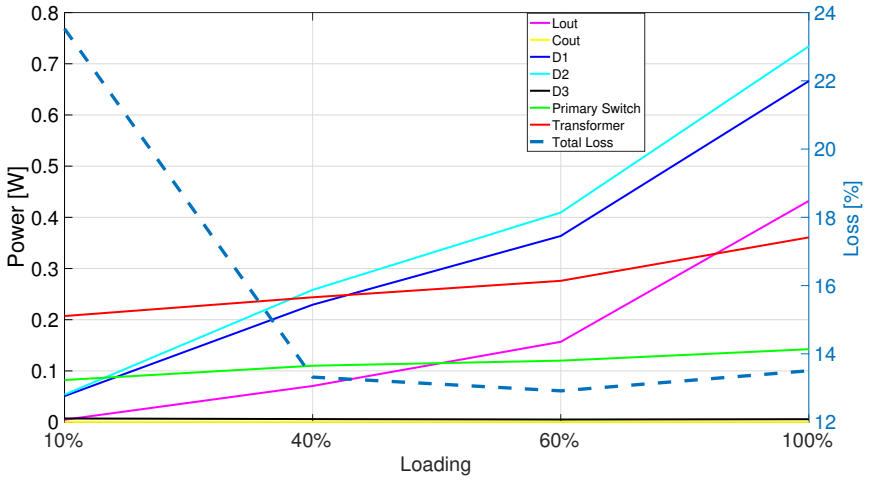


Figure 4.6: Component losses during partial loading of Forward converter with Transformer 2

4.3 Component Losses

The component losses for converters with diode rectifiers is presented graphically in Fig. 4.7 and numerically in Table 4.1. The converters are tested at rated power and their respective component losses are measured to establish their major power consumers.

In the flyback converter the diodes and transformer are the major power consumers with significantly higher output capacitor losses compared to the other converters. The difference between the two flyback topologies is the implementation of the leakage inductance, causing the total circuit losses to increase with $0.3W$, which is an increase of 11.3%, due to the added RCD snubber.

The two forward converters differ in transformer design, to be able to see the significance of the choice of low vs high magnetizing inductance. Figure 4.7 shows that the implementation of the second transformer design reduces the overall power loss by $707.5mW$, which is a reduction of 23.2%, mostly due to lower hysteresis losses. Excluding the transformer losses, the largest losses are caused by the two diodes and output inductor.

The Half-Bridge LLC operates with the best overall efficiency. The contribution of the primary switch is reduced compared to the other topologies due to its ZVS operation but share the similarities of high losses caused by the diodes.

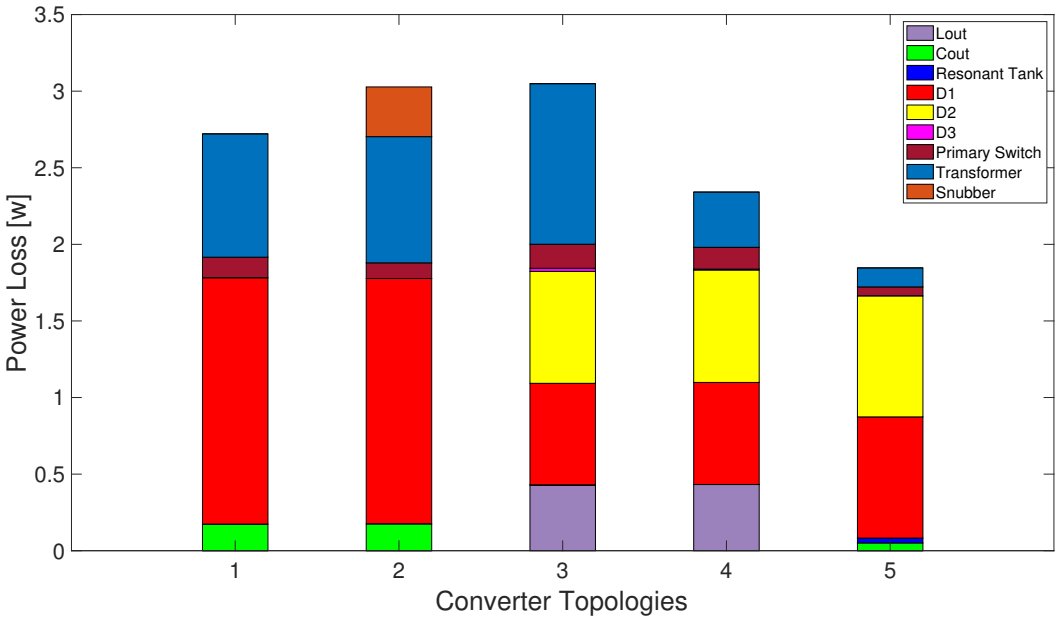


Figure 4.7: Graphical presentation of the component losses in; **(1)** Flyback Diode, **(2)** Flyback Diode Snubber, **(3)** Forward Diode Transformer 1, **(4)** Forward Diode Transformer 2 and **(5)** Half-bridge Diode LLC.

Table 4.1: Component losses of the diode implemented topologies

Component	Flyback Diode [W]	Flyback Diode RCD Snubber [W]	Forward Diode Transformer 1 [W]	Forward Diode Transformer 2 [W]	LLC Half-Bridge Diode [W]
L_{Out}			429.59m	432.10m	
C_{Out}	173.84m	175.56m	413μ	412μ	50.65m
Resonant Tank					31.85m
Diode 1 (D1)	1.6086	1.6015	662.77m	666.06m	791.08m
Diode 2 (D2)			730.42m	734m	790.59m
Diode 3 (D3)			20.20m	5.65m	
Primary Switch	133.72m	102.15m	157.27m	142.34m	57.95m
RCD Snubber		324.58m			
Transformer	805.13m	823.86m	1.04820	360.77m	124.15m
Total	2.72129	3.02765	3.048863	2.341332	1.84627

The component power loss contribution of the converters with SR is presented graphically in Fig. 4.8 and numerically in Table 4.2. The converters are tested at rated power and their respective component losses are measured to establish their major power consumers.

The reduction in power loss caused by SR implementation resulted in significantly higher efficiency for all the converters. The SR and transformer are the leading cause of power loss for both the flyback converter with and without snubber. The SR losses for the two forward converts are relatively low but the loss caused by the output inductor becomes more noticeable. In the half bridge LLC converter with SR the transformer losses are still dominant, although it still has the lowest losses compared to the other topologies.

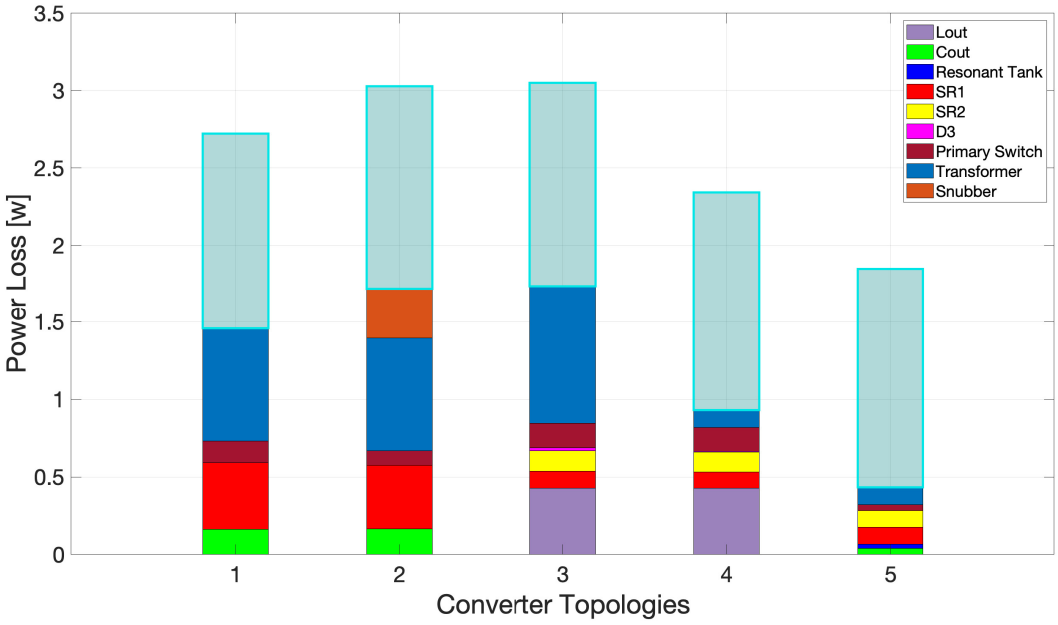


Figure 4.8: Graphical presentation of the component losses in; **(1)** Flyback SR, **(2)** Flyback SR Snubber, **(3)** Forward SR Transformer 1, **(4)** Forward SR Transformer 2 and **(5)** Half-bridge SR LLC. The transparent upper bar signifies the loss difference between diode and SR topologies.

Table 4.2: Component losses of the SR implemented topologies

Component	Flyback SR [W]	Flyback Diode RCD Snubber [W]	Forward SR Transformer 1 [W]	Forward SR Transformer 2 [W]	LLC Half-Bridge SR [W]
L_{Out}			427.25m	427.21m	
C_{Out}	161.71m	164.99m	403μ	401μ	40.38m
Resonant Tank					26.83m
SR 1	430.5m	410.07m	109.94m	103.45m	108.34m
SR 2			131.75m	129.78m	108.58m
Diode 3 (D3)			18.52m	5.65m	
Primary Switch	138.71m	92.84m	159.7m	153.08m	35.82m
RCD Snubber		321.66m			
Transformer	726.78m	727.77m	886.96m	110.80m	114.061m
Total	1.4577	1.71733m	1.734523	930.371m	434.011m

4.4 Modeled Converter Current and Voltage Behaviour

4.4.1 Effects of Leakage Inductance

The voltage across the primary switch for the flyback converter with and without leakage inductance can be seen in Fig. 4.9 and Fig. 4.10. In Fig. 4.9 the first oscillation reaches 800V, the breakdown voltage of the switch, then the voltager ripple slowly dies out. For the case with a RCD snubber in Fig. 4.10, the RCD snubber limits the peak voltage ripple to 732V.

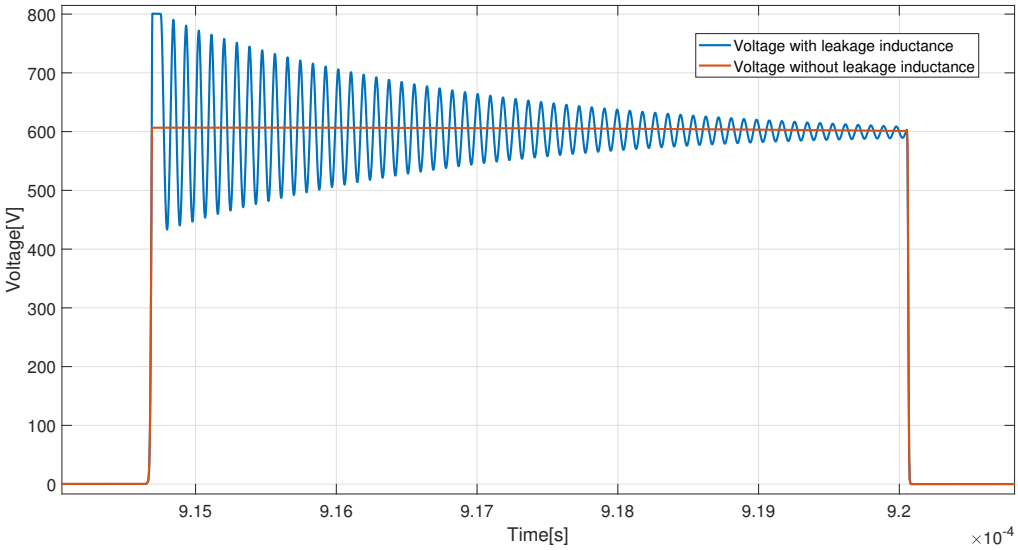


Figure 4.9: Voltage across primary switch, with leakage inductance(blue) and without leakage inductance(red). The leakage inductance contributes to a voltage ripple which reaches 800V and thus causes a breakdown of the switch.

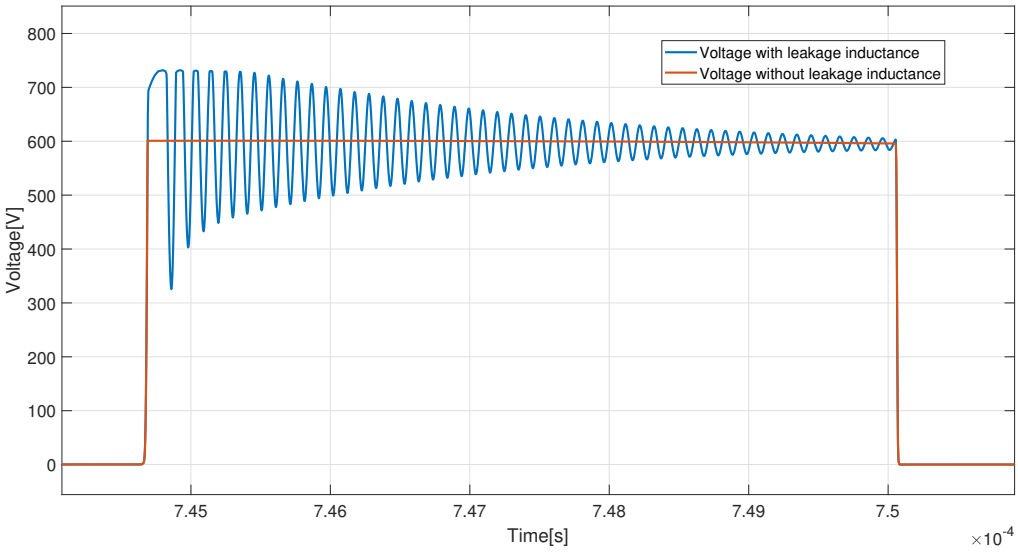
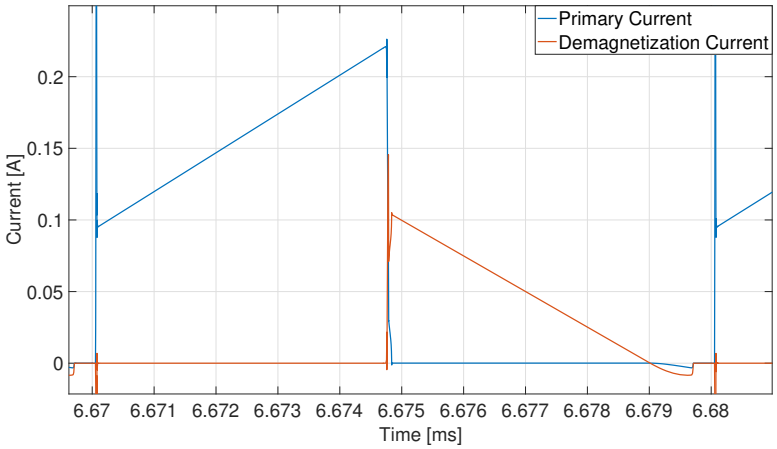


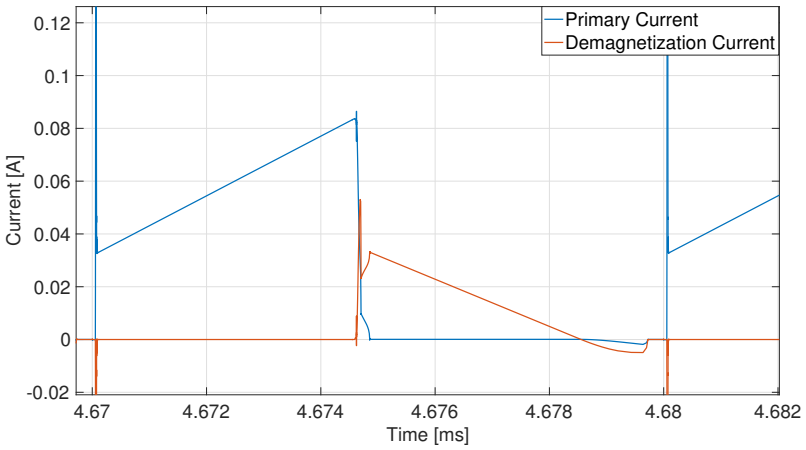
Figure 4.10: Voltage across primary switch, with leakage inductance and RCD snubber(blue) and without leakage inductance(red). With a RCD snubber the highest voltage ripple reaches $732V$, which is within safe operation for the switch.

4.4.2 Impact of Transformer Windings in Forward Converter

The primary and demagnetization current in the diode implemented forward converter are presented in Fig. 4.11. Where Fig. 4.11 (a) and (b) are the current behaviour with transformer design 1 and 2 respectively. The implementation of transformer 2, caused the magnetizing current to drop significantly due to its high magnetizing inductance. The resulting winding and hysteresis losses caused by the two transformer implementations are presented in Table 4.3. The implementation of transformer 2 reduced the hysteresis losses by 75.4% but increased the winding loss by 61.8%. The hysteresis losses in the forward converter with transformer design 1 comprised 92.84% of its total losses, while for transformer design 2 its 50.70%.



(a) Forward converter with diode rectifier and transformer design 1



(b) Forward converter with diode rectifier and transformer design 2

Figure 4.11: The forward converter primary and demagnetizing current through the transformer. Figure (a) has a peak demagnetizing current of 104.43mA. Figure (b) has a peak demagnetizing current of 33.269mA

Table 4.3: The winding and hysteresis losses for the two transformer designs implemented in the forward diode converter.

Transformer components	Case 1	Case 2
Winding Losses [W]	75m	121.37m
Hysteresis losses [W]	973.2m	239.4m
Total losses [W]	1.0482	360.77m

4.5 Economical Impact of Increasing Converter Efficiency

Because a more efficient DC-DC converter has lower energy losses, the end user is able to reduce the energy usage. The converter will also have less of a negative impact on the environment during its operation. To evaluate the economical benefits of upgrading from diode rectification to synchronous rectification a present value analysis is performed using (2.57). The converter used in this evaluation is the LLC half bridge converter which had a reduction in losses of $1.41W$[1] with SR at rated operation. The future electricity price is assumed to be constant and set to the average price per kWh in the second half of 2018. This price is $1.53kr/kWh$ for a normal household with a yearly consumption of $\geq 15000kWh$ and includes various power grid fees, value-added tax and electricity tax [29]. The discount rate is taken as 5% for three different cases to use as a comparison. One case is for a mobile phone charger which will be in use 2 hours per day, a second case is for a LED driver that is in use 24 hours per day and a third case is for a LED driver used 10 hours per day. For the third case with the 10 hour LED driver, the discount rate is varied $p = 5\% \pm 2.5\%$ to compare the effects of different discount rates. The present value for implementing SR in the phone charger and LED drivers can be seen in Fig. 4.12 for different lifetimes. The effect of diminishing return due to the discount rate can be seen as the curves starts tapering off as time goes on.

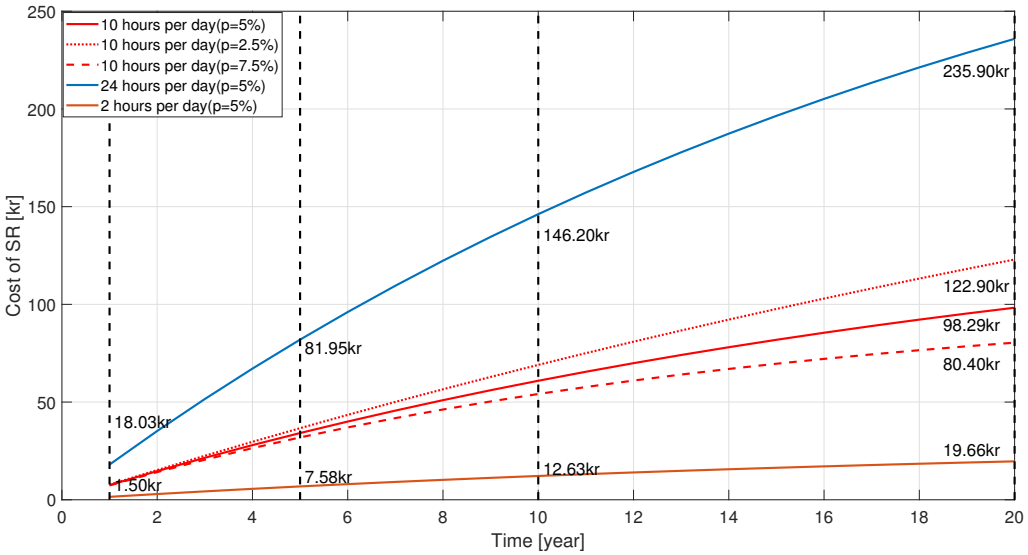


Figure 4.12: Present value analysis for SR implementation in LLC converter. For use $10h/day$ $p = 5\% \pm 2.5\%$(red), $24h/day$ $p = 5\%$(blue) and $2h/day$ $p = 5\%$(brown).

Assuming a normal life time for a phone charger to be five years, highest investment to ensure positive revenue is given to be $7.58kr$ while for the LED drive is $81.95kr$.

[1] Obtained at rated power of $15W$

Thus, there might not be an economic drive for SR in a phone charger, but investing SR into LED driver may lead to a more profitable solution. The effect of varying the discount rate can be seen for the case which is on 10 hours, the red lines starts out similar and as time goes on their inclination differs more and more. Comparing with the converter with $p = 5\%$ after 20 years, with $p = 2.5\%$ the present value is 25.0% higher and with $p = 7.5\%$ the present value is 18.2% lower. This goes to show the importance of estimating the discount rate. Undervaluing the discount rate may lead to overpaying for the components and overvaluing it may lead to missing out on an investment opportunity. For devices with long planned lifetime, efficiency improvements also starts to become more impactful. This goes to show that the application is very important when it comes to increasing its efficiency. This was for a $15W$ converter and as the power levels increases so does the losses, thus there will be an increased present value from reducing losses at higher power levels.

5

Discussion/Conclusion

The results show that the diodes are one of the major causes of power loss and that implementation of SR reduced the total losses significantly. All of the topologies are positively impacted by SR, but its significance is most noticeable in the half-bridge LLC. The effect of tuning the transformer design can be seen in the comparison between the two forward converters. In the first forward design, the core losses where dominant while for the second converter the core losses got reduced by 66%. This shows that the transformer design can be refined to increase transformer efficiency. There are however precautions that must be made when increasing the number of turns, as the leakage inductance increases quadratically with the number of turns. Other possibilities of reducing the core losses could be to re-design the transformer with a smaller core or different ferrite material while still maintaining the same number of turns.

The half-bridge LLC SR proved to be the topology operating with the highest consistent efficiency over the operating region. Its low magnetizing current together with the natural ZVS of the primary switch reduces core and switching losses. After implementing the LLC converter with diode rectifier into LTspice, circuit nonidealities cause the output voltage to fall below $5V$ at unity resonance tank gain. The optimal operating point is for unity resonance tank gain, where the switching frequency is $f_{r1} = 100kHz$ and thus the load was fitted to give $15W$ output power for an output voltage below $5V$. This may result in increased diode losses and might be why the LLC converter shows the best efficiency improvement with SR.

The flyback with diode rectifier deviated from the pattern of reduced efficiency below 20%, this may be due to it entering DCM at about 50% loading. The voltage gain changes for DCM as transfer function become dependent on load resistance, magnetizing inductance and switching frequency, leaving a duty cycle of $D = 0.18$ at 10% loading. By designing the flyback with a lower ripple factor, DCM could be pushed back further. A lower ripple factor would also reduce the transformer hysteresis loss at the cost of requiring a higher magnetizing inductance.

By looking at the electrical efficiency measurements, the difference with the simulations may be partly down to higher quality components but also non-idealities not included in the simulations. Due to a non-optimized transformer, lack of active clamp and demarcated factors like power density, no conclusions on what absolute values of converter efficiency can be determined. What can be concluded is that SR can be used to improve the efficiency significantly and that LLC converters show a lot of potential for efficient power conversion. The present value calculations for

the LLC converter with SR would also suggest that stricter regulations for DC-DC converter efficiency need to be introduced to drive the development of more environmentally friendly converters, as it can not always be justified economically.

6
Future work

To be able to analyze the converter efficiency more accurately, more nonidealities should be implemented into the simulation model. To derive a converter topology with the maximum possible efficiency, materials like GaN and techniques like active clamping should be investigated further.

Transformer: In this thesis the converter transformer was covered lightly, and the design provided was not optimal. An accurate transformer model would help in the understanding of the converter efficiency and would be necessary for accurate modeling. However, the transformer is probably the most complex component in the converter making it not fit the scope of this thesis. A future study would involve evaluating different transformer core geometries and core materials in terms of efficiency, size and EMI. Winding methods, air gap and the effects or raising the frequency would also be interesting.

Controller/Transient analysis: There are many methods to control a switching converter but a study of the performance of different control methods could not be included in this work. This would give insight for implementation of new efficient topologies like active clamping, more optimal usage of SR and possibilities for increasing operating frequency. By implementing a controller, transient analysis would be useful to verify the dynamics of the converter and its applicability to different tasks. This may also be useful in understanding how to efficiently run the converter in partial loading and with varying loads.

GaN HEMT: The emerging technology of high electron mobility transistors like the Gallium Nitride field effect transistor could open up new possibilities for faster switching due to lower gate capacitance while also providing low ON-resistance. However, its still not an established technology and there are not a lot of LTspice models available.

Design a converter with hardware: By constructing a simple converter, following the chosen control IC "typical application" schematic from its data-sheet, simulation can be paired with real measurements. This would allow one to verify the validity of simulations through comparison and find ways to improve them. This would also cause the evaluation to take the power density into account. The power density influences every other part of the design as it is an incentive to push the operating frequency higher and to increase the efficiency to reduce the generated heat.

Active clamp: The idea of implementing active clamp could result in higher ef-

ficiency as energy is not dissipated, but returned to the load. This also opens the possibility to operate with higher switching frequencies as generated heat is reduced. To be able to verify the implementation and efficiency improvement, models should be created, simulated and compared. Possibilities of size and power density comparison between RCD snubber and active clamp could also be of interest.

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A

Appendix

Load[%]	V-in[V]	I-in[A]	P-in[W]	V-out[V]	I-out[A]	P-out[W]	Efficiency[%]	EfficiencyError[%]
1,4	305,3	0,0006	0,168	5,079	0,014	0,071	42,3464	4,7020
2,6	305,3	0,0009	0,281	5,009	0,026	0,130	46,3671	3,1217
3,2	305,3	0,0011	0,342	5,023	0,032	0,161	47,0076	2,6214
4,2	305,3	0,00132	0,403	5,019	0,042	0,211	52,3077	2,4967
5,3	305,3	0,0014	0,437	5,038	0,053	0,267	61,1605	2,7082
5,3	305,3	0,0015	0,452	5,04	0,053	0,267	59,1177	2,5352
5,8	305,3	0,0015	0,467	5,043	0,058	0,292	62,6179	2,6036
5,8	305,3	0,0016	0,488	5,039	0,058	0,292	59,8309	2,3868
7,1	305,3	0,00192	0,586	5,057	0,071	0,359	61,2524	2,0685
7,4	305,3	0,00206	0,629	5,057	0,074	0,374	59,5019	1,8863
7,9	305,3	0,0023	0,687	5,058	0,079	0,400	58,1697	1,7053
10,6	305,3	0,0028	0,849	5,053	0,106	0,536	63,1079	1,5417
13,9	305,3	0,0035	1,069	5,047	0,139	0,702	65,6528	1,3290
19,3	305,3	0,0047	1,426	5,045	0,193	0,974	68,2928	1,1146
24	305,3	0,0056	1,710	5,042	0,24	1,210	70,7782	1,0229
33	305,3	0,0075	2,290	5,035	0,33	1,662	72,5647	0,8853
47	305,3	0,0107	3,267	5,019	0,47	2,359	72,2112	0,7509
57,2	305,3	0,0123	3,755	5,014	0,572	2,868	76,3745	0,7561
77	305,3	0,0174	5,312	5,005	0,77	3,854	72,5469	0,6539
110,9	305,3	0,0225	6,869	4,51	1,109	5,002	72,8113	0,6256
111,8	305,3	0,0141	4,302	2,5	1,118	2,795	64,9747	0,6172

Figure A.1: 5W Converter. Measured values for efficiency calculation with efficiency error.

Load[%]	V-in[V]	I-in[A]	P-in[W]	V-out[V]	I-out[A]	P-out[W]	Efficiency[%]	EfficiencyError[%]
111,42	305,3	0,0210	6,411	1	2,674	2,674	41,7076	0,3624
112,50	305,3	0,0368	11,223	2,657	2,7	7,174	63,9224	0,5187
112,29	305,3	0,0471	14,389	3,765	2,695	10,147	70,5179	0,5623
94,58	305,3	0,0480	14,654	4,835	2,27	10,975	74,8953	0,5966
76,29	305,3	0,0387	11,815	4,882	1,831	8,939	75,6569	0,6114
65,46	305,3	0,0327	9,983	4,915	1,571	7,721	77,3437	0,6342
52,79	305,3	0,0263	8,029	4,953	1,267	6,275	78,1560	0,6567
45,00	305,3	0,0229	6,976	4,977	1,08	5,375	77,0510	0,6604
41,25	305,3	0,0208	6,344	4,988	0,99	4,938	77,8376	0,6776
36,83	305,3	0,0185	5,648	5,002	0,884	4,422	78,2884	0,6966
36,42	305,3	0,0184	5,608	5,004	0,874	4,373	77,9817	0,6949
32,63	305,3	0,0172	5,245	5,02	0,783	3,931	74,9403	0,6774
28,96	305,3	0,0149	4,543	5,032	0,695	3,497	76,9832	0,7205
25,25	305,3	0,0127	3,871	4,97	0,606	3,012	77,8006	0,7627
20,04	305,3	0,0104	3,175	4,987	0,481	2,399	75,5482	0,7943
18,96	305,3	0,0094	2,867	4,992	0,455	2,271	79,2307	0,8686
18,58	305,3	0,0096	2,940	4,991	0,446	2,226	75,7128	0,8212
16,75	305,3	0,0091	2,790	5,003	0,402	2,011	72,0748	0,7995
15,75	305,3	0,0090	2,751	4,98	0,378	1,882	68,4336	0,7640
13,88	305,3	0,0079	2,412	4,986	0,333	1,660	68,8403	0,8178
11,54	305,3	0,0068	2,085	4,934	0,277	1,367	65,5438	0,8411
10,38	305,3	0,0060	1,844	4,942	0,249	1,231	66,7326	0,9201
8,67	305,3	0,0052	1,581	4,955	0,208	1,031	65,1704	0,9909
7,29	305,3	0,0045	1,365	4,966	0,175	0,869	63,6811	1,0721
6,29	305,3	0,0040	1,221	4,98	0,151	0,752	61,5771	1,1247
5,92	305,3	0,0036	1,108	4,918	0,142	0,698	63,0149	1,2397
4,88	305,3	0,0031	0,931	4,929	0,117	0,577	61,9324	1,4007
4,29	305,3	0,0027	0,837	4,935	0,103	0,508	60,7641	1,5027
3,46	305,3	0,0023	0,705	4,943	0,083	0,410	58,1741	1,6665
3,33	305,3	0,0023	0,687	4,947	0,08	0,396	57,6133	1,6890
2,42	305,3	0,0025	0,763	4,938	0,058	0,286	37,5243	1,0035
2,00	305,3	0,0021	0,626	4,948	0,048	0,238	37,9481	1,2083
2,29	305,3	0,0022	0,672	4,946	0,055	0,272	40,5011	1,2111
1,96	305,3	0,0020	0,611	4,951	0,047	0,233	38,1096	1,2405

Figure A.2: 12W Converter. Measured values for efficiency calculation with efficiency error.

Load[%]	V-in[V]	I-in[A]	P-in[W]	V-out[V]	I-out[A]	P-out[W]	Efficiency[%]	EfficiencyError[%]
2,2	305,3	0,0045	1,374	19,2	0,051	0,979	71,2742	1,1942
3,3	305,3	0,0060	1,841	19,21	0,079	1,518	82,4348	1,1377
3,9	305,3	0,0073	2,220	19,21	0,092	1,767	79,6258	0,9875
5,5	305,3	0,0110	3,367	19,2	0,131	2,515	74,6913	0,7680
6,1	305,3	0,0120	3,670	19,19	0,144	2,763	75,3019	0,7512
6,5	305,3	0,0130	3,975	19,19	0,155	2,974	74,8288	0,7276
6,7	305,3	0,0132	4,036	19,21	0,158	3,035	75,2014	0,7278
9,2	305,3	0,0168	5,135	19,21	0,217	4,169	81,1772	0,7373
10,5	305,3	0,0186	5,691	19,21	0,249	4,783	84,0532	0,7468
11,3	305,3	0,0202	6,176	19,2	0,268	5,146	83,3131	0,7288
12,5	305,3	0,0220	6,707	19,2	0,296	5,683	84,7298	0,7307
15,9	305,3	0,0282	8,613	19,2	0,378	7,258	84,2681	0,7020
17,8	305,3	0,0305	9,299	19,2	0,423	8,122	87,3343	0,7213
22,6	305,3	0,0385	11,739	19,19	0,535	10,267	87,4592	0,7072
30,4	305,3	0,0515	15,723	19,18	0,721	13,829	87,9528	0,6978
50,3	305,3	0,0836	25,529	19,15	1,192	22,827	89,4145	0,6960
76,6	305,25	0,1274	38,889	19,1	1,815	34,667	89,1425	0,6874
88,2	305,3	0,1449	44,229	19,09	2,09	39,898	90,2084	0,6942
102,2	305,3	0,1674	51,092	19,07	2,423	46,207	90,4381	0,6946
104,6	305,3	0,1710	52,206	19,06	2,48	47,269	90,5423	0,6952

Figure A.3: 45W Converter. Measured values for efficiency calculation with efficiency error.