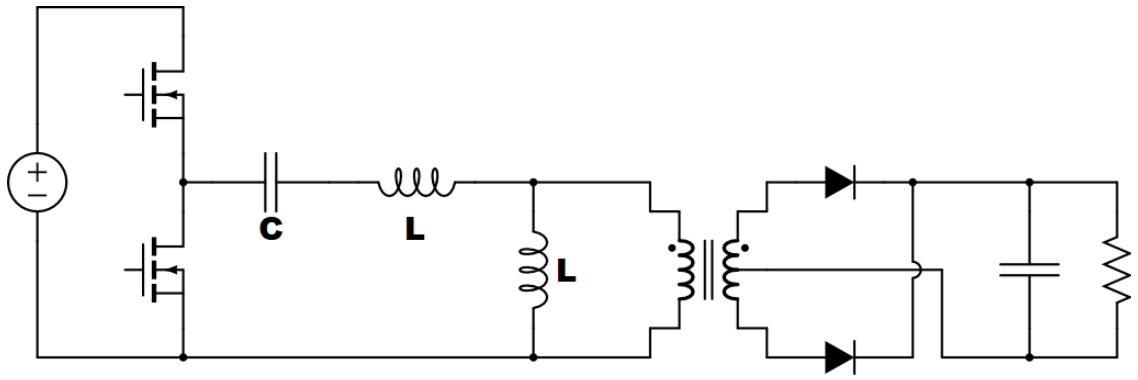
CHALMERS
UNIVERSITY OF TECHNOLOGY



Investigation of LLC converter benefits

A study about resonant converter benefits in low-power telecom applications

Master's thesis in Electric Power Engineering

George Falk
Niklas Midefelt

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

Master's thesis 2019

Investigation of LLC converter benefits

A study about resonant converter benefits in low-power telecom applications

George Falk
Niklas Midefelt

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2019

Investigation of LLC converter benefits
A study about resonant converter benefits in low-power telecom applications
George Falk
Niklas Midefelt

Supervisor: Fredrik Larsson, Ericsson AB
Examiner: Torbjörn Thiringer, Electrical Engineering

Master's Thesis 2019
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: A half-bridge resonant LLC circuit which is investigated in the report.

Typeset in LaTeX
Gothenburg, Sweden 2019

Investigation of LLC converter benefits
A study about resonant converter benefits in low-power telecom applications
George Falk
Niklas Midefelt
Department of Electrical Engineering
Chalmers University of Technology

Abstract

The report covers the topic whether if it's beneficial to exchange an active clamp forward converter to a resonant LLC converter for a certain telecom application with 55W of output power. Theoretically the resonant converter should perform better with its zero voltage switching, also known as soft switching. The investigation is performed by simulating both the circuits to be able to draw conclusions. The main aspects to evaluate is the efficiency, the electromagnetic interference and the cost of the converters. The efficiency at the operation point of the forward converter was simulated to 95.4% and the resonant converter to 95.3% respectively, for a 300kHz design. What was also found to be interesting is that when the switching frequency was doubled, it was found that the forward converter efficiency is 92.1% and the resonant converter efficiency is 94.7%. This lead to a sidetrack where increasing the switching frequency was explored, which is clearly in the resonant converters favour. The electromagnetic performance is better for the resonant converter and the cost of both converters in terms of component count is approximately the same. For the same input/output scenario as used today in the application, the resonant converter was found to have a possibility to perform marginally better, but it is not certain without a physical product.

Keywords: Resonance converter, Efficiency, EMI, LLC, Zero voltage switching.

Acknowledgements

We want to thank Fredrik Larsson, our supervisor at Ericsson, who gave us guidance through the project. Additionally we want to thank our examintor Torbjörn Thiringer who besides his role as examinator gave as a push in the beginning of project, when the going was though, and pointed out more than once which improvements that could be done.

Besides giving our gratitude to the company Ericsson, we want to thank Stefan Bryne. Stefan is a consultant working at Ericsson who was much welcome to discuss technical details about our project, especially concerning semiconductor devices, his area of expertise.

Contents

List of Abbreviations

V_{DS}	Drain Source Voltage of MOSFET
V_{GS}	Gate Source Voltage of MOSFET
CCM	Continuous Conduction Mode
CM	Common mode
DM	Differential mode
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
HB	Half-Bridge
HBLLC	Half-Bridge LLC converter
LCC	Converter with 1 inductance and capacitor in series with a capacitor in parallel
LLC	Converter with 1 inductance and capacitor in series with an inductance in parallel
PCB	Printed Circuit Board
PRC	Parallel Resonant Converter
SPRC	Series-Parallel Resonant Converter
SRC	Series Resonant Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1

Introduction

1.1 Problem Background

Within telecommunication the standard supply voltage for the system is $-48V$ [1]. Usually there is a need for $12V$, $5V$ and $3V$ on the printed circuit board (PCB) and this is achieved through on-board converters [2]. Traditionally, hard switching topologies have been chosen due to their simplicity and low price. The consequences of using hard switching methodologies is high switching stresses and for higher frequencies, large spikes in current ($\frac{di}{dt}$), as well as voltages ($\frac{dV}{dt}$), creating electromagnetic interference (EMI) [3].

Another topology of converters are resonant converters, which switches with zero voltage over or zero current through the switch which increases the efficiency and decreases the EMI [3]. The topology has been used in telecommunication industry for powers in the kW range, the front end conversion [4], [5]. A resonance converter could also affect the entire board for the better with reduction of EMI from the converter. It could therefore be interesting to investigate how the resonant converter is suited for lower powers and on-board conversions for a telecommunications PCB compared with a switch mode topology as done today. Figure 1.1 shows an overview of a telecommunication power system and how the voltage level is transformed from grid level to PCB levels through the front end and the on board conversions stages, where the focus of this investigation is the on board conversion.

The results from this project can be relevant for other on board power converter designs, especially within telecom. Interesting sustainable and social aspects regarding project are material selections, energy usage and efficiency.

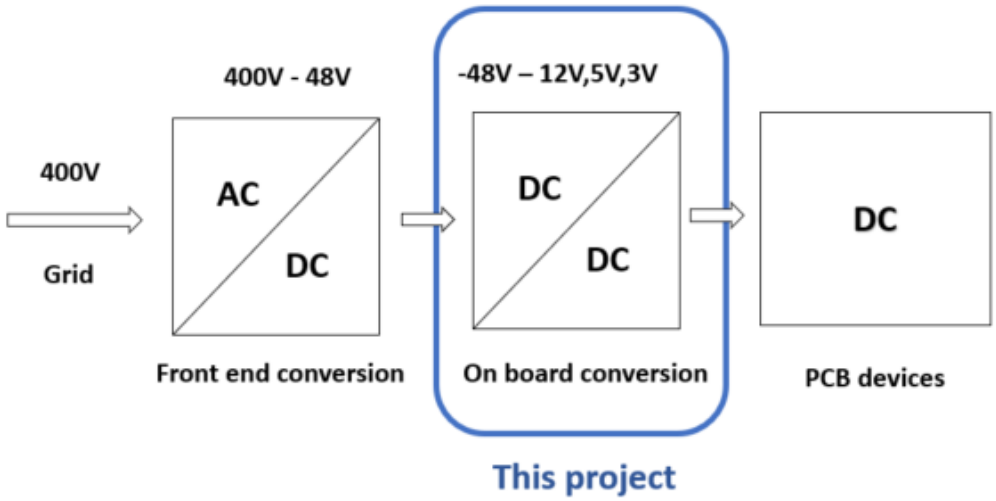


Figure 1.1: Overview of a telecommunication power system and focus of project

1.2 Previous Work

The majority of previous work for the resonant converter topology has been done for optimizing the efficiency and usually for higher power ratings (kW), such as in front end telecom applications but also the technology has become popular concerning battery charging for electric vehicles [6], [7].

Investigations with ratings of 150W has been done where different resonant circuits and converter topologies has been used, where results in efficiency's are promising, compared to conventional hard switching converters [8]–[11] . A rated power of $100W$ has been implemented as well with a high voltage input ($400V$) compared to an telecom on board scenario ($-48V$), where different voltage and current scenarios will change design aspects in many details in [12]. Resonant circuit implementations has been done for lower power ratings as well, such as zero voltage transitioning buck converters within $15 - 35W$ and $15 - 50W$ range, where the simulated efficiency results are approximately 95 percent over the complete power range [13], [14].

Considering EMI, resonant circuits are usually known for low EMI, but as the $\frac{dv}{dt}$ waveforms are reduced more low frequency noise content appears [15]. Differential mode (DM) noise is not a problem, but common mode (CM) noise due to $\frac{dv}{dt}$ from converter nodes propagating through parasitic capacitance's from transformer windings into ground causing noise [16]. Ways of handling this can be shielding or interleaving the current [17], [18].

All in all many investigations have been done within the resonant converter topic but the majority been done for higher power ratings and optimized considering primarily efficiency. The results from this investigation will help in either recommending or not recommending the resonant topology for low power ratings for instance for on board PCB design.

1.3 Purpose

To investigate if there are any and what suitable resonant converter alternatives for the specific DC/DC application within $50 - 60W$ power range that is used today considering efficiency, EMI and cost. Secondly, present a suitable design.

1.4 Scope

The investigation targets a converter with the specification presented in Table 1.1. There are other scenarios where the converter could be implemented but this thesis work will focus on this specification.

Table 1.1: Converter specification

Input Voltage	36-60 V
Output Voltage	5-6 V
Output Power	50-60 W

The primary focus of the report is investigating if resonant converters are suitable for the application and secondly to construct a suitable design. Due to time limitations and workload a complete manufactured converter will not be made. The consequence of the last mentioned point is that no physical measurements will be conducted on the designed circuit which limits the comparison of the simulation and actual measurement.

A delimitation will be to not check the thermal properties of the components. This is to limit the amount of complexity of the project. The thermal aspect does not directly affect the efficiency or EMI if its assumed that the circuit does not break with the chosen components due to thermal characteristics. This decision is made since the study will be theoretical.

Simulations are considered as steady state evaluation where transient events not related to the steady state operation such as start up transients, sudden line and load variations are not considered. In other words the stages front end conversion and PCB devices in Figure 1.1 are considered as ideal and constant. For evaluating the resonance converters suitability, the drive circuit implementation is excluded. The specific drive circuits for the switches and feedback control between input and output is not investigated.

Conclusions regarding radiated EMI will have to be excluded. This is because the simulation tool does not provide any information regarding this and the circuit will not be built and therefore there will be no measurements.

1.5 Environmental and Ethical aspects

In an investigation and design stage the environmental and ethical aspects should be considered so that the products can go through laws and legislation's. Within EU the Restriction of Hazardous Substances Directive exists (RoHS) [19]. The aim is to reduce the amount of electrical and electronic equipment that is going to waste and not being recycled. If the resonant converter shows higher efficiency than the hard switched, then the frequency of design can be increased and the size of the passive components can be reduced. This will reduce the amount of material usage for components such as capacitors, inductors and transformers, which is beneficial.

DC/DC converters use switches which usually are semiconductor devices. Semiconductors are using combinations of materials such as Silicon Carbide SiC, or a new trend for recent years, Gallium Nitrate GaN for high frequency designs (MHz). If using GaN is more unsustainable than using SiC, then higher frequency selections has a disadvantage. How the selection of components is done must consider how the extraction of the raw materials that affect the environment and can therefore affect design choices.

An investigation resulting in a more efficient DC/DC converter for the application than the existing converter could be for the greater good as less electricity would be needed, Even if the electricity used is unsustainable produced or not, a solution with higher efficiency would use less of the electricity, which is good.

Concerning ethics and telecommunication two relevant aspects are military usage and wire-tapping. Could this project in the long run improve products that are used in a purpose of hurting people or perhaps spying purposes? How the company uses its product is hard to say but until someone proves unethical usage, it will be assumed no harm is done from products or their application.

2
Theory

This chapter will present the most important theory and background material to the project results.

2.1 Resonant Converters

The difference from the hard switching converters is that the resonant converters has a so called resonance circuit that is constructed with different configurations of inductances and capacitors depending on which characteristics that are required. The load resonant converters are using a resonance tank which allows what is called soft switching, which reduces the stress on the switch and should allow higher frequencies to be utilized as the switching losses decrease [20]. The following section will present the basic concepts and usual configurations of this category of resonant DC DC converters

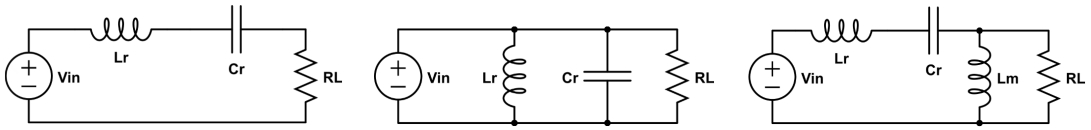
2.1.1 Load Resonant Converters

The load resonant converters can be divided into three groups, the series, the parallel and the series-parallel. Series resonant converters (SRC) has as resonant tank, an inductor and a capacitor, in series with the load. The SRC acts like a current source for the load. The major advantages of this type of configuration is the low device current and low conduction loss. Another advantage is that the series capacitor makes it difficult to saturate the transformer since it blocks the DC component of the current. The disadvantages is that the output voltage is difficult to regulate during low or no load conditions and the output capacitor has to be able to handle high output ripple current. This makes it difficult to be in high current and low voltage applications. As the tank is in series with the load, the voltage gain will never be above 1 [21].

As the name suggests, the difference of the SRC and the parallel resonant converter (PRC) is how the load is connected. By connecting the load in parallel the PRC acts like a voltage source instead of a current source. The PRC does not need as big variation in frequency as the SRC to control the output voltage with load variations. The output current of the PRC is independent of the output voltage. The advantage of the PRC is that is suitable for high current and low voltage application and the load can also be short circuited. The PRC has a high device current, which does not decrease with the load, which leads to bad efficiency at lighter loads which is its

major disadvantage.

Series-parallel resonant converters (SPRC) combines the advantageous characteristics of the SRC and PRC which makes it a good option to use. It has an additional capacitor or inductor connected in the resonant tank. All of the variations can be seen in Figure 2.1 The 2 most common combinations of SPRC circuits are the LLC and the LCC. The LLC is a SRC which has an extra inductor connected in parallel making it a SPRC and the LCC is the same but with a capacitor in parallel. There are a lot of other combinations that are possible for the resonant tank [20].



(a) SRC **(b)** PRC **(c)** SPRC

Figure 2.1: Conventional Load Resonant Converters

2.1.2 Switching Methodology

Switching losses for power converter applications are one of the biggest issues together with conduction losses. Higher switching frequencies makes it possible to reduce the size and weight of the components which is beneficial, but the upper frequency limit depends on how much switching losses that can be tolerated. It is possible to use snubber circuits, to move the switching losses but instead energy is dissipated in the snubber [3]. Two methods to reduce switching losses for the resonant converter are to accomplish either zero current switching (ZCS) or zero voltage switching (ZVS).

To reduce the electrical stress during turn on for a switch it is beneficial with zero voltage over switch before the turn on process starts, hence ZVS. ZVS is achieved by reducing the voltage over the switch by external means so that there is no voltage over the switch when it turns on [20], [21]. Figure 2.2 shows an example of a MOSFETs turn on process where the drain source voltage has dropped to zero before the gate signal is applied.

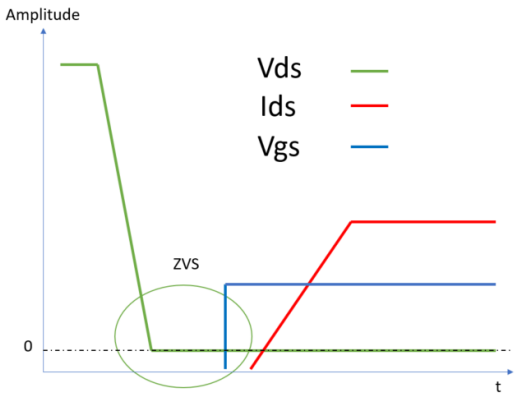


Figure 2.2: ZVS during turn on process of MOSFET

To reduce electrical stress and losses over the switch during the turn off process, the current conducted through the switch should be zero. This why it is called zero current switching (ZCS). If the current is not zero, power dissipation will appear during the turn off process when the voltage increases over the switch. To prevent this the goal is to shape the current waveform during the conducting time interval, by using inductive and capactive elements so that the current is zero when the turn off process of the switch starts [20].

Both ZVS and ZCS reduces the losses but ZVS is preferred due to during the turn on process reverse recovery of the free wheeling diode exists. ZVS is usually preferred such that the biggest loss is reduce.

2.1.3 Working Principles

The half bridge LLC (HBLLC) circuit is presented in Figure 2.3, where compared to an ordinary half bridge a resonant tank is placed on the primary side and the inductor between the output capacitor and output load is not needed. The circuit operation is similar to a half bridge converter but with a sinusoidal waveform of the current i_{Lr} due to the resonant tank. Similar as an ordinary half bridge there is a transformer magnetizing current i_{Lm} which changes sign of the slope dependent on the voltage v_{Lm}, which is dependent of which switch Q_1 or Q_2 that is conducting. The voltage of L_3 is positive for positive v_{Lm}, causing D_1 to conduct and the other way around for D_2.

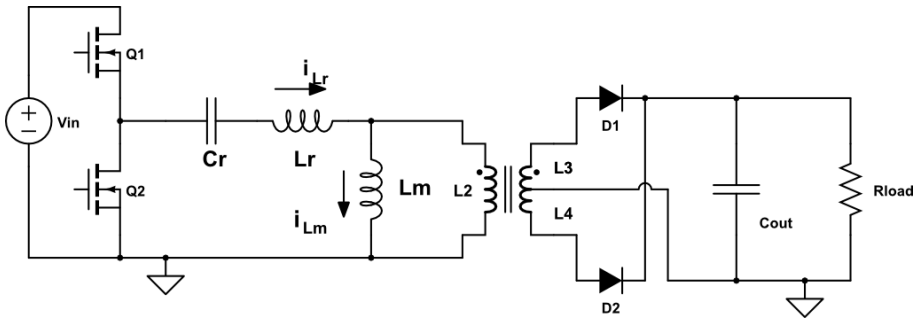
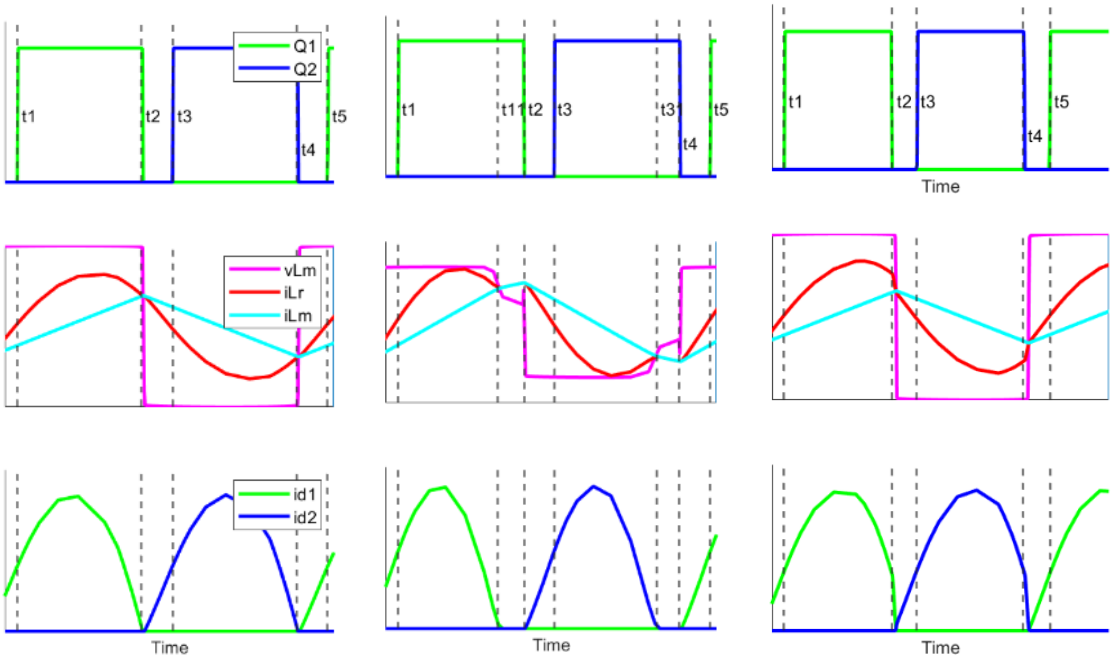


Figure 2.3: Basic schematic of the HBLLC converter

The topology uses a frequency based control where varying the switching frequency instead of duty cycle the impedance of the resonant tank causes to vary and therefore the output voltage can be controlled. Depending on how much gain is needed, the switching frequency has to be changed relative to the resonance frequency. Both increasing and decreasing voltage gain is possible by changing the switching frequency above or below the resonance frequency. In Figure 2.4 the most important waveforms of the converter is presented for three different frequency operations. Between times $t1$-$t2$ Q1 is active, between times $t3$-$t4$ Q2 is active, cycle repeats at $t5$.



(a) $f_{sw} = f_0$ **(b)** $f_{sw} < f_0$ **(c)** $f_{sw} > f_0$

Figure 2.4: Operational waveforms HBLLC

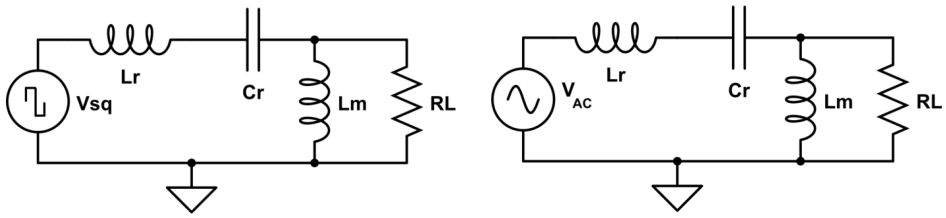
- $f_{sw} = f_0$ normalized gain:
  When the switching frequency equals the resonance frequency the current through the resonant inductor,i_{Lr}, is continuously conducting which results in a continuous power transfer, see Figure 2.4a. The power transfer through diodes changes direction when i_{Lr} equals the magnetizing current , i_{Lm}. Between times t_2-t_4 the transformer voltage, v_{Lm}, will be negative, resulting in diode D_2 conducting. Between times t_4-t_2 v_{Lm}, will be positive, resulting in diode D_1 conducting.

- $f_{sw} < f_0$, boost operation:
  When the switching frequency is lesser than the resonance frequency the currents i_{Lr} and i_{Lm} will become equal before Q_1 turns off. This leads to an interval t_{11}-t_2 without power transfer and circulating currents instead, see Figure 2.4b. The power transfer will continue when Q_1 turns off, resulting in a change of the transformer voltage, v_{Lm}, from positive to negative. In the primary side current changes direction and instead diode D_2 will conduct.

- $f_{sw} > f_0$ buck operation:
  When the switching frequency is higher than the resonance frequency, the switch Q_1 will turn off before currents i_{Lr} and i_{Lm} are equal, resulting in extra switching losses, see Figure 2.4c. The power transfer is continuous where the diode D_2 conducts for negative v_{Lm}, which is between $t2$-$t4$, and vice versa for diode D_1. Secondary side rectification is not soft switched for this operation.

2.1.4 Analytic Model of the Converter

For designing a resonant converter a transfer function is helpful to predict the circuit behaviour for different frequencies. As a complete converter circuit includes switches, duty cycles and other problematic considerations, a simplification called First Harmonic Approximation is often used for AC analysis [21]. The primary side voltage source and bridge switches are represented as an square wave voltage source, which can be simplified as an AC input only including the first harmonic of the DC signal. Figure 2.5a shows the DC simplification and Figure 2.5b shows the AC simplification of circuit. The secondary side of circuit is simplified and transformed to primary side of circuit and represented as a resistive load.



(a) Nonlinear DC sqaure wave input

(b) Linear AC input simplification

Figure 2.5: First Harmonic simplification of load resonant converter

2.1.5 Circuit Design

To design the resonant converter according to the characteristics that it needs, certain parameters has to be determined or chosen. The following equations will be used to achieve the correct characteristics of the converter, starting by choosing the resonance frequency which is going to be utilized.

The resonance frequency of the LC resonance tank is calculated as,

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}[Hz] \tag{2.1}$$

where L_r is the resonance inductance and C_r resonance capacitance.

For many calculations the normalized frequency is used. This normalized frequency is

$$f_n = \frac{f_{sw}}{f_0}[Hz] \tag{2.2}$$

where f_{sw} is the switching frequency and makes it possible to calculate the gain achieved with any switching frequency. By calculating with the normalized frequency it is possible to chose the resonance frequency and switching frequency to a desired level after calculating most of the parameters.

When having an LLC circuit there are 2 frequencies where the circuit resonates since there is a magnetizing inductance, L_M. This frequency is called f_p and is defined as,

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_M)C_r}}[Hz] \tag{2.3}$$

where L_r is the resonance inductance, L_M is the magnetizing inductance and C_r resonance capacitance.

The ratio between the magnetizing inductance and the resonant inductor is called L_n,

$$L_n = \frac{L_M}{L_r} \tag{2.4}$$

and is important for the characteristics of the converter. A higher value improves efficiency and increases the switching frequency spectrum needed while some of the achievable gain is lost. A lower ratio requires a more narrow frequency spectrum and the achievable gain is increased, but is less efficient. Which means that there is a trade of. L_n is usually in the range of 1-10. [21], [22].

The equivalent resistance of the load can be calculated as

$$R_e = \frac{8n^2V_o}{\pi^2 I_o} = \frac{8n^2}{\pi^2}R_L[\Omega] \tag{2.5}$$

where V_o is the output voltage, I_o is the output current and R_L is the load resistance.

The quality factor Q_e is a factor to help the design of the voltage gain characteristics of the converter. The quality factor describes how damped the resonant circuit is. A higher quality factor results in a more narrow bandwidth of the converter. This factor is defined as

$$Q_e = \frac{\sqrt{\frac{L_r}{C_r}}}{R_e} \tag{2.6}$$

where R_e is the equivalent resistance from (2.5).

The possible voltage gain of the converter is defined as M_g and is obtained by the converters transfer function, see Figure 2.5b, which yeilds

$$M_g = \mid \frac{(j\omega L_r || R_e)}{(j\omega L_r || R_e + j\omega L_r + \frac{1}{j\omega C_r})} \mid . \tag{2.7}$$

But with the the normalized variables derived in (2.2), (2.4), (2.5) and (2.6) the equation for the voltage gain can be rewritten into a normalized version. This means

that the equation can be used without having any specific values for the components. It makes it possible to use this equation to design the gain characteristics of the converter when there are a lot of uncertainty's regarding component values but the amount of needed gain is known. The equation is rewritten to,

$$M_g = \left| \frac{L_n f_n^2}{[(L_n+1)f_n^2 - 1] + j[(f_n^2 - 1)f_n Q_e L_n]} \right| . \tag{2.8}$$

After the needed voltage gain has been determined, the transformer ratio n in a half bridge converter can be calculated by

$$n = M_g \frac{V_{in}}{2V_o} \tag{2.9}$$

where V_{in} is the input voltage, V_o is the output voltage and M_g is the desired gain over the resonant tank. At resonance frequency M_g is 1.

The voltage gain interval shall make it possible to obtain the highest but also the lowest output voltage. This should also take the input voltage in consideration, a lower input voltage would require a larger gain to achieve the correct output voltage for example. The maximum voltage gain can be obtained through

$$M_{g,max} = \frac{2nV_{o,max}}{V_{in,min}} \tag{2.10}$$

The minimum voltage gain is defined as

$$M_{g,min} = \frac{2nV_{o,min}}{V_{in,max}} \tag{2.11}$$

Figure 2.6 shows the maximum gain value of given a Q by varying L_n in (2.8). This makes it possible to choose the appropriate induction ratio to achieve the correct voltage.

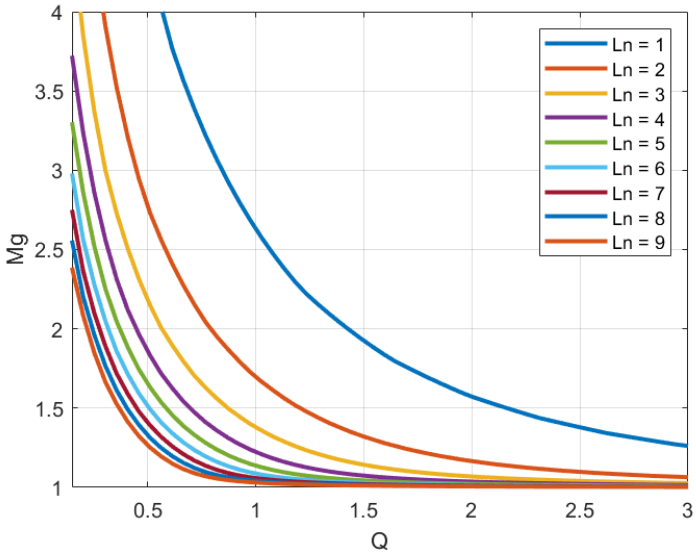


Figure 2.6: Voltage gain as a function of Ln and Q

A selected inductance ratio, L_n, can be used with a varying quality factor instead which is shown in Figure 2.7. The figure shows the amount of gain which is achievable with different quality factors for a normalized frequency from (2.2). It can be observed that all quality factors generate a voltage gain of 1 at the resonance frequency, ($f_n = 1$). The boundary between ZCS and ZVS can be visualized by the black dotted line. To achieve ZVS the converter needs to always operate at a higher frequency then at the maximum gain for the selected Q value, in other words, at a higher frequency then the black dotted line. Figures 2.6 and 2.7 displays (2.8) in two different ways. They are helpful in designing the converter since they both display how the different parameters affect the voltage gain.

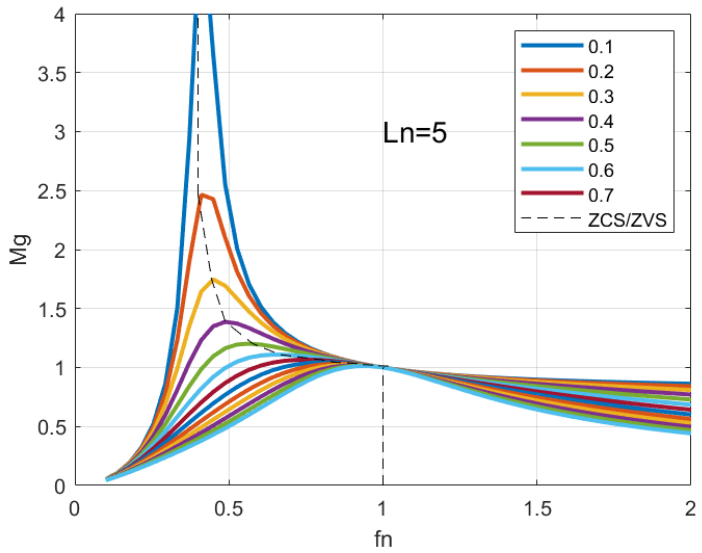


Figure 2.7: Voltage gain vs normalized frequency for a selected Ln and varying Q

2.1.6 Ensuring Zero Voltage Switching

To ensure there is enough inductive energy according to [21]

$$\frac{1}{2}(L_M + L_r)I_{mPeak}^2 \geq \frac{1}{2}(2C_{eq})V_{in}^2, \tag{2.12}$$

where I_{mPeak} is the peak magnetizing current and C_{eq} the equivalent stray capacitance. The deadtime t_{dead} should be sufficiently large so that MOSFET drain source voltage can fall to zero before turn on, yielding

$$t_{dead} \geq 8C_{eq}f_{sw}L_M. \tag{2.13}$$

A third condition that is important as well is that

$$C_r > C_{eq} \tag{2.14}$$

where C_r is the resonant capacitor. If the condition is not full filled, the energy conversion from C_r during dead time can not be ignored, which will interfere with

the C_{ds} charge and dicharge process. In a simplified case with no stray capacitance in the circuit, $C_{eq} = 2C_{ds}$, the MOSFETs drain source capacitors. Operating in ZCS the soft switching of the primary side switches is lost and therefore not beneficial. High current spikes are produced from reverse recovery spikes from the body diode during turn on, which causes both losses and more EMI emissions [21].

2.2 Forward Converter

The forward converter is a step down, hard switching converter. The forward converter is derived from the buck converter but with a transformer in the circuit. For continuous conduction mode (CCM) the ratio between the input and output is,

$$\frac{V_o}{V_d} = \frac{N_2}{N_1} D \tag{2.15}$$

where V_d is the input voltage, $\frac{N_2}{N_1}$ is the turns ratio and D is the duty cycle.

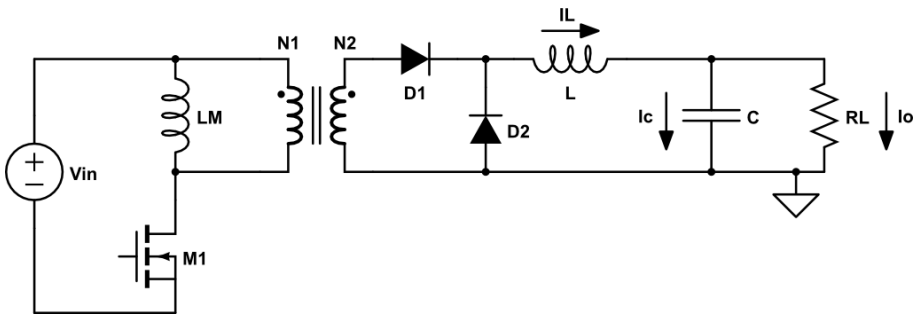


Figure 2.8: Forward Converter

Figure 2.8 displays a forward converter and the important currents and their direction.

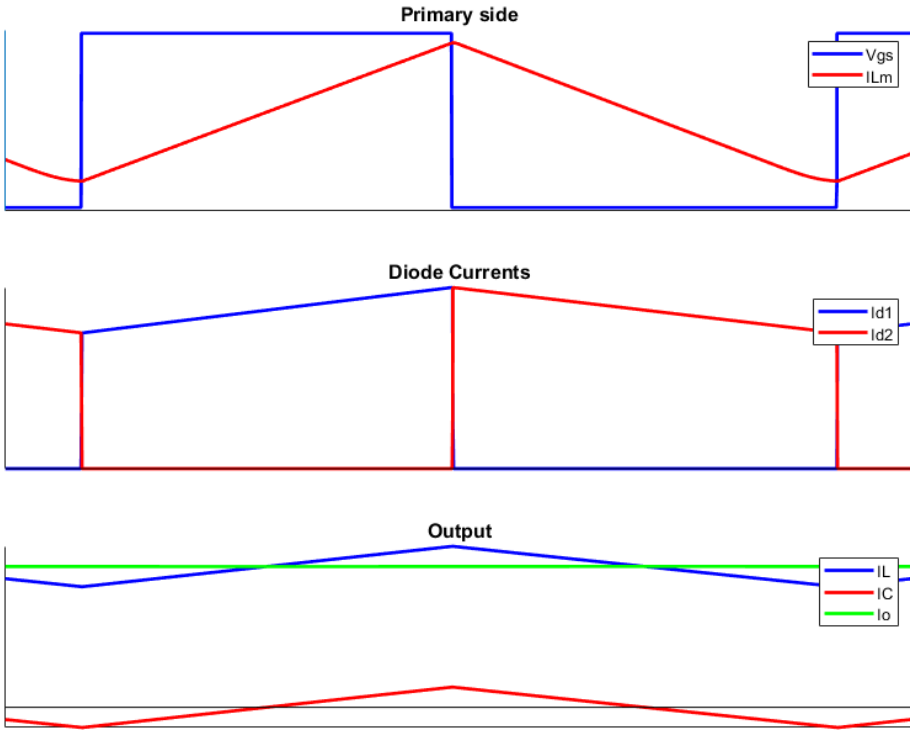


Figure 2.9: Working principle waveforms for the forward converter

During CCM the forward converter is expected to have the currents displayed in 2.9. It can be observed that the transformer magnetizing current, I_{Lm}, increases when the switch is on and decreases when the switch is of which is what transfers power through the transformer. The diode currents I_{d1} and I_{d2} is the same as I_L. To get a DC output I_L needs to be compensated with the output capacitor. This is displayed by I_C which oscillates around 0. When $I_L > I_o$ the capacitor is charged and when $I_L < I_o$ the capacitor is discharged.

2.2.1 Active Clamp

An issue with the forward hard switching converter is the hard switching. To lower the losses the utilization of an active clamp is possible. An active clamp is a capacitance and switch in parallel with the original switch, which is turned on when the MOSFET (M1) in Figure 2.8 is turned off. The capacitance (C_{clamp}) discharges when the M2 MOSFET is turned on in Figure 2.10 which also displays the active clamp.

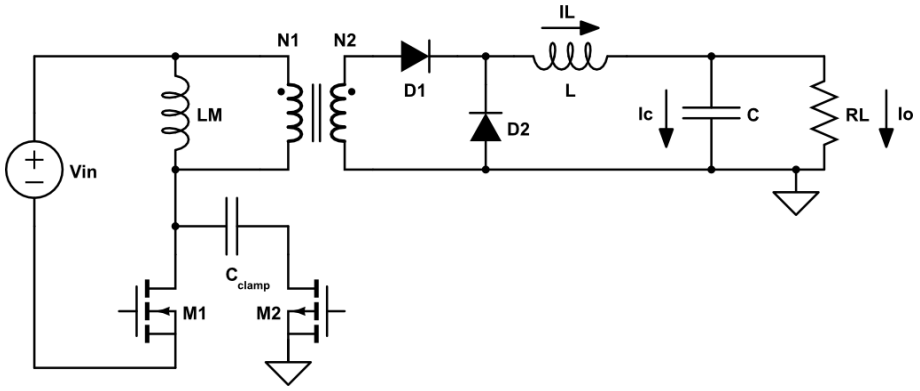


Figure 2.10: Forward converter with active clamp

The energy in the magnetizing inductance must be equal during on and off time of the switch,

$$V_{in}DT = (V_{Cclamp} - V_{in}) \cdot (1 - D)T \tag{2.16}$$

in steady state operation where T is the whole period and D is the duty cycle. Which means that the needed capacitor voltage rating can be calculated as,

$$V_{Cclamp} = \frac{V_{in}}{(1 - D)} \tag{2.17}$$

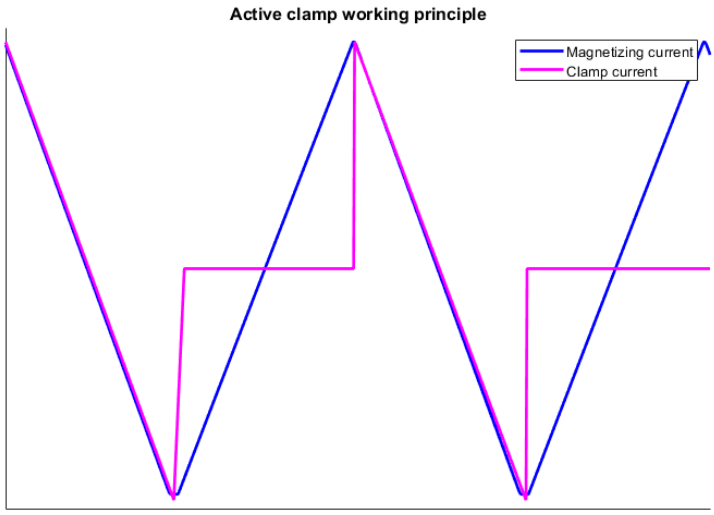


Figure 2.11: Magnetizing and active clamp current

In Figure 2.11 the ideal current waveforms are displayed. They illustrate how the clamp capacitor is used together with the magnetizing current. When the main switch is on and the magnetizing current is rising the active clamp is turned off and the other way around.Benefits of an active clamp is the reduction of switching losses and the energy stored in the magnetizing inductior is circulated rather than dissipated [23].

2.3 Power Electronics Losses

All types of converters do have losses which effects the efficiency. There are different losses and they occur in different types of components in the circuit. The main overall losses are conducting and switching losses, where the later can be divided into turn on and turn off losses.

2.3.1 Diode Losses

To understand the losses of the diode a simple model is used and can be seen in Figure 2.12. In the model a series resistance and a voltage source is placed in series with an ideal loss less diode. The series resistance illustrates the conduction losses while the voltage source represents the voltage drop across the diode, this is also known as the threshold voltage.

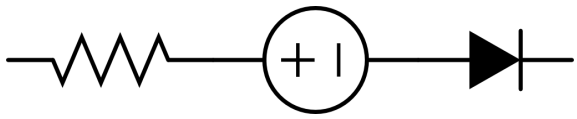


Figure 2.12: Simple model of the diode

The conduction losses for a diode are given by

$$P_{diode} = V_{th} I_{o,avg} + R_d I_{o,rms}^2 \tag{2.18}$$

where V_{th} is the threshold voltage, $I_{o,avg}$ the average output current, R_d the diode dynamic resistance and $I_{o,rms}$ the output RMS current [24].

Reverse recovery of a diode is a short time period where the diode conducts current in the opposite direction during its turn off, due to the removal of minority carriers [25]. This phenomena can be seen in Figure 2.13. The charge Q_{rr} which is the area marked in the figure represents the losses. The amount of charge can approximately be calculated as,

$$Q_{rr} \approx \frac{I_{rr} t_{rr}}{2} \tag{2.19}$$

where I_{rr} is the peak recovery current and t_{rr} is the recovery time. With the charge Q_{rr}, the power losses from the diode reverse recovery current is calculated as,

$$P_{rr} = V_o Q_{rr} f_{sw}. \tag{2.20}$$

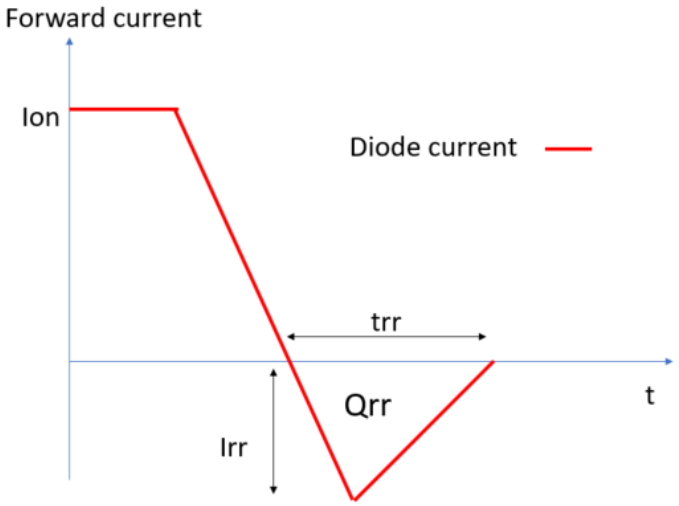


Figure 2.13: Reverse recovery characteristics of a diode

2.3.2 MOSFET Losses

The MOSFET conduction powerloss can be calculated through

$$P_{DS} = R_{DS,ON} I_{DS}^2 \tag{2.21}$$

where P_{DS} is the conduction power loss, $R_{DS,ON}$ is the dynamic series resistance as a, I_{DS} is the drain source current. In reverse direction the forward diode blocks and instead the free wheeling diode can conduct, its power loss can be calculated according to (2.18).

The MOSFET switching losses can be divided into turn on and turn off power losses. The losses are achieved as the drain voltage and the drain current do overlap in the turn on and the turn off process of the device. The worst case of turn on power loss can be calculated through

$$P_{ON} = U_{DS,Peak} I_{DS,Peak} \frac{t_{ri} + t_{fu}}{2} fsw + Q_{rr} U_{DS,Peak} fsw \tag{2.22}$$

where P_{ON} is the turn on switching power loss, $U_{DS,Peak}$ the peak drain-source voltage, $I_{DS,Peak}$ the peak drain-source current, t_{ri} the current rise time and t_{fu} the voltage fall time. The turn off switching power loss can be calculated in a similar manner, but without the reverse recovery term resulting in

$$P_{OFF} = U_{DS,Peak} I_{DS,Peak} \frac{t_{ri} + t_{fu}}{2} fsw \tag{2.23}$$

where P_{OFF} is the turn off power loss.

2.3.3 Transformer Losses

The transformer also contributes to losses in the circuit. The main power losses comes from the conduction losses and the core losses. These losses are represented

in the model with resistances. These can be seen in Figure 2.14. The conduction losses and leakage inductance is represented by R_p, L_p, R_s, and L_s for the primary and secondary side. These losses comes from the resistance of the coil in the windings. With an increase in frequency the conduction losses increases due to the skin and proximity effects.

R_c and L_m represents the iron core and the losses in it. R_c is the conduction losses and L_m is the magnetizing inductance. N1 and N2 are the windings of the transformer, this transformer in the model is an ideal transformer just representing the turns ratio. The losses in the core is called hysteresis losses, the changing magnetic field also causes eddy currents which also contributes to the losses. The winding and core losses are the dominating losses in transformer components.

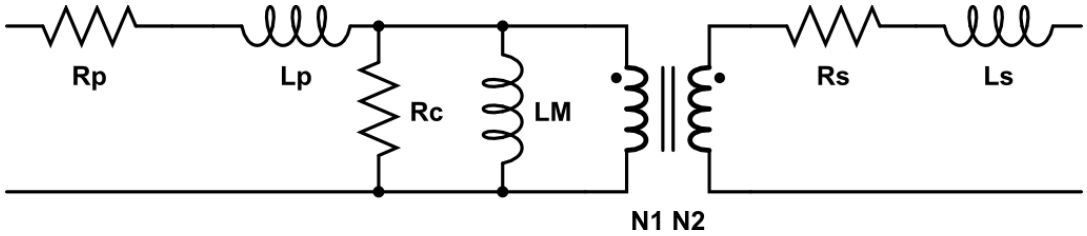


Figure 2.14: Transformer model

For a resonant tank configuration like the LLC which uses two inductors, leakage and magnetizing inductor can be combined in the transformer. The leakage inductance can be changed by changing the distance between windings [24].

2.4 EMI

Disturbances found in a electrical systems can come from the same system or other nearby systems, where the later mentioned is referred to as EMI. The main source of EMI in power converters originates from the switch and transformer. The switching results in ripple currents and also induce currents in stray capacitances. EMI can appear as conducted or radiated disturbances. To keep this disturbance low, electromagnetic compatibility (EMC) standards have been set. EMC is essentially that every circuit in a multi-circuit arrangement should not emit more EMI then the limit and should be able to keep the EMI below the limit. Which means that one circuit should not affect the ones around it.

The voltage disturbance caused by EMI can be divided into 3 general cases.

1. Noise
2. Transients
3. Short-duration impulses superimposed on the mains voltage

EMI can be transmitted through wires (conducted) or through space (radiated). Below 10 MHz the conducted EMI is a lot larger then the radiated. The conducted

EMI appears in 2 forms, common-mode (CM) and differential-mode (DM). [26]

2.4.1 Common and Differential Mode

Common mode noise is conducted to the ground in the circuit through the parasitic capacitances. The main source of CM noise is from the semiconductor switching devices in the converter. The high derivative of the voltage is the main source of the CM current. The total CM current of the converter is defined as

$$i_{cm} = \sum C_{para} \frac{dv}{dt} \tag{2.24}$$

where C_{para} parasitic (stray) capacitances to ground in the circuit from any $\frac{dv}{dt}$ node in the circuit. [27]

Differential mode EMI only flows through the wires of the circuit, between the positive and negative conductor. It can be considered as a circulating current in the circuit. DM noise originates mostly from ripple in the input current of the converter. This is possible to counteract rather easily by having a large input capacitance to lower the input ripple. A consequence of this is that DM noise is mainly present in other parts of the power supply circuit, such as a power factor correction circuit (PFC) before the converter. Consequently the DM noise does not need to be considered when a large input capacitor is present.

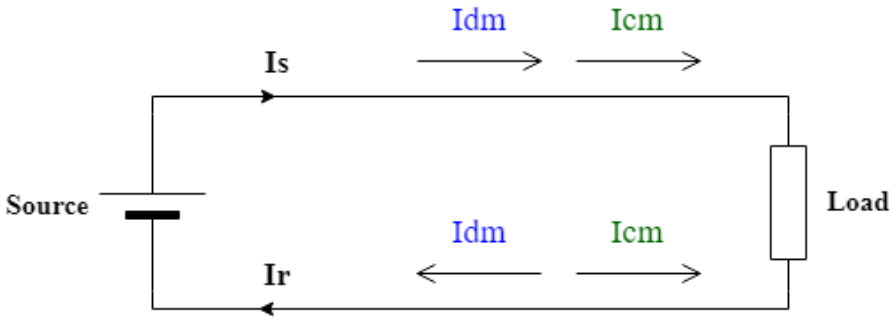


Figure 2.15: Visualization of common and differential mode

Both CM and DM can be seen in Figure 2.15. The most important thing to consider is that CM noise generates an imbalance of the current because of how the noise travels through the circuit, which means that $I_s \neq I_r$. As mentioned above DM can be filtered with a capacitance since the noise travels in the same direction as the current, and in a circuit without CM I_s would be equal to I_r.

For normal operation there are certain standards that must be forfilled. The telecom converters goes under the standard EN 55022 which comes from the CISPR 22 standard. There are 2 limits, one for the average noise and one for quasi peaks [28].

2.5 Cost

The net present worth (NPW) can be calculated according to

$$NPW = \frac{C}{(1+i)^t} - I \tag{2.25}$$

Where C is the cash flow, i is the discount rate, t the economical life length of investment and I the investment cost. The residual value is assumed as zero.

3
Design

The following chapter will include the design procedures and what assumptions where made to achieve the needed simulation result.

3.1 Evaluation

When designing the converter it is important to have an understanding of what is important for the project. The 3 main criteria to be evaluated with the design is how efficient it is, how much EMI can be expected and how much does it cost. This needs to be in relation to the forward converter which is used for the application already.

3.1.1 Converter Specification

The converter specifications that where provided and will be looked at is presented in Table 3.1. The rated output operation point that will be related to is specified as $5.5V$ with $10A$, or in other words, $55W$ of output power. The switching frequency is set to $300kHz$, as the forward converter in operation today.

Table 3.1: Converter specification

Input Voltage	$36 - 60V$
Output Voltage	$5 - 6V$
Output Power	$50 - 60W$

3.1.2 Efficiency

Efficiency is evaluated by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{losses}} \tag{3.1}$$

where P_{out} is the measured output power, P_{in} the measured input power and P_{losses} the estimated power losses. The power losses of the converter is calculated by,

$$P_{losses} = P_{rectifier} + P_{sw} + P_{trafo} + P_{other} \tag{3.2}$$

where $P_{rectifier}$ is the power losses over the rectifying components, P_{sw} is the power losses over the switching components, P_{trafo} is the power loss in the transformer and

P_{other} are the sum of all other small losses found in other non ideal components of the circuit. Depending on if the secondary side of the converter consists of diodes or MOSFET:s the $P_{rectifier}$ will be very different in terms of size. As long as the rectifying side uses the same component (diode or MOSFET) the comparison should still be valid.

Identifying the biggest losses of the circuit is important to see what can be improved. The theory suggests that the resonant converter is better for higher frequencies since the switching losses are lower. Therefore operation points at higher frequencies will also be evaluated.

3.1.3 EMI

When using power converters EMI will be present as a consequence of the fast switching that is done. EMI will be evaluated by comparing the frequency spectrum for the converters. Radiated EMI can't be simulated in the software used.

3.1.4 Cost

The cost will be evaluated by comparing the different converter circuits and look at their differences rather then the individual components. Some of the components will be kept the same for both circuits to be able to give a fair estimate, these components can be seen in section 3.3. Circuits that drive the converters will be assumed to have the same cost.

3.2 Resonant Converter Design

The following section will present the resonant converter considerations made before simulating a preliminary design.

3.2.1 Resonant Converter Choice

As resonant converters are often used for high power ratings a full bridge setup is commonly used. For high primary currents the conduction losses are lower when using four switches compared to two, but on the other hand it is more expensive as there are two extra switches [29]. For medium power range a half bridge can be considered due to the lower cost but also due to higher efficiency's at lower power ratings [30].

The possibility of both step up and down is good taking into account if a converter shall have a wide application range but also galvanic isolation. Topologies such as buck and boost are therefore excluded. Flyback and Forward are relevant alternatives but their high voltage over the switch during turn off, compared with the full- or half bridge, are bad for the switch as well as the EMI performance [30]. For a wide output range one should consider the switch utilization factor, how close in relation input and output voltages are, where the bridge has good performance for

a wide input output relation compared to other mentioned topologies [3]

For the secondary side, a full bridge rectifier or a full wave rectifier can be used. For high voltage ratings it is recommended to use a full bridge as diodes then are exposed for half the voltage but on the other hand one uses two extra diodes [29]. Full wave was chosen for preliminary design, as the voltage rating is low, the number of switches is less and the conduction losses are less as well.

A galvanic isolated half bridge converter is chosen to be investigated.

3.2.2 Resonant Tank Choice

A resonant converter is based on a resonant circuit but also its converter topology. There are several resonant circuits and topologies which could probably achieve the performance needed for the application. The project will look at the most promising topology with regard to what was investigated in Section 1.2 to achieve the best possible result.

The most simple load resonant circuits are SRC and PRC but because of their drawbacks mentioned in Section 2.1.1 it is more suitable to use 3 resonant elements in the circuit. This is called SPRC and combines the most important positive characteristics of the SRC and PRC at the cost of another component. Researches regarding circuits with bigger resonant tanks consisting of 4 or more components do exist [31]. Their biggest advantage is related to bidirectional power transfer and will not be further looked into as scenario given is unidirectional.

Of the three element resonant converters the LLC and LCC resonant circuits are most frequently used, where LLC has shown higher efficiency than LCC in the $100W$ region [8], [12]. LLC uses one less component as inductors can be integrated within the transformer in the form of leakage inductance, but the LLC utilizes 2 capacitors, where an extra capacitor has a cost and size disadvantage [12]. For LCC in high voltage applications there are advantages when using a transformer with high turns ratio which results in high parasitic capacitance in transformer and hence act partly as a resonant component [12]. High turns ratio and high voltage will not be used in this investigation and therefore the LCC benefits are not relevant. LLC is chosen as the resonant circuit to continue investigating, see section 2.1.3.

3.2.3 Resonant Tank Design

From given specification in Table 3.1 combined with (2.9) the preliminary turns ratio was approximated. The turns was rounded off such that a suitable voltage gain interval is received and rated operation as close as possible to the resonance frequency is recommended. The maximum and minimum voltage gain was calculated through (2.10) and (2.11) combined with the maximum and minimum output volt-

ages. Voltage drops assumptions where changed depending on diode and secondary rectifier stage model.

Higher switching frequencies can reduce the size of passive and active components in converter circuits, but on the other hand risk of disturbing telecommunication applications on PCB. The preliminary design considered the 150kHz limit (fundamental) for electrical devices for which EMI laws/tests has to be evaluated for. For a better comparison between HBLLC and existing converter the actual frequency today used was later designed for. The preliminary L_n value was selected following recommendations from [21],[32]. With the proposed L_n value and previous calculated maximum voltage gain, using Figure 2.6 the intersection gave the preliminary quality factor.

Using Figure 2.7 but with specified values of maximum and minimum voltage gain, a new quality factor can be chosen such that the output load requirments are achievable. In Figure 3.1 the maximum voltage gain vs normalized frequency characteristic are visualized. The red curve shows how the designed converter can vary between M_{gmax} and M_{gmin} by varying the frequency within the normalized frequency interval of fnmin and fnmax, for the maximum load. The component values of resonant tank was calculated by using (2.1), (2.2), (2.4) and (2.6). An easy verification of C_r and L_r values calculated is to recalculate the qualitiy factor and resonance frequency with the calculated C_r and L_r values.

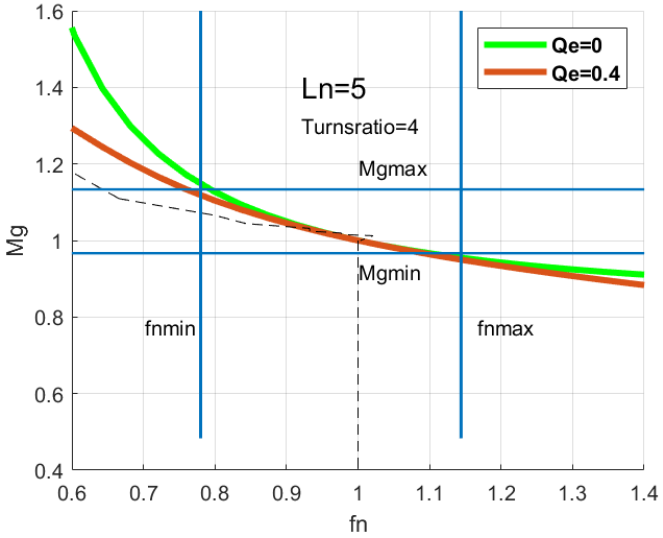


Figure 3.1: Preliminary resonant tank design

The final resonant tank design was made considering both input and output variations, resulting in a wider voltage gain interval and therefore a smaller L_n value was used such that approximately the same frequency interval could be used as previous design. Compared to the preliminary resonant tank design, the final considers the turns ratio on todays transformer.

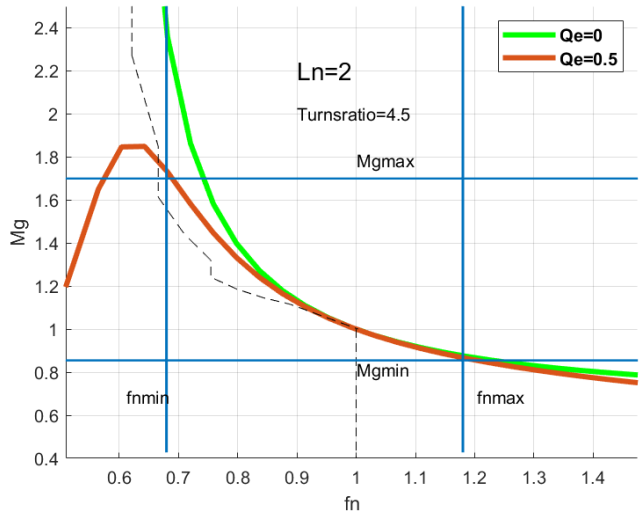


Figure 3.2: Final resonant tank design

3.3 Circuit Components

Components that are present in both converters are approximated to be the same. This is to make the comparison as fair as possible and see what difference the different topology makes rather than the complete design. Small variations in components exists due to the resonant tank elements.

3.3.1 Transformer

The transformer used in the simulation is based on measurements and data sheets of the one used on the forward converter used for the operation today. The implemented values are presented in Table 3.2. These values are not the same for the resonant converter since the open circuit inductance and leakage inductance is customized to fit the LLC setup. The turns ratio was changed for the version of the circuit which utilizes rectifying diodes. The turns ratio was then changed to approximately 4:1. This was done order to compensate for the voltage drop over the diodes. The values in the table are measured at 100kHz, which means that physically they will most probably change when increasing the frequency of the circuit.

Table 3.2: Transformer data

Characteristic	Value	Unit
Turns ratio	4.5:1	
Open Circuit Inductance	255	μH
Leakage Inductance	350	nH
Primary Series Resistance	45	mΩ
Secondary Series Resistance	2.4	mΩ
Capacitance	450	pF

3.3.2 Equivalent Series Resistance

A big advantage of an LLC resonant tank is to remove switching losses and the disadvantage is the extra conduction losses that the LLC stage produces. The equivalent resistance values of L_M was chosen as DC resistance value from the existing used transformer, see Table 3.2. The value for L_r was decided from an inductor with similar inductance and rating needed for scenario. The equivalent resistance for inductors has a small frequency dependence from the skin effect and proximity dependence that is small and ignored.

The equivalent resistance value for C_r was chosen by finding a capacitor with appropriate capacitance value and rating for the scenario. The equivalent resistance value for C_r is frequency dependent, a characteristic that is assumed handled by LTspice. The equivalent resistance is reduced with higher frequencies, a property that should benify higher frequency designs. The output capacitors values were choosen from the todays used forward converter solution.

Table 3.3: Additional ESR data

ESR	Value	Unit
C_r	50	mΩ
L_r	5	mΩ
C_{out}	15	mΩ

3.3.3 Output Capacitor

The output capacitor was picked to match the values of the physical one that is in the converter used in the application today. This decision was made to make the results more comparable instead of designing a new capacitor for the resonant converter. Dimensioning after hold up time was ignored due to only investigating steady state behavior of circuit.

3.3.4 Input Capacitor

The input capacitors are assumed to be large, to remove the input current ripple and therefore the DM currents of the EMI can be neglected, see section 2.4. In other words is the input voltage source plus the input capacitors belonging to the earlier converter stage and are therefore not explicitly investigated in this report.

3.3.5 MOSFET

The switches used are MOSFETs, due their suitability for high frequency applications and commonly used for switch mode power supply applications. The primary and secondary side switches for the HBLLC will use the same MOSFETs as the forward converter solution, BSZ0902NS. The MOSFET in question has a combination of low $R_{DS,ON}$ and Q_g, total gate charge, compared to many other MOSFETs in the LTspice library for similar voltage ratings. Low $R_{DS,ON}$ is very important for the

application as the duty cycle is almost 50%, Low Q_g value is important for a fast discharge of the MOSFET drain source capacitors, much related to dead time and to achieve ZVS.

Table 3.4: Relevant MOSFET data BSZ0902NS

Parameter	Value	Unit
R_{dson}	3.5	mΩ
Q_g	26	nC
C_{oss}	600	pF
t_{don}	4.2	ns
t_r	5.2	ns
t_{don}	21	ns
t_f	3.6	ns

4

Circuit Verification

This chapter explains the verification process of the circuits before collecting specific results. The chapter also presents some of the specific characteristics and behaviors of the two converters.

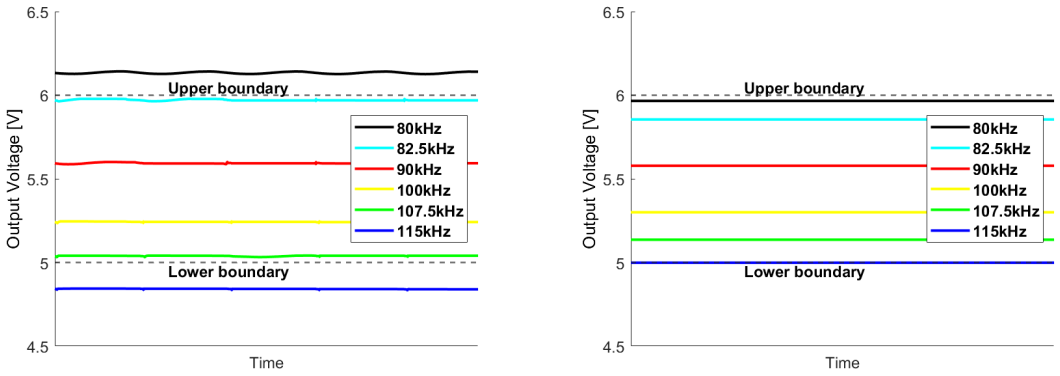
4.1 Base Simulations

An electrical model is built to be able to simulate the resonant converter and evaluate the criteria given in Section 1.3. The model is built in LTspice since its a powerful simulation tool for electrical circuits and easy to handle. The LTspice model of the preliminary converter was built according to Figure 2.3. The preliminary circuit behavior and design was evaluated through approaches explained in coming subsections, all considering the preliminary tank design.

4.1.1 Output Behaviour

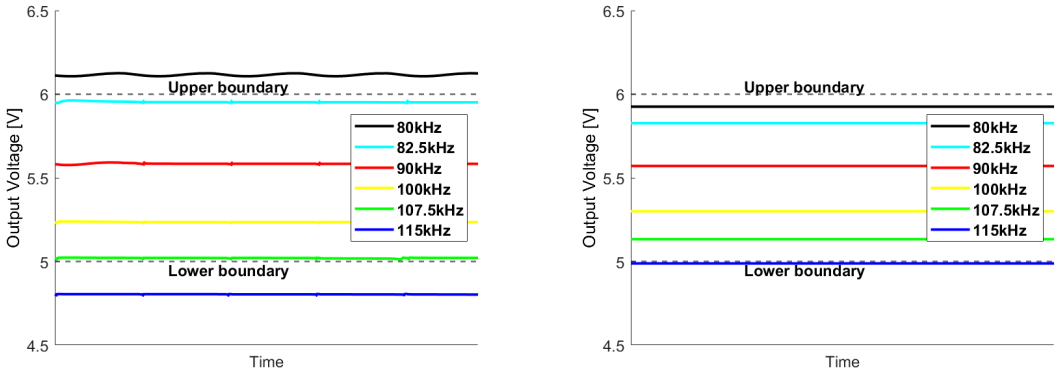
To verify that the simulated converter could achieve the specifications from Table 3.1, the output voltage for a certain power level and at different switching frequencies were plotted. The design can regulate the output voltage by varying the switching frequency. The basic waveforms that were expected was achieved, with similar behavior as shown in Figures 2.4a, 2.4b and 2.4c. The simulations were done with a constant power load such that the power of 50 and 60 W was constantly drawn from converter circuit.

The converter can achieve the upper and lower power limit and vary the voltage within the specified voltage interval. From Figure 4.1a the frequency interval is around 82.5 to 107.5kHz, and the frequencies 80 and 115kHz are outside the voltage interval. For the calculated design shown in Figure 4.1b, the frequencies 80 kHz and 115 kHz are within the voltage interval. The behavior between a DC transient analysis vs a steady state AC analysis using the first harmonic simplification is not the same. The results between simulated and calculated values vary more as the switching frequency differentiates more from the resonance frequency. The conclusion is that for the same voltage gain interval the simulated characteristics requires a lesser frequency interval compared to the calculated.



(a) Simulated **(b)** Calculated

Figure 4.1: Simulated and calculated output voltage, 50W



(a) Simulated **(b)** Calculated

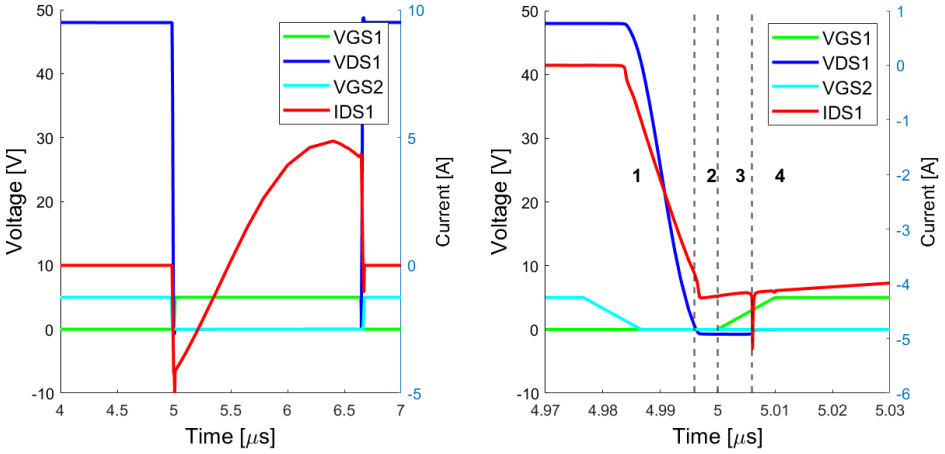
Figure 4.2: Simulated and calculated output voltage, 60W

4.1.2 Zero Voltage Switching

An important criteria and one of the main goals with resonant converters is achieving ZVS, see Section 2.1.2, to reduce the voltage stress for switch during turn on. The requirement was checked in two ways, from theoretical equations and from simulations. Equation (2.12) and (2.13) were evaluated with the preliminary design values where big margins existed. The resonance capacitance was much greater than the equivalent capacitance of the MOSFETs and in that way (2.14) was full filled. For verifying ZVS from simulations, the turn on behavior of the switch was checked for the minimum, resonance and the maximum switching frequencies such that the drain source voltage had reached to zero before gate source voltage was applied.

In Figure 4.3 the most important waveforms of one MOSFET are visualized during one period together with a zoom of the turn on process, for $f_{sw} = f_0$ and rated load. The turn on behavior can be divided into four intervals, where the MOSFETs behavior will be different for each of them. During the first interval, the drain source

voltage, $VDS1$, is positive and the drain source current ,$IDS1$, is negative. The current is in other words going through the anti parallel body diode. This will continue until $VDS1$ drops below zero. For the second interval $VDS1$ is negative due to the body diode voltage drop and a power dissipation occurs. The gate source voltage, $VGS1$, has not been applied and the MOSFET is not conducting. In the third interval, $VGS1$ is applied and the MOSFET is turned on but there is still a negative current, hence both the MOSFET and the body diode are able to conduct. In the fourth interval the MOSFET conducts and the body diode is reversed biased.



(a) MOSFET period overview **(b)** MOSFET turn on zoom

Figure 4.3: Primary side MOSFET waveforms overview and turn on waveforms for ZVS condition

4.1.3 Power Losses

For assuring simulation quality and understanding of the model behavior the different losses in circuit were estimated and calculated. The most important losses for a HBLLC are the conduction losses of the rectifying diodes and the switching losses of the MOSFETs [9]. The conduction loss in the secondary side rectifying diodes were estimated by (2.18) using the existing converters MOSFET $R_{ds,on}$ value. The difference between the LTspice model loss compared to (2.18) were close, verifying the understanding of the model behavior.

The MOSFETs drain source losses were split into turn on, turn off and conduction losses for being able to evaluate its loss behavior for different frequencies and loads. The turn off loss were estimated through (2.23) which matched simulation results well. The turn on loss was calculated as the average power dissipation over the intervals 2 and 3 in Figure 4.3. Considering interval 1 aswell, the power loss would be negative as the turnoff loss associated with the switch turning off is considered (which will look like generated power in the perspective of the switch about to turn on). The assumption can be verified where the power loss during turn off is identical in appearance and quantity to the one appearing during interval 1.

The power losses were calculated for different frequencies and loads, where the general behavior followed the characteristics that were expected. Using (3.1) the LTspice measured input and output powers could be compared to the estimation of losses, where the resulting efficiency's were similar.

4.2 Rectifying MOSFET implementation

For making a more realistic model of the converter scenario the rectifying diodes were aimed to be replaced with MOSFETs. The implementation for this investigation was important in many aspects.

- Firstly, implementing a MOSFET rectifying stage for lowering the secondary side conduction losses, the largest power loss in circuit.
- Secondly, verifying and implementing soft switching on the secondary side of the circuit, a result from the primary side ZVS behavior [24], much relevant both in efficiency and EMI perspectives.

From many unsuccessful tries of active rectification two conclusions where drawn. First, the secondary side circuit, see Figure 2.3, must be changed such that the body diode does not conduct when the output capacitor voltage is higher than the transformer voltage. This is a problem as the body diode will conduct the current in opposite direction as from what is preferred. To prevent this, switches and respective connections where placed according to Figure 4.4, such that the MOSFETs source pin is connected to ground.

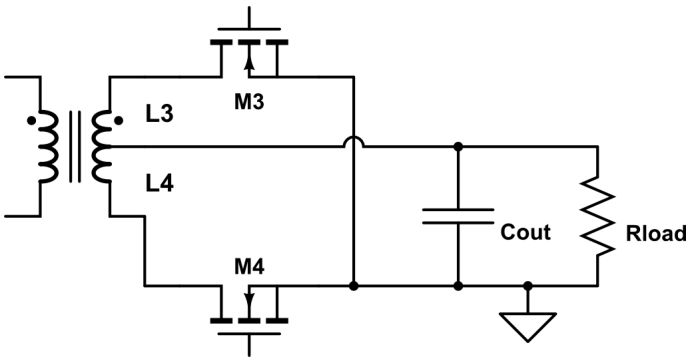


Figure 4.4: Secondary circuit configurations with rectifying MOSFETs

The second conclusion was related to the secondary gate signals which carefully must be designed for creating a model that should be valid for more than one specific scenario. To summarize, the basic idea was to receive the secondary side current waveforms seen in Figure 2.4. The control has in simulation not used an all ready made drive circuit. Instead a voltage source for each switch has been used, yielding that settings have been costumed made for rectifying switches. The most important problems mentioning were due to

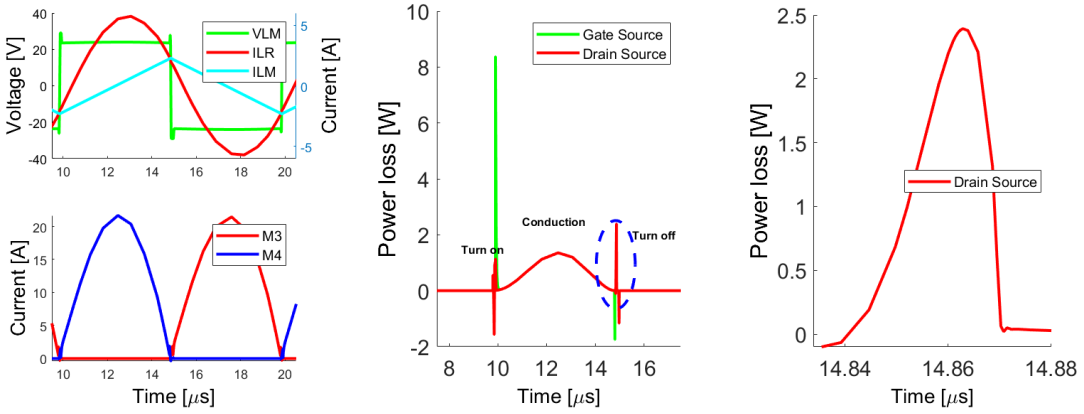
- Dead time between the four switches, where the solution was to use time dependent variables and carefully draw the waveforms with focus on whats

happening between the time of the primary first and second MOSFET gate signals.
- Phase shift between primary and secondary side gate signals, which is dependent on the frequency scenario. The solution was to use three different gate signal settings, one for each of the three frequency scenarios.
- For frequencies where $f_{sw} \neq f_0$ the gate signals need to be adapted depending on how far the switching frequency is from the resonance frequency. The solution was to create frequency dependent linearly terms compensating the gate signals.

4.2.1 Verification MOSFET implementation

The most important primary and secondary side waveforms for the rectifying MOSFET implementation, for rated load and operated at resonance frequency, are seen in Figure 4.5. The primary side transfomer waveforms and the secondary side currents waveforms in Figure 4.5a are close to the ideal case, see Figure 2.4a.

In Figure 4.5b one of the rectifying MOSFETs power loss is visualized during turn on, conduction and turn off. The drain source power loss spike is usually the dominating one during turn on but is small compared to the gate source spike. By zooming in on the positive turn off spike, see Figure 4.5c and estimating the power loss as one triangle, the turn off loss over period could be estimated. The loss for this frequency would be close to 7.2mW, which is close to negligible in the context. This means that the MOSFET is utilizing soft switching.

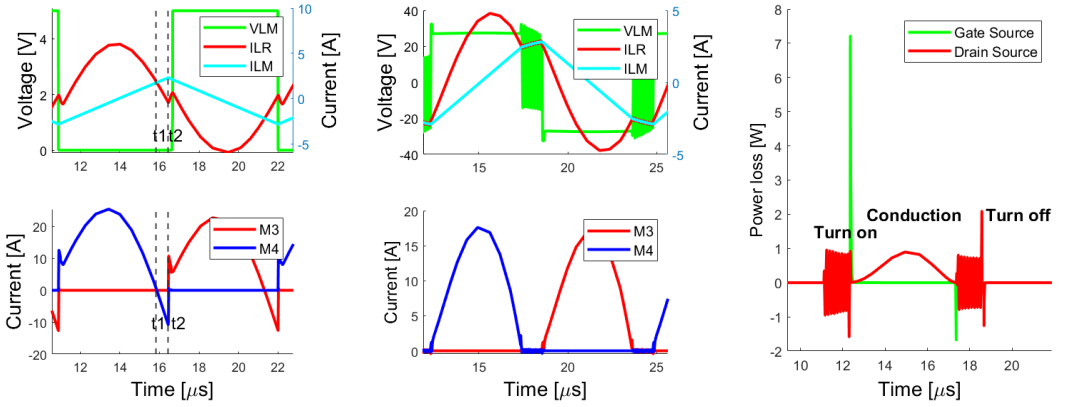


(a) Waveforms **(b)** MOSFET loss **(c)** Turnoff loss zoom

Figure 4.5: Rectifying MOSFET waveforms operated at resonance frequency

In Figure 4.6 the most important waveforms concerning the primary and secondary sides of circuit are shown lowering the switching frequency. The behavior of the secondary side current is not ideal, see Figure 4.6a. The timing of the secondary MOSFET is switching at the time t_2 when it should switch at the time t_1, the time instance where I_{LM} and I_{LR} becomes equal.

By creating a frequency dependent variable the control settings can be adjusted to be used for frequencies lesser than resonance frequency as well, yielding results of Figure 4.6b. When I_{LM} and I_{LR} become equal the power transfer stops where L_M will go from a scenario of being shunted to the reflected load R_e to a no shunt scenario. The sudden circuit change will make L_M participate in the resonance and its voltage V_{LM} oscillate. The high frequent oscillations in the transformer voltage can have an impact from an EMI perspective. From Figure 4.6c the secondary side MOSFET still achieves soft switching, which is expected for operation below resonance frequency.



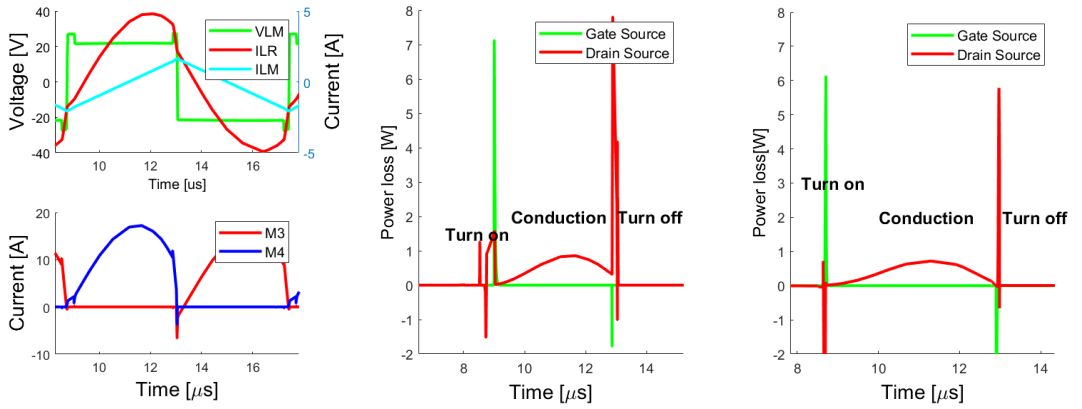
(a) Unsuccessful waveforms

(b) Successful waveforms

(c) Succesful MOSFET loss

Figure 4.6: Rectifying MOSFET waveforms operated below resonance frequency

In Figure 4.7 the primary side waveforms are close to the ideal case for switching frequency greater than resonance, but the secondary current is not perfectly switched. In Figure 4.7b, a small loss area can be seen at turn on, a consequence from the body diode conducting, something that is happening during turn off as well. With better settings of the MOSFET gate signal the body diode conduction loss can be reduced, see Figure 4.7c. The amplitude of the drain source power loss during turnoff loss is higher in than previous two frequency scenario, but for frequencies above resonance the reverse recovery losses is expected to exists, see Section 2.1.3.



(a) Unsuccessful waveforms

(b) Unsuccessful MOSFET loss

(c) Successful MOSFET loss

Figure 4.7: Rectifying MOSFET waveforms operated above resonance frequency

The expected waveforms and behaviors for the rectifying implementation is achieved for the different frequencies. The rectifying switching losses are close to zero. The conduction through the body diode and the gate signal settings are both playing a crucial part for the difference in behavior between simulations and theory. The switching losses are insignificant compared to the conduction losses, at least for the frequencies used for the base simulation, but they do not equal zero.

4.3 Factors that affect Zero Voltage Switching

To be able to keep the efficiency of the converter ZVS needs to be achieved during the whole working range of the converter. The switching losses will increase substantially if ZVS is lost and there are factors which affects this.

4.3.1 Dead Time

The most important factor for achieving ZVS is sufficient dead time. If increasing the switching frequency a sufficient dead time must exist between the switches on both primary and secondary side gate signals such that a short circuit does not appear. For higher frequencies the complete time period will be smaller but the dead time should remain approximately constant. A non sufficient dead time will create a short circuit and a too large dead time will create extra conduction loss, see Figure 4.3. The minimal dead time can be calculated from the MOSFETs specifications shown in Table 3.4. The deadtime used was two times the minimal, yielding a safe margin from ZCS.

Of the three frequency cases, see Section 2.1.3, for switching frequency equals or above resonance the current on secondary side of circuit is always conducting. A dead time for secondary switches is still needed, creating a gap where the body diodes will conduct instead. The relation between frequency, gate drive and dead

time are important for assuring as little body diode conduction as possible since that is where the greater losses appear.

4.3.2 Transformer Capacitance

Besides sufficient MOSFET dead time, the ZVS condition is dependent on how fast the MOSFET drain source capacitors can be discharged, which is affected by stray capacitance in the circuit. The transformer has a stray capacitance which now shall be considered in an independent investigation, by inserting C_{stray} from the primary side to the secondary side center tap, see Figure 4.8. The transformer used for the forward converter solution is not center tapped, which the transformer needs to be for the full wave implementation. An assumption is therefore made that the size of C_{stray} is the same between a center tapped vs a non center tapped configuration.

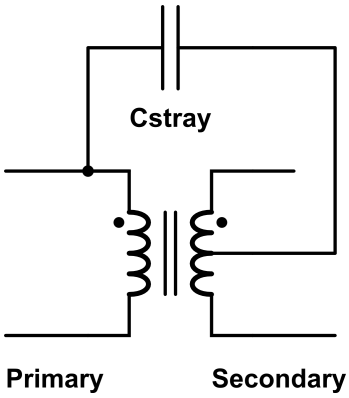
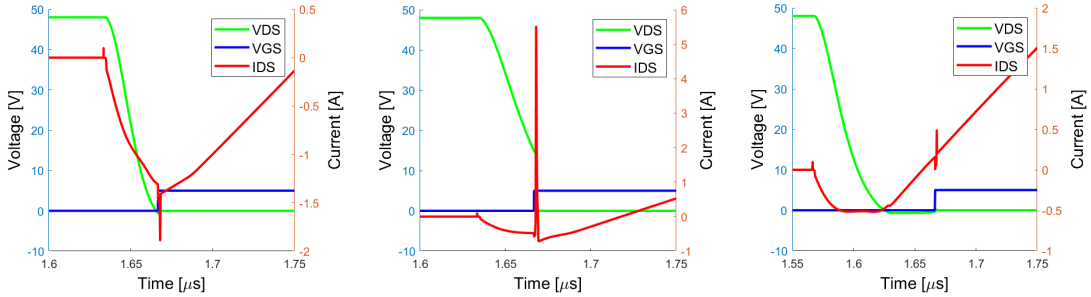


Figure 4.8: Configuration of added transformer stray capacitance C_{stray}

For the preliminary design using 600kHz switching frequency, see Figure 3.1, one of the primary MOSFETs turn on waveforms are shown for three scenarios in Figure 4.9. In Figure 4.9a the drain source voltage falls to zero just before the gate source voltage starts, where the operation is very close to the boundary of ZVS and ZCS. Adding the transformer stray capacitance in the circuit, the drain source voltage fall time is increased and ZVS is not achieved, see Figure 4.9b. ZCS is achieved instead, easy recognized by its current spike which is a consequence of operating in this region, see Section 2.1.6. To still achieve ZVS a longer dead time is needed such that the drain source voltage receives a longer time margin to fall from its peak to its zero value before the gate source voltage is applied. This can be observed in Figure 4.9c where the dead time has been increased.



(a) Original **(b)** Added C_{stray} **(c)** Increased deadtime

Figure 4.9: Achieving ZVS with a stray capacitance

The scenario of adding transformer capacitance can be evaluated by equations as well, using variables and assumptions from Table 4.1 combined with (2.12) and (2.13), giving the results of achieving ZVS or not according to Table 4.2.

Table 4.1: Conditions used for evaluating

Variable	Assumption
L_m,L_n,n,V_{in},Im_{peak},f_{sw}	Preliminary design 600kHz
C_{ds}	C_{oss} MOSFET data
C_{stray}	Transformer data
Deadtime	33ns and 100ns

The results differ for the original scenario, where from simulation its expected that both energy and dead time conditions are full filled, which they are not from (2.12) and (2.13). As ZVS is very close to not be achieved, the mismatch between simulation and calculations is not considered as a problem. One reason for the mismatch could be related to the equivalent capacitance, where perhaps the C_{oss} in LTspice simulation is not the same as the C_{oss} typical value from the MOSFET data sheet. For the other two cases, C_{stray} added and increased dead time, simulations and calculated results match.

Table 4.2: Calculated results of achieving ZVS or not

Case	Energy	Dead time
Original	OK	Fail
C_{stray} Added	OK	Fail
Increased dead time	OK	OK

Adding stray capacitance increases the MOSFET drain source voltage fall time and as a consequence the dead time must be increased to satisfy the ZVS conditions. The match between the theoretical equations and the simulation results is satisfactory. As the stray capacitance in the circuit is frequency dependent, but with an unknown behavior it is hard to in a realistic way, implement the component and knowing how

to select the dead time for different frequencies. The C_{stray} used was measured for a certain frequency, see Section 3.2 and how realistic it is using this value for higher frequencies is much uncertain, therefore C_{stray} is not further evaluated in report.

4.4 Existing Active-clamped forward converter

To compare the results of the resonance converter, a forward converter with active clamp is also implemented in LTspice. This is the type of converter that is used for the telecom application now. The converter is presented in Figure 2.10. It works just like an ordinary forward converter but with an active clamp which transfers the energy from the magnetizing inductance (LM) to the capacitor (C_{clamp}) during the off time. This increases the efficiency of the converter since some of the otherwise lost energy is stored and reused. The converter also has a RC-snubber on the secondary side of the transformer. This was decided to be left in the circuit since the comparison should be as fair as possible against the converter that is used in the physical applications.

The forward converter constructed in LTspice is a simpler version of the real converter. The converter is verified by comparing it with measured values from the real converter. The simulated converter matches the measured values well enough to be able to draw conclusions. The simulated version does have a slightly higher efficiency than the real one, this is probably a consequence of not having the driving circuit drawing any power and some parasitic elements are not present in the LTspice model. The comparison with the resonant converter should still be valid since it is also simulated.

4.4.1 Basic Waveforms

The forward converter used in the application today is rated with an output voltage of $5.5V$ and an output current of $10A$, which is $55W$. The waveforms from simulated version used in this project is shown in Figure 4.10. It can be observed that the output power in the simulation for the rated operation is $55W$ just as expected with very low ripple. The primary side of the transformer has some ripple when the switch turns on and off, this is a direct consequence of the transformer parameters, in particular the leakage inductance and open circuit inductance from Table 3.2 [33]. The inductor current is from the secondary side inductor. The converter is operating in CCM since the inductor current is always > 0.

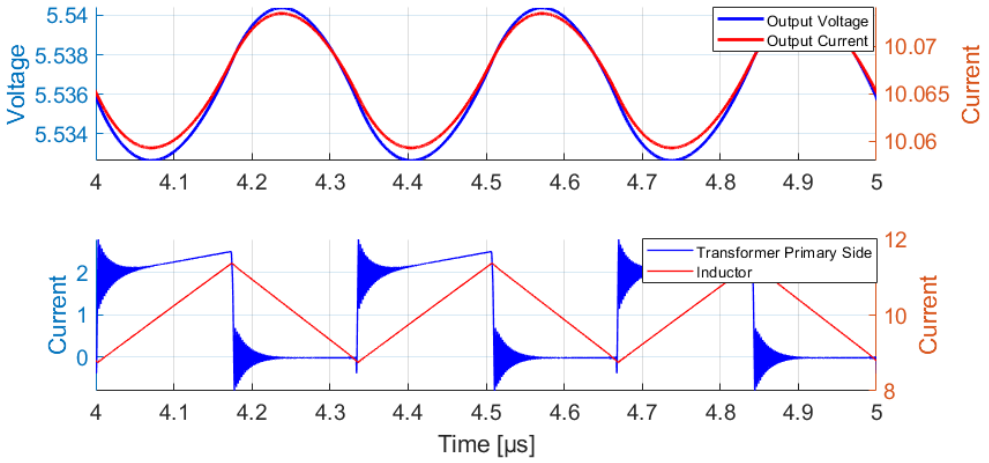


Figure 4.10: Forward converter waveforms

5
Efficiency

The most important factor of the converter is the efficiency. Without a good efficiency the converter would not be usefull. The efficiency for the converters will be presented for different input and output voltages, different frequencies and the most importantly losses will be visualized.

5.1 Input Voltage Variations

When the input voltage varies the converters must be able to keep the voltage at a correct level by adjusting the duty cycle for the forward converter and by adjusting the frequency for the resonant converter. Table 5.1 shows how the forward converter can adjust to input and output variations by changing its duty cycle during the operation. The efficiency is kept high at all 3 input voltages. It can reach the output power needed with any configuration of possible input voltages that can occur.

Table 5.2 shows how the resonant converter converter can adjust to input and output variations by changing its frequency during the operation. Compared to Table 5.1, Table 5.2 shows a higher efficiency for 4 out of 5 cases but in general the results are very similar in efficiency.

Table 5.1: Performance during input voltage variations for the forward converter

Input Voltage	Output Voltage	Duty Cycle	Output Power	Efficiency
36V	5.5V	73%	55W	93.2%
48V	5.5V	54%	55W	95.4%
60V	5.5V	43%	55W	95.75%
36V	6V	79%	60W	91.8%
60V	5V	39%	50W	95.7%

Table 5.2: Performance during input voltage variations for the HBLLC

Input Voltage	Output Voltage	Frequency	Output Power	Efficiency
36V	5.5V	240kHz	55W	93.82%
48V	5.5V	282kHz	55W	95.32%
60V	5.5V	354kHz	55W	96.55%
36V	6V	230kHz	60W	93.74%
60V	5V	390kHz	50W	95.52%

5.2 Efficiency at 300 kHz

The forward converter is switching with 300kHz and to get a valid comparison the resonance frequency of the HBLLC circuit is set to 300kHz.

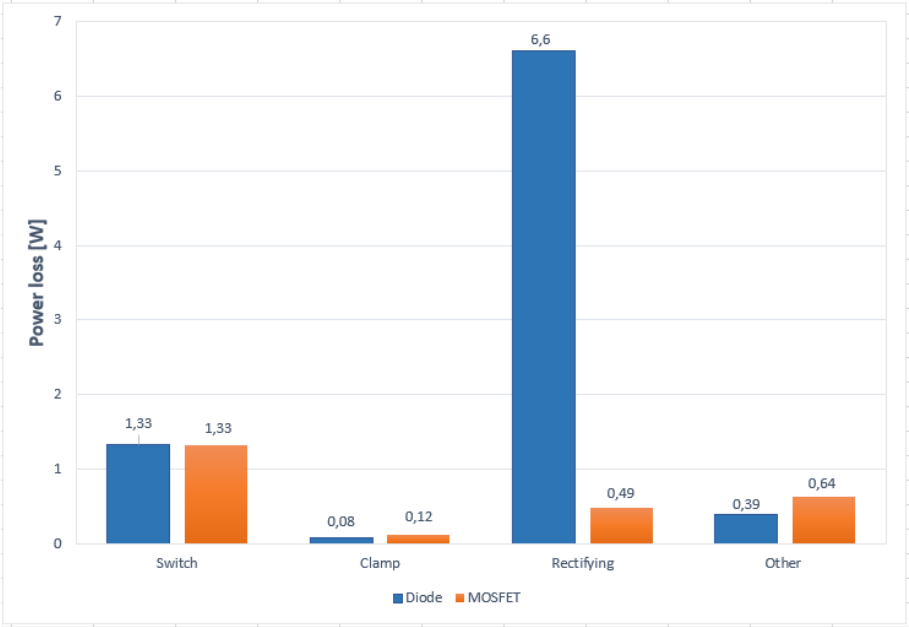


Figure 5.1: Forward Converter Losses

In Figure 5.1 the losses for different rectifying circuits are displayed for 55W output power of the forward converter. The blue stacks are for the diode rectifier while the orange stacks are for the MOSFET rectifier. The stack named "other" represents transformer and output capacitance losses. It can be observed that the rectifying diodes contributes with the largest losses. The most interesting result is that the primary switch contributes with the second most losses. This can be compared Figure 5.2, where the primary switching losses are considerably lower. Another interesting result is that the rectifying MOSFETs loss for both the circuits are approximately the same at 300kHz.

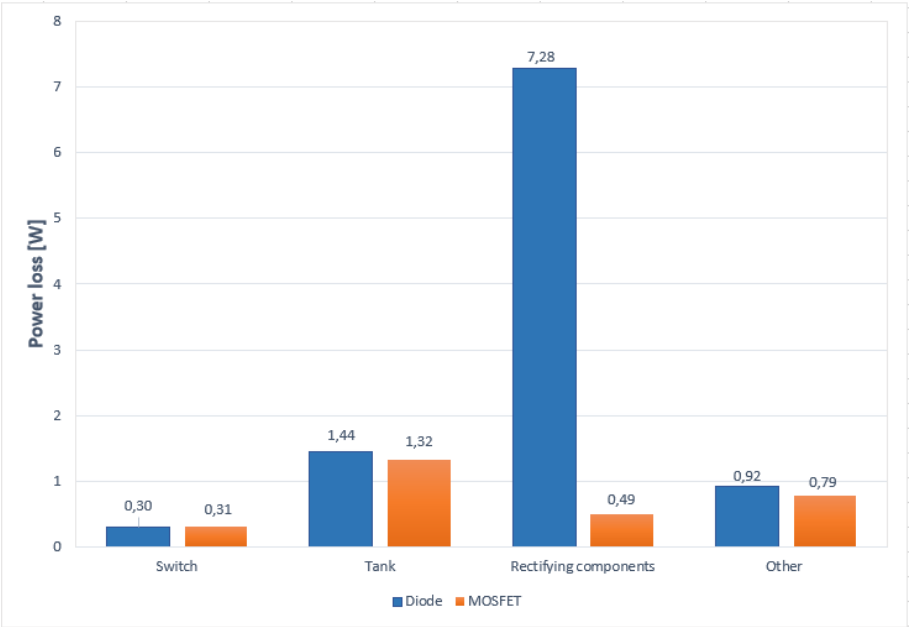


Figure 5.2: HBLLC Converter losses

The efficiency for the converters at the rated operation point is presented in Table 5.3. The forward converter converter shows higher efficiency at the operation point for both a diode and MOSFET rectifier.

Table 5.3: Efficiency for converters at rated load, 300kHz design

Rectifier	Forward converter [%]	HBLLC [%]
Diode	85.6	84.1
MOSFET	95.4	95.3

Table 5.4 presents the switch losses for the resonant converter, both primary and secondary side for rated load and a switching frequency lower than the resonance frequency. The turn on loss is not zero, due to body diode conduction, see Section 4.1.3. Conduction and turnoff loss quantities are as expected. On the secondary side, conduction losses should be the dominating and switching losses close to zero. The switching loss during turn off is not equal to zero due to a small spike, similar as in Figure 4.6. Also small body diode conduction exists due to non perfect switching, affecting turn on and turn off. The results are fine for a functional circuit but improvements can be done, see Section 9.2.

Table 5.4: Breakdown switch losses at rated load and $f_{sw} < f_0$

	Turn ON [mW]	Conduction[mW]	Turn off [mW]
Primary side	35	50	222
Secondary side	26	427	30

Table 5.5 presents the tank losses for the MOSFET implementation at rated load and switching frequency lower than resonance. As expected the resonant capacitor

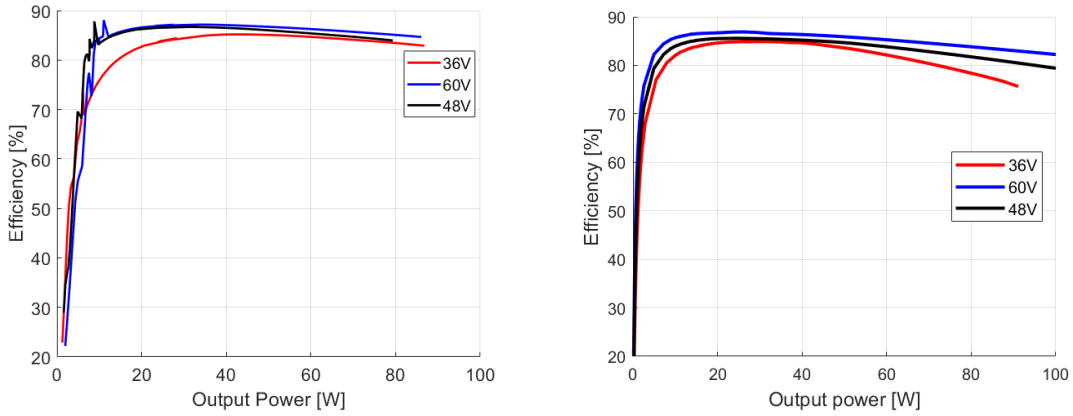
contributes to the majority of loss. For the same equivalent resistance value of C_r and L_m the power loss in the capacitor will always be greater for all loads as the RMS magnetizing current always will be lesser than the RMS current going through the capacitor.

Table 5.5: Breakdown of tank loss at rated load and $f_{sw} < f_0$

	Cr [mW]	Lr [mW]	Lm [mW]
Power loss	822	82.2	420

5.2.1 Load Variations

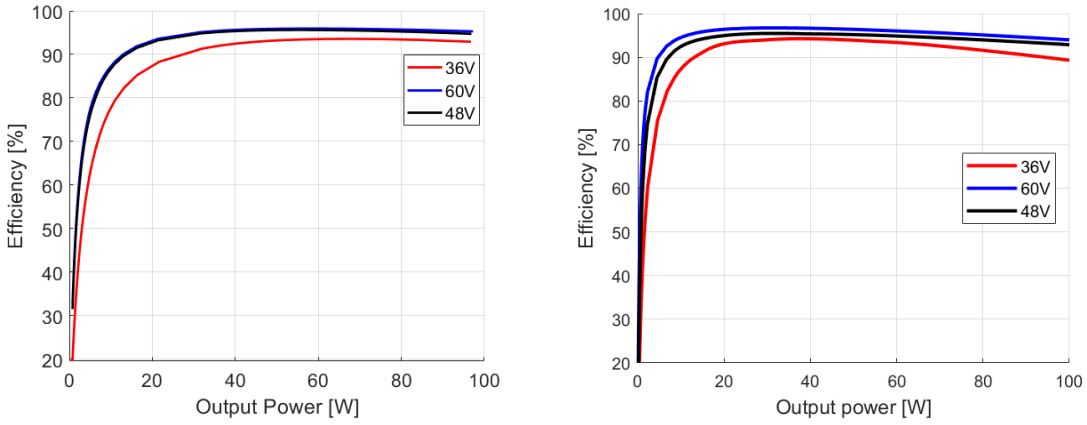
This section will investigate the efficiency for different loads at 3 cases of input voltages with either the diode or MOSFET rectifier. The forward converter is simulated with the input voltages and corresponding duty cycle from Table 5.1 at the 55W operation point. The resonant converter is respectively simulated at the input voltages and frequency from Table 5.2 at the 55W operation point.



(a) Forward Converter **(b)** Resonant Converter

Figure 5.3: Efficiency with a diode rectifier at 300 kHz

From Figure 5.3 it can be observed that the resonant converter is better for power levels lower then the rated operation. This is due to that the switching losses is the largest loss in percentage, and is kept the same when the output power decreases since the frequency is still the same. At higher power than 60W the efficiency for the resonant converter is lower where the conduction loss is the higher loss. The resonant converter has a longer on time and it has 2 primary switches which conduct approximately half of the period each while the forward only has 1. The reason for the 36V input dropping in efficiency for higher loads is due high conduction loss, where the output voltage can not for the simulated frequency stay above 5V for powers above 80W, yielding extra high current. For powers below 25W the 36V scenario cannot keep the voltage below 6V. In a more realistic efficiency sweep the frequency should be changed for each operating point. This is related to control aspects which are not considered.



(a) Forward Converter **(b)** Resonant Converter

Figure 5.4: Efficiency with a MOSFET rectifier at 300 kHz

Figure 5.4 shows approximate the same result as Figure 5.3 but with an overall increase in efficiency over the whole load spectrum. The resonant converter is still better at lower power but is much closer to the forward at the power levels above rated power. In both figures it can be seen in the case of a 36V input, the efficiency is affected negatively. The overall effect of voltage variation over the whole load spectrum has a lower impact on the resonant converter in relation to the forward converter.

What is not considered though is the power loss of driving the circuit, which for the forward converter is adjusting the duty cycle at a given frequency and for the resonant converter its needed to adjust the frequency. The frequency variation depending on input voltage, shown in Table 5.2, is quite large and could need a more complex controller and comparison circuit. This is neglected for both circuits in the figures but when implemented it might have an undesirable effect on the expected result.

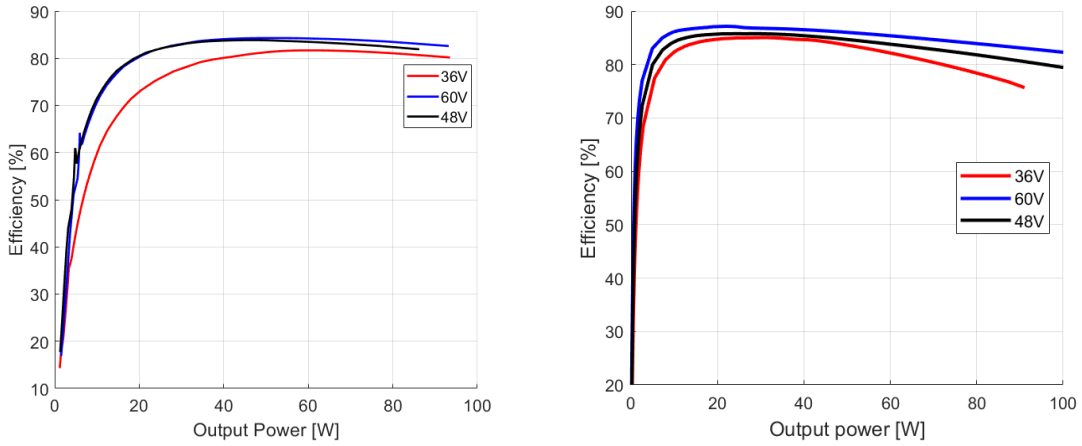
5.3 Efficiency at 600 kHz

When the switching frequency of both the circuits is twice as high, the results are getting more interesting. In Table 5.6 it can be observed that the efficiency is not the same as in Table 5.3. Compared to the 300kHz design, where the forward converter showed better results, for the 600kHz case the HBLLC shows a very small change in loss and shows more promising result than the forward converter. The efficiency of the forward converter is lower mostly because of the increased switching losses of the primary switch while the switching losses for the resonant converter is approximately the same.

Table 5.6: Efficiency for the converters at rated load, 600 kHz design

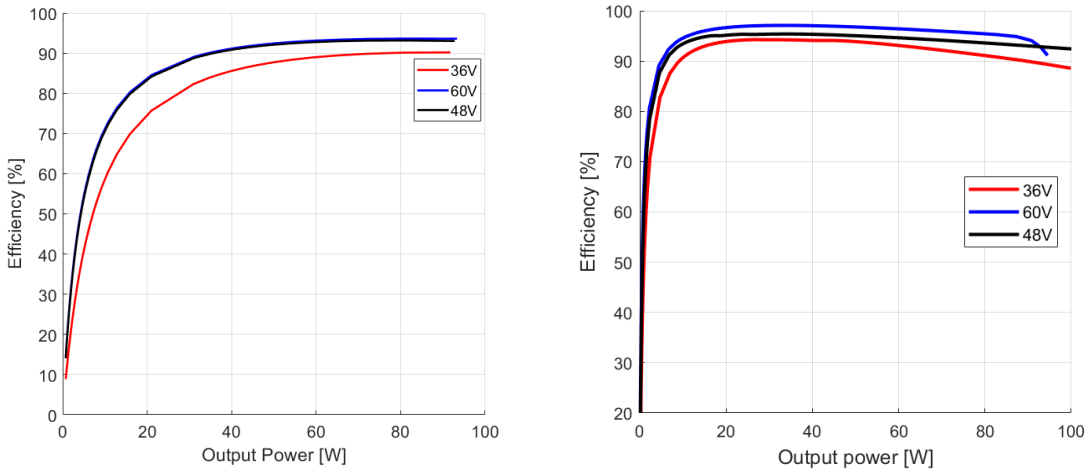
Rectifier	Forward converter [%]	HBLLC [%]
Diode	83.6	84.0
MOSFET	92.1	94.7

At 600 kHz the same scenario for efficiency graphs are presented as in Section 5.2. Besides from the less noise in Figure 5.5a then in Figure 5.3a there are not a lot of differences. The most important thing though, is that the forward converter requires more power to get up to approximately the same efficiency as the HBLLC. This is due to the increasing switching losses, which is an even bigger percentage of the total losses at 600 kHz.



(a) Forward Converter **(b)** Resonant Converter

Figure 5.5: Efficiency with a schottky diode rectifier 600 kHz



(a) Forward Converter **(b)** Resonant Converter

Figure 5.6: Efficiency with a MOSFET rectifier 600 kHz

The resonant converter efficiency curves in this section is almost identical to the ones in Section 5.2. What's interesting is that even at twice the original frequency, the converter is still as efficient over the whole spectrum. This phenomena is due to the ZVS, which means that the frequency of the switching is not important since the losses are so low. Assuming that the resonant tank is being redesigned for the HBLLC circuit for every new resonance frequency to keep it working properly. By doing this it could have an effect on the overall result since the forward converter is kept the same with an increased frequency and adjusted duty cycle. The forward converter might have performed better if it also where redesigned for the new frequency.

These results lead to increasing the frequency even further to see what it does and what further conclusions could be taken. This can be read about in Chapter 7.

6
Electromagnetic Interference

Results regarding EMI and how it was measured is displayed in the following chapter. Everything is analyzed from simulation and no results are measured on an actual circuit.

6.1 Input Filter

When performing the EMI simulations an input filter was implemented to the converter to achieve better results. The input filter can be seen in Figure 6.1 and it consists of a CM choke, a DM filter and capacitances to ground. These capacitances contributes to making the conductors into a positive and a negative one instead of one of them being grounded. Investigating EMI with the input filter included should bring some more realistic results. The filter does not affect the efficiency enough to be worth considering.

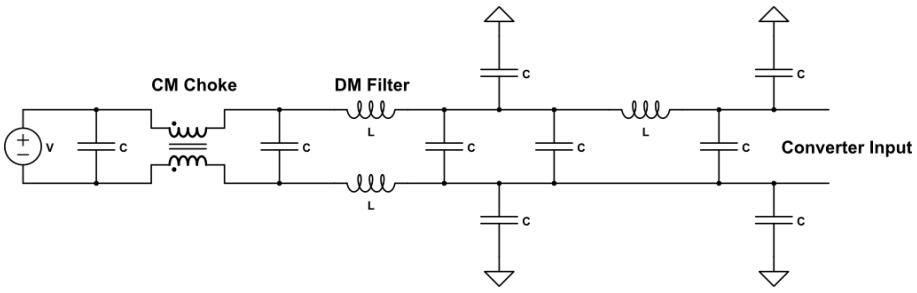


Figure 6.1: Input Filter

6.2 Frequency Spectrum at Resonance

The points in the circuit which are investigated are the input voltage and current to the converters. Measuring this together with the input filter gives an overview of the EMI noise created by the circuit. The input voltage to the converters can be seen in 6.2. In the figure it can be observed that the HBLLC consists of a lower amplitude for the spectrum up to 1 MHz. Both frequency spectrum's consists of peaks at the switching frequency and multiples of the switching frequencies. For every multiple, except 2 (600kHz), the HBLLC amplitude is much lower.

Another interesting thing to notice in the same figure is that the level between the peaks is considerably lower for every frequency below 1 MHz. Overall the level of the HBLLC is substantially lower than the forward converter. So according to the simulation the HBLLC performs better when it is operating at resonance frequency with regard to voltage noise. The amplitude of the EMI analysis is not certain, but the results should be comparable since they are simulated with the same conditions.

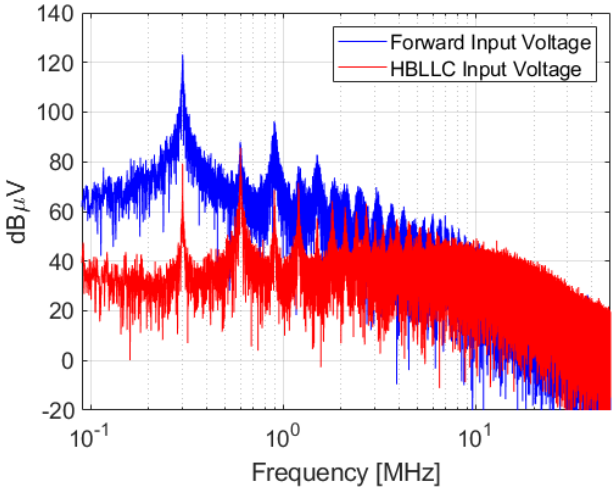


Figure 6.2: Voltage EMI at the input

The current through the converters was also investigated. The frequency spectrum of the current at the input is very similar the voltage frequency spectrum and can be observed in Figure 6.3. The overall amplitude is lower then in Figure 6.2. Other then that, there is not a lot more to be seen from the figure which was not present in the voltage noise.

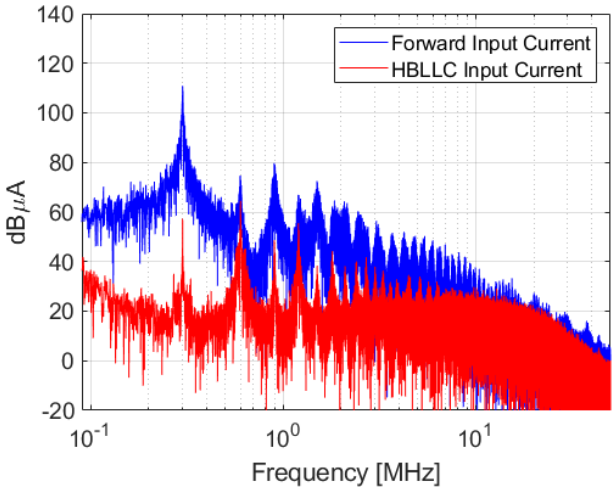


Figure 6.3: Current EMI through the converter, measured at the input

6.2.1 Other Frequencies

Since the HBLLC is controlled by manipulating its switching frequency the input voltage were also investigated for the usual cases of a switching frequency that is both higher and lower than the resonance frequency. The forward converter spectrum is unchanged.

The case of $f_{sw} < f_0$ can be seen in Figure 6.4. It can clearly be seen, just as expected, that the spectrum is shifted to slightly lower frequencies since the switching frequency is lowered. The biggest difference that can be observed is that the peak at $2f_{sw}$ is now higher in amplitude relative to the forward converter. But, when comparing the noise at the switching frequency, the HBLLC is lower then before and performs even better. Other then that, the spectrum looks approximately the same as before.

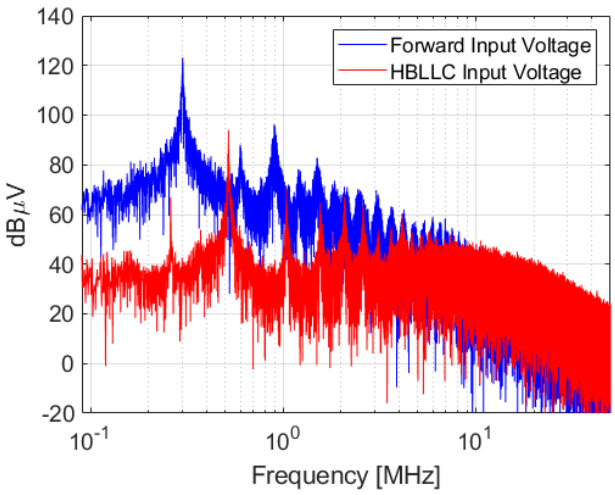


Figure 6.4: Voltage EMI at the input for $f_{sw} < f_0$

For $f_0 < f_{sw}$ which can be observed in Figure 6.5 the EMI performance seems to be the best for the 3 different options. Whats interesting is that the peak at the switching frequency pretty much disappears. The reason for this in our case is uncertain and not really known. From the waveforms in the time domain its expected to be lower, but to disappear completely was not expected.

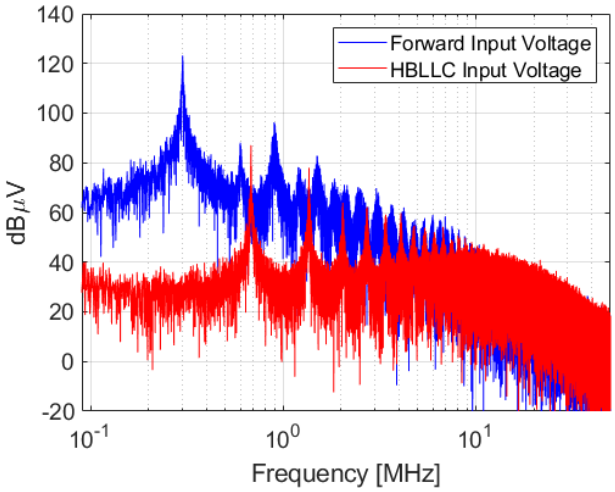


Figure 6.5: Voltage EMI at the input for $f_{sw} > f_0$

From the presented results on the EMI performance, it can be concluded that the HBLLC performs better overall for a resonance frequency of 300kHz and switching frequencies above or below 300kHz. From a pure EMI perspective the HBLLC would be preferred for the application based on our simulation results.

7

Increasing the Switching Frequency

To see the benefits of achieving ZVS for the HBLLC circuit, simulations at frequencies up to 3.6MHz where performed for both converters. The HBLLC circuit should theoretically be able to perform better at higher frequencies compared with the forward converter. To be kept in mind is that the transformer for the forward converter was never changed and the HBLLC circuit runs at resonance frequency. This makes the comparison not entirely fair and it probably has a big margin for error. Both circuits use the MOSFET rectifier in this chapter.

7.1 Increased Frequencies

At 300kHz it has been shown that the circuits are fairly similar in efficiency, see section 5.2. But more interesting results can be seen when the frequency increases. In Figure 7.1 it can be observed that the forward converter efficiency is somewhat linearly related to the switching frequency of the converter. The efficiency decreases to approximately 50% when the frequency is 3.6MHz, 12 times the original 300kHz. The HBLLC efficiency also decreases almost linearly but with a much slower pace and is still at around 90% at 3.6MHz.

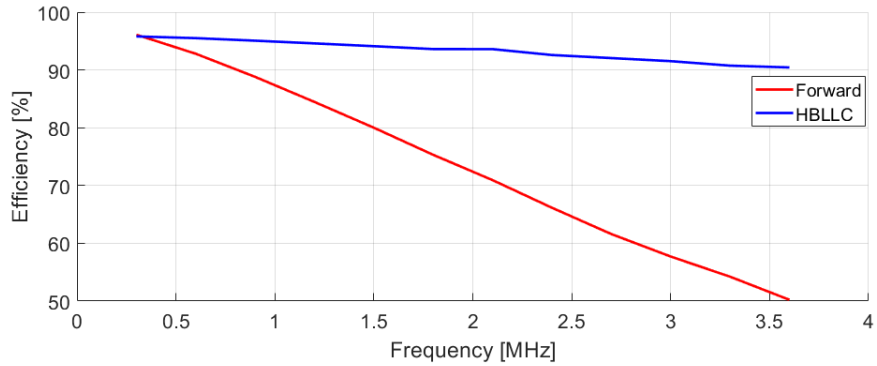


Figure 7.1: Efficiency comparison when increasing the frequency for rated load

The two first subfigures in Figure 7.2 shows in blue how the voltage and power is close to constant when increasing the frequency and at the same time redesigning the tank. Similar is shown in red for the forward converter but it is not redesigned

for every frequency.

The last subfigure compares the primary switching losses of the converters. It can be observed that the forward converter primary switching losses increases linearly with the frequency which is the reason for the behaviour in 7.1. The HBLLC does also increase linearly with the frequency but with a lower loss at 300kHz and a lot less increment over the spectrum which makes the HBLLC circuit considerably much more efficient.

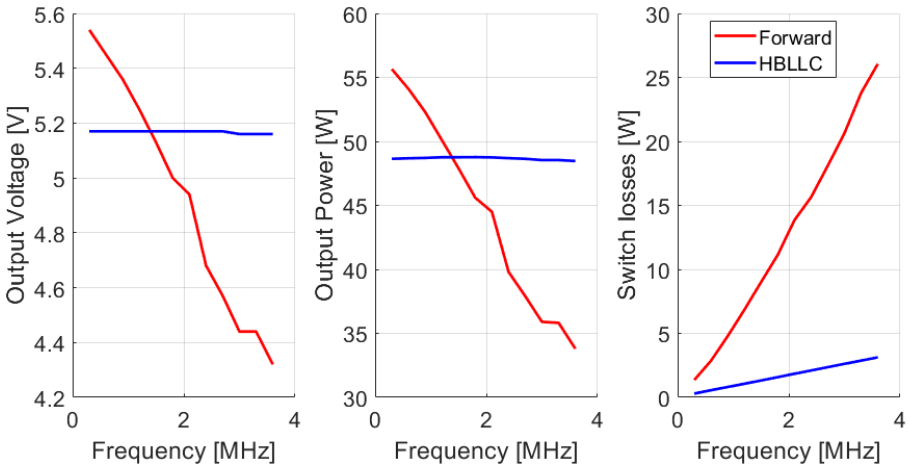


Figure 7.2: Comparison of output voltage, output power and primary switching losses for the forward converter and HBLLC

The switches on the secondary side of the converters does also contribute to the efficiency. In Figure 5.1 and 5.2 it can be observed that the secondary side switches for rectification contributes to approximately the same amount of losses for 300kHz. When the frequency is increased to 3MHz the losses for the HBLLC circuits secondary side switches is approximately $0.7W$, while the forward secondary side switch losses is approximately $2.4W$. Just as expected the losses on the secondary side for the HBLLC is close to unchanged while the forward losses has increased considerably relative to what they were. However, these losses does not have nearly the same impact on the efficiency as the primary switching losses displayed in Figure 7.2 and is therefore not looked further into.

When increasing the frequency and simulating a new resonant frequency the resonant tank has to be redesigned according to section 2.1.5. At higher frequencies, smaller inductors and capacitors has to be used as seen in Figure 7.3. The value of C_r and L_r decreases at the same rate and linearly. By doubling the switching frequency, the value of the components would be halved which should have an impact on the cost and size of the components.

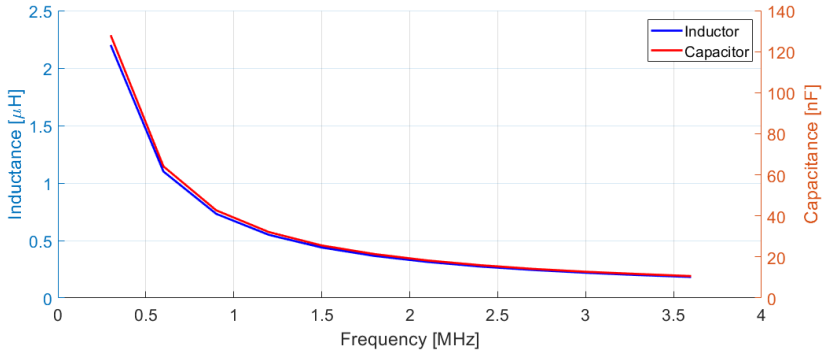
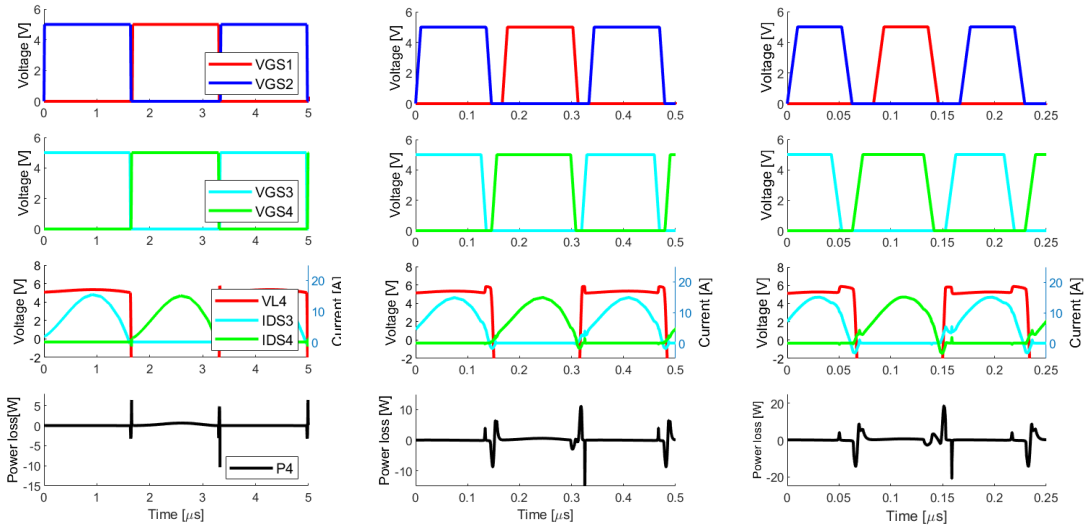


Figure 7.3: Component size in relation to increased resonance frequency

7.2 Waveform Distortion

Increasing the frequency in the design affects the waveforms, which is presented in Figure 7.4 for three different frequencies, all operating at their respective resonance frequency. In the Figure 7.4a the power loss of a secondary side MOSFET can be observed where there are small spikes resembling turn on and turn off losses but it is negligible in context since the conduction loss is dominating. In Figure 7.4b the frequency has increased so that the dead time is visible in the duty cycle. The turn on and turn off related body diode conduction is increasing in relevance for the rectifying loss with increasing frequency. From Figure 7.4c the dead time of the secondary side gate source voltages is more clear where during secondary dead time, body diodes are conducting. This is easily seen from the positive bump in $VL4$. During turn on and turn off less ideal current waveforms are seen compared to the first case in 7.4a. This is a consequence of the control settings not being perfect as the frequency is increased. The conclusion is that for high frequencies the control settings will be much important for yielding low rectifying losses. Higher frequencies then 6MHz gives strange waveforms from simulations, something that can partly be explained from (2.14), where for 6MHz the ratio between C_r and C_{eq} is approximately 5 and equation argument is not clearly approved.



(a) 300kHz **(b)** 3MHz **(c)** 6MHz

Figure 7.4: Gate and secondary side waveforms for increased frequency, operated at resonance frequency

By increasing the frequency the component size and values can be decreased while still achieving a high efficiency. The ZVS criteria needs to be full filled at the desired frequency or else the HBLLC would have similar switching losses as the forward converter. With a faster MOSFET the efficiency would be better at the higher frequencies since the rise and fall time of the MOSFET would occupy less time of the entire switching period. At some point the resonance capacitor could get small enough to interfere with the capacitance in the switches with increasing frequency, which would interfere with the resonance.

8

Cost

This chapter will present some of the component difference between the two investigated circuits and a small cost analysis, for a switching frequency of 600kHz.

8.1 Quantity of Components

The most relevant components and their quantities in both converter circuits are listed in Table 8.1. Same components are used in respective circuit but their configuration and how they are used differs. This is commented together with quantity.

Table 8.1: Components, quantity and configuration comment for converters

Component	HBLLC [no. + comment]	Forward converter [no. + comment]
MOSFET	4	4
Transformer	1, center tapped	1, normal tapped
Inductor	1, integrated	1, output
Capacitor	1, tank	1, clamp
Drivecircuit	1, frequency control	1 duty cycle control

8.2 Investment Cost

In Table 8.2 the most relevant components costs are estimated for the HBLLC. Where the important thing to highlight is the high cost of the transformer. No transformer has been found that suits the theoretical design which makes this estimation uncertain. Two partly suitable transformers were found. The transformer for the forward converter is custom made where the prize is unknown. Drive circuit costs are assumed to be equal. All costs are presented as per component, if approximately 100 components ordered, no shipping prize. The costs are gathered from web electronic sellers such as Mouser and Digikey [Accessed 2019-05-29]. The conclusion is that all costs are low compared to the transformer and the transformer cost is uncertain.

Table 8.2: Estimated HBLLC costs at low frequencies

Component	Cost	Part no.
MOSFET	\$0.57	BSZ0902NS
Transformer	\$4.7, \$9.9	750312504, 750310355
Capacitor	Table 8.3	
Drivecircuit	\$0.92	ICE2HS01G

The costs are more uncertain if looking at higher frequencies. For higher frequencies the MOSFET cost is expected to increase, due to higher performance demands. The transformer cost will decrease due to lesser material used. In other words, the costs in Table 8.2 will be frequency dependent. Depending on the chosen frequency, the cost of the passive components change. Table 8.3 shows how the resonant capacitor changes in prize for an increase of frequency. The resonant capacitor cost is small compared to other components at higher frequencies.

Table 8.3: Cost of a resonant capacitor depending on frequency

	300 kHz	600 kHz	900 kHz
Cr	128nF	64nF	32nF
Cr prize	\$0.131	\$0.067	\$0.055
Part no.	C0603C124K5RACTU	C0603C683K5RECAUTO	C0603C333K5RECTU

8.3 Operating Cost

For 300kHz the forward converter shows higher efficiency for the rated operation point and therefore this frequency will not be evaluated. From Table 5.6 the HBLLC shows higher efficiency for a 600kHz design at rated operation point, which could be used for a cost analysis. The cash flow C of one HBLLC compared to one forward operating for one year could be estimated. By taking the difference in efficiency at rated operation for the converters and multiplying it with the rated power, the difference in losses during operation is received. This multiplied with an assumed electricity price and one year in constant operation will yield the possible operating cost savings according to

$$C = (0.947 - 0.921) * 0.055[kW] * 0.12[\$/kWh] * 24 * 365[h * days] = 1.5[\$/year]. \tag{8.1}$$

The cash flow that costumer can save in operating costs for one product during one year operation is small.

8.4 Net present Worth

To continue the analysis it will be assumed that only the resonant capacitor is different in the circuits. The transformer costs will be assumed to be equal. The clamp

capacitor is very small and neglected in the analysis. The difference in investment cost is assumed to only rely on the resonant capacitor, see Table 8.3.

The net present worth can be calculated by assuming the economical life length as fifteen years and assuming discount rate as two percent. The cash flow from (8.1), the investment cost difference from Table 8.3 are used combined with (2.25) for a 600kHz design, yielding

$$NPW = \frac{\$1.5}{(1.02)^{15}} - \$0.067 = \$1.048. \tag{8.2}$$

The cash flow is substantially larger than the investment cost, yielding a high net present worth. The operation cost is in reality paid by costumer, but with a more sufficient product it is assumed that Ericcson can sell their product for a higher price. The assumption results in that the HBLLC can not cost more than the forward plus the NPW if there should exist any chance of profit for the company.

The number of produced PCBs that would use this converter is assumed to be 40 per hour. Assuming 8h shifts, production running 47 weeks per year, five of seven days are working days result in

$$PCB = 40 * [st/h] * 8[h] * 47 * 5[weeks * days] = 75200[st/year]. \tag{8.3}$$

Assuming a payback time of HBLLC implementation of one year, the amount of produced PCBs multiplied with the NPW would then give the development cost budget, approximately $75000.

8.5 Cost Summary

The quantity difference of components are small, yielding no clear results when comparing the converter circuits. The investment costs are dependent on the transformer mainly but also the frequency, which affects both the active and passive components. According to the analysis made the costumer would benefit of the solution through the lesser operating costs. The company could benefit as the prize of the product could be increased if the product is more efficient.

With greater knowledge concerning the economical assumptions, the reliability of the results can be improved. Assumptions such as differences in initial cost (transformer dependent), payback time, number of produced PCBs etc. are important assumptions for concluding if the HBLLC is supported economically for 600 kHz or not.

9
Conclusion

The simulated results suggests that the HBLLC is a candidate to replace the forward converter for the telecom application. The simulated efficiency's at rated operation for the 300kHz design are 95.3% for the HBLLC and 95.4% for the forward converter. This in itself does not show clear benefit for the HBLLC. When the input and output voltage is varied the HBLLC shows a higher efficiency for 4 out of 5 scenarios. Even if the efficiency is approximately the same for 300kHz switching frequency, the HBLLC performs better when considering EMI. The HBLLC EMI spectrum is all in all lower than the forward up to 1 MHz where the noise of the converters becomes similar.

For higher switching frequencies the HBLLC outperforms the forward converter because of the ZVS which lowers the switching losses significantly. The simulated efficiency's at rated operation for the 600kHz design are 94.7% for the HBLLC and 92.1% for the forward converter. When increasing the frequency to 3.6MHz, the efficiency's are around 90% for HBLLC and 50% for the forward converter. The ZVS can be further improved, especially concerning the active rectification which is of importance for higher frequencies. With regards to cost, the HBLLC should not be a lot more expensive relative to the forward converter. The difference in cost is not crucial compared to the other results.

9.1 Recommendation

The HBLLC definitely has potential to be better then the existing forward converter. It is recommended to continue the research and build a physical circuit to verify some of the simulated results and to be able to draw further conclusions.

9.2 Future Work

If the work is to be continued, there are a few areas that should be investigated. To start of with, there are several control considerations important for the LLC converter but the most important is a better and more stable way to perform the active rectification frequency control. The quality of control implementation is much related to what switching losses that appear, from theory, losses that should be zero. The secondary side control should be able to handle many different frequencies and

still keep a good quality, otherwise body diode conduction can appear. It is recommended to use an existing drive circuit solution instead of simulating with individual voltage sources, which hopefully will give an easier and more realistic control implementation.

The primary side control needs to be improved as well. The turn on loss related to body diode conduction can be kept smaller than in our simulations but one is taking a risk of getting closer to ZCS operation. Depending on how parasitic capacitance's affect at higher frequencies more dead time might be need for still assuring ZVS for other frequencies.

Within the thesis, non steady state behavior was decided not to be investigated. How the converter handles start up, sudden transients in load or input, need to be simulated before stating a physical evaluation. Concerning control, for more realistic simulation results of the efficiency curves it would be good to find the optimal frequency for each load case, instead of keeping frequency fixed during load sweep as now.

The transformer for the LLC application needs to be custom designed if it is going to be adapted after the theoretical design. It is crucial to investigate if the theoretical design is possible to achieve. In other words, is it possible to manufacture a transformer according to the inductance of the final tank design and still manage ratings related to for example voltage and current? If design can be done, what will its ESR values be? If the ESR values are greater than the existing converter transformer, efficiency will be affected negatively. The cost of converter will be much more clear when a transformer investigation has been done.

To get a real evaluation, a resonant converter needs to be built. The simulation results tells one story but the real world might be quite different. With more parasitic elements the results might not be as good and there would be a way to tell if EMI is more or less problematic, especially radiated EMI. Parasitic elements and noise maybe could affect the capability to achieve ZVS. Estimated efficiency and cost will receive more reliability if built circuit aswell.

There are many different component configurations that could be edited. Changing the MOSFETs in the circuit would be interesting. Changing them into faster ones could mean that even a better performance would be achievable for higher frequencies. There are a lot of other combinations of resonant circuits and resonant tanks that could be tested to see if they fit better for the purpose. A buck converter with an LCC resonant tank is one example of the many combinations available to try out.

Bibliography

[1] J. Akerlund, "-48 v dc computer equipment topology-an emerging technology", in *INTELEC - Twentieth International Telecommunications Energy Conference (Cat. No.98CH36263)*, Oct. 1998, pp. 15–21. DOI: 10.1109/INTLEC.1998.793472.

[2] E. Lam, R. Bell, and D. Ashley, "Revolutionary advances in distributed power systems", in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03.*, vol. 1, Feb. 2003, pp. 30–36. DOI: 10.1109/APEC.2003.1179172.

[3] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics*, 2:nd Edition. John Wiley & Sons, 1995, ISBN: 978-0471584087.

[4] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "Llc resonant converter for front end dc/dc conversion", in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 2, Mar. 2002, pp. 1108–1112. DOI: 10.1109/APEC.2002.989382.

[5] Y. Huang, L. Sinopoli, R. Petkov, and G. Anguelov, "High voltage, high power, high efficiency, digitally-controlled llc converter for telecom applications", in *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, Sep. 2014, pp. 1–7. DOI: 10.1109/INTLEC.2014.6972168.

[6] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An LLC resonant dc-dc converter for wide output voltage range battery charging applications", *IEEE Transactions on Power Electronics*, 2013, ISSN: 08858993. DOI: 10.1109/TPEL.2013.2241792.

[7] "A 10kW 97%-efficiency LLC resonant DC/DC converter with wide range of output voltage for the battery chargers in plug-in hybrid electric vehicles", in *2012 IEEE Transportation Electrification Conference and Expo, ITEC 2012*, 2012, ISBN: 9781467314077. DOI: 10.1109/ITEC.2012.6243457.

[8] S. Mao, J. Popovic, R. Ramabhadran, and J. A. Ferreira, "Comparative study of half-bridge LCC and LLC resonant DC-DC converters for ultra-wide output power range applications", in *17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*, 2015, ISBN: 9789075815221. DOI: 10.1109/EPE.2015.7311786.

[9] C. A. Cheng, H. W. Chen, E. C. Chang, C. H. Yen, and K. J. Lin, "Efficiency study for a 150W LLC resonant converter", *Proceedings of the International Conference on Power Electronics and Drive Systems*, pp. 1261–1265, 2009. DOI: 10.1109/PEDS.2009.5385876.

[10] J. Luo, J. Wang, Z. Fang, J. Shao, and J. Li, "Optimal design of a high efficiency LLC resonant converter with a narrow frequency range for voltage regulation", *Energies*, 2018, ISSN: 19961073. DOI: 10.3390/en11051124.

[11] T. Qian and Q. Wu, "A scheme of a resonant forward-flyback converter with suppressed frequency variation", *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3711–3716, 2018, ISSN: 08858993. DOI: 10.1109/TPEL.2017.2766024.

[12] A. Pawellek, C. Oeder, J. Stahl, and T. Duerbaum, "The resonant LLC vs. LCC converter - Comparing two optimized prototypes", in *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings*, 2011, ISBN: 9781457705427. DOI: 10.1109/ECCE.2011.6064064.

[13] S. Shiva Kumar, A. K. Panda, and T. Ramesh, "A ZVT-ZCT PWM synchronous buck converter with a simple passive auxiliary circuit for reduction of losses and efficiency enhancement", *Ain Shams Engineering Journal*, vol. 6, no. 2, pp. 491–500, 2015, ISSN: 20904479. DOI: 10.1016/j.asej.2014.10.018.

[14] S. Pattnaik, A. K. Panda, and K. Mahapatra, "Efficiency improvement of synchronous buck converter by passive auxiliary circuit", *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2511–2517, 2010, ISSN: 00939994. DOI: 10.1109/TIA.2010.2070831.

[15] D. A. Torrey, "Comparison of Hard Switched, Edge-Resonant, and Load Resonant DOC Converters Using a Common Power Stage", pp. 1588–1595, 1998.

[16] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in dc-dc converters", *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4968–4977, 2013, ISSN: 02780046. DOI: 10.1109/TIE.2012.2224071.

[17] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Analysis and reduction of common mode EMI noise for resonant converters", *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 566–571, 2014. DOI: 10.1109/APEC.2014.6803365.

[18] D. Fu, P. Kong, S. Wang, F. C. Lee, and M. Xu, "Analysis and suppression of conducted EMI emissions for front-end LLC resonant DC/DC converters", *PESC Record - IEEE Annual Power Electronics Specialists Conference*, pp. 1144–1150, 2008, ISSN: 02759306. DOI: 10.1109/PESC.2008.4592084.

[19] The European Parliament and the Council of the European Union, "DIRECTIVE OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL on the restriction of the use of certain hazardous substances in electrical and electronic equipment (Recast)", 22 March, 2011, pp. 1–66.

[20] M. H. Rashid, H. Shu Yuen (Ron), and H. S.H. Chung, "Resonant and soft-switching converters", in *Power Electronics Handbook*, 2011, pp. 339–382, ISBN: 9780123820365. DOI: 10.1016/B978-0-12-382036-5.00016-1.

[21] H. Huang, "Designing an LLC Resonant Half-Bridge Power Converter", pp. 3.1–3.27, 2011.

[22] M. A. Halim, M. N. Seroji, and M. N. B. Hidayat, "Analysis characteristics and optimal design procedure of half-bridge LLC loaded resonant converter",

PECon 2012 - 2012 IEEE International Conference on Power and Energy, no. 06, pp. 564–569, 2012. DOI: 10.1109/PECon.2012.6450278.

[23] B. Bell, *Operation and Benefits of Active-Clamp Forward Power Converters*, 2011.

[24] STMicroelectronics, "An introduction to LLC resonant half-bridge converter, Appl. Note AN2644", pp. 1–64, 2008.

[25] Infineon, "MOSFET Power Losses Calculation Using the Data- Sheet Parameters, Appl. Note V 1.1 2006", pp. 1–24, 2008.

[26] A. M. Trzynadlowski, "EMI effects of power converters", in *Power Electronics Handbook*, 2011, ch. 42, pp. 1381–1396, ISBN: 9780123820365. DOI: 10.1016/B978-0-12-382036-5.00042-2.

[27] "Design criteria for resonant tank of LLC DC-DC resonant converter", in *IECON Proceedings (Industrial Electronics Conference)*, 2010, ISBN: 9781424452262. DOI: 10.1109/IECON.2010.5674988.

[28] T. Hegarty, "An overview of conducted EMI specifications for power supplies", 2018. [Online]. Available: http://www.ti.com/lit/wp/slyy136/slyy136.pdf.

[29] Infineon, "Resonant LLC Converter Operation and Design, Appl. Note AN 2012-09 V1.0", pp. 1–19, 2012.

[30] B. Bell, "Topology Key to Power Density in Isolated DC-DC Converters", no. February, pp. 16–20, 2011. [Online]. Available: https://www.powerelectronics.com/dc-dc-converters/topology-key-power-density-isolated-dc-dc-converters.[Accessed:25-Jan-2019].

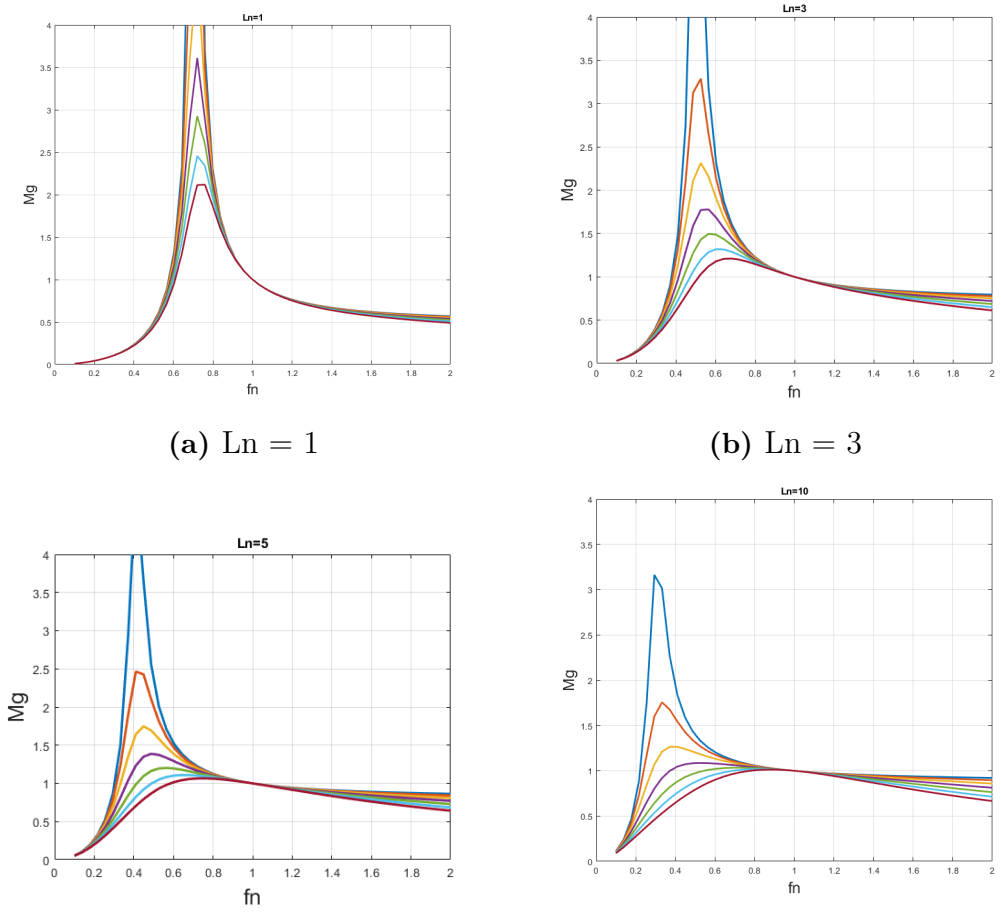
[31] J. Song, D. Yang, C. Zhang, and B. Duan, "Hybrid Control Method for CLLLC Resonant Converter with Low Output Voltage Ripple", *IFAC-PapersOnLine*, vol. 51, no. 31, pp. 680–684, 2018, ISSN: 24058963. DOI: 10.1016/j.ifacol.2018.10.157.

[32] R. L. Lin and C. W. Lin, "Design criteria for resonant tank of LLC DC-DC resonant converter", in *IECON Proceedings (Industrial Electronics Conference)*, 2010, ISBN: 9781424452262. DOI: 10.1109/IECON.2010.5674988.

[33] V. Ricchiuti, "Introduction to Transformer Magnetics", 2000. [Online]. Available: https://www.networking.pulseelectronics.com/hubfs/signal-transformer/Introduction-Transformer-Magnetics.pdf?hsLang=en-us.

A

Inductance ratio and Quality factor effects on the transfer function



(a) Ln = 1

(b) Ln = 3

(c) Ln = 5

(d) Ln = 10

Figure A.1: Different inductance ratios

In Figure A.1 it can be observed that an increase of the induction ratio increases the the switching interval in which where the switch needs to operate to be able to achieve a certain gain. With an increasing inducting ratio, while keeping the same

quality factor (Q), the maximum gain also decreases which can be observed when comparing Figure A.1a and Figure A.1d for example.