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Design of a phase locked loop for 60 GHz/ 30 GHz signal generation in 22 nm FDSOI technology for wireless transceivers

Master's thesis in Computer science and engineering

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Abstract

Phase Locked Loops (PLLs) are fundamental components in communication systems used in frequency synthesis, carrier recovery and modulation. Massive Multiple Input Multiple Output (MIMO) based millimeter wave communication systems demand reference frequencies with high spectral purity. Low power implementation of PLLs in deep submicron CMOS processes is essential in the current market demand for integrated transceivers for future communication systems like 5G. This thesis deals with the design of a 60 GHz PLL in 22 nm FDSOI technology for use in 5G transceiver systems.

Keywords: PLL, 5G, 22 nm, VCO, injection locking, phase noise, charge pump, PFD

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Sajeendran Bhuvanendran Sathiabhama, Gothenburg, April 25, 2019

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Acronyms

5G Fifth generation. 1

ADE Analog Design Environment. 24, 26
AR/VR Augmented Reality Virtual Reality. 1

DAC Digital to Analog Converter. 1, 2
DSP Digital Signal Processing. 1

HB Harmonic Balance. 25

ILFD Injection Locked Frequency Divider. 32

LNA Low Noise Amplifier. 1

MIMO Multiple Input Multiple Output. v, 1
mmwave millimeter wave. 1

PA Power Amplifier. 1
PGA Programmable Gain Amplifier. 2
PLL Phase Locked Loop. 2, 3, 9
PNOISE Periodic Noise. 25, 26
PSS Periodic Steady State. 24, 26, 31

Q quality. 5, 25, 26

RF Radio Frequency. 1

TRAN transient. 24, 26, 31, 33, 35

ViVA Virtuoso Visualization and Analysis Tool. 24

1
Introduction

This chapter gives a background to the project and describes the objectives and limitations for the design.

1.1 5G communication transceivers

Fifth generation (5G) mobile networks are pursued as high data rate radio access technology in the millimeter wave (mmwave) spectrum (28 GHz, 38 GHz, 60 GHz). The technology standardization is on its way and is expected to be deployed for commercial applications by 2020[1], [2]. The new technology aims to cater to the needs of upcoming applications like smart city, connected cars, health, entertainment (Augmented Reality Virtual Reality (AR/VR)), smart grid etc. to name a few.

As new technological challenges are introduced because of wide bandwidth, higher frequency band, usage of Multiple Input Multiple Output (MIMO) technology etc., alternate transceiver architectures to enable low-cost low-power CMOS solutions for the mass market is a hot topic in the industry. Hence researchers have focused on architecture level as well as circuit level optimization to cater to the needs of the industry.

1.2 Radio architectures

The radio transmitters are classified into different types like direct conversion, variable Intermediate Frequency(IF), heterodyne, polar etc. similarly the radio receivers can be of different type like direct conversion, hetrodyne, low IF etc.[3]. However, depending on the signal used for communication signal processing, the typical radio can be classified into two architectures - IQ and polar. In the IQ or quadrature radio architecture, the in-phase and the quadrature components of the complex baseband signals are used for the transmission and reception. An example transmitter operating on baseband IQ signals and using direct conversion is shown in fig.1.1. The transmitter consists of a Digital Signal Processing (DSP) block handling the baseband signal processing for upsampling and lowpass filtering (together known as interpolation) followed by a Digital to Analog Converter (DAC) block. Filters are added for anti-aliasing and spurious signal removal. The local oscillator generates the Radio Frequency (RF) or mmwave signal at the transmit frequency. A mixer upconverts the analog signals to RF or mmwave frequency band, a Power Amplifier (PA) amplifies the signal and an antenna transmits the signal. At the receiver side, the Low Noise Amplifier (LNA) amplifies the received signal, a mixer downconverts

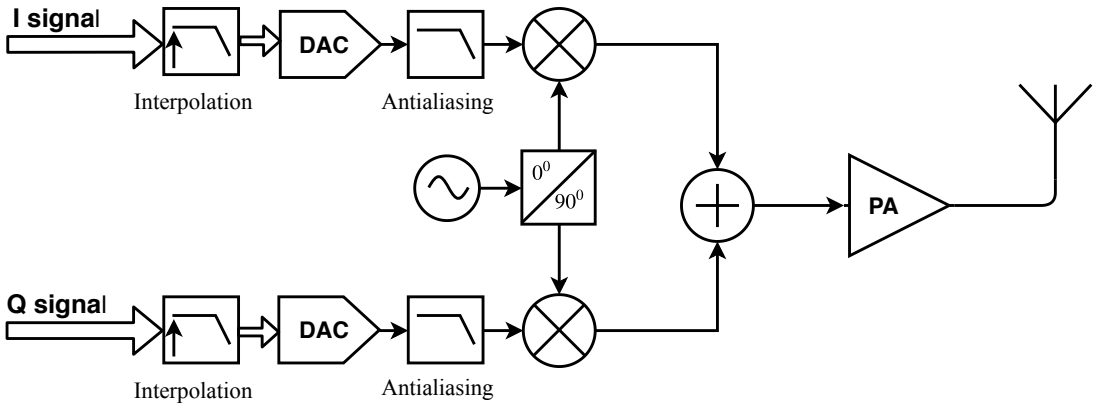


Figure 1.1: An example IQ transmitter architecture with baseband direct upconversion[3]

the RF signal, a Digital to Analog Converter (DAC) digitizes the baseband signal and a DSP block does the necessary processing to extract the information.

The polar architecture uses the amplitude and phase signals instead of the I/Q signals that the quadrature architecture uses. An example implementation utilizing digital PLL is shown in fig.1.2[3]. In this example implementation, the I/Q signals are interpolated first for high sampling rate and image frequency removal. The polar signals comprising of amplitude and phase information are generated from the I/Q signals. The phase modulation of carrier signal is formed with the help of a a digital PLL whose phase reference depends on the carrier frequency and the phase signal derivative. The amplitude signal is amplified using a Programmable Gain Amplifier (PGA) and is fed to a DAC and a reconstruction filter to generate the analog amplitude signal. The modulated complex waveform is generated by multiplying the amplitude signal and the phase modulated signal. This is fed to power amplifier and transmitted via the antenna.

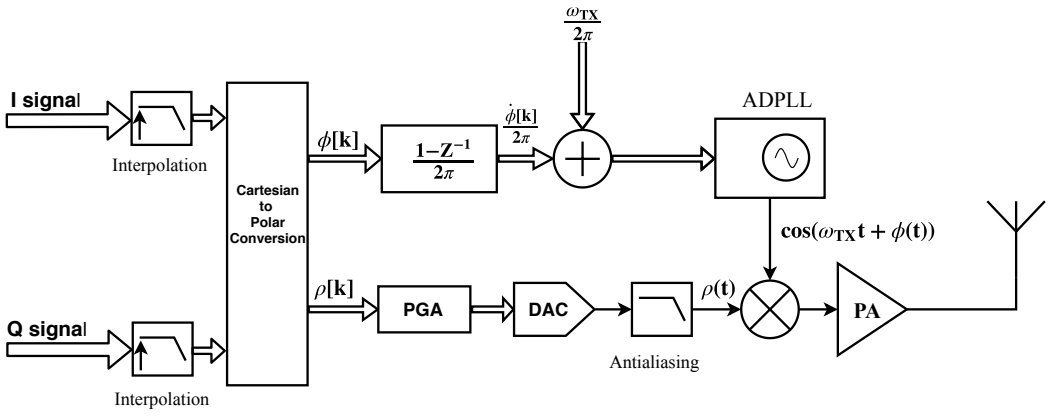


Figure 1.2: An example polar transmitter architecture[3] utilizing digital PLL

The quadrature architecture has the advantage of symmetric channels for both I and Q channels. Moreover, the bandwidth of the baseband signals is smaller

compared to the polar signals for the same RF bandwidth. However, the quadrature architecture suffers from the necessity to use linear power amplifier. In contrast, the polar architecture allows the usage of high efficiency switching mode power amplifiers if the peak-to-average-power (PAPR) is low[4] . But, the polar transmitter architecture suffers from the fact that the signal paths of the two signals, a(t) and ϕ(t) are different and this leads to timing alignment issues[5].

1.3 Goal of project

An alternate implementation of the polar transceiver as depicted in fig.1.3 is currently being pursued at Chalmers University. In this transceiver, the DSP block generates the amplitude (A[N_1 :0] and phase signals ($\phi[N_2 : 0]$) from the baseband data. The Phase Locked Loop (PLL) and the phase rotator generates the phase modulated carrier. The RF DAC amplitude modulates this signal and is sent to the antenna for transmission. The receiver is designed to operate at 60 GHz an the transmitter at 30 GHz so that the power amlifier at the receiver has little pulling effect on the local oscillator[6]. Keeping the phase rotator outside of the carrier generation process addresses the problem of wide bandwidth polar signal (1 GHz). The RF DAC block is capable of amplitude modulation of a phase modulated input signal and has already been implemented in 22 nm technology[7].

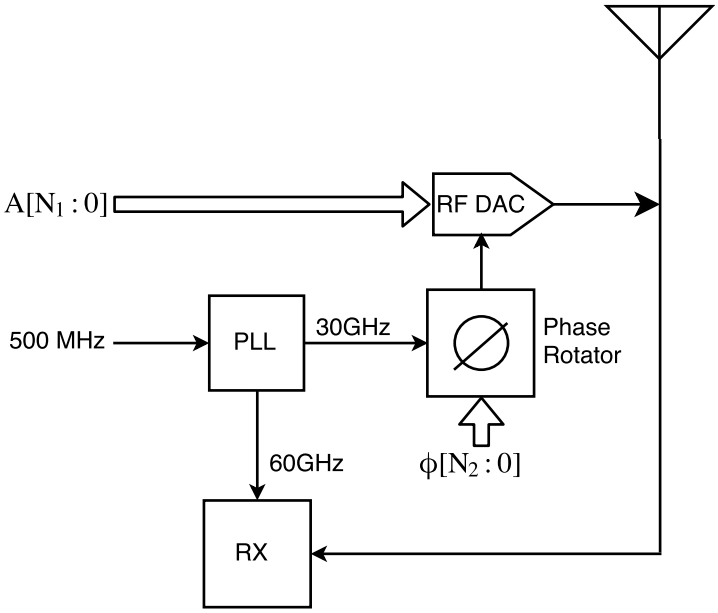


Figure 1.3: Polar Transceiver architecture with baseband direct conversion

The goal of the project is to design and simulate a PLL (Phase Locked Loop) chip to generate a reference 60 GHz signal for receiver side and a 30 GHz signal for the phase rotator at transmitter side as in fig.1.3. Emphasis is given towards low power and low phase noise implementation.

1.3.1 Prestudy

The basic PLL sub-blocks are shown in fig.1.4. The PLL is a closed loop system in which the output phase is locked to the input phase with the help of feedback[8]. A Voltage Controlled Oscillator (VCO) generates the 60 GHz output signal for the receiver side. An injection locked frequency divider (ILFD) generates a 30 GHz for the phase rotator mentioned in fig.1.3 to convert the phase signal to 30 GHz phase modulated signal. An important phenomenon occurring in the transceivers is the local oscillator pulling due to the power amplifier at the receiver side. By keeping the main oscillator run at 60 GHz and the receiver side at 30 GHz helps in reducing the local oscillator pulling problem.

The scaled down output frequency and input reference frequency are compared to get the phase error. The phase error is filtered and used to control the oscillation frequency of the VCO. The VCO and the ILFD circuits constitute the high frequency front ends. The phase detector and loop filter are low frequency backends. These constitute a mixed signal PLL as opposed to an all-digital PLL (ADPLL) which uses digital dividers and counters at the frontend as well.

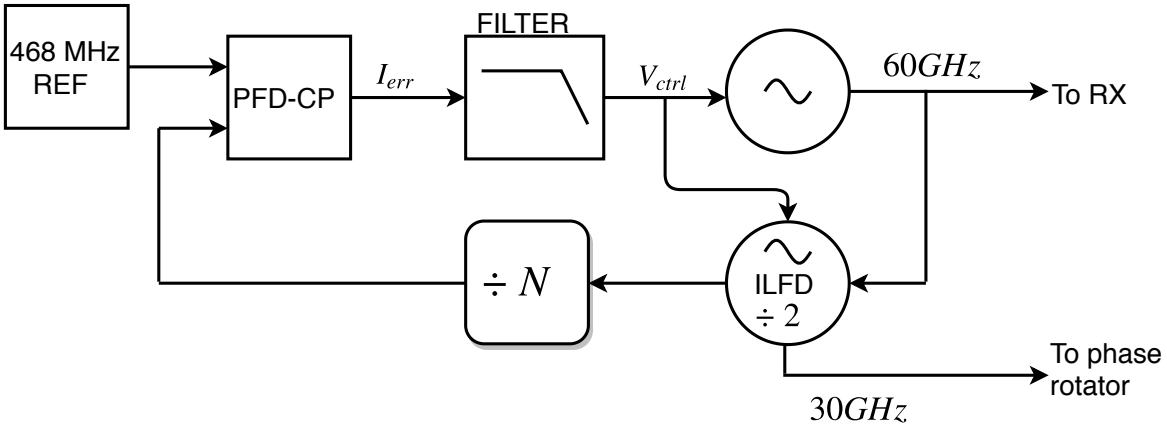


Figure 1.4: Basic PLL block diagram

The PLL provides the stable output carrier references at 30 GHz and 60 GHz. The phase modulation is done in a separate block at the output instead of doing it in the loop. This way, the challenges associated with the PLL design and the wide band phase modulation can be addressed separately.

For initial system simulations, the system specification based on the literature survey and previous experience[9] is used and is as follows.

- Phase detector : Phase frequency detector (PFD) with output charge pump (CP)
- Loop Filter : Passive RC second order
- VCO : LC based
- Divider : Injection Locked Divider followed by a True Single Phase Clock based divider
- Input reference frequency : 468 MHz

- Loop Bandwidth : 2 MHz
- $K_{VCO} = 2\,\mathrm{GHz\,V^{-1}}$
- $I_P = 2\,\mathrm{mA}$
- $K_P = \frac{I_p}{2\pi}$

The 22 nm FDSOI technology from Global Foundaries (GF22FDX) is selected for the design. Since the VCO and frequency divider constitute the mmwave frequency circuits, detailed study and time is needed in the design. A varactor tuned LC oscillator is a common circuit in mmwave circuits[10] but poses challenges in terms of tank circuit quality (Q) factor for on chip realization[11]. The phase noise inherent in oscillator also poses challenge for low power design, as according to Leeson's model for Phase noise, the phase noise is inversely proportional to the power and directly proportional to the frequency of oscillation[12].

Cadence tools will be used for circuit simulations. The layout is not aimed for, but may be started provided the planned activities are finished within the scheduled time frame. The successful completion of design stage and hence the masters thesis is based on successful simulation results from circuit simulation for the system.

1.4 Outline

The thesis report is organized as follows. The background theory of PLL system and circuit level working of individual subblocks are explained in theory section. The design section explains the design process for the system. The results of simulation are consolidated in the results section. The observations from the thesis is concluded in the conclusion section.

2
Technical Background

This chapter explains the basic working of a PLL and the models used for system simulation.

2.1 Working of PLL

A phase-locked loop is a closed loop feedback system first introduced in 1932[13] and is shown in fig.1.4. It consists of a Voltage Controlled Oscillator (VCO) at its core running at an output frequency. However, the frequency of oscillation may not be stable due to the internal component mismatches and temperature variations. A divider chain in the feedback system generates a scaled down version of the output signal.

For the divider chain, a division ratio of 128 is necessary for a reference frequency of 468 MHz and output frequency of 60 GHz. This requires design of a toggle flip-flop based divider operating from 60 GHz down to 468 MHz. However, the toggle flip-flops are feasible in the range of 30 GHz. Hence an Injection Locked Frequency Divider (ILFD) circuit is used at the output of VCO for the initial frequency division by two. This 30 GHz signal can be used at the receiver side as well for signal detection. The ILFD is followed by toggle flip-flop based frequency divider for providing the feedback signal to the phase frequency detector (PFD).

The PFD then compares this scaled down signal with a reference signal. The phase difference is converted to a current pulse with the help of a charge pump and is converted to a voltage and filtered using the low-pass filter. This error voltage acts as the control voltage for the VCO and keeps the frequency of oscillation stable.

2.2 PLL terminology

Traditional PLLs are characterized by acquisition range, capture range, lock range, tracking range etc. However, for modern PLLs the distinctions in different frequency ranges are not needed and hence only the following terms are explained.

Hold-in Range : It is the frequency range over which the PLL is able to maintain its lock statically and the PLL drifts out of lock forever after this range. It is obtained from the fact that the phase error is at its maximum for a frequency offset of the hold range. This is however limited by the VCO tuning range.

Lock-in Range : It is the frequency range over which a PLL is able to lock to the reference frequency within a single period of the beat frequency.

Lock-in time: It is the time taken to lock to the reference frequency.

Pull-in Range : It is the frequency range over which a PLL is able to lock to, however this is a slower process due to multiple beat notes needed compared to lock-in.

Pull-in Time : It is the time required for pull-in process.

Pull-in and lock-in are part of the acquisition process and hold-in is part of the tracking process. The lock-in and pull-in process are visualized in fig.2.1.

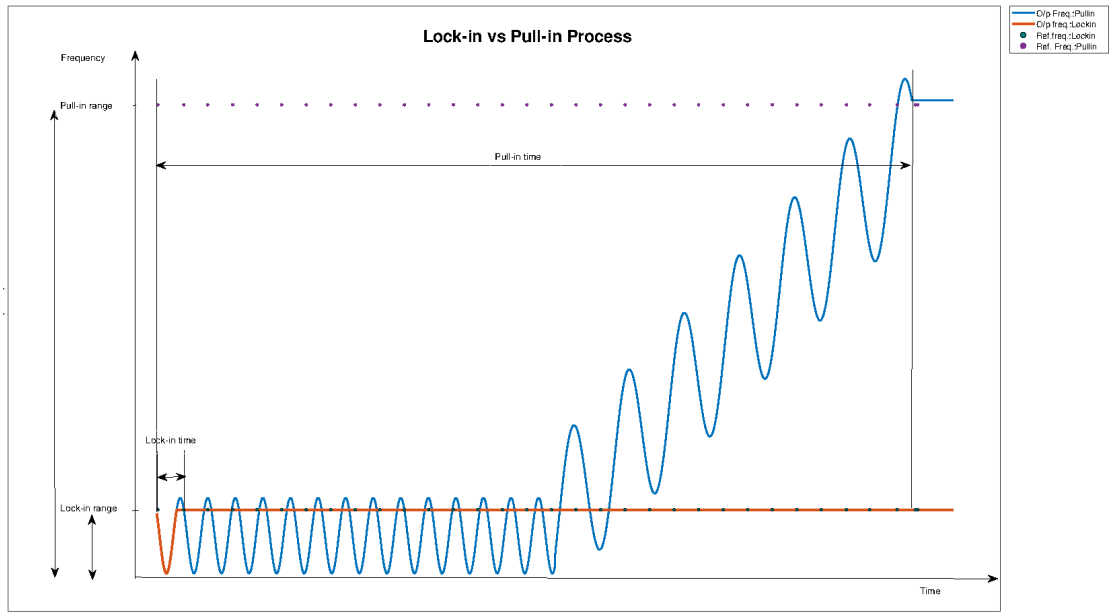


Figure 2.1: Lock-in and Pull-in process

2.3 Linear Model for PLL design

A PLL with small phase deviation about its centre frequency after achieving lock state can be approximated with the help of a linear lowpass model. This assumption, presumably reduces the complexity of simulation at the oscillation frequency of 60 GHz. Obviously, the locked state approximation ignores the initial transient conditions. Also, the approximation of small phase deviation is valid as the loop bandwidth is kept small for fast locking. A linear model in the s domain is used for the initial calculations. After that, all the signals are referred to the phase signals instead of the voltage signals and hence phase transfer functions are used for the blocks. A linear phase domain model for the PLL is shown in fig.2.2. The phase/frequency detector is represented by a difference unit followed by a gain section representing the charge pump. The gain magnitude is then $I_p 2\pi$ where the 2π represents the frequency to phase conversion and I_p is the charge pump current gain in the range of milliamperes.

The filter is followed by a VCO which for a phase signal is an ideal integrator with gain K_0 with the units of $\mathrm{GHz\,V^{-1}}$. The divider feedback is a gain (or attenuation) with magnitude 1/N. The closed loop transfer function of the system, H(s)

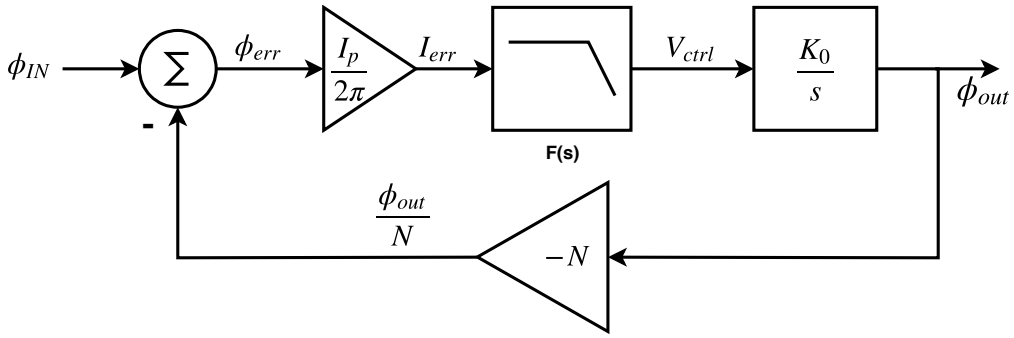


Figure 2.2: Linear Phase Model of PLL

is then given by

$$H(s) = \frac{K_p F(s) K_0/s}{1 + K_p F(s) K_0/s} \tag{2.1}$$

2.4 Circuit Topologies

In this section, the different sub circuits used in the PLL is discussed. The various performance measures and design considerations are explained.In the first section the LC cross-coupled VCO is discussed and the phase noise parameter is detailed. It is followed by the discussion of ILFD and the TSPC based divider. Later the Phase Frequency Detector and the Charge Pump circuit is discussed.

2.4.1 VCO

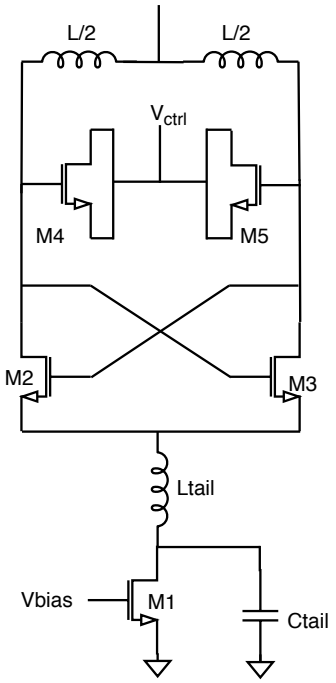


Figure 2.3: Voltage Controlled Oscillator

A varactor tuned LC oscillator with tail current biasing is used and is common in these frequency ranges. The LC oscillator consists of a passive tank circuit resonating at the oscillation frequency. The capacitor of the tank is made of accumulation mode MOSFET shorted at the drain and source. This terminal acts as the tuning port, since the voltage applied at this port will change the reverse bias and hence the capacitance. The accumulation mode is ensured by selecting the nMOS in nwell and hence the inversion mode is prevented.However, the losses associated with the circuit attenuates the oscillation. Hence, a cross-coupled pair (M_2 and M_3) with tail current biasing (M_1) provides the necessary loss compensation and is known as the negative gm circuit. The cross-coupled pair switches between saturation and cut off and hence acts as current steering circuits.

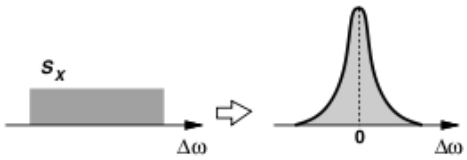
The oscillator can operate in two regimes- current limited and voltage limited, depending on the bias current at the tail. In the current limited regime, the tank amplitude is determined by the tail current and the tank impedance. This mode of operation is characterized by less tail current distortion and smaller voltage swing. In voltage limited regime, the cross-coupled pair transistors enter triode region. This mode is characterized by more output voltage swing, but with tail current distortion.

In order to obtain maximum voltage swing, the voltage limited regime is used in the design described in this report. To avoid the tail current distortion associated with this mode of operation, a tail filter capacitor (C_{tail}) is used to bypass high frequency components. In addition, the source node of the cross-coupled pair is at the second harmonic and a peaking inductor (L_{tail}) together with the node parasitic capacitance enhances the second harmonic injection. This improves the phase noise performance[14], an important parameter for the VCO and is discussed below.

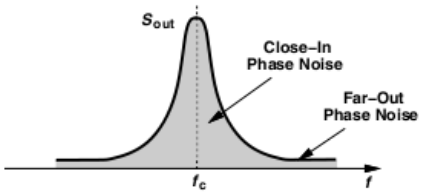
Phase Noise

Phase noise is one of the important parameters for a VCO and determines the spectral purity of the PLL as well. As shown in fig.2.4b, the phase noise causes the output frequency spectrum to be a range of spectral components centered around the oscillation frequency. The cause of phase noise can be represented with the help of noise shaping of flat noise band around the centre frequency. The phase noise is specified with the help of noise power in a bandwidth of 1 Hz at a specific offset from the centre frequency. The unit is $\mathrm{dBc\,Hz^{-1}}$ where the dBc stands for dB with respect to the carrier and signifies the normalization of noise power to the carrier power.

The impact of phase noise on the receiver system is significant. For example, an unwanted signal can exist close to the signal frequency at the receiver side. The mixer available at the receiver translates the frequency of the received signal to a different frequency by a process known as downconversion. In a Super-heterodyne architecture, the downconverted signal occurs at an intermediate frequency. In a Direct conversion architecture, it occurs at a low frequency. In both cases the interference signal cannot be filtered out and will be indistinguishable from the actual signal distorting the signal received. Another impact is the phase rotation of the received signal constellation increasing the bit error rate of the receiver. This calls for specific phase recovery algorithms at the receiver side[6].



(a) Noise shaping in LC oscillator[6]



(b) Phase noise curve for LC oscillator[6]

2.4.2 Injection Locked Frequency Divider

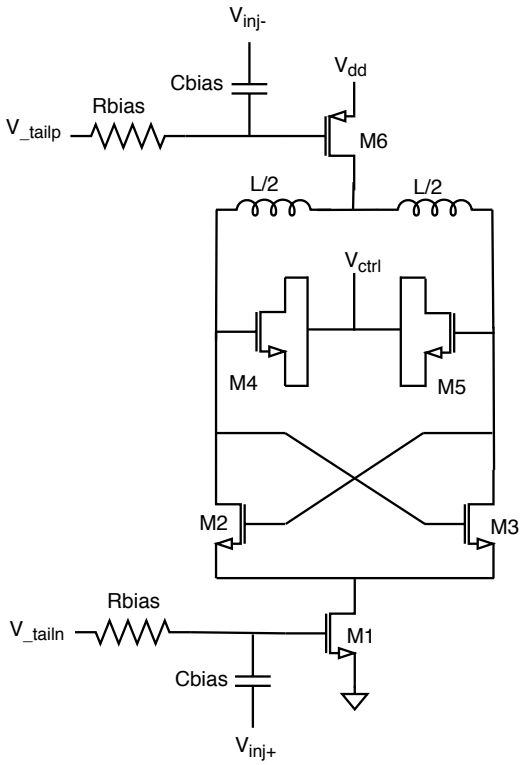


Figure 2.5: Injection Locked Frequency Divider

An injection locked frequency divider (ILFD) is an oscillator with external signal injected in order to lock the frequency of oscillation. The ILFD circuit consists of a VCO circuit, but biased at lower current requirements since the oscillation is sustained by injection from an external source. The injected signal transfers power at second harmonic and hence the injection point has to be at a second harmonic node which for an LC oscillator is the source node of cross-coupled pair.

The circuit consists of a tank circuit (L, M_4, M_5) and a cross-coupled pair (M_2 and M_3) similar to a VCO and oscillates at 30 GHz. The DC bias and RF injection is provided by the transistors, M_1 and M_5. In contrast to the tail current source in VCO, the tail and top bias transistors in ILFD acts as RF devices operating in the active region. The DC and AC bias are applied through the resistor, R_{bias} and the

capacitor, C_{bias} respectively.

Due to the reduction in number of zero crossings by a factor of 2, the phase noise in ILFD is expected to have a phase noise improvement of 6dB[15]. Different points of injection for the oscillator are reported in the literature like the output node[14], the tail bias current source or across the cross coupled pairs[16].

For the thesis, a differential topology of injection is used with the help of a dual biasing using top PMOS and bottom NMOS pair in order to provide a symmetric load to the VCO. The symmetric load to the VCO is advantageous in terms of obtaining the maximum voltage swing from the VCO. In addition, the ILFD circuit gains from the additional power being injected and hence improves the phase noise. As far as I know, this topology is not reported elsewhere in literature.

As shown in the figure 2.5, the circuit is symmetrical and accepts differential input signals from VCO.

Locking Range

One of the important parameter for the ILFD is the locking range and is defined as the frequency range for which the injection happens. Once successful injection happens, the DC power required by the ILFD circuit is the minimum compared to the case when its out of lock. Moreover, once lock is reached the circuit is capable of resisting the changes in output signal frequency even if the injected signal is deviating from its centre frequency.

The locking range of conventional injection locked frequency divider is given by

$$\omega_L = \frac{\omega_0}{2Q}.\frac{I_{inj}}{I_{osc}} \tag{2.2}$$

where I_{inj} is the injection current, I_{osc} is the oscillation current, ω_0 and Q are the free running frequency and Q factor of the tank respectively, analyzed in detail by the popular works of Adler[17], Kurakowa[18] and Razavi[15]. The equation simply states that for higher locking range, I have to intentionally lower the Q factor and/or increase the injection current. This is in contrast to the Q factor requirement for an oscillator and hence the lower output swing compared to that of an oscillator. However, wide locking range is still possible without compromising much on the Q factor of the tank[9].

2.4.3 Prescaler

The output of the ILFD at 30 GHz is divided to the reference frequency of 468 MHz by the prescaler chain. The CML based dividers consume more power and hence the True Single Phase Clocking (TSPC) based dividers are utilized for low power consumption and high speed operation. TSPC is a Clocked CMOS (C^2MOS) circuit of the dynamic logic families and hence has a low frequency limit around a few hundred MHz[19].

The circuit, initially reported by Yuan and Svensson[20] with optimization recommended by Huang et.al [21] is used for the design. The feedback is provided from the inverted output for toggle configuration. The circuit consists of three

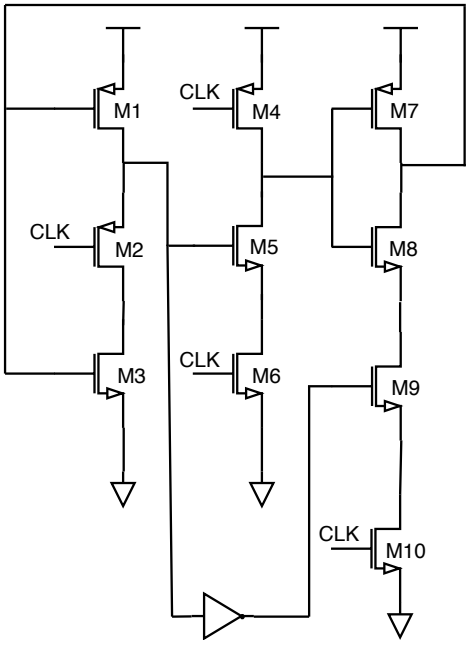


Figure 2.6: TSPC schematic 1

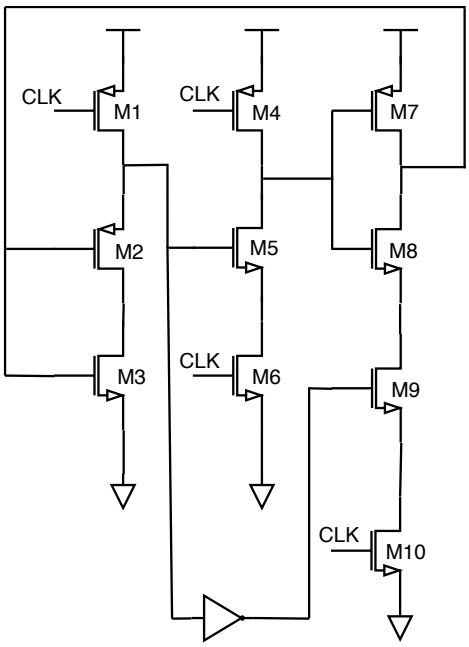


Figure 2.7: TSPC schematic 2

clocked buffer stages in series and can be seen as clocked capacitors. The phase of the clock is held by the first stage during the acquisition phase while the later stages are in the precharge phase. During next clock phase change, evaluation of the charge acquired in the first stage happens at the last stages. In the last stage, a fourth transistor is used to hold the charge controlled by the inverted first stage output[21]. This circuit is used for the first stage of the divider (30 GHz to 15 GHz).

The circuit in fig.2.7 is identical to the first one except that the clock nodes are near the rail which eases the sizing requirement to two rather than four in the

original circuit[20].

In Dynamic CMOS circuits, due to the loading of pull up PMOS stages by the subsequent stages, a dip in the voltage is normally observed[22]. In order to avoid this, weak PMOS transistors called keeper transistors are added at the output node either with grounded gate or inverted output connected to the gate. This is implemented in the TSPC circuits as well[21].

Referring to the fig.2.8, the pMOS together with the nMOS logic forms the dynamic circuit and the pMOS, M_{11} controlled by the inverter forms the keeper circuit and prevents the output voltage from dropping .The division of (15 GHz to 463 MHz) is done by the circuit of fig.2.8 which is as reported in the paper[21].

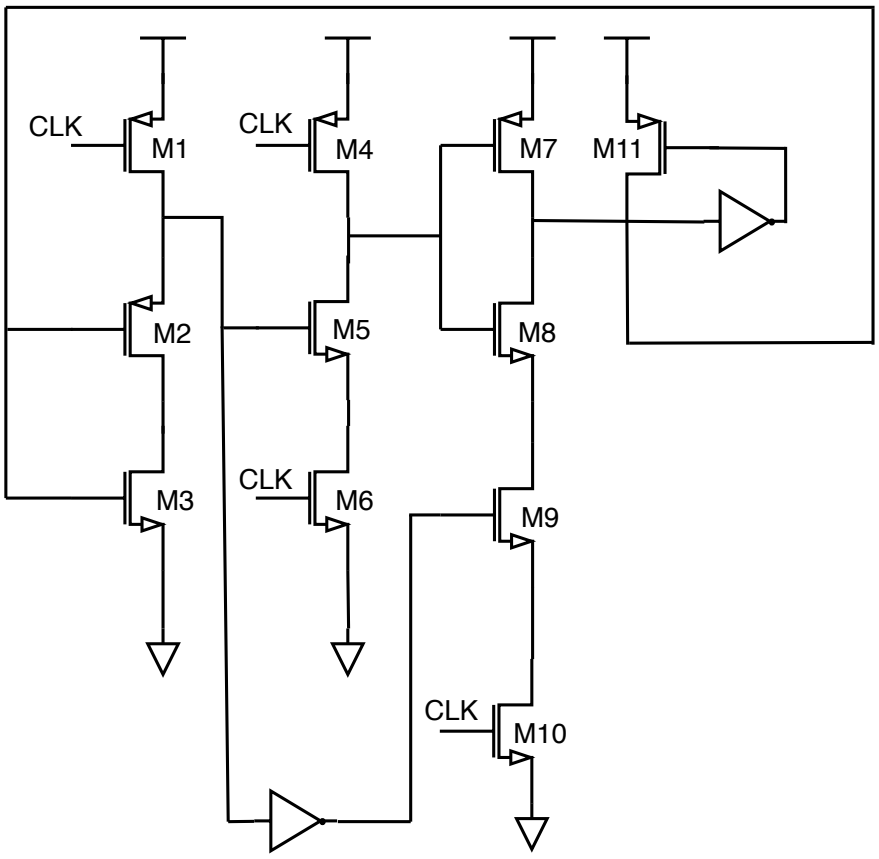


Figure 2.8: Keeper circuit added to TSPC based divider[21]

2.4.4 Phase Frequency Detector

A PFD circuit with two flip flops and a reset circuit using NAND gate is used[6] as in fig.2.9. The flip flops are TSPC based and provide the up and down signals depending on whether the input signal phase is above or below the reference phase. The PFD circuit essentially compares the phase of the input signals and provide pulses corresponding to the phase or frequency difference. The up or down signal is activated based on whether the difference is positive or negative.

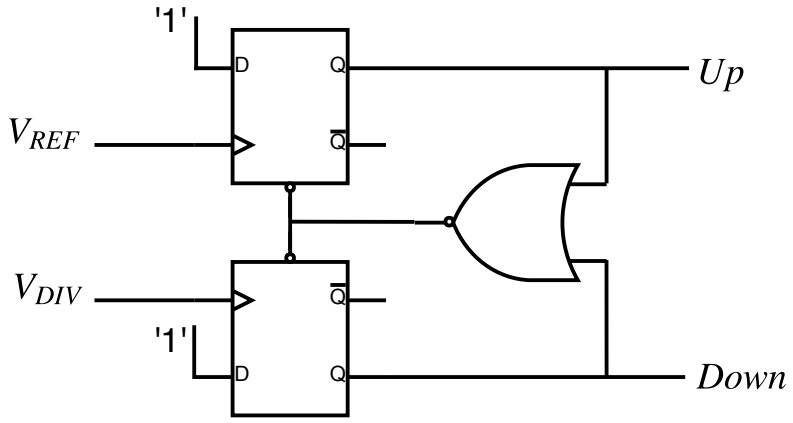


Figure 2.9: Phase Frequency Detector block diagram

When both the reference frequency and divider frequency are equal and the phase of reference frequency is more, the up signal is high with constant width as shown in fig.2.10.

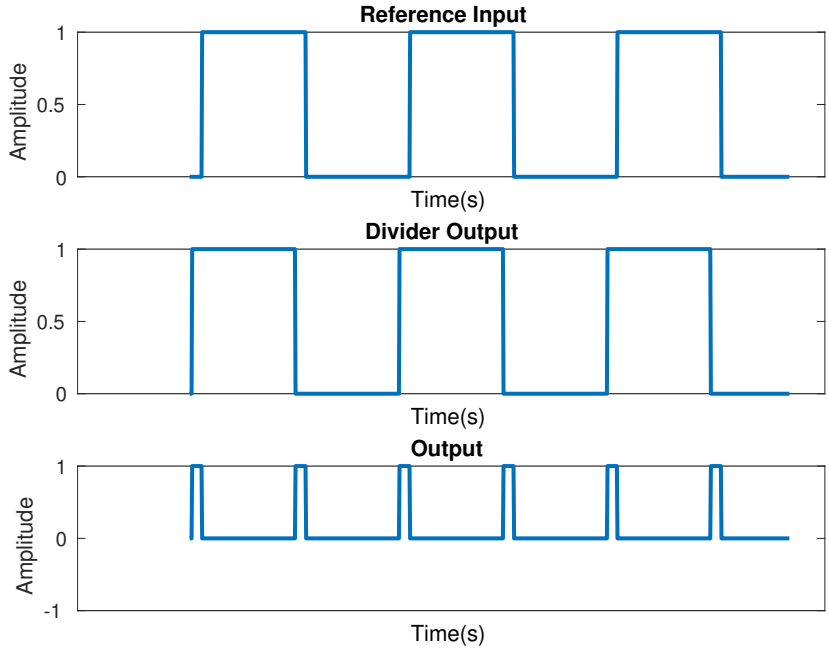
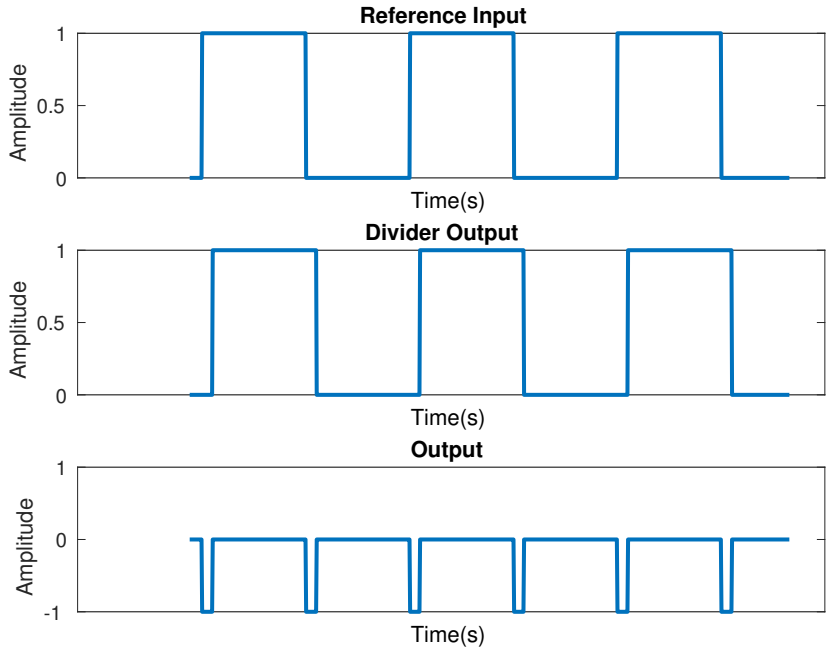
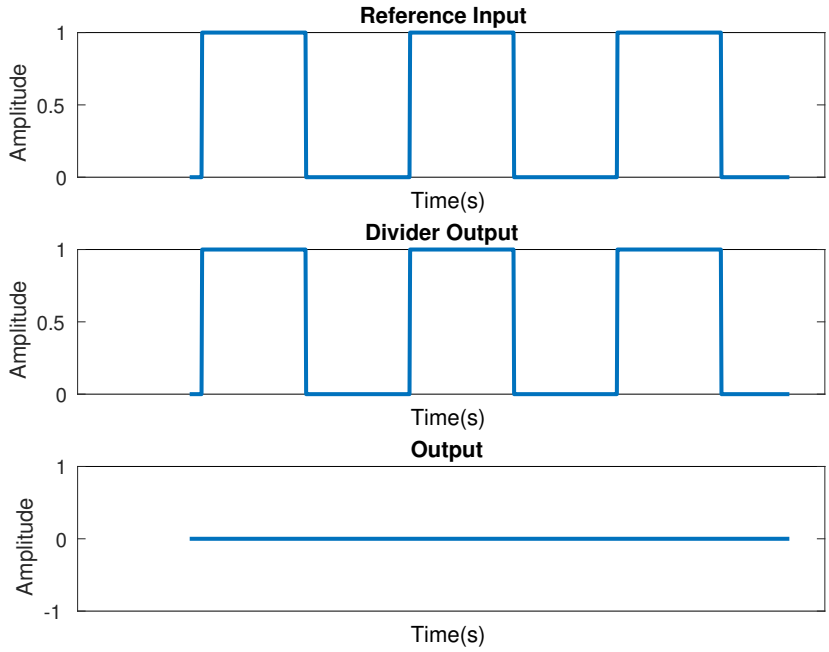


Figure 2.10: PFD output and input waveforms: $freq_1 = freq_2$, $\phi_1 > \phi_2$

When both the reference frequency and divider frequency are equal and the phase of divider frequency is more, the down signal is high with constant width as in fig.2.11a. When both the reference frequency and divider frequency as well as the phase are equal the up and down signals are low as in fig.2.11b.



(a) $freq_1 = freq_2$, $\phi_1 < \phi_2$

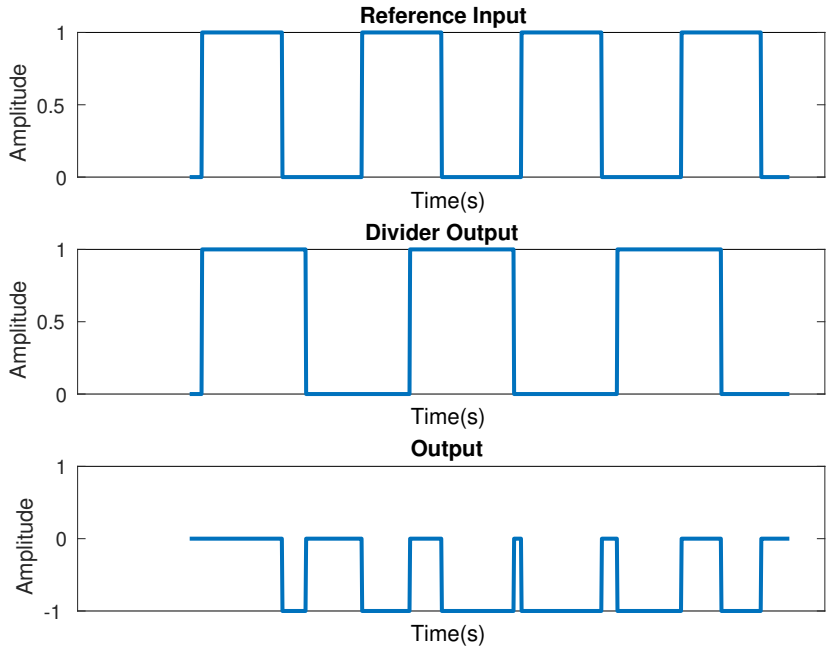


(b) $freq_1 = freq_2$, $\phi_1 = \phi_2$

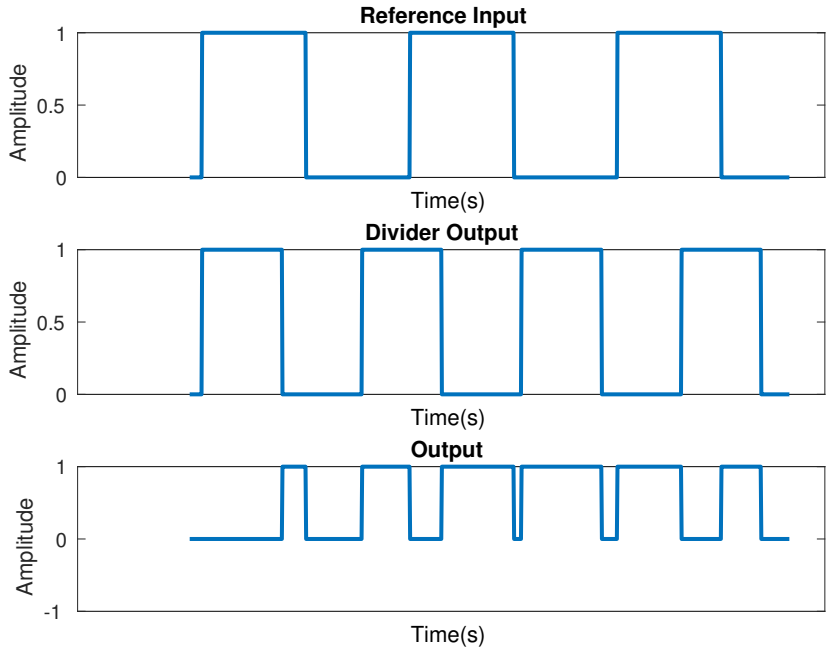
Figure 2.11: PFD output and input waveforms

When both the reference frequency and divider phases are equal and the frequency of divider frequency is more, the down signal is high with varying width as in fig.2.12a. When both the reference frequency and divider phases are equal and

the frequency of reference frequency is more, the down signal is high with varying width as in fig.2.12b.



(a) $freq_1 < freq_2$



(b) $freq_1 > freq_2$

Figure 2.12: PFD output and input waveforms(contd.)

The circuit implementation is shown in fig.2.13 and uses two TSPC based D flip flops and is re-settable via the reset inputs controlled through the NOR gate.

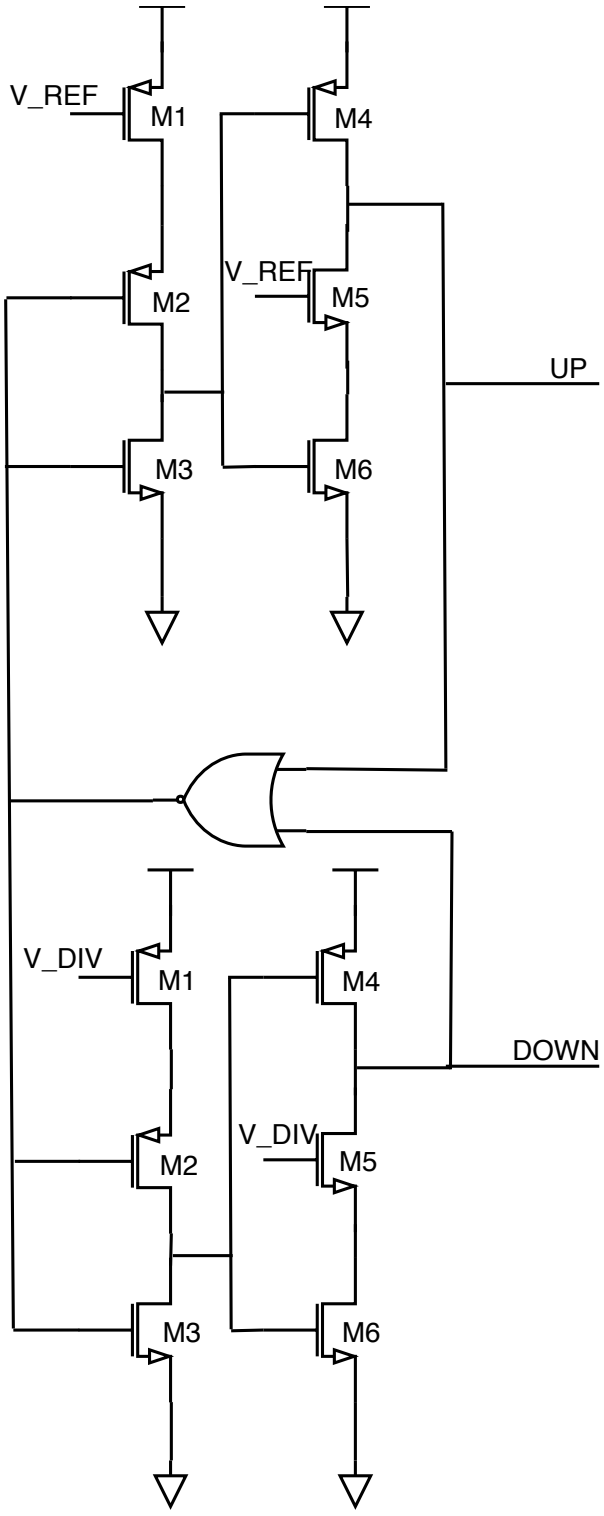


Figure 2.13: Phase Frequency Detector circuit

2.4.5 Charge Pump

The pulses provided by the PFD is converted into corresponding current pulses by the charge pump. It consists of a two switches (M_5 and M_6) toggling two current sources (M_4 and M_7). The biasing of current source is provided by the resistor R and the transistors- M_1, M_2, and M_3. M_1 and M_3 are diode connected transistors keeping the gate source voltage constant for M_4 and M_2 respectively except for the difference in threshold voltage.

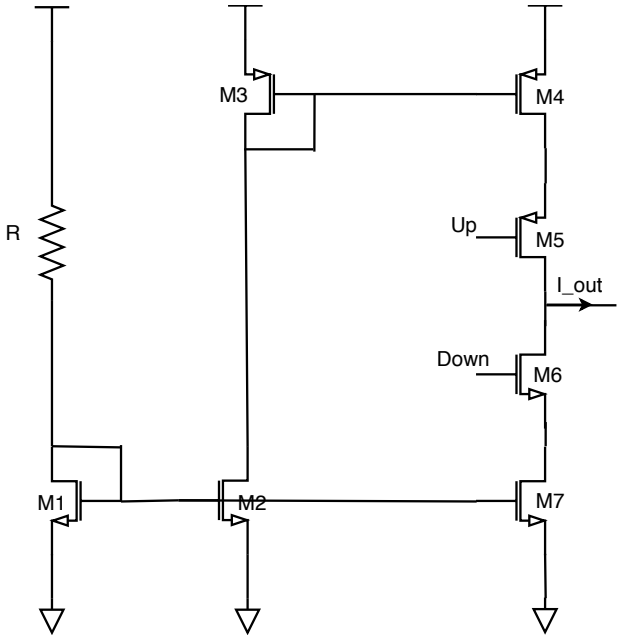


Figure 2.14: Charge Pump Circuit

2.5 Type II PLL with PFD/CP

A type II PLL is characterized by two ideal integrators in the loop; one by the VCO and the second by the charge pump together with the filter capacitor. These two integrators form two poles in the imaginary axis making it unstable and hence adding a resistor, R_1 in series adds losses leading to stability. In this configuration, PFD/CP output has ripple in the time domain which can be reduced with the help of a small capacitor in parallel to the CP output adding an additional pole[6].

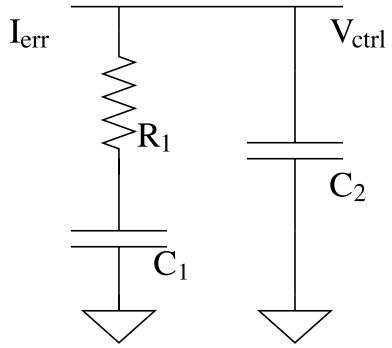


Figure 2.15: Second Order Filter

Even though there are different options for the phase detector available like XOR, multiplier based etc. the charge pump based Phase Frequency Detector (PFD) has replaced them in the recent years due to the following reasons[8].

- Ability to act as frequency detection for out of lock state and phase detection once in lock.
- Ability to respond to even small variations in phase errors.

2.5.1 Parameters

Second order systems are characterized by the damping factor (ζ) and natural frequency (ω_n). Even though the type II PLL is a third order system (two ideal integrators and a stability enhancement pole), the second order parameters can be used for design. In doing so, the stability enhancement pole is considered separately for PM calculations. The characteristic equations can be summarized as

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p}{2\pi C1} K_{VCO}} = \frac{\zeta^2 (R_1 C_1 s + 1)}{s^2 + 2\zeta\omega_n + \omega_n^2} \tag{2.3}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi}} \tag{2.4}$$

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}} \tag{2.5}$$

The poles and zeros can be expressed in terms of ζ and ω_n as

$$\omega_{p1,2} = [-\zeta \pm \sqrt{\zeta^2 - 1}]\omega_n \tag{2.6}$$

$$\omega_{p3} = \frac{C_1 + C_2}{R_1 C_1 C_2} \tag{2.7}$$

$$\omega_z = \frac{-\omega_n}{2\zeta} \tag{2.8}$$

$$PM = \tan^{-1}(4\zeta^2) - tan^{-1}(4\zeta^2 \frac{C_1 C_2}{C_1(C_1 + C_2)}) \tag{2.9}$$

For maximizing the PM, and to avoid instability the ω_{p3} is selected at 5 to 10 times ω_n and the the following inequalities are valid[6].

$$C_2 \leq 0.2C_1 \tag{2.10}$$

$$R_1^2 \leq \frac{2\pi}{I_p K_{VCO} C_{eq}} \tag{2.11}$$

The order of the PLL system is one plus the filter order and affects the steady state as well as the transient response of the system. The steady state error for step, ramp and parabolic change in reference phase is zero for a third order PLL. To obtain minimum steady state phase error, a third order PLL is needed and hence a second order filter is used for the system.

In this work, the Bode plot is used for the closed loop system response visualization and the calculation of phase margin. As mentioned before, the second filter capacitor has the role of increasing the phase margin but the lock time is increased.

2.6 Technology Details

For the design simulations, the 22 nm FDSOI platform from Global Foundaries called 22FDX^{TM} is used. The FDSOI stands for Fully Depleted Silicon on Insulator and is characterized by a reduced bulk region separated from the substrate using a buried oxide layer known as BOX layer.

The presence of BOX layer enables the usage of back gate biasing through body for reduced threshold voltage (FBB/Forward Body Bias) or reduced power consumption (RBB/Reverse Body Bias). Moreover some of the parasitic effects of the active regions to the body (substrate effects) are reduced due to the BOX layer lowering the substrate losses in passives such as inductors and varactors. Global Foundaries offer the base PDK along with extensions for rfa (radio frequency and analog) which is used in this work.

3
Design

In this chapter we describe the design procedure used for the various sub components in the PLL design. This is accomplished with the help of Cadence simulations with the 22FDX library from Global Foundaries.

3.1 Design Philosophy

We used a top-down and bottom-up approach in the project. In this approach, we made a top-down design using the MATLAB system models. We did this with the help of initial parameter values from previous experience and literature survey in order to calculate the loop filter parameters using MATLAB scripts. Then we did the circuit simulations from bottom up using transistor level SPICE simulations in Cadence.

3.2 System design of PLL

We used the linear model of PLL for low phase deviation approximation explained in section 2.3. MATLAB scripts provide the system transfer function using the sub component transfer functions. We verified the scripts with the help of numerical example from [6]. The unknown parameters are the loop filter passives calculated based on the system design parameters - damping factor, input frequency, output frequency, charge pump current and VCO gain.

A LabVIEW GUI controls the design requirements and visualize the results. This is shown in fig.3.1. The system parameters are damping factor (ζ), input frequency (ω_{in}) and output frequency (ω_{out}). The circuit design parameters are loop filter passives (R_1, C_1, C_2), charge pump current (I_p) and VCO gain (K_0).

For initial calculations, we used the estimated system parameter values from section 2.3 for initial calculations. We replaced these values with the values from circuit simulations at the final stage to obtain the correct loop filter parameters. The phase margin column indicates the stability of the loop and the design is expected to have a phase margin value of more than 50^0. For the initial run of the GUI, the "calculated" button is disabled to see the results in "outputs" columns. Enabling the "calculated" button loops back this value to see how much phase margin we have and slight change of the loop parameters is possible afterwards.

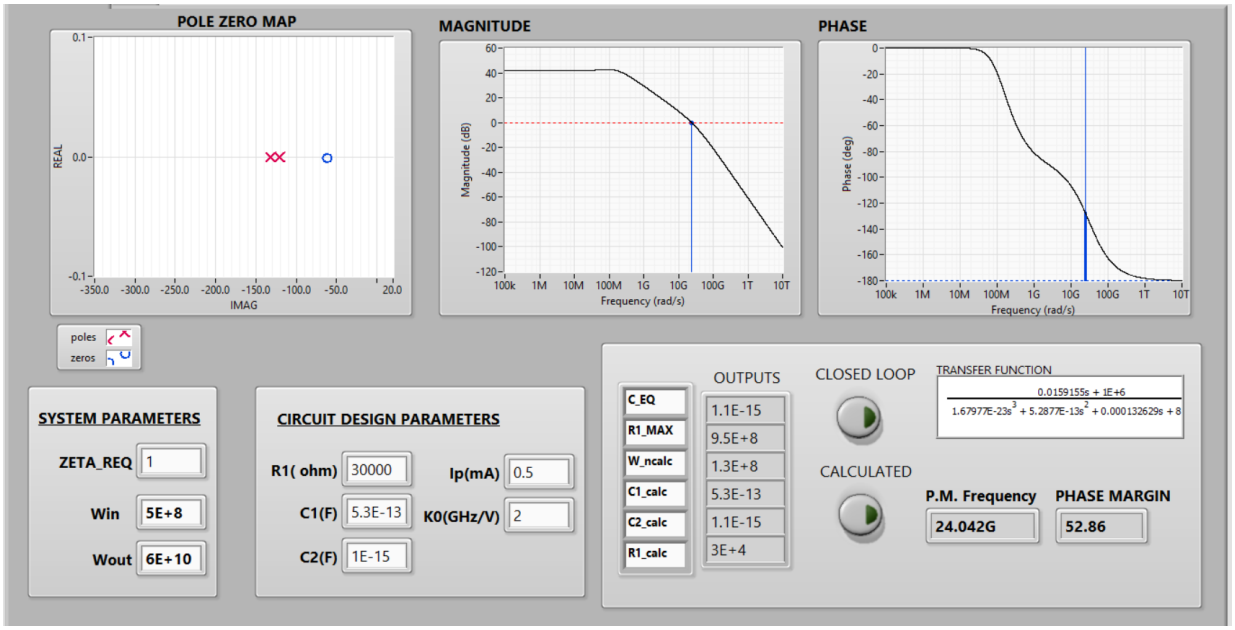


Figure 3.1: PLL system design GUI in LabVIEW

3.3 Circuit Design

The circuit design comprises the bottom up phase and we used a systematic approach of designing the subsystems by building individual component. The circuit limitations, theory of operation, how each component affects the performance etc. gives insight to the designing of each component. The presence of parasitics also complicates a closed form solution for these circuits. The systematic approach gives good learning outcomes. The design kit provides layout verified models for the RF and mm wave components. We used the 9-metal-layer stack called Layer 11 for the simulation.

Cadence provides the analog design environment and the data visualization environment under the brand name of Virtuoso Analog Design Environment (ADE) and Virtuoso Visualization and Analysis Tool Virtuoso Visualization and Analysis Tool (ViVA) respectively. Cadence provides the simulator engine for RF circuit simulation under the name of Spectre RF.

The design phase consists of creating the test bench in schematic window, obtaining required performance of the component by varying the device parameters, setting up the analysis method in ADE and visualizing the results in Virtuoso ViVA. The following analysis methods are used in the simulation[23].

DC : In the DC analysis, the operating point of the device is obtained. In addition, the parasitic information can be obtained if the option for saving all the parameters for the device is selected in the ADE window.

TRAN : TRAN stands for the transient simulation and provides the time variation of the signals from the nets and ports selected in the schematic.

PSS : PSS stands for periodic steady state analysis and calculates the steady state response to a time varying input. Spectre RF provides two methods for PSS.

1. Shooting method : This method is also known as Newton method and is

a time domain method. This method is suggested for circuits with sharp transitions such as ring oscillators and circuits with digital elements such as dividers.

2. Harmonic Balance (HB) method : This method is a frequency domain method. It is recommended for mildly nonlinear circuits such as LC oscillators and circuits with distributed components such as transmission lines.

PNOISE : PNOISE stands for periodic noise analysis and is a time domain method. It computes the noise generated by the various components in the circuit after considering the effect of periodically time varying bias point.

3.3.1 Design of VCO

One can design the VCO for low power as well as low phase noise. Both requires different strategies for passive selection and transistor sizing[24]. In this project, the focus is on the low power design. We started with the passive design for resonance and tuning range, the cross coupled pair and tail current design for sustained oscillation, and the filters for removing harmonics as discussed in section 2.4.1.

Inductor Design

The inductors demonstrates a phenomenon called self resonance in which the parasitic capacitance of the inductor causes a resonance. This affects the performance of the oscillation and the size of the inductor is selected such that the self resonant frequency (f_{sr}) is at least twice the operating frequency, i.e $f_{sr} \geq 120\,\text{GHz}$.

Since the amplitude of oscillation is proportional to the tank impedance (ωL), it is better to select maximum inductance so that the output voltage swing is also maximized. However, the Q factor of the inductor at this point may not be the best and hence degrades the phase noise.

A Cadence utility available which plots the inductor parameters from the property window through which we can get the Q factor and inductance values. The self resonance frequency can be observed as a peak in inductance and sudden reversal of value indicating a capacitance effect. The Q factor is in the range of 25-35. The final sizing is consolidated in table 4.2 after iterations for meeting the VCO specifications.

Varactor Design

The 22FDX library offers MOSFETs in nwell as varactors. This is advantageous for improving the tuning range and for overcoming the non-monotonic behaviour compared to MOS varactors on pwell[6]. The MOSFETS in nwell will not enter into strong inversion and hence has better tuning range. The super low threshold voltage nFETs (slvtnfet_6t) is used which has the following parameters.

- Length of the ncap channel
- Width of the ncap channel
- Number of gates

By decreasing the channel length, the channel resistance can be reduced improving the Q factor. However, the gate-source and gate-drain overlap capacitance reduce

the tuning range. Also, the gate width can be divided to multiple fingers to reduce the gate resistance. The test bench consists of two series varactors with a DC voltage of 900 mV at the signal ends, an AC voltage of 1 V amplitude at one end and the control voltage at the common terminal. This simulates the expected condition of the varactor in the circuit. A parametric sweep provides the capacitance and the Q factor variation calculated using the formula

$$\begin{aligned} C &= \Im(\frac{I_c}{2\pi V} \times f_{osc.}) \\ Q_{var} &= \frac{\Im(V/I_c)}{\Re(V/I_c)} \end{aligned} \tag{3.1}$$

where V is the applied voltage in test bench. We verified the test bench using an ideal known capacitor. The varactor Q factor is in the range of 4-5 and is poor compared to that of the inductors.

The total Q factor of the tank is given by

$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{3.2}$$

Thus the Q factor of the tank is limited by the varactor[24] for this technology. The sizing for the varactors is consolidated in table 4.2.

Tail current source design

We used a tail current of 2 mA for initial calculations based on the low power design requirement and literature survey. Since the tail transistor is not directly connected to the output node, sufficient channel length is used to improve the output resistance needed for the current source. The DC simulation in ADE provides the DC current for a given bias voltage. The size is tabulated in table 4.2.

Cross coupled pair design

The cross coupled pair sizing should be such that the parasitics loaded to the tank is minimum and at the same time the oscillation starting condition of $g_m R_p > 2$ is satisfied[6]. Multiple iterations of sizing of all the components are needed at this point and the circuit simulation results are used to arrive at a closed form result. However, an initial passive sizing and the tail source sizing reduces the effort in big optimization runs.

The oscillation frequency, amplitude of oscillation and phase noise requirements mentioned in section 1.2.1 are kept as the targets. The TRAN analysis is used to confirm oscillation in time domain. The PSS and PNOISE is used for obtaining the spectrum and the phase noise values. The final sizing satisfying the design requirement is consolidated in table 4.2.

Tail filter design

Based on the insights of the working of tail filter mentioned in section 2.4.1, the inductor is first inserted. The amplitude of the second harmonic at the output node

is reduced with the help of this inductor and hence the sizing is obtained by a sweep for minimum amplitude of the 120 GHz signal at the output node. After this, the tail capacitor is placed parallel to the current source for filtering the higher order harmonics in the tail current source. The sizing is consolidated in the table 4.2.

Transistor	Size (W/L)
M_1	30 µm/18 nm
M_2	25 µm/18 nm
M_3	25 µm/18 nm
M_4	45 µm/24 nm
M_5	45 µm/24 nm
L	6 µm wide× 70 µm dia.
L_{tail}	6 µm wide× 25 µm dia.
C_{tail}	0.75 pF

Table 3.1: VCO component sizes

The sizing mentioned in table.4.2 is after the connection of ILFD at the output as this affects the tuning frequency also.

3.3.2 Design of ILFD

ILFD design follows an oscillator design at 30 GHz by scaling up the tank components and the active devices follows a mixer design. By injecting the external signal, the oscillation can be sustained. Also, slight tuning of the ILFD tank components are needed for obtaining the exact lock. The phase noise curve at the ILFD output confirms the locking of the circuit.

Transistor	Size (W/L)
M_1	6 µm/20 nm
M_2, M_3	25 µm/18 nm
M_4, M_5	90 µm/24 nm
M_6	6 µm/20 nm
L	6 µm width × 60 µm dia. (2 turns: 4 µm spacing)
R_{bias}	1kΩ
C_{bias}	100 fF

Table 3.2: ILFD component sizes

3.3.3 Design of prescaler

The TSPC based divider is designed for divide by 64 stage for achieving the signal for comparison with the reference signal. This is achieved with the help of a series of 6 divide by two stages. The sizing is obtained by scaling down of the sizing mentioned in [21] and is consolidated in table 3.3.

Transistor	Size (W/L)
M_1	2 µm/20 nm
M_2	1.1 µm/20 nm
M_3	0.9 µm/20 nm
M_4	2.6 µm/20 nm
M_5	3.1 µm/20 nm
M_6	6.2 µm/20 nm
M_7	2.2 µm/20 nm
M_8	1.8 µm/20 nm
M_9	2.6 µm/20 nm

Table 3.3: Prescaler component sizes

All the five transistors - three in the keeper circuit (M_{11} and two in the inverter) and two in the intermediate inverter in fig.2.8 are sized at the minimum width and length (300 nm/18 nm).

3.3.4 Design of PFD

The sizing for the PFD was obtained from the detailed study done by Razavi[25] for low phase noise. The sizing is consolidated in table 3.4.

Transistor	Size (W/L)
M_1, M_2	1.4 µm/20 nm
M_3	12 µm/20 nm
M_4	25 µm/20 nm
M_5, M_6	10 µm/20 nm

Table 3.4: PFD component sizes

3.3.5 Design of CP

The charge pump is a basic current mirror with two switches and the components are designed for a reference current of 1 mA and a CP current of 2 mA. The sizing is consolidated in table 3.5.

Transistor	Size (W/L)
M_1	2 µm/20 nm
M_2	2.2 µm/20 nm
M_3	6.2 µm/20 nm
M_4	14.7 µm/20 nm
M_5	13.5 µm/20 nm
M_6	5 µm/20 nm
M_7	4.6 µm/20 nm
R	290Ω

Table 3.5: CP component sizes

4

Results

This chapter discusses the results of system simulation in MATLAB and circuit simulation in Cadence using the GF 22FDX library.

4.1 System simulation

We got the loop filter passives from the system level simulation using MATLAB. We used the system and circuit parameters from the literature survey for the first cut design and is later replaced with the actual circuit parameters from the Cadence simulation results. They are consolidated in table 4.1 for the filter circuit in fig.2.15.

R_1	2.3 kΩ
C_1	7.6 pF
C_2	15 fF

Table 4.1: Loop filter component values

We used the Bode diagram of the closed loop response of PLL system model to study the system simulation as shown in fig.4.1. We verified the phase margin requirement of 50^0 at the reference frequency of 468 MHz.

The use of second capacitor, C_2 is evidently visible in the plots as a notch in the response improving the phase margin. The closed loop response is shown in 4.1 and open loop response in 4.2. The overshoot can be seen in the step response plot for the closed loop PLL system in fig.4.3.

The PLL system response in fig.4.3 signifies two parameters for the PLL-the settling time (1.7us) and the settling value which is equal to the division ratio (64).

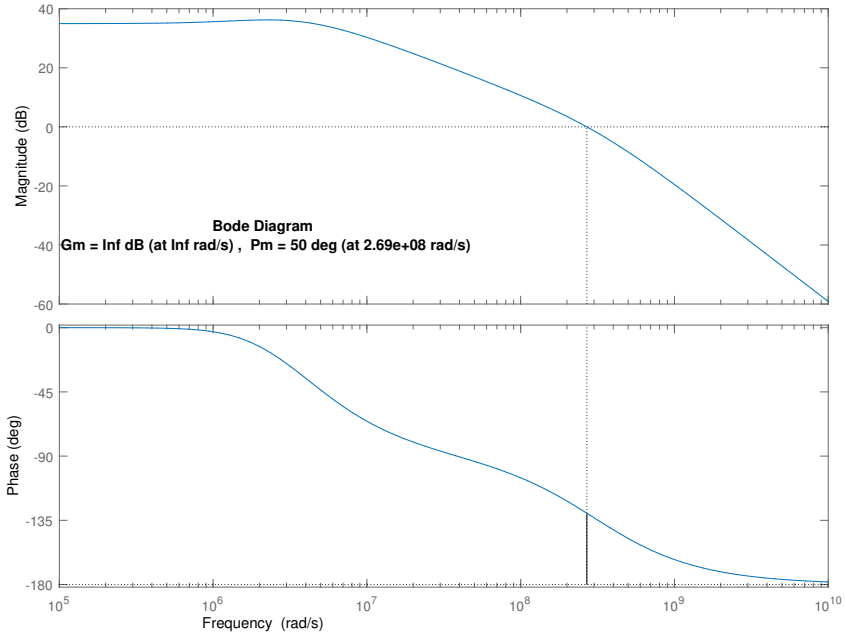


Figure 4.1: PLL closed loop response

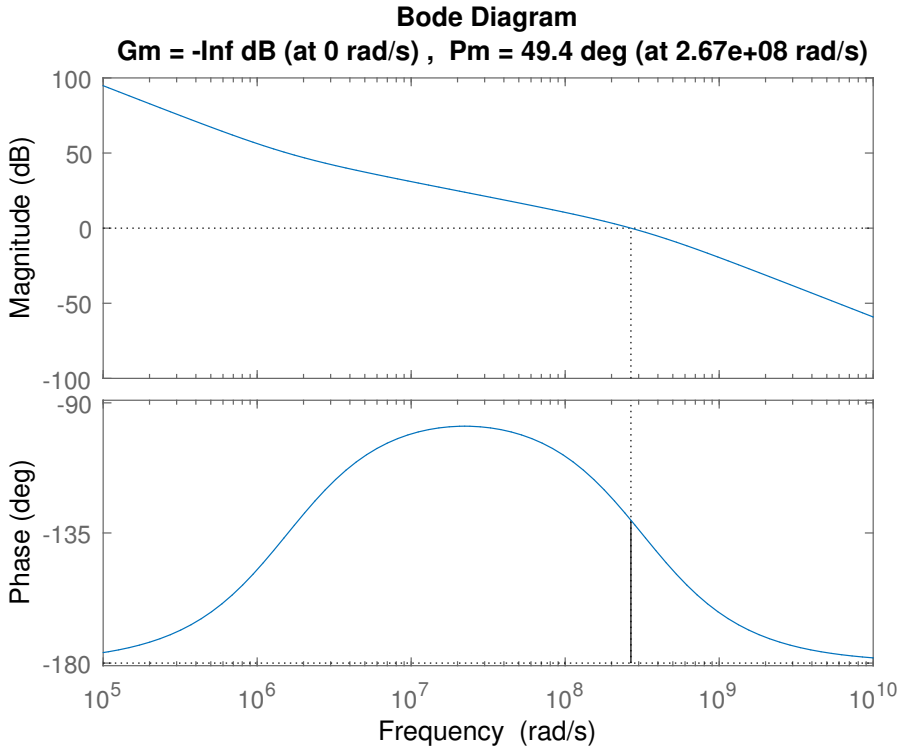


Figure 4.2: PLL open loop response

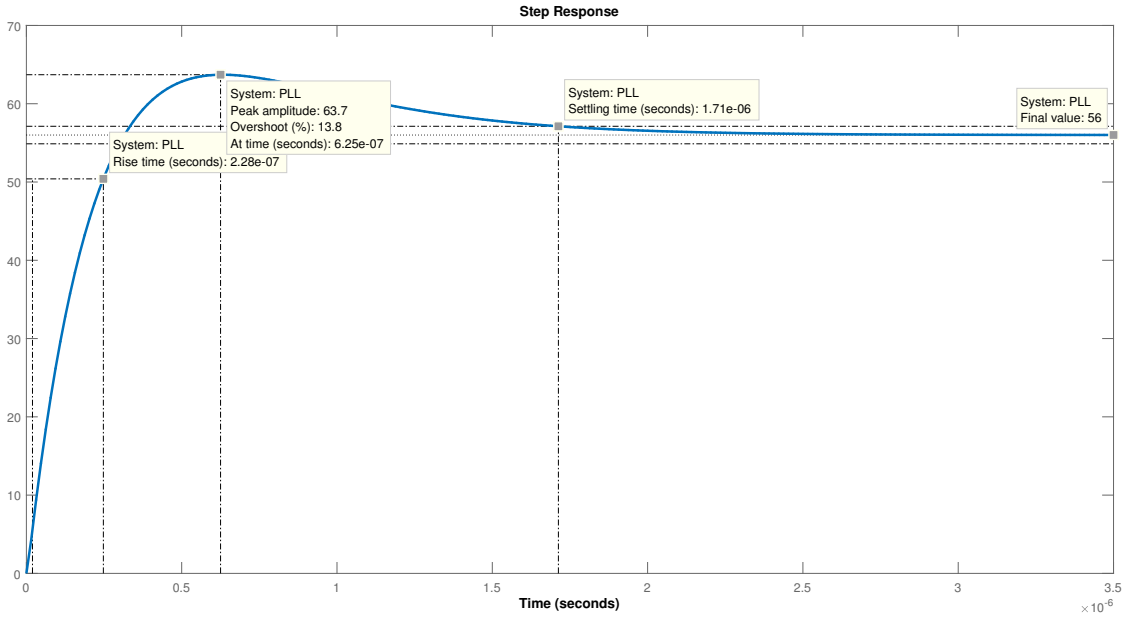


Figure 4.3: PLL system step response

4.2 Circuit simulations

We used multiple runs of subsystem level circuit simulations before arriving at the final design closure. The circuit simulation results of the subsystems and the PLL system are consolidated below.

4.2.1 VCO with ILFD

The output signal waveform is observed in the transient simulation for a swing of 1.2V and a tuning range of 6 GHz. This is further verified in the Periodic Steady State analysis. The phase noise is plotted as in fig.4.4. The phase noise is expressed in dBc Hz^{-1} which expresses the noise power with respect to the carrier power at 60 GHz. As observed in fig.4.4, the noise power decrease monotonically as one observe away from the carrier frequency. For comparison purpose, the phase noise at a frequency offset of 1 MHz is specified.

The figure of merit (FoM) is 179 dB (worst case) and the tuning frequency for the VCO is 54 GHz to 60 GHz when the control voltage is swept from 0 to 900 mV. The VCO results are consolidated in table 4.2.

PN@1 MHz	−82 dB to −90 dB
Figure of Merit	−179 dB to −180 dB
Voltage Swing	1.2 V
Frequency	54 to 60 GHz
Power Dissipation	6 mW

Table 4.2: VCO results summary

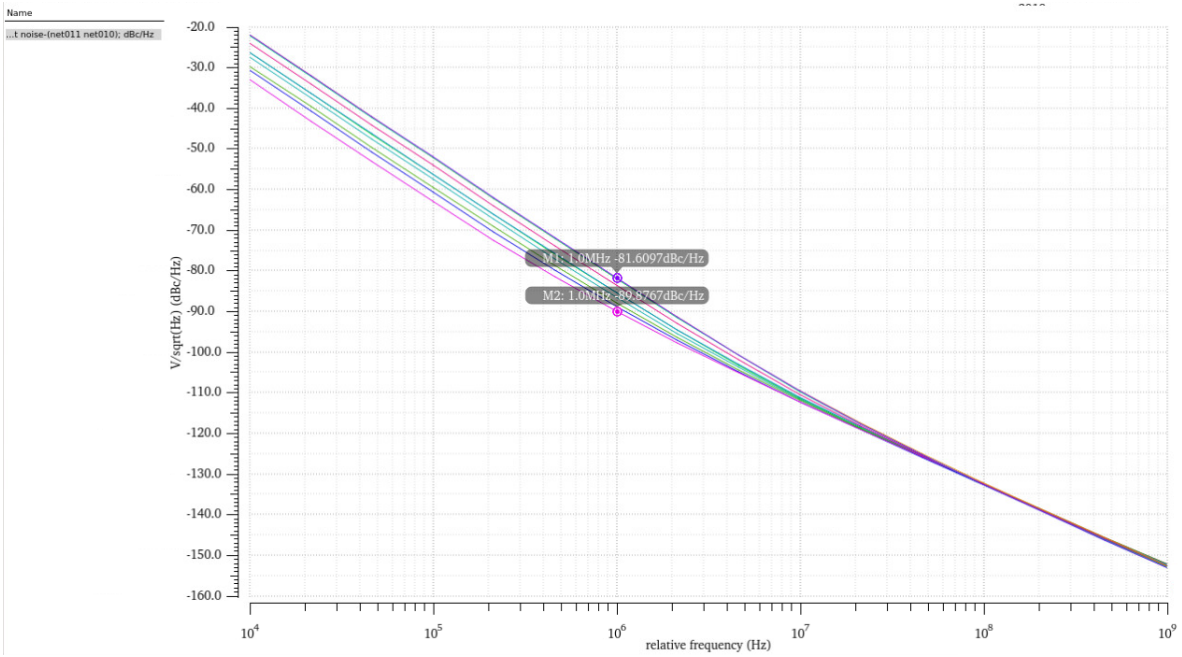


Figure 4.4: Phase noise plot of VCO

For the ILFD, a 6dB improvement in the phase noise is expected as mentioned in section 2.3.2. This is confirmed in the phase noise plots of fig.4.6. The tuning of ILFD using the control voltage causes the frequency change from 27 GHz to 30 GHz as shown in fig.4.5. The results are summarized in table 4.3. These results are after the connection of VCO circuit to the injection ports. The DC bias of 300 mV is used for the simulations and hence a low power of 2 mW is consumed.

PN@1 MHz	−88 dB to −96 dB
Voltage Swing	900 mV
Frequency	27 GHz to 30 GHz
Power Dissipation	2 mW

Table 4.3: ILFD results summary

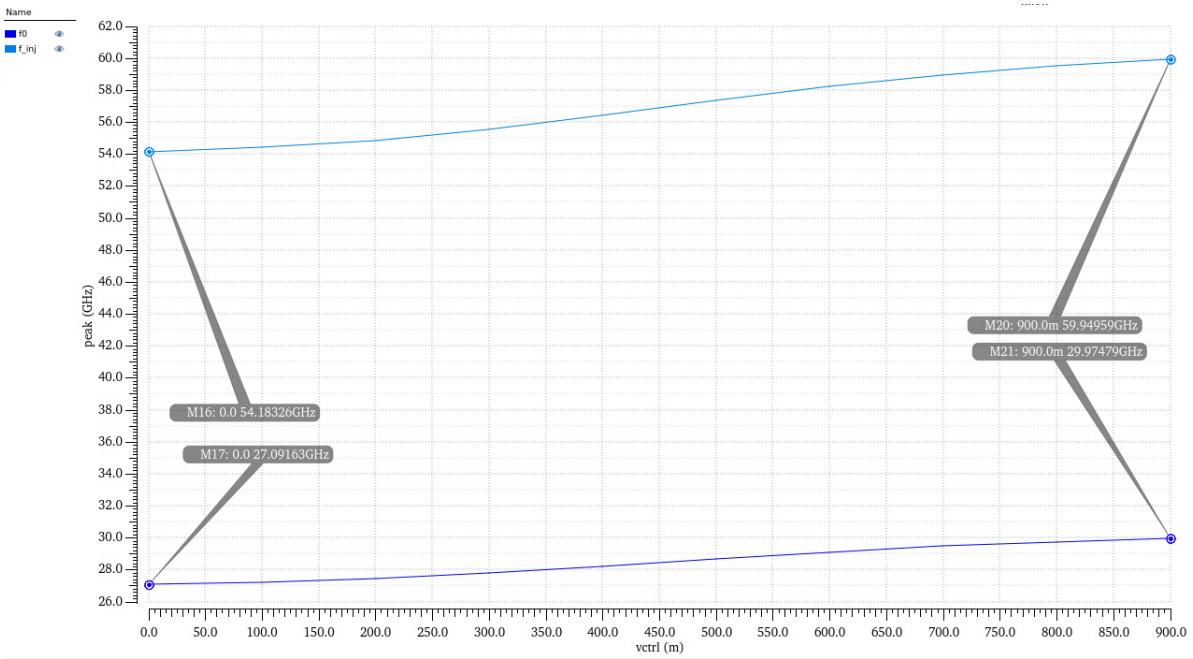


Figure 4.5: Tuning of ILFD and VCO frequency by control voltage variation

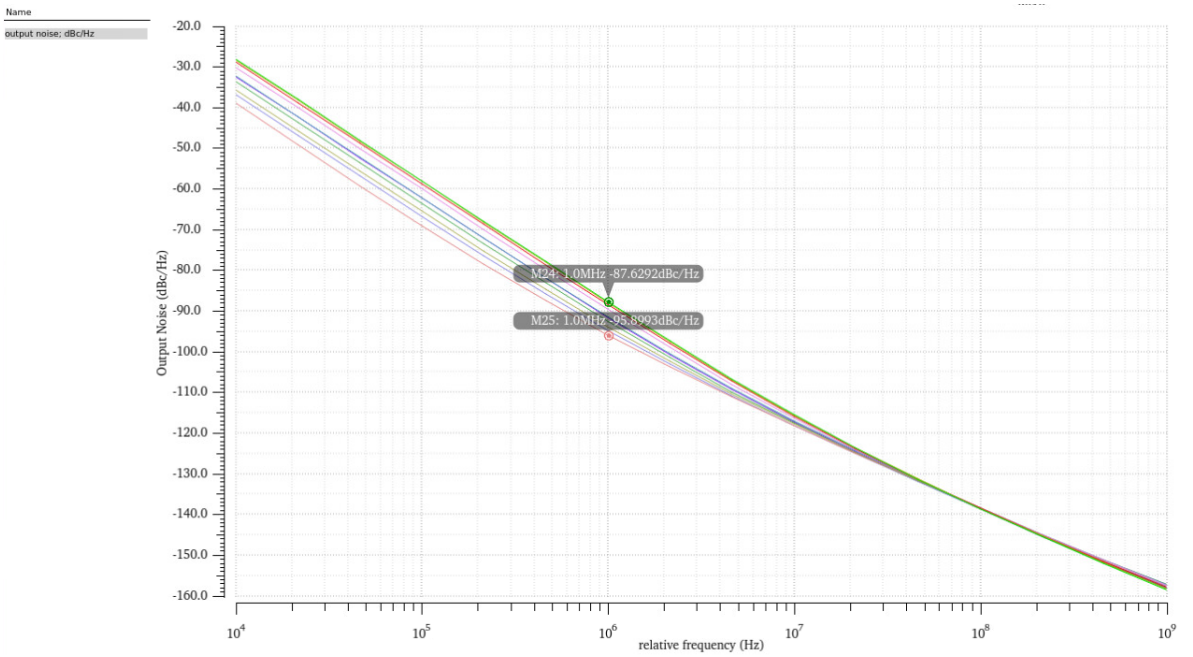


Figure 4.6: Phase noise in ILFD output

4.2.2 Divider

The divider accepts input at 30 GHz and converts it into 478 MHz by dividing the input by 64. A transient (TRAN) simulation before connecting the keeper circuit shows the amplitude dropping effect as shown in fig.4.7. After connecting the keeper circuit, this is solved as shown in fig.4.8.

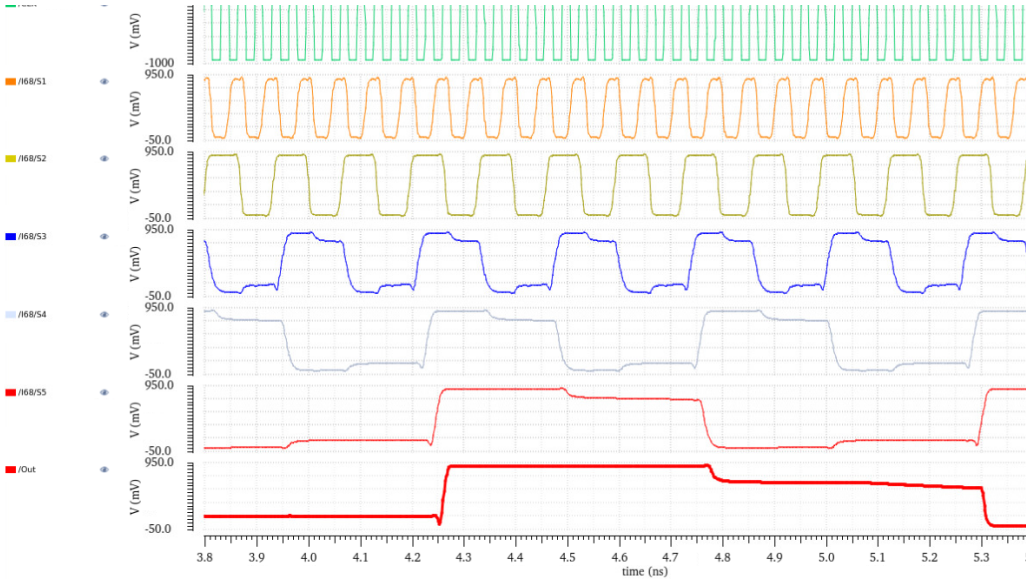


Figure 4.7: Divider chain waveforms (Without keeper): Input clock, stages 1 to 6 output waveforms

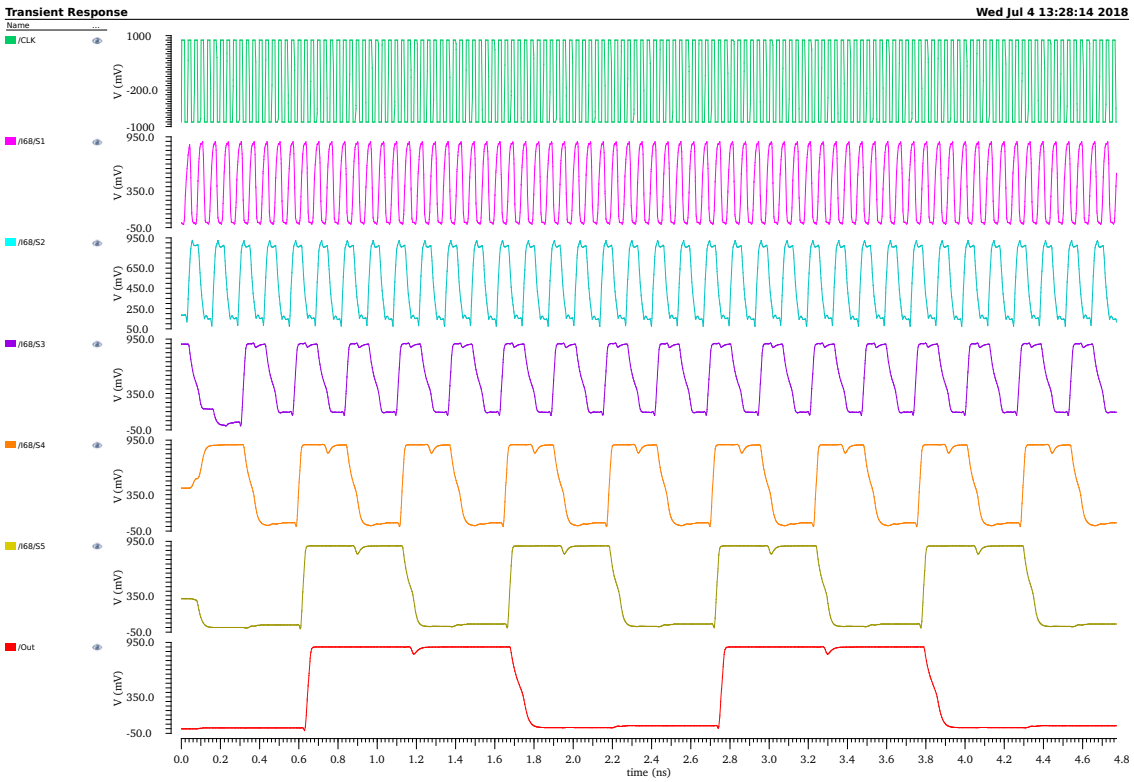


Figure 4.8: Divider chain waveforms (With keeper): Input clock and stages 1 to 6 output waveforms

4.2.3 PFD, CP and loop filter

The charge pump is tested with the help of injecting a DC voltage at the output node to simulate the changing control voltage and activating the up and down signals to simulate the PFD output separately. The charge pump current of 2 mA is confirmed for both the cases as shown in fig.4.9.

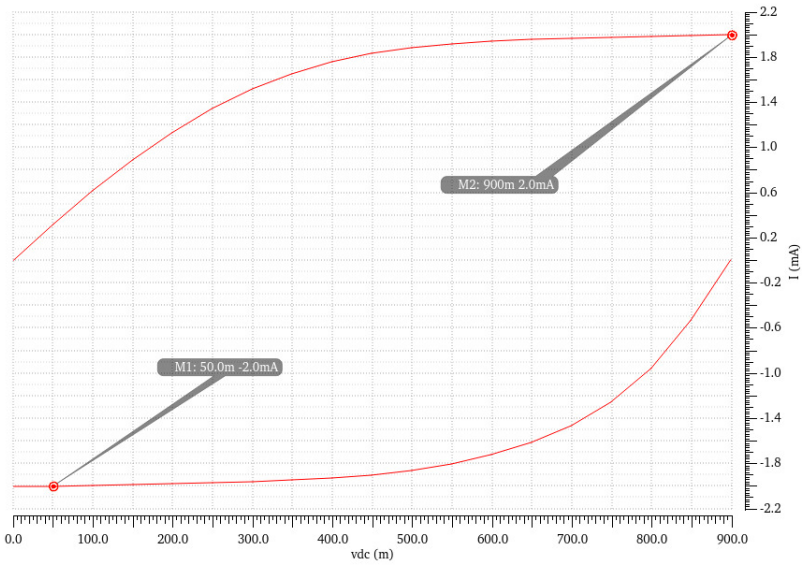


Figure 4.9: Charge pump current for Up (top) and Down (bottom) signals activated

The PFD, CP and loop filter in cascade is tested in transient simulation. Input reference frequency is changed in order to get the output filtered control voltage.

The control voltage waveform for the three different conditions is shown in fig.4.10.

4.2.4 PLL closed loop responses

After the testing of individual subsystems, the entire PLL is simulated using transient (TRAN) analysis. The simulation is run with the reference frequency at the initial free running frequency of the divider (490 MHz) calculated from the ILFD oscillation frequency obtained in the design.

The control voltage settling is observed to ensure the PLL lock. The control voltage settles to 100 mV$\pm$10 mV at 1.4 µs demonstrating the lock as shown in fig. 4.11. This agrees with the system simulation result of 1.76 µs settling time.

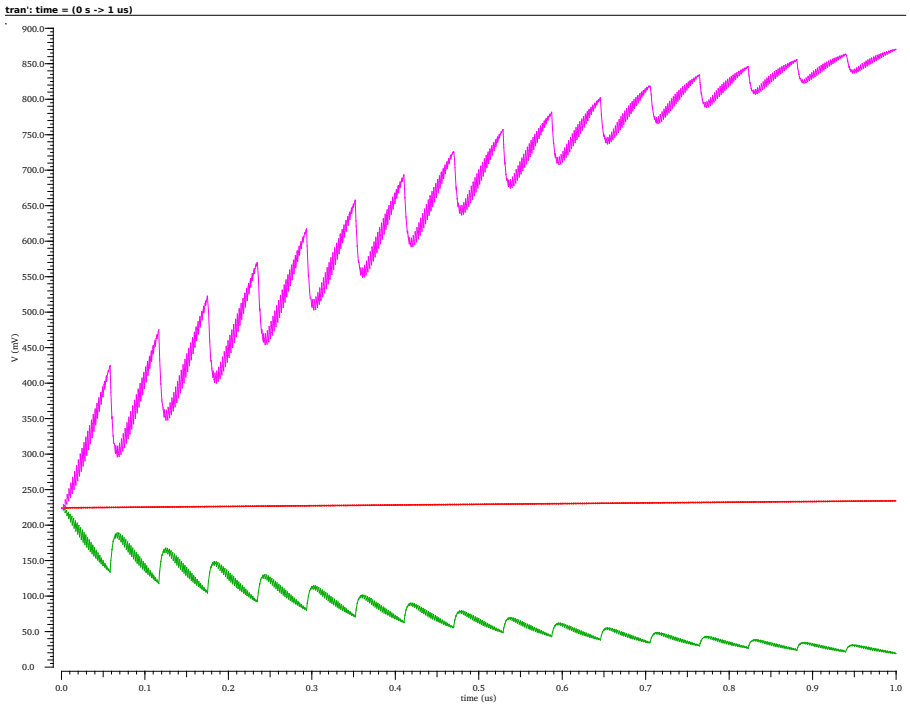


Figure 4.10: Control Voltage for $f_{div} < f_{ref}$ (Pink) b. $f_{div} = f_{ref}$ (Red) c. $f_{div} > f_{ref}$ (Green)

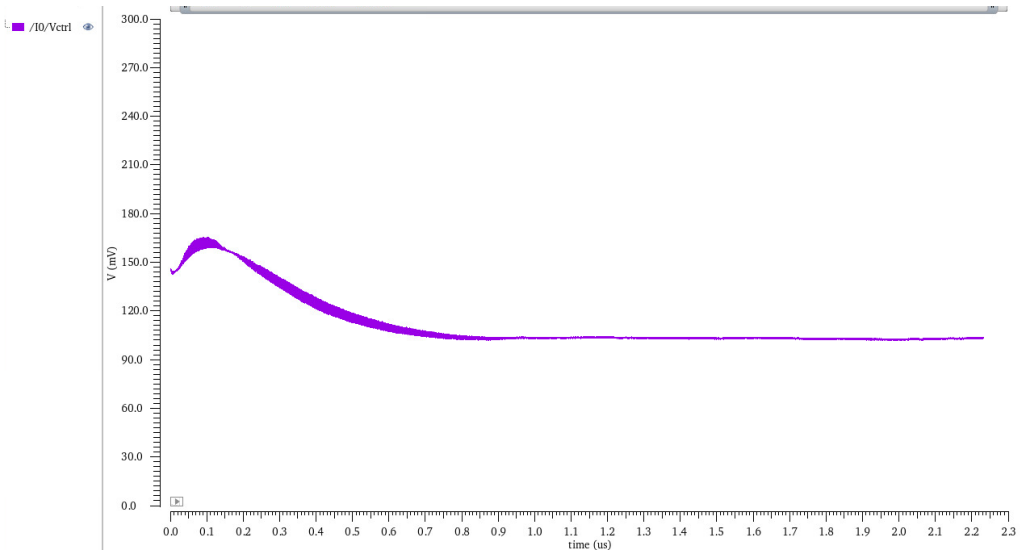


Figure 4.11: PLL control voltage at the input of VCO

4.3 Results discussion

The overall Phase Locked Loop is successfully closed as indicated by the control voltage settling in fig. 4.11. The complete system parameters of this work are compared in table.4.4 with a 65 nm implementation with identical architecture (but with

CML based divider) as this work[26] and a 22 nm implementation with a different topology (24 GHz PLL and a frequency tripler).

Specification	[26]	This work	[27]
PLL Locking Range	56.8–66.5 GHz	54.2–60 GHz	71–76 GHz
Technology Node	65 nm	22 nm	22 nm
PLL architecture	LC VCO : CML divider chain : PFD CP : Second Order RC filter	LC VCO: LC ILFD: TSPC divider: PFD CP : Second Order RC filter	24 GHz subsampling PLL + IQ frequency tripler
Reference Frequency	234 MHz	468 MHz	2.4 GHz
Settling time	< 1 µ sec	< 2 µ sec	< 6 µ sec
Supply voltage	1.2 V	1.2 V	Not available
Power Consumption			
VCO	5.6 mW	6 mW	Not available
Pre-scaler	13.2 mW	2 mW	Not available
Divider chain	9.6 mW	1.4 mW	Not available
PFD & CP	1.8 mW	Not available	Not available
Total	30.2 mW	12 mW	30 mW

Table 4.4: Comparison of PLL results of this work with others

The work in [26] is identical to my work but in a different technology node (65 nm). The power savings is evident in the divider chain and the ILFD in my work. This may be due to the usage of Current Mode Logic (CML) which has the advantage of being fast and power hungry[6].

The work in [27] has a different topology but uses the 22 nm technology for implementation. A 24 GHz quadrature PLL is used along with a frequency tripler to generate a 71 GHz output signal. The power consumption is identical to that in [26] and both are almost 3 times as high as my design. However, the results cited in [26] and [27] are based on measurement results and the results shown in this work is based on simulation results. Hence chip tapeout and measurements are necessary for actual comparison.

5
Conclusion

In this work, the design of a Phase Locked Loop (PLL) at 60 GHz/30 GHz signal is presented. We used a top-down and bottom-up approach in which the system simulation and circuit simulation are used together to understand the trade-offs. The whole process from literature study to schematic-based circuit implementation has been documented. The circuit has been implemented in a 22nm FDSOI CMOS process.

We attempted a new way of injection at the output of the VCO for a symmetric injection. This topology has an additional benefit of reduced phase noise due to the symmetric injection. However, additional simulation runs are needed for looking into the specific performance improvements to the overall PLL design. Comparison with contemporary works[26][27] indicates my implementation has lower power consumption, at least in simulation. However, actual measurements after chip tapeout is necessary to make a final conclusion.

During the initial planning phase itself the scope of the thesis work was limited to design alone and it proved useful to focus on the design issues. I faced major hurdles in terms of report making mainly in judging the level of details that need to be available in the document.

For future improvements, the layout will be a first priority to see how the results change. Also the performance improvement, if any, due to the proposed ILFD injection need to be proven in silicon by tape-outs and measurements.

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