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Auto-Calibrating Fast Digital Integrator for Magnetic-Field Measurement

Master's Thesis in Embedded Electronic System Design

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Master's thesis 2018

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A high-precision device for magnetic field strength measurement at CERN

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Abstract

The trajectory of particle beams in the large hadron collider (LHC) of CERN depends on the magnetic field in the LHC. The magnets in the LHC are tested and characterised to study the field quality, strength, direction etc. The field strength is measured in realtime using a digital integrator with an analog acquisition system. This analog front end suffers from offset and gain errors due to manufacturing and non-manufacturing variations resulting in measurement errors. Inaccuracies and drawbacks related to magnetic measurements at best decrease the performance of the integrator and at worst result in loss of beam. This thesis work aims to design an integrator with real-time calibration to identify and correct such systematic errors. The calibration involves determining coil attenuation using ratiometric method, designing potentiometer interface for DAC and implementing best-fit line to correct gain and offset errors of ADC. The calibration system conditions the signal before the start of integration and is critical for the integrator's accuracy. Results show that the calibration system ensures a high degree of accuracy, limiting the output variation to 2.17 least-significant bits (LSB). This sytem, when coupled with trapezoidal integrator, registered an average accuracy of 1.74 LSB, an order of three improvement in comparison to the previous version of the integrator.

Keywords: rotating coil, magnetic field measurement, best-fit calibration, ratiometric measurement, trapezoidal integrator.

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Trishna Rajkumar
Gothenburg, 2018

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1
Introduction

At the European Organization for Nuclear Research (CERN)[1], the design and realization of the circular particle accelerator, large hadron collider (LHC), has not only created new frontiers in particle physics but also has had a huge impact in varied fields of engineering, particularly in magnet design and measurements. The main elements of the accelerator are the radio frequency (RF) cavities accelerating the particles, the dipole magnets bending them to follow the circular orbit, and the quadrupole magnets focusing the beam to maintain a proper intensity and size. High kinetic energy is imparted to particle beams by applying electromagnetic field in the accelerator. A particle of charge q moving through an electromagnetic field is subjected to the Lorentz force given by

$$\vec{F} = q \cdot (\vec{E} + v \times \vec{B}) \tag{1.1}$$

where F is the electromagnetic force exerted by the electric field E and the induction field B on the particle with velocity v. As can be seen from (1.1), the force on the particle depends on both the electric field and the magnetic field. The uniform fields of a dipole magnet have a bending effect on electrically charged particles by virtue of Lorentz force. The movement of an electrically charged particle in a magnetic dipole field depends on the particle's velocity and the properties of the magnetic field. This imposes stringent constraints on the quality of the magnets and their measurements as any variation in field strength or direction could deflect the beam from its trajectory resulting in the loss of beam. According to Faraday's law, voltage is induced in a rotating coil placed in a magnetic-field. The strength of this magnetic-field is obtained by integrating the induced voltage over a period of time. This requires the use of an integrator and the quality of the measured field strength depends on the accuracy of the integrator.

For the accelerator magnets at CERN, a fast digital integrator (FDI) is designed to measure the field strength. The acquisition line of the FDI is susceptible to offset and gain errors, fluctuations in voltage reference, temperature effects etc and these errors reduce the measurement accuracy. When a signal with an offset is integrated, its effect is amplified depending on the integration time. This results in a drift in the integrated voltage which degrades the magnetic-field measurement. Therefore, systematic correction mechanisms have to be devised to mitigate such errors [25].

[1]The name CERN is derived from the acronym for the French 'Conseil Européen pour la Recherche Nucléaire', a provisional body founded in 1952 with the mandate of establishing a world-class fundamental physics research organization in Europe [12].

The aim of this project is to implement an auto-calibrating FDI for magnetic field strength in the range of 0.1 mT to 10 T with an accuracy of 1 least-significant bit (LSB) for a gain of 1. To achieve this high accuracy, a robust calibration system for the acquisition line is necessary. It mainly involves determining coil attenuation with an accuracy of 100 µV/V (that is, 100 ppm), calibrating the digital-to-analog converter (DAC) and designing a best-fit technique for the analog-to-digital converter (ADC) that can determine and correct the gain and the offset errors in the acquisition line with an accuracy of 1 LSB for a gain of 1.

This thesis work has been carried out at the Magnetic Measurements Division at CERN which is responsible for high-quality and reliable magnetic measurements for permanent, superconducting and radioactive magnets [13]. The research here is primarily focussed on the design of advanced magnetic-measurement techniques and the design of tools for the calibration of sensors and electronic instruments used for measurements.

1.1 Project Scope

The following tasks are defined within the boundaries of the project in terms of approach, milestones and deliverables. They are expected to be completed by the agreed timeline.

- Design a system to measure the coil resistance and calculate the attenuation factor by using ratiometric technique.
- Devise a mechanism to calibrate the DAC that supplies the programmable reference voltage to ADC.
- Calibrate ADC for gain and offset errors using best-fit implementation.
- Design an integrator in start-stop trigger mode using trapezoidal method.

The final deliverable is an auto-calibrating FDI with an accuracy of 1 LSB for a gain of 1.

1.2 Thesis Outline

This report is divided into five chapters that explain the design, implementation, results and limitations of our thesis work.

Chapter 2 presents the instrumentation for magnetic measurements and explains the rationale behind the design choices in this thesis work. Chapter 3 introduces in detail the calibration system and the integrator, their design details and the hardware used for the implementation.

The results of this thesis work are presented in Chapter 4. This chapter explains the experiments set up to ascertain the accuracy of each system and discusses the significance of the results obtained. We conclude with a discussion on the limitations of our design and possible future improvements in Chapter 5.

2
Background

The LHC has three main components namely the two beam pipes, the accelerating structures and the magnet system as shown in Fig. 2.1. Protons travel in the opposite direction inside the two beam pipes. These protons are accelerated by applying strong electric fields in smaller accelerators connected to the LHC before entering the beam pipe. The dipole magnets surrounding the pipe ensures that the circular trajectory of the beam is maintained. The dipoles along with additional magnets like quadrupoles, sextupole, octupole form the magnet system of the LHC.

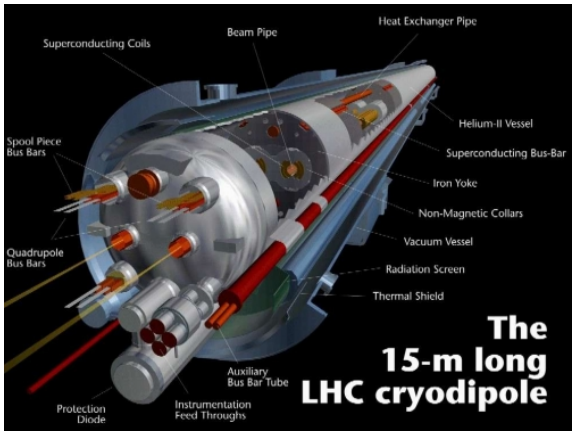

Figure 2.1: A section of LHC.

Source: CERN

The following sections present an overview of the relevant previous work in the field of magnetic measurement. It also explains the rationale for the design choices in this thesis work, namely the use of rotating-coil technique for magnetic measurement, ratiometric measurement to determine coil resistance, best-fit method for ADC calibration, trapezoidal method for numerical integration and the need for an FPGA-based solution for the integrator.

2.1 Instrumentation

For the LHC magnets, various parameters like the field strength, direction, errors in the field profile, location of the magnetic center are obtained in the form of an integral over the magnet length. The source measurement device must cater to a

wide range of fields spanning from 0.1 mT (corrector magnets) to the order of 10 T (main bending dipoles) with an accuracy better than 100 µT/T (100 ppm) [24]. The following section gives a brief overview of a selection of magnetic measurement techniques.

2.1.1 Magnetic Resonance Technique

The nuclear magnetic resonance technique is frequently used not only for calibration purposes but also for high-accuracy field mapping. In this technique, a sample of water is placed inside an excitation coil powered by a radiofrequency oscillator. The frequency of the nuclei of the water sample is directly proportional to the magnetic field strength. Though it provides high accuracy ($\pm$ 10 µT/T), it needs a uniform field to obtain a coherent signal [24] and thus cannot be employed for measuring varying fields.

2.1.2 Hall Probes

Hall probes exploit the Hall effect [17] to measure magnetic fields. They can measure non-uniform fields but cannot be used in stand-alone mode as they require an additional measurement method to account for the proportionality coefficient between the Hall signal and the magnetic field value.

2.1.3 Flux Gate Magnetometer

A flux gate magnetometer consists of a core around which are wrapped two coil windings: drive and sense winding. As the current flows through the drive winding, each winding generates a field in the opposite direction thus cancelling each other's effect. But when an external field is applied, one winding comes out of saturation earlier than the other one. During this time the fields do not cancel out and there is a net change in flux that induces a voltage and the corresponding field can be measured. This technique is restricted to low fields and is well-suited for static operation [24].

2.1.4 Rotating Coil

The rotating coil method is a general and accurate method to measure the field quality of magnets [25]. An induction coil is placed on a circular shaft and rotated in the field to be measured. The rotating coil cuts the flux lines and a voltage is induced. This voltage is then integrated to determine the field strength. It is widely used given its ability to measure properties of the magnetic field like strength, poles, angle, direction.

Other methods like magneto-resistivity effect, magnet resonance imaging, SQUIDS etc are described in [10]. These methods are complementary and a combination of them could meet the requirements of the measurement range and field strength [24] but in this thesis work rotating coil method is preferred as this technique on its own can be used for both fixed and varying field with wide range of field strengths.

2.2 Digital Integrator

The rotating-coil technique relies on the use of an integrator to integrate the voltage samples in determining the field strength. This section presents a brief overview of the types of numerical integration and the integrators designed at CERN.

2.2.1 Numerical Integration

The integral of a function, *f(x)*, can be thought of as the area between the curve and the x-axis. For continuous signals, the area under the curve, A, is determined using the exact method i.e.,

$$A = \int_a^b f(x)dx \tag{2.1}$$

For integrating discrete signals, numerical methods which are an approximation of the exact integration are used. For the design of FDI, three methods namely the rectangular, trapezoidal and Simpson's rule were assessed for their accuracy and complexity.

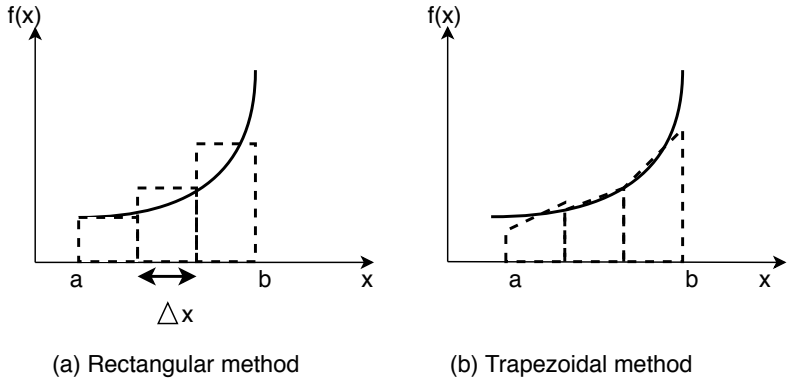

Figure 2.2: Rectangular and trapezoidal integration.

1. Rectangular method: is the most straightforward method wherein the area is divided into a series of rectangles between the integral limits and the integral is given by total area of all the rectangles. The area under the curve approximated by the rectangular method is given by:

$$\int_a^b f(x)dx = f(x_1)\Delta x + f(x_2)\Delta x ... + f(x_n)\Delta x \tag{2.2}$$

   where $f(x_n)\Delta x$ is the area of each rectangle.
2. Trapezoidal method: the accuracy of the rectangular method is improved by replacing the rectangles with trapezoids as shown in Fig. 2.2. The area of a trapezoid, A_{tr}, is given by:

$$A_{tr} = [f(x_1) + f(x_2)]\frac{\Delta x}{2} \tag{2.3}$$

Summing the area of all the trapezoids, the area under the curve is given by:

$$\int_a^b f(x)dx = [f(a) + f(x_1)]\frac{\Delta x}{2} + [f(x_1) + f(x_2)]\frac{\Delta x}{2} + \\ ... + [f(x_n) + f(x_b)]\frac{\Delta x}{2} \tag{2.4}$$

Re-arranging (2.4),

$$\int_a^b f(x)dx = \frac{\Delta x}{2}[f(a) + 2f(x_1) + 2f(x_2)..... + 2f(x_n) + f(b)] \tag{2.5}$$

3. Simpson's rule: higher integration accuracy can be obtained by approximating the curve to a higher order function. In Simpson's rule, the curve is approximated through parabolic interpolation [23]. The integral is determined using (2.6).

$$\int_a^b f(x)dx = \frac{\Delta x}{2}[f(a) + 4f(x_1) + 2f(x_2) + \\ ....2f(x_{2n-2}) + 4f(x_{2n-1} + f(b)] \tag{2.6}$$

This method requires that the total number of subdivisions in the interval be an even number. This cannot be guaranteed in our design as the triggers for the integration are asynchronous and the intervals could be even or odd depending on the arrival of the trigger and the required integration time. Though this method is significantly more accurate than trapezoidal, due to its increased complexity and latency we have decided to use the trapezoidal method for the current version of the FDI.

2.2.2 Portable Digital Integrator

The portable digital integrator (PDI) is based on a voltage-to-frequency converter (VFC) with a maximum frequency of 500 kHz and a full scale of 10 V. The VFC has two pulse outputs, one proportional to the input voltage and the other one, a fixed reference frequency. These pulse outputs are fed to counters and the difference of their count value at the end of the measurement period is proportional to the integral of the input voltage [15]. The total number of pulses n, is given by,

$$n = \int_{\Delta t} f dt = K \int_{\Delta t} V_{\text{in}} dt \tag{2.7}$$

where K is the proportionality constant, f is the frequency of the square waveform produced by the VFC and V_{in} is the input voltage. The flux variation $\Delta\phi$ is given by

$$\Delta\phi = \frac{n}{K} \tag{2.8}$$

The resolution of the VFC is inversely proportional to the sampling rate and hence accuracy cannot be guaranteed at high sampling rate. The minimum integration interval is limited by the VFC maximum frequency, and hence higher acquisition speed cannot be accomodated by this integrator.

2.2.3 Fast Digital Integrator

Given the limitations of PDI, an alternative design called fast digital integrator, was conceived at CERN [8, 9] (this version is referred to as FDI_{v1} hereon). It is designed for high-speed magnetic measurements and is based on rectangular integration method. The architecture of FDI_{v1} is shown in Fig. 2.3

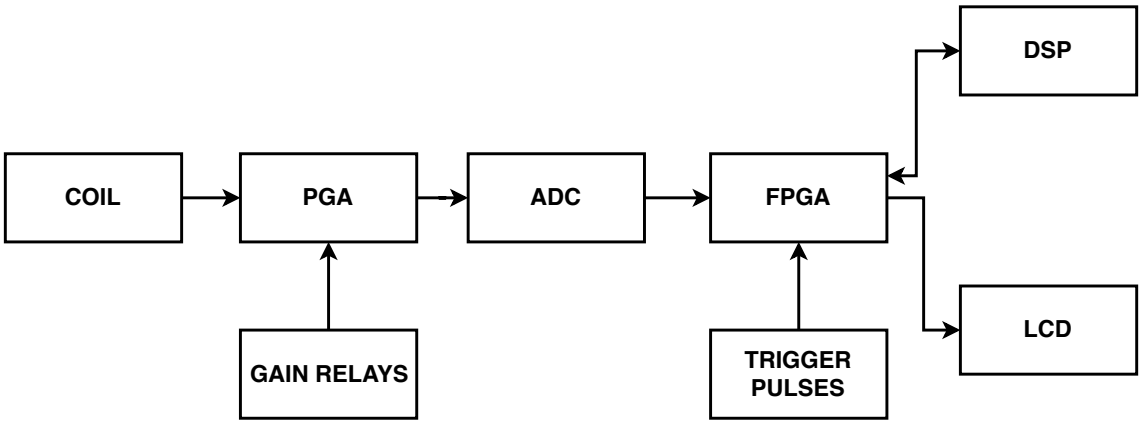

Figure 2.3: The architecture of FDI_{v1}.

The first stage is a programmable-gain amplifier (PGA) that adjusts input voltage to fit within the voltage range of the system (small gain for large signals and vice-versa) to enable measurement of a wide range of magnetic field. The amplified signal is then digitized by the ADC and integrated by a digital signal processor (DSP). The FPGA is responsible for the offset and gain calibration and the storing of calibration coefficients. It also handles the I/O management between the calibration block, memory and DSP.

The voltage samples of the rotating coil are integrated between two trigger pulses using the rectangular method and the flux variation in this interval is given by,

$$\Delta\phi = V_{\mathrm{k}_1} t_{\mathrm{ak}} + \sum_{i=2}^{N} V_{\mathrm{k}_i} t_{\mathrm{k}_i} + V_{\mathrm{k}_{N+1}} t_{\mathrm{bk}} \tag{2.9}$$

where N is the number of samples between two trigger pulses, V_{k_i} is the i^{th} voltage sample digitized by the ADC, t_{ak} is the time interval between the first trigger pulse and the next pulse of the ADC clock, t_{bk} is the time interval between the next trigger pulse and the previous pulse of the ADC clock, and t_{k_i} is the ADC clock period. In this architecture, the DSP acts as the processor and FPGA as the I/O manager. The future plan for the FDI is to have portability with other communication buses (PCIe, PXIe and VME) with limited maintenance. In light of the changes foreseen for the future FDI, a new architecture is conceived for the FDI as shown in Fig. 2.4.

In this new version, the DSP is replaced by the FPGA for the following reasons:

1. The DSP is not well adapted when there are many inputs/outputs in addition to multiple communication interfaces.

2. Given the need for limited maintenance, it's easier to manage a single component (FPGA) as opposed to two (FPGA+DSP).

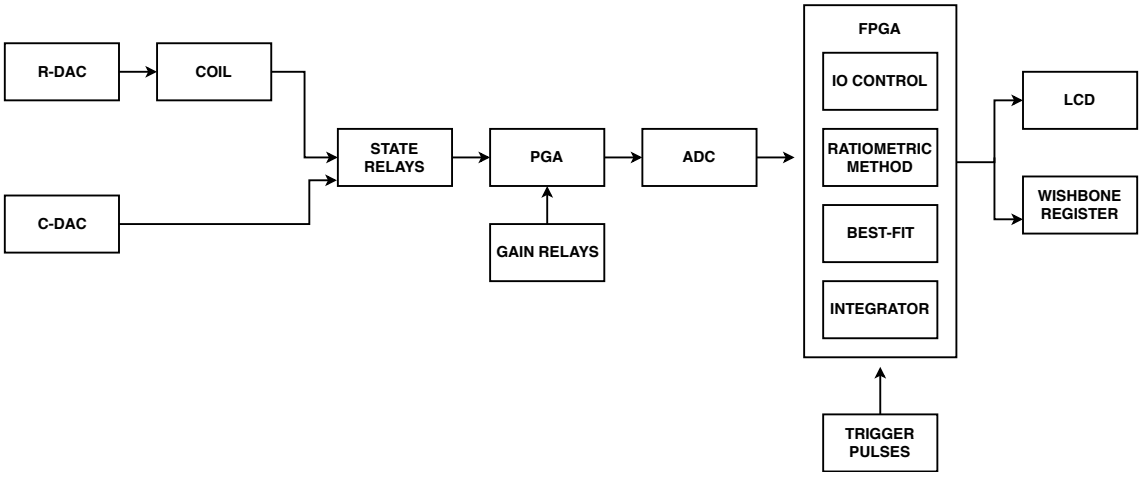

Figure 2.4: The new auto-calibrating FDI architecture.

In this new version, the FPGA not only acts as the IO manager but is also responsible for the calibration and integration. The calibration system comprising of ratiometric method, best-fit method and the potentiometer interface for DAC calibration are designed using the FPGA. The rectangular method used in the older version for integration is replaced by the trapezoidal method implemented in the FPGA. Two DAC namely ratiometric DAC, R-DAC, and calibration DAC, C-DAC, are used in the calibration system. R-DAC provides the coil voltage to determine the attenuation due to the coil and C-DAC provides the reference voltages for the best-fit calibration and digitized voltages for the integrator. The state relays switch the input to (a) C-DAC during DAC and ADC calibration, (b) to coil during ratiometric calibration and integration. The PGA is controlled by the gain relays that switch between a set of 12 gains to provide adequate SNR in the system. The output is displayed on the LCD and also stored in wishbone registers.

Wishbone registers are user-defined registers generated by a tool 'wbgen2' to access the FPGA through a wishbone bus [26]. The wishbone system-on-chip (SOC) interconnection architecture, also known as wishbone bus, is a free, open-source standard that defines a common interface among Intellectual Property (IP) Cores in a SOC [27]. It enables design reuse by providing a common interface between IP cores. A wishbone master driver communicates with the FPGA board through the PCIe interface. The tool wbgen2 is used to create a 'slave core', an HDL entity which is connected to wishbone bus on one side, and on the other side it provides ports for accessing memory mapped registers, FIFOs and RAMs. This tool is configured to generate wishbone registers to access the FPGA. The various inputs required for the calibration system are written to the wishbone register by the FPGA during initialization. The calibration and integration status along with their outputs are stored in wishbone registers that are accessible to the users through a PC.

2.3 ADC Calibration Technique

The ADC transfer curve can be modelled using an end-fit or best-fit line to correct the gain and offset errors. The end-fit line used in FDI_{v1} cannot provide an accuracy of $\pm 10\,\mu T/T$ and as a result it was decided to implement best-fit calibration in this thesis work.

2.3.1 End-Fit

The end-fit line connects two extremities of the transfer curve of ADC as shown in Fig. 2.5. It is a simple technique that gives a rough estimate of the gain and offset errors. In practice, the more uneven the transfer curve, the more points must be used to account for the integral non-linearity (INL). For accurate measurements, it is better to use the best-fit line to determine gain and offset errors [22].

2.3.2 Best-Fit

The best-fit line is constructed to minimise the deviation of the line from the actual transfer curve as shown in Fig. 2.5. An n-point best-fit line forms the basis of measurement of gain and offset errors in the ADC calibration. The number of points has a direct bearing on the measurement accuracy and calibration time. Accuracy increases with the number of points but so does the calibration time. To reduce the calibration overhead, the upper limit on the number of points is set to 32.

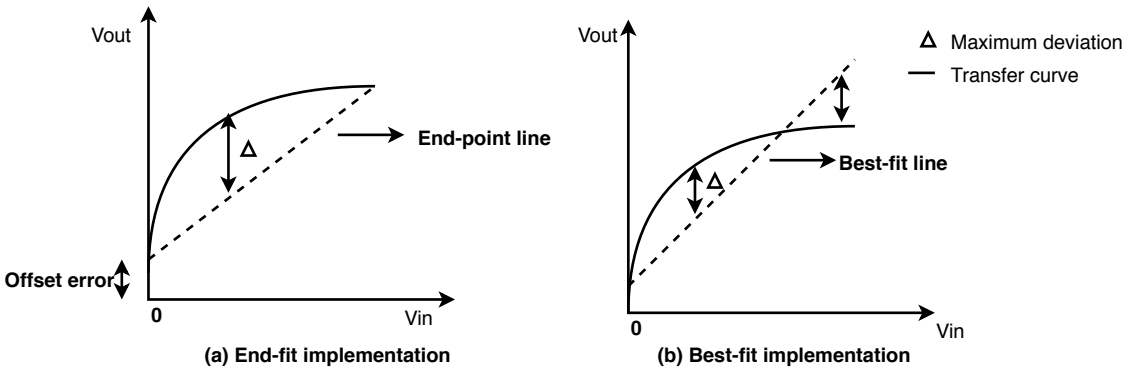

Figure 2.5: End-fit and best-fit lines.

3

Implementation

In this chapter, we discuss the design details and the hardware implementation of the calibration system and the integrator.

The main objective of the calibration system is to reduce the FDI errors by correcting the gain and offset errors of the ADC that digitizes the input voltage for the FDI. To reduce calibration errors, it is important to consider the effect of the front-end analog circuitry and account for the errors introduced by this circuitry.

The front end of the FDI consists of a Coil-PGA-ADC chain as shown in Fig. 2.4, that amplifies and digitizes the voltage induced in the coil. The induced coil voltage acquired by the FDI, V_{ATTN}, is subject to attenuation due to the coil resistance, R_{S}, as shown in Fig. 3.1. We use ratiometric method to determine this attenuation.

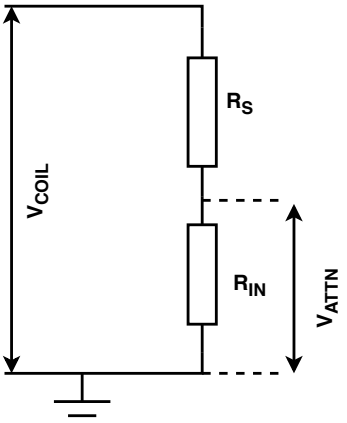

Figure 3.1: Coil attenuation due to source resistance, R_{S}.

The best-fit ADC calibration requires the input signal to span the entire ADC voltage range of ± 10 V to model the transfer curve with minimal errors. For lower field strength, the induced voltage doesn't span this range and in stronger fields, the voltage exceeds this range. This necessitates the need for a PGA circuit that amplifies or reduces the input signal so that it would sweep the ADC voltage span. It is also used to provide adequate SNR for coils with low induced-voltage. The PGA comprises a set of operational amplifiers (op-amps) with gains ranging from 0.1 to 500. The selection of the op-amps is controlled by the gain-relay controllers as shown in Fig. 3.2. These relay-controllers can be switched manually by the user or by the calibration system. The different gains can be used in combination to measure coil voltage from 20 mV to 100 V.

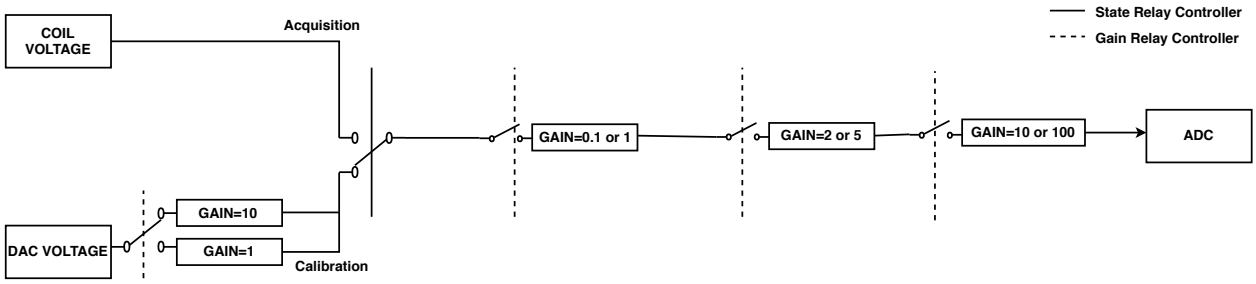

Figure 3.2: Functional block diagram of the PGA block.

But the op-amps in the PGA block suffer from offset errors due to the inherent component mismatch. Since the reference voltages for the ADC calibration are obtained from the DAC-PGA chain as shown in Fig. 3.3, the ADC calibration is affected by this offset which varies with the selected gain. Therefore the DAC-PGA chain must be calibrated to remove this variable offset prior to the ADC calibration and it is done so using digital potentiometers (DPOT). The calibration system essentially involves: (a) calibrating the analog circuitry to account for the attenuated coil voltage and correcting the gain and offset errors of the PGA-DAC chain; (b) calibrating the ADC of its inherent gain and offset errors. The block diagram of the calibration system is shown in Fig. 3.3.The calibration of FDI is divided into three parts, each corresponding to a subsection:

1. Determine the coil resistance and the attenuation using ratiometric method.
2. Calibrate the DAC using digital potentiometer.
3. Calibrate the ADC for offset and gain correction using best-fit line.

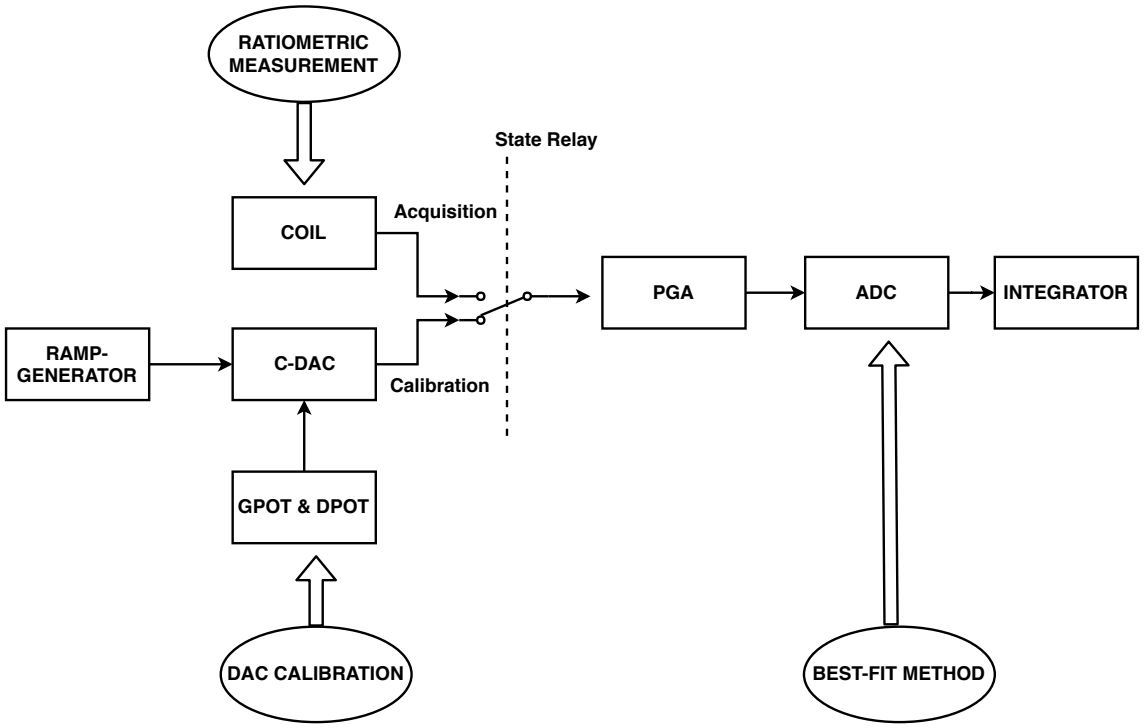

Figure 3.3: Functional block diagram of the calibration set-up.

3.1 Ratiometric Measurement

The attenuation due to the coil resistance is calculated by the voltage-divider rule applied to the circuit in Fig. 3.1,

$$V_{\mathrm{ATTN}} = \frac{V_{\mathrm{COIL}} \times R_{\mathrm{IN}}}{R_{\mathrm{S}} + R_{\mathrm{IN}}}, \tag{3.1}$$

where V_{ATTN} is the attenuated output voltage, V_{COIL} is the voltage applied to the coil, R_{S} is the coil resistance and R_{IN} is the input resistance of the integrator (typically about 2 MΩ ±0.1%).

The coil resistance, R_{S}, is determined using ratiometric technique. In this technique, the measured quantity is proportional to the ratio of two voltages rather than an absolute voltage. When the two voltages are proportional to the same reference, the ratiometric method eliminates voltage reference errors [11].

The factor by which V_{COIL} gets attenuated is called the attenuation factor and the inverse is the gain-correction factor, C_{gf}, given by

$$C_{gf} = 1 + \frac{R_{\mathrm{S}}}{R_{\mathrm{IN}}} \tag{3.2}$$

To determine R_{S} ratiometrically, the voltages $V_{\mathrm{P}} - V_{\mathrm{M}}$ and $V_{\mathrm{M}} - V_{\mathrm{N}}$ are derived from a differential voltage V_{RDAC}, applied to the coil as shown in Fig. 3.4. A 1 kΩ resistor is used for R_{REF}.

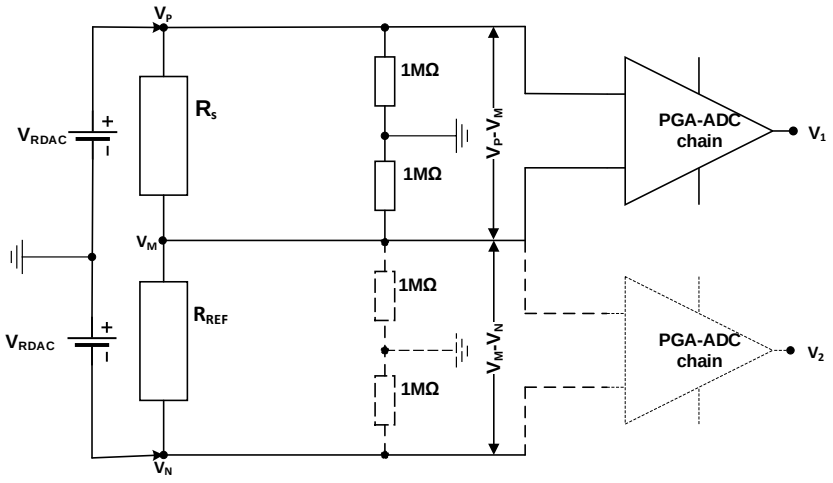

Figure 3.4: Coil resistance measurement set-up.

A relay is used to switch the input of the PGA-ADC chain from $V_{\mathrm{P}} - V_{\mathrm{M}}$ to $V_{\mathrm{M}} - V_{\mathrm{N}}$. The equivalent circuits are shown in Fig. 3.5.

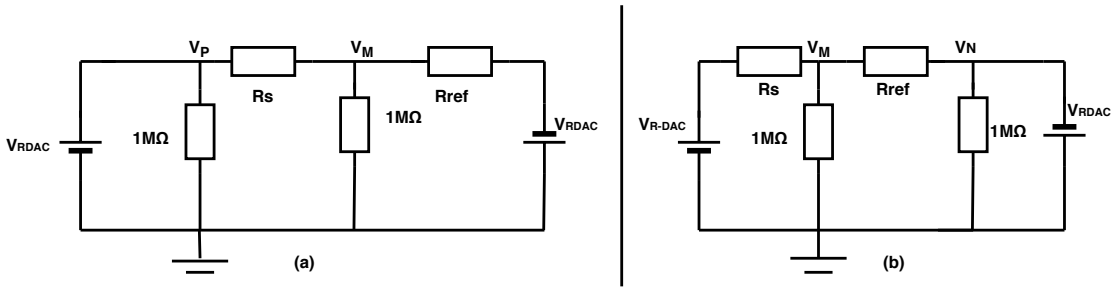

Figure 3.5: Circuits to determine (a) $V_\mathrm{P} - V_\mathrm{M}$ and (b) $V_\mathrm{M} - V_\mathrm{N}$

Solving (a) and (b) by superposition theorem, we obtain the following voltages:

$$V_\mathrm{P} - V_\mathrm{M} = \frac{R_\mathrm{S}(R_\mathrm{REF} + R_\mathrm{IN})}{R_\mathrm{S}(R_\mathrm{REF} + R_\mathrm{IN}) + R_\mathrm{IN}R_\mathrm{REF}} + \frac{R_\mathrm{S}R_\mathrm{IN}}{R_\mathrm{REF}(R_\mathrm{S} + R_\mathrm{IN}) + R_\mathrm{S}R_\mathrm{IN}} \tag{3.3}$$

$$V_\mathrm{M} - V_\mathrm{N} = \frac{R_\mathrm{S}(R_\mathrm{REF} + 2R_\mathrm{IN})}{R_\mathrm{S}(R_\mathrm{REF} + R_\mathrm{IN}) + R_\mathrm{IN}R_\mathrm{REF}} \tag{3.4}$$

Substituting R_IN= 2 MΩ and R_REF= 1 kΩ, the ratio of (3.3) and (3.4) gives R_S in kΩ:

$$\frac{V_\mathrm{P} - V_\mathrm{M}}{V_\mathrm{M} - V_\mathrm{N}} = \frac{2001R_\mathrm{S}}{2000 + R_\mathrm{S}} \tag{3.5}$$

Re-arranging (3.5) for R_S we get:

$$R_\mathrm{S} = \frac{2000(V_\mathrm{P} - V_\mathrm{M})}{2001((V_\mathrm{M} - V_\mathrm{N}) - (V_\mathrm{P} - V_\mathrm{M}))} \tag{3.6}$$

Subsituting (3.6) in (3.2), the gain-correction factor is determined to be

$$C_\mathrm{gf} = 1 + \frac{V_\mathrm{P} - V_\mathrm{M}}{2001((V_\mathrm{M} - V_\mathrm{N}) - (V_\mathrm{P} - V_\mathrm{M}))} \tag{3.7}$$

3.1.1 Hardware Implementation

The functional block diagram of the ratiometric system is represented by Fig. 3.6.

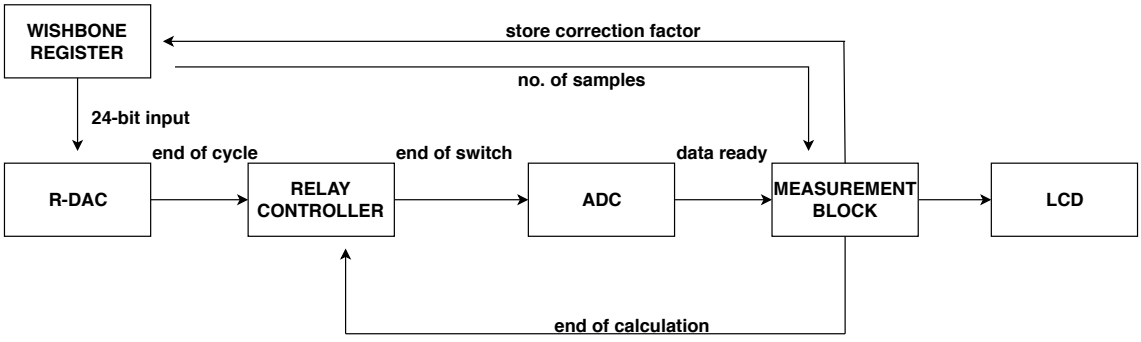

Figure 3.6: Functional block diagram of the ratiometric measurement system.

The system functionality and details of the components are explained below:

1. **Wishbone register**:
   In this design, three wishbone registers are created to store the input digital value for the R-DAC, the coil resistance and the attenuation factor calculated by the measurement block.
2. **Ratiometric digital-to-analog converter**:
   AD5660 [2] is the R-DAC used to provide V_{RDAC} voltage across the coil based on the wishbone value set by the operator. It is a serial 16-bit, low power DAC with a resolution of 153 µV (10V/65536). After the conversion of the data, the R-DAC interface sends an 'end of cycle' signal to the relay controller.
3. **Relay controller**:
   A surface mount relay G6K [14] is used to switch the input voltage of the PGA-ADC chain. This subminiature model is opted due to the space constraints on the board. The input to the PGA-ADC chain is switched from $V_{\mathrm{P}} - V_{\mathrm{M}}$ to $V_{\mathrm{M}} - V_{\mathrm{N}}$ based on the 'end of calculation' signal received from the measurement block. The relay interface signals the ADC to start conversion by generating an 'end of switch signal' when the relay position changes.
4. **Analog-to-digital converter**:
   A 20-bit, bipolar low-power successive approximation register (SAR) based ADC, LTC2378 [20], is used to digitize $V_{\mathrm{P}} - V_{\mathrm{M}}$ and $V_{\mathrm{M}} - V_{\mathrm{N}}$. A throughput of 1 million samples per second (Msps) with no cycle latency and a resolution of 19 µV ($20\mathrm{V}/2^{20}$) makes the LTC2378 an ideal candidate for precise and high-speed measurement systems.
5. **Measurement block**:
   This block averages the digitized voltage from the ADC and calculates the coil resistance and gain-correction factor based on (3.6) and (3.7). The number of samples for averaging is accessed from the wishbone register. An 'end of calculation' pulse is generated by this block to signal the relay controller to switch to the next voltage to be determined. The calculated values are stored in the wishbone register and displayed on the LCD.

3.2 DAC Calibration

In FDI_{v1}, the voltage references for the ADC calibration were obtained from a resistor-network partitioning [6]. This increases the error due to the resistor tolerance and makes the calibration dependent on the temperature. Such errors are overcome in this implementation by employing a fully digital solution mainly based on a 20-bit DAC, C-DAC.

The DPOT used to correct the offset error is referred to as O-POT and the gain correcting DPOT is referred to as G-POT. The O-POT is connected to the offset nulling circuit of the output op-amp and employs trimming to adjust the offset. The G-POT trims the C-DAC reference voltage to reduce the gain error. The C-DAC is calibrated manually by end-point calibration and the sequence is explained as follows: First, the offset error is calibrated by setting the input to the negative end-point and the digital input of the O-POT is adjusted until the offset of the high-

gain or low-gain differential amplifier as shown in Fig. 3.7 is nullified. The gain error is calibrated next by setting the input to positive end-point and adjusting G-POT until the deviation is minimised. The O-POT is adjusted again by setting the input to 0 V to remove the remnant offset after the gain calibration. The digital value set in the potentiometers corresponding to the offset and gain calibration is then stored in a wishbone register.

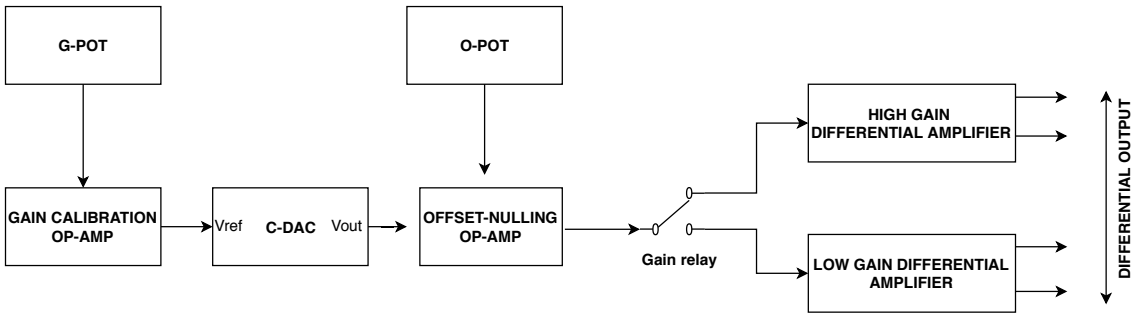

Figure 3.7: Functional block diagram of DAC Calibration

3.2.1 Hardware Implementation

1. **Operational amplifier**:
   A high-precision operational amplifier, AD8675 [4], is configured as gain calibration op-amp and offset nulling op-amp as shown in Fig. 3.7 to nullify the gain and offset error of the DAC and the analog circuitry. Due to its ultralow offset, drift and voltage noise over the full operating temperature range it doesn't corrupt the calibration with its own offset and hence is well suited for this design.
2. **Digital Potentiometer**:
   AD5292 [1], a 1024-position digital potentiometer is used to calibrate the DAC-PGA chain. Adjustment of the wiper position is done through an SPI interface designed in the FPGA.
3. **Calibration digital-to-analog converter**:
   In this design, AD5791 [3], a 20-bit bipolar DAC also referred to as C-DAC, provides the reference voltages to calibrate the ADC. To achieve higher precision, the resolution of the DAC must be equal or greater than ADC to calibrate it below half LSB. Another design requirement for the DAC is that it must be bipolar since the voltage on a coil is bipolar and it is necessary to calibrate the ADC on both positive and negative reference voltages. The instrumentation DACs found on the market currently offer 20-bit resolution and AD5791 is one among them. Since it satisfies all the above requirements, it is chosen for ADC calibration.
4. **Gain Relay**:
   The system uses different gains to increase the range of operation as explained in section 2.2.3. During ADC calibration, the gain relays are used to set different gains based on the input voltage of the DAC so that the reference voltages span from -10 V to 10 V. They are also used to direct the DAC output

to their corresponding amplifier based on the applied gain, that is, for gains less than 1 (high input voltage), the relay directs the DAC output to the high voltage differential amplifier and for gains greater than 1 (low input voltage), it is directed to low-voltage amplifier.

5. **Differential Amplifier**:
   A differential amplifier prior to the ADC input increases the common mode rejection ratio (CMRR) to ensure accuracy in the ADC calibration. The DAC calibration system uses two differential amplifier at its output to route high-voltage (±100 V) and low-voltage(±10 V) signals. LTC6090 [21] is used as the high-voltage amplifier and AD8676 [5] is used as the low voltage differential amplifier with a supply range of ± 12 V.

3.3 Best-fit Implementation

The transfer curve of an ideal ADC has a linear characteristic as shown in Fig. 3.8. An ideal ADC would have zero offset and a slope of 1. But, in practise, an ADC suffers from offset error due to which a non-zero output is present in the absence of input voltage and from gain errors where the transfer curve deviates from the ideal slope. These errors affect the accuracy of measurements and must be corrected by calibrating ADC at the beginning of every measurement.

The first step in the ADC Calibration is to obtain the ADC transfer curve given by (3.8) by determining its slope m and offset b,

$$y_{\mathrm{i}} = m \times x_{\mathrm{i}} + b \tag{3.8}$$

where y_{i} is the uncalibrated output of the ADC and x_{i} the input reference voltage generated by C-DAC. A set of 32 points with 16 points on either side of the vertical axis is used to generate a best-fit line of the uncalibrated ADC transfer curve as shown in Fig. 3.8.

In the best-fit line, all points except the end-points are equidistant with a step-size, I (in V), given by:

$$I = \frac{20}{n \times G} \tag{3.9}$$

where n is the number of best-fit points and G is the gain of the system. The maximum and minimum value of the ADC dynamic range are more prone to non-linear effects and can have a disproportionate effect on the best-fit line and in the calculation of m and b. Hence the end-points are selected with half the step-size from their preceeding point and as such only the points barring the end-points are equidistant.

Least squares method [18] is used to determine m and b from the best-fit line as it aims to minimise the deviation, rather the squared deviations from the ideal transfer curve. The squared deviation is calculated using:

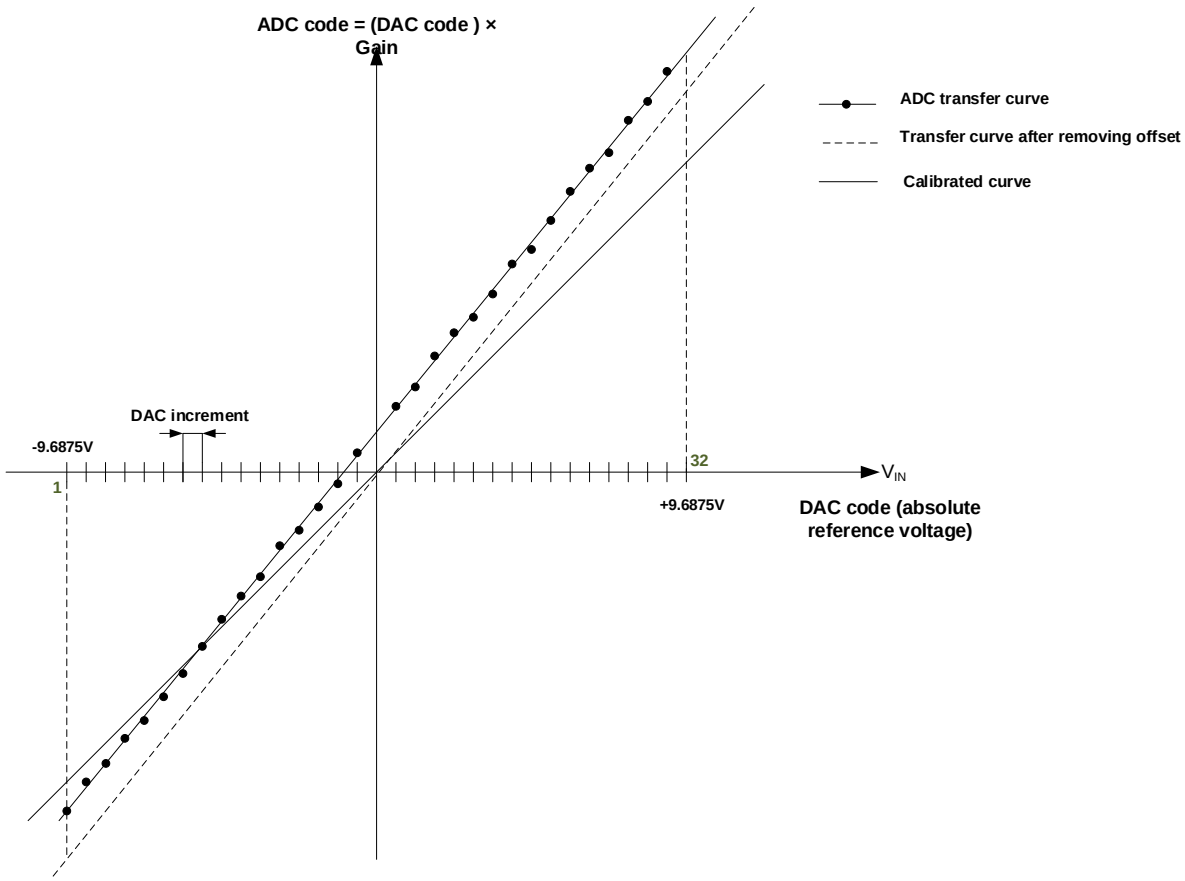

Figure 3.8: Calibration using best-fit line.

$$D^2 = \sum_{i=1}^{n} [y_\mathrm{i} - (mx_\mathrm{i} + b)]^2 \tag{3.10}$$

The coefficients m and b are obtained by setting D^2 to a minimum i.e

$$\frac{\partial D^2}{\partial m} = -2 \sum_{i=1}^{n} [y_\mathrm{i} - (a + bx_\mathrm{)}]x_\mathrm{i} = 0 \tag{3.11}$$

$$\frac{\partial D^2}{\partial b} = -2 \sum_{i=1}^{n} [y_\mathrm{i} - (a + bx_\mathrm{i})] = 0 \tag{3.12}$$

Solving the simultaneous linear equations (3.11) and (3.12), m and b are obtained as follows:

$$m = \frac{n \sum_{i=1}^{n} x_i y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} y_i}{n \sum_{i=1}^{n} x_i^2 - (\sum_{i=1}^{n} x_i)^2} \tag{3.13}$$

$$b = \frac{\sum_{i=1}^{n} y_i \sum_{i=1}^{n} x_i^2 - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} x_i y_i}{n \sum_{i=1}^{n} x_i^2 - (\sum_{i=1}^{n} x_i)^2} \tag{3.14}$$

3.3.1 Hardware Implementation

The functional block diagram of the ADC calibration system is shown in Fig. 3.9.

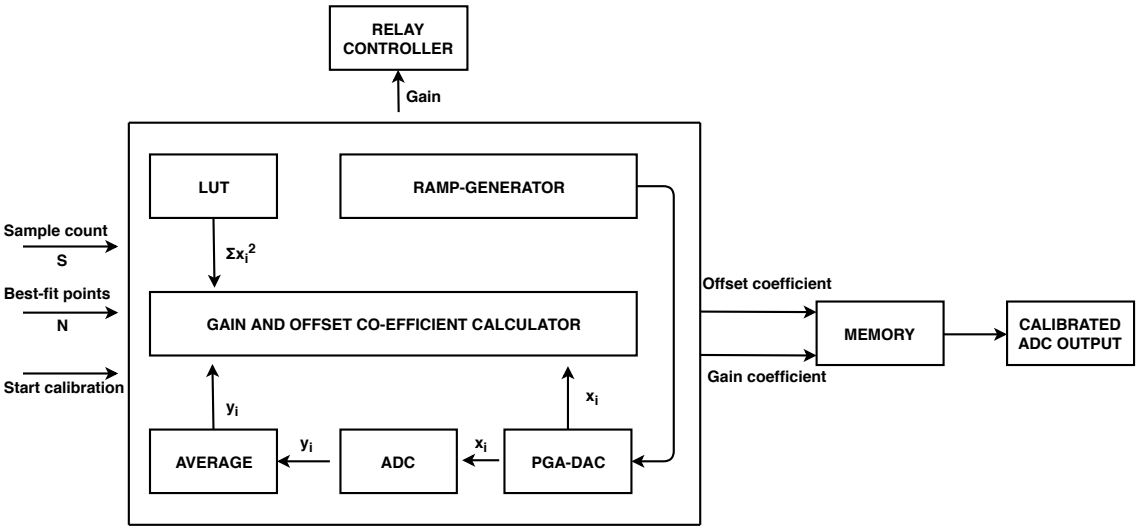

Figure 3.9: Functional block diagram of ADC calibration.

Since the induced voltage can be of positive or negative amplitudes, the bipolar ADC, LTC2378, is used to digitize the input signal. This results in $\sum_{i=1}^{n} x_i = 0$, reducing (3.13) and (3.14) to:

$$m = \frac{\sum_{i=1}^{n} x_i y_i}{\sum_{i=1}^{n} x_i^2} \tag{3.15}$$

$$b = \frac{\sum_{i=1}^{n} y_i}{n} \tag{3.16}$$

The ramp-generator generates a voltage ramp of interval I given by (3.9). The term $\sum_{i=1}^{n} x_i^2$ in (3.15) is a constant for each best-fit point and is stored in the look-up table (LUT). These constant values are given in Table 3.1.

Table 3.1: $\sum_{i=1}^{n} x_i^2$ values for best-fit points.

Best-fit point	$\sum_{i=1}^{n} x_i^2$ (in HEX)
4	4C4B400000
8	A037A00000
16	1443FD00000
32	28A67E80000

A sequence of 32 digital data is generated by the ramp-generator covering the dynamic range of the ADC. This data is fed to the DAC-PGA-ADC chain and each sample is repeated a number of times to average the noise and the inaccuracies of the measurement. The ramp voltage amplified by the PGA, x_i, averaged ADC output, y_i, and $\sum_{i=1}^{n} x_i^2$ are then used by the coefficient calculator to determine m and b for the 12 gains. The coefficients are then stored in a RAM block and are used to calibrate the ADC output using:

$$y_{cal} = \frac{y_{uncal} - b}{m} \tag{3.17}$$

To account for the coil attenuation, (3.17) is modified to incorporate the gain-correction factor, C_{gf}, as shown below:

$$y_{cal} = \frac{(y_{uncal} - b)C_{\mathrm{gf}}}{m} \tag{3.18}$$

3.4 Fast Digital Integrator

For rotating coil measurements, the FDI releases a flux sample at each trigger pulse by integrating the coil voltage between two triggers. The flux between two trigger pulses is given by

$$\phi(t) = \int_{start}^{stop} V(t)dt \tag{3.19}$$

Using the trapezoidal method explained in section 2.2.1, the flux is determined as follows:

$$\int_{start}^{stop} V(t)dt = \frac{\tau_{\mathrm{ADC}}}{2}[V(t_0) + 2V(t_1) + ... + 2V(t_{n-1}) + V(t_n)] \tag{3.20}$$

where $V(t_i)$ are the ADC codes sampled between two triggers. The magnetic field B is given by

$$B(t) = \phi(t).(g/A) \tag{3.21}$$

where g is the coil correction factor specified by the coil manufacturer (dependent on the length) and A is the coil effective area.

3.4.1 Hardware Implementation

The block diagram of the FDI is shown in Fig. 3.10 and the function of the components are explained below:

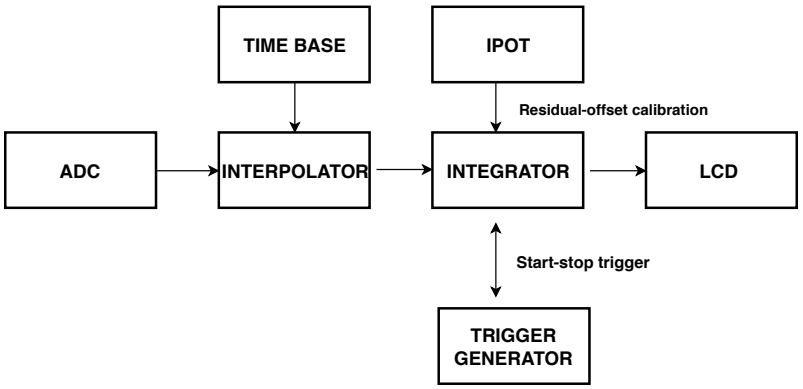

Figure 3.10: Functional block diagram of the FDI.

1. Configurable internal trigger generator: This block generates a series of pulses whose width, period and number can be configured by the user. It can also delay the external triggers generated by a pulse generator board. It works in two configurations namely
   (a) Start-stop mode: generates a continuous set of trigger pulses until the sequence is terminated by the user manually.
   (b) Burst mode: generates a fixed number of pulses based on the count value configured by the user.
2. Timebase: measures the interval between two trigger pulses. Fig. 3.11 shows the block diagram of the design. The global timer is a free-running 48-bit counter of 10 ns resolution derived from the onboard 100 MHz oscillator. The counter starts when a start pulse is received and on receiving the stop pulse the counter value is deducted from the global timer to obtain the integration interval. The counter is reset to 0 at every stop pulse and restarted on the start pulse.

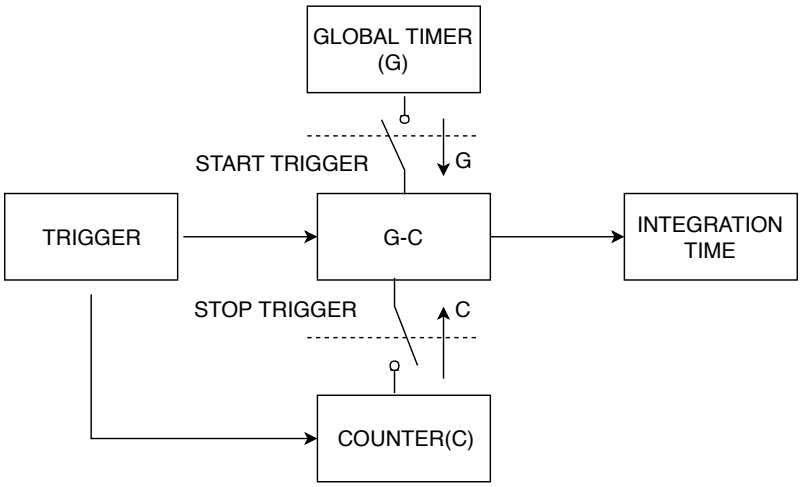

Figure 3.11: Functional block diagram of the FDI Timebase.

3. Interpolator: The triggers generated are asynchronous with ADC samples and they might occur during the ADC conversion time when there is no corresponding digital data. In such cases, the missing data is reconstructed using linear interpolation given by (3.22).

$$V_{\text{k-1}} = \frac{(V_0 \times \tau_{\text{ak0}}) + (V_1 \times \tau_{\text{bk0}})}{\tau_{\text{ADC}}} \tag{3.22}$$

where V_{k-1} is the interpolated value, τ_{ADC} is the ADC conversion time of 1 µs, τ_{ak0} and τ_{bk0} are the time interval between ADC sample and the occurence of the trigger.

Fig. 3.12 shows the start-stop integration when the triggers, T_0 and T_1, are asynchronous with ADC. In such cases, the interpolated signal V_{k-1} and V_k are used to determine the flux based on (3.23).

$$\int_{start}^{stop} V(t)dt = \tau_{\text{ak0}}\left[\frac{V_{\text{k-1}} + V_1}{2}\right] + \tau_{\text{bk1}}\left[\frac{V_{\text{k}} + V_5}{2}\right] + \frac{\tau_{\text{ADC}}}{2}\left[V_1 + 2V_2 + ... + 2V_{n-1} + V_5\right] \tag{3.23}$$

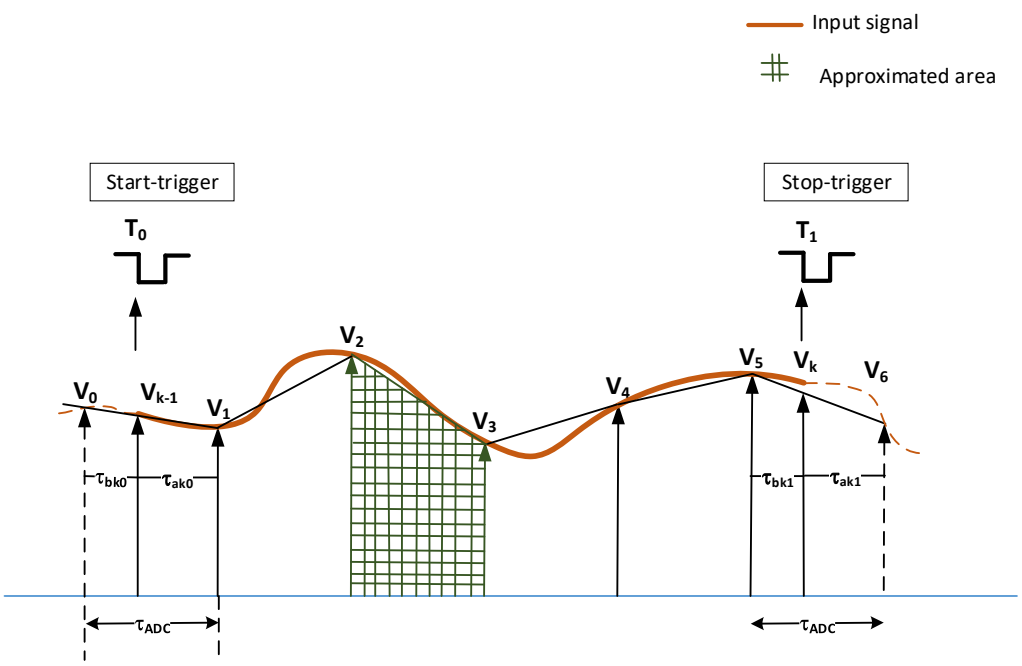

Figure 3.12: Integration by start-stop trigger. $V_0, V_1 ... V_6$ are the ADC data generated at an interval τ_{ADC}. The area covered by the input signal during the conversion time is approximated by the trapeziod. The dotted lines represent the signals outside the triggers.

4. Fine offset compensation : A digital potentiometer [1], referred to as IPOT is used to remove any residual offset originating from factors external to the board, such as, the length of the cable between the source and the ADC, impedance of the voltmeter etc. Such offsets are removed after best-fit calibration by manually adjusting the potentiometer until the offset is completely reduced to 0 V.

4

Results and Discussion

This chapter presents the tests conducted to verify the functionality of the calibrating system and the integrator. The results obtained for each tests are reported in this chapter along with a discussion of their implications.

4.1 Ratiometric Measurement

Ratiometric measurement ensures that the measured resistance, R_{S}, and gain-correction factor, C_{gf}, is not affected by the changes in reference voltage. An accuracy of $100\,\mu\mathrm{V/V}$ in C_{gf} is set as the design objective of this measurement and a variation of $\pm 1\ \Omega$ in R_{S} is considered permissible.

4.1.1 Measurement of Errors in R_{S} and C_{gf}

The functionality of the design is tested for two resistors: $9.982\,12\,\mathrm{k\Omega}$ and $390\,\Omega$. The input voltage is varied with a step-size of $0.625\,\mathrm{V}$ and an average of 1024 ADC samples are taken at each voltage level. The tables 4.1 and 4.2 present the errors obtained in the measurement of R_{S} and C_{gf}. The error in the measurement of R_{S}, E_{r}, is calculated using:

$$E_{\mathrm{r}} = R_{\mathrm{a}} - R_{\mathrm{m}} \tag{4.1}$$

where R_{a} and R_{m} are the actual and measured resistance respectively.
The error in the measurement of C_{gf}, E_c, is determined using:

$$E_{\mathrm{c}} = \frac{C_{\mathrm{a}} - C_{\mathrm{m}}}{C_{\mathrm{a}}} \tag{4.2}$$

where C_{a} and C_{m} are the actual and measured values respectively.

Table 4.1: Ratiometric measurements for R_S= 9.98212 kΩ.

R_S= 9.98212 kΩ, C_{gf}=1.00499106		
Voltage(V)	E_r (Ω)	E_c (µV/V)
0.625	4.59	0.23
1.25	2.25	0.12
1.875	1.52	8.02
2.5	1.05	6.03
3.125	0.87	5.03
3.75	0.85	5.03
4.375	0.72	4.04
5	0.57	6.90

Table 4.2: Ratiometric measurements for R_S= 390 Ω.

R_S= 390 Ω, C_{gf}=1.000195		
Voltage(V)	E_r (Ω)	E_c (µV/V)
0.625	-0.00051	0
1.25	-0.00154	0
1.875	-0.00103	0
2.5	-0.00077	0
3.125	-0.00051	0
3.75	-0.00051	0
4.375	-0.00051	0
5	-0.00051	0

Though the error in the measured R_S is negligible for both the resistors, we notice an increased error with lower input voltage. This, we suspect, is due to the increased effect of noise at lower amplitudes coupled with the inherent tolerances of the R_{REF} and R_{IN} resistors. In (3.3) and (3.4), the tolerance of R_{REF} and R_{IN} is ignored to simplify the implementation in FPGA, this could be one of the reasons for the variations in R_S. However, a variation of ±1Ω is well within the permissible limit of the FDI. To limit the variations and to ensure high SNR, it is recommended to use high input voltage for measurements.

The measured C_{gf} was found to have a minimum accuracy of 100 µV/V at all the tested voltage levels. The ratio of R_S and R_{IN} used to determine C_{gf} can tolerate variations in R_S in the range of 100 Ω to guarantee this accuracy.

4.1.2 Effect of Number of ADC samples

As the number of samples increase, the noise and inaccuracies are averaged and it improves the overall accuracy but it increases the calibration time. Therefore, it is necessary to ascertain the effect of the samples on the accuracy of the measurement. The experiment in section 4.1.1 is repeated for N= 2^{15} and 2^{20} samples. In both the cases, no variations were observed in R_S and C_{gf} for both the resistors. With the

current design, we could obtain a high accuracy with minimum calibration time by using the least number of samples (1024) in the system.

4.2 DAC Calibration

The deviation in the C-DAC transfer curve is determined at the negative full-scale for the offset error and at the positive full-scale for gain error. The end-points are selected in the range of ± (8 to 9 V) to avoid the non-linear region of the C-DAC. In the experiment described below, 8.75 V and -8.75 V are selected for the calibration.

The C-DAC is first calibrated to remove the offset error using O-POT, followed by gain calibration using G-POT. The offset of the DAC for low-voltage high-gain configuration (LV-config) is determined by setting the input to -8.75 V. The O-POT is then adjusted to trim the offset by trial and error. The gain error is nullified by setting the input to 8.75 V and adjusting the G-POT until the voltage deviation is minimised. The corresponding G-POT value is the gain coefficent. The input is then set to 0 V and the offset is trimmed further using the O-POT to obtain the final offset coefficient. These coefficients are stored in the O-POT and G-POT wishbone registers as initialization values for C-DAC calibration. This experiment is repeated for low-voltage high-gain configuration (HV-config) by setting the inputs to -87.5 V, 0 V and 87.5 V. Tables 4.3 and 4.4 show the voltage deviations and the DPOT correction value for LV-config and HV-config.

Table 4.3: Calibration values for LV-config

Input(in V)	Pre-calibration (in V)	Post-calibration(in V)	POT value (in hex)
0	0.2520 m	3.8 μ	28A
8.75	8.74932	8.75001	077
-8.75	-8.74882	-8.75001	

Table 4.4: Calibration values for HV-config

Input(in V)	Pre-calibration	Post-calibration(in V)	POT value (in hex)
0	7.65 m	0.165 m	22F
87.5	87.5181	87.5010	380
-87.5	-87.5034	-87.5013	

A comparison of DAC error for the end-points before and after calibration denoted by E_{pre} and E_{post} is shown in Fig. 4.1. The error is calculated using:

$$E_{pre} = \frac{V_{\mathrm{a}} - V_{\mathrm{pre}}}{V_{\mathrm{a}}} \times 100 \tag{4.3}$$

$$E_{post} = \frac{V_{\mathrm{a}} - V_{\mathrm{post}}}{V_{\mathrm{a}}} \times 100 \tag{4.4}$$

where V_a is the end-point input voltage, V_{pre} is the output before calibration and V_{post} the voltage after calibration.

Figure 4.1: Margin of error reduction in DAC after calibration.

4.3 ADC Calibration

The best-fit method is tested for N=4, 8, 16 and 32 points using 2^{16} samples per best-fit point for a gain of 1. The test set-up for the ADC calibration is shown in Fig. 4.2.

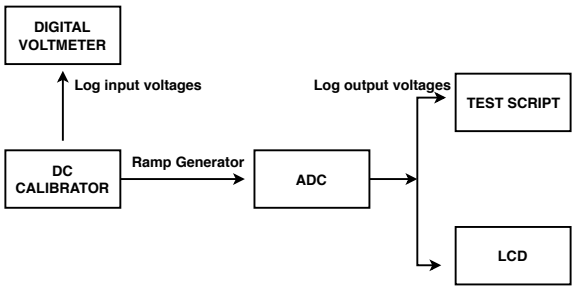

Figure 4.2: Block diagram of ADC calibration test set-up.

A DC calibrator, Yokogawa GS200 [16] is used to generate a voltage ramp in the

range [-7 V, 7 V]. The generated voltages are measured using a digital voltmeter, Keysight 34470A [19] that provides readings with 7.5 digit accuracy. This feature is particularly useful to measure the LSB which requires 7 digit accuracy. The generated ramp is fed to the ADC and the output is logged by a linux-based script that is synchronised to the calibrator. It logs the ADC output and converts the signed hexadecimal to decimal values for data analysis.

The output deviation in LSB, D_{cal}, is calculated using the below formula:

$$D_{\text{cal}} = \frac{V_{\text{in}} - V_{\text{ADC}}}{\text{LSB}} \tag{4.5}$$

wherein V_{in} is the ramp voltage, V_{ADC} is the corresponding ADC output and LSB = 19 µV. Fig. 4.3 reports the output deviation post calibration for different best-fit points. The results show that the deviation is minimum for 32 points which has an average accuracy of 2.17 LSB for a gain of 1. Though this design registers a higher accuracy (order of 3) from the previous version, there are cases where the calibration accuracy is lower than 3 LSB. This could be due to the following reasons:

1. Non-linearity of the ADC transfer curve at higher voltages could adversely affect the slope of the best-fit curve resulting in higher deviations.
2. The measurement set-up operating at voltages in μV range is highly susceptible to external noise.
3. Offset errors induced due to the length of the cables used in the test set-up. The instruments used for testing (calibrator, voltmeter) are themselves prone to noise and could possibly affect the accuracy of the readings.

Table 4.5 shows the gain and offset errors of all the gains in the system for 32-point best-fit line.

Table 4.5: ADC Gain and offset errors for 12 gains

Gain	Gain error	Offset error (in mV)
0.1	0.998832	-0.458
0.2	0.998787	-0.572
0.5	0.998584	-0.820
1	0.998804	-0.420
2	0.998762	-0.515
5	0.998562	-0.668
10	0.998240	-0.992
20	0.998199	-1.650
50	0.997997	-3.452
100	0.992832	-6.351
200	0.992725	-12.188
500	0.992450	-29.297

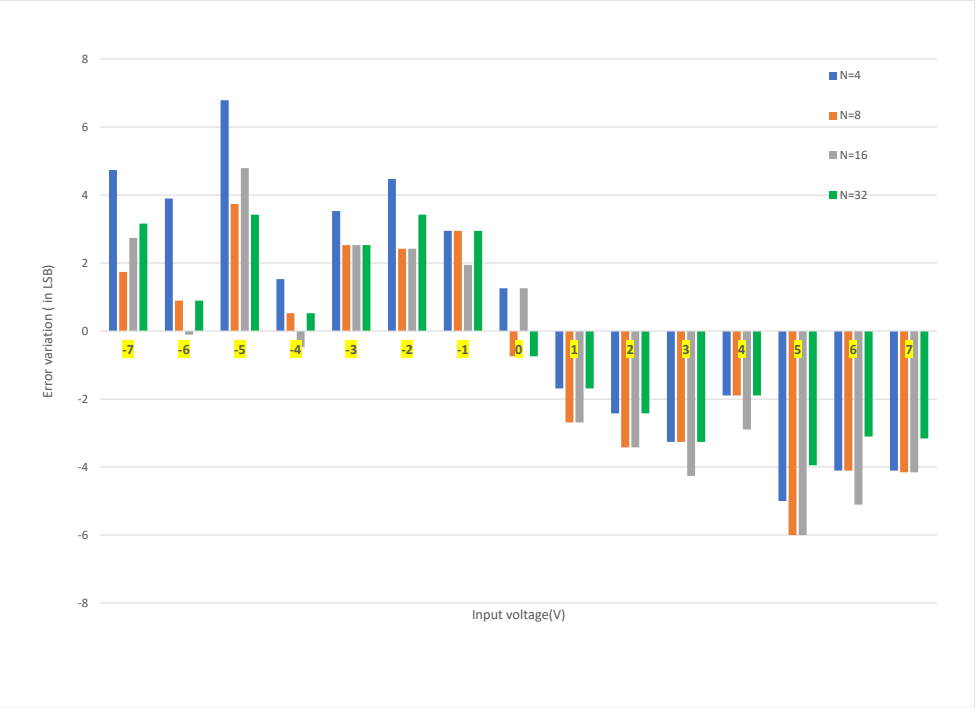

Figure 4.3: Best-fit comparison for N= 4, 8, 16 and 32 points. The y-axis represents the output deviation post best-fit calibration for a gain of 1.

4.4 Fast Digital Integrator

The FDI is tested using a ramp voltage (V_{IN}) in the range [-8, 8] after calibrating the ADC. The residual offset post ADC calibration is trimmed by manually tuning the IPOT until the offset is nullified. Each voltage of the ramp is integrated for 5 triggers with integration interval of 1s each. Each voltage is then averaged to determine the flux deviation.

The flux deviation, D_{flux}, is given by :

$$D_{flux} = \frac{\phi_e - \phi_o}{\text{LSB} \times 1s} \tag{4.6}$$

where ϕ_o is the flux obtained from the integrator, ϕ_e is the expected flux. Since a constant voltage is integrated for a duration of 1 s each, the expected flux $\phi_e = V_{\text{in}}$.

The flux obtained and the error are reported in Fig. 4.4. The FDI registers an average accuracy of 1.74 LSB which is quite close to the goal of this thesis work but there are voltages at which the flux deviation is around 2-4 LSB. In Fig. 4.4, an increase in the error is observed for higher voltages, this is due to the larger

calibration errors and the ADC non-linearity at these voltages. Another source of error is the timebase that measures the integration interval. The counter used in the timebase has a delay of 20 ns owing to the state-machine that requires 2 cycles of 10 ns each to detect the trigger and register the global timer.

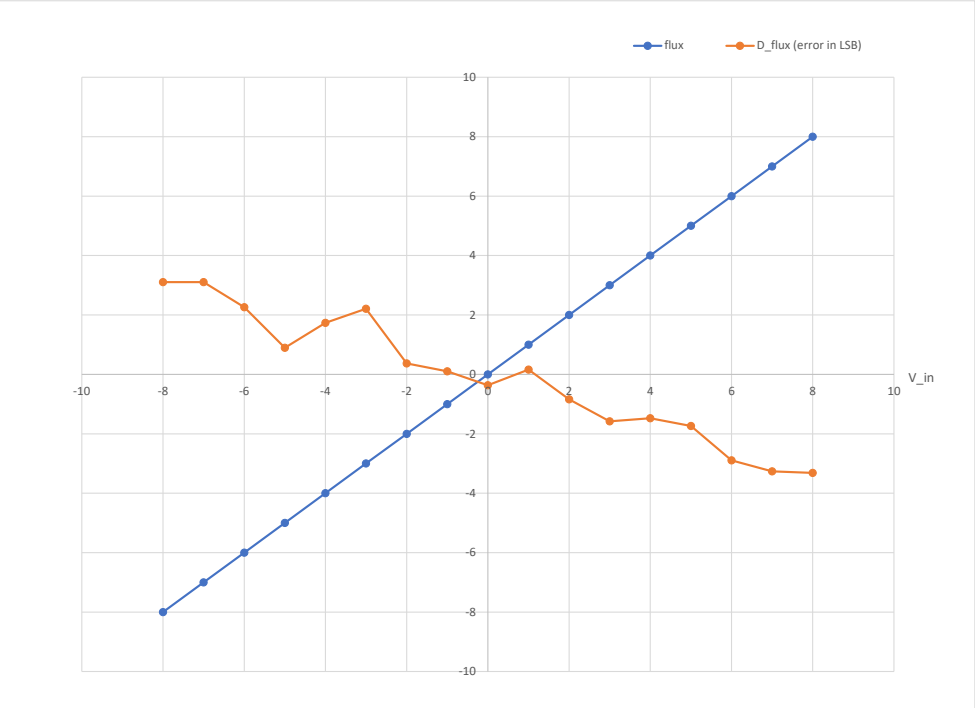

Figure 4.4: Flux and corresponding measurement error in FDI. The x-axis represents the applied voltage. The flux (in V s) and the flux deviation (in LSB) are represented by the y-axis.

5
Conclusion

In this thesis work, we have designed and implemented an auto-calibrating fast digital integrator that can detect and correct coil attenuation, gain and offset errors and determine the magnetic field strength with an accuracy of about 2 LSB. The FPGA-based FDI architecture not only overcomes the accuracy limitations of the previous design [8] but also has lesser maintenance requirements due to the replacement of the DSP by the FPGA which now acts as both the processor and the IO manager. The PGA provides a set of 12 gains that enables the FDI to measure wide range of voltages from 20 mV to 100 V. This feature apart from maintaining adequate SNR also allows us to work with different types of measuring coils (fixed, rotating, stretched wires etc) enabling us to measure various kinds of magnets. The combination of internal calibration for coil resistance, DAC, ADC and external calibration involving IPOT makes the FDI less prone to errors due to temperature, aging, reference voltages, errors in voltage generators etc. The 32-point best-fit method, which is the heart of the calibration system limits the errors in the field measurement to 2 LSB which is about 38 µV. This marks a significant improvement from the previous design considering that the earlier version could ensure an accuracy of about 7 LSB using a 18-bit ADC [7]. The calibration system coupled with the PGA makes the FDI a versatile measurement device that could be employed to measure different types of magnets like dipoles, quadrupoles, superconducting magnets etc under varied conditions of gain and offset errors.

5.1 Limitations

The results obtained for the FDI seem promising and it could very well become the de-facto device for field strength measurement at CERN in the future but the current design has its limitations which are listed below :

1. It is hard to ensure high accuracy and limit the errors to 2 LSB for voltages above 8 V due to the non-linearity of the ADC at high voltages. Due to the time constraints of the thesis work, the ADC non-linearity and measures to counter its effects has not been analysed. As a result, the current design suffers from errors greater than 2 LSB for high voltages.
2. The accuracy of 2 LSB is guaranteed only for gain of 1 as discussed in chapter 4. For higher gains, the accuracy is much lower due to the increased effect of noise and amplification of offset errors. Accuracy for higher gains is beyond the scope of this thesis work and hence has not been considered.
3. The FDI has been tested in the lab which has controlled conditions as opposed

to in-field testing where the hardware is more susceptible to humidity, temperature variations etc. It is likely that accuracy might deteriorate under those conditions and higher number of ADC samples might be required to ensure the same accuracy in field. This results in an increased calibration time.

5.2 Future Work

The potential improvements that could enhance the performance of the FDI are listed below:

1. Investigate the effect of the ADC non-linearity at higher voltages and its effect on calibration. Investigate calibration design schemes that can circumvent this problem.
2. Automatic calibration of IPOT using binary search algorithm instead of manual adjustment for fine offset calibration.
3. Investigate techniques to reduce the latency of Simpson's rule and the effect of this method in reducing the integration errors.
4. The current design uses 67 % of the DSP slices in the FPGA due to several mathematical operations involving Multiply-Accumulate (MAC). Although the hardware resources have not been exhausted yet, it would be prudent to employ reusability of these blocks by creating an arithmetic block consisting of multipliers, accumulators and dividers that are multiplexed across different modules in the system.

6
Bibliography

[1] Analog-Devices. *AD5292*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD5291_5292.pdf.

[2] Analog-Devices. *AD5660*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD5620_5640_5660.pdf.

[3] Analog-Devices. *AD5791*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD5791.pdf.

[4] Analog-Devices. *AD8675*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8675.pdf.

[5] Analog-Devices. *AD8676*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8676.pdf.

[6] P. Arpaia, U. Cesaro, and P. Cimmino. "Enhanced fast digital integrator for magnetic measurements". In: *Review of Scientific Instruments* 88.8 (2017), p. 085103.

[7] P. Arpaia, V. Inglese, and G. Spiezia. "Performance Improvement of a DSP-Based Digital Integrator for Magnetic Measurements at CERN". In: *IEEE Transactions on Instrumentation and Measurement* 58.7 (July 2009), pp. 2132–2138. ISSN: 0018-9456. DOI: 10.1109/TIM.2008.2006723.

[8] P. Arpaia et al. "A fast digital integrator for magnetic field measurements at CERN". In: *Instrumentation and Measurement Technology Conference, 2006. IMTC 2006. Proceedings of the IEEE*. IEEE. 2006, pp. 67–71.

[9] P. Arpaia et al. "Performance of a fast digital integrator in on-field magnetic measurements for particle accelerators". In: *Review of Scientific Instruments* 83.2 (2012), p. 024702.

[10] L. Bottura and K. N. Henrichsen. *Field measurements*. Tech. rep. CERN, 2002.

[11] Campbell-Scientific. *Voltage measurement accuracy, self-calibration, and ratiometric measurements*. 1.04.2018. URL: http:/www2.ece.rochester.edu/courses/ECE111/voltaccy.pdf.

[12] CERN. *About CERN*. 5.09.2018. URL: https://home.cern/about.

[13] CERN. *TE-MSC-CERN*. 22.12.2017. URL: https://te-msc-mm.web.cern.ch/about-us.

[14] Omron Electronic Components. *G6K-Surface Mounting Relay*. 2018. URL: http://omronfs.omron.com/en_US/ecb/products/pdf/en-g6k.pdf.

[15] P. Galbraith. *Portable digital integrator*. Tech. rep. 1993.

[16] GS200. *DC-Calibrator*. 2018. URL: https://cdn.tmi.yokogawa.com/IMGS210-01EN.pdf.

[17] E. H. Hall. "On a new action of the magnet on electric currents". In: *American Journal of Mathematics* 2.3 (1879), pp. 287–292.

[18] J. F. Kenney and E. S. Keeping. *Mathematics of statistics*. Vol. 1. Van Nostrand Princeton, NJ, 1962, pp. 199–237.

[19] Keysight. *34470A-DVM*. 2018. URL: https://literature.cdn.keysight.com/litweb/pdf/5991-1983EN.pdf?id=2318052.

[20] Linear-Technology. *LTC2378-20*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/237820fb.pdf.

[21] Linear-Technology. *LTC6090*. 2018. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/6090fe.pdf.

[22] F. Maloberti. *Data converters*. Springer Science & Business Media, 2007.

[23] J. R. Nagel. *Introduction to Numerical Integration*. 2018. URL: http://www.ece.utah.edu/~ece6340/LECTURES/Jan30/NumericalIntegration.pdf.

[24] G. Spiezia. "A Fast Digital Integrator for magnetic measurements". PhD thesis. University of Naples Federico-II, 2008.

[25] L. Walckiers. "Magnetic measurement with coils and wires". In: *arXiv preprint arXiv:1104.3784* (2011).

[26] Wishbone. *Wishbone documentation*. 13.02.2018. URL: https://www.ohwr.org/projects/wishbone-gen/wiki/wbgen2-documentation.

[27] Wishbone-Interface. *Wishbone System-on-Chip (SoC)Interconnection Architecture for Portable IP Cores*. 2011. URL: https://cdn.opencores.org/downloads/wbspec_b3.pdf.

A

Appendix 1

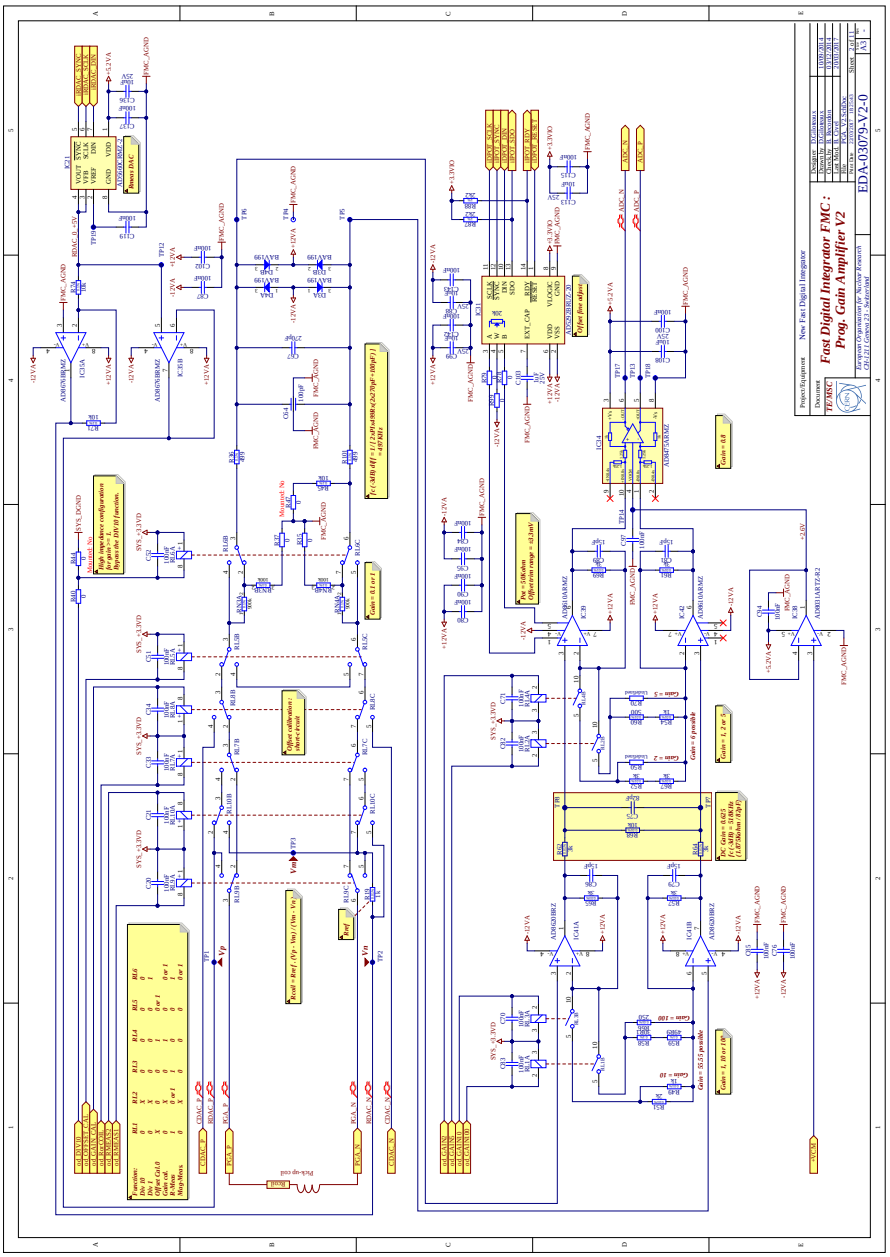

Figure A.1: Analog front end comprising of PGA and IPOT [Image source: CERN]

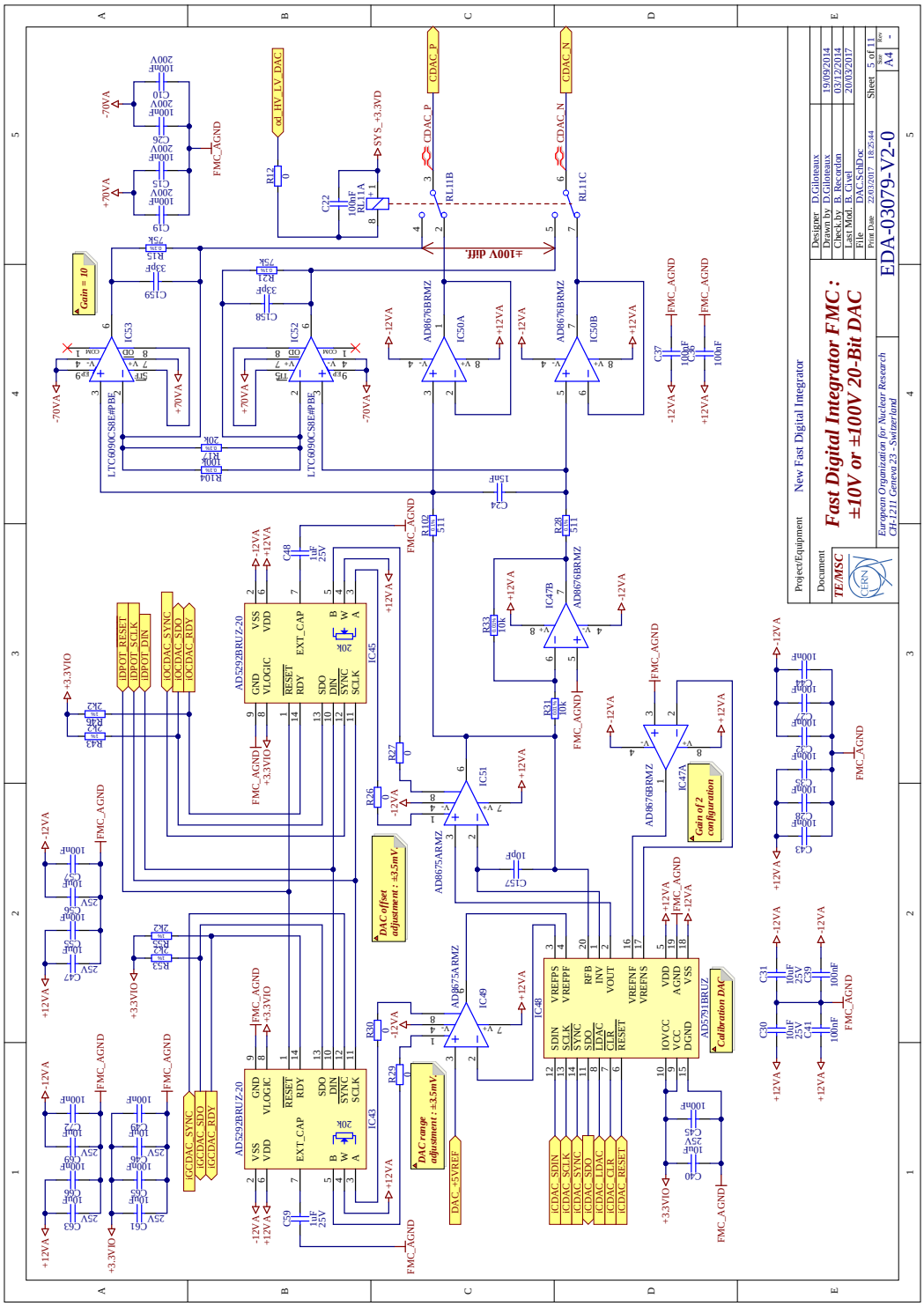

Figure A.2: High-voltage and low-voltage configuration for DAC and GPOT-DPOT schematic [Image source: CERN]