CHALMERS
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# A Deeply Integrated Active Antenna

## PCB Bow-tie Antenna integrated with a Tunnel Diode

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Electrical Engineering
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Gothenburg, Sweden 2017

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# Abstract

The trend to operate next generation wireless systems at higher frequencies is made possible by employing increasingly smaller electronic components while achieving higher levels of system integration at the same time. Ultimately, the wireless system becomes integrated into a single multifunctional component, or single inhomogeneous material. This phenomenon is described by the term "Deep Integration" and requires a novel co-design approach that differs from a traditional "bottom-up" design flow. The Deep Integration top-down design flow yields a merged system that is potentially more optimal than when a traditional interconnected subsystem approach is followed.

A first investigation is made into a self-amplifying antenna consisting of a bow-tie PCB antenna and a tunnel diode. The co-design requires the use of both the electromagnetic simulation software CST and the circuit solver ADS. It is explained how this design, a so-called antennafier, can provide higher overall power gain (e.g. EIRP) relative to its passive counterpart. A prototype design is described and recommendations are given that will lead to improved active antenna designs in the future.

Keywords: Deep Integration, Active Integrated Antenna, Tunnel Diode, CST, ADS

# Acknowledgements

At this point, I would like to thank my supervisor, Rob Maaskant, for the opportunity that he gave me to work on a such interesting master thesis and also for his triggering help that made me go on until the end. Furthermore I would like to express my appreciation to my co-supervisor, Christian Fager, for his invaluable suggestions and recommendations whenever needed.

Last but not least, I would like to dedicate this master thesis to my family, without their huge support I would not have managed to achieve my goals and dreams.

Nikolaos Kollatos, Gothenburg, August 2017

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# Introduction

## 1.1 Deep Integration

The classical "bottom-up" design approach that is followed in the design process of wireless systems typically assumes that every component used in the system has a common reference impedance and needs to be matched and optimized as if they were isolated from each other. A different concept was recently proposed, where every component is no longer optimized in isolation and all of them are integrated over the same substrate, eventually merged into one large system which meets the specific design requirements [1]. This concept is called "Deep Integration" and a system designed with this approach merges the functionalities of separate components into a compact unit, among which the antenna and electronics, as e.g. shown in Fig. 1.1. Furthermore, EM subsystem interference is potentially eliminated because it is designed as one system, so the entire system is expected to have a better overall performance.

The term "antennafier", which was introduced back in the 1960s and is found in various research projects and publications ([10, 14, 17, 26, 27]), describes the integration of an antenna system with an amplifier on the same structure and combines both subsystems into one. The system keeps the advantages of both subsystems and also becomes more compact which is an important issue on modern communication systems.

In this project, a prototype design is presented which incorporates a bow-tie antenna and a tunnel diode integrated on the same PCB and placed inside the antenna conductor. The diode is DC-biased through the antenna conductors. The tools used for the co-simulations were the EM software CST and the circuit design tool ADS for modelling the electronic component. The aim of this work is to take the first steps towards a deeply integrated active antenna system.

## 1.2 Thesis overview

After the introduction to the Deep Integration concept in this chapter, the second chapter describes the modelling and electrical characteristics of the tunnel diode. Then, chapter 3 presents the main design process which is the simulation of the passive antenna and the 3-port network approach of the active antenna. It also

compares two different antennas that were simulated. Chapter 4 includes the system fabrication and the measurement results and compares them with the simulations. Last, in the fifth chapter the conclusion and some recommendations for future work can be found.

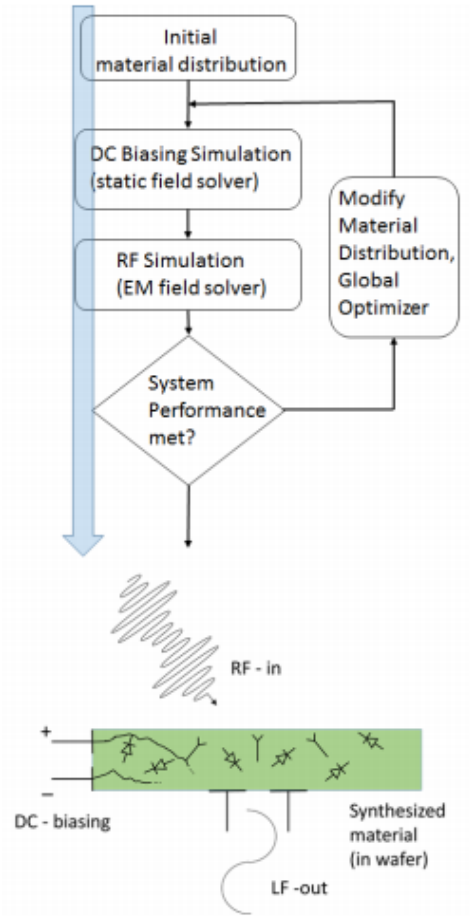



**Figure 1.1:** Deep Integration – a new material synthesis concept

# 2

# The Tunnel Diode

This chapter is an introduction to the nonlinear device that is used in this project, i.e. the tunnel diode (TD), describes its electrical characteristics, and shows an elementary circuit where the TD acts as an amplifier.

## 2.1 Introduction

A Tunnel Diode (TD) is a highly-doped semiconductor device with nonlinear behavior, which is widely known for its ability to exhibit Negative Differential Resistance (NDR). The working principle of this device is based on the tunnelling effect, which is a quantum mechanical phenomenon. Details on quantum tunnelling effects are beyond the scope of this project and can be found in [3].

A TD can work well into the microwave frequency region and thanks to the NDR it is used in different applications such as oscillators, amplifiers and switching circuits [3]. Its main advantages are the high switching speed, the low power dissipation as it works at relatively low DC voltage and current, the ease of integration in most circuits where being used and the durability that it has, even in high temperature conditions [3]. Furthermore, diodes in general are the most fundamental building blocks in electronics as they can be used to represent pn-junctions even inside transistors or other semiconductor devices. This and the NDR properties are the main reasons for which the TD has been chosen in this particular project on Deep Integration.

On the contrary, one main drawback of this device is the low voltage swing in the negative resistance region which limits us from using high amplitude signals. Furthermore, a TD works properly in the application circuits mentioned above only when it is biased in the NDR region, so care must be given when designing a circuit that contains this device.

## 2.2 Tunnel Diode Characteristics

In this section, the characteristics of the TD will be presented. The symbol of the tunnel diode is shown in Fig. 2.1

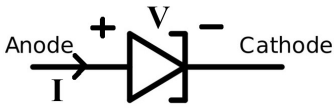



**Figure 2.1:** Electrical symbol of a Tunnel Diode

In this project, the tunnel diode model 1N3716 [4] is used and its characteristic values of currents and voltages that were used for the calculations of I-V curve are given in Table 2.1.

**Table 2.1:** TD's characteristics (to be discussed in 2.5

| | | | |
|---|---|---|---|
| $V_\mathrm{p}$ | 65 mV | $I_\mathrm{p}$ | 4.7 mA |
| $V_\mathrm{v}$ | 350 mV | $I_\mathrm{v}$ | 0.6 mA |
| $T$ | 300 K | $n$ | 1 (for Germanium) |

### 2.2.1 I-V curve and electrostatic nonlinear model

It is already mentioned that this diode exhibits a nonlinear I-V behaviour. This nonlinearity of the I-V curve is the result of three different phenomena, so there are three different mathematical terms the superposition of which forms the overall I-V curve. The independent variable is the applied voltage (V) and the dependent is the current (I). These three terms are given as [28]:

1. The tunnelling current, $I_\mathrm{t}$, which describes the tunnelling effect and includes the negative resistance region of the diode's I-V curve. This current is given by

$$I_\mathrm{t} = \frac{I_\mathrm{p}}{V_\mathrm{p}} V \left(1 - \frac{V}{V_\mathrm{p}}\right) \tag{2.1}$$

where $I_\mathrm{p}$ is the peak current of the diode, $V$ is the applied voltage and $V_\mathrm{p}$ is the peak voltage of the I-V curve.

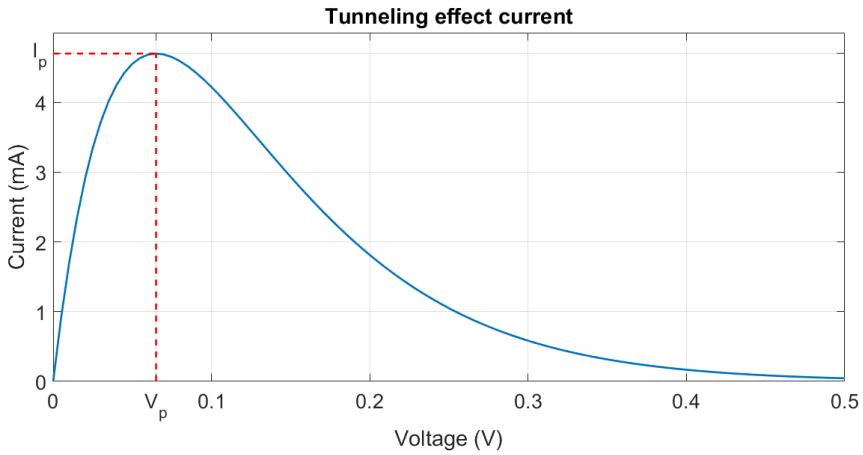



**Figure 2.2:** Tunneling Effect Current $I_\mathrm{t}$

2. The excess current, $I_x$, which describes impurities of the device and usually sets the minimum value of the valley voltage ($V_v$). It is given by

$$I_x = I_v e^{(A_2(V-V_v))} \tag{2.2}$$

where $I_v$ is the valley current, $V_v$ is the valley voltage and $A_2$ is the excess factor which is used for scaling.

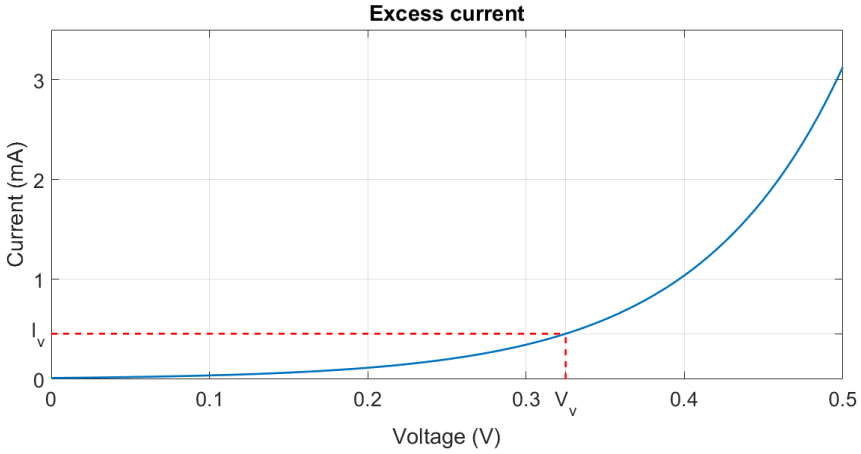



**Figure 2.3:** Excess Current $I_x$

3. The normal diode current, $I_d$, which describes the device's nature as a diode. It is given by

$$I_d = I_s(e^{(qV/nkT)} - 1) \tag{2.3}$$

where $I_s$ is the saturation current, $q$ is the electron charge, $n$ is the ideality factor, $k$ is Boltzmann's constant and $T$ is the room temperature. (see Table 2.1)

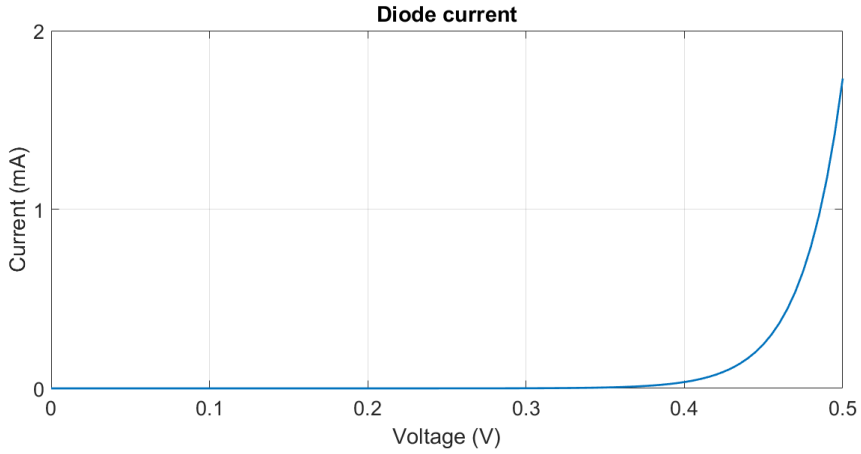



**Figure 2.4:** Normal Diode Current $I_d$

The superposition of the above terms gives the current of the tunnel diode $I$, which is shown in Fig. 2.5

$$I = I_t + I_x + I_d \tag{2.4}$$

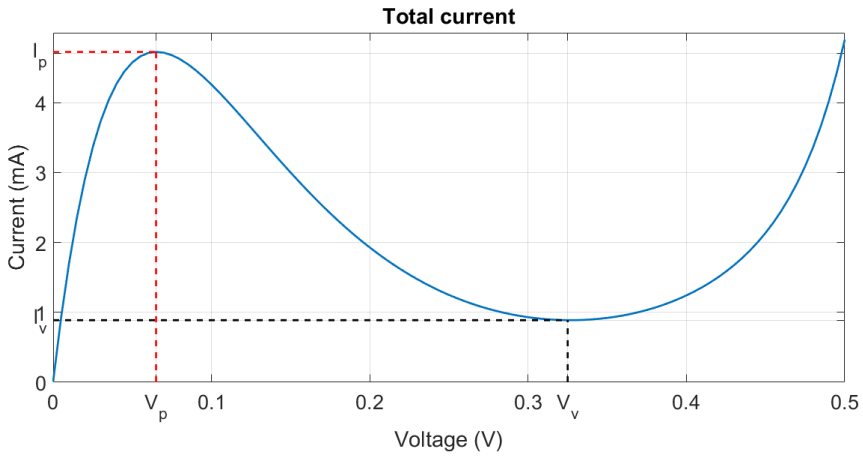



**Figure 2.5:** Tunnel Diode Current $I$

From Fig. 2.5 it is clear that there exists three regions in which the I-V curve can be decomposed under forward bias condition. These regions are the following:

1. From zero voltage until the peak voltage $V_\mathrm{p}$ the current is increasing and reaches the peak current $I_\mathrm{p}$.
2. Although the voltage is increasing further, the current is now decreasing (due to the tunnelling effect) until it reaches the valley current $I_\mathrm{v}$ (and the corresponding $V_\mathrm{v}$). This is the negative resistance region.
3. When the voltage continues to increase beyond the valley voltage the current increases too and eventually follows the normal diode's current law.

In order this diode to work as a NDR it must be biased in the second region. An assumption should be made about the voltage range where the curve can be considered linear. In this project, it is assumed that the linear region is between 0.1 V and 0.2 V, so the diode is biased in the middle point, therefore the operating point is at $V_\mathrm{dc} = 150$ mV and $I_\mathrm{dc} = 3$ mA.

The value of the negative resistance can be calculated by finding the gradient of the curve at the operating point. By doing so, this value is $R_\mathrm{n}$ = -40 Ω.

The implementation of Eqs. (2.1) to (2.4) and the resulting plots were done and created in MATLAB, respectively. The excess factor $A_2$ is equal to 11 (emperically determinded).

### 2.2.2 Electrodynamic model and linear equivalent circuit model

In RF circuit design the tunnel diode is modelled under small-signal excitation by its equivalent linear circuit where the different parasitic capacitances are taken into account. When biased in the NDR region the electrodynamic model of the Tunnel Diode is displayed in Fig. 2.6, modelled in ADS.

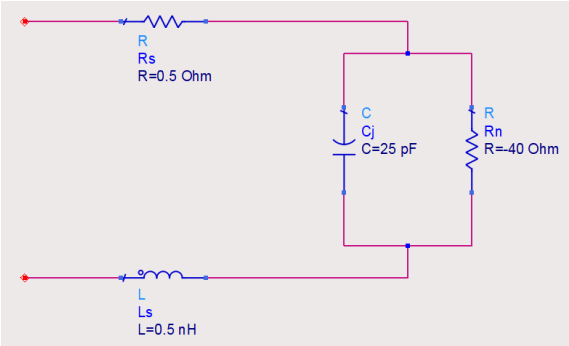



**Figure 2.6:** Equivalent small-signal circuit model of the Tunnel Diode when biased in the NDR region

As seen in Fig. 2.6, this equivalent circuit consists of a series resistance ($R_\mathrm{s}$), a series inductor ($L_\mathrm{s}$) and the parallel connection of a capacitor ($C_\mathrm{j}$) and the negative resistance ($R_\mathrm{n}$). The inductance, capacitance and negative resistance (or conductance as given in the datasheet [4]) represent the intrinsic and extrinsic package parasitics of the device which determine the self-resonant frequency of the device, i.e. the frequency at which the imaginary part of the equivalent input impedance ($Z_\mathrm{in}$) of the device is zero. The values of the components in the schematic of the above figure are taken from the diode's datasheet and are henceforth used in this project.

The input impedance of the equivalent circuit of Fig. 2.6 is calculated as

$$Z_\mathrm{in} = R_\mathrm{s} + j\omega L_\mathrm{s} + \left(\frac{1}{j\omega C_\mathrm{j}}\right) || R_\mathrm{n} \tag{2.5}$$

The real and imaginary parts of $Z_\mathrm{in}$ are shown in Fig. 2.7, where it can be seen that the self-resonant frequency is $f_\mathrm{res} = 1.4$ GHz.

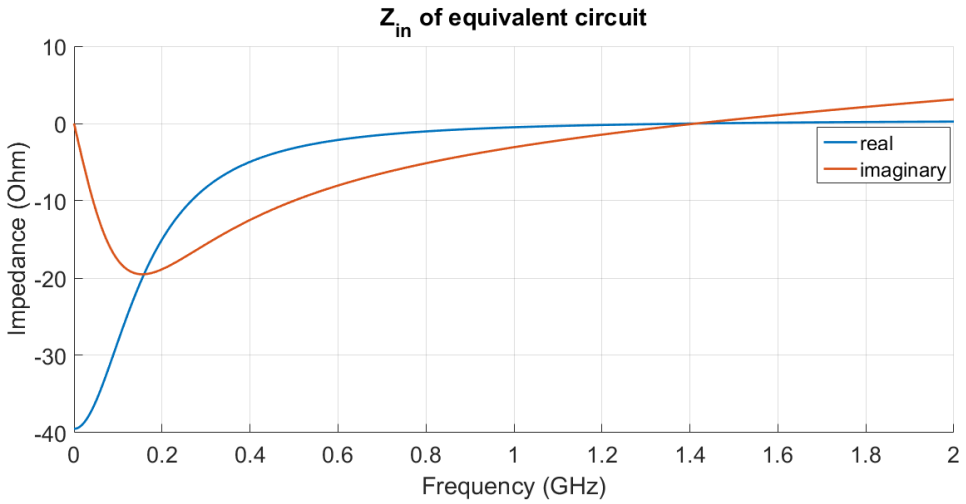



**Figure 2.7:** Real and Imaginary parts of $Z_\mathrm{in}$

## 2.3 An amplifier circuit

### 2.3.1 Voltage and Power Gain

In this section, a simple amplifier circuit will be presented, which consists of a resistor and the diode described as a negative resistance $R_{\mathrm{n}}$. The purpose of this is to show that a device with a negative resistance can amplify AC signals applied to them, as long as it is biased properly. The schematic of the basic circuitry is shown in Fig. 2.8.

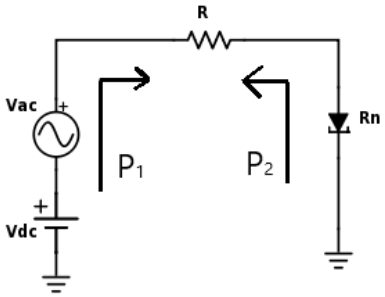



**Figure 2.8:** Schematic of a simple amplifying circuit

In the analysis the diode is modelled as a negative resistance and the circuit is just the connection of $R$ and $R_n$ in series. The AC source is used to supply the circuit with the signal of proper amplitude (voltage or current) and the DC source is used to bias the tunnel diode in the negative resistance region. This is the condition that allows the diode to be modelled as a single resistance with negative value.

At RF, the circuit of Fig. 2.8 is then a simple circuit with two resistors in series. The analysis of this circuit is as follows:

The input voltage $V_{\mathrm{in}}$ is an AC voltage source, so $V_{\mathrm{in}}$=$V_{\mathrm{AC}}$. The output voltage is measured as the voltage across the load resistance $R$, as seen in Fig. 2.8. In order to find the output voltage one can apply the simple equation of a voltage divider, thus

$$V_{\mathrm{out}} = \frac{R}{R + R_{\mathrm{n}}} V_{\mathrm{in}} \tag{2.6}$$

The voltage gain is defined as the ratio of the output voltage ($V_{\mathrm{out}}$) over the input voltage ($V_{\mathrm{in}}$), i.e.

$$A_{\mathrm{v}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{R}{R + R_{\mathrm{n}}} \tag{2.7}$$

This voltage gain can be higher than 1 because of the negative resistance which makes the sum of the denominator of Eq. (2.7) smaller than the numerator (in absolute value). It can also take negative values which means that the output and input voltages have a 180° phase difference. The following plot shows how $A_{\mathrm{v}}$ changes when $R$ takes values from 0 to 100 Ω, while $R_{\mathrm{n}}$=-40 Ω.

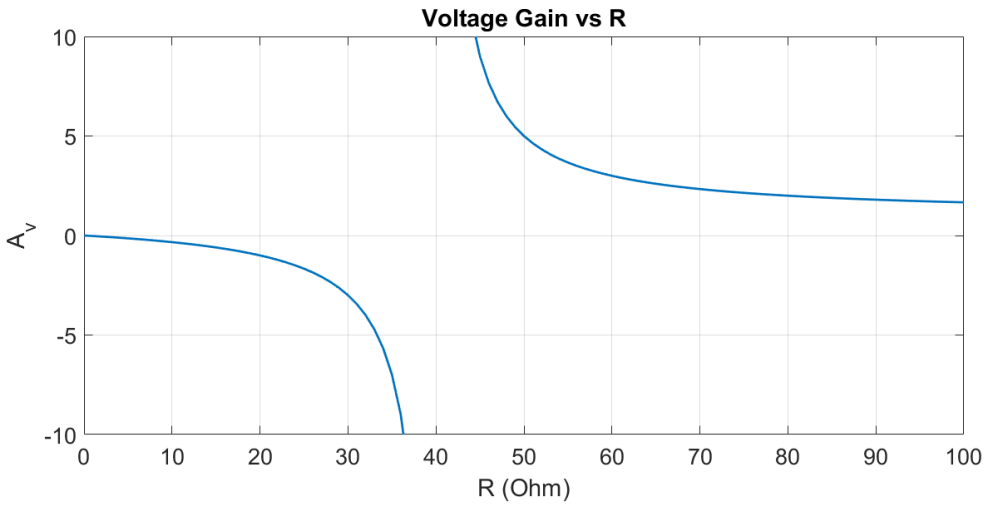



**Figure 2.9:** Voltage Gain ($A_v$) versus Resistance ($R$)

Next, a nonlinear circuit is simulated in ADS to examine the large-signal behaviour. For this purpose we make use of the electrostatic nonlinear I-V characteristics of the diode, instead of considering it as a resistor with a negative value (though not more realistic because parasitics are now neglected). This circuit also contains an AC source with internal impedance ($Z_s$) (fixed value of 50 Ω), an ideal capacitor that blocks the DC current, an ideal inductor that acts as a DC feed for the DC source and two current probes, $I_{probe1} = I_{probe2}$, which are used to measure the power dissipation at the load resistance $R$. Fig. 2.10 shows the circuit diagram

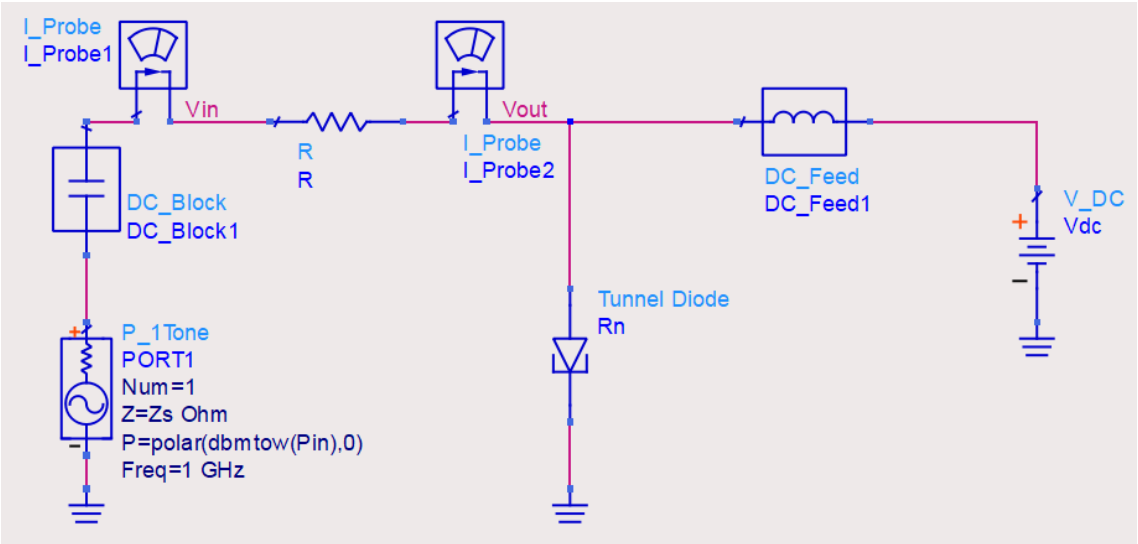



**Figure 2.10:** ADS circuit diagram of the amplifier setup

The resistance $R$ is again variable from 0 to 100 Ω and now the diode is modelled using the equations from Sec. 2.2.1. The voltage gain is calculated as $V_{out}/V_{in}$ and is shown in Fig. 2.11

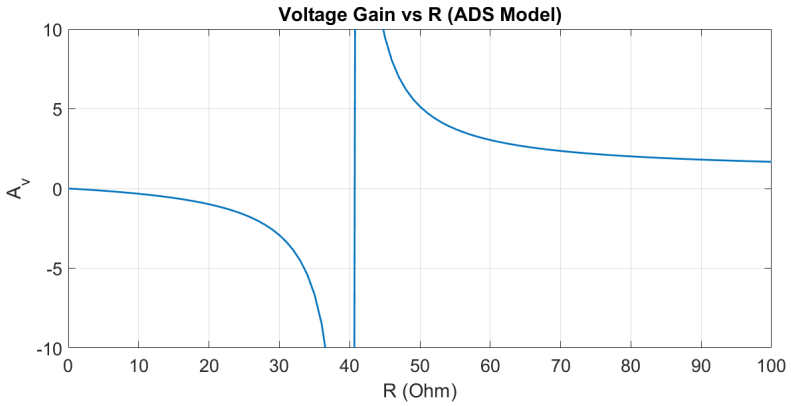



**Figure 2.11:** Voltage Gain ($A_\mathrm{v}$) versus Resistance (ADS model)

It is obvious that Figs. 2.9 and 2.11 are in good agreement and it is clear that the voltage gain is between 1 (when $R$ is 0 and $R_\mathrm{n}$ different than 0) and $\pm$ infinity (when $R$ tends to $R_\mathrm{n}$). For values of $R$ less than $|R_\mathrm{n}|$ the voltage gain becomes negative.

In order to find the power gain, the following definition is used (see Fig. 2.8)

$$G_\mathrm{p} = \frac{P_1 + P_2}{P_\mathrm{in}} \tag{2.8}$$

where $P_1$ is defined as the power that the source delivers to the resistance $R$ (after some dissipation in its source impedance $Z_\mathrm{s}$), $P_2$ is defined as the power flowing from the common node between $R$ and tunnel diode into $R$ and $P_\mathrm{in}$ is the available power from the source, i.e.,

$$P_1 = \frac{1}{2}\,\mathrm{Re}(V_\mathrm{in} I_1^*) \tag{2.9}$$

$$P_2 = -\frac{1}{2}\,\mathrm{Re}(V_\mathrm{out} I_2^*) \tag{2.10}$$

and $I_1$=$I_2$.

The power gain with respect to the value of the resistance $R$ is plotted in Fig. 2.12

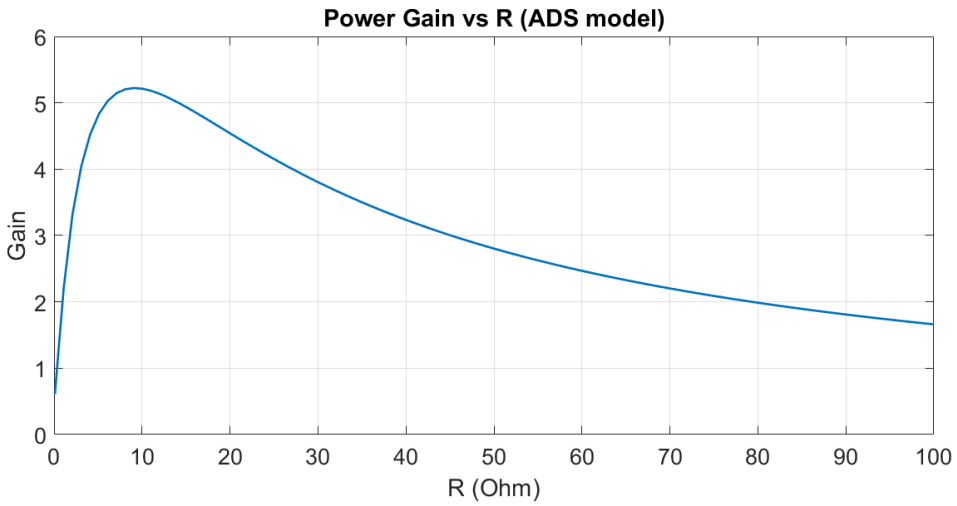



**Figure 2.12:** Power Gain ($G_\mathrm{p}$) versus Resistance $R$ (ADS model)

The way that power gain is defined shows two things:

1. The numerator $P_1+P_2$ should be higher than the available power $P_\mathrm{in}$ from the source in order to have gain. From Fig. 2.12 it is obvious that this happens in the circuit of Fig. 2.10.
2. $P_2$ is positive which means that power flows back to the resistance (see Fig. 2.8) and this is caused by the tunnel diode and its ability to present negative resistance. A positive change in the voltage causes a negative differential change in the instantaneous current, so the device actually generates power and gives it back to the circuit (active device) [5].

### 2.3.2 Load line example

The load line analysis is used in order to find the operating point (OP) and acceptable level of output signal without it being distorted. This analysis is applied to the circuit of Fig. 2.13 (as in [29])

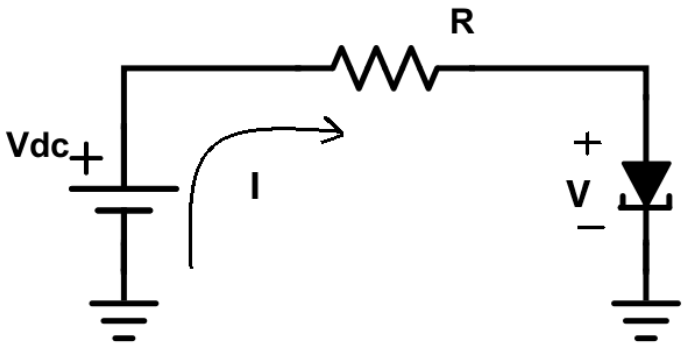



**Figure 2.13:** Load line circuit

It was mentioned above that the region where a fair assumption about the linearity of the I-V curve can be made, is between 0.1 V and 0.2 V. The operating point is in the middle of this range (0.15 V). At this point, the tangent line to the curve represents the negative resistance of the device. For this example, a value of 30 Ω is used for the load resistance. The load line is the line that passes through the operating point and satisfies the equation

$$V = V_{\mathrm{dc}} - IR \tag{2.11}$$

where $V_{\mathrm{dc}}$ is the DC source voltage and $IR$ is the voltage drop across the load resistor $R$.

The load line is steeper than the tangent line because the resistance is lower and because it is crucial for stability reasons that it does not meet the I-V curve at no more than one point. Otherwise there will be multiple operating points and the circuit will not be stable. $V_{\mathrm{dc}}$ is the DC source voltage and is equal to $V$ when the current is zero, i.e. it is equal to the open-circuit voltage ($V_{\mathrm{oc}}$). On the other hand, when $V$ is zero, the current is called short-circuit current ($I_{\mathrm{sc}}$) and is equal to

$$I_{\mathrm{sc}} = \frac{V_{\mathrm{oc}}}{R} \tag{2.12}$$

The crossing points with the x-axis and y-axis are $V_{\mathrm{oc}}$=0.24 V and $I_{\mathrm{sc}}$=8 mA, respectively.

The last thing that comes out from this analysis is the acceptable level of output (and input) voltage level without distortion. This is shown in Fig. 2.14. Two lines parallel to the load line are drawn that indicate the input voltage swing $V_{\mathrm{in}}$ (peak-to-peak), which in this case is 20 mV. Then, the output voltage swing $V_{\mathrm{out}}$ is found by observing the crossing points of the two above lines with the I-V curve. The difference between them is the output voltage (p-p), which in this case is 70 mV. Combining the above, the voltage gain is equal to

$$A_{\mathrm{v}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{70\mathrm{mV}}{20\mathrm{mV}} = 3.5 \tag{2.13}$$

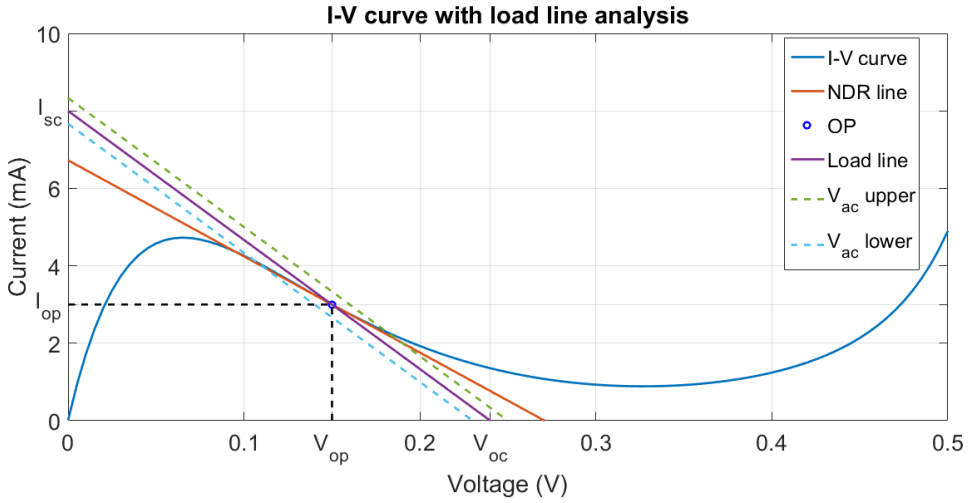



**Figure 2.14:** I-V curve and Load Line analysis

# 3

# The Antennafier

In this chapter, the passive antenna is presented, modelled and simulated in the EM simulation software CST. Then the active structure is introduced and the simulation results are shown.

## 3.1 Introduction

The term "antennafier" used in this project to describe the integrated antenna structure that was introduced back in the 1960's in various scientific papers and studies ( [14], [26], [27]). It usually refers to the integration of an antenna and an amplifier (antennafier), a structure that combines the functions of both devices. The concept of the antennafier is that it keeps the characteristics of the passive antenna (such as radiation pattern, directivity etc.) and can improve its attributes by adding the characteristics of the amplifier (gain).

In this project, the antennafier structure is examined as a first step towards Deep Integration, so the developed prototype may not be optimal but does provide us with hands-on experience. The power gain can be defined as the ratio between the total radiated power (from the antenna) and the available power from the source, i.e.

$$G = \frac{P_{\text{rad}}^{\text{tot}}}{P_{\text{avs}}} \tag{3.1}$$

In a passive antenna this gain is always lower than unity because the antenna cannot radiate more power than what the feeding source can deliver. It should not be confused by the antenna gain, which is the ratio of the radiated power per solid angle in the direction of maximum directivity to the power radiated from a lossless isotropic antenna. Note that the term "total radiated power" is also different in the two cases and it will be explained later in this text.

The designed structure is a bow-tie antenna using coplanar waveguide line (CPW) technology. The main reason for this selection is that the CPW structure is convenient for this type of antenna, it has relatively low losses, it does not need a balun and it provides a ground plane in the same plane as the transmission line (copper strip) without the need of drilling via-holes.

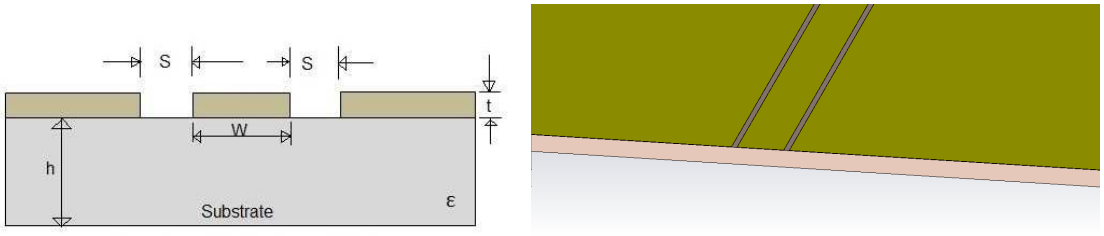
The process that has been followed for this structure includes the design and simulation of the passive antenna in CST, the creation of an equivalent circuit model

in ADS and the combination of the two softwares to perform EM and circuit simulations for the active antenna model, which is considered as a 3-port network (as it will be seen in Sec. 3.4).

A coplanar waveguide is a type of planar transmission line which has a dielectric substrate layer and three metallic conductors on top. The middle conductor is the signal line and the two others are acting as finite ground planes. Both support forward and reverse current waves. More specifically, the structure supports a quasi-TEM mode and the E-field is directed from the middle conductor strip towards the two ground planes (depending upon the phase). The effective permittivity and the line impedance of the CPW are given by equations found in [6], however, in this project a built-in tool in the CST software is used in order to determine the design parameters needed for the CPW. The design parameters of a CPW are:

1. Width of center conductor, $w$
2. Space between center conductor and ground planes, $s$
3. Height of the substrate, $h$
4. Thickness of copper layer, $t$

Fig. 3.1 shows a typical CPW structure




**(a)** **(b)**

**Figure 3.1:** Coplanar Waveguide: (a) design parameters; (b) CST model

The values of the design parameters that were used in this project are given in Table 3.1. The substrate is FR4 with relative permittivity $\epsilon_r$=4.3 and loss tangent tan$\delta$=0.025. Also, the line impedance is $Z_0$=50 Ω.

**Table 3.1:** CPW design parameters

| Parameter name | w | s | h | t |
|---|---|---|---|---|
| Value (mm) | 4.2 | 0.5 | 1.6 | 0.035 |

## 3.2 Passive Antenna and CST Simulations

### 3.2.1 Design Parameters and CST model

The type of antenna selected initially was a bow-tie antenna in CPW technology, which is a type of a wideband dipole antenna and is designed for operation at $f_0$=1 GHz and is matched to a 50-Ohm CPW line. For these types of antennas there are no exact design equations. However, the equations in [7] were used for this antenna as a starting point, after which it was fine-tuned. The geometry of the antenna with the different design parameters and its model in CST are shown in Fig. 3.2.

$$a = \frac{1.6\lambda_0}{\epsilon_r} \tag{3.2}$$

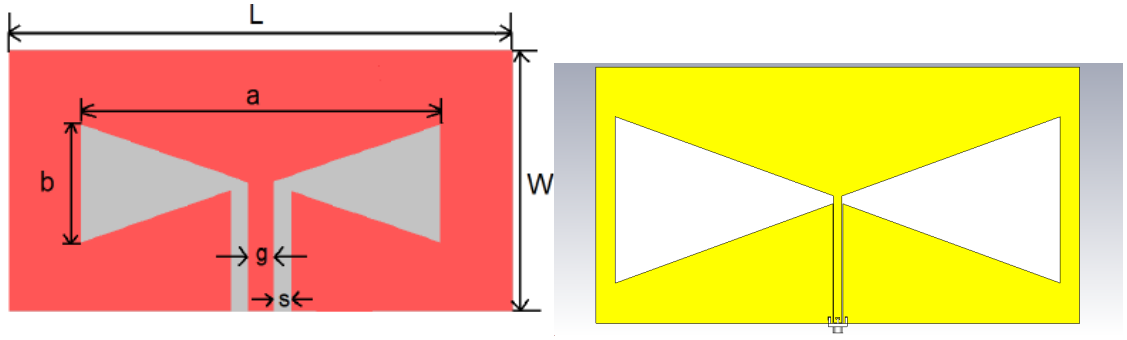
$$b = \frac{0.5\lambda_0}{\epsilon_r} \tag{3.3}$$

$$L = \frac{a}{0.92} \tag{3.4}$$

$$W = \frac{b}{0.55} \tag{3.5}$$

where, $\lambda_0$ is the free-space wavelength and $\epsilon_r$ is the relative permittivity of the substrate material.

The fine-tuned geometrical parameters are listed in Table 3.2. For the feeding of the antenna a common 50-Ohm SMA connector is used (shown also in the figure)




**(a)** Theoretical Design **(b)** CST model

**Figure 3.2:** Coplanar Waveguide: (a) design parameters; (b) CST model

**Table 3.2:** Antenna design parameters

| Parameter name | a | b | L | W |
|---|---|---|---|---|
| Value (mm) | 228 | 85 | 247.83 | 130.77 |

### 3.2.2 Simulations

The simulations were performed in CST. The output parameters include the reflection coefficient ($S_{11}$), realized gain of the antenna, and the E- and H-plane radiation patterns. The reflection coefficient of this antenna shows its wideband property as it is below -10 dB in the frequency range from 0.683–1.31 GHz (Fig. 3.3).

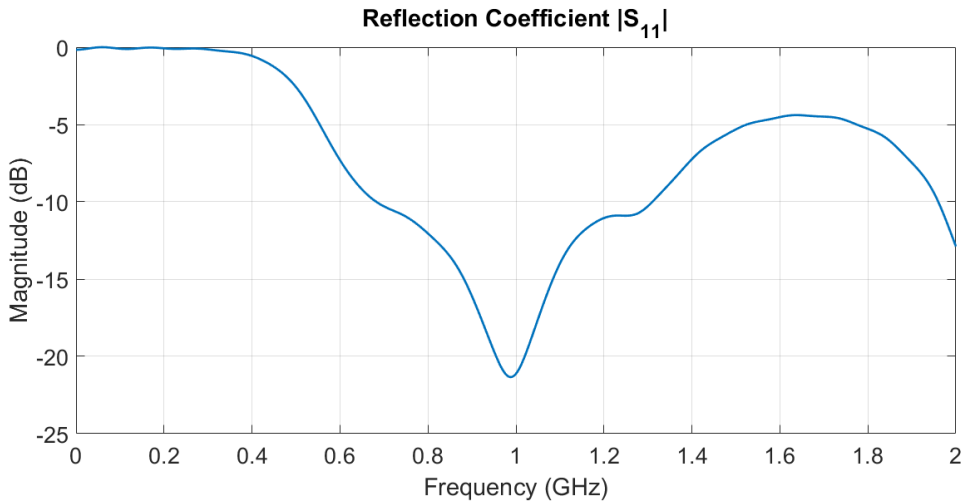



**Figure 3.3:** Reflection Coefficient $|S_{11}|$ in dB

Next, the 3D radiation pattern, the realized antenna Gain, and the E- and H-plane pattern cuts are presented. The antenna radiates in the z-axis direction which is the direction normal to the x-y plane in which the antenna is located.

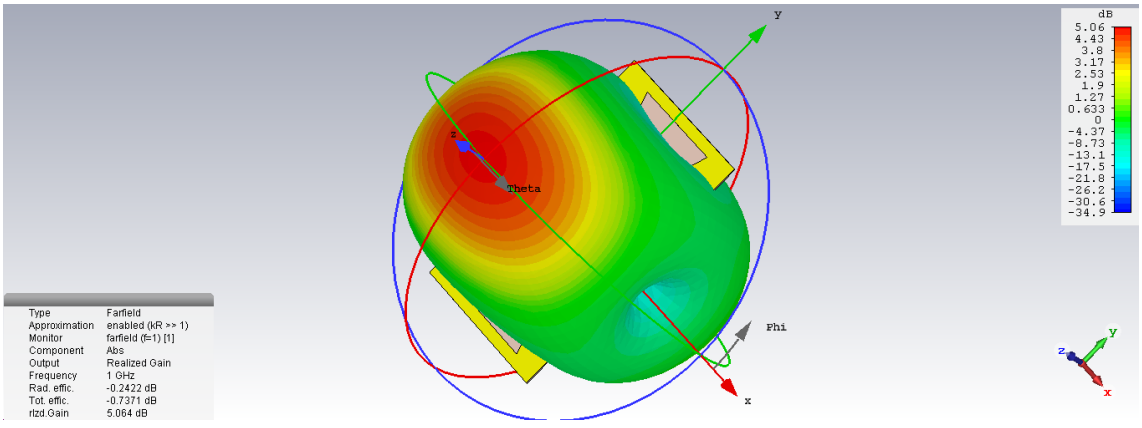



**Figure 3.4:** 3D antenna realized gain pattern

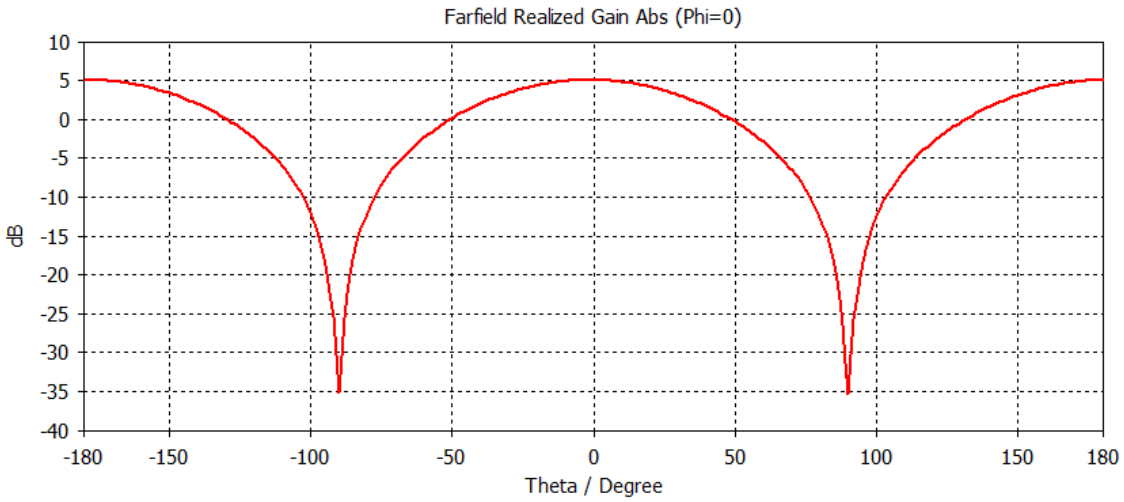
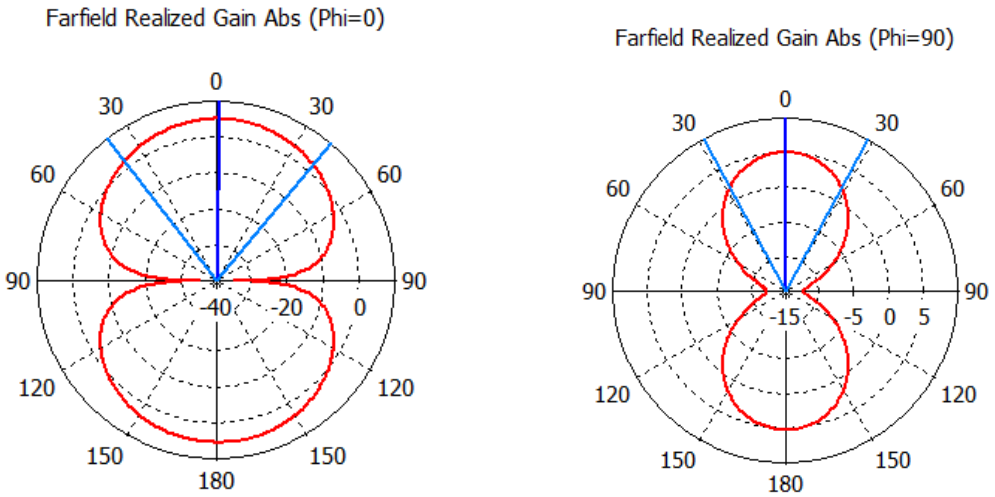



**Figure 3.5:** Cartesian plot of E-plane far-field realized gain pattern




**(a)** E-Plane **(b)** H-Plane

**Figure 3.6:** (a) E-plane pattern; (b) H-plane pattern

From the figures above it is evident that the maximum antenna gain is **5.93 dBi** and it radiates in both directions along the z-axis ($\theta = 0$ and $\theta = 180°$).

## 3.3 Feeding Circuit

The feeding of the passive antenna is through the coaxial 50-Ohm SMA connector which provides the power from the RF source to the antenna. However, in the case of the active antenna, which is the antenna integrated with the tunnel diode, the semiconductor component needs to be biased, so a DC source is needed to provide

the proper biasing as well. The DC and RF signals can be combined either externally and directly on the tunnel diode or internal which means that a bias-tee should be integrated on the PCB and therefore be designed. The external case represents a less integrated solution, thus a DC supply network is designed on the PCB.

A bias-tee is used to bias the desired device with the proper current (or voltage) and also to isolate the DC current from the RF source and the RF signal from the DC source. To this end, a capacitor that allows high frequencies to pass through it and blocks the low frequency signals is placed near the RF source. This is called a DC-block. Accordingly, an inductance that allows the low frequencies to pass through it and chokes the high frequency signals is used. This is called a DC-feed. The schematic of a typical bias-tee is shown in Fig. 3.7.

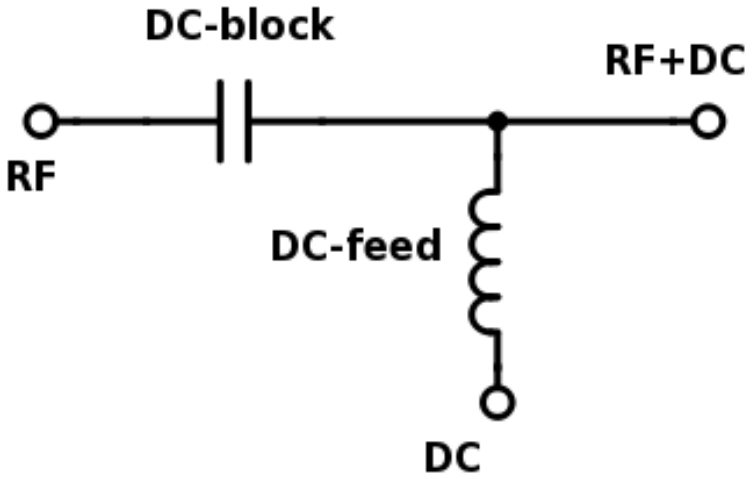



**Figure 3.7:** Schematic of a typical Bias-T

The bias-tee integrated on the CPW line is located before the antenna on the PCB, as seen in Fig. 3.8. There are various ways to implement it, either with lumped discrete components or in a distributed fashion using transmission lines/stubs. Both have been tested and simulated but the most straightforward way at these relatively low frequencies was to use lumped components, such as SMD capacitors and inductors. The DC-block is implemented by a capacitor of 10 pF, which is placed on the signal path (center conductor) and gaps equal to the various capacitor sizes are created so that they can be mounted easily.

After some transmission line length there is a T-junction that splits the line and connects the part of transmission line that carries the DC current, which is a high-impedance line of smaller width (compared to the center 50-Ohm conductor). This T-junction contributes to a desired mismatch between the RF and DC line. The DC-feed is implemented by a 50 nH inductor, mounted across a gap on the DC center line. Fig. 3.8 displays the schematic of the implemented bias-tee and the CST model of the feeding network.

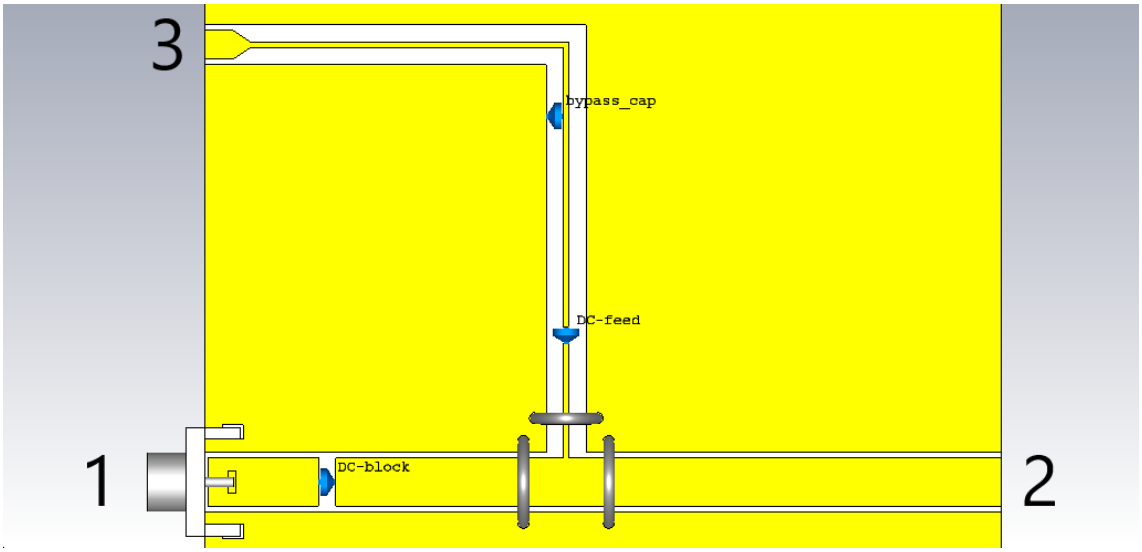



**Figure 3.8:** Designed Bias-T in CST

The part of transmission line that extends from the center conductor and has the DC-feed inductor on it has a length equal to a guided quarter-wavelength $\lambda_g$ where there is one bypass capacitor that is connected to the ground plane and is used to bypass the unwanted frequencies to the ground (low-pass filter). The DC-current is applied to the conductor after bending the line to the PCB edge.

In order to check its performance, the above feeding network is simulated and the 50-Ohm S-parameters are examined, especially $S_{11}$, $S_{21}$, $S_{31}$, $S_{32}$, and $S_{33}$, as shown in Fig. 3.9 and Fig. 3.10.

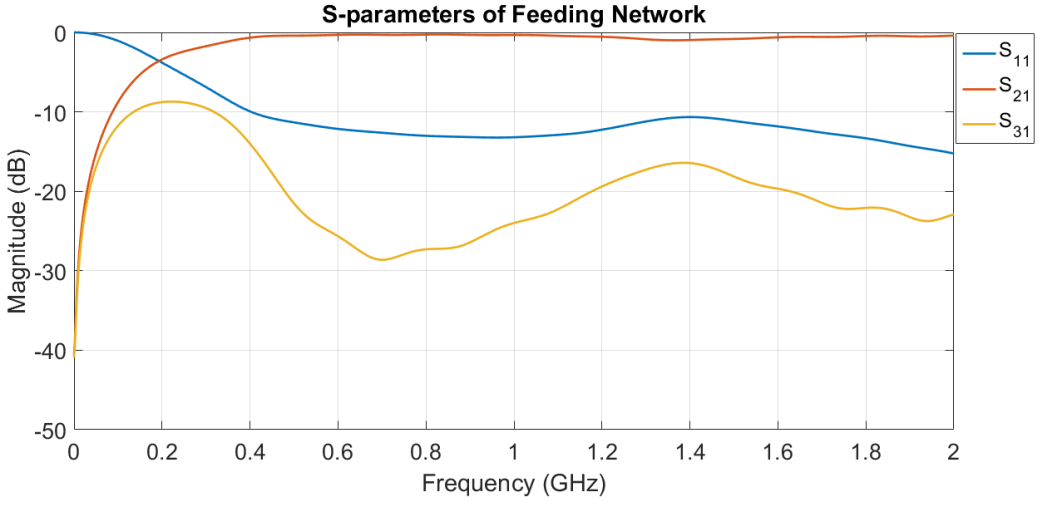



**Figure 3.9:** $S_{11}$, $S_{21}$, $S_{31}$ parameters of the feeding network

The transmission coefficient $S_{21}$ at RF frequencies is close to 0 dB which means that the signals of those frequencies are fully transmitted from port 1 (RF) to port 2 (antenna) and signals at DC are rejected if they are transmitted between those two ports. Similarly, the transmission coefficient $S_{31}$ is below -10 dB in most of the

frequency span, which means that isolation between the ports 1 (RF port) and 3 (DC port) is sufficient.

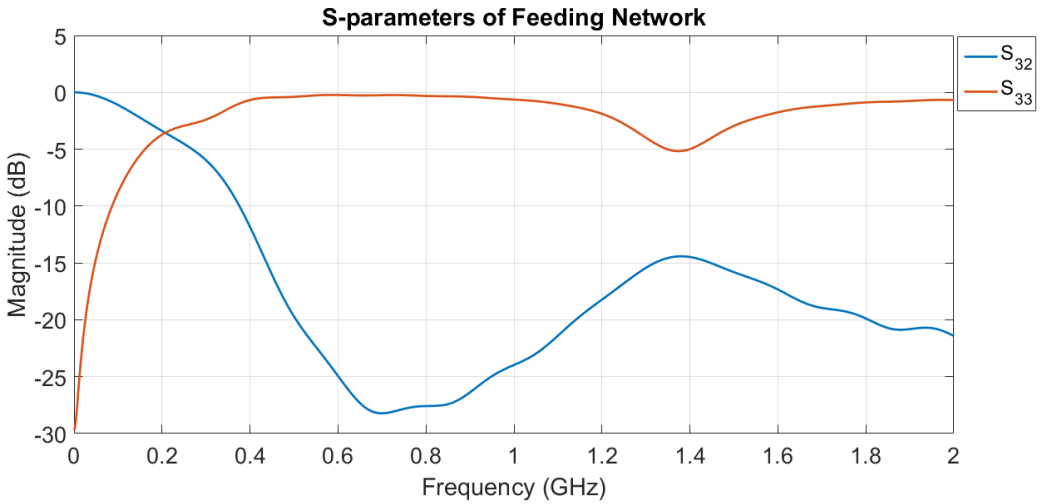
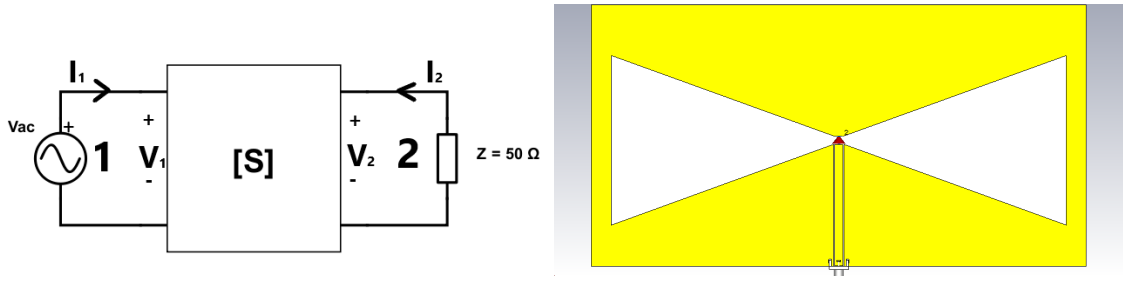



**Figure 3.10:** $S_{32}$, $S_{33}$ parameters of feeding network

## 3.4 Active Antenna model

### 3.4.1 Antenna as a 2-port Network

The active antenna includes the integration of the Tunnel Diode on the same PCB, namely inside the passive antenna. Several steps were followed in this design process. First, a gap where the Tunnel Diode will be placed should be created, therefore a small metal strip from the center conductor is removed. This is shown in Fig. 3.11(b). As there is no model for the TD in CST, the following was done: a 50-Ohm impedance lumped port was assigned to the gap, the antenna was simulated as a 2-port network. The schematic respresentation of the antenna model and the CST model are shown in Fig. 3.11




**(a)** Schematic of the 2-port antenna **(b)** CST model of the 2-port antenna

**Figure 3.11:** 2-port antenna model

The antenna as a 2-port network can be represented by a T-network using the Z-

parameters which are obtained through: $[Z] = Z_0 ([I] + [S])^{-1} ([I] - [S])$ and thus described by the equations (definitions for port voltages and currents as in Fig. 3.11)

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \tag{3.6}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \tag{3.7}$$

Because the passive antenna is reciprocal, $Z_{12}$=$Z_{21}$. The corresponding equivalent circuit model of this network is

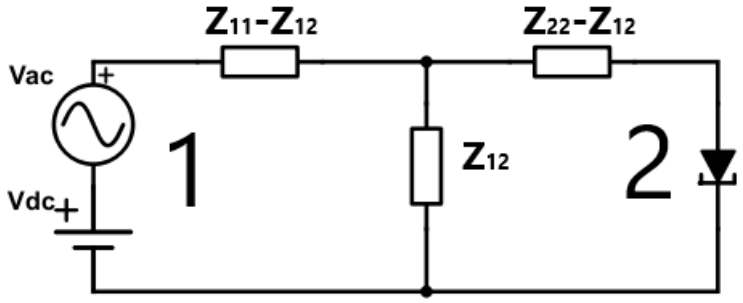



**Figure 3.12:** T-network equivalent of passive antenna

### 3.4.2 Feeding network and 3-port circuit

Besides connecting the diode to the antenna, the next step is to attach the feeding network (RF and DC sources) to it. Then, the circuit becomes a 3-port network, with port 1 being the RF source, port 2 is where the TD is connected and port 3 is the DC source. The feeding network is already integrated on the PCB and is described by the 3-port S-parameters, so there is no need of additional DC-block and DC-feed components.

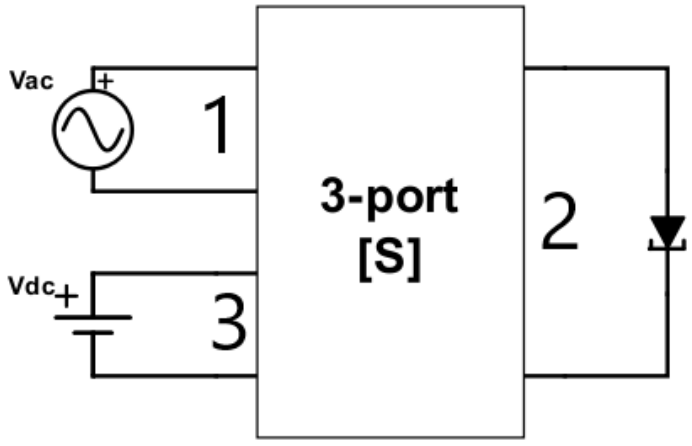



**Figure 3.13:** 3-port network with TD connected at port 2

Two types of simulations were performed. The first type is using the static small-signal linearized model which describes the diode as a negative resistance of -40 Ω. The second type is using the electrodynamic model of the diode and it takes into account the equivalent circuit when the diode is biased properly and includes the intrinsic semiconductor and extrinsic package parasitics. Although the first simulation setup is simpler to understand, the second one is more accurate since it is more complete and realistic. Both simulations will be presented.

### 3.4.3 Simulations using the small-signal linearized electrostatic model

The TD is biased in the negative resistance region and hence it is represented by a single resistance of $-40\Omega$. The schematic of this configuration is shown in Fig. 3.14

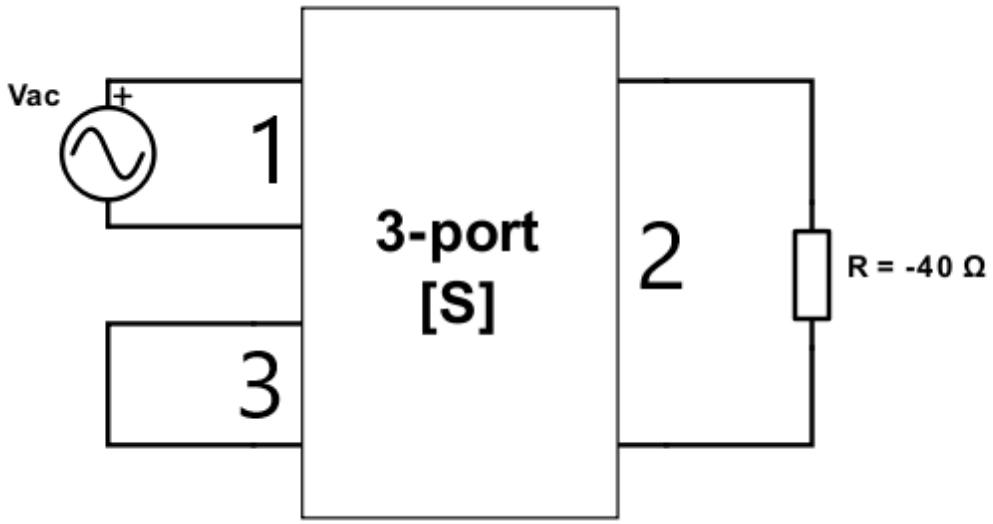



**Figure 3.14:** Tunnel diode described by the small-signal linearized model

Port 1 is terminated with a 50-Ohm RF source, port 2 is terminated with -40 Ω (Tunnel diode) and port 3 is the DC source (assuming a short circuit). Note that the 3-port S-parameters are extracted from the CST simulations when all ports are terminated by 50-Ohm loads and then a 3-port component is created in ADS which imports the CST S-parameters.

Two types of simulations for this part in ADS were performed. First the feeding structure and the 2-port antenna (Sec. 3.4.1) are treated as separated S-parameter objects connected in cascade. The other type is when the feeding network and antenna are integrated together and the whole circuit is a 3-port network modeled in CST. Both configurations are shown as an ADS circuit in Fig. 3.15 and Fig. 3.16. The simulation results are shown in common plots where the legend ADS corresponds to the setup of Fig. 3.15 and the legend CST corresponds to the setup of Fig. 3.16.

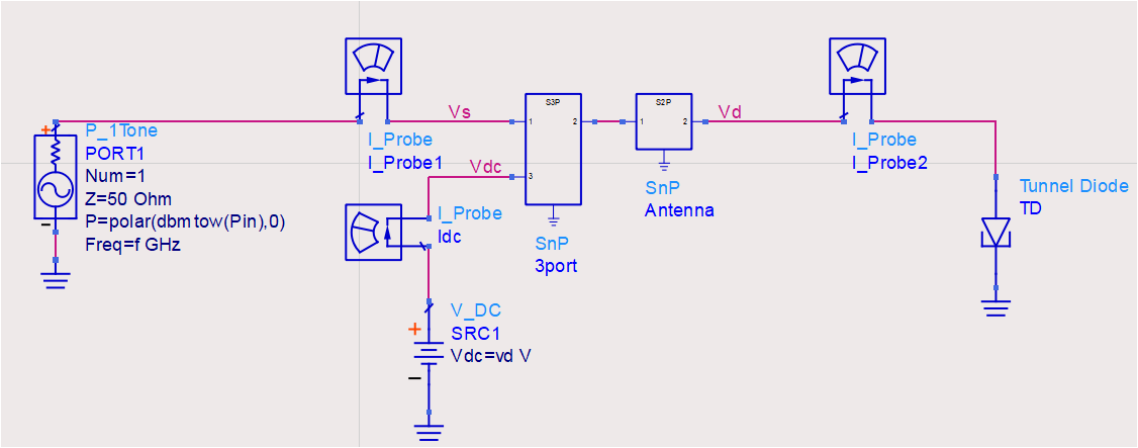



**Figure 3.15:** ADS circuit of separate components

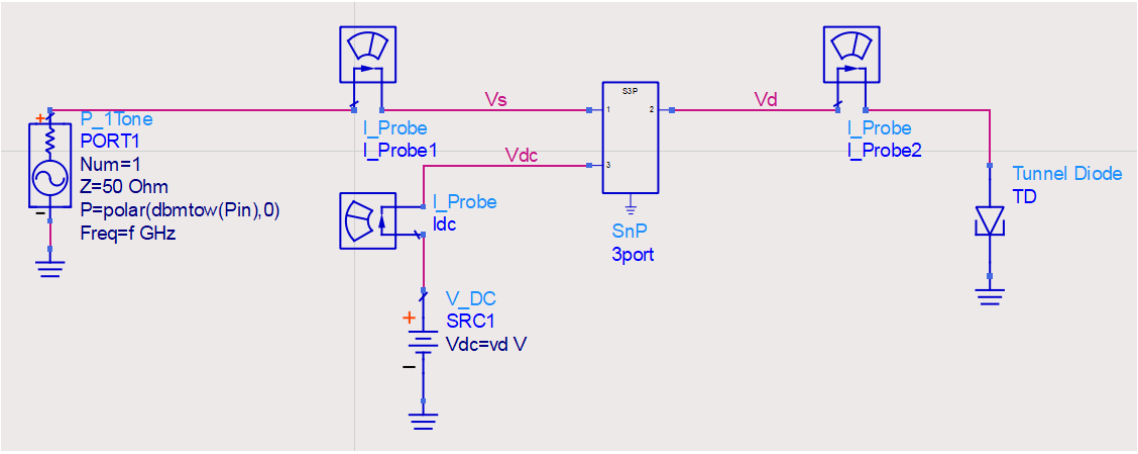



**Figure 3.16:** ADS circuit of 3-port network

Next, Harmonic Balance simulations involving S-parameters are performed and are presented in Fig. 3.18 and Fig. 3.19. In the Harmonic Balance simulations, the Power Gain, the Return Loss and the efficiency of the circuit are the main parameters that are examined and presented here. These parameters are defined as:

**Power Gain** is defined as the ratio between the total radiated power and the power available from the source (at the fundamental frequency)

$$G = \frac{P_{\text{rad}}^{\text{tot}}}{P_{\text{avs}}} \tag{3.8}$$

where

$$P_{\text{rad}} = P_1 + P_2 \tag{3.9}$$

$$P_1 = \frac{1}{2}\,\text{Re}(V_s I_1^*) \tag{3.10}$$

$$P_2 = -\frac{1}{2}\,\mathrm{Re}(V_\mathrm{d} I_2^*) \tag{3.11}$$

**Return Loss** is defined as the ratio between the power that is incident to port 1 of the 3-port antenna network and the reflected power which returns to the source

$$\mathrm{RL} = \frac{P_\mathrm{inc}}{P_\mathrm{refl}} \tag{3.12}$$

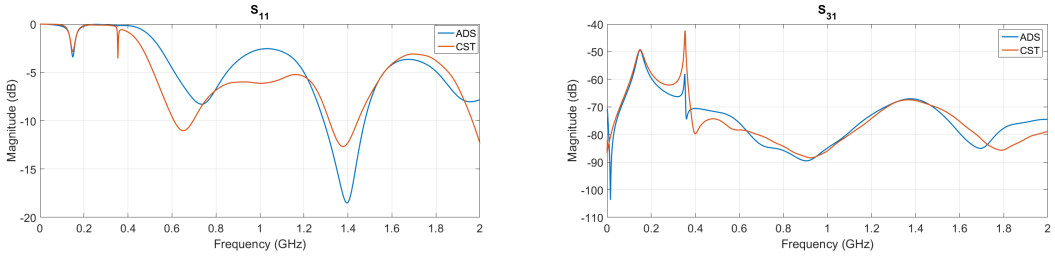
**Efficiency** is defined as the ratio between the total radiated power (at the fundamental frequency) and the sum of the power available from the source (also at the fundamental frequency) and the dc power

$$\mathrm{eff} = \frac{P_\mathrm{rad}^\mathrm{tot}}{P_\mathrm{avs} + P_\mathrm{dc}} \tag{3.13}$$

where

$$P_\mathrm{dc} = V_\mathrm{dc} I_\mathrm{dc} \tag{3.14}$$

First, the S-parameters are shown and the two cases, i.e. Fig. 3.15 (legend ADS) and Fig. 3.16 (legend (CST)), are compared by plotting them in the same figure (3.17).




**(a)** $S_{11}$ of active antenna **(b)** $S_{31}$ of active antenna

**Figure 3.17:** S-parameters of the 3-port active antenna

From those figures it is clear that the two types of simulations are quite close and the minor differences that occur are probably caused by the differences between the ideal cascade connection in the ADS model and the other one which includes the over-the-air coupling which has been accounted for in the EM-simulation.

The next set of figures are results from the Harmonic Balance ADS simulations.

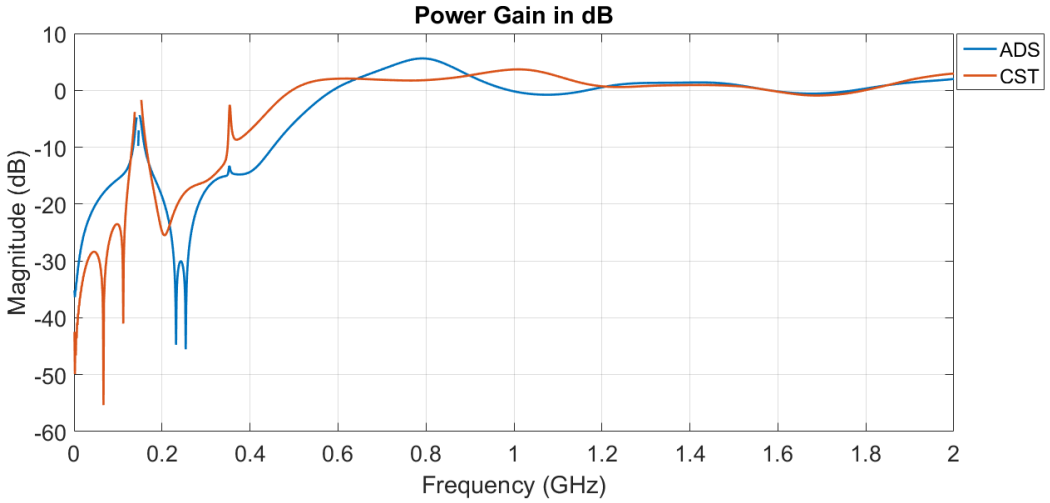
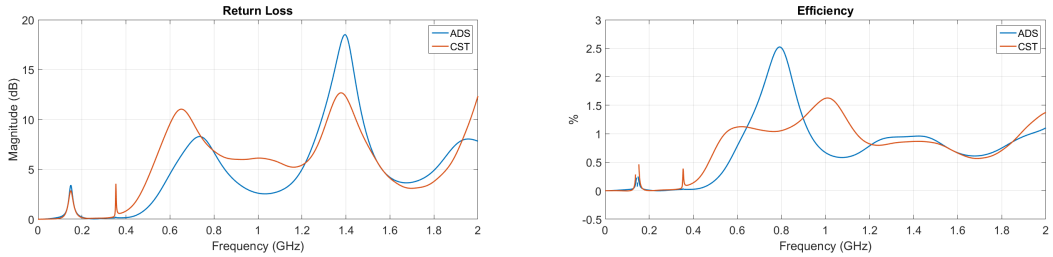



**Figure 3.18:** Power Gain of the Active Antenna (for electrostatic diode model)




**(a)** **(b)**

**Figure 3.19:** (a) Return Loss, and ;(b) Efficiency

Fig. 3.18 shows that when the diode is described by the electrostatic nonlinear model, it is possible for the circuit to have power gain, i.e. the tunnel diode acts as an amplifier and generates power and delivers it back to the antenna so it can be radiated. Fig. 3.19(a) shows the Return Loss of the circuit, which according to the definition should be positive and it is, as shown in this plot. Last, Fig. 3.19(b) shows that the efficiency of the whole circuit is rather low which is expected because the RF power is much lower than the DC power needed for the biasing of the diode. This is a disadvantage of the designed structure, because one the one hand the diode can handle low amplitude RF signals but on the other hand it requires more DC power in order to operate properly (but still this DC power is rather low). Although the results are promising, the electrostatic nonlinear model is not frequency dependent and therefore the electrodynamic linearized model is needed for a more realistic circuit representation at RF and for small signals.

### 3.4.4 Simulations using the small-signal electrodynamic linearized model

The only difference between the concept presented in the previous subsection and here is that port 2 is now terminated by the equivalent circuit of Sec. 2.2.2 (Fig. 2.6. The ADS circuit is shown in Fig. 3.20.

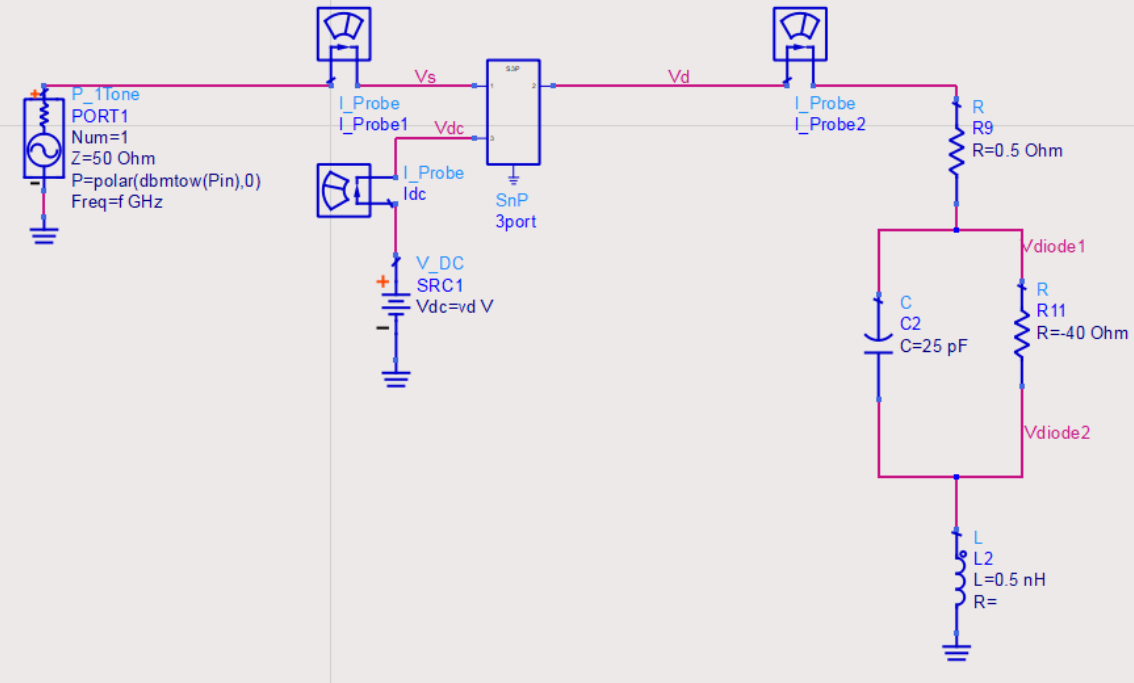
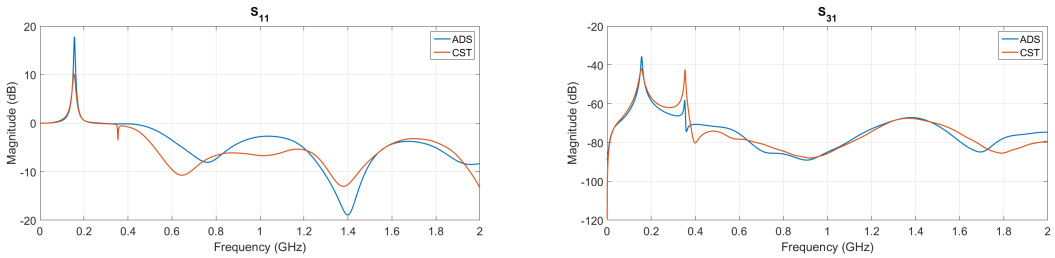



**Figure 3.20:** ADS circuit of the 3-port antenna network with NDR diode model

The same type of simulations as in the previous section were performed and the results are presented in Fig. 3.21 for comparison.




**(a)** $S_{11}$ of active antenna **(b)** $S_{31}$ of active antenna

**Figure 3.21:** S-parameters of active antenna using the equivalent linearized circuit model of the TD

Upon comparing the above figures with Fig. 3.17 it is obvious that they are quite similar except for the high peak at around 150 MHz. This relatively large reflected power is not something desirable and it needs to be minimized (or even eliminated).

The $S_{31}$ plot shows that RF and DC ports are well isolated. The ADS Harmonic Balance simulation results are shown in Fig. 3.22 and Fig. 3.23.

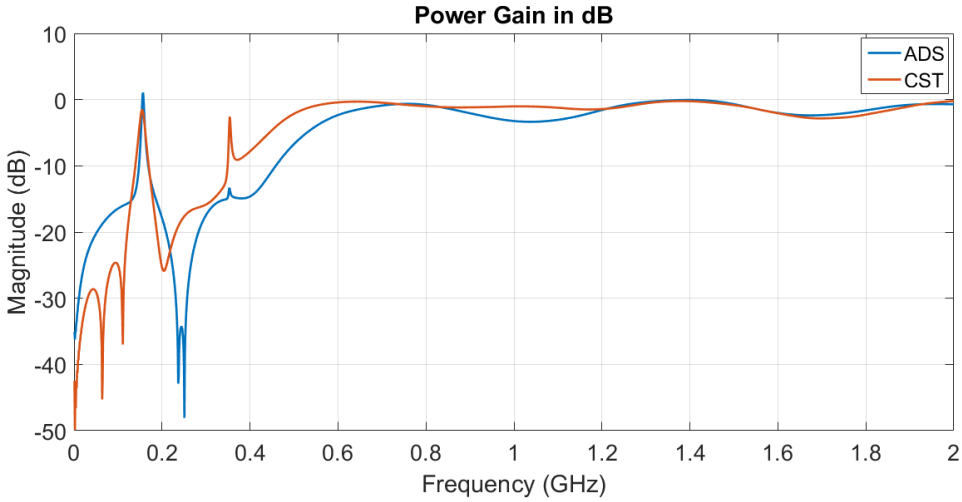
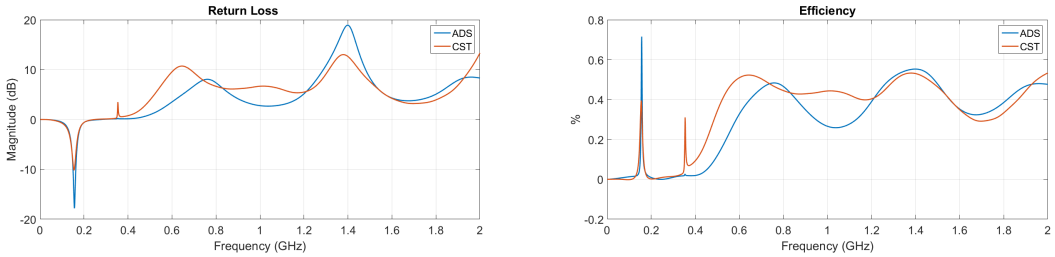



**Figure 3.22:** Power Gain of Active Antenna (for the electrodynamic diode model)




**(a)** **(b)**

**Figure 3.23:** (a) Return Loss; (b) Efficiency

In this case there is no power gain, as it is everywhere below 0 dB, expect for a peak at 150 MHz which is slightly above 0 dB but it is caused by leakage. The return loss shows a similar behavior as in Fig. 3.19, while the efficiency has reduced further (less than 1%). This performance degradation is caused by the external (package) parasitics of the diode.

To improve performance, the antenna was modified to operate at lower frequencies where pakage parasitics are less pronounced, as explained in the following section.

## 3.5 Modified Active Antenna prototype and Simulation results

To improve the performance, a modified active antenna prototype is designed and will be presented next. The model of the tunnel diode was kept the same, i.e., the

linearized electrodynamic model was used, since the electrostatic nonlinear model is inaccurate at 1 GHz. The solution is to move towards lower frequencies where the models are more accurate. First, the passive antenna is presented, then the active 3-port network model is used and the above-described simulations are repeated.

### 3.5.1 Passive antenna

The proposed modification to make the antenna work at lower frequencies is to enlarge the antenna by attaching a closed metallic wire to each side of the PCB so as to realize a continuous closed loop extended from the bow-tie design (Fig. 3.24). The total length of the loop edge-to-edge is $L_{\text{loop}}$=1 m.

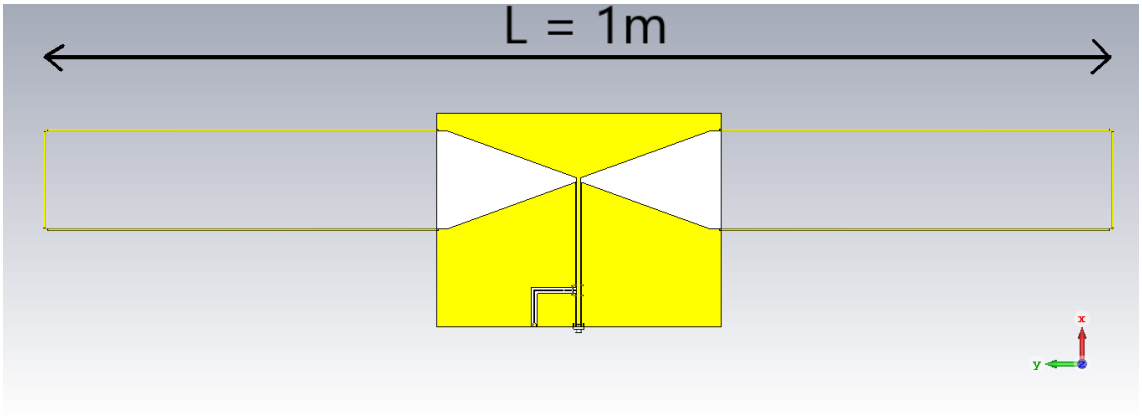



**Figure 3.24:** Modified Antenna model in CST

The reflection coefficient of this antenna, the 3D radiation pattern, antenna (realized) gain, and both the E- and H-plane cuts are given in Fig. 3.25 – 3.28.

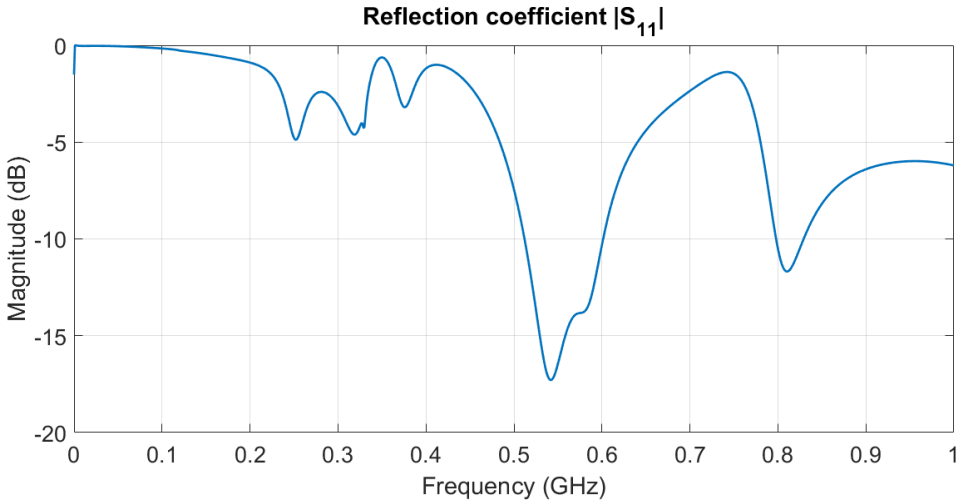



**Figure 3.25:** Reflection Coefficient $|S_{11}|$ in dB

Fig. 3.25 shows the reflection coefficient of the passive antenna with the operation

point with good 50-Ohm match at 540 MHz.

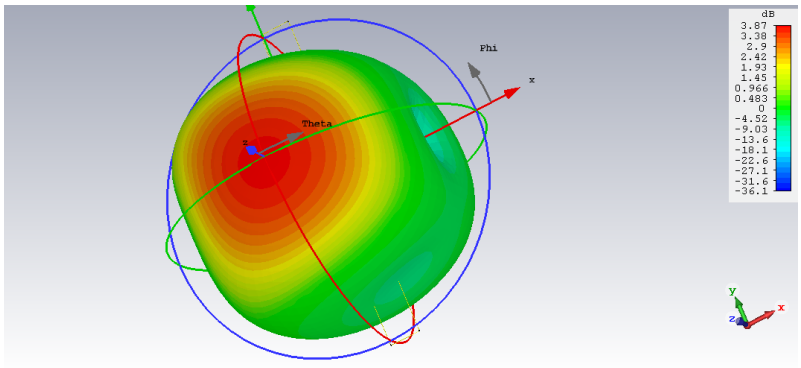



**Figure 3.26:** 3D antenna realized gain pattern

The antenna radiates in the same direction as the previous one but has slightly larger $\theta_{3\text{dB}}$.

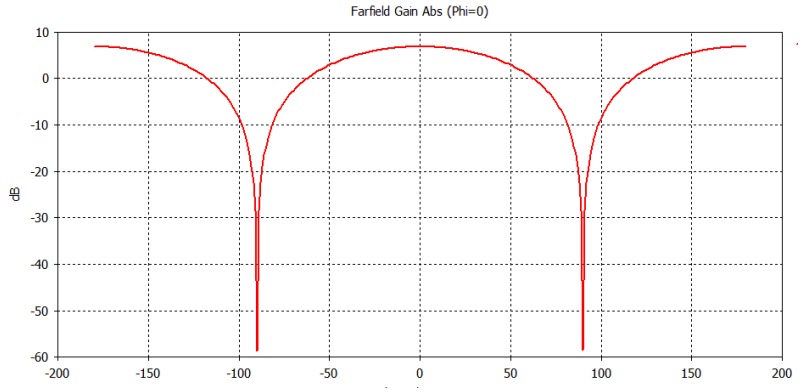
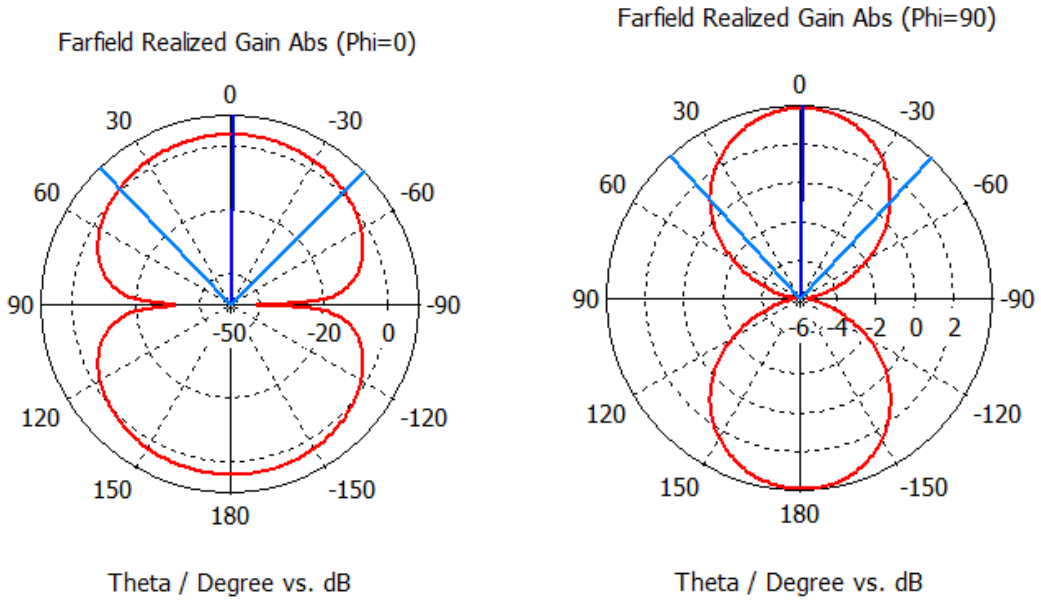



**Figure 3.27:** Cartesian plot of E-plane far-field realized gain pattern

### 3.5.2 Active Antenna model

The complete PCB antenna includes the feeding network that was presented in Sec. 3.3 and the passive antenna of Sec. 3.5.1 and the same set of simulations as before were performed. In this case, the simulations with the electrostatic nonlinear model are disregarded and the results using the linearized electrodynamic model are displayed. In addition, simulations where the power available from the source $P_{\text{avs}}$ was varied are also shown.




**(a)** E-Plane **(b)** H-Plane

**Figure 3.28:** (a) E-plane pattern; (b) H-plane pattern

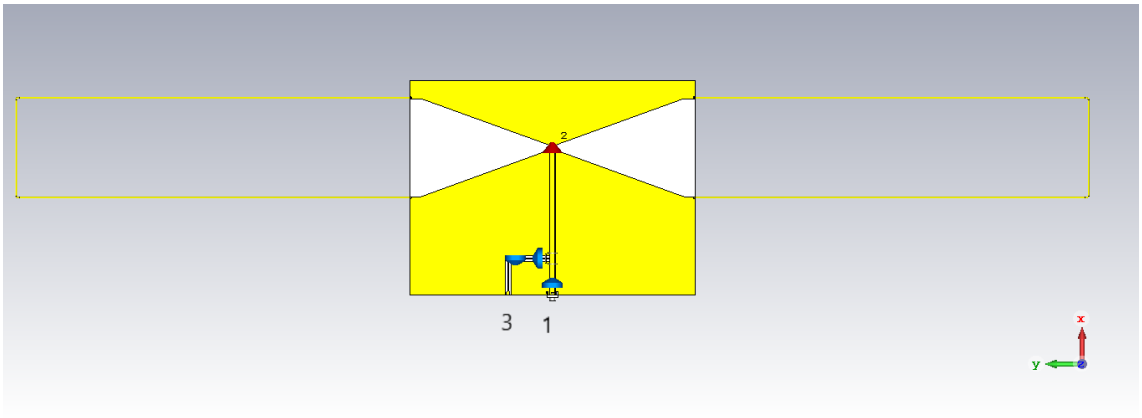
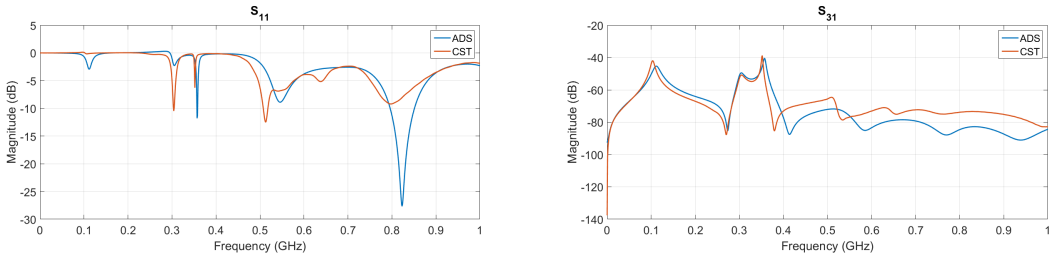



**Figure 3.29:** Active PCB Antenna

The S-parameters of this active antenna are shown in Fig. 3.30.




**(a)** **(b)**

**Figure 3.30:** S-parameters of active antenna using the small-signal equivalent circuit of the TD. (a)$S_{11}$; (b)$S_{31}$

Observing the two figures, they are quite similar and in the CST model (Fig. 3.30(a)) a dip at 300 MHz appears. Fig. 3.30(b) shows that the RF and DC ports are well isolated.

The ADS Harmonic Balance simulations (using the nonlinear diode model) are shown next, to examine the power gain, return loss and efficiency of the circuit. In addition to these plots, an extra set of simulations was performed for the above measurements but with respect to the power available from the source $P_{\text{avs}}$. These help when one needs to decide about the RF power level that should be provided to the circuit.

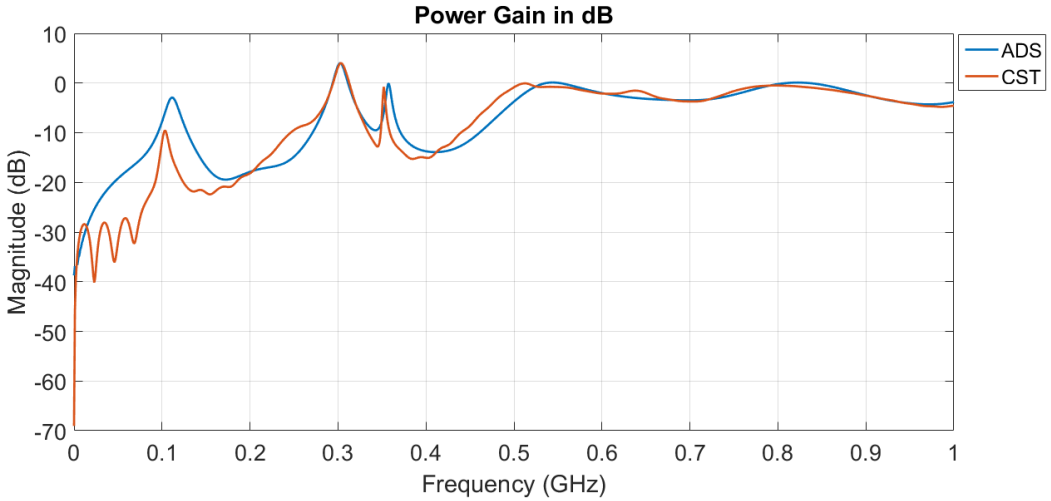
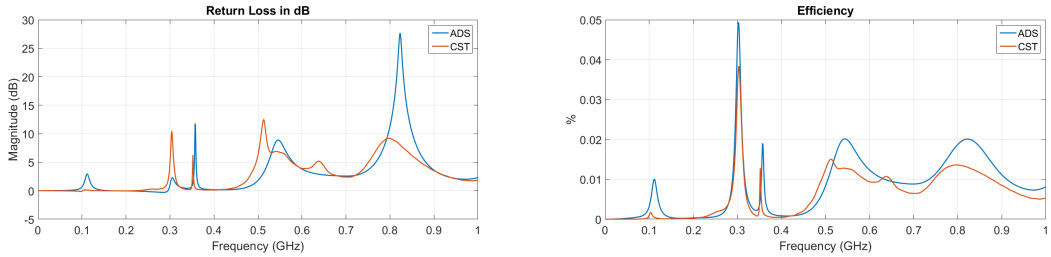


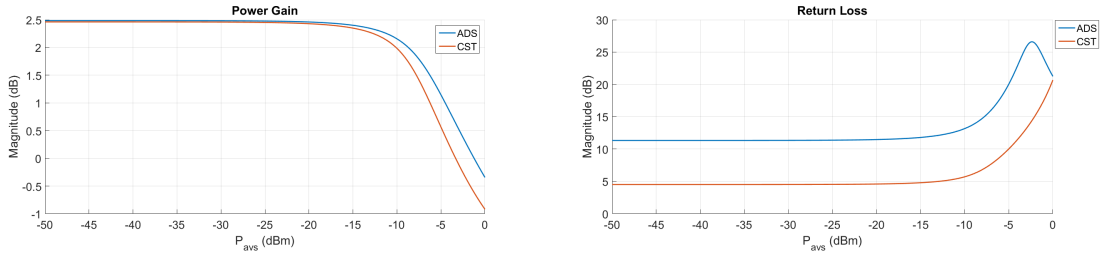

**Figure 3.31:** Power Gain of the Active Antenna




**(a)** **(b)**

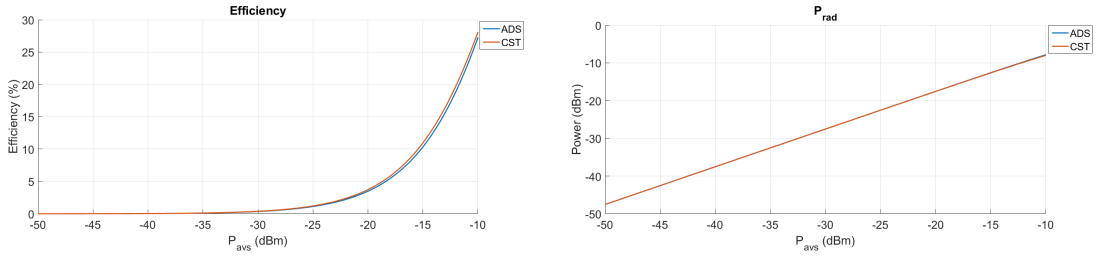
**Figure 3.32:** (a) Return Loss, and; (b) Efficiency

Fig. 3.31 shows that at f=300 MHz the circuit provides 4 dB of power gain which is not high but for a proof-of-concept prototype design in such an early stage is promising enough. The Return Loss (Fig. 3.32(a)) is positive in the whole frequency span which is a desirable and expected behavior. The efficiency (Fig. 3.32(b)) is quite low and that is because the level of the RF power that this device handles in the above simulations is much lower than the DC power level needed for biasing the TD.




**(a)** Power Gain **(b)** RL

**Figure 3.33:** (a) Power Gain, and;(b) Return Loss vs $P_{\text{avs}}$




**(a)** **(b)**

**Figure 3.34:** (a) Efficiency, and; (b) Radiated Power vs $P_{\text{avs}}$

Fig. 3.33 shows that both the Power Gain and Return Loss are stable until $P_{\text{avs}}$ is increased to -15 dBm after which the power gain starts to drop which means that the performance of the system is degrading (it reached saturation). This can also be seen in Fig. 3.34(b) where beyond -15 dBm the radiating power seems to follow

a less linear slope. Last, from Fig. 3.34(a) it can be concluded that the efficiency is getting higher beyond -25 dBm which is because the amount of RF power that the source provides is larger than the amount of DC power needed to bias the TD. Although the above plot shows that higher RF power means higher efficiency, or lower return loss, the TD cannot support higher amplitude RF signals at its input, so there is a limitation in the RF power level (as mentioned before: -15 dBm).

# 4

# Measurement Results

This chapter describes the measurements that have been conducted and also includes the comparisons between simulations and measurements.

## 4.1 Tunnel Diode Measurements

First, the DC characteristics of the Tunnel Diode were measured, i.e. the I-V curve is extracted by measuring the current through the diode. The measurement setup consists of a DC power source, a multimeter connected in series to measure the current, the Tunnel Diode connected directly to an SMA connector, a multimeter connected in parallel to the Tunnel Diode to measure the voltage across it and a bias-T, see Fig. 4.1. The voltage across the diode ($V_\mathrm{d}$), is controlled by the DC voltage source and the current through the diode ($I_\mathrm{d}$) is measured. The bias-T is used to provide a 50-Ohm termination at the RF port and for the diode to see an impedance that is well-defined over a large frequency range (resistive load) than when connected directly to a DC source (short-circuit). Fig. 4.1 shows the bias-T port connections.

After performing the above measurements, the DC I-V curve is extracted and overlayed with the theoretical one that was presented in Chapter 2. Fig. 4.2 shows the agreement between these two curves.

It is seen that the measured I-V curve is in reasonable agreement with the theoretical one, with some differences in the negative resistance region (NRR). There is a region where the slope is getting less steep (from 180 mV to 320 mV) and this is likely caused by the self-oscillating tunnel diode (DC power converted into RF power, thereby affecting the DC I-V characteristics).

The oscillations of the tunnel diode were also observed when the RF port of the bias-T was afterwards connected to an oscilloscope (with 50-Ohm termination) and when biased in the NR region. This setup is used to check if there are signals present in the frequency spectrum when the diode is only DC-biased while no RF signal is applied to it. Furthermore, it is a way to check the stability of the diode. If there is a signal (or signals) in the spectrum this means that the diode is likely to start oscillating. Fig. 4.3 shows the measurement setup and the oscillation observed on the oscilloscope display.

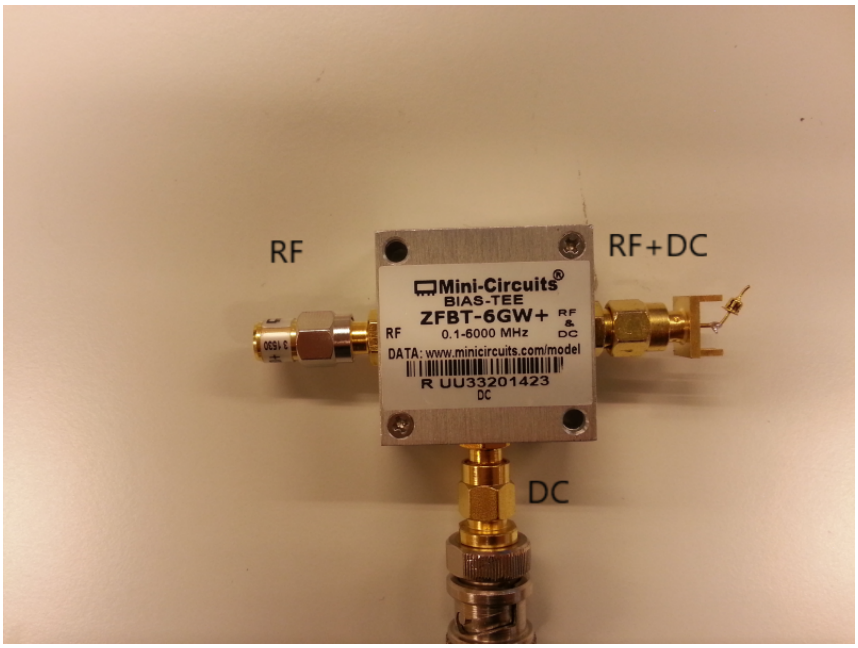



**Figure 4.1:** Diode connected to Bias-T

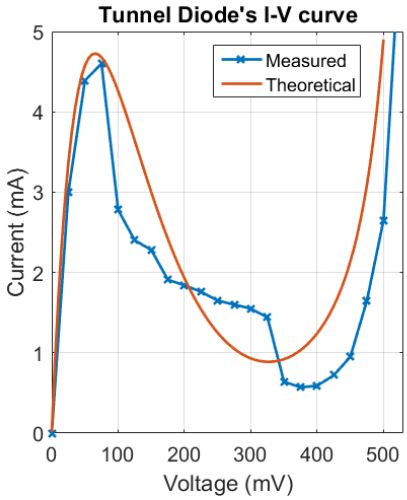
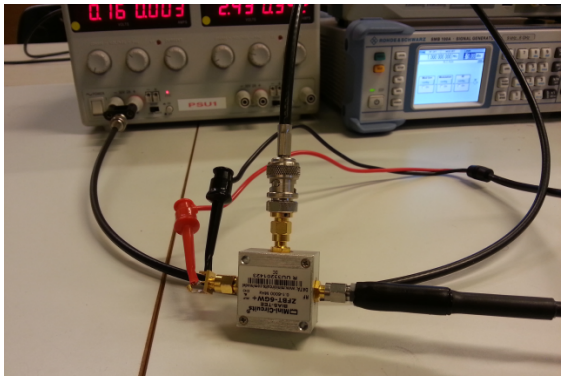
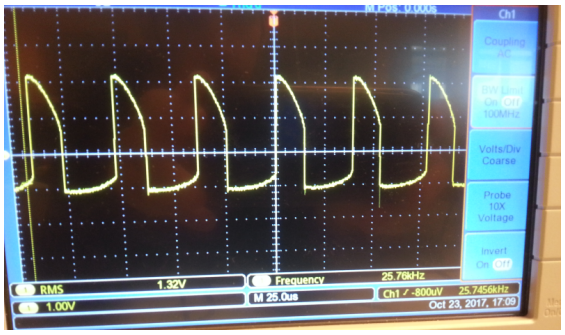



**Figure 4.2:** I-V curve of the tunnel diode, DC characteristics



**(a)**




**(b)**

**Figure 4.3:** (a) Diode connected to an oscilloscope; (b) Oscillation signal

From Fig. 4.3(b) it is evident that there is an oscillating signal and the frequency of that signal is 25.7 kHz, which is a very low frequency but it still can affect the performance of the diode as it consumes DC power and affects the I-V characteristics as shown in Fig. 4.2. Despite the oscillations, the question is whether these oscillations are also observed when the diode is placed on the antenna since it represents a different loading environment, which is what is examined next.

## 4.2 PCB Antenna with integrated feeding network

### 4.2.1 Passive Antenna

The PCB antenna that was fabricated is the one presented in Sec. 3.5. The material of this PCB is FR4 with relative permittivity $\epsilon_r = 4.3$, loss tangent tan$\delta$=0.025 and substrate thickness $h = 1.6$ mm. The material of the metallic wire that was used for the loop is copper and is soldered on the edges of the PCB as shown in the simulations section. One SMD capacitor and one SMD inductor were used for the feeding network as DC block and DC feed, respectively. Also, a capacitor was used (in parallel to the DC line) as a DC decoupling element. The diode port is short-circuited in the passive case that is discussed first. The measurements made and shown in this section are for the S-parameters of the PCB antenna circuit, specifically $S_{11}$, which is the reflection coefficient of the antenna at its RF port. The instrument used for measuring the reflection coefficient ($S_{11}$) is a Vector Network Analyzer (VNA) with 50-Ohm source impedance.

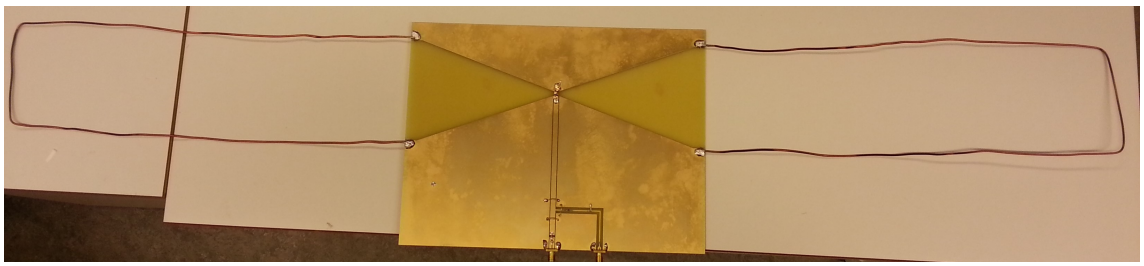


**Figure 4.4:** The manufactured passive antenna

The $S_{11}$ derived from the CST simulations and the measurement result are shown in Fig. 4.5 for comparison. It can be seen from this figure the antenna behaves as expected from the simulations since the two curves are in a reasonable enough agreement.

Measuring both the $S_{11}$ and the far-field characteristics of this antenna would require an anechoic chamber that is suitable for low frequency measurements. The available chamber at Chalmers would not give accurate enough measurement results for the far-field patterns. Hence, the results are not presented in this section but solely for the $S_{11}$ measurements which are affected due to reflections as well, but in a minor

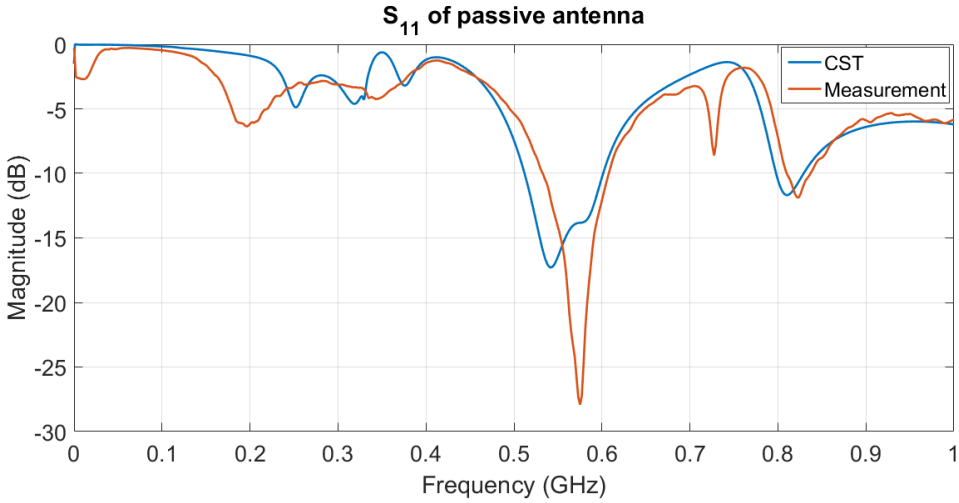



**Figure 4.5:** The $S_{11}$ of the passive antenna

way. The next step for the measurements is to examine the active case, where the tunnel diode is soldered onto the PCB. Fig. 4.6 and Fig. 4.7 show the SMD components and the diode soldered onto the circuit board.

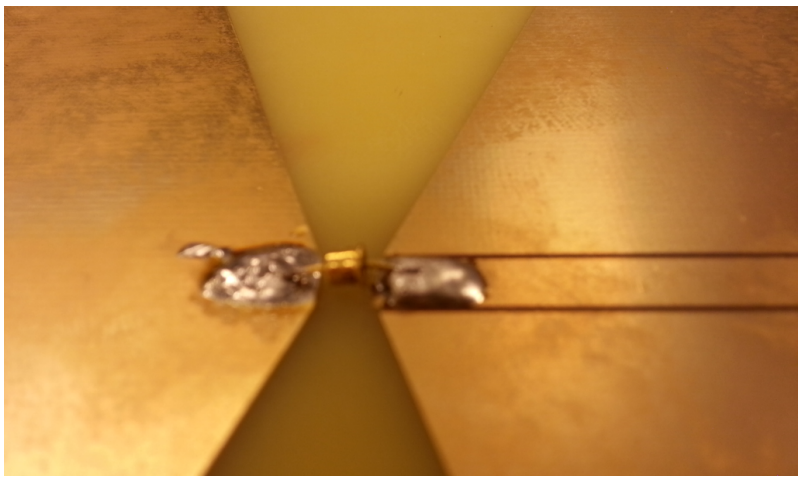


**Figure 4.6:** Diode on the PCB across the bow-tie antenna gap

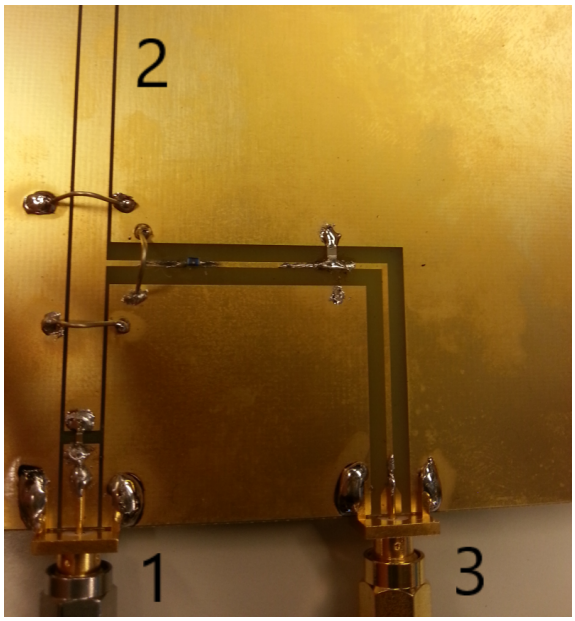



**Figure 4.7:** Feeding Network with SMD components and CPW air bridges

### 4.2.2 Active Antenna

Before measuring the $S_{11}$ of the active antenna, a check on the presence of oscillation needs to be done. Therefore, the RF port of the antenna circuit is connected to a spectrum analyzer. The DC power supply is connected to port 3 of the circuit and the diode is biased at the desired operating point. If there are no signals present in the spectrum (assuming no external RF sources), then the structure is stable. The setup for the above measurement and the results on the screen of the spectrum analyzer are shown in the next figures. It is pointed out that the measurement was also performed in an anechoic chamber with similar results.

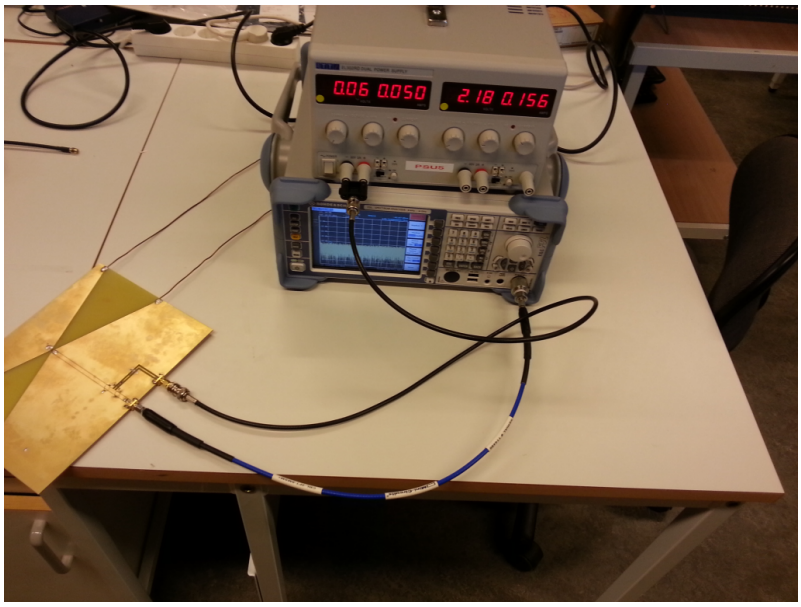


**Figure 4.8:** Measurement setup of the active antenna for detecting oscillations (actual measurement was carried out in an anechoic chamber)

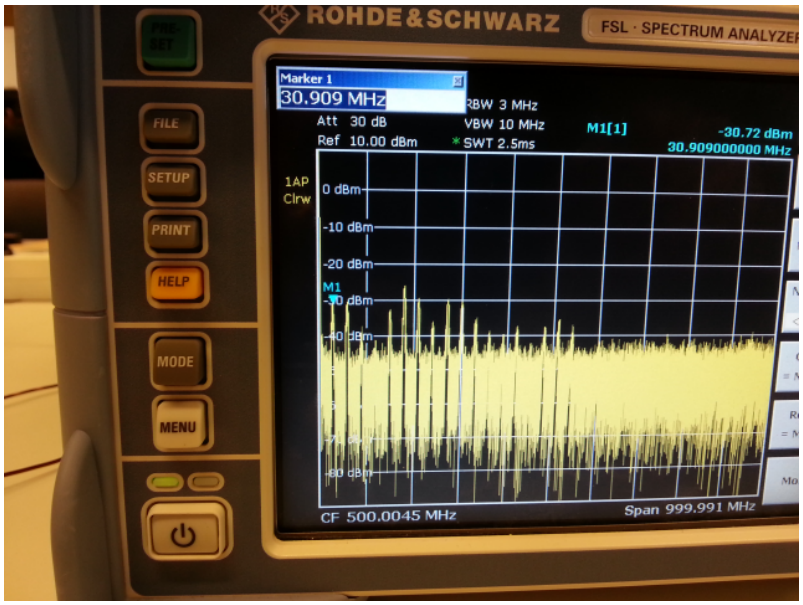



**Figure 4.9:** Spectrum analyzer showing the spectral components due to self-oscillations

It is clear from the spectrum in Fig. 4.9 that the diode is oscillating and produces harmonics corresponding to unwanted oscillatory signals. This means that the circuit is unstable and the oscillations need to be eliminated.

## 4.3 PCB debugging

To eliminate the oscillations that were observed in the previous section, different solutions were tried. The first one was to change the values of the SMD components, especially the DC-decoupling capacitor. Different values from 10 pF to 2.2 $\mu$F were tried, however, the only thing noticed was a shift of the oscillation frequency. This method gave no improvement and another solution was considered.

Another idea that was tried was to unsolder the SMD components and to use an external feeding network instead. The feeding network was the bias-T that was used to bias the tunnel diode in Sec. 4.1. This setup is shown in Fig. 4.10

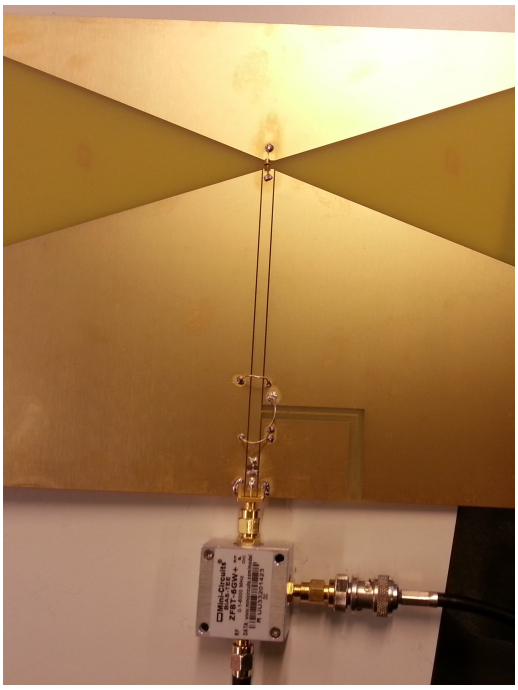


**Figure 4.10:** External feeding network using an external bias-T

Unfortunately, upon connecting the RF port of this structure to the spectrum analyzer revealed that the oscillations are still present and the conclusion is that the instability of the circuit has not been eliminated before the end of this project, due to limited time constraints. Therefore, other methods need to be found to stabilize the circuit in the future.

The most important conclusions from these observations are that the antennafier is a concept that works in theory, but that one has to carefully design a stable environment for it to work also in practice, in case tunnel diodes are used.

Although the simulations indicate that it is possible to achieve 2.5 dB power gain, the project has unfortunately not led to a working prototype. Nonetheless, the first co-simulation steps toward a deeply integrated antennafier have been taken that already provided many insightful results. More detailed conclusions and future recommendations are provided in Chapter 5.

# 5

# Conclusions and Recommendations

## 5.1 Conclusion

In this project, a prototype PCB active antenna was designed and fabricated as a first step towards Deep Integration; a nonlinear device that can act as an amplifier has been integrated along with a typical passive antenna. The components chosen for this purpose were a bow-tie antenna and a tunnel diode, the latter of which has a negative resistance region in its I-V curve that makes it possible to amplify the signal applied to it. The design process included the modelling of the tunnel diode in MATLAB and ADS, followed by the modelling and simulation of the passive antenna in CST and lastly the combination of both components. The final electromagnetic model was described by a 3-port network and was subsequently imported and simulated in ADS.

It was shown that additional power can be radiated by using a tunnel diode, which is caused by its ability to function as a negative resistance and deliver RF power like a dependent generator source back into the antenna. Since this returned power is mostly radiated by the antenna power gain becomes possible. The expected theoretical power gain for a single tunnel diode was shown to be 2.5 dB. Also, the return loss is shown to be satisfactory at the frequency of interest, which is desired. The active integrated antenna does not seem to be very efficient as a class-A amplifier but this is quite reasonable as the DC power needed for its biasing is much larger than the RF power. In fact, the DC supplied power is as large as 0.45 mW, while the RF available input power is only in the order of 1 $\mu$W (power gain is 2.5 dB).

## 5.2 Recommendations and future work

The used tunnel diode presents negative resistance at low frequencies. High-frequency antennafiers can be realized in future by choosing different nonlinear components with smaller parasitics that will amplify the signals at higher frequencies more efficiently.

The stability of the entire circuit could not be realized due to limited time constraints. Another aspect that could be examined is the possibility of adding more

nonlinear devices connected in series (or other kind of connections) along the antenna conductor and examine whether the gain and output power performance of the overall system is improved by distributing nonlinear semiconductor (negative) material along the metal of the antenna.

Finally, the use of a transistor may reduce the oscillatory behavior of the antennafier due to a better intrinsic isolation between output (e.g. drain) and input (e.g. gate) of such devices, as opposed to the one-port tunnel diode. A transistor will provide also higher gain. Fig. 5.1 shows a passive linear material distribution which embeds localized FETs instead. There is no local ground, FETs are characterized as 3-terminal nonlinear electrodynamic devices. Both DC (biasing) and RF (+harmonic) currents flow throughout the multifunctional medium.

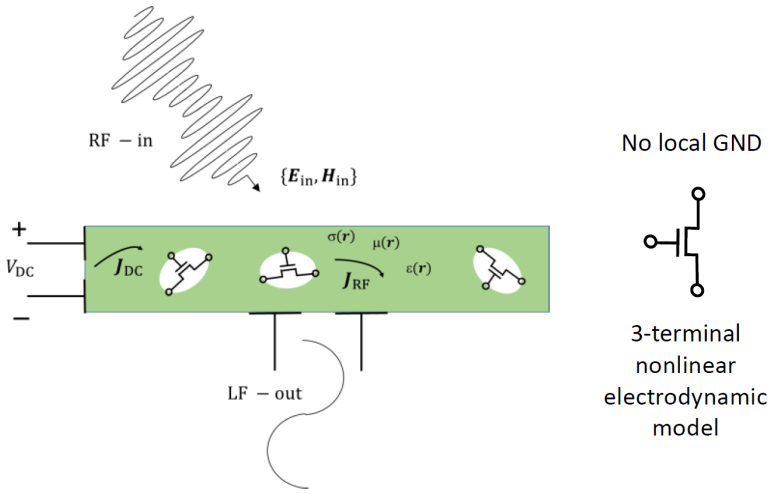



**Figure 5.1:** Deep Integration – a new material synthesis concept employing FETs as opposed to diodes.

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# A

# Appendix-Thesis defence presentation

CHALMERS

## A Deeply Integrated Active Antenna

PCB Bow-tie antenna integrated with a Tunnel Diode

MASTER THESIS PROJECT - 2017

NIKOLAOS KOLLATOS



CHALMERS

## CONTENTS

- Motivation
- Tunnel Diode
- Antennafier and Simulation Results
- Measurement results
- Conclusion and Suggested Future work



CHALMERS

## Motivation

- Deep Integration concept
- Proof of concept thesis project
- Antennafier concept (antenna+amplifier)
- PCB bow-tie antenna integrated with a Tunnel Diode
- EM-simulations for Antenna and ADS simulations for electronics

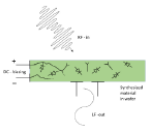


Image taken from "Rob Maaskant, Research Proposal on Deep Integration"



CHALMERS

## Tunnel diode

- Non-linear highly-doped semiconductor device
- Negative Differential Resistance (NDR)
  - $R_{diff} = \frac{dV}{dI}$
- Use in many applications as an oscillator, amplifier, switching circuits
- Diodes, fundamental building blocks in electronics
- Diode symbol


Image taken from Wikipedia

## Tunnel diode

- Advantages
  - Ease of integration on PCB circuits
  - High durability
  - Low power dissipation
- Disadvantages
  - Low voltage swing at the output
  - No isolation between input and output



## Tunnel diode (IV-characteristics)

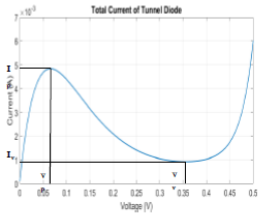
- Superposition of three current components
  - Tunneling current
  - Excess current
  - Normal diode current
- Total current of the diode

$$I = \frac{I_p}{V_p}\left(1 - \frac{V}{V_p}\right)V + I_v e^{(A_2(V-V_v))} + I_s e^{\left(\frac{qV}{nkT}-1\right)}$$



## Tunnel diode (IV-characteristics)

- Peak current ($I_p$)
- Negative Resistance Region (NRR)
- Valley current ($I_v$)
- Electrostatic non-linear model, not frequency dependent

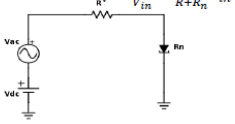


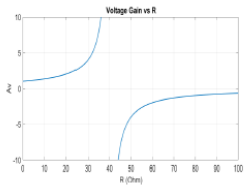



## An amplifier circuit

- Simple amplifier circuit
- Voltage gain

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R}{R+R_n}V_{in}$$



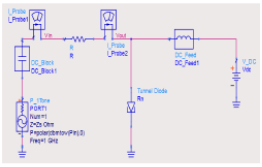



## An amplifier circuit (ADS circuit)

- Power Gain

$$G = \frac{P_1 - P_2}{P_{avs}}$$

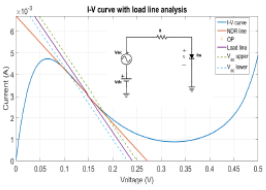
- $P_1 = \frac{1}{2}Re\{V_{in}I_1^*\}$
- $P_2 = \frac{1}{2}Re\{V_{out}I_2^*\}$
- $P_{avs}$ the available power from the source





## Load line example

- Example: R=30 Ohm
- $V = V_{oc} - IR$
- $V_{oc}$ where load line meets x-axis
- $I_{sc} = \frac{V_{oc}}{R}$ where load line meets y-axis
- Parallel lines show RF voltage swing
- Voltage gain 3.9





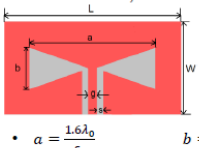

## Antennafier and Simulation results

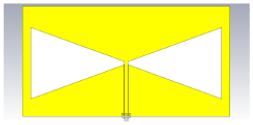
- Antennafier (antenna + amplifier)
- Combines the functions of an antenna and an amplifier
- In principal, it keeps the attributes of the passive antenna
- Active device when integrated with the amplifier
- PCB antenna on CPW



## Passive Antenna

- CPW structure, slot bow-tie antenna



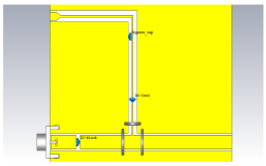
- $a = \frac{1.6\lambda_0}{\varepsilon_r}$ $b = \frac{0.5\lambda_0}{\varepsilon_r}$ $L = \frac{a}{0.92}$

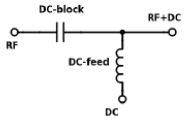
$$W = \frac{b}{0.55}$$

Design equations taken from "Khalid Hamed Alharbi, Afesomeh Ofiare, Jue Wang, Monageng Kgwadi, Ata Khalid, and Edward Wasige, Broadband Slotted Bow-tie Antennas for Terahertz Resonant Tunneling Diode Based Oscillators, Progress In Electromagnetics Research Symposium Proceedings"

## Feeding Structure on PCB

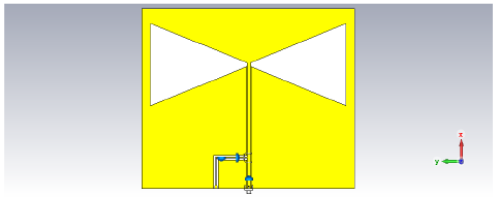
- Need of feeding structure to supply the DC bias, lumped components







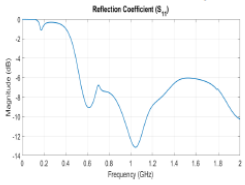

## PCB Passive antenna with bias-T

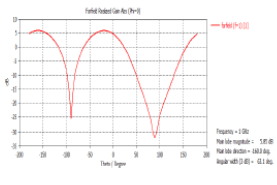




## PCB Passive antenna with bias-T

- Reflection Coefficient, Realized Gain

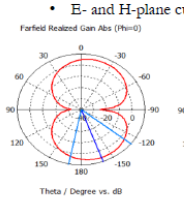


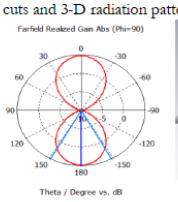



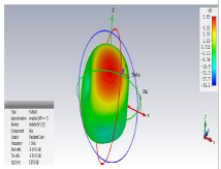



## PCB Passive antenna with bias-T

- E- and H-plane cuts and 3-D radiation pattern



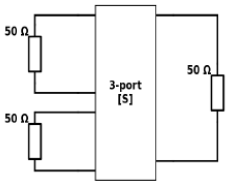


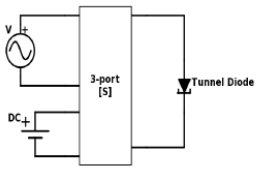
## Active Antenna (3-port model)

- Design approach
  - Diode integrated with antenna
  - EM simulations for a 3-port antenna model
  - Export S-parameters and import in ADS
  - All ports are 50-Ohm terminated
  - Connect RF and DC sources
  - Connect the diode on "diode port" where it is a 50-Ohm termination port (in CST)
  - Simulations with both diode models (static and equivalent in ADS)



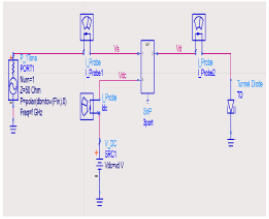
## Active Antenna (3-port model)

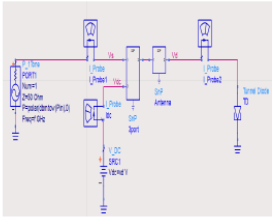





## Active Antenna (3-port model in ADS)







## Active Antenna (3-port model in ADS)

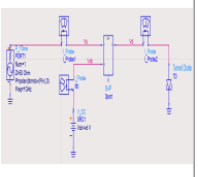
- Define power gain as

$$G = \frac{P_{rad}}{P_{avs}} = \frac{P_1 - P_2}{P_{avs}}$$

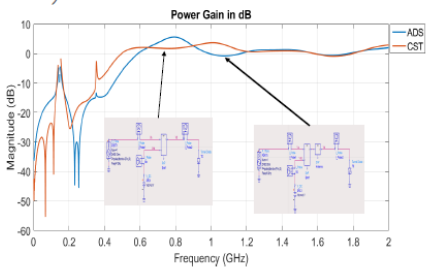
where

$$P_1 = \frac{1}{2} Re\{V_S I_1^*\}$$

$$P_2 = \frac{1}{2} Re\{V_d I_2^*\}$$



## Active Antenna (3-port model in ADS)

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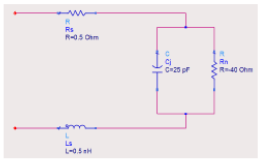
## Tunnel diode (Equivalent Model)

- Equivalent circuit when diode is biased in the NRR
- Frequency-dependent linearized model



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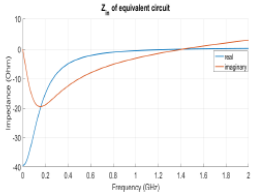
## Tunnel diode (Equivalent Model)

- Input impedance
- Resistive-cutoff frequency $\mathrm{Re}\{Z_{in}\}=0$
- Self-resonant frequency $\mathrm{Im}\{Z_{in}\}=0$

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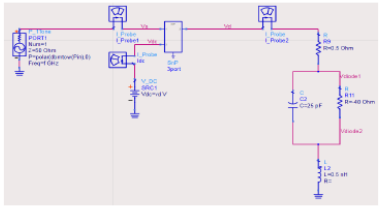
## Active Antenna (3-port model in ADS)



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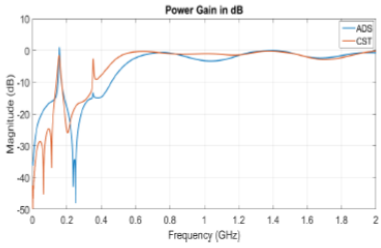
## Active Antenna (3-port model in ADS)

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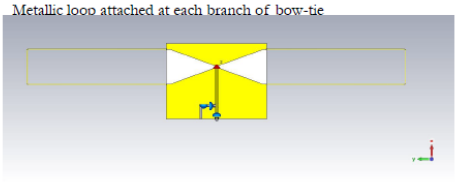
## Modified Active Antenna

- Modify so that it the antenna works in lower frequency
- Metallic loop attached at each branch of bow-tie



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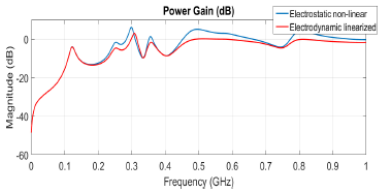
## Active Antenna (3-port model in ADS)

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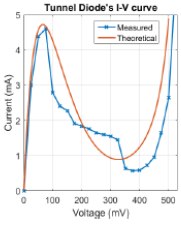
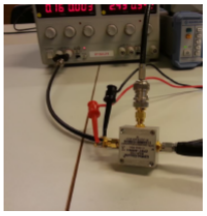
## Measurement Results

- Measured the IV curve of the diode
- Current going through the diode with variable voltage



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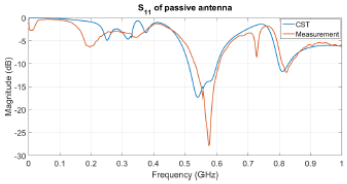
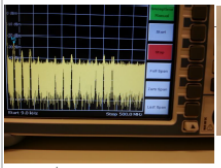
## Measurement Results

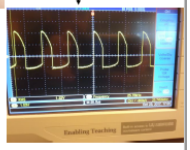





## Measurement Results



Oscilloscope



Oscillations in the entire structure measurement

Only diode circuit



## Conclusions and Future Work Suggestions

- Possible to have power gain (using the definition of this project)
- Low frequency function of tunnel diode
- Improve the design of antenna
- Test the same design approach with different amplifying device (transistors)



## Thank you

Questions?