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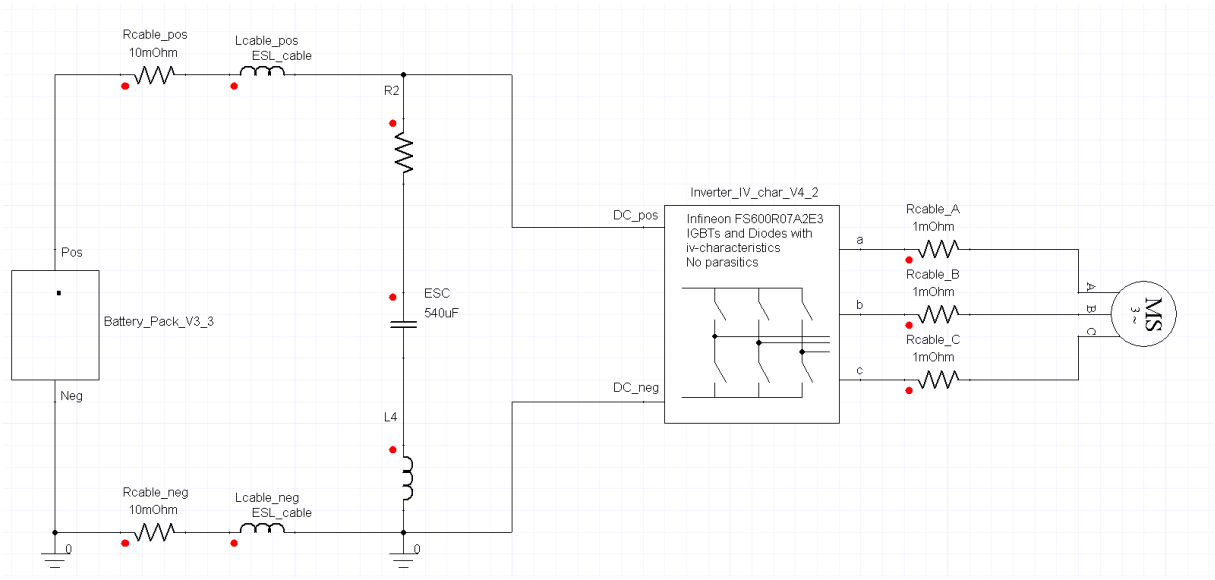

SiC Converter for Electrical Vehicle – DC-Link Ripple

Master's thesis in Electric Power Engineering

ANTON HOLM

Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2017

MASTER'S THESIS 2017

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Cover: Simplified figure of the simulation model used throughout the thesis, closer described in Section 3.2.

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Abstract

The increased focus towards electrification of the transportation sector increases the need for smaller, lighter, cheaper and more efficient inverters for use in drivetrains. In most of these inverters, the DC-link capacitor makes up a large portion of the total inverter volume and weight. It is therefore interesting to analyze the DC-link current and voltage ripple which is one of the major dimensioning factors of the DC-link capacitor. Throughout this thesis, simulations of the DC-link ripple are performed to evaluate how well the actual ripple can be predicted for a PMSM-drivetrain. In addition to this, an investigation of the impact of switching from Si-IGBTs to SiC-MOSFETs is performed. To accomplish this and to evaluate the simulation model, the simulation model was compared to both theoretical calculations as well as with actual measurements on a drivetrain.

By comparing simulation results with actual measurements on a drivetrain, it was showed that the fundamental components of the DC-link current ripple can be simulated with 5 % accuracy for the evaluated operating points. This proves that system-level transistor models produce a good result in relation to their complexity. However, the simulated DC-link voltage was not as accurate. This can be derived to the DC-link capacitor model which did not accurately enough reproduce the transfer function from the injected inverter current to the voltage ripple on the DC-link. It was also shown that the impact on ripple was negligible when using SiC-MOSFETs as opposed to the original Si-IGBT if all other parameters were kept constant. SiC-MOSFET was shown to have advantages over Si-IGBT in that the switching frequency could be increased, as well as increased efficiency. The efficiency could especially be increased when using reverse conduction which showed no impact on overall ripple levels.

By having a simulation model that can accurately reproduce the DC-link ripple, better dimensioning of the DC-link capacitor and other converters attached to the DC-link can be performed. Also, parameter optimization for ripple minimization can help to reduce cost, size, weight and materials used in inverters for EV/HEV applications.

Keywords: SiC, Silicon Carbide, Reverse conduction, Inverter, DC link, Ripple, Ripple simulation, PMSM drivetrain, Electric vehicle.

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Finally, I would like to give my gratitude to Volvo Cars and the entire RIFEL-group. It is with their support that this thesis could be performed and I am thankful for them allowing me access to their work and the necessary materials needed for this thesis. Discussions with, and help from, several individuals from the RIFEL-group was essential especially during the creation of the simulation model.

Anton Holm, Gothenburg, 2017

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1 Introduction

1.1 Background

Electrification of vehicles has become increasingly important as the demand for sustainable transportation increases. For both hybrid-electric vehicles (HEV) and electric vehicles (EV), DC-AC converters needs to be implemented to convert the DC-voltage of the battery to the controlled AC-voltage that is needed for the electric machine. However, a drawback of conventionally used silicon (Si) IGBT converters is the fact that they are limited in switching frequency due to high losses. Switching to silicon-carbide (SiC) MOSFET would enable higher efficiency at higher switching frequencies [1].

Most of the passive components in a converter (e.g. DC-link capacitor, line filter and heatsink) will be reduced in size if a converter with higher efficiency and higher switching frequency could be used. When taking into account that these passive components usually constitutes about 70-80 % of the total weight and volume of a typical converter, a substantial size reduction for a converter of the same output power can be achieved [1].

In addition to the fact that being able to use smaller DC-link capacitors would lead to a cheaper, smaller and lighter converter there could also be reasons of sustainability for striving towards smaller DC-link capacitors and should therefore be investigated with regards to the materials used in their construction.

An increased switching frequency will also result in a lower DC-link voltage and current ripple, something that is often desired as it reduces stress on the other components connected to the same DC-link. In a HEV and EV, examples of other units can be other inverters, DC/DC converters, air conditioning units and the high voltage battery itself. Being aware of the ripple level emitted by a converter as well as which factors that affect the magnitude and distribution of the ripple is very important when designing an electric drivetrain. Traditional simulation models used during development are in many cases aimed at full-vehicle simulations where factors such as efficiency are of greater interest. To solve this, a more advanced model of the converter that takes its non-ideal behavior into account becomes necessary.

Detailed system simulations is the main focus area of the project Ripple and Electromagnetic Fields in Electric vehicles (RIFEL), that has been undertaken by Volvo Cars, Chalmers University of Technology and RISE. This thesis will be based around the Ansys Simplorer simulation model as well as the drivetrain rig built as a part of this project.

1.2 Aim and Problem Statement

The purpose of this thesis is to investigate and model the voltage and current ripple emitted on the DC-link by a DC-AC converter used in a hybrid electrical vehicle to drive a permanent-magnet synchronous motor (PMSM). The effects of using SiC MOSFETs compared to conventional Si IGBTs will be explored as well as identifying which parameters that are most important for the emitted ripple level. In addition to this, the obtained simulation results will be compared to measurements on an existing Si-IGBT converter.

To fulfil the aim of the thesis the following points will be addressed:

- Modelling of the semiconductor switches and the surrounding circuitry to best reproduce the DC-link ripple.
- Factors that affect the DC-link ripple spectrum.
- Modelling of the DC-link capacitor to best represent the capacitor used in the actual system.
- Changes in inverter power loss when using SiC-MOSFET, along with reverse conduction, in comparison to Si-IGBT.

1.3 Scope

The surrounding equipment, battery, cables and electrical machine will be considered as ideal components since the main focus of this thesis lies on the inverter. In addition to this, the modelling will not consider any thermal dependence of the included components. Also, the impact of different switching strategies will not be evaluated in this thesis; only PWM-switching will be implemented to evaluate the influence of the hardware.

1.4 Environmental and ethical aspects

This thesis touches on subjects that include both ethical and environmental aspects, thus this section will briefly analyze possible implications as well as give an account of how the workflow of this thesis has been designed to address these issues.

As previously mentioned, the DC-link capacitor makes up a significant part of a typical inverter in an EV/HEV [1] making the inverter both heavier, bulkier and more expensive the bigger the DC-link capacitor is. As a result of this, the DC-link capacitor also becomes a big source of electronic waste when recycling and disposing of old inverters.

The main dimensioning factor when it comes to the DC-link capacitor size is the DC-link current ripple emitted by the inverter. Prediction of the DC-link ripple is often done through simple calculations and estimations that yield uncertainties and thus the size is often exaggerated. Having a simulation model that better reproduces the DC-link behavior of the inverter could help in selecting a DC-link capacitor large enough to fulfil the ripple requirements but without over-dimensioning it. Not only could this mean a decrease in capacitor size and weight, but also less use of materials. In addition to this, determining the exact ripple level of the DC-link also reduces the need to over-engineer all peripheral components connected to the DC-link which decreases the cost of these components. This in turn leads to HEV and EV that are cheaper to produce which could help accelerate the transition from combustion engines.

Another approach to decrease DC-link capacitor size is through minimizing the DC-link current ripple. Typically, this is done through increasing the switching frequency of the inverter, however the silicon-IGBTs typically used are limited in their use in high-frequency applications. One possible solution to this is the silicon-carbide (SiC) technology [2]. Using SiC-MOSFETs as an alternative to Si-IGBTs higher switching frequencies can be achieved while still retaining a high efficiency during switching [2]. Because of this increase in switching

frequency and decrease in inverter losses the total size and weight of the inverter can be decreased, both through a smaller DC-link capacitor as a result of the lower ripple, as well as through less cooling needed due to lower losses.

Simulation models are used more and more frequently during research and development. As described in [3], simulation models are to a great extent taking over the role that was previously held by experiments. This sort of change brings with it ethical and societal dilemmas that needs to be considered when developing as well as using simulation models, computational calculations and their results.

Several different aspects regarding the development and the usage of simulation models need to be considered to ensure that the models and their results, can be considered both ethical and sustainable from a societal point of view [3]. To start with, the limitations of the model needs to be clearly defined, such as to inform the user of possible operating points at which the simulation model will not give feasible/usable results. To address this issue throughout this thesis, any assumptions or simplifications made are clearly stated and the possible implications are discussed so that the user is aware of how the data has been collected and how it should be used.

The second aspect that needs to be considered is the validation of the simulation model. Simulation model verification is often costly in both time and money and can be done in a multitude of different ways where comparison with experimental data is the most common method [3-5]. When it comes to accommodating this issue, the workflow of the thesis has been set such that initial theoretical calculations of the ripple emitted by the inverter is calculated, followed by simulations of the system and ending with measurements on a physical system. In this way, the simulation model can be compared and verified against two different sources; theory and experimental results.

2 Theoretical background

2.1 PMSM drivetrain

Permanent magnet synchronous machine (PMSM) traction systems are popular within EV and HEV due to its high-power density [6, 7]. The most basic version of a typical drivetrain consists of a PMSM and a three-phase inverter which is fed from a battery as shown in Figure 2.1. To better understand the reason of DC-link current and voltage ripple, some base knowledge of PMSM-based drivetrains is needed and will thus be covered in the following chapters.

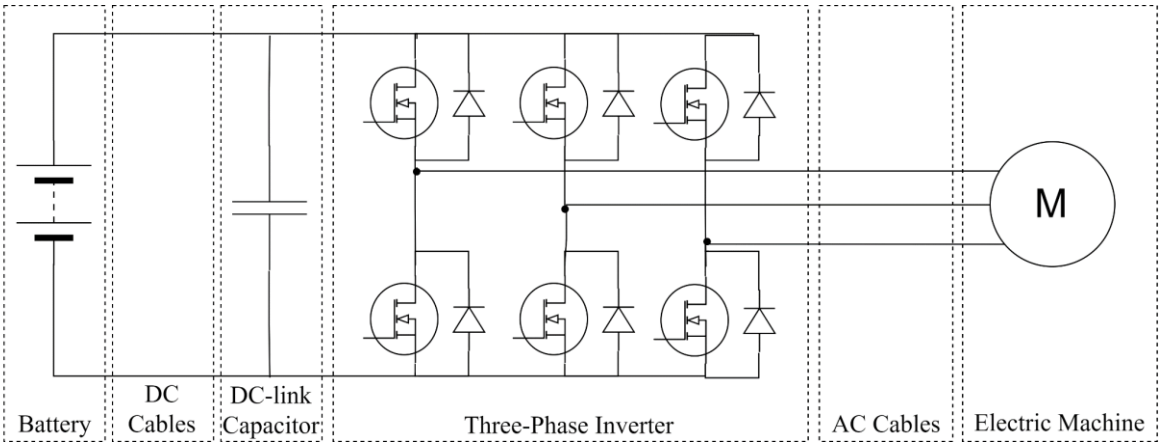

Figure 2.1. Overview of a typical PMSM drivetrain, including battery, cables, DC-link capacitor, three-phase inverter and the electric machine.

2.2 Permanent Magnet Synchronous Machine

As previously mentioned, the PMSM is often considered for EV/HEV applications due to its high power density [6]. The main reason for this, and what separates a PMSM from other electrical machines, is the fact that it uses permanent magnets to create rotor flux instead of windings fed through commutators as is the case for traditional DC-machines. This means that no rotor windings are necessary and thus no copper losses will take place in the rotor, which reduces the losses inside the rotor and therefore also the rotor temperature. As a result of this, more power can be put through a PMSM than for example a DC-machine of similar rotor/stator size before the same rotor-temperatures are reached [8]. Another benefit of not having any rotor windings and thus no commutators or brushes is the fact that there are less components in need of regular maintenance. One downside is that it is no longer possible to use the excitation of the rotor windings to control the machine since the flux produced by the permanent magnets are fixed [8]. Due to this an inverter with associated control system is required to control the speed and torque.

2.2.1 Reference Frame Transformation

To simplify the control and modelling of a PMSM, dq-transformation is often used. This procedure includes replacing the three 120º separated windings generally associated with a three-phase machine with two equivalent orthogonal windings that produce the same resulting space vectors. In addition to this, the reference frame is also shifted from the stator (stationary)

to the rotor (rotating) [9]. Typically, this transformation is performed in two steps, Clarke- and Park-transformation.

The Clarke transformation takes care of the first part, moving from a three axes reference frame denoted abc on the left-hand side of Figure 2.2 into the two stationary orthogonal axes, α and β. This transformation is due to this commonly referred to as αβ-transformation or two-phase stator reference frame. This equivalent two-phase system can reproduce the same resulting voltage, current and flux phasors as the original three winding system asides from any zero-sequence present in the system. However, for normal operation of three-phase machines, the zero-sequence is not present as the machine impose a balanced load [9].

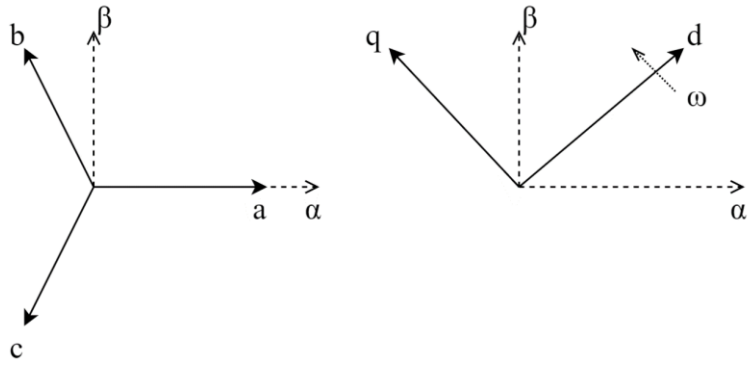

Figure 2.2. Visualization of the different reference frames, abc, αβ and dq.

The Park transformation takes this one step further by introducing a rotating reference frame. In much the same way as for Clarke transformation, the result is a two-phase orthogonal system denoted d and q, but as indicated in the right-hand side of Figure 2.2 it rotates with the speed ω. This speed is the same as the rotor speed meaning that the dq-reference frame rotates along with the rotor and is thus often referred to as the rotor reference frame [9].

2.2.2 Equivalent Equations of a PMSM

In the dq-reference frame the stator voltage of the machine can be described by

$$\mathrm{v_d}(t) = R_s i_d(t) + \frac{d\psi_d(t)}{dt} - \omega_e(t)\psi_q(t) \tag{2.1}$$

$$\mathrm{v_q}(t) = R_s i_q(t) + \frac{d\psi_q(t)}{dt} - \omega_e(t)\psi_d(t) + \omega_e(t)\psi_m \tag{2.2}$$

where v_d, v_q, i_d and i_q are the dq-components of the stator voltage and current, R_s is the stator resistance, ω_e is the electrical speed of the machine, ψ_d and ψ_q are the dq-components of the flux linkage and ψ_m is the permanent magnet flux linkage. The flux linkage can be described by

$$\psi_d(t) = i_d(t)L_d \tag{2.3}$$

$$\psi_q(t) = i_q(t)L_q \tag{2.4}$$

where L_d and L_q represents the dq-components of the stator inductance. Due to saliency, the non-symmetry of the rotor geometry and materials, the d- and q-inductance varies depending on the rotor position. In addition to this, magnetic saturation also causes the inductance values to differ depending on the current through the windings. Finally, the torque equation can be written as

$$T_e(t) = \frac{3p}{4}\left(\psi_m i_q(t) + (L_d - L_q) i_d(t) i_q(t)\right) \tag{2.5}$$

where p represent the number of poles in the PMSM.

2.2.3 Control of PMSM

By using (2.1) to (2.5), a dq-oriented control system can be implemented to control the PMSM. One of the major benefits of the dq-reference frame is that during steady-state the voltage and current vectors are rotating at the same speed as the reference frame and can thus treated as DC-quantities. This enables the use of regular PI-controllers.

Typically, a control system based on PI-controllers for a PMSM includes three main parts; a speed controller, a current controller and a field-weakening algorithm. The speed controller takes a speed reference input as well as a measurement of the actual speed and produces a dq-current reference as seen in Figure 2.3. These dq-currents are typically found using maximum torque per ampere (MTPA) which produces the combination of d- and q-current that results in the lowest total stator current for a given torque requirement. The desired dq-current reference is fed into a PI current controller. The current controller then compares the reference currents with the actual current to the machine. This current controller can, using equations derived from (2.1) and (2.2), generate a dq-voltage reference which becomes the voltage reference for the inverter that is connected to the machine.

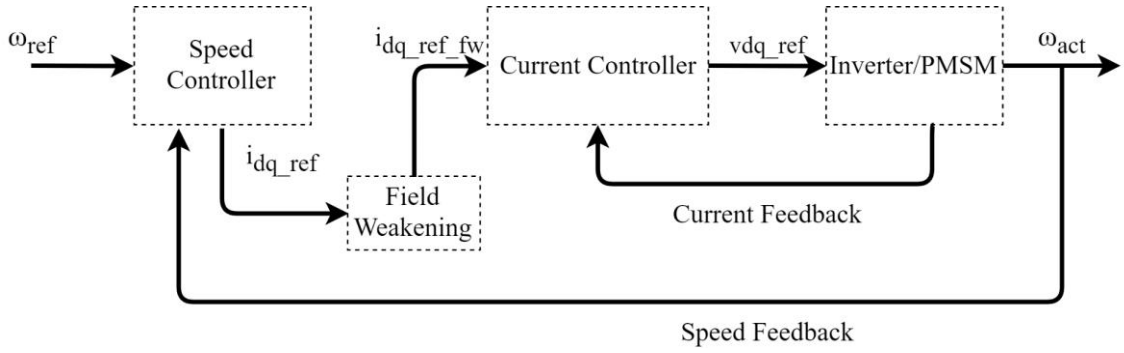

Figure 2.3. Block diagram of simplified control system.

One problem when controlling a PMSM is that back-emf of the machine increases as the speed increases which can be seen in the third and term of (2.1) and (2.2). At high speeds, this means that more voltage must be supplied to the terminals than what is available on the DC-link only to overcome the back-emf. This condition can be described as

$$v_s = \sqrt{v_d^2 + v_q^2} \leq v_{s,max} \tag{2.6}$$

where v_s denotes the stator voltage and $v_{s,max}$ is the maximum stator voltage that can be applied [10]. The resulting dq-voltage reference from the current controller can be compared to the maximum available stator voltage and if this condition is not met, field weakening can be used to decrease the back-emf produced by the machine [10]. What field weakening does is that it reduces the back-emf components of (2.1) and (2.2) by choosing a dq-current reference outside of the MTPA-curve, in Figure 2.3 referred to as $i_{dq\_ref\_fw}$. This results in a decreased torque but it also enables operation of the machine at higher speeds than base speed or the same stator voltage [10].

2.3 Three-Phase Inverter

To be able to control the PMSM by means of voltage and frequency control from a DC supply, a three-phase inverter is commonly used. The three-phase inverter consists of six semiconductor-switches, most commonly IGBTs or MOSFETs, that are controlled in such a way that a three-phase output voltage with variable amplitude and frequency can be achieved. Connected opposite to each transistor are antiparallel diodes which provide a path for the current to flow in the opposite direction of the transistor during operation of an inductive load such as an electric machine [11]. Figure 2.4 shows a typical three-phase inverter including the DC-link capacitor on the left-hand side. Each vertical pair of switches are often referred to as phase-legs and the middle point of each phase-leg constitute the three output phases of the inverter denoted as *A*, *B* and *C* in Figure 2.4.

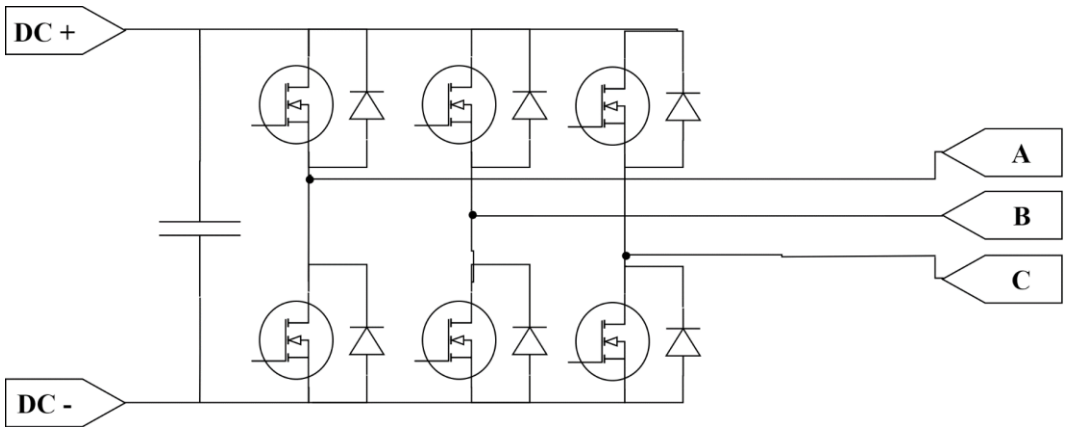

Figure 2.4. A schematic view of a three-phase inverter without any parasitic elements.

By alternating which transistor in each phase leg that is turned on, the mid-point and thus the output of the inverter, is either connected to the positive or negative side of the input DC-voltage. By alternating between these two in different ways, a controlled output voltage and frequency can be achieved [12].

2.4 Pulse-Width-Modulation (PWM)

To control the different switches of the inverter in order to create a sinusoidal output, pulse-width modulation (PWM) is often used. The operating principle is to generate three control signals which each control one phase leg of the inverter, see Figure 2.5. There are two levels to the control signal (high and low) which determine which switch of the phase leg that should be

closed respectively open. Since closing both switches of a phase leg at the same time would result in a short circuit of the DC-link, the two switches are operated in inverse with respect to each other.

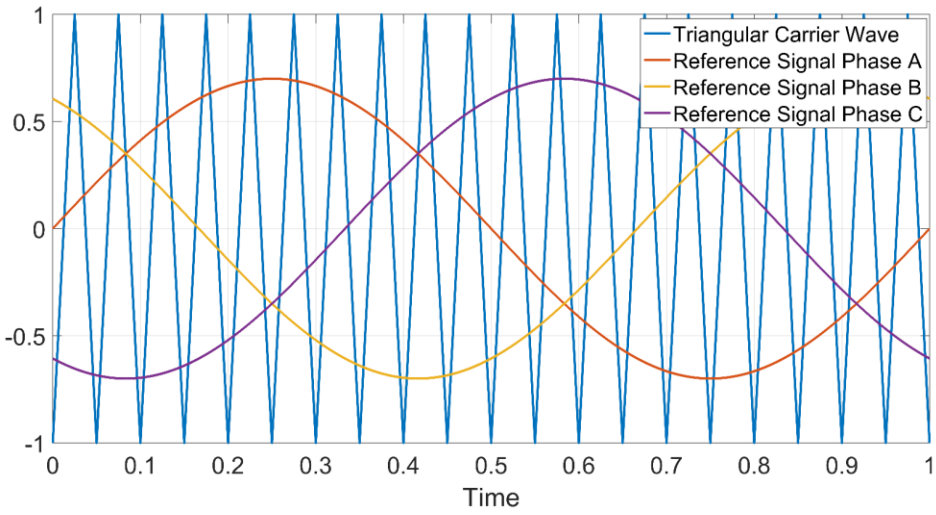

Figure 2.5. Triangular carrier wave used in PWM and sinusoidal reference signal. $m_a = 0.7$ and $m_f = 20$.

The control signals can be generated by comparing the three sinusoidal (one for each phase) reference signals to a triangular carrier wave. When the reference signal is greater than the carrier wave, the control signal for that phase is set high while the opposite applies when the reference falls below the carrier wave. This is visualized in Figure 2.6 where the control signal is created by comparing the carrier wave and the reference signal. The same is done for the two other reference signals to generate control signals for all three phase-legs. As previously mentioned, the two switches in each phase leg are operated inversely to each other which gives that the upper switch in a phase leg is turned on by a high control signal while the lower switch is turned on by a low control signal.

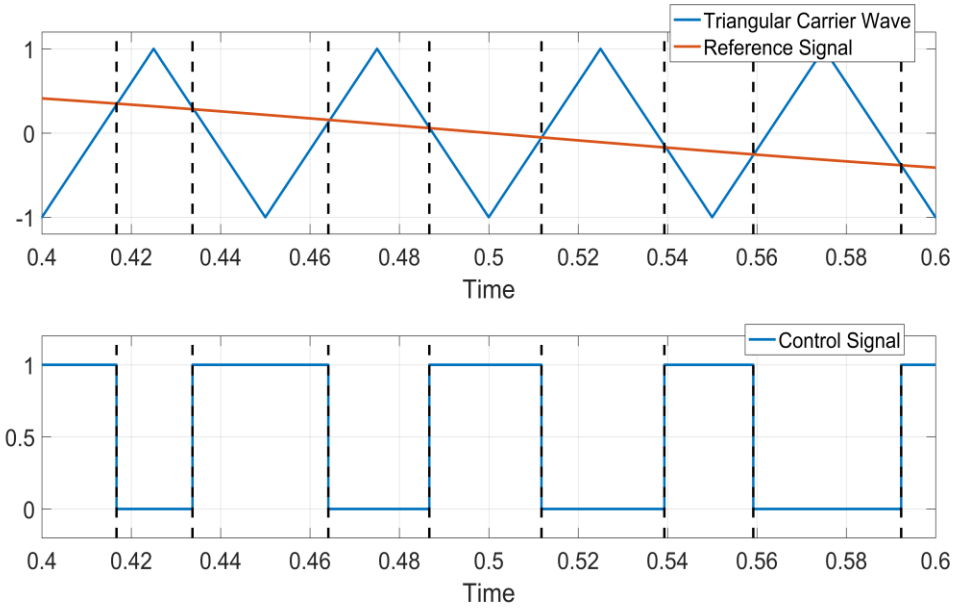

Figure 2.6. Control signal generated by comparison of a reference signal with a triangular carrier wave.

Two parameters that governs the performance of the PWM is the amplitude modulation ratio (m_a) and the frequency modulation ratio (m_f). The amplitude modulation ratio is defined as

$$\mathrm{m_a} = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{2.7}$$

where $\hat{V}_{control}$ denotes the amplitude of the sinusoidal reference signal and $\hat{V}_{tri}$ is the amplitude of the triangular carrier wave signal [13]. The frequency modulation ratio is defined as

$$\mathrm{m_f} = \frac{f_{sw}}{f_o} \tag{2.8}$$

where f_{sw} is the carrier wave frequency which corresponds to the switching frequency of the inverter and f_o is the reference signal frequency which corresponds to the fundamental component of the output [13]. Figure 2.5 depicts a typical scenario with amplitude modulation ratio, between the carrier wave and reference signals, of 0.7 and a frequency modulation ratio of 20.

2.5 Battery Modelling

When simulating a PMSM driveline for EV or HEV applications, additional components needs to be considered as well. As the power source in this case consists of a battery connected via non-ideal cables, the DC-side can no longer be considered constant with zero impedance. A commonly used battery simulation model is the second order RC equivalent circuit depicted in Figure 2.7 [14]. This battery model includes the open-circuit voltage denoted as E, the internal resistance R_S, which contributes to most of the ohmic losses as well as two RC-circuits which help to model polarization effects within the battery [15, 16]. By implementing two RC-links the dynamic behavior of the battery can be modeled. It also adds a time dependence to the output voltage rather than simply making the output voltage dependent on the voltage drop over R_S [15, 16].

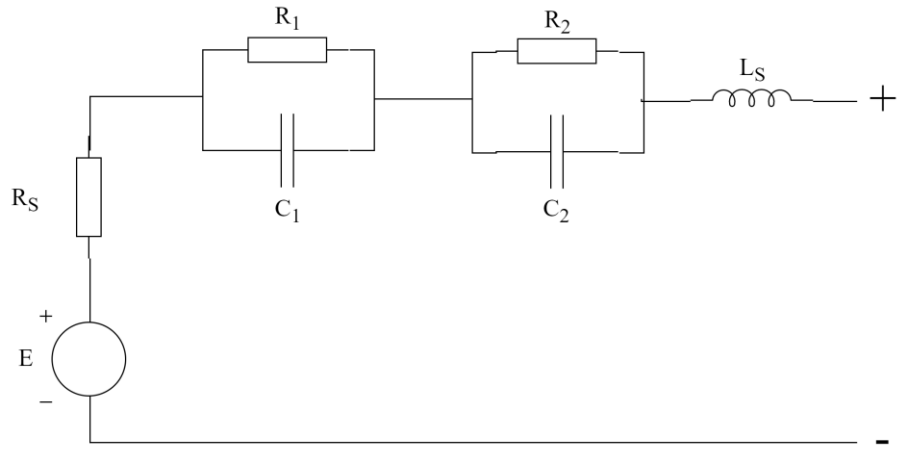

Figure 2.7. Battery model including internal battery voltage source, series resistance and inductance and a second order RC circuit.

2.6 Cable Modelling

As previously mentioned, the nonidealities of the cables connecting the battery to the inverter and the inverter to the electric machine also needs to be considered since they introduce more resistance and inductance to the system. In this thesis, this influence is modelled as a series resistance and a series inductance, see Figure 2.8. However, more advanced models such as the pi-model are available but due to reasons of simplicity, these models are omitted in this work [17, 18].

Figure 2.8. Cable model with series inductance (L_s) and resistance (R_s).

2.7 DC-link Capacitor

Attached to the DC-side of the inverter is a DC-link capacitor whose main functions include filtering of the DC-side voltage and attenuation of the ripple currents that are drawn from the DC-link by the inverter. DC-link capacitors does not only fill a very important role in the operation of a typical EV driveline but are most often bulky and heavy and can contribute to a significant portion of the total inverter volume and weight [19, 20].

2.7.1 Capacitor Modelling

Several different complexities of non-ideal modelling of capacitors are available, all with different applications and with different number of non-ideal effects being taken into consideration. One of the most commonly used simulation models is depicted in Figure 2.9 .This model consists of the equivalent series resistance (R_{ESR}) and the series inductance (L_S). The equivalent series resistance (ESR) is a lumped parameter representation of the resistive and dielectric losses of the capacitor while the inductance is introduced by the leads or terminals of the capacitor as well as the construction of the capacitor itself [21].

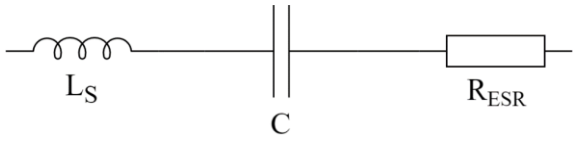

Figure 2.9. Capacitor model including equivalent series resistance (R_{ESR}) and series inductance (L_S).

2.8 Ripple in three-phase inverters

2.8.1 DC-side harmonic content

When analyzing the DC-side harmonic content a common simplification is to consider the two IGBTs and antiparallel diodes of each phase-leg as a single ideal switch, see Figure 2.10.

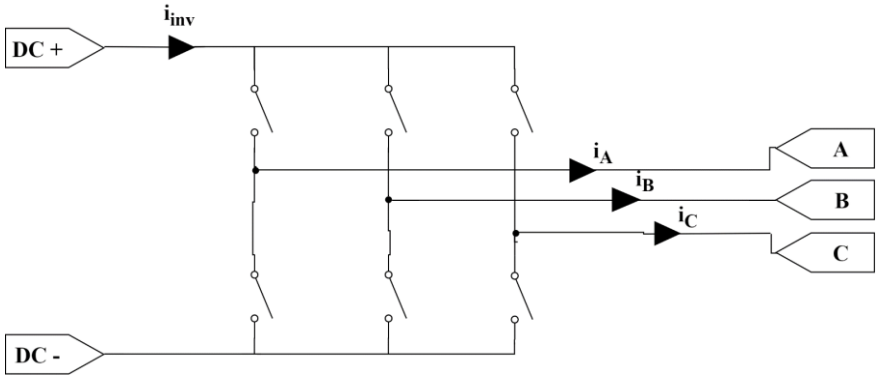

Figure 2.10. Three-phase inverter where the transistors are approximated with ideal switches.

The current drawn by the inverter (i_{INV}) is dependent on the phase currents i_A, i_B and i_C as

$$i_{INV} = S_A i_A + S_B i_B + S_C i_C \tag{2.9}$$

where S_A, S_B and S_C are the switching functions of the three phase legs that originate from how the upper and lower switch in each phase leg is operated [22]. The three output currents of the inverter are in the ideal case sinusoidal and due to the balanced inductive load, each phase current can be expressed as

$$i_A = I_0 \cos(\omega_o t + \varphi) \tag{2.10}$$

$$i_B = I_0 \cos\left(\omega_o t - \frac{2\pi}{3} + \varphi\right) \tag{2.11}$$

$$i_C = I_0 \cos\left(\omega_o t - \frac{4\pi}{3} + \varphi\right) \tag{2.12}$$

where φ is the is the load angle and I_0 is the current magnitude. To determine the switching functions of a PWM-controlled three-phase inverter, double Fourier series method was introduced by [23] and is a generally accepted approach.

By using the double Fourier series method, solving for the switching functions and using this in (2.9) in combination with (2.10) (2.11) and (2.12), it has been shown in [24] that the resulting inverter current can be described by

$$\begin{aligned} i_{INV} = {} & \frac{3}{4} m_a I_0 \cos\Phi \\ & + I_0 \frac{2}{\pi}\frac{1}{2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m} J_n(m\frac{\pi}{2}m_a)\sin\left((m+n)\frac{\pi}{2}\right)\Big[\cos(m\omega_c t \\ & + (n-1)\omega_o t - \Phi) + \cos(m\omega_c t + (n+1)\omega_o t + \Phi) \\ & + \cos(m\omega_c t + (n-1)\omega_o t - \Phi - (n-1)\frac{2\pi}{3}) \\ & + \cos(m\omega_c t + (n+1)\omega_o t + \Phi - (n+1)\frac{2\pi}{3}) \\ & + \cos(m\omega_c t + (n+1)\omega_o t - \Phi + (n-1)\frac{2\pi}{3}) \\ & + \cos(m\omega_c t + (n+1)\omega_o t + \Phi + (n+1)\frac{2\pi}{3})\Big] \end{aligned} \tag{2.13}$$

in which $J_n(x)$ denotes the Bessel function of the first kind, while ω_c and ω_o is the switching- and output frequency respectively. This equation shows how the current into the inverter behaves and how it is affected by PWM-parameters such as switching- and output frequency, load angle and amplitude modulation ratio.

Figure 2.11 depicts the inverter current that results from solving (2.13) using the two different operating points specified in Table 2-1, with operating point 1 on the left and operating point 2 on the right. As seen from the figures, the inverter current depends heavily on the operating point. The results of these theoretical calculations can be useful when verifying initial simulation results as they should match the current drawn by a simulated ideal inverter using PWM-control during the same operating conditions.

Table 2-1. Parameters used in theoretical calculations.

Parameter	**Value**	
	Operating Point 1	**Operating Point 2**
f_{sw} *[kHz]*	10	10
f_o *[Hz]*	200	100
φ *[rad]*	π/4	π/6
m_a	0.7	0.3
I_o *[A]*	50	30

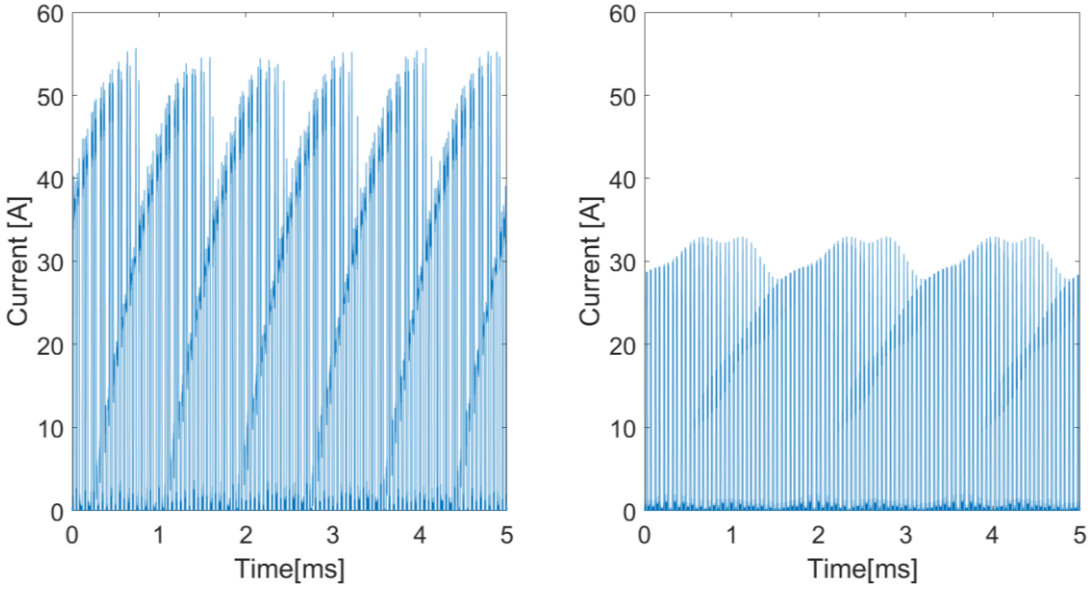

Figure 2.11. Theoretical inverter current for operating point 1 (left) and operating point 2 (right) without a DC-link capacitor.

To be able to compare and evaluate the result of the theoretical calculations, performing an FFT gives the harmonic content in the frequency domain, see Figure 2.12. The largest harmonic content for a PWM-controlled three-phase inverter is expected to be found at twice the switching frequency, in this case 20 kHz. Worth noting is the fact that the switching frequency is not present in the harmonic analysis for either operating point, sidebands are however present at the switching frequency [24]. By analyzing this figure, it becomes clear that the ripple harmonics vary heavily on which operating point that is chosen. The switching frequency was kept constant for the two operating points but the fundamental frequency of the output was

changed which alters where the side-band harmonics end up. The biggest difference between the two operating points is how the change in load angle, amplitude modulation ratio and current level adjusted the distribution of ripple; Operating point two had a large decrease in ripple at 20 kHz but a major increase at 40 kHz as opposed to the first operating point.

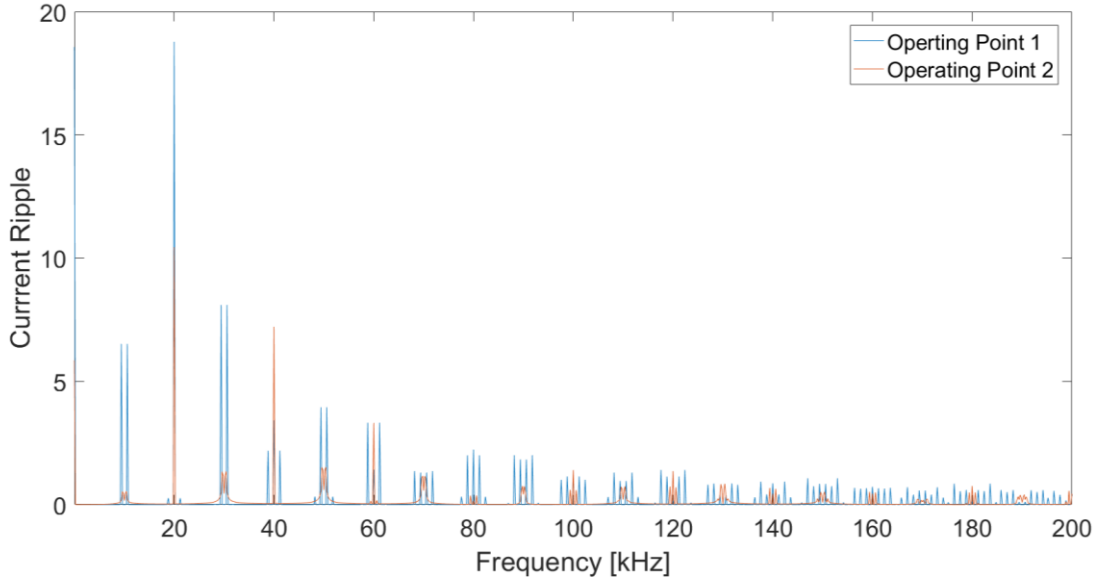

Figure 2.12. FFT of the theoretical inverter current up to 100 kHz not including DC-component for two different operating points.

2.8.2 Ripple mitigation

It is important to make a distinction between the two regularly occurring phenomenon; ripple and switching transients. In Figure 2.13, typical DC-link voltage is shown, there exists periodic variations around the DC-value of the voltage with a marked amplitude of 2 V and high frequency transients at each transistor switching. The periodical triangular-shaped variations are often denoted as ripple and the high frequency spikes that occur during switching of the transistors are called switching transient. The transient spikes occur due to the switching of the transistor in conjunction with the inductances that exists around the transistor. The ripple however is determined by how the inverter is operated as well as the parameters of the DC-link capacitor.

Mitigation of voltage and current ripple can be accomplished in two ways; by decreasing the amount of ripple produced or by increasing the attenuation of ripple. As discussed in Section 2.7, the DC-link capacitor is very important when attenuating the DC-link current ripple, thus one way to attenuate the ripple further is to increase the size of the capacitor.

One way to decrease the total ripple is to increase the switching frequency. Not only does this move the ripple components into higher frequencies and possibly out of the audible range, but it also decreases the ripple magnitude. This occurs since there is less time between the turn on and turn off instances and thus the DC-link capacitor will be able to easier supply the energy needed during these shorter intervals [20]. This decreased energy or charge that must be stored/supplied by the capacitor results in smaller variation of capacitor voltage.

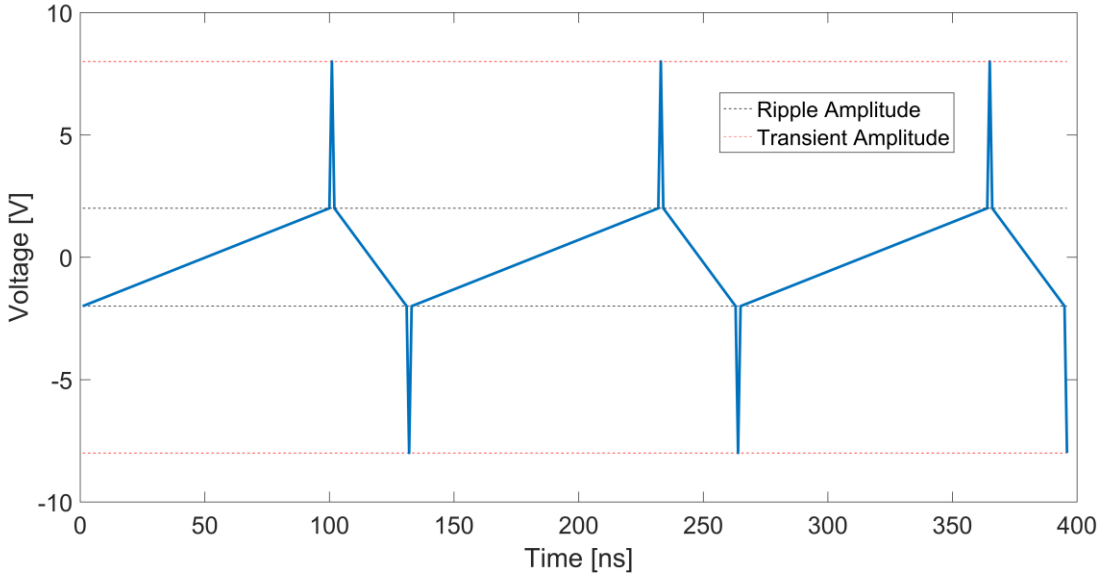

Figure 2.13. Illustration of ripple and switching transients in a typical DC-link voltage.

Minimizing the parasitic elements such as the stray inductances inside the inverter and the DC-link capacitor is another way to try and decrease the resulting switching transients. Figure 2.14 shows some of the parasitic inductances (L_1, L_2 and L_3) that occur in a physical inverter. These parasitic elements influence the switching transients since high voltages can occur when inductances see high current derivatives when a transistor is turned on or off [20]. Studies have also shown that the values of the parasitic elements, e.g. capacitor and cable series resistance and inductance can greatly impact both current and voltage ripple [25].

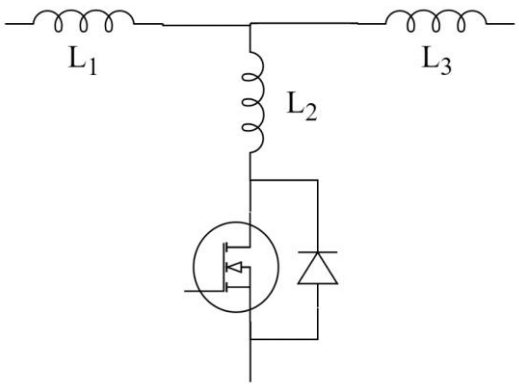

Figure 2.14. Parasitic inductances surrounding one of the transistors in a three-phase inverter.

2.9 SiC MOSFET

Silicon has long been the dominating choice when it comes to semiconductor technology and in the case of high power inverters, silicon IGBTs are commonly used. However, silicon-

carbide (SiC) technology has been a possible competitor due to some of its material advantages. SiC has a higher electron band-gap which results in a higher electric breakdown field and gives the ability to block higher voltages than silicon. In addition to this, SiC also has better thermal conductivity. SiC might also motivate the use of MOSFETs instead of IGBTs which would enable the use of higher switching frequencies and other benefits associated with MOSFETs [2].

2.9.1 Reverse conduction

An IGBT cannot conduct negative current due to the internal pn-junction which means that all negative current must flow through an antiparallel diode. The MOSFET can (asides from the dead-time) conduct negative current in parallel with the antiparallel diode [26]. Since conduction losses are associated with the square of the current, the overall conduction losses can be decreased if the current is split between the transistor and the antiparallel diode during the negative half of the fundamental period [26].

2.10 Semiconductor Loss Calculation

When using a three-phase inverter it can be beneficial to have a way to calculate the losses inside the semiconductor device. For a typical inverter, this would include either MOSFETs or IGBTs as well as the antiparallel diodes. For these devices, there are three main sources of loss that can be investigated; conduction losses, switching losses and blocking losses. However, the blocking losses are usually considered small enough to be neglected [27, 28]. The total loss can be expressed as

$$P_L = P_C + P_{SW} + P_B \approx P_C + P_{SW} \tag{2.14}$$

where P_L is the total semiconductor loss, P_C is the conduction loss, P_{SW} is the switching loss and P_B represents the blocking loss [27, 28]. The switching losses of both the MOSFET, IGBT as well as the antiparallel diode can be estimated by using the turn-on and turn-off energies (E_{ON} and E_{OFF}) given in their respective datasheets as

$$P_{SW} = (E_{ON} + E_{OFF}) f_{SW} \tag{2.15}$$

where f_{SW} denotes the switching frequency [27, 28].

The conduction losses for the three semiconductor devices needs to be determined in different ways for the three different devices. For an MOSFET, the average conduction losses during one switching cycle can be expressed as

$$P_{CM} = R_{DSon} {I_{DSrms}}^2 \tag{2.16}$$

where P_{CM} denotes the average conduction losses, R_{DSon} corresponds to the on-state drain-source resistance and I_{DSrms} is the rms-value of the drain-current of the transistor [28]. For an IGBT the equivalent equation is

$$P_{CT} = u_{CE0} I_{cav} + R_C \cdot I_{crms}^2 \tag{2.17}$$

where P_{CT} is the average IGBT conduction losses, u_{CE0} represents a constant voltage drop over the transistor during on-state, I_{cav} is the average collector-current, R_C denotes the on-state

resistance and I_{crms} represents the rms-value of the collector-current [27]. For the antiparallel diode, the equivalent equation become

$$P_{CD} = u_{D0} I_{Dav} + R_D I_{Drms}^2 \tag{2.18}$$

which gives that the average diode conduction losses (P_{CD}) can be calculated as a function of the equivalent diode on-state voltage drop u_{D0}, the average diode current I_{Dav}, diode resistance R_D and the rms-value of the diode current I_{Drms} [27, 28].

3 Case Set-Up

For all simulations and measurements performed, the DC-link voltage and current ripple is defined as the voltage over the DC-link capacitor and current from the battery respectively. The analyses and simulations performed in this thesis can be divided into three parts:

- Measurements and characterization of physical components in the actual drivetrain such as the DC-link capacitor.
- Ansys Simplorer simulations where a model of the drivetrain is implemented and in which the effect of parameter variation on ripple is investigated.
- Comparison between obtained simulation results and measurements on the full drivetrain rig available at Chalmers.

Throughout this thesis a method of visualizing the total ripple content in all frequencies of interest using the concept of total harmonic distortion (THD) was incorporated to complement the FFT-curves. The square root of the square sum of the most prominent frequency components were used as a measurement of total ripple. As opposed to conventional THD, this value is not normalized to the fundamental frequency component as the fundamental component (two times the switching frequency) contributes to the distortion, i.e. a larger fundamental component should equal a larger THD.

3.1 Measurements on Capacitor, characterization

As mentioned in Section 2.7 and 2.8, the DC-link capacitor plays a major part in the level of voltage and current ripple that can be expected on the DC-link. Due to this, the characterization and modelling of the actual DC-link capacitor becomes important. To properly replicate the behavior of the 540 µF film capacitor, a measurement of the impedance over a large frequency range is necessary. As seen in Figure 3.1 the capacitor investigated in this thesis has ten terminals, where the leftmost terminals is the positive and negative connection to the DC-link. The top three pairs each connect to a respective phase-leg of the inverter while the spare terminals at the bottom right are dedicated for any auxiliary supplies. This means that several measurements must be performed to be able to fully characterize the device. Table 3-1 shows summary a of the most important properties of the DC-link capacitor.

Figure 3.1. The DC-link capacitor used in the inverter with separate terminals for each phase leg.

Table 3-1. DC-link capacitor parameters.

Parameter	Value
Capacity	540 µF ± 5 %
Current rating	120 A (rms)
Type	Film capacitor
Length	240 mm
Width	63 mm
Depth	45 mm

To measure the impedance of the different terminals of the DC-link capacitor with high accuracy over a wide frequency range, an Omicron Bode 100 vector network analyzer was chosen as measurement tool. It is necessary to connect the capacitor to the measuring equipment as closely as possible since it reduces the stray inductance and contact resistance. To do this in best manner, small leads were soldered to each terminal of the capacitor and a B-WIC impedance adapter was used as seen in Figure 3.2. This setup enables measurement of the capacitor impedance over the full frequency range of the Bode 100 (10 Hz to 40 MHz). Care was taken during calibration of the network analyzer, especially the short-circuit calibration, as it impacts the accuracy of low impedance measurements. The settings used in the Bode Analyzer Suite for the capacitor measurements and the accuracy of the Bode 100 can be seen in Table 3-2 and Table 3-3 [29].

Figure 3.2. Close-up of impedance measurement connection.

Table 3-2. Settings used in Bode Analyzer Suite for capacitor measurements.

Setting	Value
Mode	Frequency Sweep (Impedance Adapter)
Start freq.	10 Hz
Stop freq.	40 MHz
Sweep mode	Logarithmic
No. of points	201
Level	13 dBm
Receiver bandwidth	10 Hz

Table 3-3. Bode 100 measurement accuracy [29].

Characteristic [23ºC ±5ºC]	Rating
Accuracy of Source level	± 0.3 dB (1Hz - 1MHz) ± 0.6 dB (1MHz - 40MHz)
Frequency accuracy	±15ppm (<1 year after calibration) ±25ppm (<3 year after calibration)
Noise floor gain measurement	1 Hz – 5 kHz: -100dB 5 kHz – 50 kHz: -110dB 50 kHz – 20 MHz: -115dB 20 MHz – 40 MHz: -110dB
Gain error Phase error	< 0.1 dB (calibrated) < 0.5º (calibrated)

3.2 Simulation model

The simulation model of the electrical driveline is implemented in Ansys Simplorer as a part of the Rifel-project including Volvo Cars AB, RISE and Chalmers University of Technology. Figure 3.3 depicts the original system model available at the start of the thesis which was to be improved upon and Figure 3.4 shows how the original inverter was modelled. In order to analyze the DC-link ripple, focus will be put on the inverter and the DC-link capacitor.

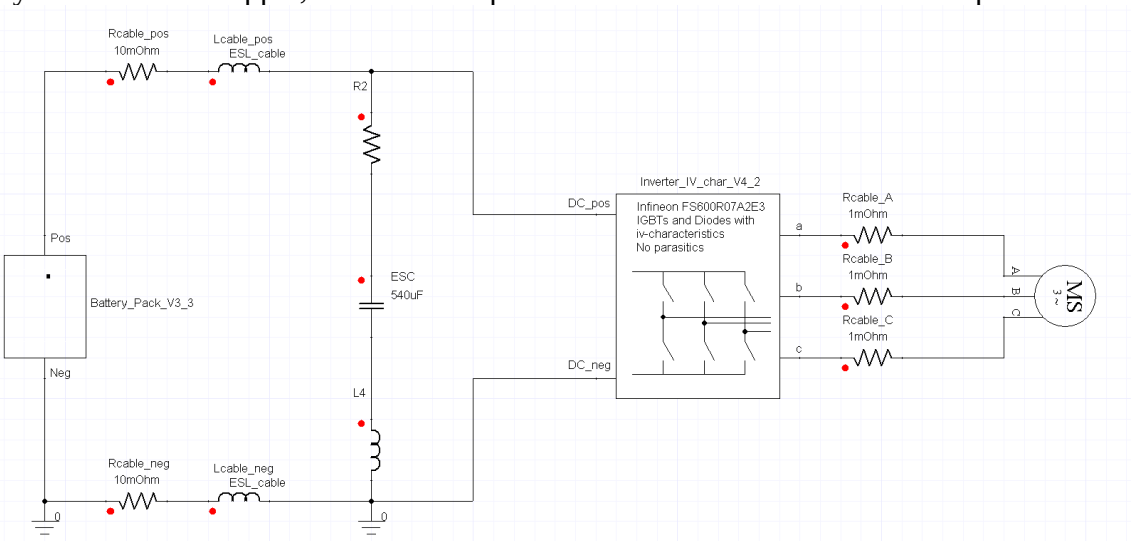

Figure 3.3. The Ansys Simplorer simulation model which includes battery model, DC-cable model, DC-link capacitor, inverter model, AC-cables and machine model.

The input references to the simulation model are the machine speed and the desired torque. These references are converted into current references and used in the actual controller which is modelled in MATLAB Simulink. The controller consists of a speed and current controller as described in Section 2.2.3. In addition to the control system, sinusoidal reference signals are generated from the dq-voltage reference to be used in PWM-operation. Appendix 1 shows the entire control system including a more detailed schematic of the current and speed controller, the field weakening algorithm and the sinusoidal reference waveform calculations. In this thesis, no changes will be made to the control system other than changing the switching frequency of the PWM controller. Note that the control system seen in Appendix 1 includes additional PWM and SVM reference waveform generation methods which are not used in this thesis.

The inverter model seen in Figure 3.4 initially included no parasitic elements and only considered the simplest IGBT model in Ansys Simplorer. This ideal IGBT is meant to be used as a system level IGBT and only takes into consideration the voltage-current relationship without any dynamic switching behavior. This voltage-current relationship (or iv-characteristics) can either be set by manually entering a forward voltage and bulk resistance, or tracing the V_{ce}-I_c curve available in the datasheet. By using this configuration, the voltage over the transistor (V_{CE}) is calculated as

$$V_{CE} = f(i_C(t), [control\ signal]) \tag{3.1}$$

where i_C is the transistor current and the control signal indicates the component state as seen in Table 3-4. There is no threshold voltage on the gate of the ideal transistor, instead the gate voltage is a pure control signal.

Table 3-4. Transistor state as a function of gate voltage.

Gate Voltage	Transistor State
> 0	ON
≤ 0	OFF

The ideal IGBT model does not include an anti-parallel diode so an ideal diode was chosen alongside the transistor, see Figure 3.4. This diode has similar characteristics as the IGBT where a forward voltage and bulk resistance is supplied and the resulting diode voltage is calculated in the same manner as (3.1) but without the dependence of the control signal.

The basic dynamic IGBT model takes the dynamics of the transistor voltage and current during switching into account. In addition to this, it also takes into consideration the thermal behavior of the transistor and includes an antiparallel diode. This device can be characterized using data available in the datasheet supplied by the manufacturer through the Characterize Device tool available in Ansys Simplorer. This model is useful when the switching energy and the switching times needs to be decided as it provides accurate voltage and current waveforms during turn on and off.

The Si-IGBT module used in the drivetrain is the Infineon FS600R07A2E3 from which the iv-characteristics has been implemented the simulation model. A similar SiC-MOSFET module can be found from Cree (CAS300M12BM2) which has similar current rating but can block

higher voltages. Table 3-5 shows a comparison of the general design parameters for both transistors.

Table 3-5. IGBT and MOSFET parameters.

IGBT Parameter	Value	MOSFET Parameter	Value
On state resistance	9.2 mΩ	On state resistance	4.2 mΩ
Collector-Emitter blocking voltage	650 V	Drain-Source blocking voltage	1200 V
Continuous collector current	600 A	Continuous drain current	423 A
Pulsed collector current	1200 A	Pulsed drain current	1500 A
Stray inductance	14 nH	Stray inductance	15 nH
Turn on time	170 ns	Turn on time	144 ns
Turn off time	470 ns	Turn off time	212 ns
Turn on energy	9 mJ	Turn on energy	5.8 mJ
Turn off energy	14 mJ	Turn off energy	6.1 mJ

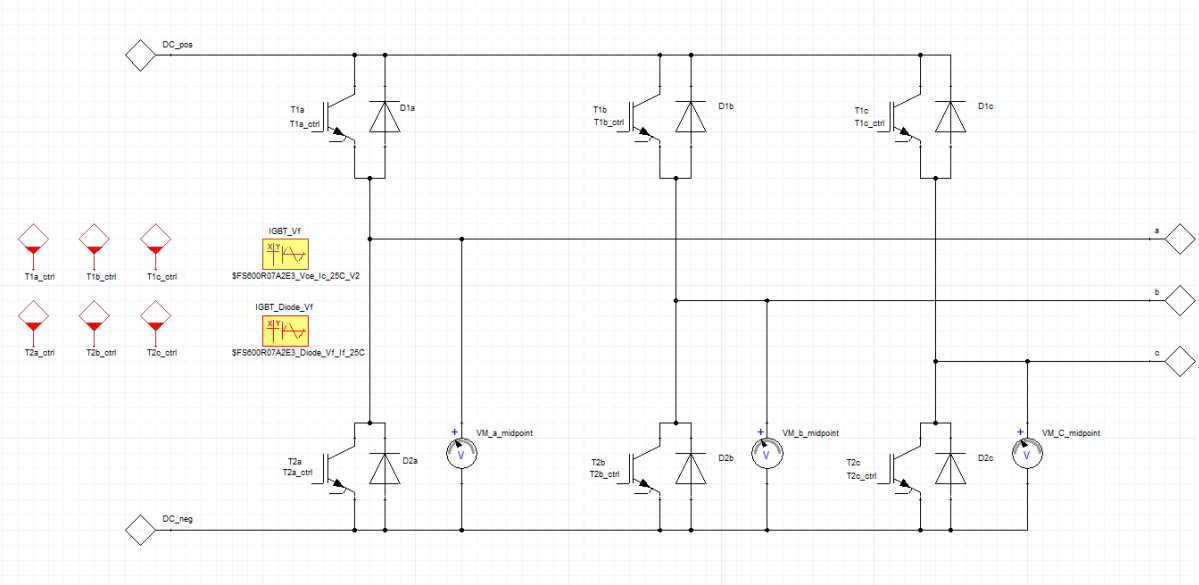

Figure 3.4. The initial inverter model containing no parasitic elements, only considering the iv-characteristics of the IGBTs and antiparallel diodes.

As mentioned earlier, this thesis is focused around modelling of the inverter and DC-link capacitor. Therefore, components such as the battery, the electrical machine and the cables have been simulated using less complex models and their parameters have been kept constant. The high-voltage battery has been modelled as described in Section 2.5 with a second order RC equivalent circuit and a series inductance L_S. The parameters of the battery are presented in Table 3-6.

Table 3-6. Simulation parameters for the high-voltage battery.

Parameter	Value
C1	10 pF
C2	10 pF
R1	96 mΩ
R2	96 mΩ
Rs	96 mΩ
Ls	100 nH
E1	350 V

The DC-cables were modelled by a simple series resistance of 10 mΩ and inductance with an approximated value of 500 nH. However, the AC-cables were modelled by a resistance of 1 mΩ as the inductance of the AC-cable can be considered negligible in comparison with the inductance of the electric machine. Finally, the PMSM was modelled by the built-in model synchronous machine permanent excitation without damper. The modelling of this component follows the equations given in Section 2.2 and Table 3-7 contains the parameters entered into the Ansys simulation model asides from the stator inductances L_d and L_q. Since the inductance is dependent on the saliency of the machine as well as saturation, it is determined by a look-up table derived from FEM-simulations of the electric machine.

Table 3-7. Simulation parameters for the Ansys PMSM model.

Parameter	Description	Value
J	Inertia	0.035 kgm^2
k_e	Rotor-flux constant	0.0471
Rs	Series resistance	13.3 mΩ
p	Number of pole-pairs	4

3.3 Base Verification

A validation of the simulation method and control system was performed to evaluate the performance of the initial simulation model since it is the foundation of the thesis. Figure 3.5 compares the theoretical inverter current described in Section 2.8.1 with simulation results from the ideal simulation model. By comparing the current into the inverter for both the theoretical calculations and simulations, the harmonic content introduced by the PWM switching can be verified.

The operating point chosen for the simulation was given by a torque reference of 20 Nm with a machine speed of 3000 rpm which results in an output electric fundamental frequency of 200 Hz. The amplitude modulation ratio during this simulation was measured to 0.44 and the resulting inverter current can be seen on the right-hand side of Figure 3.5. By using the same amplitude modulation ratio (m_a) and output frequency in (2.13) the current seen on the left-hand side of Figure 3.5 can be generated. For both the simulation and the theoretical calculations, the switching frequency was set to 10 kHz. In Figure 3.5 it can be seen that that there are some differences in shape between the simulated and calculated inverter current. Several things could be contributing to these differences; The theoretical equation could contain errors. Additionally, the implementation of the theoretical equation could, through assumptions and simplifications made during the derivation, be missing certain terms. In addition to this, the

operating point might differ slightly between the calculations and simulations, causing differences in the resulting current shape.

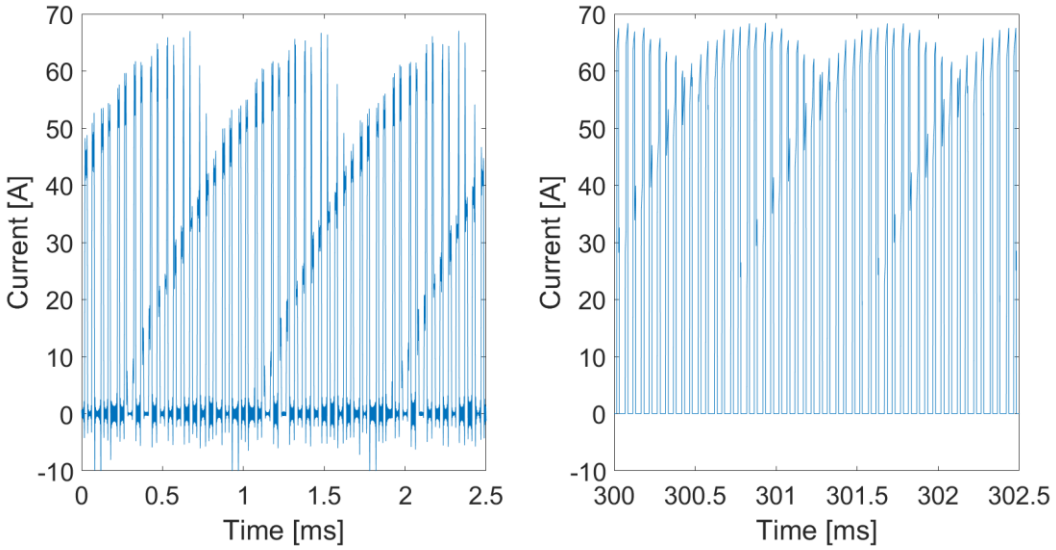

Figure 3.5. Inverter current for both theoretical calculations (Left) as well as simulations (Right).

By performing an FFT-analysis on the resulting inverter currents of the two cases, Figure 3.6 can be generated. It can be verified that the ripple is present at all the same frequencies for both simulations and theoretical solution. Even though the relative sizes of each contained in both simulations and theoretical solutions are the same, there is a big difference in magnitude, see Figure 3.7 for a zoom of the 20 kHz and 50 kHz ripple components.

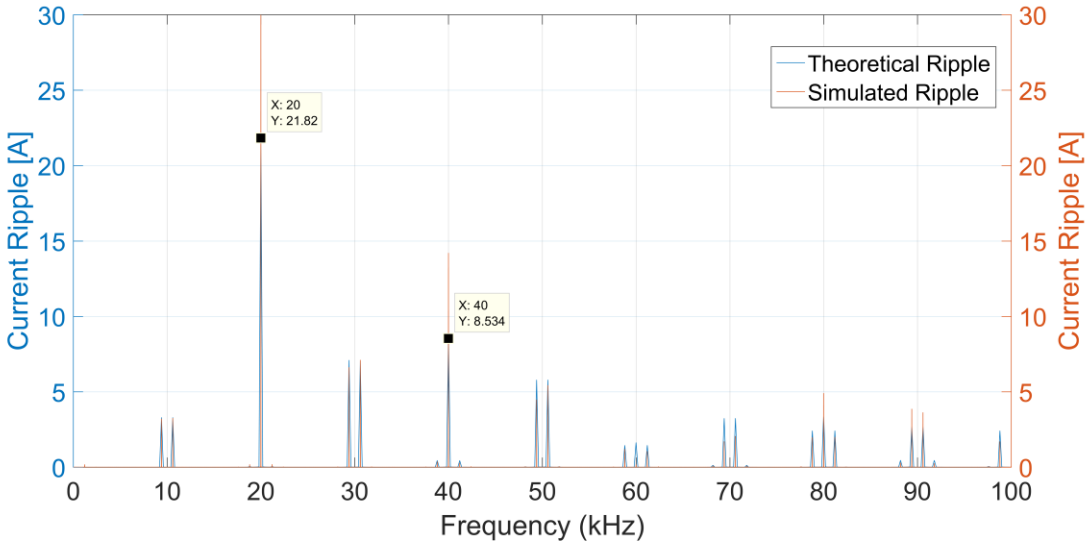

Figure 3.6. FFT of the inverter current for theoretical solution and simulations, markers indicate ripple amplitude of theoretical calculations at 20 and 40 kHz.

If Figure 3.6 and Figure 3.7 are analyzed, it can be seen that the simulated ripple has a significantly higher amplitude at the 20 and 40 kHz component where the biggest deviations can be seen. This probably stems from a parameter mismatch between the simulations and calculations. Most likely the output current amplitude was higher during the simulations, and thus resulted in higher 20 and 40 kHz ripple components. The amplitude modulation ratio,

switching frequency and output frequency was however identical and thus the distribution of current ripple in the frequency domain became similar in the two cases.

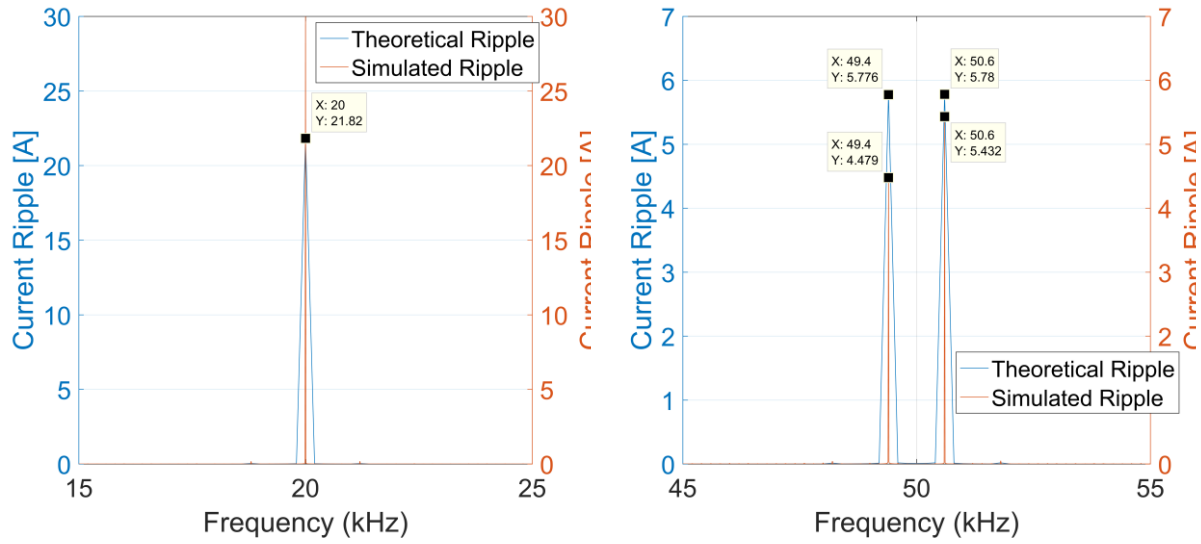

Figure 3.7. Zoom in at 20 kHz (left) and zoom in at 50 kHz (right).

3.4 Measurements on actual inverter

A complete drivetrain-rig was available at Chalmers which made it possible to compare the results generated by the simulation model with measurements of an existing drivetrain. To simulate different load conditions, a DC-machine was used to brake the PMSM which is connected via the differential transmission used in the actual vehicle. This transmission has a gear ratio of 10:1 which means that 10 rpm on the PMSM corresponds to 1 rpm on the braking DC-machine. However, the right drive-shaft was locked in place leaving only the left shaft free to rotate which reduces the effective gear ratio to 5:1. The PMSM is operated by the three-phase inverter powered by the high-voltage battery while the DC-machine is operated by a converter connected directly to the grid, see Figure 3.8.

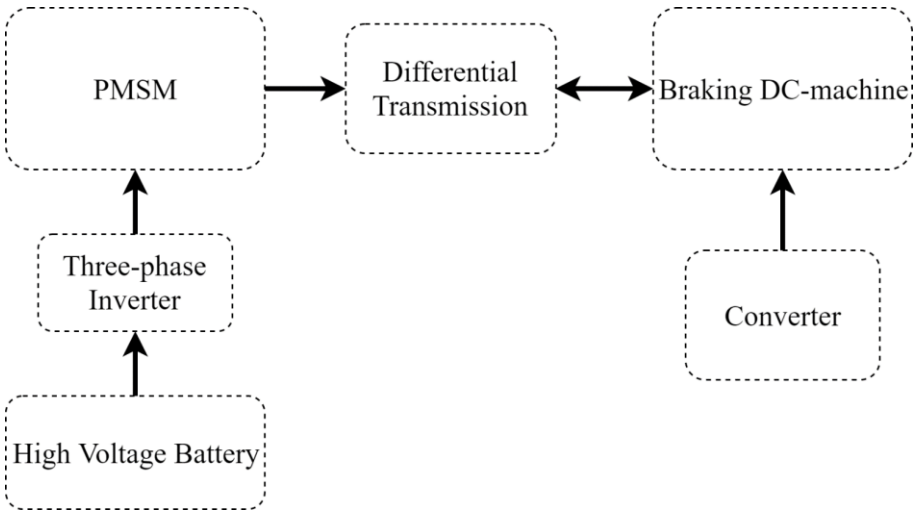

Figure 3.8. Block diagram of the drivetrain-rig at Chalmers.

For all measurements performed on this drivetrain rig, the operating point given by a certain torque and speed reference has been reached by controlling the braking DC-machine with a fixed speed while applying a constant torque from the PMSM. All communication and control of the PMSM and the three-phase inverter was conducted via an existing CAN-bus interface.

The DC-link voltages and currents were measured alongside the output current and the line-line voltage. As the DC-cable connecting the high-voltage battery and three-phase inverter is shielded, a break-out-box was used to access the two conductors. Rogowski coils were used on both the positive and the negative conductor to measure the DC-link current and a differential voltage-probe was connected between the two conductors to measure DC-link voltage. The output AC-currents were measured with Rogowski coils attached to the cables running from the inverter to the PMSM, in addition to this differential voltage probes connected to the machine terminals measured output line-line voltages. Table 3-8 includes the measurement equipment used for measuring these AC and DC quantities. As seen in Figure 3.9 the DC-link voltage and current was measured on the high voltage battery side while the AC-quantities was measured on the machine side. Photographs of the drivetrain-rig and measurement locations can be found in Appendix B.

Table 3-8. Measurement equipment used during drivetrain rig measurements.

Measurement	Instrument
DC-link voltage	Teledyne LeCroy ADP305
DC-link current (positive)	PEM CWT 1B Ultra Mini Rogowski Coil
DC-link current (negative)	PEM CWT 6B Ultra Mini Rogowski Coil
Machine line-line voltage	Teledyne LeCroy HVD3106
Machine line current	PEM CWT 3R Rogowski Coil

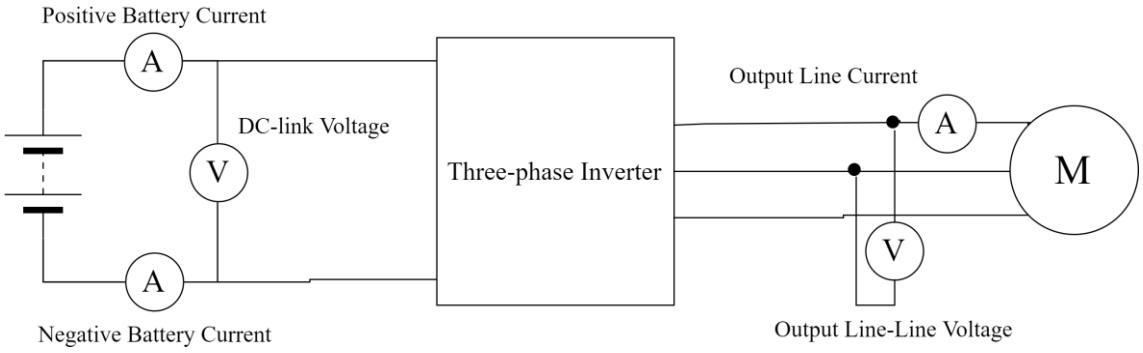

Figure 3.9. Measurements taken at drivetrain rig at Chalmers.

4 Evaluation/Analysis

4.1 Transistor modelling

The first area of focus was to determine how to model the transistors throughout the thesis since this determines the minimum time-step during simulation. Several alternatives are available but the two techniques evaluated here are the ideal IGBT model and the basic dynamic IGBT as described in Section 3.2.

4.1.1 Ideal Transistor Models

As discussed in Section 2.8.1, the ripple emitted to the DC-link by a three-phase inverter using PWM switching is in theory mainly dependent on parameters such as amplitude modulation ratio, output current magnitude and switching frequency rather than the actual transistors used within the inverter. To simplify the construction and control of the inverter, studies were initially performed using more ideal IGBT:s modeled in Ansys as described in Section 3.2. These models act as a switch, turning on when the gate signal goes above 0, and turns off at a gate signal of 0 or lower. In addition to an ideal switching behavior, this transistor model includes the iv-characteristics of the IGBT. This is the relationship between the collector current and the collector-emitter voltage which is traced from the datasheet.

The initial simulation results for a steady state operating point of 3000 rpm and 20 Nm, results in the DC-link current and voltage waveform presented in Figure 4.1 by using a minimum simulation time-step of 10 ns. Stray inductance in the DC-link cables were present during these simulations (see Section 3.2) as well as an arbitrary value of ESR and ESL to represent the presence of non-idealities in the DC-link capacitor. If the DC-link voltage in the left of Figure 4.1 is analyzed it can be seen that large voltage overshoots occur at the switching on each IGBT. Figure 4.2 depicts the same DC-link voltage but zoomed along the y-axis to visualize the actual voltage ripple which has an amplitude of about 0.7 V.

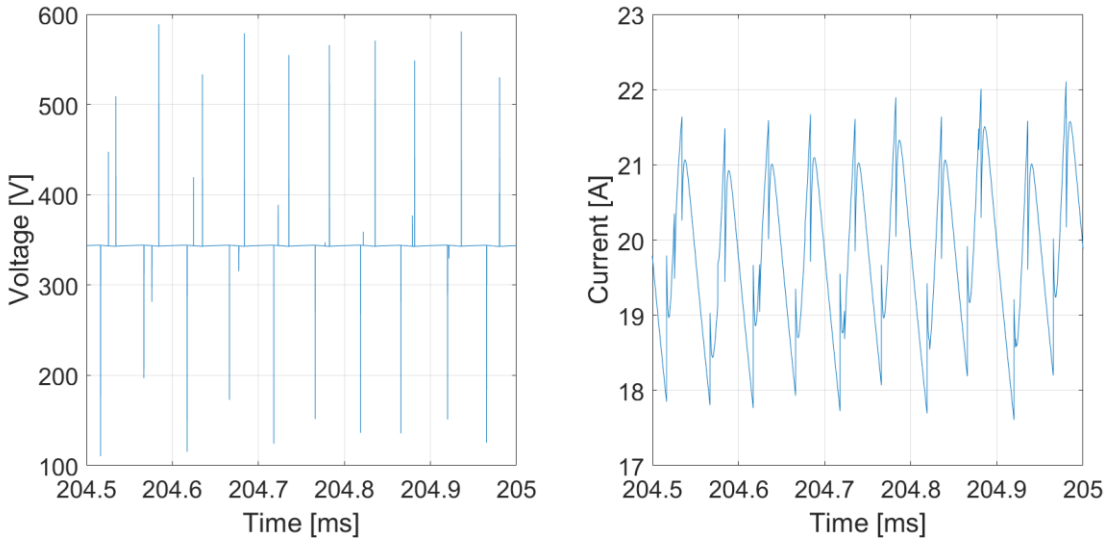

Figure 4.1. Simulated DC-link voltage (left) and current (right) waveforms.

These voltage transients are the result of the ideal transistors going from fully blocking to fully conducting current during one simulation time step. This causes a very high current derivative on the DC-link which in turn causes a large overshoot due to the inductances present in the DC-cables, battery model and the DC-link capacitor. The value of these transients should not be considered as accurate, since they are an artefact of a non-realistic switching event and their amplitude is dependent on the minimum time-step of the simulation.

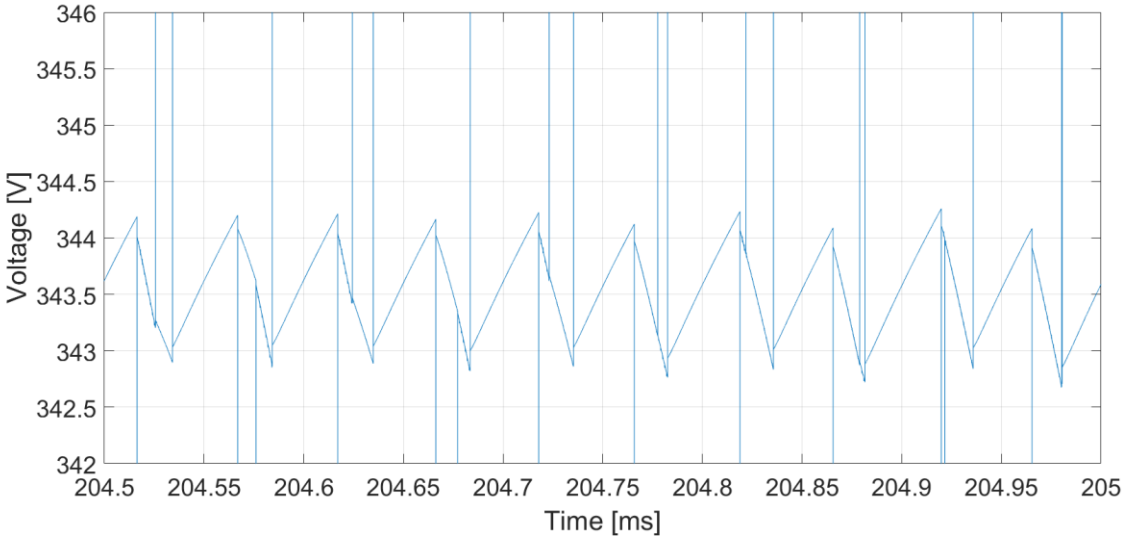

Figure 4.2. Simulated DC-link voltage zoomed along y-axis.

To further analyze the influence of these voltage transients the current into the inverter is plotted in Figure 4.3 where the left graph shows the current during the entire simulation interval and the right graph depicts a zoom along the x-axis to illustrate the high current derivatives. As expected, the rise and fall time of the current becomes equivalent to the minimum simulation time-step.

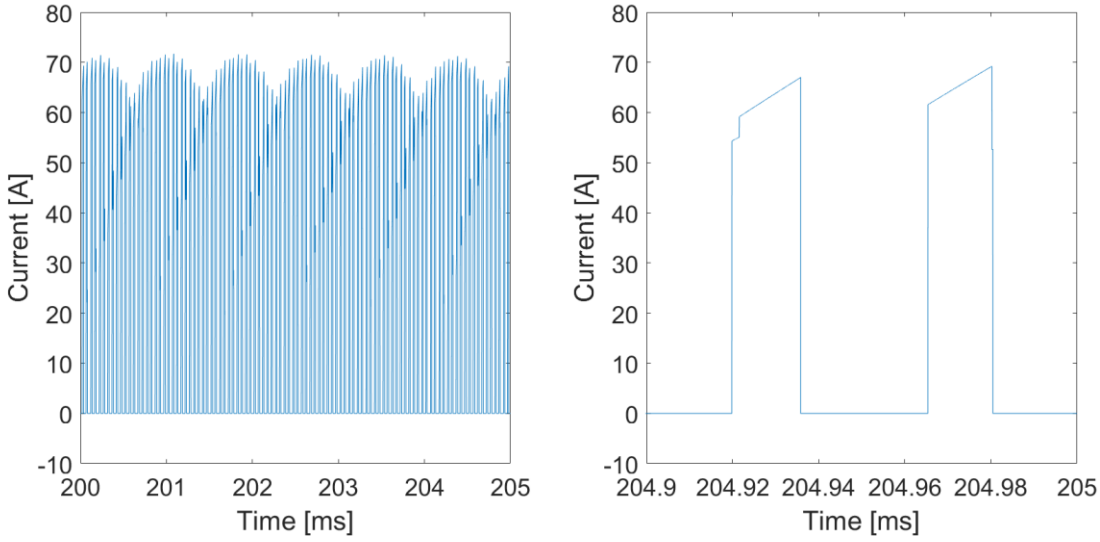

Figure 4.3. Simulated inverter current, during entire simulation (left) and zoom along x-axis (right).

A frequency analysis of the DC-link current and voltage can be seen in Figure 4.4 where a FFT is shown of the voltage (left) and current (right) up to 200 kHz excluding the DC-component. By analysis of these FFT-plots it can be seen that the frequency content of the current resembles the frequency content seen in the theoretical calculations in Section 2.8.1, i.e. the frequency content has a similar distribution to what has been seen before.

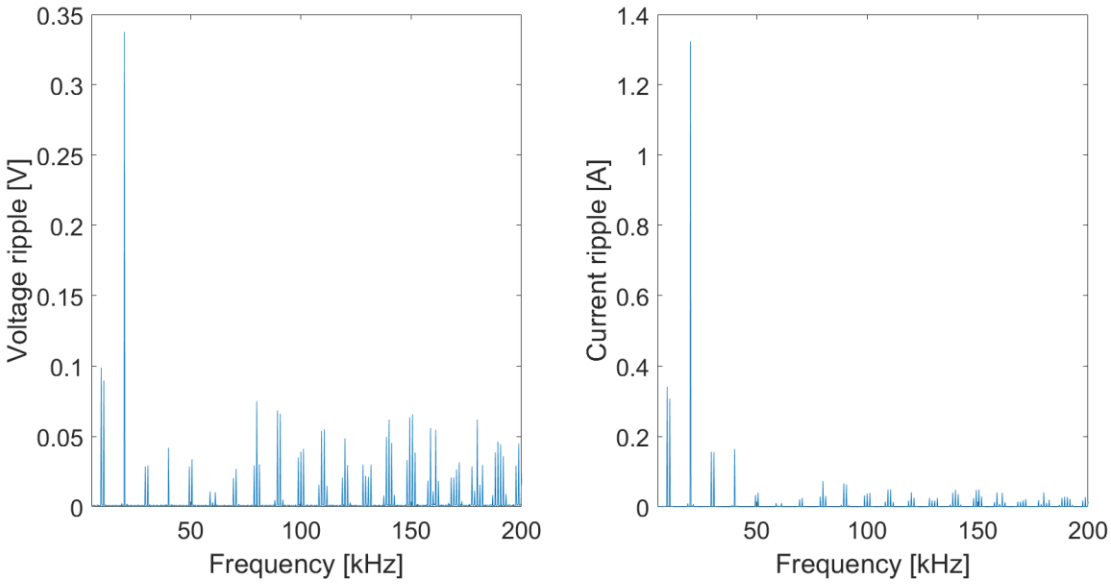

Figure 4.4. FFT of DC-link voltage (left) and current (right).

A problem with performing FFT analysis of the DC-link voltage seen in Figure 4.1 is the fact that the voltage overshoots only contain one simulation time step; the voltage reaches its maximum value in one time step and then falls back down during the next time step. This is not ideal for the FFT-analysis as the transients only contain one sample point. In theory, the transients should contain mostly high frequency components, but low sampling rate causes the transients to bleed into a lower frequency spectrum. Decreasing the minimum simulation time-step is not an adequate solution as this only increases the speed at which the transistors turn on and off and thus also increases the speed and magnitude of the voltage transients.

The typical way to decrease the transients that occur during switching of the transistors is to place an RC-snubber in parallel with the transistors. As the losses during switching was not of immediate importance during the initial simulations, RC-snubbers were placed in parallel with all transistors as seen in Figure 4.5. The idea of these RC-snubbers is that they will limit the rate of change of the voltage over the transistors and thus ensure that switching cannot be done during one time step.

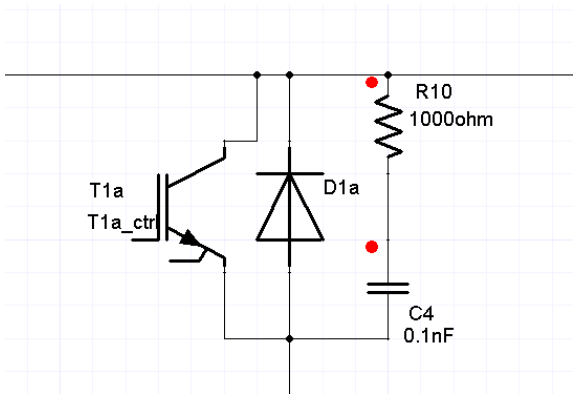

Figure 4.5. Transistor with RC-snubber mounted in paralell.

Simulations were performed using the capacitance and resistance values seen in Figure 4.5, which results in a time constant of 100 ns, which roughly corresponds to the turn on/off times of the real transistors used. The resulting DC-link voltage, with and without a snubber circuit, can be seen in Figure 4.6. It can be seen that the transients on the DC-link voltage are not noticeably affected by the introduction of the RC-snubbers. This can further be seen in Figure 4.7 where the inverter current after the introduction of the RC-snubbers is visualized, and can be seen to have the same rise and fall time as seen in Figure 4.3. Simulations were performed for several other values of resistance and capacitance with both the same and different time-constant with no effect on the turn on and off transients. To understand why the RC-snubbers did not affect the switching times as expected, the ideal transistor model in Section 3.2 is analyzed. As mentioned, the voltage across the transistor is a function of the current through the transistor itself and not the other way around. This means that as soon as the transistor gets a turn on-signal, it immediately closes and allows the full current to flow through the transistor in one time-step.

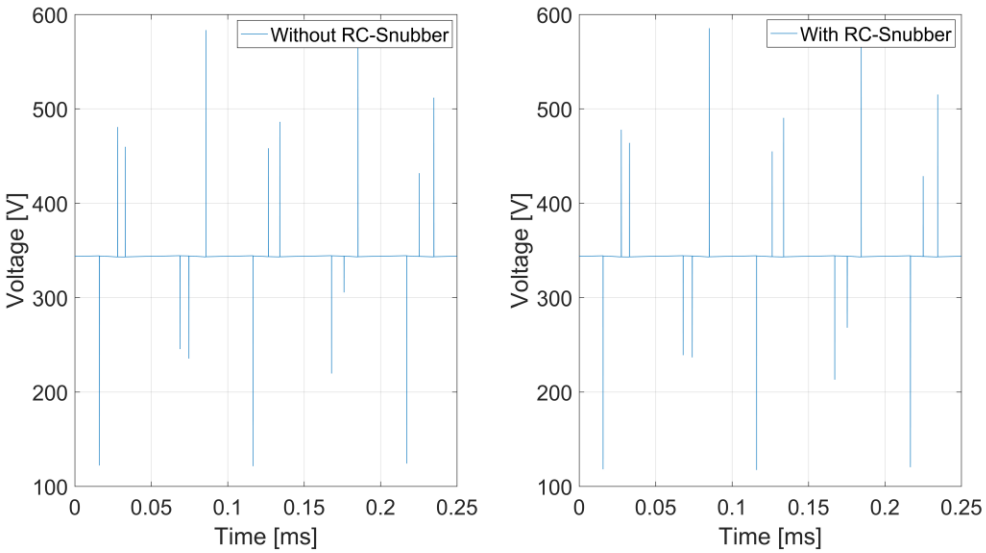

Figure 4.6. DC-link voltage with (right) and without (left) an RC-snubber in parallel with the transistors.

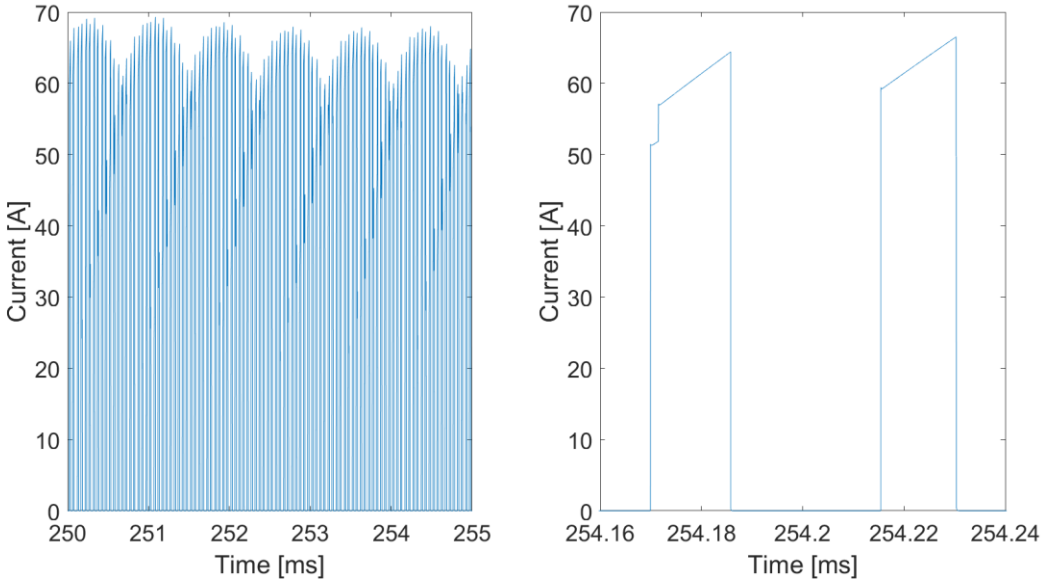

Figure 4.7. Inverter current using RC-snubbers, right plot shows a zoom along the x-axis.

Another method to artificially slow the switching speed of the transistors is to import the inverter current from the simulations into MATLAB and process it to remove the high derivatives. The MATLAB-script in Appendix C was created to find these instances of high current derivate and replace them with a specified rise and fall time instead of the 10 ns that stems from the simulation time step. This enables replacing the entire inverter/machine part of the simulation model with a current source where the modified inverter current can be used as an input to generate an inverter current with more realistic current derivatives. In addition to this, the possibility to simulate with smaller time step without changing the switching times and thus gaining more data-points during each voltage spike is also gained. This results in a better FFT analysis and the result of this ramping of the inverter current can be seen in Figure 4.8 where a zoom along the x-axis around one switching instance is shown. In this case the current turn-off has been changed from 10 ns to 100 ns.

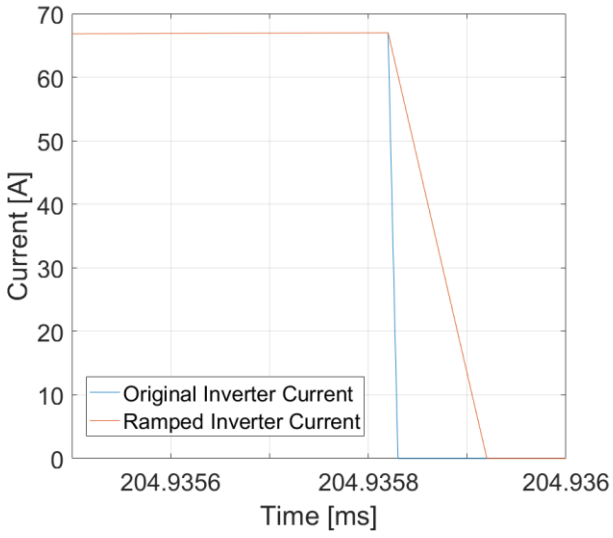

Figure 4.8. Zoom along the x-axis of inverter current before and after slowing down fall and rise times.

To ensure that this change in the inverter current does not influence the resulting ripple components, an FFT analysis of the inverter current before and after the ramping was performed, see Figure 4.9. The left plot of Figure 4.9 shows the frequency spectrum up to 200 kHz excluding the DC-component while the right plot shows the frequency content between 0.5 MHz and 10 MHz. As seen from the analysis, the ramping of the inverter current did not affect the frequency content noticeable at all in the lower frequency spectrum but had an effect in the MHz-range. This is natural as time periods of 10 ns and 100 ns correspond to frequencies of 100 MHz and 10 MHz, respectively. To simulate the resulting DC-link ripple with a modified inverter current, a current source was used to replace the inverter and electrical machine, see Figure 4.10.

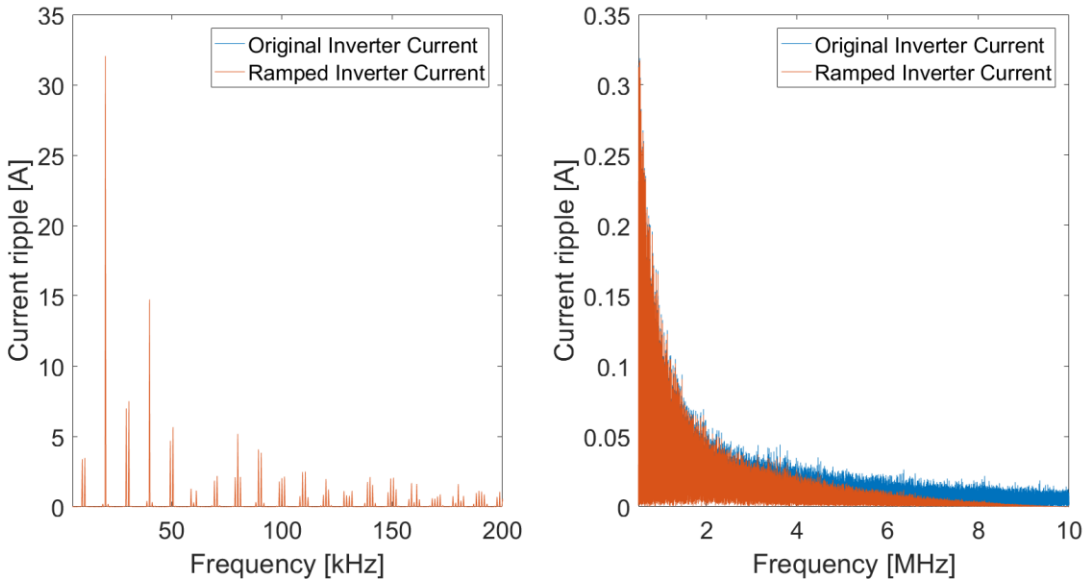

Figure 4.9. Frequency analysis of inverter current, both original and modified. Left plot shows frequencies up to 200 kHz while the right plot depicts the 0.5 to 10 MHz range.

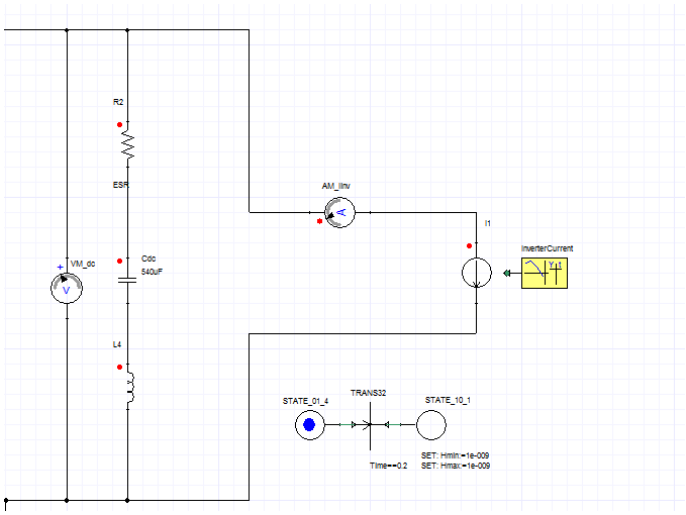

Figure 4.10. Current source replacing inverter and electrical machine during DC-link ripple analysis.

By implementing this current source model, the DC-link voltage wave-forms seen in Figure 4.11 were obtained. Figure 4.11 depicts the original DC-link voltage waveform (left), the DC-link voltage waveform obtained when using the current source model with the original inverter current (middle) and the voltage waveform obtained when using the current source model along with the ramped inverter current (right). By analyzing the waveforms in Figure 4.11 it can be seen that the voltage did not change from the left to the middle plot. This indicates that using a current source to simulate the actual inverter and machine works well and produces the correct voltage waveforms and therefore also the correct voltage ripple. From the right-hand plot, it can be seen that the voltage transients became lower than in the previous simulations as a result of the lower current derivative. In addition to this, it can also be seen that the voltage transients now contain several data-points and can therefore be better analyzed by the FFT algorithm.

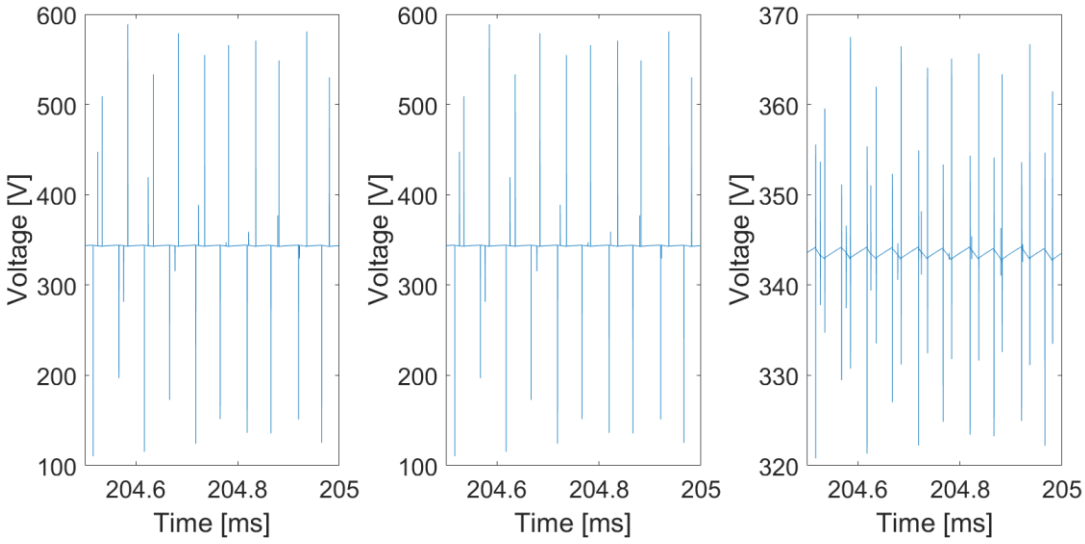

Figure 4.11. DC-link voltage waveforms for standard simulation (left), current source model without ramping inverter current (middle) and current source model with 100 ns ramped current (right).

An FFT analysis of the obtained voltage waveform and comparison to the original DC-link voltage was done in Figure 4.12. By analyzing the frequency content using a ramped inverter current from a current source, it can be seen that the frequency amplitudes were changed slightly. The harmonics are still found in the same frequencies as expected from Section 2.8.1. In particular frequencies above 50 kHz were affected where the ripple amplitude was found to be approximately 50 % lower than the original DC-link voltage.

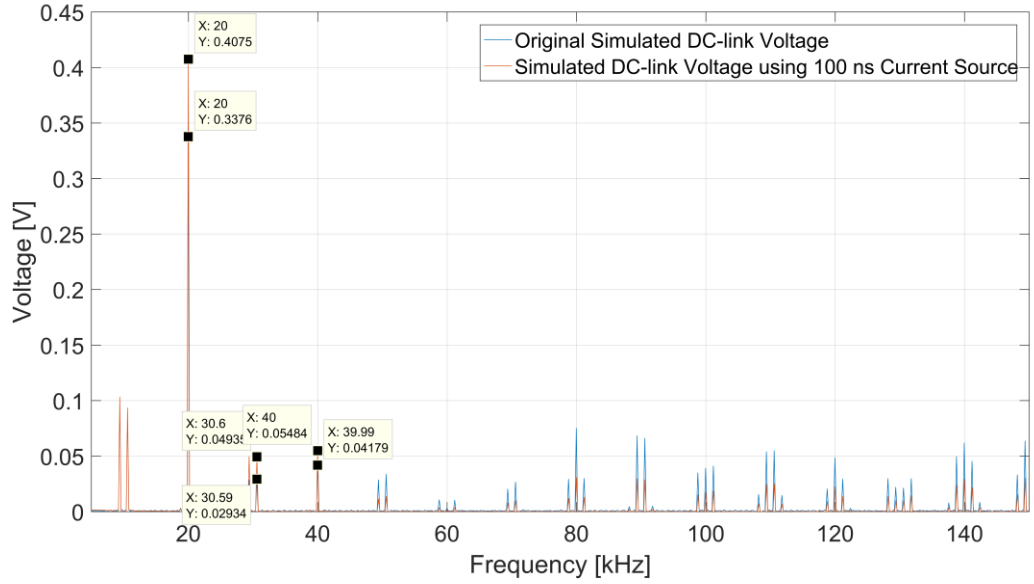

Figure 4.12. Frequency analysis of the DC-link voltage before and after ramping inverter current and implementing current source model.

As a final way to evaluate the influence of the voltage transients seen, a MATLAB-script was created to remove the transient spikes entirely by identifying areas of high derivatives and replacing them with a straight line from the value before the transient to the value after the spike, see Appendix D. The resulting DC-link voltage from the simulations can be seen in Figure 4.13, where the simulated DC-link voltage without transients are compared to the original voltage. As can be seen the two voltages are identical except from the removed transients.

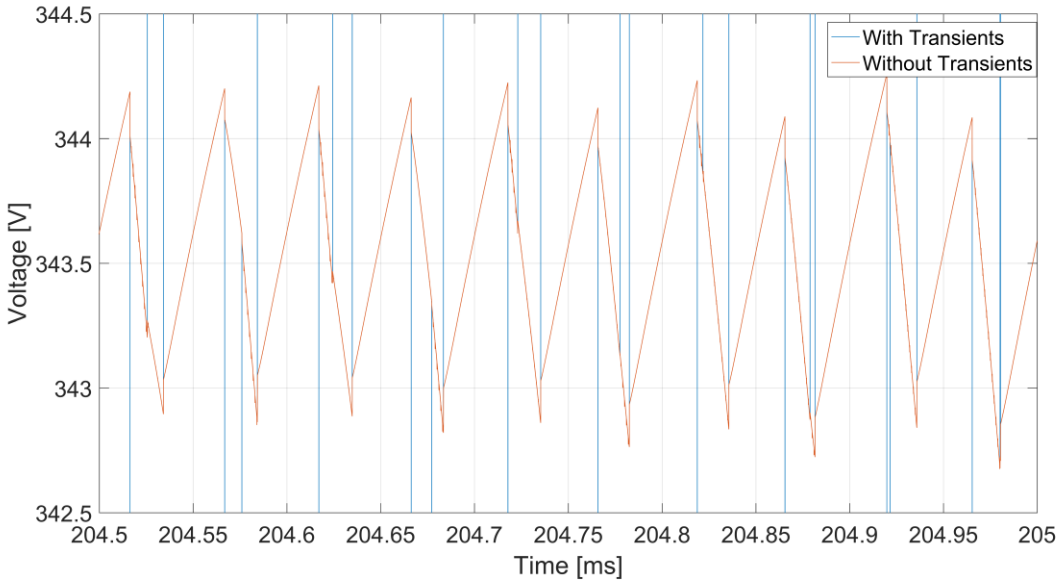

Figure 4.13. Simulated DC-link voltage with switching transients removed.

The resulting FFT analysis of the DC-link voltage before and after removing the transients can be seen in Figure 4.14. It can be seen that removing the spikes show a similar behavior for

higher frequencies (>50 kHz) as what was observed when ramping the inverter current, where the ripple components are suppressed even further. However, for the 20, 30 and 40 kHz components something unexpected happened, where the frequency content increased when the transients where removed.

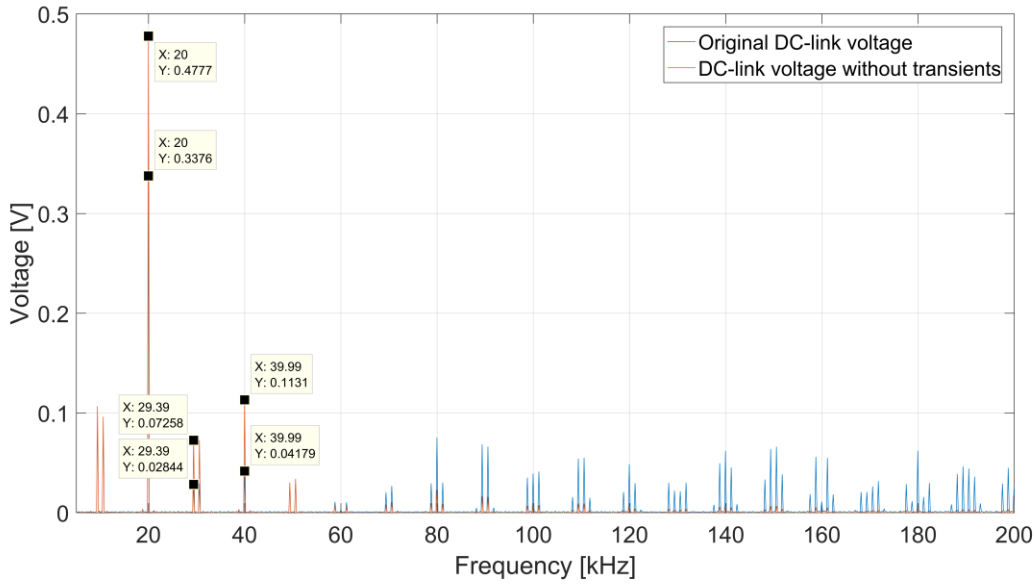

Figure 4.14. FFT of DC-link voltage before and after removing switching transients.

To investigate why the fundamental frequency component was increased when removing the transients, a FFT analysis was performed on the transients alone. This data was extracted through subtracting the DC-link voltage without transients from the original DC-link voltage as seen in Figure 4.15 and Figure 4.16.

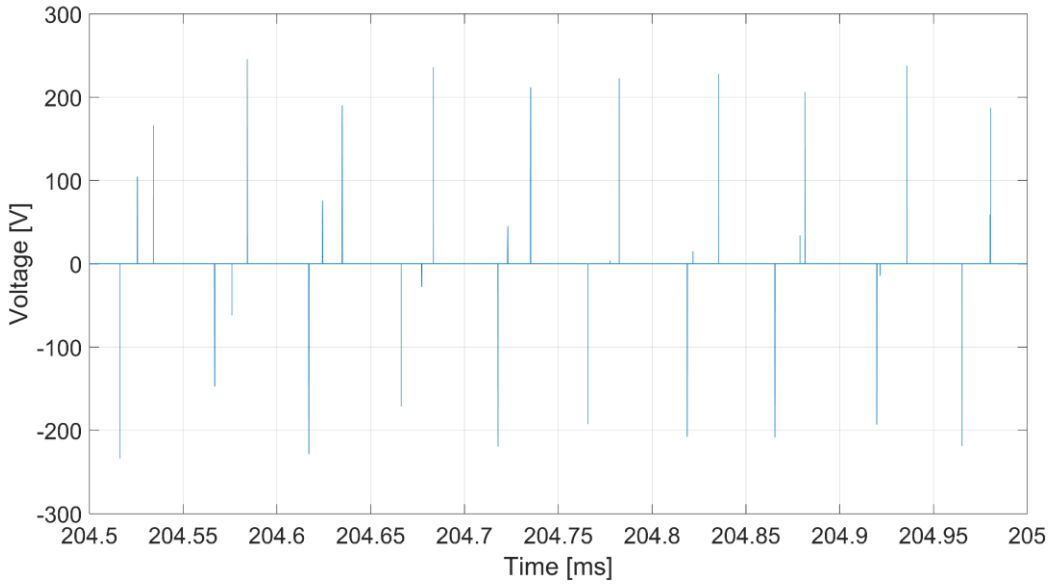

Figure 4.15. Simulated DC-link voltage transients isolated.

The FFT analysis indicates that the transients contain a fundamental 20 kHz component. To see why the transients decrease the fundamental frequency component, the 20 kHz component of

both the original DC-link voltage and the transients are plotted in Figure 4.17. Here it can be seen that they are phase-shifted with approximately 180º which explains why the transients suppress the lower frequency components of the DC-link voltage.

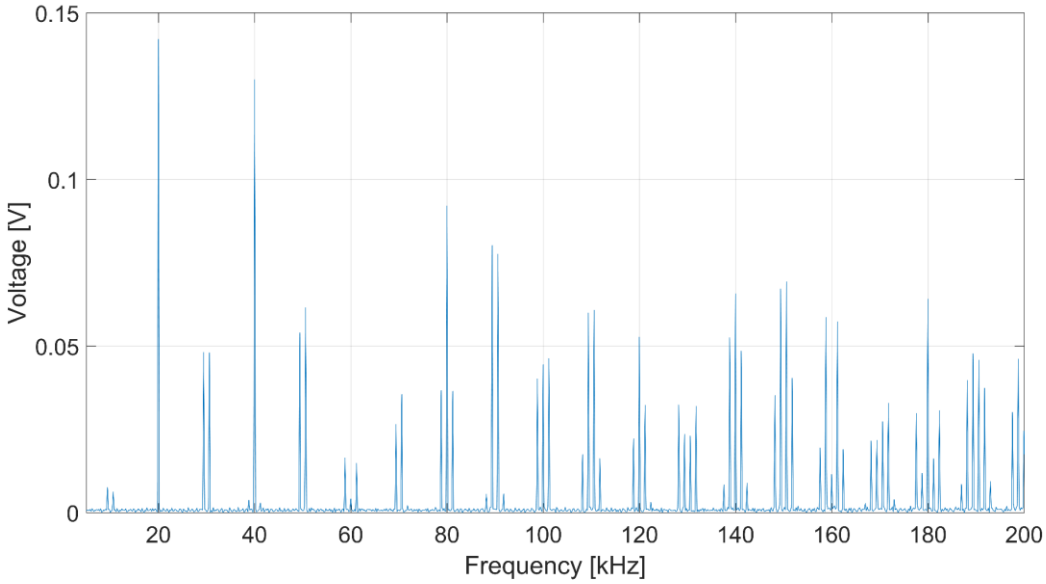

Figure 4.16. FFT of simulated DC-link voltage transients.

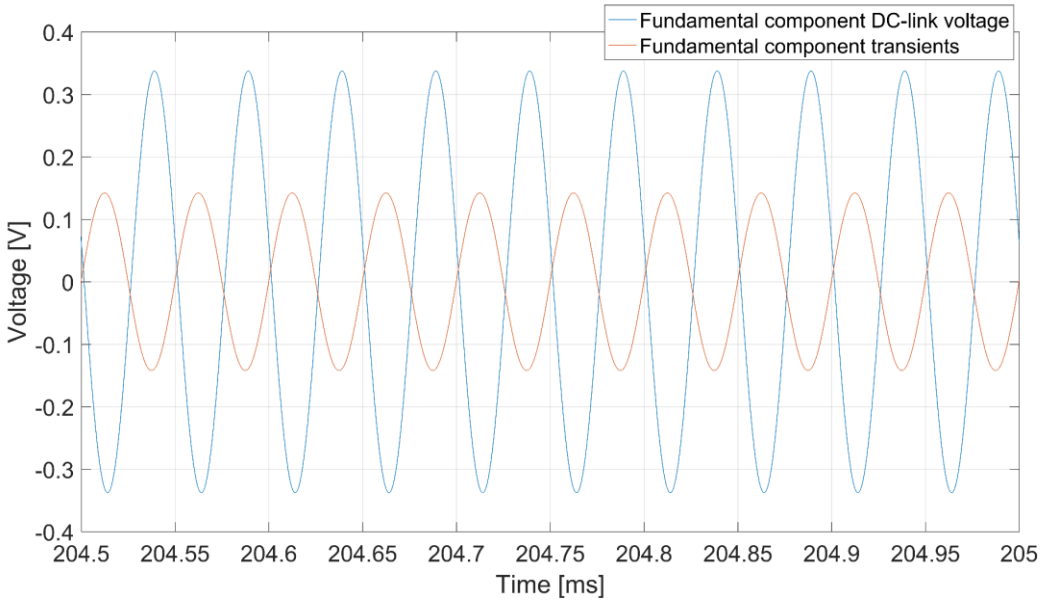

Figure 4.17. Fundamental components of simulated DC-link voltage as well as switching transients

4.1.2 Basic Dynamic Transistor modelling

As mentioned in Section 3.2, more advanced transistor models are available in Ansys Simplorer. In order to evaluate the impact of using a transistor model that takes the dynamics of the switching into account, two basic dynamic transistor models were created in Ansys. One was modelled after the Infineon IGBT in the actual inverter and the other after the CREE SiC-MOSFET equivalent. Both were implemented via the Simplorer device characterization wizard

based on the data and curves available in their respective datasheets to model their dynamic behaviors. Some of these parameters are seen Table 3-5. The inverter model can be seen in Figure 4.18 where a total stray inductance of 22 nH has been implemented into each phase leg to better simulate the real inverter. To drive the transistors a simple gate-drive block was implemented, which provides the ± 15 V gate voltage specified in the datasheet through a 2.5 Ω gate-resistance.

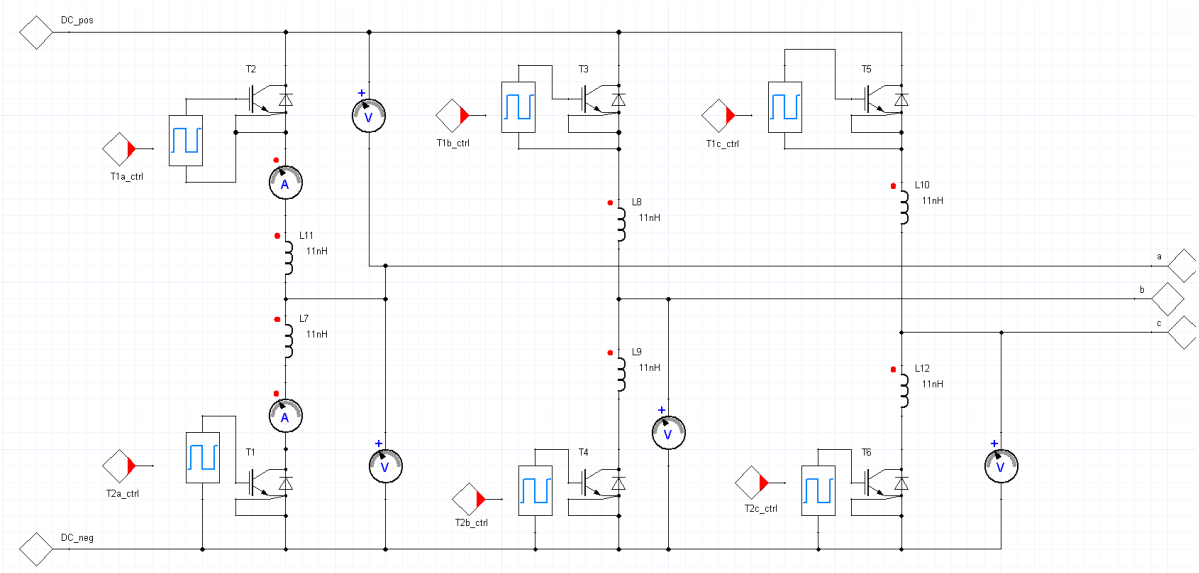

Figure 4.18. Inverter model containing the dynamic IGBTs and a 22 nH stray inductance.

By performing a simulation of the same operating point as for the ideal transistors, the switching waveforms for the IGBTs can be seen in Figure 4.19. In comparison with the switching waveforms obtained with ideal transistors, a distinct difference can be seen in both rise and fall-time but also a current overshoot during turn on.

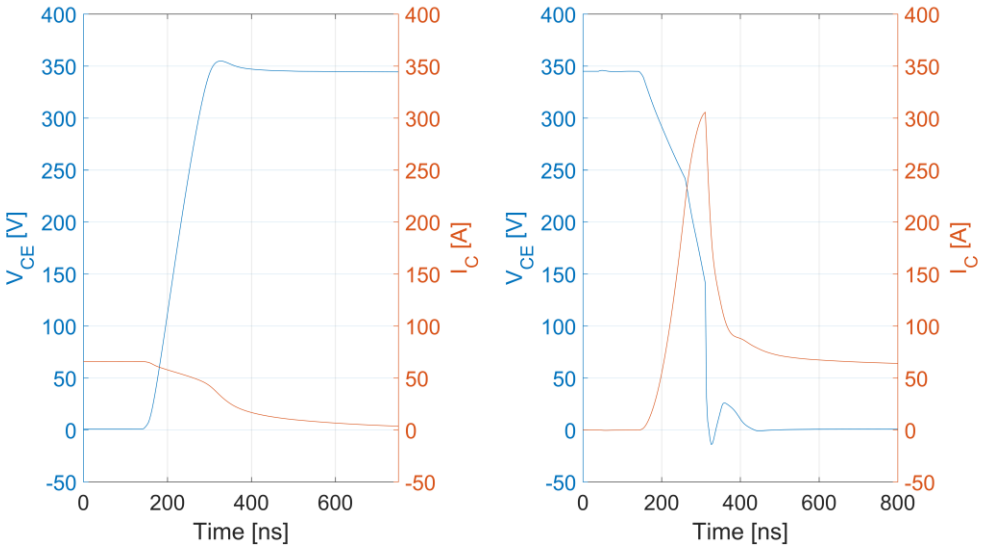

Figure 4.19. Collector-emitter voltage and collector current for turn OFF (left) and turn ON (right) using the basic dynamic IGBT-model.

One reason behind the current over-shoot, since increasing dead-time did not improve the situation, would be the reverse recovery current of a diode in the same phase leg. Even though the transistor and body-diode of the IGBTs are incorporated into one module the diode current is accessible in Simplorer. The same turn-on sequence as shown previously is seen again in Figure 4.20, but with the addition of the current through the body diode that is located in the second transistor of the phase-leg. The polarity of the diode current has been reversed to give the reverse recovery current the same sign as the transistor current. It can be seen that the shape of the reverse recovery current resembles the transistor current overshoot and they are completely in phase. Due to this, the reverse recovery of the transistor body-diodes is most likely the cause of the current overshoots seen during turn-on.

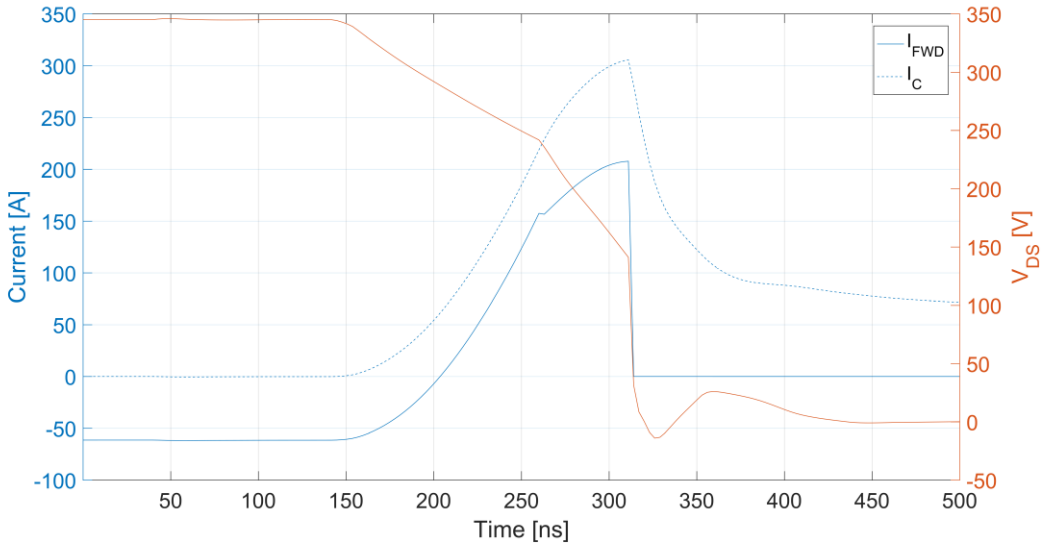

Figure 4.20. Simulated transistor voltage and current during turn-on along with body diode in opposite transistor.

The results of the increased switching times and current overshoot can be seen in the inverter current in Figure 4.21. As seen in comparison with the inverter current using ideal transistors, the same basic undelaying inverter current exists but with large current spikes during switching.

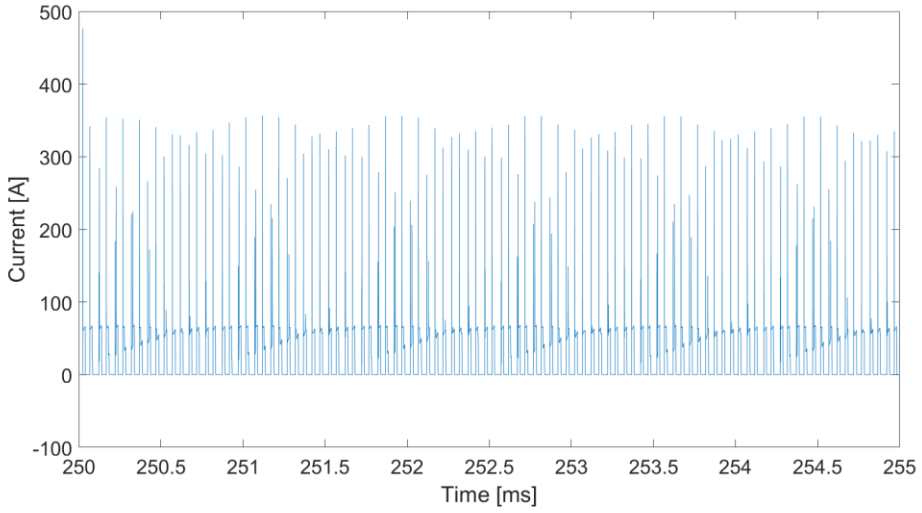

Figure 4.21. Simulated inverter DC-link current using the basic dynamic transistor-model.

The FFT of the DC-link current in Figure 4.22 shows that the frequency components of the ideal and dynamic transistor models follow each other closely within the 0-200 kHz range except for a few distinct frequencies highlighted in Table 4-1. Higher frequency components are affected to a greater extent than lower frequencies by the change between ideal and dynamic transistors. The exceptions to this are the frequency components at 60 and 100 kHz. At 60 kHz, the dynamic IGBTs cause a frequency component not present in the original inverter current, something that was unexpected as this is a multiple of 3 of the switching frequency and should thus be eliminated by the three-phase symmetry if the system. At 100 kHz the content is decreased when switching to the basic dynamic transistor model.

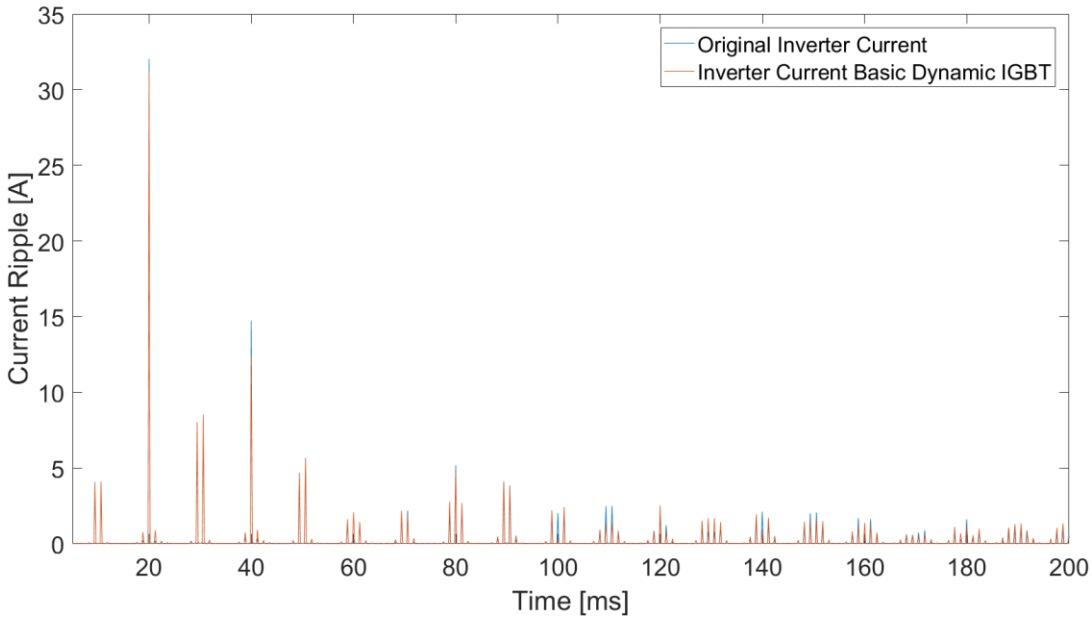

Figure 4.22. FFT-analysis of the inverter current using the basic dynamic transistor-model.

Table 4-1.Current ripple amplitude using ideal and basic dynamic IGBTs.

	Current Ripple Amplitude	
Frequency [kHz]	**Ideal IGBT**	**Basic Dynamic IGBT**
40	14.73 A	12.39 A
60	0.2983 A	2.053 A
100	2.019 A	0.3266 A
109.4/110.6	2.462 A	1.376 A
140	2.109 A	0.9655 A
149.4/150.6	2.059 A	1.608 A
179.4/180.6	1.606 A	1.186 A

Introducing dynamic transistors had an impact on the resulting DC-link ripple but it also increased the complexity of the simulation model and the simulation times. To justify the added complexity, the transient behavior of these simulation models needs to be thoroughly validated. Due to the large number of degrees of freedom and tuning variables, much time would have had to be spent to validate the switching. Due to lack of time and not having access to actual

switching waveforms from the real inverter it was deemed too complicated to try and address the problems seen using the dynamic transistor model, including investigating the reverse recovery current of the body diode.

Since no adequate way was found to model the transient that stem from the transistor it was decided to not put emphasis on the frequency content added by the switching. This means that most of the analyses done in this thesis was performed by using the ideal IGBTs and by removing the voltage transients. The use of the basic dynamic transistors was deemed unnecessary as they contribute to a much longer simulation time while producing a transient switching behavior that could not be verified. Removing the voltage transients will produce a frequency analysis of the underlying fundamental ripple components but it will not include the influence of the switching behavior.

4.2 DC-Link Capacitor

The impedance of the DC-link capacitor was measured from 10 Hz to 40 MHz, see Figure 4.23 and Figure 4.24. The first thing that can be noted is that the resonance between the capacitor and inherent stray inductance occurs at approximately 53 kHz. The impedance of the capacitor reaches a minimum and the phase angle changes from -90º to +90º when the impedance changes from capacitive to inductive. The differences in measured impedance seen between the three terminals is a result of the accuracy of the Bode 100 at low impedances, as seen in Table 3-3, as well as the fact that the DC-link capacitors internal structure could cause slightly different impedances to be seen from different terminals.

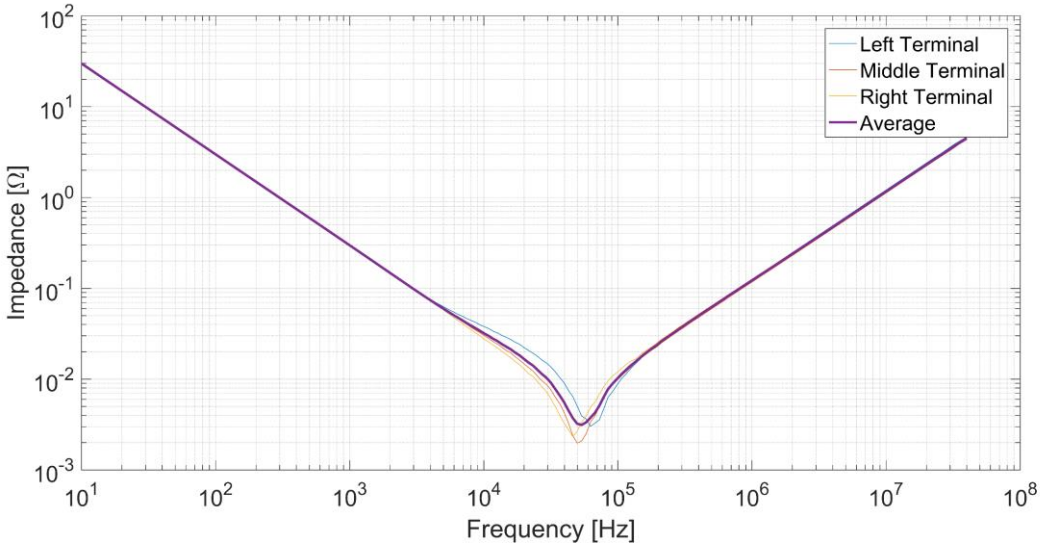

Figure 4.23. Absolute value of the measured capacitor impedance magnitude.

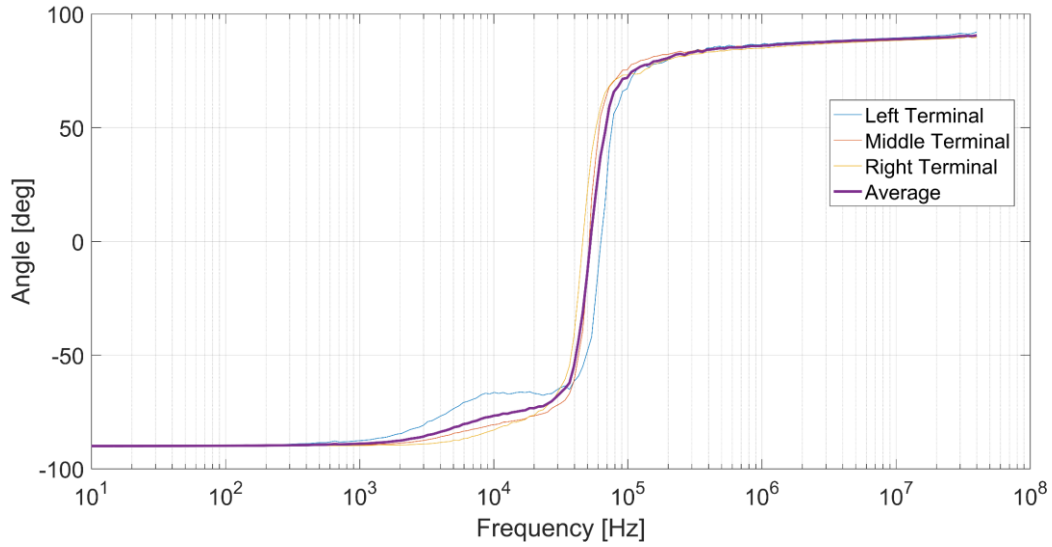

Figure 4.24. Measured phase of the capacitor impedance.

By using the model in Figure 2.9, the total impedance can be described as

$$Z_{TOT} = R_{ESR} + j\omega L_{ESL} + \frac{1}{j\omega C} \tag{4.1}$$

where ω is the angular frequency. This means that the real part of the measured impedance should correspond to the series resistance of the capacitor, see Figure 4.25. It can be seen that the real part of the impedance measured over the capacitor terminals was not constant. Since the DC-link capacitor has very low ESR, it is difficult for the Bode 100 to measure it accurately. To obtain the most accurate value of the series resistance, the value was extracted from the real part of the impedance at the resonance frequency as both the capacitive and inductive parts should influence the reading the least at this point. The value of the ESR at 53 kHz was measured to 2.5 mΩ.

In the same way, the imaginary part of the impedance should correspond to the series connection of the impedance from the series inductance and the capacitance of the capacitor, see Figure 4.26. As seen in (4.1), the capacitance is dominating at low frequencies and inductance is dominating at high frequencies. In other words, the capacitance and inductance of the capacitor can be determined by solving

$$Z_{IMAG\_Lo} \approx -\frac{1}{\omega C} \tag{4.2}$$

where Z_{IMAG_Lo} is the imaginary part of the measured impedance at low frequencies, as well as

$$Z_{IMAG\_Hi} \approx \omega L_{ESL} \tag{4.3}$$

where Z_{IMAG_Hi} is the imaginary part of the measured impedance at high frequencies.

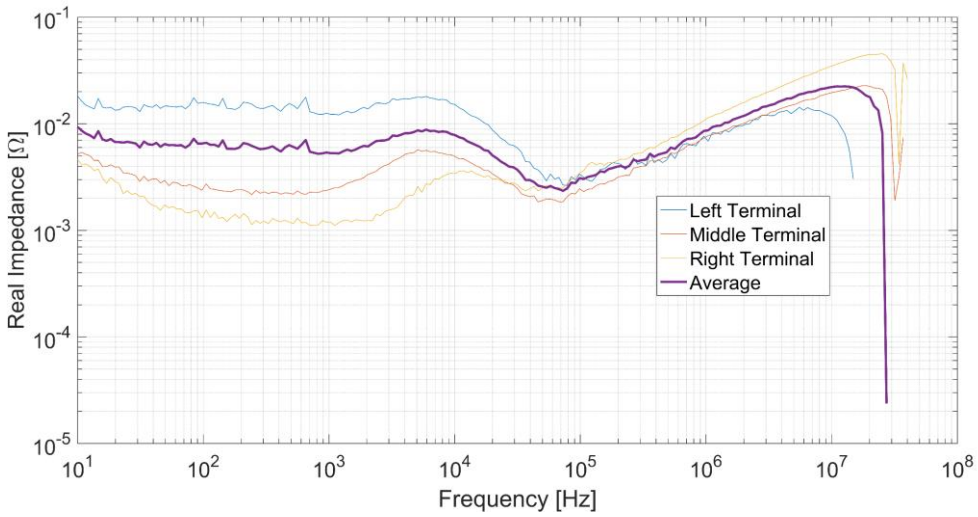

Figure 4.25. Real part of measured capacitor impedance.

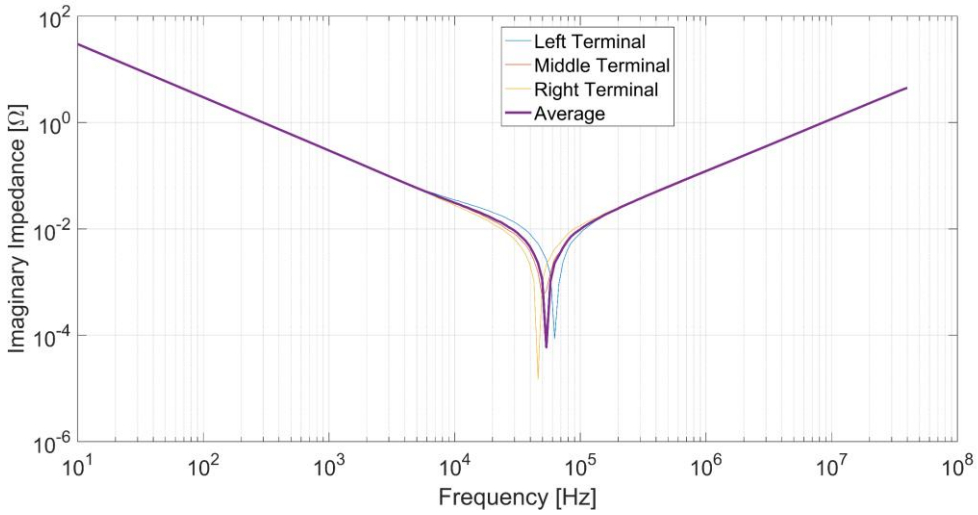

Figure 4.26. Imaginary part of measured capacitor impedance.

To get a good estimation of the capacitance value, (4.2) and (4.3) were solved for the ten lowest respectively highest frequencies and an average was calculated. This resulted in a calculated capacitance of 533 µF which corresponds well with the rated capacitance of 540 µF at low frequencies. For high frequencies, the inductance was found to be approximately 18 nH when the impact of the capacitive part was neglected. To confirm this value, the stray inductance expected to generate the same resonance frequency as seen in Figure 4.23 with a capacitance of 533 µF becomes 16 nH which is a difference of about 10 %.

If all three parameters are known, a model of the DC-link capacitor that includes the series equivalent resistance and inductance as seen in Figure 2.9 can be implemented. Simulations were performed of the initial system described in Section 3.3 using the same operating point (3000 rpm, 20 Nm), see Figure 4.27.

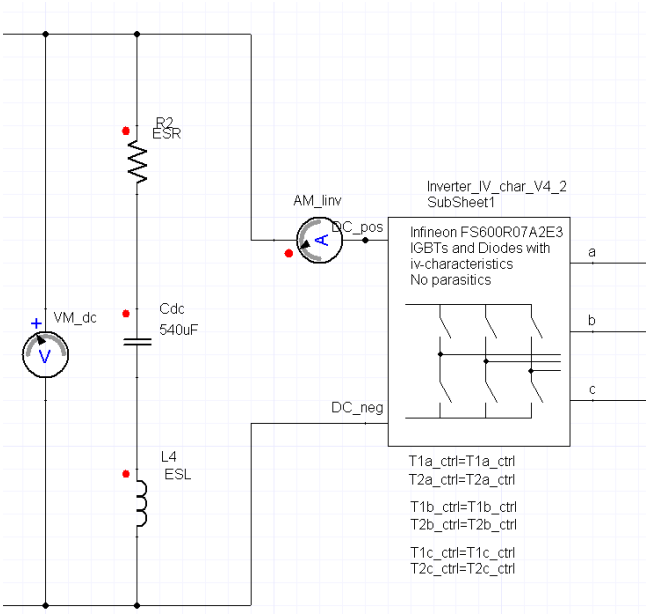

Figure 4.27. Conventional DC-link capacitor modelling including a series resistance (ESR) and a series inductance (ESL).

The resulting DC-link current and voltage waveforms are seen in Figure 4.28. From these figures, it becomes apparent that the waveforms are changed for both voltage and current when introducing ESR and ESL into the DC-link capacitor. The voltage waveforms get increased distortion and a larger fundamental ripple amplitude. The distortion is even clearer in the DC-link current waveforms. Without parasitic elements in the DC-link capacitor, the resulting current ripple is smooth but by introducing series inductance and resistance, the current waveform becomes distorted at each transistor switching interval. This is most likely due to the fact that the inductance in the capacitor now inhibit the capacitors attenuating properties at higher frequencies, thus the distortions in close proximity to each switching event.

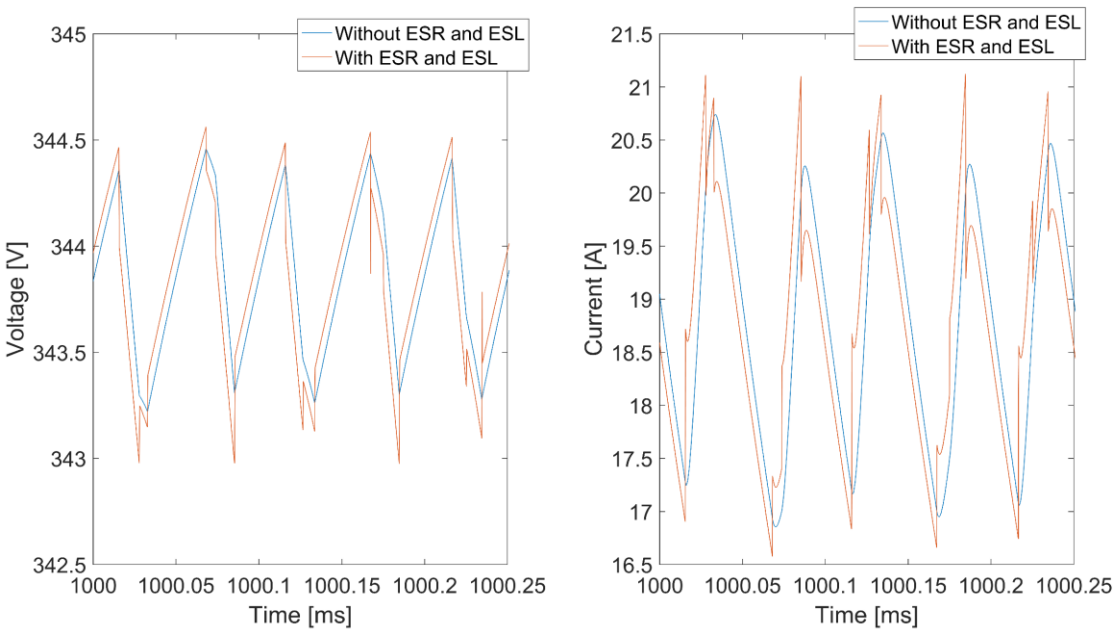

Figure 4.28. DC-link voltage (left) and current (right) waveforms for simulations both with and without ESR and ESL.

To further visualize the harmonic content of the two simulations and the differences between the two, FFT-calculations were performed and are visualized in Figure 4.29. The general conclusion drawn by these frequency spectrums is that the introduction of non-idealities such as ESL and ESR into the DC-link capacitor increases the ripple components at almost all frequencies. One exception is the current ripple at 20 kHz where the introduction of the ESR and ESL slightly decrease the ripple component. Although it does appear that the biggest differences can be seen for frequencies above 50 kHz where the non-idealities of the capacitor increase the ripple amplitudes the most.

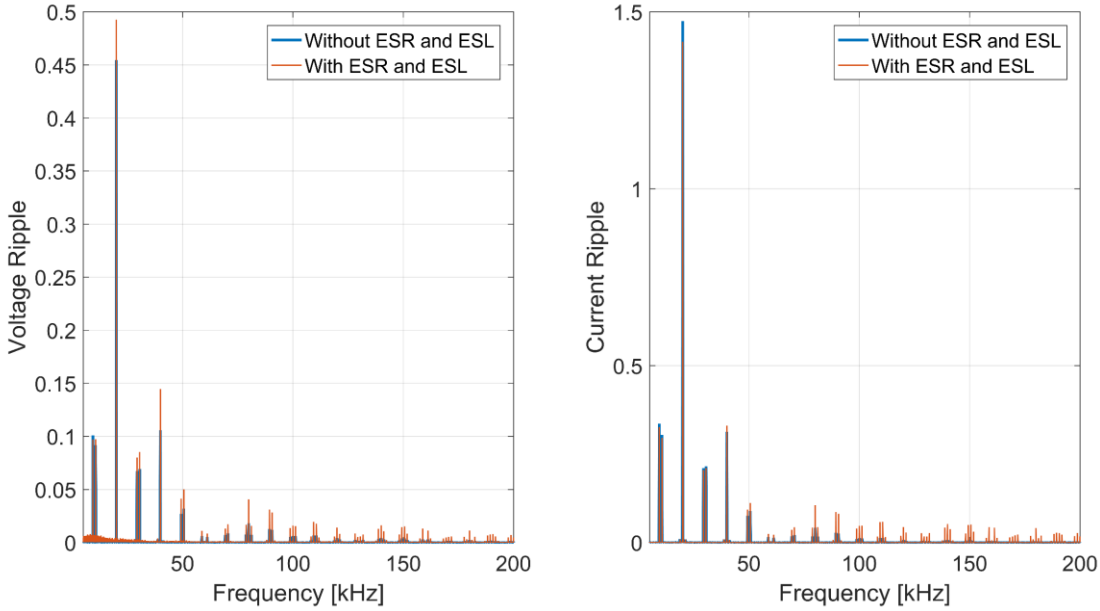

Figure 4.29. FFT of the DC-link voltage (left) and current (right) waveforms for simulations both with and without ESR and ESL.

Considering the way that the actual DC-link capacitor seen in Figure 3.1 and how the inverter is designed, the conventional capacitor simulation model described in Section 2.7 might not be the optimal representation of the actual behavior. Due to the fact that the capacitor has two separate terminals for each phase leg, the physical connection between the capacitor and the inverter is more adequately represented by the model in Figure 4.30. Each phase-leg has a separate connection to the DC-link capacitor which also acts as the only connection to the battery. This means that the stray inductance and resistance of the DC-link capacitor terminals is connected between the battery and the converter and thus carries the entire DC-link current and not solely the ripple current into the capacitor as with the previous model.

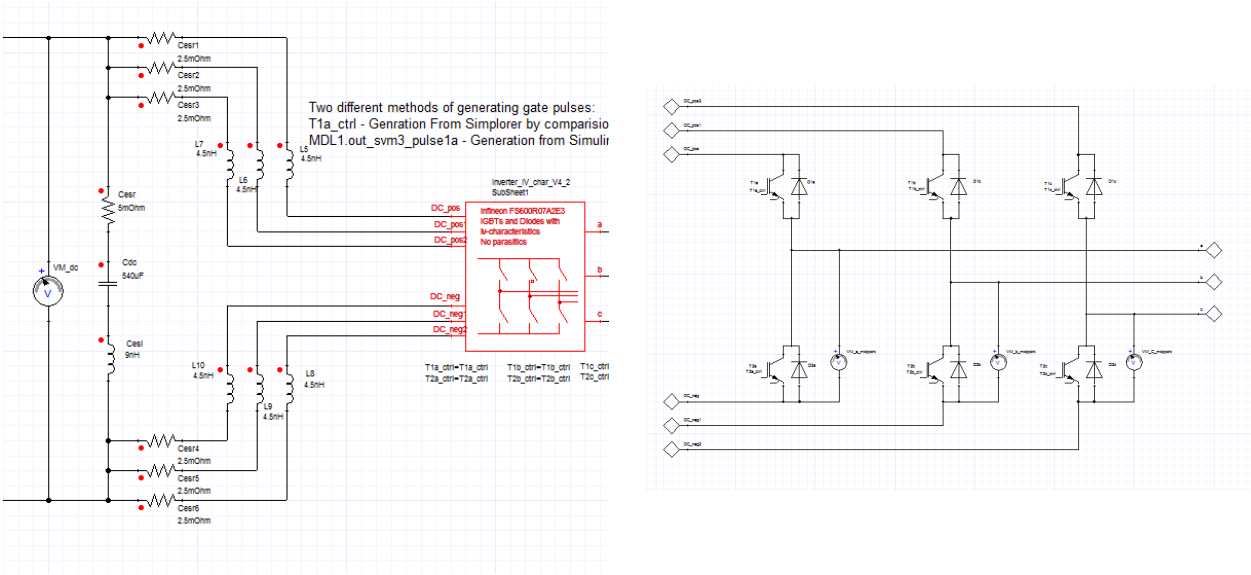

Figure 4.30. Modelling of DC-link capacitor where stray elements are separated into branches that represents the physical construction. The right side shows the connections inside the inverter.

For the same operating point (3000 rpm, 20 Nm) two more simulations were performed. Once with the impedance divided equally between branches and typical ESR/ESL and one where all impedance was located in the branches. Figure 4.31 and Figure 4.32 depicts the voltage and current waveforms on the DC-link with three different implementations of the nonidealities of the DC-link capacitor. The comparison is made between having all impedance in a series connected ESR and ESL, having all impedance located in the individual branches that connects the capacitor to the inverter, and by having the impedance split equally between the two. By comparing the DC-link current in Figure 4.32 with the current seen in Figure 4.28 that includes all parasitic elements inside the branches of the capacitor model and not having any typical ESR or ESL produced a DC-link current closely resembling the one achieved where no ESR or ESL was present at all. In much the same way sharing the impedance between series connected and inside the branches produces a sort of mid-point between the two other simulations. Similar reasoning can be made for the DC-link voltage by comparing Figure 4.31 and Figure 4.28.

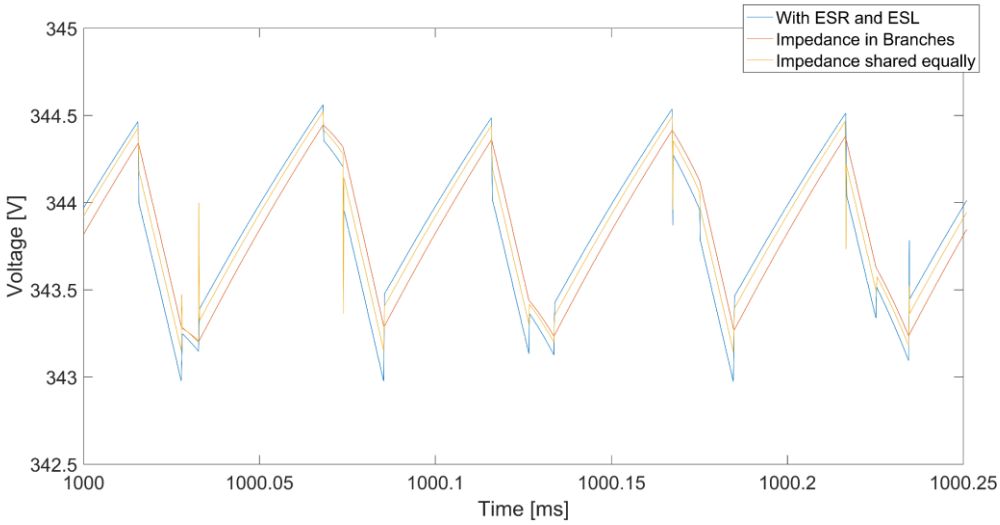

Figure 4.31. Simulated DC-link voltage waveforms for three different capacitor models.

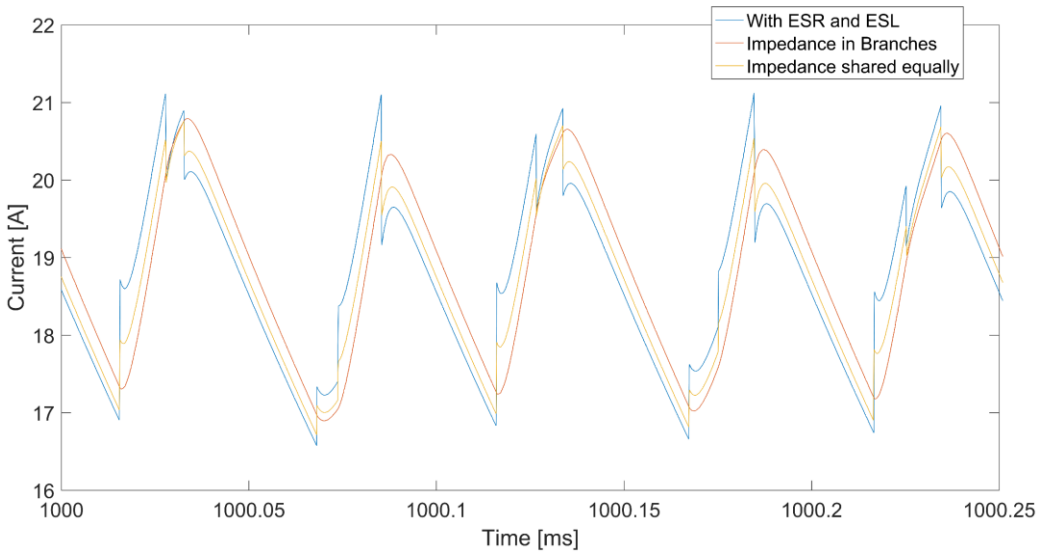

Figure 4.32. Simulated DC-link current waveforms for three different capacitor models.

Through FFT analysis of the DC-link voltage and current it can be observed that a lower amplitude of the ripple components is obtained when the impedance is located solely in the branches. The amplitude of ripple then increases as more and more of the impedance is shifted from the branches and put in series with the capacitor. This is valid for both the current and the voltage ripple and the observations are in-line with what could be seen from the current and voltage waveforms themselves. By moving more of the impedance into the terminals that connects the capacitor to the inverter, the attenuation is increased and the amplitude of ripple components on the DC-link is decreased.

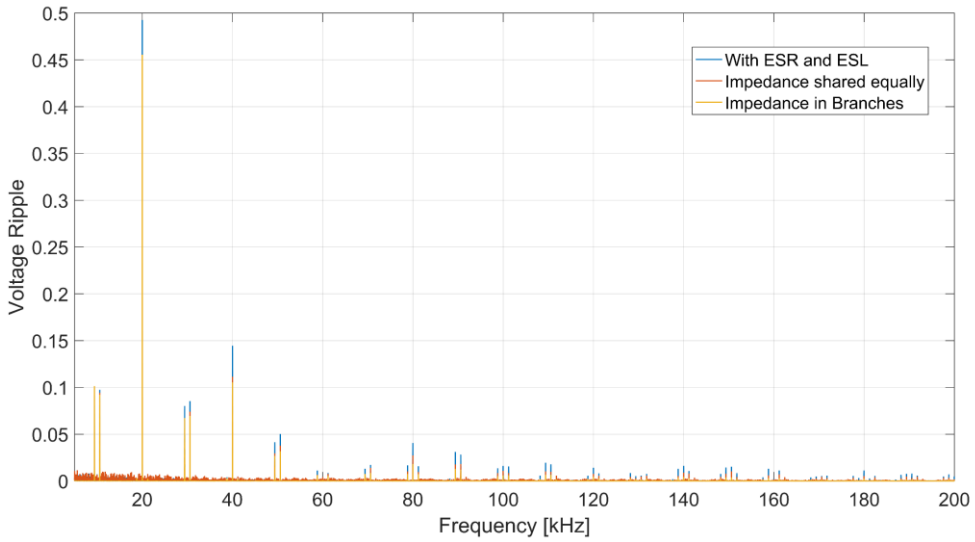

Figure 4.33. Simulated DC-link voltage ripple for three different capacitor models.

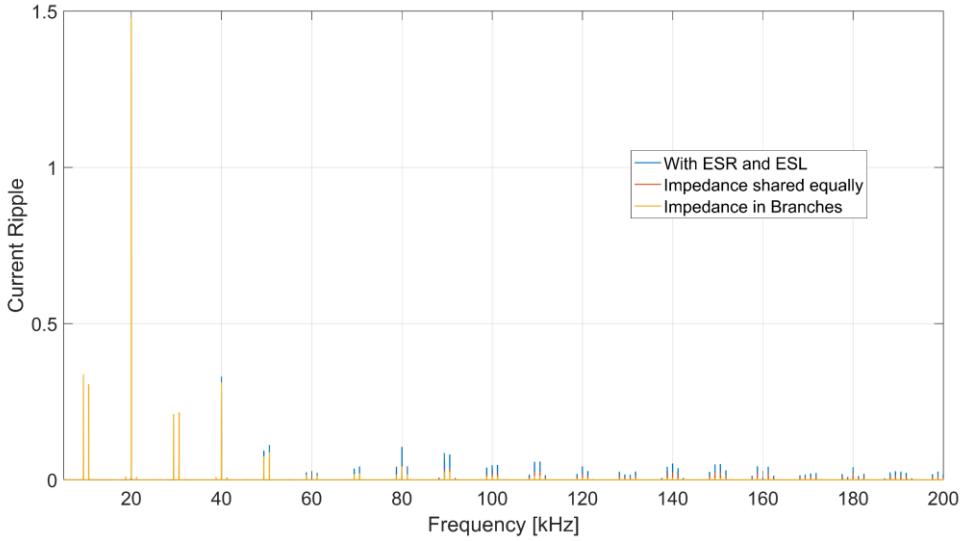

Figure 4.34. Simulated DC-link current ripple for three different capacitor models.

The results of these simulations show that it is important for ripple estimation how the nonidealities of the capacitor is modelled. Since the DC-link capacitor has a very specific shape and the connection between the DC-link and the inverter goes through the terminals of the capacitor, this becomes even more important. However more measurement and modelling work is needed to identify what percentage of the parasitic elements are present in the branches respectively the capacitor. These measurements were not possible due to the internal composition of the capacitor (consisting of several series and parallel-connected smaller capacitors) and the measurement equipment at hand. Due to not having determined where the parasitic elements reside, the first simulation model containing a ESR and ESL was used throughout this thesis as opposed to the more advanced model.

A better way to try and model the behavior of the DC-link capacitor would be to inject a current with varying frequency onto each of the three output terminals of the capacitor and measure the resulting voltage ripple at the DC-input terminals. From this voltage, an S-function could be developed to describe the dynamic behavior of the capacitor.

4.2.1 Dependence on ESR and ESL

To investigate the impact that the ESR and the ESL have on the resulting DC-link current and voltage ripple, simulations was performed for different parameter values. Both the ESR and ESL was swept individually from 20 % to 250 % of the measured values for the real capacitor (from here on referred to as “nominal values”).

A summary of how ESR and ESL affected the DC-link ripple can be seen in Figure 4.35. The first thing that can be noted is that ESR appears to have similar effect on both DC-link voltage and current ripple THD. The ripple components increase with an increased ESR, however the effect is greater, as a percentage of the nominal ripple, for the DC-link current. Although, the dependence on capacitor ESL is quite different; For the DC-link voltage ripple no major changes in ripple THD can be seen as a result of changing the ESR, however a small local minimum can be seen at 125 % of the nominal ESL. For the DC-link current ripple a very different pattern emerges when studying the ripple THD. As for the voltage, a local minimum

can be seen at 125 % of nominal ESL, with the THD increasing significantly, around 20 %, for both increased and decreased values of the ESL.

Both of these finds suggest that for the system simulated, with the current switching frequency, load etc., the most beneficial ESL value is 125 % of the nominal value, which most likely is due to the resonance frequency being located at an optimum frequency for attenuating the inverter ripple components.

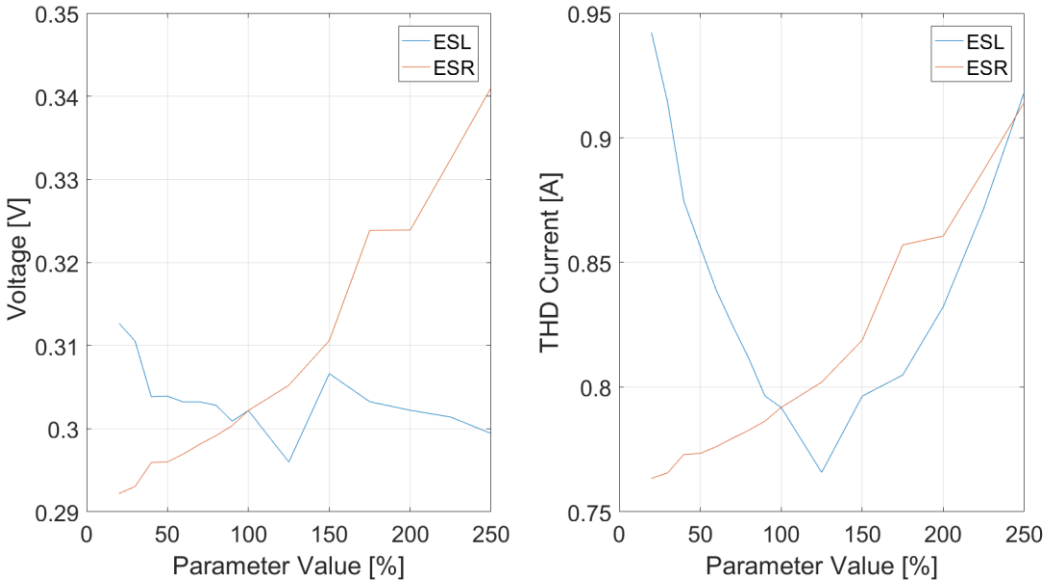

Figure 4.35. Simulated DC-link voltage (left) and current (right) ripple for different values of capacitor ESR and ESL.

As the ESR appeared to affect the ripple almost linear, and ESL showed no particular effect on the voltage ripple, the DC-link current FFTs of three different ESL-values is showed in Figure 4.36. Note that each FFT is shifted to showcase their individual amplitudes easier. The values chosen are the smallest, nominal, respectively largest value of the ESL to showcase the extreme points. A lower value of the ESL gives a higher fundamental component of the ripple than what is seen for a high ESL. However, for the higher order components the amplitude increases drastically for higher values of ESL, causing the total ripple THD to become close to the one seen for the small ESL. The nominal value of the ESL can be seen to give a midway of the two extremes; The fundamental component is smaller than for a low ESR, but higher order components are attenuated better than in the high ESR-simulation.

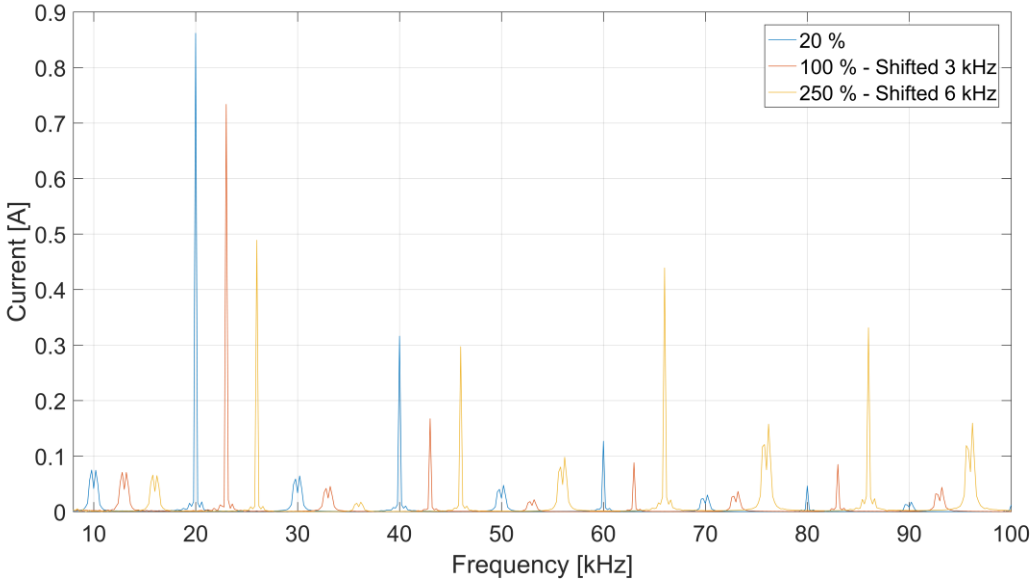

Figure 4.36. FFT of simulated DC-link current for 20 % and 250 % of nominal ESL.

4.2.2 Comparisons to similar capacitors

As the ripple dependence on parameters such as capacitor ESL was seen to be quite large in some of the simulations performed in Section 4.2.1, an investigation of a few similar DC-link capacitors was performed to visualize typical differences in capacitor ESR and ESL. These values correspond to a variety of similar DC-link capacitors, see Table 4-2, and will be referred to as alternative DC-link capacitor 1 through 3 for simplicity.

Table 4-2. D. Alternative DC-link capacitors considered.

	Alternative 1	Alternative 2	Alternative 3
Manufacturer	AVX	EPCOS	EPCOS
Model	FHC26I0507K--	B25655J4507K005	B25655P4607J011
Capacitance [µF]	500	500	600
Voltage rating [V]	450	450	450
Current rating [A(rms)]	170	120	150
Parasitic Inductance [nH]	15	15	25
Series resistance [mΩ]	0.45	1	0.6

The resulting DC-link voltage and current ripple can be seen in Figure 4.37 for a single operating point (1500 rpm, 20 Nm). As the largest differences in ripple can be seen at 20, 40, 60 and 80 kHz each of these frequencies are shown in greater detail in Figure 4.38 to Figure 4.41.

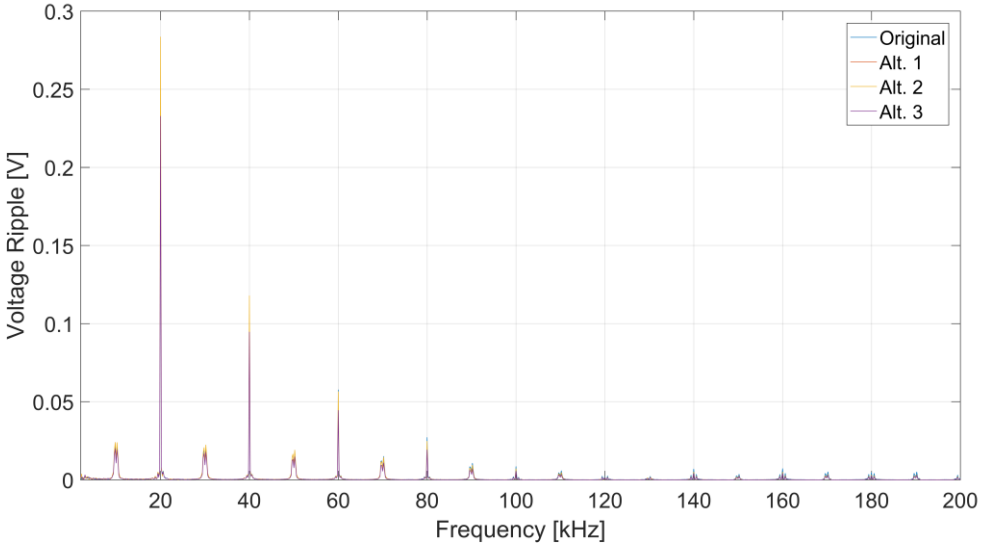

Figure 4.37. DC-link voltage and current ripple with different DC-link capacitors.

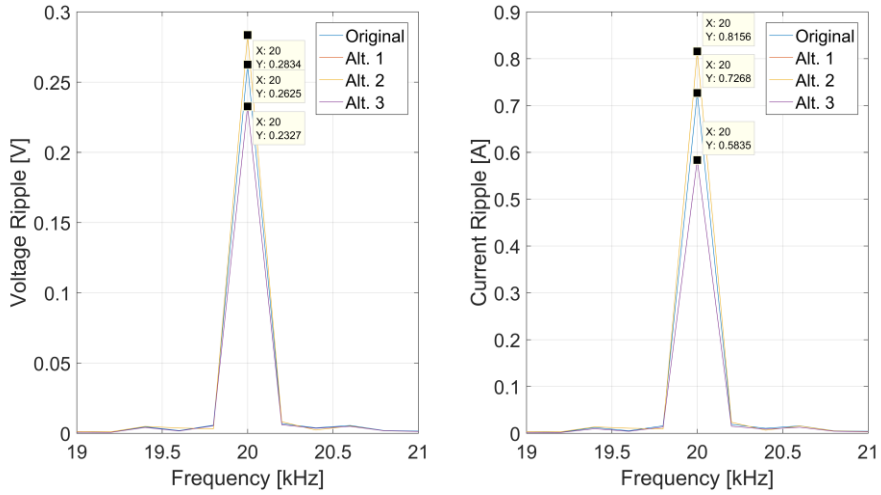

Figure 4.38. DC-link voltage and current ripple with different DC-link capacitors, zoomed around 20 kHz.

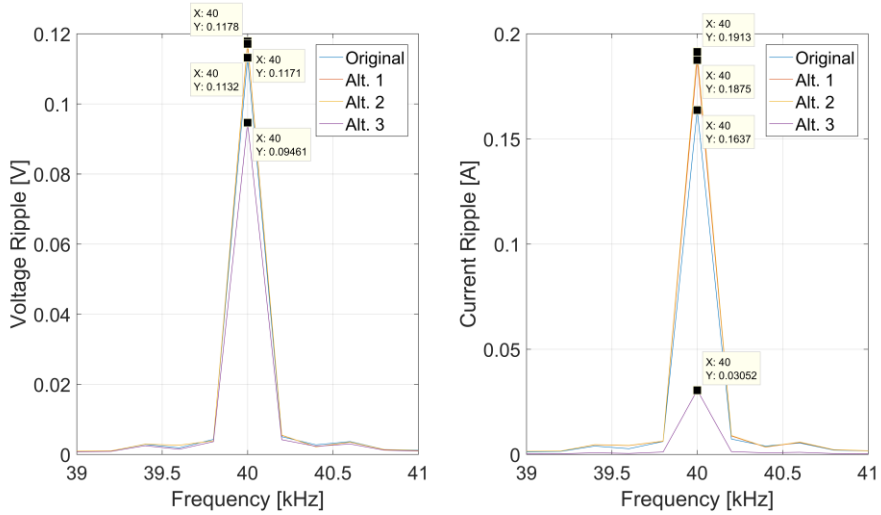

Figure 4.39. DC-link voltage and current ripple with different DC-link capacitors, zoomed around 40 kHz.

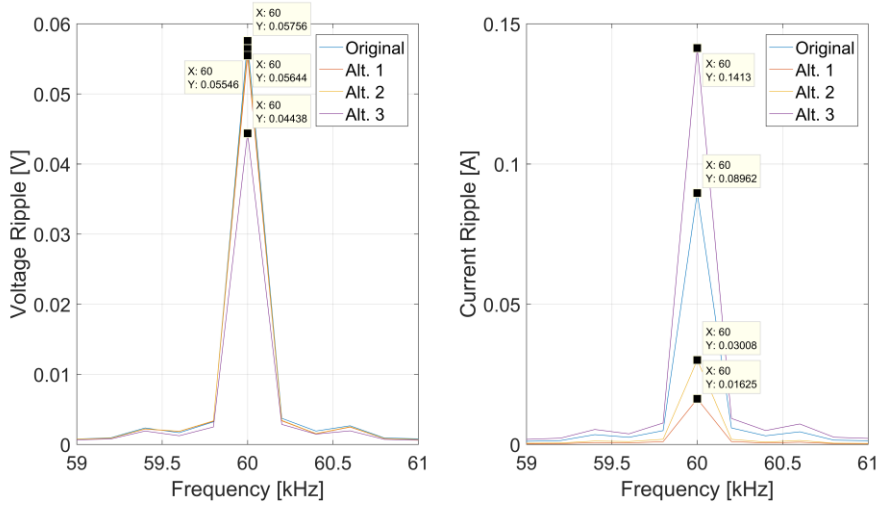

Figure 4.40. DC-link voltage and current ripple with different DC-link capacitors, zoomed around 60 kHz.

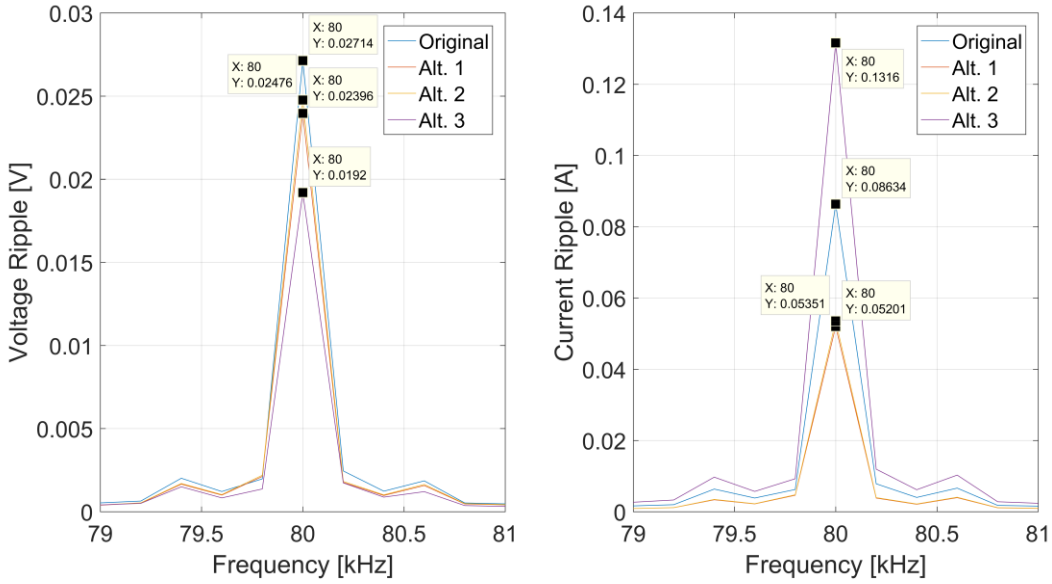

Figure 4.41. DC-link voltage and current ripple with different DC-link capacitors, zoomed around 80 kHz.

Common for all frequencies investigated is that DC-link capacitor 1 and 2 produced similar ripple components, with the exception of 60 kHz where a difference in current ripple was observed. Since the only thing separating these capacitors was the ESR it can be concluded that a change in series resistance from 0.45 to 1 mΩ will not affect the resulting voltage and current ripple in any significant way.

The lowest fundamental ripple component of both current and voltage was obtained for the third alternative DC-link capacitor. This is obvious as this capacitor has slightly higher capacitance than the other capacitors which is directly related to the fundamental ripple component. This was also the case for the 40 kHz component where the capacitance was found to be the dominant factor. For the current ripple, the amplitude was significantly lower for capacitor alternative 3.

It can also be observed that at the higher frequencies (60 and 80 kHz), significantly higher current ripple was seen for DC-link capacitor 3 and lower current ripple was seen for alternative 1 and 2. This agrees well with the fact that the third alternative has a much higher ESL whose impedance increases with frequency. For the amplitude of the voltage ripple, the relationship was different with lowest ripple for the third alternative which has the highest capacitance.

The total harmonic content, as discussed in Section 3 is shown for the four different DC-link capacitors in Table 4-3 . Here it can be seen that a very small distinguishable difference was seen between alternatives one and two while alternative three showed the lowest THD and the original capacitor the second lowest THD. This again confirms the fact that the biggest influence on both voltage and current ripple amplitude comes from the capacitance of the DC-link capacitor. It should be noted that the highest ripple amplitude is found at the fundamental frequency, at which the capacitance plays a big part. This means that if higher order ripple components were to be weighted higher than lower order components, the result of the THD might be different. These results can also be checked against what was seen in Section 4.2.1, where less ripple would be anticipated from a capacitor with as low ESR as possible, and a ESL slightly higher than the nominal value. This can be confirmed by looking at the ESR and ESL for capacitor alternative 3. It had one of the lowest ESR, along with being the only alternative with an ESL slightly higher than the nominal value of 18 nH. However, the impact of the increased capacitance of alternative 3 should not be neglected as this could be the biggest cause for lower ripple than the other alternatives.

Table 4-3. Harmonic distorition for the four DC-link capacitors.

DC-link Capacitor	THD Voltage	THD Current
Original	0.33	0.89
Alternative 1	0.33	0.93
Alternative 2	0.33	0.93
Alternative 3	0.29	0.80

It can be concluded that at lower frequencies the capacitance of the DC-link capacitor plays a significant role in the amplitude of both the voltage and the current ripple components. But for higher frequencies, the parasitic elements become more and more prominent, especially for the current ripple components.

4.3 Inverter

Countless parameters affect the resulting DC-link current and voltage ripple and in this thesis a few prominent ones were investigated and evaluated. Both parameters affecting the operating point of the inverter, such as speed and torque reference, was investigated along with blanking time and switching frequency.

4.3.1 Speed Reference

One important parameter in determining the operating point of the drivetrain is the PMSM speed-reference. The reason behind this is that an increasing machine speed requires a higher inverter output voltage due to an increasing back-EMF. This in turn affects the amplitude modulation ratio of the inverter.

To investigate the impact that the speed reference has on the resulting DC-link ripple components the system was evaluated for a span of speed references from 500 rpm to 9000 rpm. Throughout these simulations all other parameters were kept constant. The resulting THD values can be seen in both Table 4-4, where the values are given with a 1000 rpm interval, and in Figure 4.42, where a plot of the DC-link current and voltage ripple THD is shown as a function of the speed reference.

Table 4-4. Resulting simulated DC-link current and voltage ripple THD for different speeds.

Speed Reference: [rpm]	Current Ripple THD [A]	Voltage Ripple THD [V]
1000	0.622	0.234
2000	0.998	0.375
3000	1.355	0.492
4000	1.643	0.581
5000	1.826	0.629
6000	1.836	0.616
7000	1.990	0.642
8000	2.259	0.732
9000	3.130	1.002

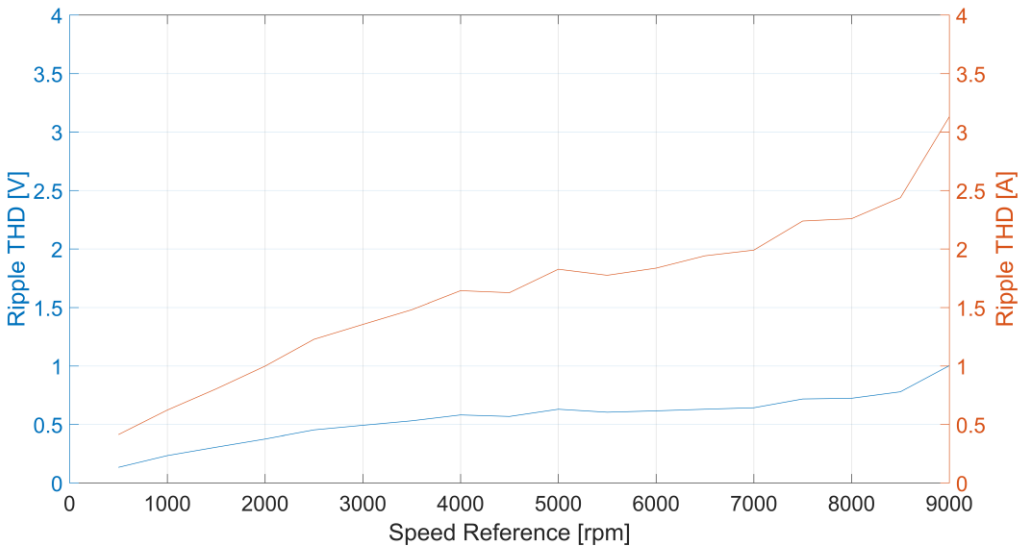

Figure 4.42. Current and voltage ripple THD as a function of speed reference.

From Figure 4.42 it can be concluded that an increase in speed reference from 500 to 9000 rpm results in an increase in the total ripple level for both DC-link current and voltage of approximately 8 times. As mentioned previously the reason that the speed reference influences the produced ripple components is due to the changing amplitude modulation ratio, see Figure 4.43 where the amplitude modulation ratio for five different speed references is plotted. This illustrates that an increasing speed reference results in a higher amplitude modulation ratio which in turn affect the ripple as stated in (2.13). As seen in Figure 4.43, the amplitude modulation ratio for each speed has a certain ripple which increases with the ratio. The ripple exists as the needed amplitude modulation ratio is continually calculated by e.g. the DC-link voltage. Due to the voltage and current ripple and other continually changing conditions, the amplitude modulation ratio has to be adjusted at each time step which produces a ripple.

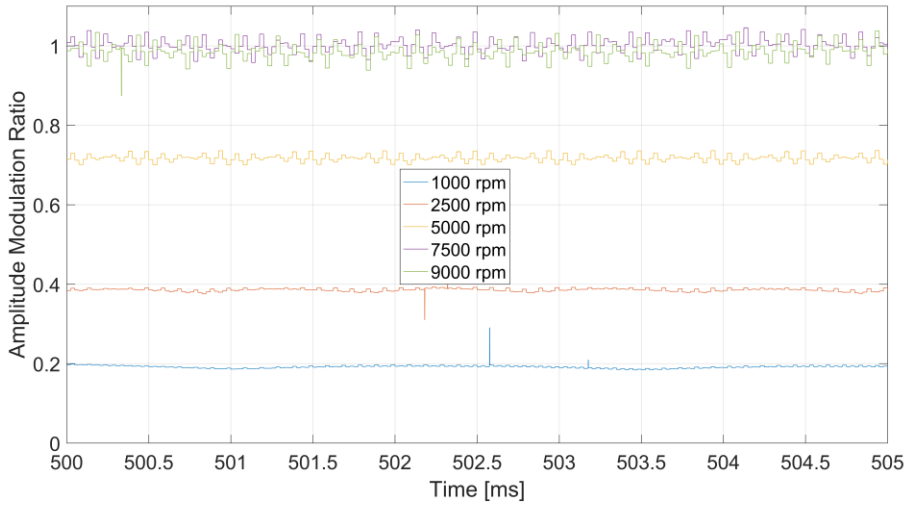

Figure 4.43. Amplitude modulation ratio of the inverter for five different speed references.

In Figure 4.44 and Figure 4.45 an FFT-plot of the DC-link current and voltage for two different speed references can be seen. In these figures, it can be seen that an increasing speed reference and therefore an increasing amplitude modulation ratio affects not only the magnitude of the ripple but also the frequency distribution. For both the DC-link current and voltage, the ripple content is pushed into a lower frequency spectrum when the reference is increased which needs to be taken into account alongside the increasing ripple magnitude.

It can be seen in both Figure 4.44 and Figure 4.45 that the 20 kHz ripple component has doubled in amplitude for the higher speed and that the ripple components around 60, 80, 100 kHz and above have higher amplitude for the lower speed reference. However, the most prominent difference is the sidebands around 10 kHz. Aside from the fact that the sidebands are located further away from 10 kHz due to the increased inverter output frequency, the magnitude of the sideband components have increased drastically as the speed increased. In other words, avoiding very high amplitude modulation ratios and overmodulation might be preferable not only to keep the total ripple magnitude lower, but also to push the ripple content into higher frequencies.

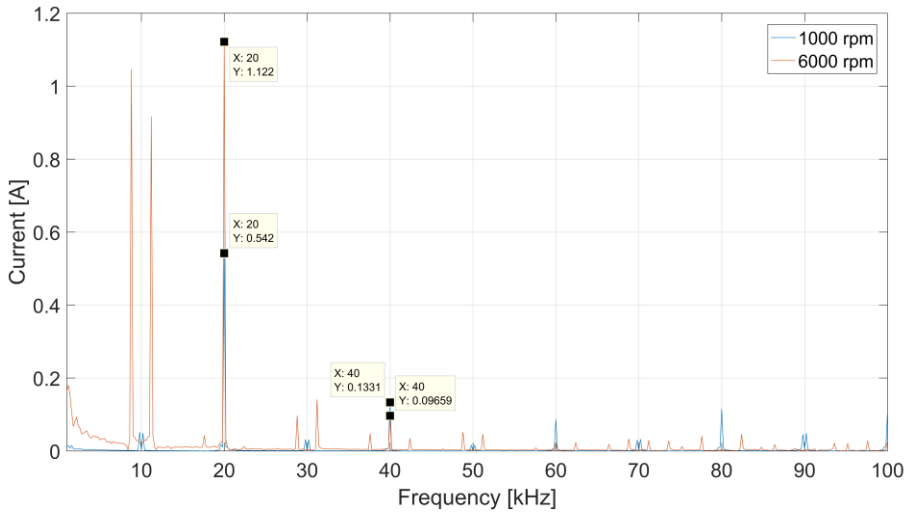

Figure 4.44. FFT of the DC-link current for speed references of 1000 rpm and 6000 rpm.

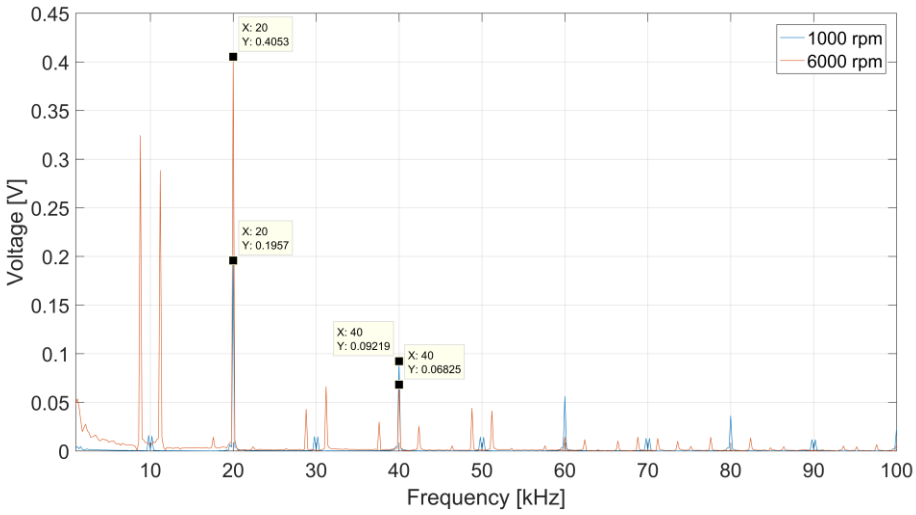

Figure 4.45. FFT of the DC-link voltage for speed references of 1000 rpm and 6000 rpm.

4.3.2 Torque Reference

Another important parameter in determining the operating point of the inverter is the PMSM torque-reference. This reference is proportional to the output current of the inverter and will therefore affect the total DC-link ripple as discussed in Section 2.8.1.

To investigate the impact that the torque reference has on the resulting DC-link ripple components the system was evaluated for a span of speed references from 5 Nm to 70 Nm. Throughout these simulations all other parameters were kept constant, e.g. 1500 rpm speed reference. The resulting THD values can be seen in both Table 4-5, where the values are given in steps of 10 Nm, and in Figure 4.46, where a plot of the current and voltage DC-link ripple

THD is shown as a function of the torque reference. From these simulations, it was concluded that the torque reference plays a major role in determining the resulting total ripple THD-level where the amplitude increased with more than 10 times when increasing the torque from 5 to 70 Nm.

Table 4-5. Resulting simulated DC-link current and voltage ripple THD for some of the torque references evaluated.

Torque Reference: [rpm]	Current Ripple THD [A]	Voltage Ripple THD [V]
10	0.402	0.154
20	0.802	0.305
30	1.222	0.462
40	1.606	0.604
50	2.048	0.766
60	2.416	0.898
70	2.824	1.040

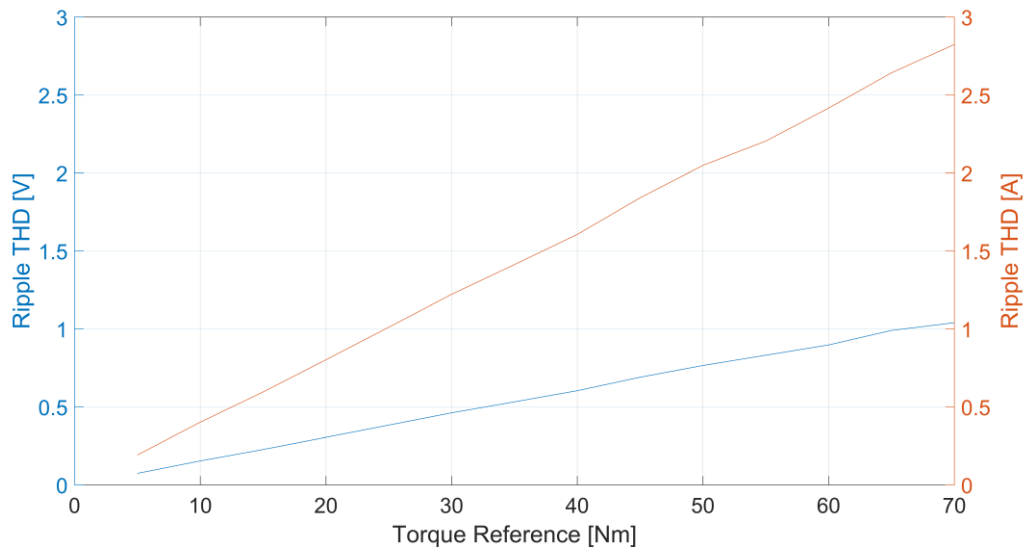

Figure 4.46. Simulated current and voltage ripple THD as a function of torque reference.

The torque reference contributes to a linear increase in ripple THD as expected. This can be seen in (2.13) which shows that the expected ripple amplitudes is linearly dependent on the output current amplitude which in turn is proportional to the produced torque of the machine. As seen in Figure 4.47, the DC-link current will increase in magnitude and will contain larger ripple components as the torque reference increases.

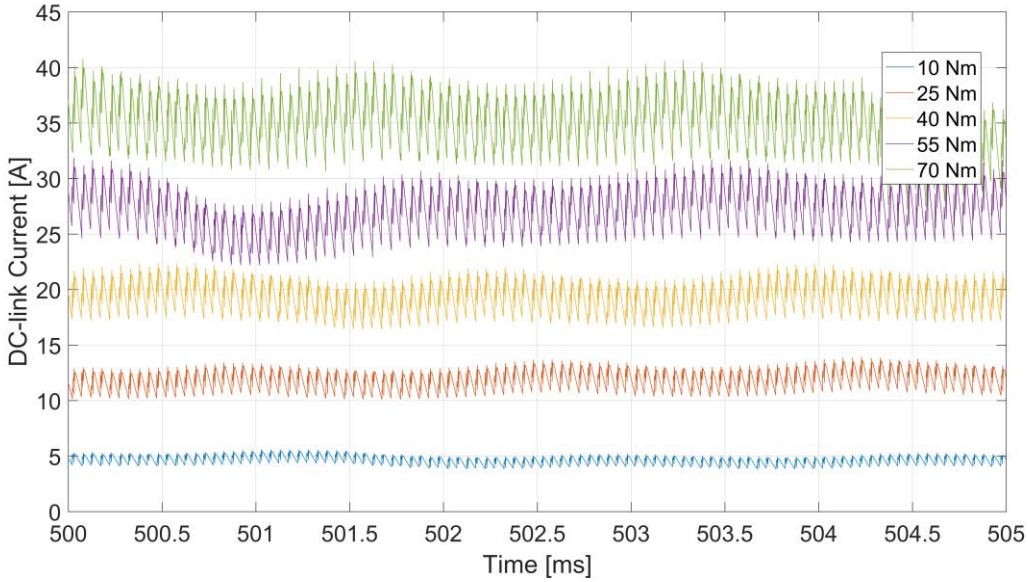

Figure 4.47. Simulated inverter input DC-link current for five different torque references.

To evaluate if an increased torque reference will have any effect on the distribution of the ripple components an FFT analysis was made, see Figure 4.48 and Figure 4.49. As follows from (2.13), the increasing current magnitude should affect all frequency components equally, and thus not give rise to any change in the ripple distribution. However, if Figure 4.48 and Figure 4.49 are observed (where the FFT of the 10 Nm simulation has been scaled up by a factor of 6 to give it a similar amplitude to the 60 Nm simulation) it can be seen that the amplitude of the low frequency ripple components will increase as the torque reference is increased.

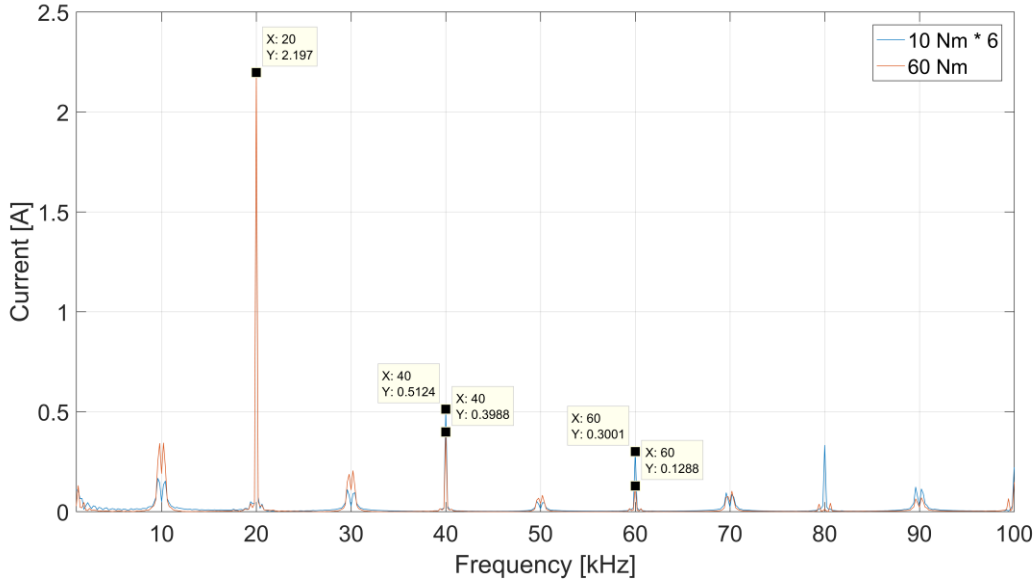

Figure 4.48. FFT of the DC-link current for torque references of 10 Nm and 60 Nm.

The redistribution of the ripple components is similar to what can be seen in Figure 4.44 and Figure 4.45 here the amplitude modulation ratio was changed and the ripple components were concentrated around lower frequencies. For an ideal inverter, the amplitude modulation ratio will not vary between the simulations of two different torque references, but simulations showed that the modulation ratio increased from 0.25 to 0.35 when increasing the torque from 10 Nm to 60 Nm. This can be explained by the fact that the increased output current results in a higher voltage drop over the cable and the machine resistance which needs to be compensated by an increased output voltage.

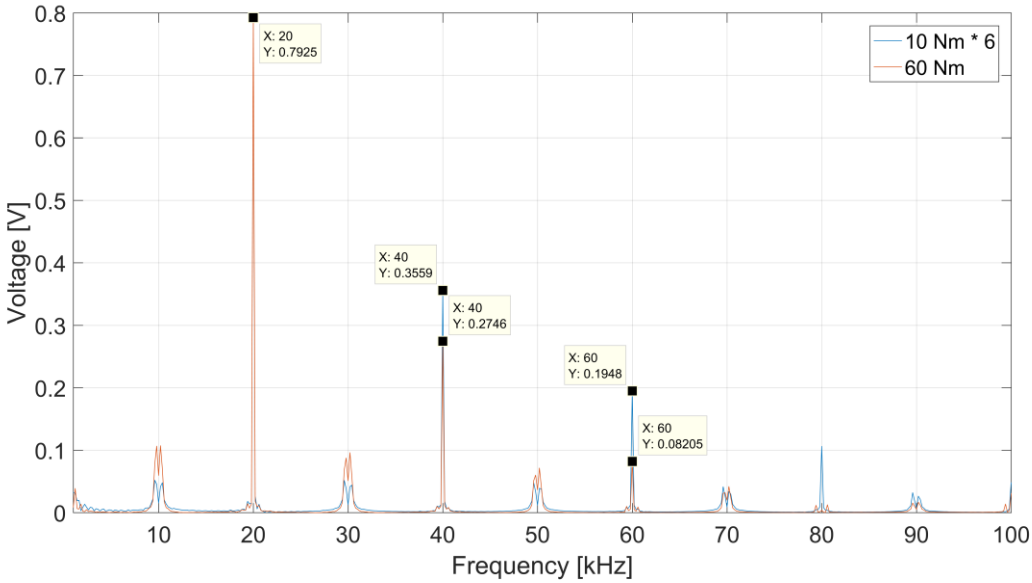

Figure 4.49. FFT of the DC-link voltage for torque references of 10 Nm and 60 Nm.

4.3.3 Switching Frequency

As described in Section 2.8.1, it can be seen that the switching frequency decides where the ripple components will be located. An analysis was performed in order to show the effect that the switching frequency has on the ripple magnitude for a given operating point. Table 4-6 shows the investigated switching frequencies and the corresponding DC-link current and voltage ripple THD. Throughout these simulations, the torque and speed references were kept constant at 20 Nm respectively 1500 rpm.

Table 4-6. Switching frequencies evaluated along with corresponding current and voltage ripple THD.

Switching Frequency: [kHz]	Current Ripple THD [A]	Voltage Ripple THD [V]
6	1.511	0.504
8	1.077	0.384
10	0.797	0.303
12	0.635	0.256
14	0.536	0.222
16	0.477	0.195
18	0.456	0.178
20	0.536	0.159
30	0.561	0.122
40	0.624	0.109
50	0.642	0.092
60	0.692	0.089

In Figure 4.50, the same DC-link ripple THD is plotted as a function of the switching frequency to better visualize the decrease in total ripple as the switching frequency is increased. From these plots, it can be concluded that the relationship between the total ripple and the switching frequency is not linear. Both the DC-link current and the voltage ripple decreases significantly when changing from 5 kHz to 10 kHz switching frequency. However, due to the non-linearity of the relationship the same significant impact cannot be seen when increasing the switching frequency further up towards 15 kHz and 20 kHz. There is still a decrease in total ripple, but the relative decrease in ripple from each increase in switching frequency is decreasing. This introduces a trade-off into selecting the switching frequency of the inverter; At some point the increased complexity brought on by increasing the switching frequency becomes larger than the benefit of the decreased total ripple that the increased switching frequency would bring.

Although increasing the switching frequency further towards 60 kHz might not be realistic, an interesting trend can be seen in the simulated DC-link ripple. After the 20 kHz mark, both DC-link voltage and current ripple continues to flatten out, however the current and voltage ripple obtain inverse dependence on the switching frequency. The DC-link voltage continues to decrease with switching frequency while the current ripple sees a small increase with the switching frequency. It should however be noted that this dependence on switching frequency is several times smaller than the dependence that can be seen between 5 kHz to 20 kHz. Once again, it should also be pointed out that switching frequencies upwards of 60 kHz are seldom used for this type of applications, but it was included in this thesis as it highlighted some interesting trends.

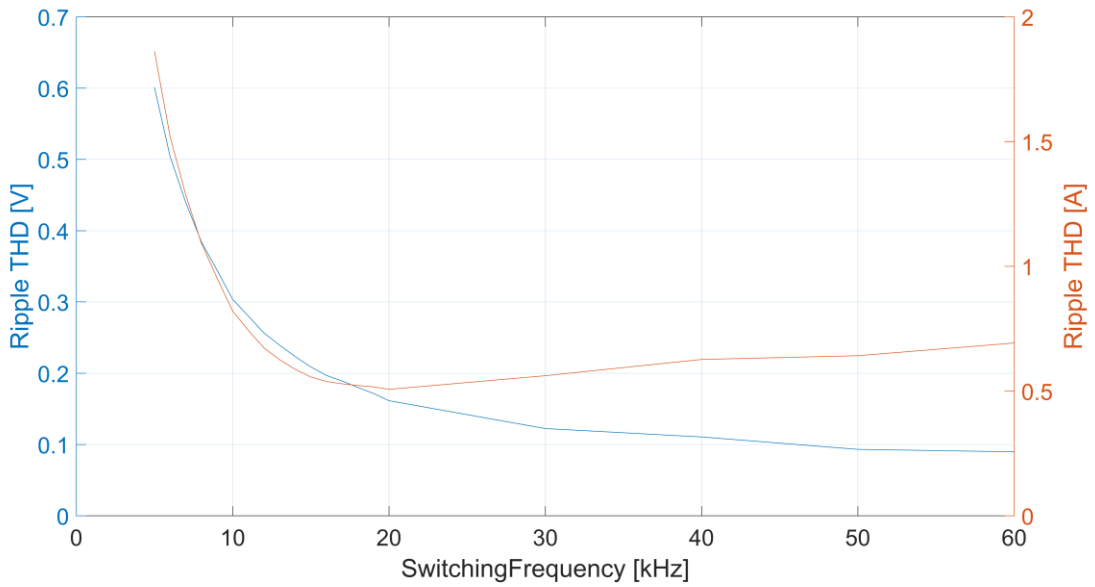

Figure 4.50. Ripple THD for both DC-link current and voltage as a function of switching frequency.

To evaluate the change in distribution of the ripple components for the lower switching frequencies an FFT was performed, see Figure 4.51 and Figure 4.52 which show the FFT-curve of the DC-link current.

Figure 4.51 shows the difference in ripple distribution when increasing the switching frequency from 5 to 10 kHz. Except from the decrease in total ripple the distribution does not change in any significant way for this increase in switching frequency. The highest frequency component is still found at twice the switching frequency and the higher frequency components will decrease exponentially.

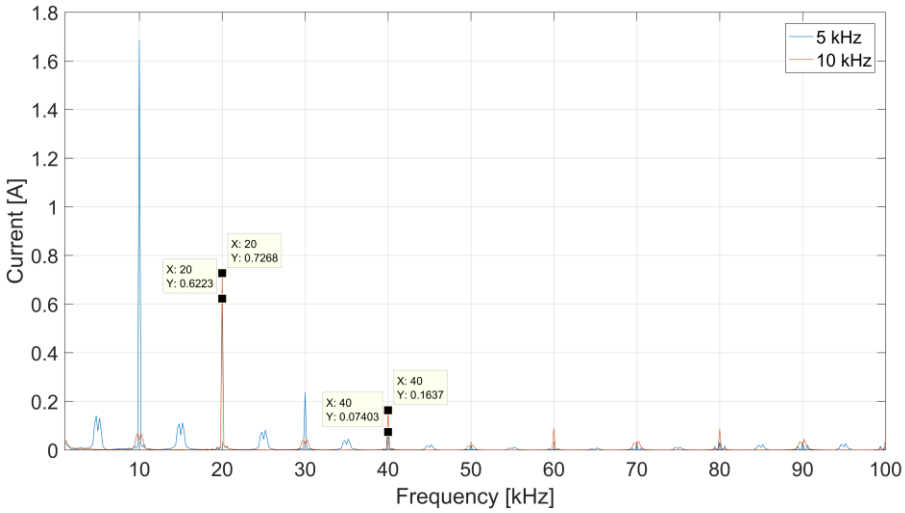

Figure 4.51. FFT of the DC-link current for switching frequencies 5 kHz and 10 kHz.

As seen in Figure 4.52 which shows the FFT of the switching frequencies 10 kHz and 20 kHz, an increase of the switching frequency also changes the behavior of the ripple. For a switching frequency of 20 kHz, the 40, 80 and 120 kHz ripple components have approximately the same amplitude and does not show the exponential decrease seen in Figure 4.51. One possible explanation for this may be the fact that the DC-link capacitor has a resonance frequency of 50 kHz which means that the attenuation of ripple quickly declines above that point. The difference between 10 kHz and 20 kHz switching frequency then becomes the fact that the fundamental components of the ripple is shifted higher up in frequency. For a switching frequency of 10 kHz the ripple components are found at 20 kHz, and multiples thereof. Increasing the switching frequency to 20 kHz, according to the theory in Section 2.8.1, results in ripple components at 40 kHz and multiples thereof.

As the lower harmonic components will have the highest amplitude, the shift in switching frequency causes more and more of the ripple produced by the inverter to end up above the resonance frequency of the DC-link capacitor as the switching frequency increases. For higher frequencies, the DC-link capacitor shows a more inductive behavior and thus the attenuation of the ripple is decreased. For the lower switching frequency, the main part of the ripple injected by the inverter has a frequency lower than the resonance frequency of the DC-link capacitor and can thus be attenuated better.

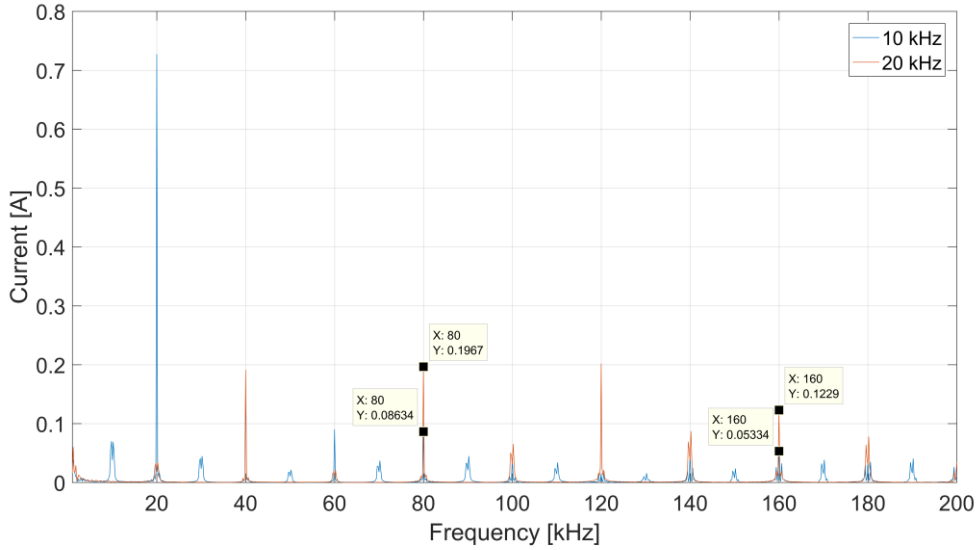

Figure 4.52. FFT of the DC-link current for switching frequencies of 10 kHz and 20 kHz.

To investigate the difference in ripple behavior at higher frequencies, FFT of the DC-link ripple was performed for the 30kHz and 50 kHz simulations, see Figure 4.53. FFT of the DC-link voltage (right) and current (right) for switching frequencies of 30 kHz and 50 kHz. The difference in trend between the DC-link current and voltage ripple at higher frequencies becomes apparent here. For the DC-link voltage the fundamental ripple component can be seen to be decreased for the 50 kHz simulation compared to the 30 kHz simulation, although the amplitude of the higher order components are increased with an higher switching frequency. However, since the fundamental component contributes the most to ripple THD this increases overall for the DC-link voltage. For the DC-link current however, both the fundamental component and the higher order components increase slightly with the increased switching frequency causing the total ripple THD to increase. However, as the used system is not designed for switching frequencies of upwards of 60 kHz emphasis should not be put on the exact values of ripple THD showed in this section, but rather the fact that the positive effects on total ripple by increasing the switching frequency is not linear.

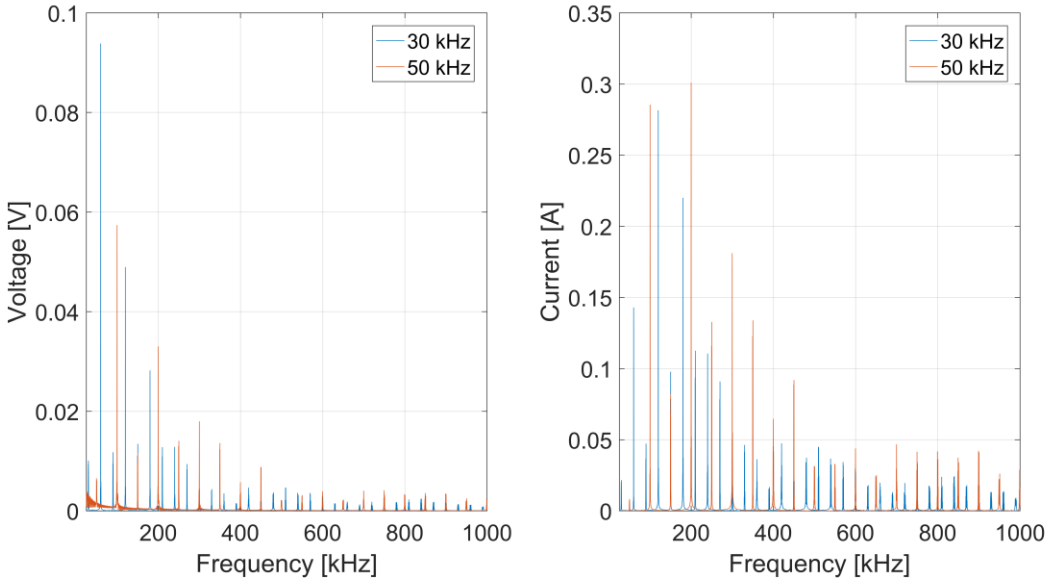

Figure 4.53. FFT of the DC-link voltage (right) and current (right) for switching frequencies of 30 kHz and 50 kHz.

Worth noting here is the fact that the THD calculations in this thesis does not weigh the different frequency components differently. Lower frequency ripple components are seen as equally undesired as higher frequency ripple components. If higher or lower order components were to be weighted, the THD-plots might look different since higher switching frequencies pushes the ripple components into higher order components.

4.3.4 Blanking time

Blanking time refers to the time at which both transistors in the same phase-leg is turned off when alternating between the upper and lower transistors and is often not considered as a contributor to the DC-link ripple. In this section, the effect of different blanking times on the DC-link current and voltage ripple is evaluated. The evaluated blanking times, along with corresponding current and voltage ripple THD can be seen in Table 4-7 for a 1500 rpm 20 Nm operating point.

Table 4-7. Blanking times evaluated along with corresponding current and voltage ripple THD.

Blanking Time: [µs]	Current Ripple THD [A]	Voltage Ripple THD [V]
1	0.812	0.309
2	0.797	0.303
3	0.799	0.304
4	0.821	0.311
5	0.824	0.312
10	0.859	0.323
15	0.882	0.330

As seen in both Table 4-7 and Figure 4.54, where the ripple THD-values are plotted as a function of the blanking time, an increased blanking time from 1 to 15 µs will generate a 10 % increase in both DC-link current and voltage ripple THD.

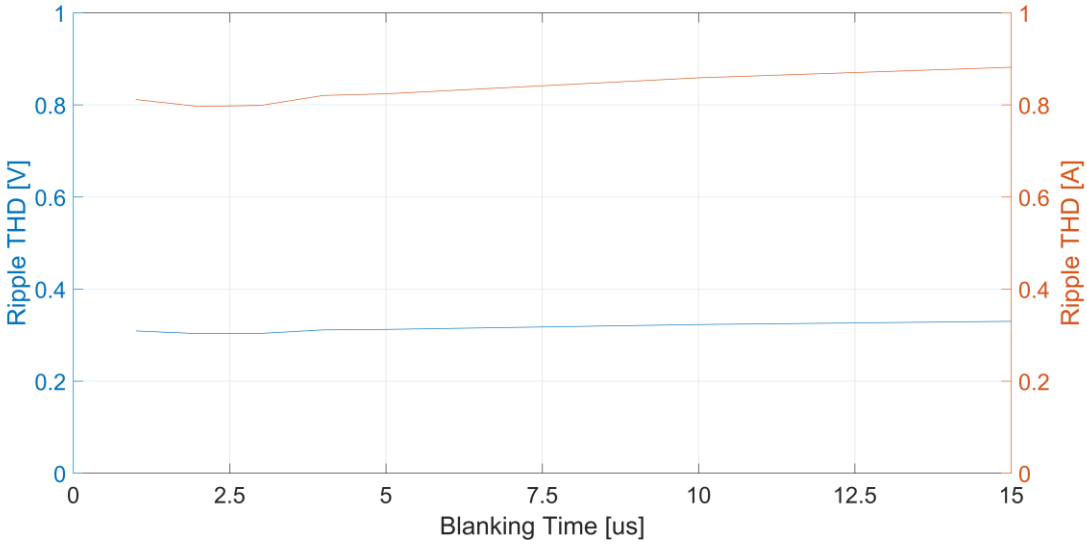

Figure 4.54. DC-link current and voltage ripple THD as a function of blanking time.

To investigate whether a change of the blanking time will have any effect on the distribution of the ripple components, Figure 4.55 and Figure 4.56 are plotted. They illustrate the DC-link current and voltage ripple FFT, respectively, for the shortest and longest blanking times investigated. For the longest blanking time (15 µs) an increase can be seen primarily in the lower order harmonics for both DC-link current and voltage. Higher frequencies (e.g. 80 kHz) are primarily present for the 1 µs blanking time.

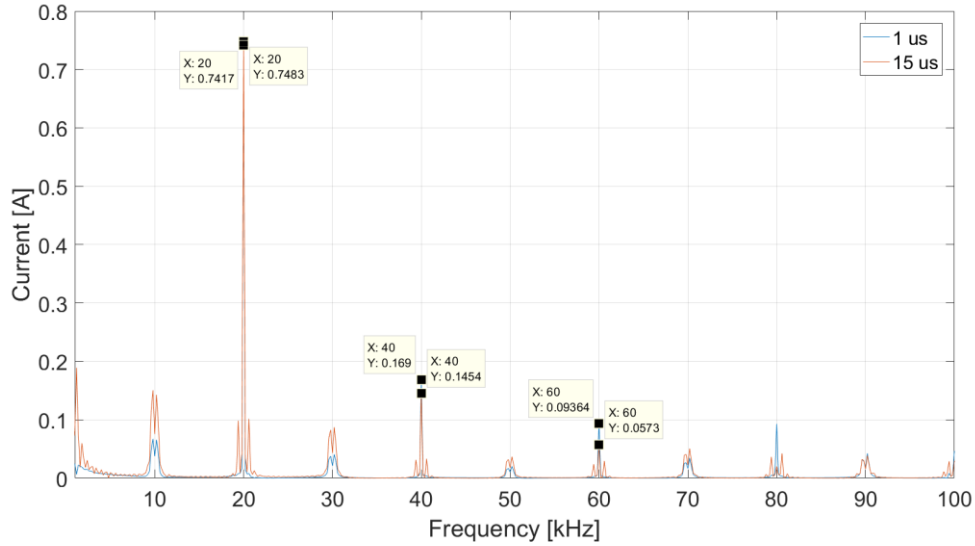

Figure 4.55. FFT of the DC-link current 1 µs and 15 µs blanking times.

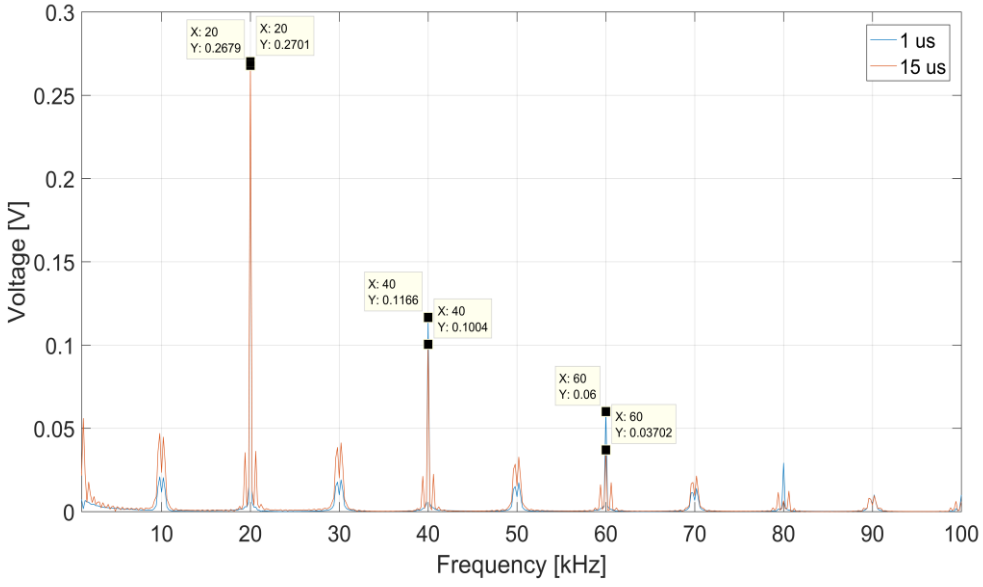

Figure 4.56. FFT of the DC-link voltage FFT for 1µs and 15 µs blanking times.

4.4 Measurements On a IGBT-Inverter

As a part of this thesis, measurements were performed on an actual drive-train to verify the results obtained from the simulation model. The main objective of these measurements were not to match the produced ripple exactly since too many parameters outside the scope of the thesis affect the ripple magnitudes, but rather to investigate the distribution of the ripple. This includes comparing the most prominent ripple components and their corresponding frequencies, as well as trying to find ripple components that are produced by phenomenon not included in the simulations.

4.4.1 Operating points

To ensure that the measurements and simulations were performed for the same conditions, two different operating points were analyzed. Two of the main simulation parameters are the machine speed and torque profiles since they dictate the current and output voltage of the inverter. Limitations in the rig gave that the operating points could not be selected within the entire operating range of the system. Due to this, measurements were performed at the two operating points specified in Table 4-8.

Table 4-8. Operating points at which measurements and simulations has been compared, converted to machine values.

Operating Point	Speed [rpm]	Torque [Nm]
1	1500	10.7
2	1500	20.0

4.4.2 Measurement results

The measurements were conducted in accordance to the measurement setup described in Section 3.4 where both AC and DC quantities were collected. The line-line voltage and phase current were measured on the inverter output and can be seen in Figure 4.57 for measurement point 2. These measurements were compared with the simulated inverter quantities to confirm the operating point of the inverter.

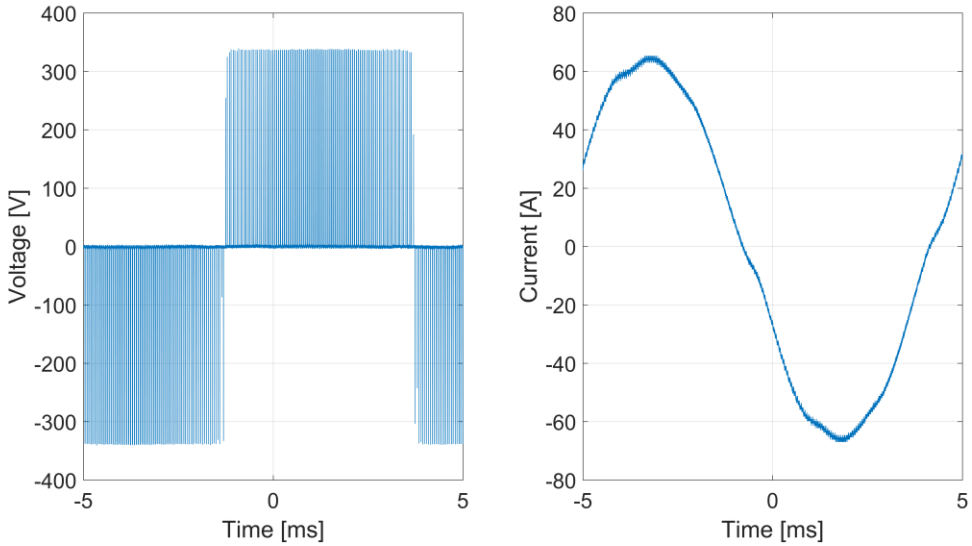

Figure 4.57. Phase-phase voltage (left) and phase current (right) for measurements of operating point 2.

When measuring the DC-side quantities (DC-link voltage and current), the measurement setup was AC-coupled to remove the DC-component of the voltage and the current. This was done to ensure that the entire vertical resolution of the oscilloscope was used to measure only the DC-link ripple. The DC-levels were recorded separately and can be seen in Table 4-9 for all measurements. Figure 4.58 shows the corresponding DC-link voltage and current waveforms for measurement point 2 respectively. As observed from these figures the fundamental triangle waveform is still present but a distinct oscillation with a frequency of 350 kHz is superimposed.

Table 4-9. DC-values of DC-link voltage and current for both measurement points.

	Value	
	DC-link voltage [V]	DC-link current [A]
Measurement Point 1	346.8	11.9
Measurement Point 2	349.5	6.5

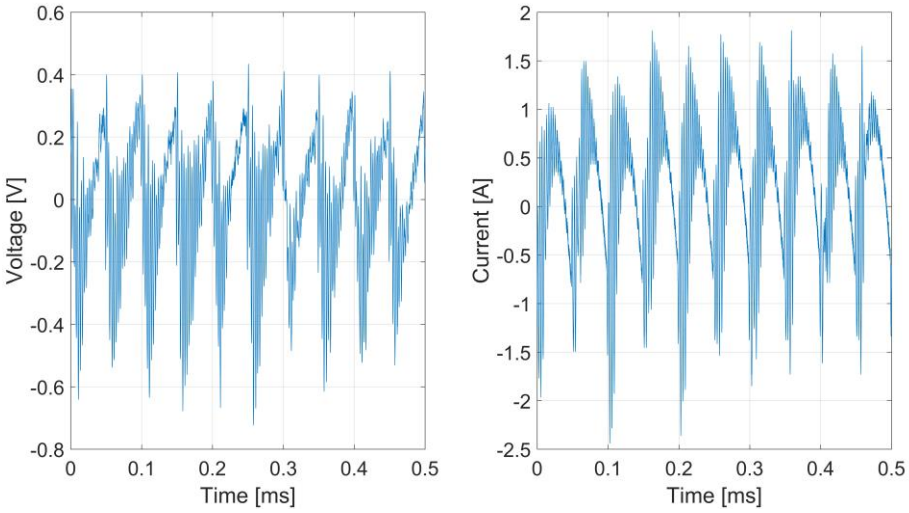

Figure 4.58. DC-link voltage (left) and current (right) for measurements of operating point 2.

To visualize this oscillation, an FFT-analysis of both the DC-link voltage and current can be seen in Figure 4.59 and Figure 4.60. From these figures, it becomes apparent that the actual drivetrain has significant ripple components around 350 kHz in both the DC-link voltage and the current.

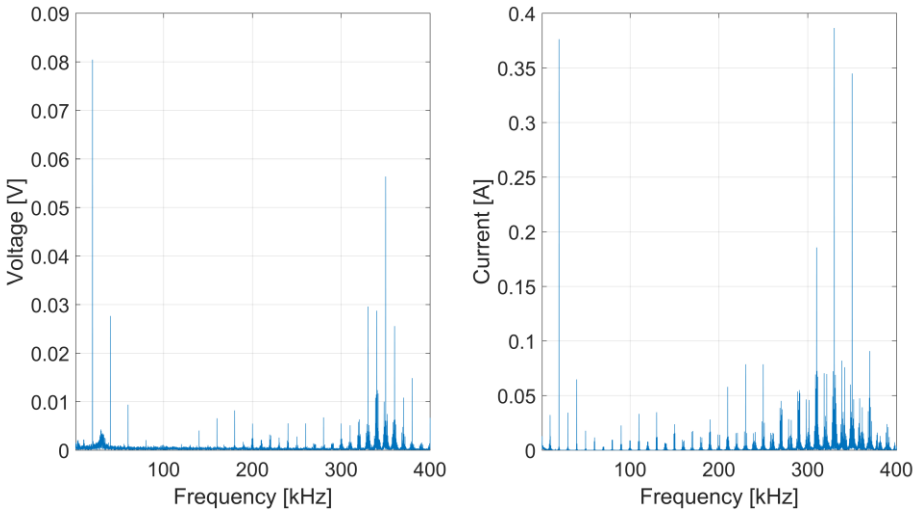

Figure 4.59. FFT of DC-link voltage (left) and current (right) for operating point 1.

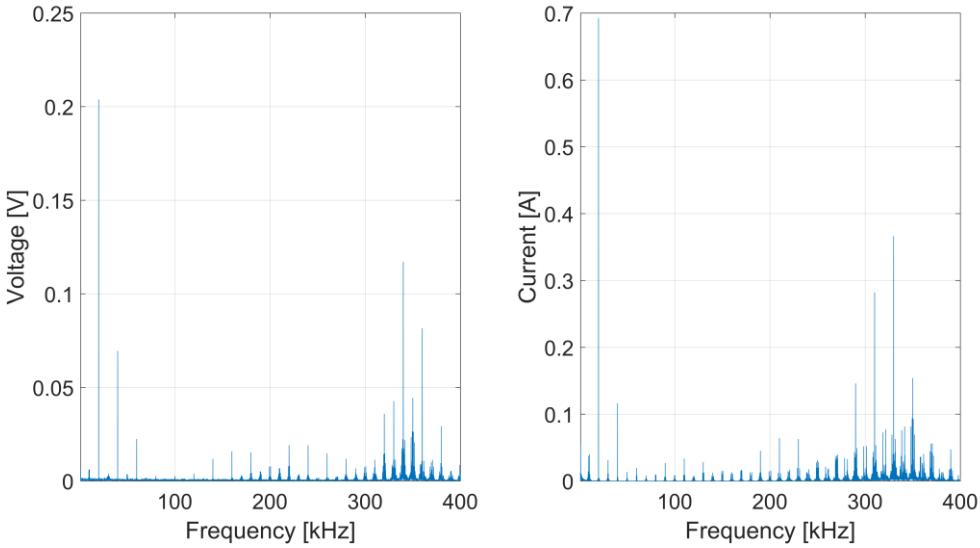

Figure 4.60. FFT of DC-link voltage (left) and current (right) for operating point 2.

To obtain a quantification of all ripple components, the ripple THD is presented in Table 4-10. The values are calculated for both measurement points and calculated in two different ways; for frequencies up to 200 kHz and for frequencies up to 400 kHz. This was done to visualize the impact of the oscillating components around 350 kHz.

Table 4-10. Ripple THD for DC-link voltage and current for measurements on drive-train.

	Measurements			
	Voltage [V]		Current [A]	
Maximum Freq [kHz]	200	400	200	400
Operating Point 1	0.086	0.116	0.391	0.709
Operating Point 2	0.218	0.274	0.708	0.887

4.4.3 Simulation results

Simulations were performed on the same operating points as for the measurements and the simulated AC-quantities can be seen in Figure 4.61. A quick inspection shows that both the line-line voltage and the phase current shows a similar frequency as the measured values. In addition to this, the phase current has the same amplitude which indicates that the operating condition of the simulation is the same as the one obtained during the measurements. By comparing the simulated DC-link current and voltage seen in Figure 4.62 and the waveforms obtained from the measurements, the fundamental shape of the current and voltage is the same for both simulation and measurements. However, the higher frequency oscillations seen in the measurements are not present in the simulation results which indicate that they are the result of a component not included in the simulation model.

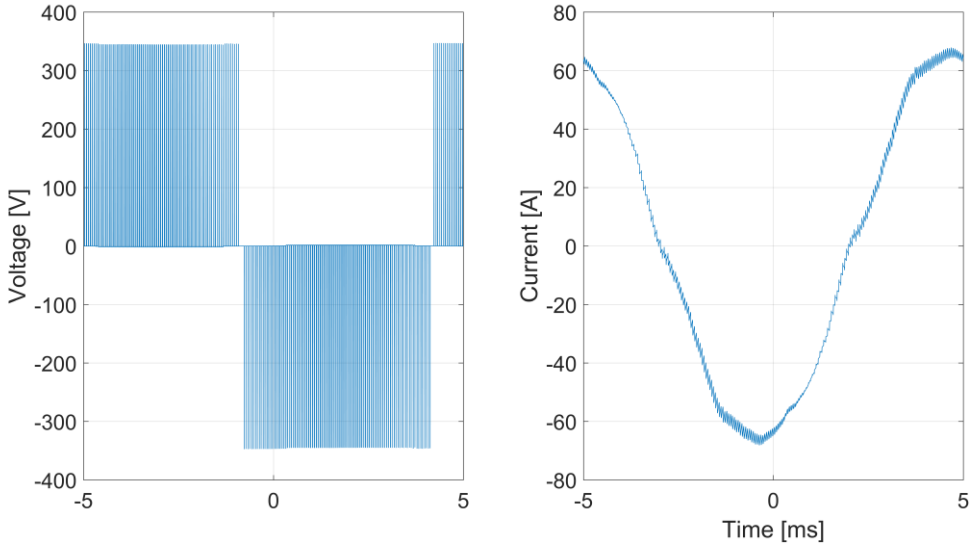

Figure 4.61. Phase-phase voltage (left) and phase current (right) for simulations of operating point 2.

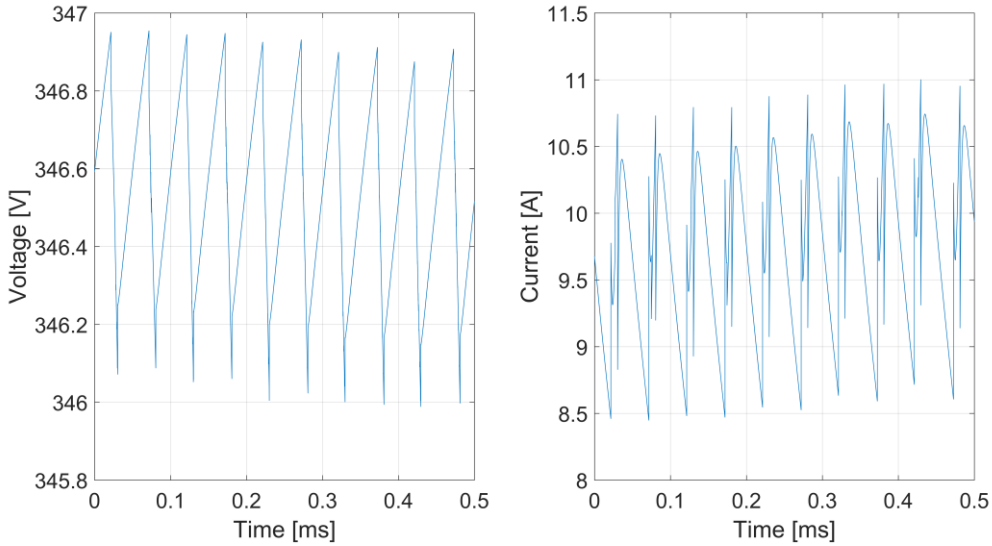

Figure 4.62. DC-link voltage (left) and current (right) for simulations of operating point 2.

To illustrate the differences between the simulation results and the measurements, Figure 4.63 and Figure 4.64 show the FFT of the DC-link voltage and current for both simulations and measurements. As observed in the waveforms, the oscillating components at 350 kHz are completely absent from the simulations, but for the measurements they will in some cases have an equally large amplitude as the fundamental ripple component.

In addition to the mismatch regarding the 350 kHz component, discrepancies can be found between the measurements and the simulations in several locations. This is however not surprising since many different components affect the actual ripple levels, e.g. battery, electrical machine and filters. However, certain conclusions can still be drawn from the FFT-plots. One example is that the relative differences between the three first harmonics (20, 40 and 60 kHz) decreases from operating point 1 to operating point 2, this means that the simulation model appears to give a better fit as the torque reference, and therefore the current magnitude, increases.

Perhaps the most important thing to notice from Figure 4.63 to Figure 4.64 is the fact that the current ripple is better approximated by the simulation model than the voltage ripple. By comparing the fundamental components, it can be seen that the difference between the simulations and the measurements was 77.4% and 29.6 % for voltage measurements 1 and 2, respectively. The corresponding values for the current ripple were 4.8 % and 5.6 %, respectively, when examining the 20 kHz fundamental ripple component. This difference is another indication that a more detailed model of the DC-link capacitor is needed. Such a model would e.g. be represented by the transfer function from the injected current from the inverter to the resulting DC-link voltage ripple.

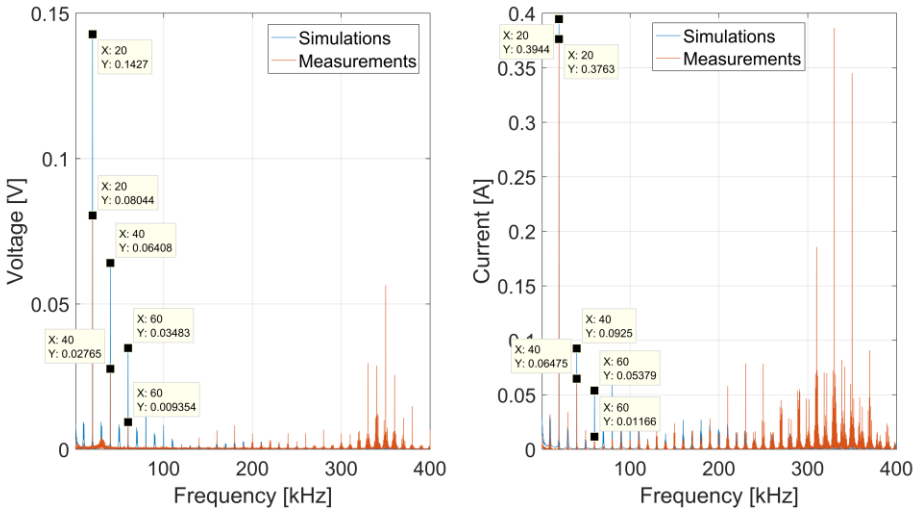

Figure 4.63. FFT of the DC-link voltage (left) and current (right) for simulations and measurements of operating point 1.

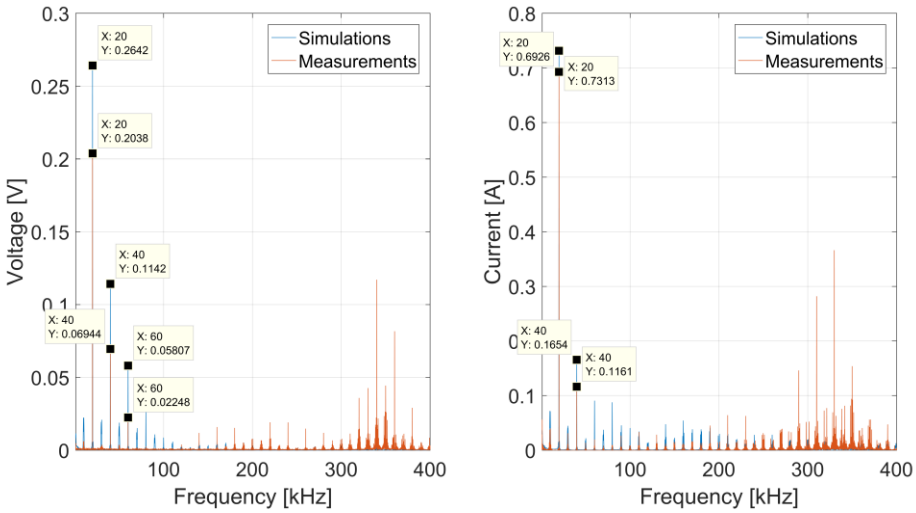

Figure 4.64. FFT of the DC-link voltage (left) and current (right) for simulations and measurements of operating point 2.

In the same manner as previous, Table 4-11 shows the total ripple harmonics for frequencies up to 200 kHz and 400 kHz for the measurements and the simulations. It can be seen that the closest fit in THD can be found for the current ripple if only frequencies up to 200 kHz are included and therefore ignoring the 350 kHz oscillatory components.

In addition to this, it can be noted that the THD increased on average 30 % for the voltage ripple and 53 % for the current when including frequencies above 200 kHz for the measurements. The THD from the simulations showed no significant difference when including higher frequency components.

Table 4-11. Ripple THD for DC-link voltage and current for measurements and simulations.

Maximum Freq [kHz]	**Measurements**				**Simulations**			
	200		400		200		400	
	Voltage [V]	Current [A]	Voltage [V]	Current [A]	Voltage [V]	Current [A]	Voltage [V]	Current [A]
Operating Point 1	0.086	0.391	0.116	0.709	0.163	0.421	0.163	0.424
Operating Point 2	0.218	0.780	0.274	0.887	0.298	0.776	0.298	0.780

In addition to the fact that the DC-link capacitor model appears to be the limiting factor, a significant oscillation was observed around 350kHz. The origin of this oscillating component is most likely due to an additional filter capacitor placed between the battery and the inverter that is not accounted for in the simulation model.

4.5 Impact of using SiC-MOSFET

As the title of this thesis suggests, and as stated in the goals of this report, one main objective is to investigate how a change from Si-IGBTs into SiC-MOSFETs would impact the inverter.

So far in this thesis it is stated that for the simulations performed, the choice of IGBT or MOSFET technology will not affect the ripple results in any significant manner. To prove this, simulations were performed using the basic IGBT model, which is used throughout this thesis, as well as a corresponding MOSFET model characterized to match the transistors in Table 3-5.

Figure 4.65 and Figure 4.66 shows the current waveforms through the upper transistor and diode for one of the phase-legs using IGBTs as well as MOSFETs. As expected, the diodes and the transistors each carry current in opposite directions. By observing these figures, it can be seen that there is no apparent difference in the current through the transistor or diode depending on which transistor that is used, since both amplitude and shape remain unchanged.

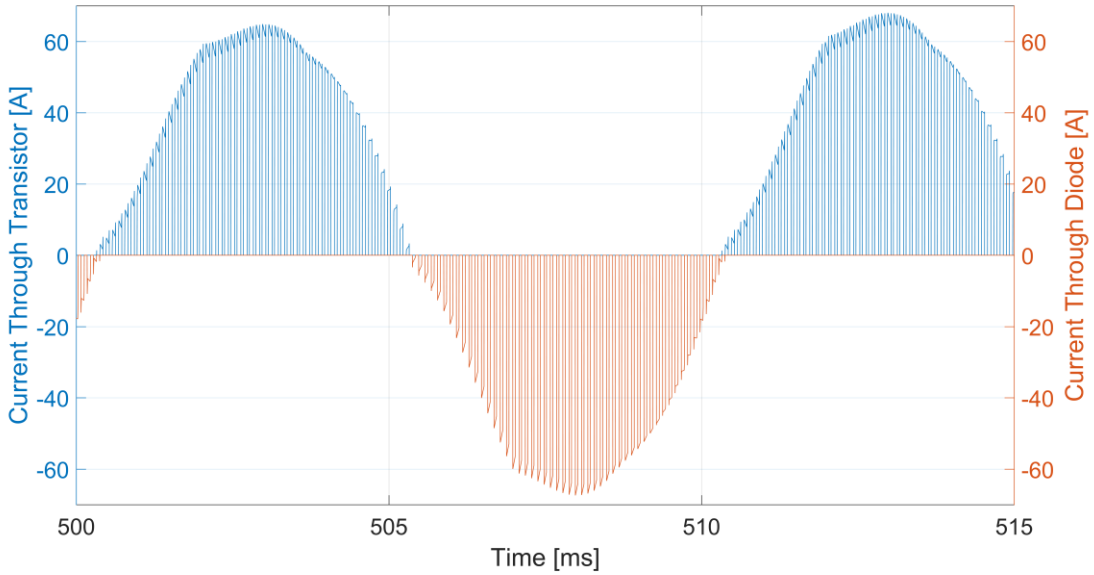

Figure 4.65. Current through the IGBT and the diode for the upper switch of the first phase leg.

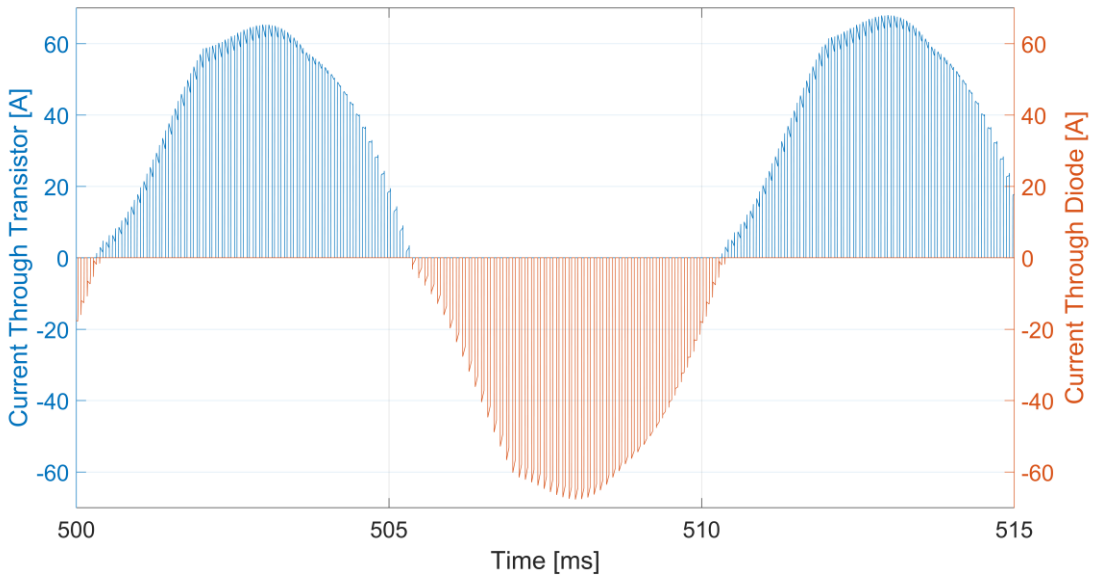

Figure 4.66. Current through the MOSFET and the diode for the upper switch of the first phase leg.

To further validate that the choice of transistor technology will not affect the ripple levels, the DC-link voltage and current FFT is plotted in Figure 4.67 and Figure 4.68, respectively. In these figures, the frequency spectrum for the MOSFET has been shifted 3 kHz for easier comparison without overlap. As seen, there is no significant difference in neither voltage nor current ripple which again shows that the difference in IV-characteristics between MOSFETs and IGBTs plays no significant role in the DC-link ripple magnitude or distribution.

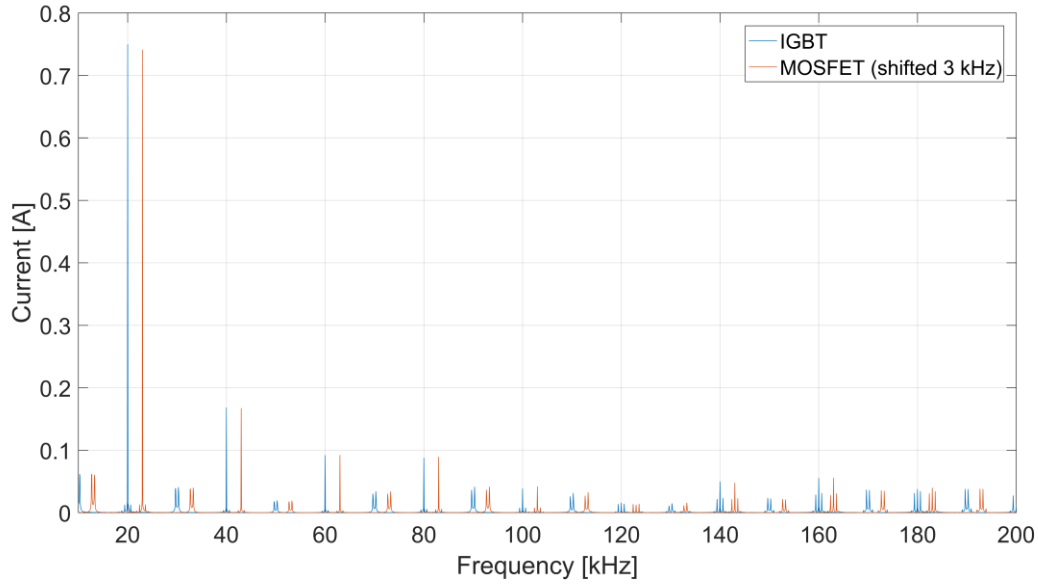

Figure 4.67. FFT of DC-link current using both IGBT and MOSFET.

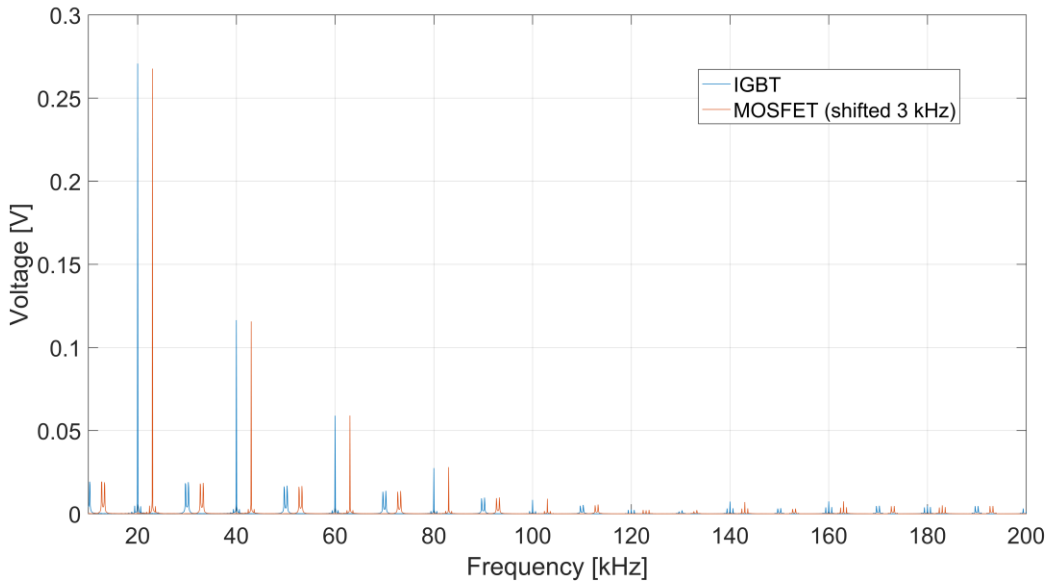

Figure 4.68. FFT of DC-link voltage using both IGBT and MOSFET.

As no major difference could be seen in the DC-link voltage or current FFT, the resulting THD-values correspond well between the two technologies, see Table 4-12.

Table 4-12. Ripple THD for DC-link voltage and current using IGBT and MOSFET.

	Ripple THD	
	Voltage [V]	Current [A]
IGBT	0.317	0.831
MOSFET	0.314	0.824

Even though the MOSFET-technology itself did not affect the DC-link ripple, it stills enables other ways to improve the DC-link ripple. Due to the fact that SiC-MOSFETs has a higher electrical field breakdown strength it can be used in higher voltage applications than conventional Si-MOSFETs. The use of SiC-MOSFETs in this drivetrain would allow the use of higher switching frequencies due the lower switching times and switching losses. This will in turn lead to lower ripple, see Section 4.3.3, and it will also give the possibility to use a smaller DC-link capacitor. Worth noting here is that an increased switching speed and switching frequency could cause more problems with transients during switching which is not addressed in this thesis due to limited transistor models.

Asides from increasing the switching frequency in order to lower the ripple levels, SiC-MOSFETs are in some cases considered as they have the potential to decrease the inverter losses. Using what was stated in Section 2.10, a basic visualization of the difference in losses between the two transistors (see Table 3-5) can be done. Figure 4.69 uses (2.15) to (2.18) to show how the conduction losses change as a function of the current and how the switching losses change as a function of the switching frequency for the two transistors. The switching losses are linear to the switching frequency and the SiC-MOSFET will always have lower losses than the Si-IGBT for a given switching frequency. The conduction losses however, contain both linear and quadratic components. Even though the IGBT has lower on-state resistance, the losses in the IGBT will be greater than in the MOSFET due to the on-state forward voltage drop. However, at a certain current the losses in the MOSFET will become greater than the IGBT losses due to the higher on-state resistance of the MOSFET.

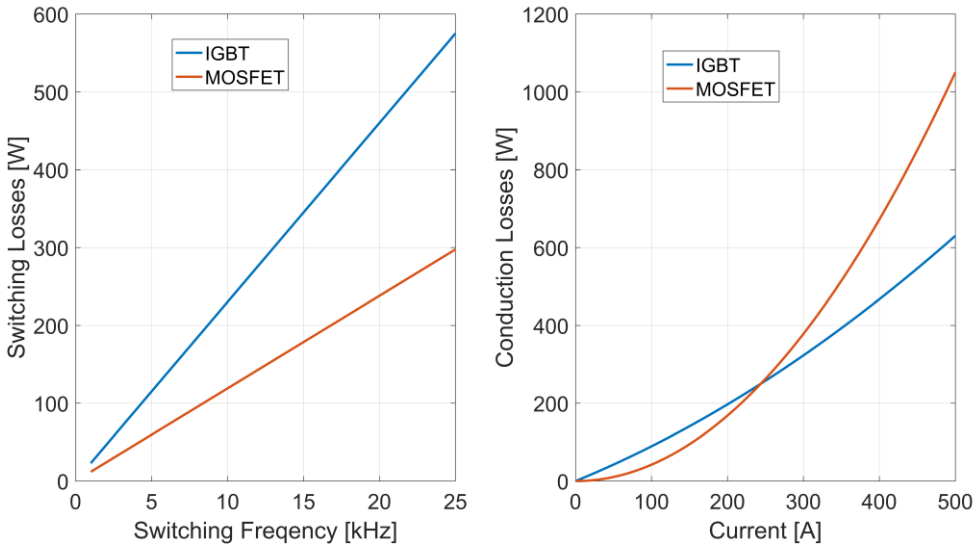

Figure 4.69. Switching losses (left) and conduction losses (right) for both IGBT and MOSFET.

A more complete comparison between the losses in a MOSFET and IGBT can be seen in Figure 4.70 where the switching and conduction losses are combined for a few operating points. As noted by the vertical dashed lines, the current at which point the losses in the MOSFET exceeds the losses in the IGBT is increased when the switching frequency increases since the difference in switching losses become more and more prominent. In this thesis, the current levels has been lower than the turning-point seen in these calculations and according to this, SiC-MOSFETs would be a preferred choice when it comes to efficiency and power loss.

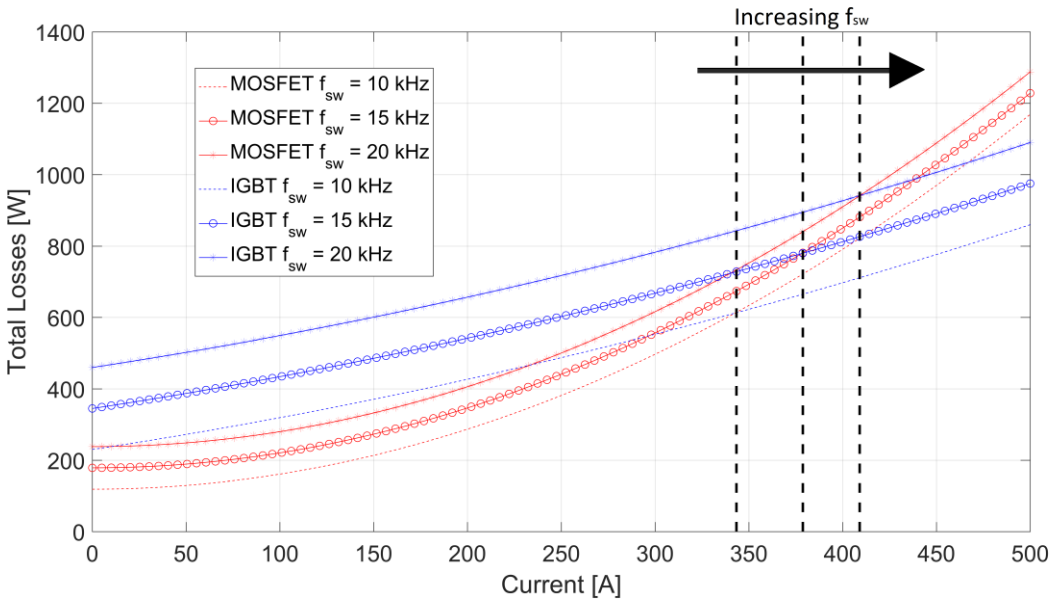

Figure 4.70. Combined switching and conduction losses for both IGBT and MOSFET.

To compare whether or not switching to SiC-MOSFETs will yield in any decrease in total loss for the current simulation model, the losses in the same transistor/diode-pair as seen in Figure 4.65 and Figure 4.66 was calculated by multiplying the sum of the current through the diode and the transistor with the voltage over the components. By averaging these results over the same interval gives the average power loss for one transistor/diode-pair. Worth noting here is the fact that neither model include a calculation the switching losses. As both devices go from blocking to conducting in one simulation time-step, the exact value of the losses is not correct, but it provides a measurement of the conduction losses for both technologies. The resulting average power loss of the IGBT and MOSFET for three different operating points can be seen in Table 4-13. For all three operating points, the losses could be reduced by 25 % to 40 %, thus indicating that even though the influence of the switching losses could not be simulated, the difference in conduction loss between the two transistors is still significant. In line with what can be seen in Figure 4.70, the smallest loss reduction can be noted for the second operating point where the current was largest due to the highest machine torque.

Table 4-13. Average total losses in one switch using two transistor models.

	Average Losses [W]	
Operating Point	**IGBT**	**MOSFET**
1500 rpm - 20 Nm	18.4	12.4
1500 rpm - 40 Nm	36.4	27.0
3000 rpm - 20 Nm	18.3	11.3

4.5.1 Reverse conduction

Another important factor when moving from Si-IGBT to SiC-MOSFET technology is the possibility to use reverse conduction to decrease the inverter losses even further. As described in Section 2.9.1, reverse conduction uses the fact that MOSFETs can conduct current in both directions when a positive gate voltage is applied. Thus, the current can be carried by the transistor in both directions and does not have to go flow the anti-parallel diode which typically has higher losses due to its forward voltage drop.

Simulations were performed not only to investigate what effect the reverse conduction had on the losses, but also to verify that doing so did not affect the DC-link ripple. As the basic MOSFET simulation model does not support reverse conduction, a workaround was created by adding a second MOSFET at each component mounted in the opposite direction. These MOSFETs will emulate the 3rd quadrant behavior of the MOSFET and are controlled by the same control signal as the original transistors. For comparisons with previous simulations, the currents through the original transistor were added together with the reverse conduction transistor to produce a total transistor current. The simulation model can be seen in Figure 4.71 where two anti-parallel transistors are placed at each switch.

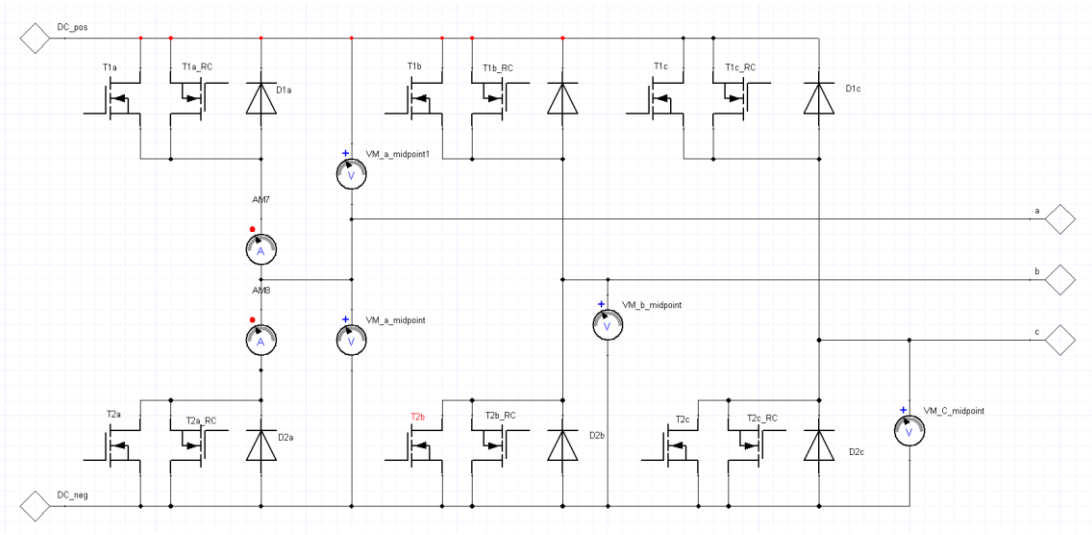

Figure 4.71. Implementation of reverse conduction using basic MOSFET models.

The resulting current waveforms of the reverse conduction simulations can be seen in Figure 4.72. At first glance, the current waveforms are very similar to the results without reverse conduction. A zoom of one negative current cycle is shown in Figure 4.73 and visualizes that for the periods where the diode previously conducted all current, the MOSFET now conduct the bulk of the current. The reason for the diode conducting all the current at the beginning and the end of each switching cycle is due to the blanking time of the inverter which inhibits the transistors from conducting.

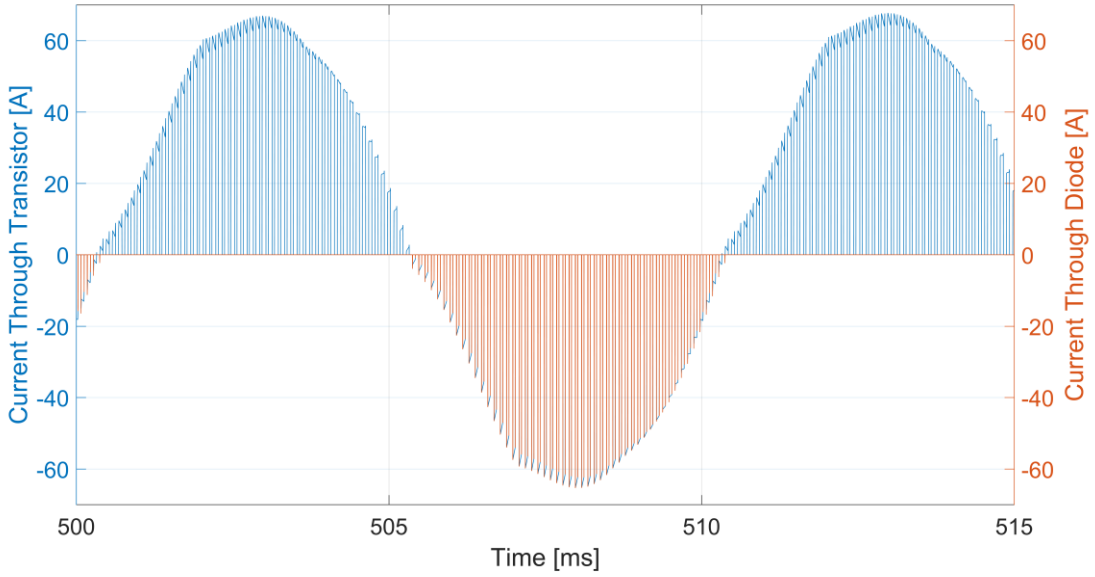

Figure 4.72. Current through MOSFET respectively diode for the upper switch of the first phase leg using reverse conduction.

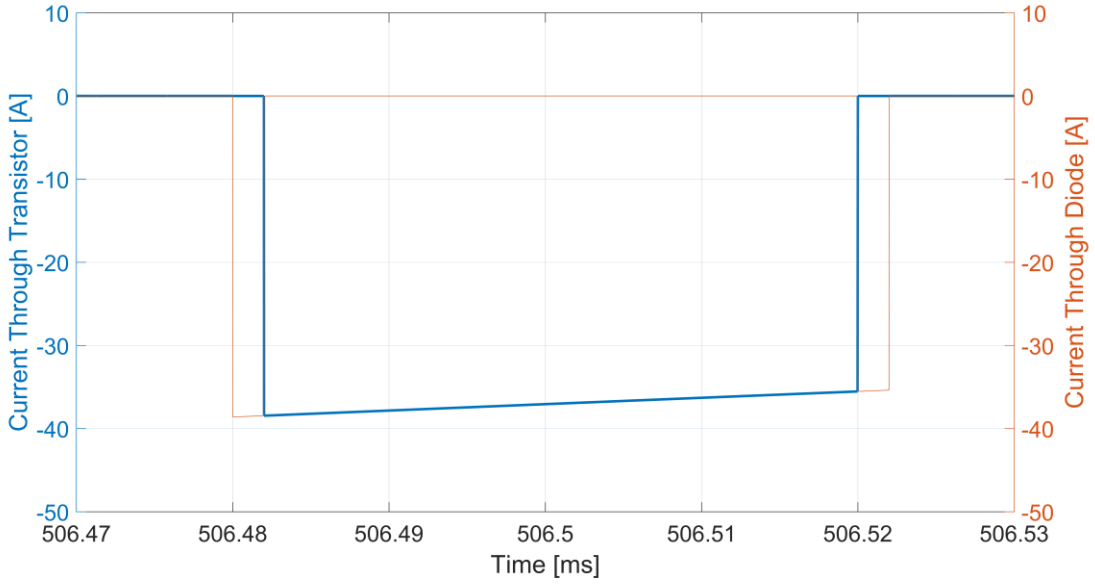

Figure 4.73. Close-up of current through MOSFET respectively diode for the upper switch of the first phase leg using reverse conduction.

By observing the DC-link voltage and current FFT in Figure 4.74 and Figure 4.75, no difference in DC-link ripple can be seen between using MOSFETS with reverse conduction or not. Even though the current commutates between the diode and the MOSFET during the negative current cycles, the DC-link ripple is not affected. The reason for this is the fact that the total current through each switch remains the same and only the distribution between the diode and transistor is changed. If the inverter is seen as a black box and observed from the DC-link, this change cannot be seen in the DC-link current.

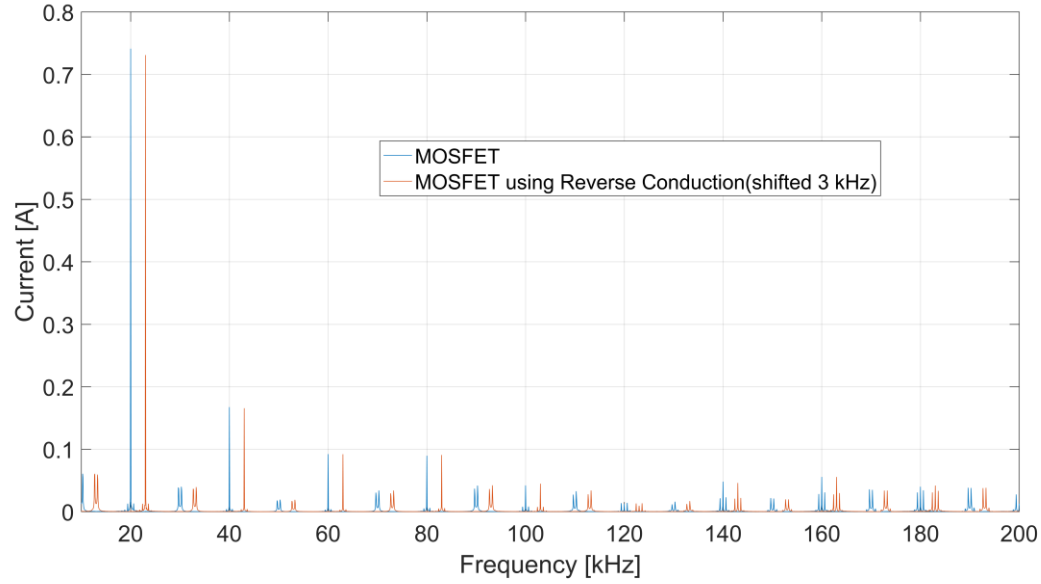

Figure 4.74. FFT of DC-link current using MOSFET, both with and without reverse conduction.

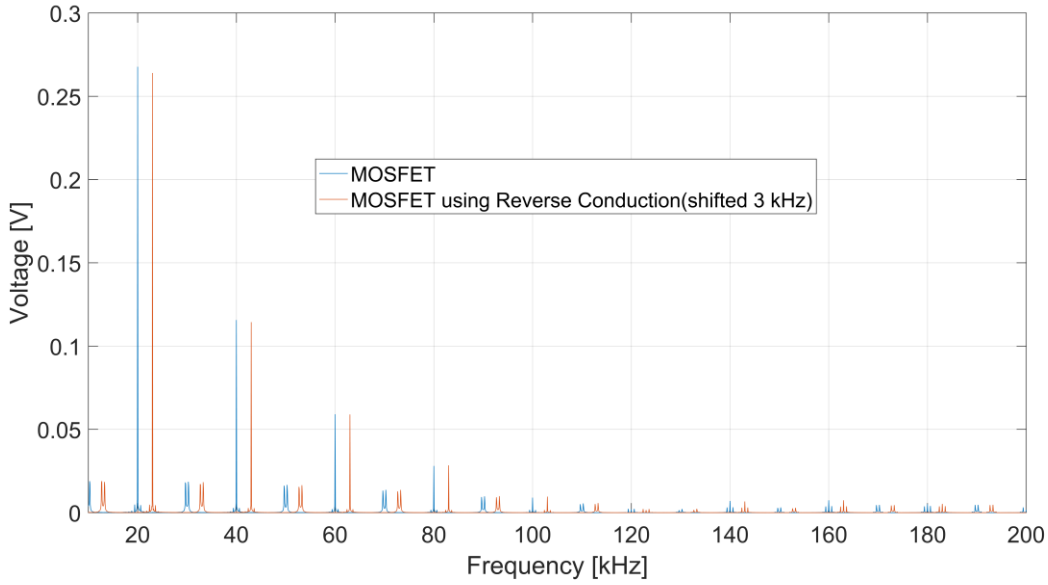

Figure 4.75. FFT of DC-link voltage using MOSFET, both with and without reverse conduction.

Since there was no difference in the harmonic content of the DC-link current and voltage, the ripple THD for voltage and current was calculated to 0.31 respectively 0.81, see Table 4-14.

Table 4-14. Ripple THD for DC-link voltage and current using three different transistor models.

	Ripple THD	
	Voltage [V]	Current [A]
IGBT	0.317	0.831
MOSFET	0.314	0.824
MOSFET + rev. cond.	0.310	0.810

The most important reason for using MOSFETs with reverse conduction is to reduce the loss when the current is flowing in the negative direction through each phase leg. The loss when using reverse conduction was calculated in the same way as described for the IGBT and the MOSFET in Section 4.5. The combined average losses of one transistor and anti-parallel diode using reverse conduction was calculated for three operating points, see Table 4-15. The losses could be reduced by between 60 % to 75 % compared to using the Si-IGBT. Worth noting is that the second operating point no longer showed the smallest reduction as it did in Section 4.5. This shows that even though the loss in the MOSFET increase more with increased current than the loss of the IGBT, the difference can be compensated by reverse conduction which decreases the losses in the anti-parallel diode. These results show that by using reverse conduction, the total loss of the inverter can be reduced. It should be noted that the losses are shifted from the diode to the MOSFET which concentrates the losses in one location.

Table 4-15. Average total losses in one switch using three transistor models.

	Average Losses [W]		
Operating Point	**IGBT**	**MOSFET**	**MOSFET + rev. conduction**
1500 rpm - 20 Nm	18.4	12.4	6.9
1500 rpm - 40 Nm	36.4	27.0	11.8
3000 rpm - 20 Nm	18.3	11.3	5.0

4.5.2 Analysis of SiC-MOSFET

Aside from the aspects not considered in this thesis, e.g. switching transients over the transistors, SiC-MOSFET appears to be a beneficial choice for this drivetrain. Not only does SiC have the potential to increase the efficiency of the inverter by reducing the losses in the transistor/diode-pair, but it also enables different inverter operating points. It gives the possibility to increase the switching frequency while still maintaining a high efficiency. An increased switching frequency can not only decrease DC-link ripple as previously shown, but it may also enable the use of a smaller DC-link capacitor. By combining this with lower inverter losses a smaller inverter can be designed which reduces both weight, volume and gives decreasing cooling needs.

5 Conclusion

The purpose of this thesis was to simulate the DC-link ripple emitted by the inverter in a PMSM-drivetrain, to investigate the dependence on certain parameters, to evaluate the difference between Si-IGBT and SiC-MOSFET, and to reflect on the obtained results and their possible implications in designing future inverters for use in EV/HEVs.

Different modelling techniques were evaluated and it was concluded that a basic system-level transistor model was sufficient for the DC-link ripple investigations in question. More advanced models that better reproduce switching transients introduced more complexity to the system, putting them out of the scope of this thesis due to increased simulation time. It has also been shown, through comparison with measurements, that the inverter simulation model used is able to reproduce the distribution of the resulting DC-link current ripple with approximately 5 % accuracy on the fundamental components. However, a better DC-link capacitor model is required to gain better accuracy in the DC-link voltage ripple. When using the system-level transistor models, it was also concluded that there was no distinguishable difference in DC-link voltage and current ripple between Si-IGBT and SiC-MOSFET technologies as a function of their different voltage-current behaviours. Although the use of SiC-MOSFETs enables the use of higher switching frequencies which results in lower overall ripple components and in turn enables the use of a smaller DC-link capacitor. However, the benefits of using SiC-MOSFETs does not end there; for the transistors investigated in this thesis, the MOSFETs proved to decrease the losses by approximately 30 % at the evaluated operating points. The losses could be reduced by approximately 35 % on average by implementing reverse conduction which also proved not to have any impact on DC-link ripple levels.

The two most prominent factors that affect the DC-link ripple were found to be the operating point (speed and torque of the machine) and the switching frequency. The speed of the machine mainly affected the ripple distribution where a higher speed produced more low-frequency components in the total ripple. On the other hand, an increase of the switching frequency decreased the ripple levels overall, although due to the relatively low resonance frequency of the DC-link capacitor, the decrease in total DC-link ripple subsided after 20 kHz.

Upon what was discussed in this thesis it can be concluded that developing a simulation model that can predict the DC-link current and voltage ripple accurately can be a very helpful tool when designing systems. By knowing the predicted ripple levels, adjusting parameters to minimize ripple allows for better dimensioning of ripple dependent components. In particular, this is true for the DC-link capacitor which constitutes a large part of the total weight and volume of the inverter, thus being able to minimize the size of the capacitor. These improvements could help to accelerate the transition into EV/HEV due to smaller and more sustainable inverters.

5.1 Proposal for Future Work

There are two main fields to which improvements could be proposed; Transistor modelling and DC-link capacitor modelling. For the transistor modelling, the need to investigate the impact of the switching behaviour is apparent. Especially as the effect of the transients would most likely increase with the introduction of SiC-MOSFETs due to faster switching and thus higher current derivatives. In addition to this, a more detailed transistor model is required to better determine inverter switching losses.

The second area is the DC-link capacitor model where multiple ways to model the capacitor were analysed. The comparisons done with actual measurement values indicated that the DC-link voltage ripple was not as accurately reproduced as the current ripple. Something that most likely indicates that a better model of the DC-link capacitor is necessary. Measurements could be performed on the DC-side of the capacitor while injecting a known current signal with varying frequency on the inverter side to be able to describe the transfer function between the ripple current and voltage ripple at the different frequencies.

The mentioned should be performed in order to get better accuracy in determining expected DC-link ripple levels injected from the inverter. To reproduce the total system behaviour, it needs to be combined with more detailed battery, cable and machine models.

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Appendix A – Simulink Control System

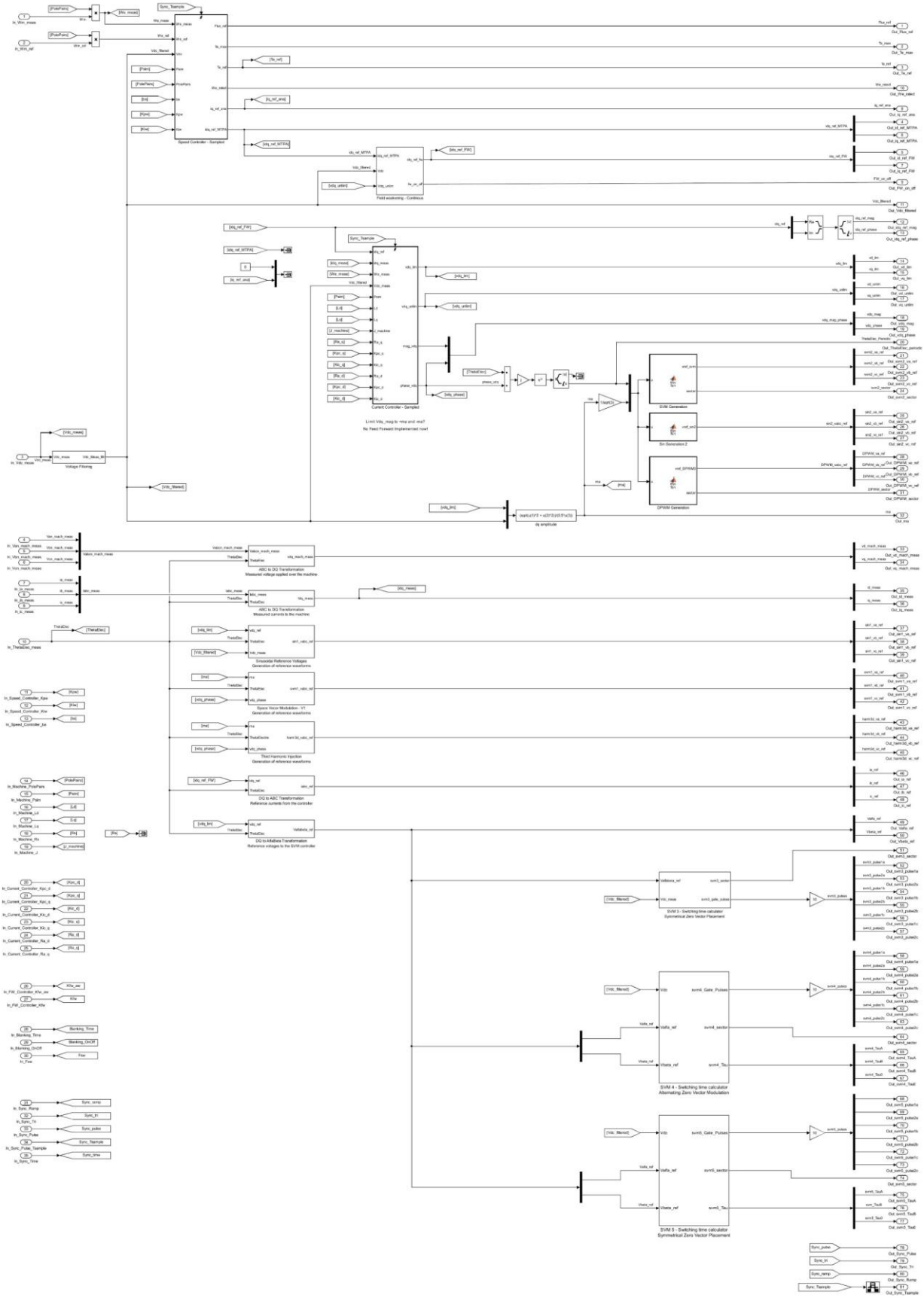

Figure A.1. Entire Simulink control system.

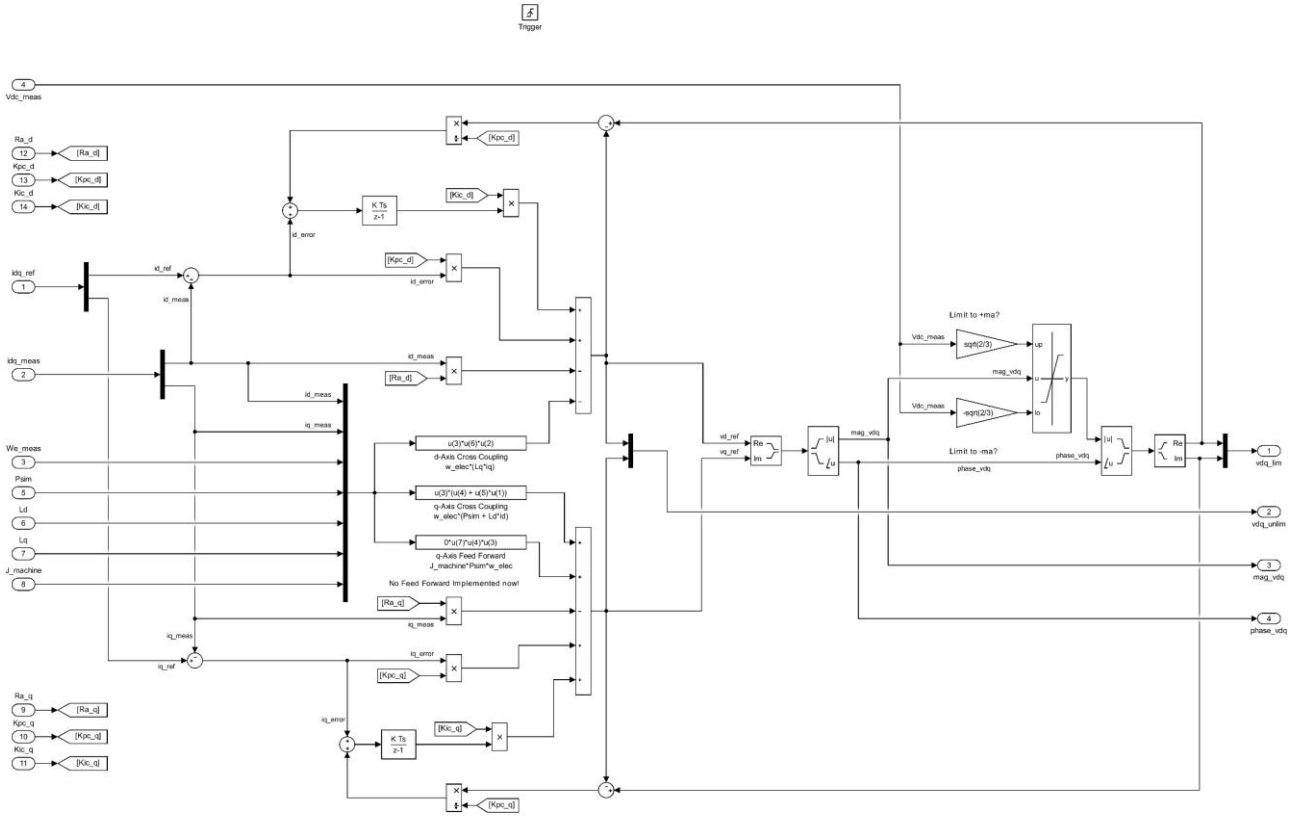

Figure A.2. Simulink current controller.

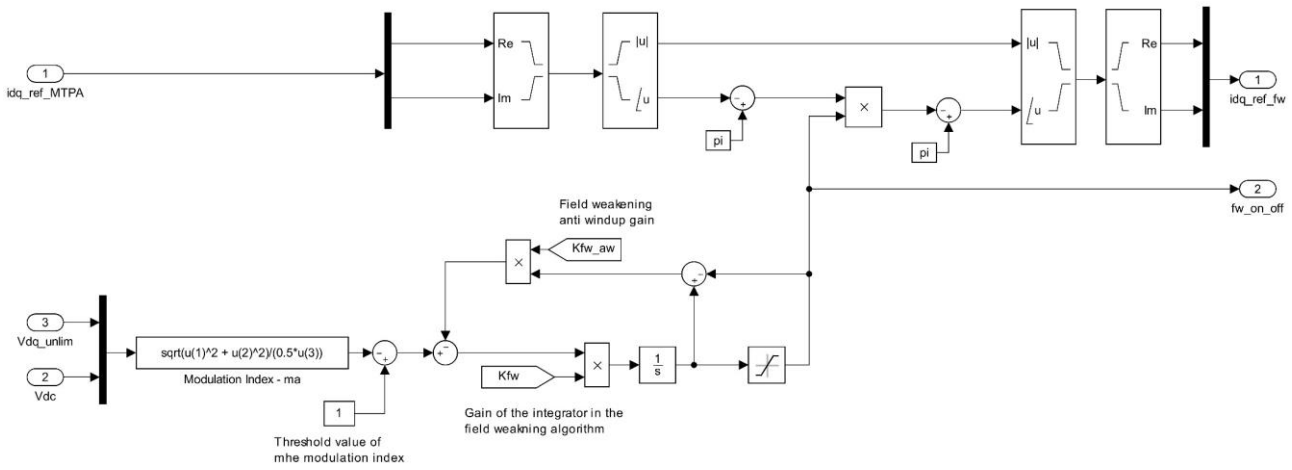

Figure A.3. Simulink field weakening algorithm.

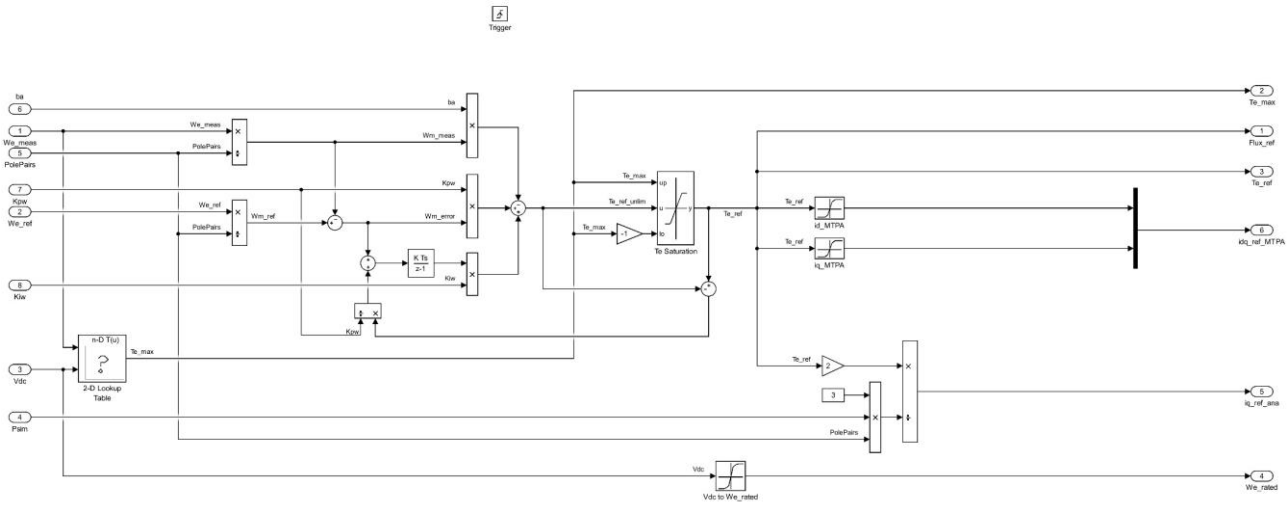

Figure A.4. Simulink speed controller.

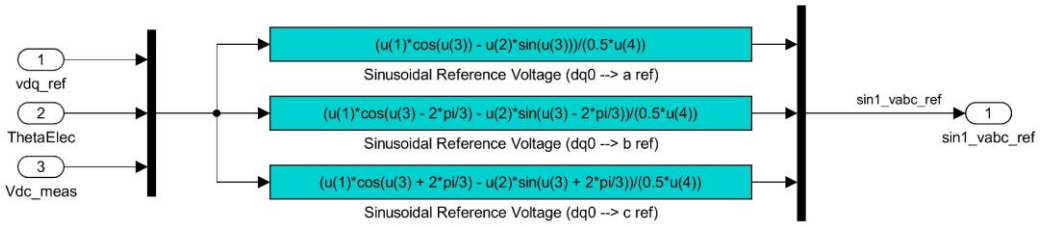

Figure A.5. Simulink PWM sinusoidal reference signal calculation.

Appendix B – Drivetrain rig

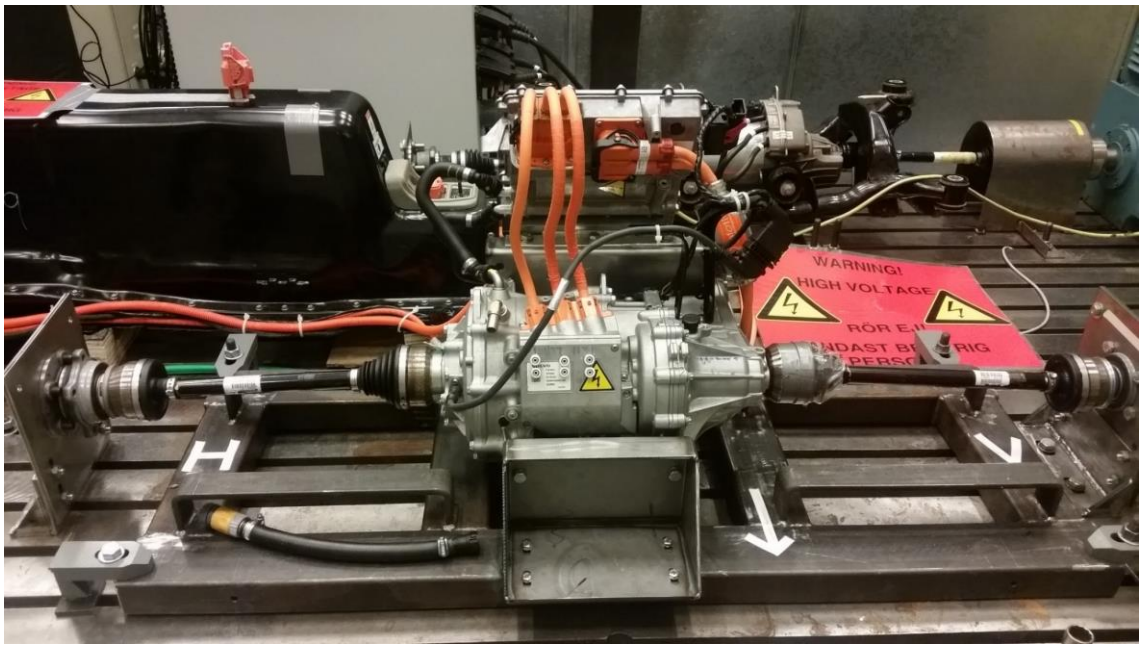

Figure B.1. Drivetrain rig at Chalmers.

Figure B.2. Braking DC-machine.

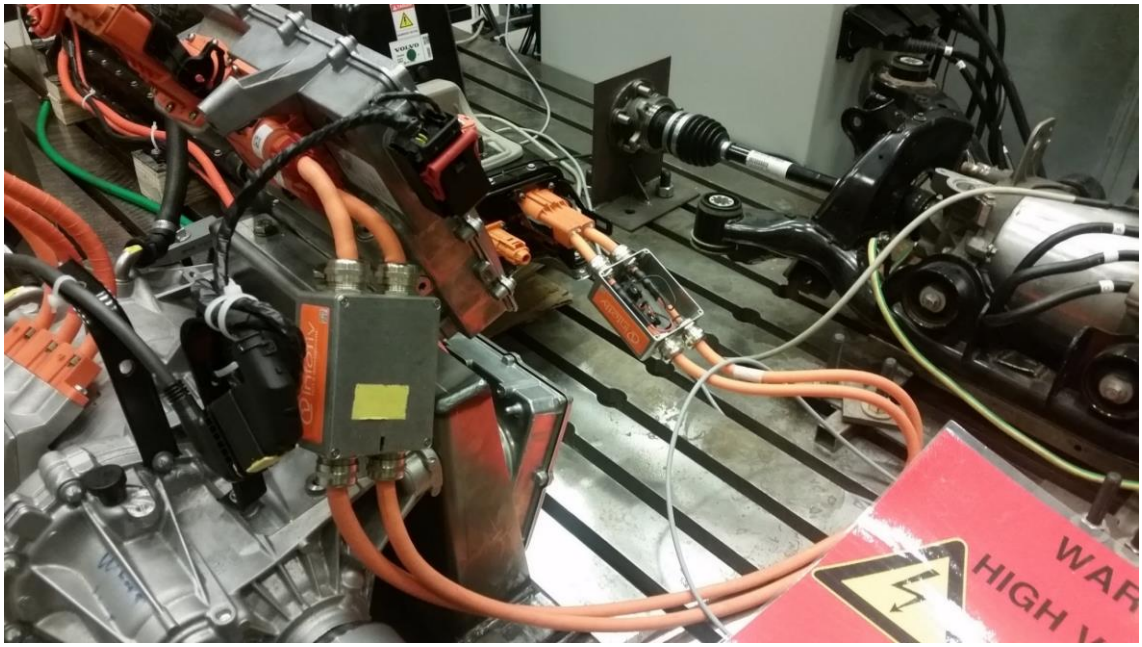

Figure B.3. Breakout-box on high-voltage battery output.

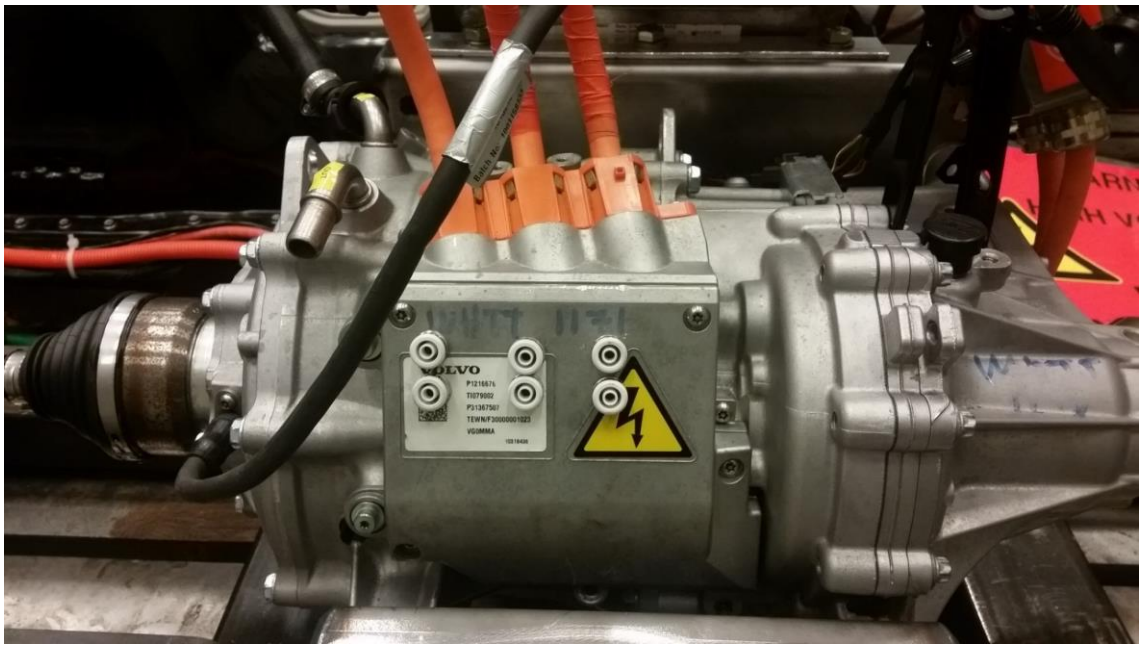

Figure B.4. Output voltage measurement points (white) and AC output cables (orange).

Appendix C – Ramp_Iinv MATLAB-script

Supply the Inverter Current and time vector to create a new inverter current that has a rise/fall time supplied starting at the indices specified.

```
function [Iinv_ramp] = Ramp_Iinv(Iinv,Rise_time,time)

Indices = 0;

for n = 2:length(Iinv(:,1))
if abs(Iinv(n,1)-Iinv(n-1,1))>1
    Indices = [Indices, n-1];
end
end

Indices = Indices(2:end);
Iinv_ramp = Iinv;
no_points = round(Rise_time/((time(end)-time(end-1))/1000))+1;

i=1;
while i < length(Iinv)
    a = i;
    if any(a==Indices)
        new_values = linspace(Iinv(a),Iinv(a+1),no_points)';
        Iinv_ramp = [Iinv_ramp(1:a-1); new_values; Iinv_ramp(a+no_points:end)];
        i = a+no_points;
    end
    i = i+1;
end
```

Appendix D – SpikKiller MATLAB-script

Removes voltage transients in the DC-link voltage.

- Output is the "filtered DC-link voltage" where transients are removed.
- Inputs are the original DC-link Voltage (Vdc), maximum allowed derivative of the voltage (der_limit) and the convergence limit (conv_limit)

```
function [Vdc_filt]=SpikKiller(Vdc,der_limit,conv_limit)

    n = length(Vdc);
    Vdc_filt = Vdc;

    i = 1;
    while i < n-2
        if abs(Vdc(i+1)-Vdc(i))>der_limit % If any step exceeds the
                                          % derivative limit
            k = 1;
            while abs(Vdc(i+k)-Vdc(i))>conv_limit && i+k<n % Looking for
                                                          % the index at
                                                          % which the
                                                          % voltage
                                                          % returns to a
                                                          % value within
                                                          % the
                                                          % convergence
                                                          % limit of the
                                                          % voltage
                                                          % previous to
                                                          % the
                                                          % transient.
                k=k+1;
            end
        Vdc_filt(i:i+k)=linspace(Vdc(i),Vdc(i+k),length(Vdc(i:i+k)))';
        i = i+k-1;
        end
        i = i+1;
    end

end
```