Thesis for The Degree of Doctor of Philosophy

# Nonlinear Modeling of FETs for Microwave Switches and Amplifiers

Ankur Prasad


Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience (MC2)
Chalmers University of Technology
Göteborg, Sweden, 2017

**Nonlinear Modeling of FETs for Microwave Switches and Amplifiers**

Ankur Prasad



ISBN 978-91-7597-648-8

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny series nr 4329
ISSN 0346-718X

Technical report MC2-373
ISSN 1652-0769
Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience - MC2

Chalmers University of Technology
SE-412 96 Göteborg, Sweden
Phone: +46 (0) 31 772 1000

Printed by Chalmers Reproservice
Göteborg, Sweden 2017

To Vihaan, Shobhit, Vatsal, Shlok, Agastya, Ananya,
And to all the kids in this world!!

*Stay hungry, stay foolish.*

- The Whole Earth Catalog, 1971

# Abstract

The exponential growth in wireless systems require rapid prototyping of radio frequency circuits (RF) using computer-aided design (CAD) enabled models. Most of the RF circuits (e.g. switches, amplifiers, mixers, etc.) use transistors as their active component for a variety of key functions. This thesis deals with application-oriented empirical modeling of high electron mobility transistors (HEMTs) for RF switches and amplifiers.

Transistors used in switching and resistive mixer circuits are typically intrinsically symmetrical around the gate. Therefore, a symmetrical small-signal model is proposed, which mirrors the transistor behavior as its source and drain terminals are interchanged. The proposed model allows a significant reduction in the number of measurements required to extract the model parameters with a minimum compromise in accuracy. The proposed small-signal equivalent circuit is extended to create a symmetrical nonlinear transistor model. It is shown that only one current and one charge expression is sufficient to model the overall nonlinear characteristics of a symmetrical transistor. The method is demonstrated first with a GaAs transistor and then extended to a GaN device, where a new symmetrical nonlinear current model is proposed.

Transistors also show trapping effects caused by the capture of electrons (and holes) in energy levels within the bandgap. This deviates the high frequency operation of a transistor from its dc-IV characteristics. Therefore, a new model based on Shockley-Read-Hall (SRH) theory is presented to correctly model the trapping effects. The proposed model differentiates the trap potential and how the trapped electrons modulate the current in a transistor. Furthermore, high power transistors often have field-plates to relax peak electric-fields, which influence both the number and distribution of the trapped electrons. Therefore, the proposed model is also used to investigate the effect of field-plates on the trapping, showing an interesting trade-off between the trap potential and modulation of the current by the trapped electrons. The investigation also opens a scope to build a trap model scalable with respect to the field-plate dimensions in GaN HEMTs.

In this work, the modeling procedures, although exemplified using GaN and GaAs HEMTs for switches and amplifiers, can be applied equally well for other FET technologies e.g., Si, SiC, GaAs, InP, and other application areas e.g. mixers, oscillators. The work has shown that by incorporating physical information in the modeling, simpler models with improved accuracy can be developed which can reduce time-to-market for new products.

**Keywords:** HEMT, model, symmetry, trap, GaAs, GaN, nonlinear model, small-signal model, symmetrical model, trap model, field-plate.

# List of Publications

## Appended Publications

This thesis is based on work contained in the following papers:

[A] **A. Prasad**, C. Fager, M. Thorsell, C. M. Andersson, and K. Yhland, "Symmetrical Large-Signal Modeling of Microwave Switch FETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 8, pp. 1590 - 1598, 2014.

[B] **A. Prasad**, C. Fager, M. Thorsell, C. M. Andersson, and K. Yhland, "Symmetrical Modeling of GaN HEMTs," Proc. *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1 – 4, San-Diego, USA, 2014.

[C] **A. Prasad**, M. Thorsell, K. Yhland, and C. Fager, "Symmetry based Nonlinear Model for GaN HEMTs," Proc. *10th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 85 – 88, Paris, France, 2015.

[D] **A. Prasad**, M. Thorsell, H. Zirath, and C. Fager, "Accurate Modeling of GaN HEMT RF Behavior Using an Effective Trapping Potential," accepted for publication in *IEEE Transactions on Microwave Theory and Techniques*, 2017.

[E] **A. Prasad**, M. Thorsell, H. Zirath, and C. Fager, "Analyzing The Back-Gating Effect in GaN HEMTs with Field-Plates Using an Empirical Trap Model," submitted to *IEEE Microwave and Wireless Components Letters*, 2017.

## Other Publications

The following paper has been published but is not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.

[F] **A. Prasad**, M. Thorsell, and C. Fager, "Behavioral Modeling of Traps in GaN HEMTs," *Swedish Microwave Days*, Linköping, 2016.

## Thesis

[G] **A. Prasad**, "Symmetrical FET Modeling," *Tekn. Lic. Thesis*, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, 2014.

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [G]. Figures, tables and text from [G] may therefore be fully or partly reproduced in this thesis.

# Notations and Abbreviations

## Notations

| | |
|---|---|
| $a_T$ | Thermal model Parameter |
| $C_{ds}$ | Intrinsic drain-source capacitance |
| $C_{gd}$ | Intrinsic gate-drain capacitance |
| $C_{gs}$ | Intrinsic gate-source capacitance |
| $C_m$ | Intrinsic transcapacitance dependent on gate-source voltage for constant drain-source voltage |
| $C_m^+$ | Intrinsic transcapacitance dependent on gate-source voltage for constant gate-drain voltage |
| $C_m^-$ | Intrinsic transcapacitance dependent on gate-drain voltage for constant gate-source voltage |
| $C_{pd}$ | Drain pad capacitance |
| $C_{pg}$ | Gate pad capacitance |
| $C_T$ | Trap capacitance in equivalent circuit model |
| $C_{th}$ | Thermal sub-circuit capacitance |
| $E_A$ | Energy level of acceptor type trap |
| $E_C$ | Conduction band energy level |
| $E_V$ | Valence band energy level |
| $FoM_{Johnson}$ | Johnson's figure of merit |
| $g_m$ | Intrinsic transconductance dependent on gate-source voltage for constant drain-source voltage |
| $g_m^+$ | Intrinsic transconductance dependent on gate-source voltage for constant gate-drain voltage |
| $g_m^-$ | Intrinsic transconductance dependent on gate-drain voltage for constant gate-source voltage |
| $I_C$ | Capture current |
| $I_{ds}$ | Drain-source current |
| $I_{ds}^{\text{Core}}$ | Core drain-source current with low trapping and thermal effect |
| $I_{ds}^{\text{Meas}}$ | Measured drain-source current with low trapping and thermal effect |

| | |
|---|---|
| $I_E$ | Emission current |
| $i_T$ | Trap current |
| $k_B$ | Boltzmann Constant |
| $L_d$ | Drain inductance |
| $L_g$ | Gate inductance |
| $L_s$ | Source inductance |
| $P_{in}$ | Incident power |
| $P_{refl}$ | Reflected power |
| $Q_d$ | Drain charge expression |
| $Q_d^{\mathrm{sym}}$ | Symmetrical drain charge expression |
| $Q_g$ | Gate charge expression |
| $Q_s^{\mathrm{sym}}$ | Symmetrical source charge expression |
| $R_{th}$ | Thermal sub-circuit resistance |
| $R_d$ | Drain resistance |
| $R_g$ | Gate resistance |
| $R_s$ | Source resistance |
| $T_A$ | Ambient temperature |
| $V_0$ | Maximum trap potential |
| $V_{ds}$ | Intrinsic drain-source voltage |
| $v_{ds}$ | RF intrinsic drain-source voltage |
| $V_{DS}$ | DC intrinsic drain-source voltage |
| $V_{ds,(i)}$ | Intrinsic in-pulse drain-source voltage |
| $V_{ds,(q)}$ | Intrinsic quiescent drain-source voltage |
| $V_{dse}$ | Extrinsic drain-source voltage |
| $V_{gd}$ | Intrinsic gate-drain voltage |
| $v_{gd}$ | RF intrinsic gate-drain voltage |
| $V_{GD}$ | DC intrinsic gate-drain voltage |
| $V_{gde}$ | Extrinsic gate-drain voltage |
| $V_{gs}$ | Intrinsic gate-source voltage |
| $v_{gs}$ | RF intrinsic gate-source voltage |
| $V_{GS}$ | DC intrinsic gate-source voltage |
| $V_{gs,(i)}$ | Intrinsic in-pulse gate-source voltage |
| $V_{gs,(q)}$ | Intrinsic quiescent gate-source voltage |
| $V_{gse}$ | Extrinsic gate-source voltage |
| $v_I$ | Input potential to trap equivalent |
| $v_T$ | Trap potential in trap equivalent |
| $V_T^{\mathrm{Eff}}$ | Effective trap potential |
| $V_{T,(00)}$ | Trap potential at $V_{gs} = V_{ds} = 0$ V |
| $\mathbf{Y_{int}}$ | Intrinsic admittance matrix for small signal model |
| $\mathbf{Y_{int}^{sym}}$ | Intrinsic admittance matrix for symmetrical small-signal model |
| $\alpha$ | Modulation factor |
| $\epsilon$ | Modeling error |
| $\epsilon^-$ | Modeling error contribution in negative $V_{ds}$ region |

| | |
|---|---|
| $\epsilon^+$ | Modeling error contribution in positive $V_{ds}$ region |
| $\tau$ | Current source delay |
| $\omega_0$ | Characteristic trap frequency |

# Abbreviations

| | |
|---|---|
| 2-DEG | 2-Dimensional Electron Gas |
| ACPR | Adjacent Channel Power Ratio |
| ANN | Artificial Neural Network |
| BJT | Bipolar Junction Transistor |
| BPF | Band Pass Filter |
| BSIM | Berkeley Short-channel IGFET Model |
| BTE | Boltzmann Transport Equation |
| CAD | Computer Aided Design |
| DC | Direct Current |
| DUT | Device Under Test |
| FET | Field Effect Transistor |
| FP | Field Plate |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| GPS | Global Positioning System |
| GSM | Global System for Mobile communications (originally Groupe Spécial Mobile) |
| HEMT | High Electron Mobility Transistor |
| IGFET | Insulated Gate Field Effect Transistor |
| InP | Indium Phosphide |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| LNA | Low Noise Amplifier |
| LSNA | Large Signal Network Analyzer |
| MESFET | MEtal Semiconductor Field Effect Transistor |
| mHEMT | Metamorphic High Electron Mobility Transistor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NL | Nonlinear |
| PA | Power Amplifier |
| pHEMT | Pseudomorphic High Electron Mobility Transistor |
| PIV | Pulsed-IV |
| RADAR | Radio Detection And Ranging |
| RF | Radio Frequency |
| SRH | Shockley-Read-Hall |
| VCCS | Voltage Controlled Current Source |
| VNA | Vector Network Analyzer |

# Contents

# Chapter 1

# Introduction

The United Nations resolution (A/HRC/32/L.20) "*The promotion, protection and enjoyment of human rights on the Internet*" adopted in June $27^{\text{th}}, 2016$ condemns internet access disruptions as a violation of human rights. Thus, the resolution seeks to make the internet (a global system of interconnected computer networks, where a part of the communication is wireless) a basic right for humans. The internet is but one, albeit prominent, of the various wireless systems existing in the world today. Other examples of wireless systems include TV/Radio broadcast, mobile communication, radio imaging and sensing, GPS navigation, Radars, atmospheric monitoring, etc. Many of these wireless systems have evolved from being a niche product to a product intended for mass market, leading to a multifold rise in the number of devices. A short time-to-market is crucial in large-volume production. This can be addressed with fast prototyping, quick testing, and first-time success for radio frequency (RF) circuit designs.

RF circuits usually contain a transceiver (or transmitter/recevier) as illustrated in Fig. 1.1. Most of the RF circuit blocks (marked in Fig. 1.1) use transistors as their active component for a variety of key functions, including the transformation of DC current to RF current (oscillation), the conversion of a signal at one frequency to another (multiplication, mixing), the redirection of a signal (switching), and the intensification and replication of a signal (amplification). Therefore, transistors often are a critical part of the circuit design. A computer-aided design (CAD) enabled transistor model with accurate prediction of its behavior allows designers to quickly test and optimize the circuit performance. This significantly reduces the number of design iterations required and shortens the turn-around time for fabricating the RF circuits.

More often than not, transistors operate as an amplifier or in a similar operating region. Therefore, more focus is given to model the transistors in such operating conditions as illustrated in Fig. 1.2. However, every model has its constraints and its validity can only be guaranteed within a certain range of e.g., bias points, frequencies, temperatures, or output power levels. Therefore, there is a need for the development of transistor models suited for their target applications.

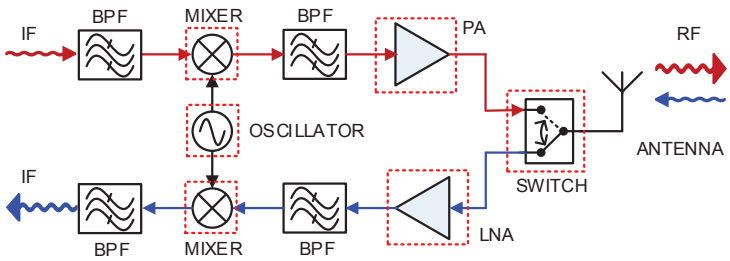



Figure 1.1: Illustration of an RF transceiver block-chain. Transistors are used in all of the marked circuit blocks (mixer, amplifiers, oscillator, switch).

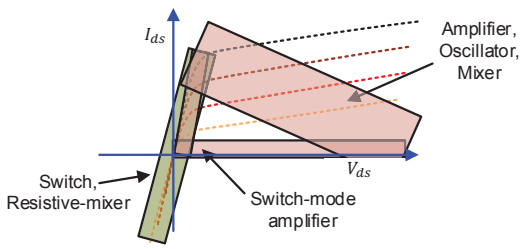



Figure 1.2: Illustration of operating region on the current-voltage (IV) characteristics of a transistor for different circuit blocks.

## 1.1 Application oriented modeling

Modern micro- and millimeter-wave circuits use different transistor technologies depending on the requirements from the intended application. Gallium Arsenide (GaAs) pseudomorphic high electron mobility transistors (pHEMTs) have been extensively used for military, communication, automotive, instrumentation applications [1]. The heterostructure in the device allows the formation of 2-dimensional electron gas (2-DEG) as shown in Fig. 1.3. The 2-DEG enables higher mobility and saturation velocity due to confinement of electrons [2, 3]. Apart from the use in amplifier circuits, GaAs pHEMTs are also used for switching functions in power amplifier (PA) modules in cellular handsets [4]. Unlike PAs, transistors used in switches are often symmetrical around the gate as shown in Fig. 1.3. This physical symmetry can be used to simplify the modeling procedure for HEMTs and other symmetrical field-effect transistors e.g. GaAs metamorphic HEMTs (mHEMTs), MOSFETs, InP HEMTs etc., except power FETs with field-plates and non-FP devices, where the gate-drain separation is typically larger than the gate-source separation [5–9].

Apart from GaAs technology, GaN HEMTs offer a unique combination of high electron mobility and high breakdown electric field, which make them ideal for high-power RF applications [10–12]. The Johnson's figure of merit ($FoM_{Johnson}$) [13] which indicates the high-frequency performance of power devices, is significantly higher for GaN compared to GaAs, and other transistor technologies as summarized in Table 1.1. This makes GaN HEMTs a potential candidate for next generation base station transceivers, space, radar, electronic counter-measure applications, etc., [12, 14–20]. However, GaN technology is constantly evolving to achieve better performance. The varying ma-

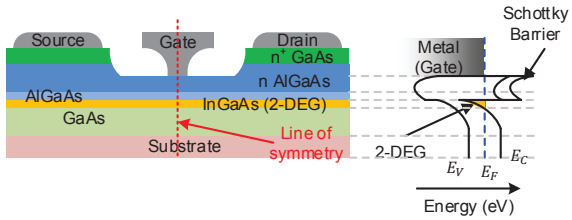



Figure 1.3: An illustration of formation of 2-dimensional electron gas (2-DEG) and symmetry in GaAs pHEMTs used in switch (and resistive mixer) circuits.

terial qualities and the growth processes often introduce trapping effects in GaN HEMTs [21,22]. These effects lead to differences in the transistor performance between the dc and high-frequency operation. Therefore, the trapping effects must also be modeled in order to correctly predict the behavior of a transistor.

Table 1.1: Johnson figure of merit for various semiconductor materials [10]

| Material | Si | GaAs | 4H-SiC | GaN |
|---|---|---|---|---|
| Breakdown electric field: $E_{br}$ ($\mathrm{MV\,cm^{-1}}$) | 0.3 | 0.4 | 3.0 | 3.3 |
| Saturation velocity: $v_{sat}$ ($10^7\,\mathrm{cm\,s^{-1}}$) | 1 | 1 | 2 | 2.5 |
| Johnson's figure of merit: $FoM_{Johnson}$ | 1 | 2.7 | 20 | 27.5 |

$FoM_{Johnson} = \frac{E_{br} v_{sat}}{2\pi}$ [13]; specified $FoM_{Johnson}$ values are relative to Si.

## 1.2 Transistor models for circuit simulation

Different kinds of transistor models are available depending on how they are derived. The majority of these are either physics-based models (e.g. [6,23–25]), surface potential-based compact models. (e.g. [26–28]), empirical models (e.g. [29–34]), table-based models (e.g. [35,36]), or artificial neural network (ANN) based models (e.g. [37–40]). On one hand, physics-based and compact models require details about the transistor to be modeled which are not commonly available. On the other hand, table-based models suffer from interpolation and extrapolation issues, and ANN-based models do not provide insights as the neurons do not contain any useful information. Empirical models, however, have been widely used for modeling high frequency transistors due to their relative simplicity and correspondence to the physical operation of a device. Fig. 1.4 illustrates a use of an empirical current model to predict the current-voltage characteristics of a transistor. Empirical models provide a good balance between the amount of prior information and the number of parameters required to build the model. Therefore continuing the tradition, this thesis focuses on empirical modeling techniques for GaAs and GaN HEMTs.

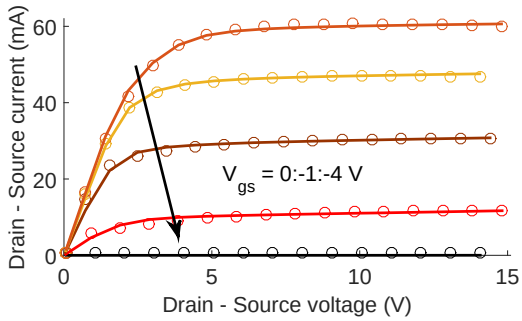



Figure 1.4: Illustration of the use of an empirical model (-) to predict measured (marker) IV-characteristics of a transistor.

## 1.3 Contributions and outline of the thesis

The thesis begins with a discussion of the empirical small signal model in Chapter 2. First, the linear operation of a transistor is analyzed for the derivation of the small-signal model. The widely used small-signal transistor model and its parameter extraction process are briefly reviewed. Thereafter, the symmetry in the transistor used in switch circuits (and resistive mixers) is considered and utilized to build a symmetrical small-signal model as proposed in [Paper A]. This is followed by a corresponding simplification in the direct extraction procedure for the symmetrical model. In the end, a modified optimization based extraction is presented wherein the symmetry is used to improve the small signal extraction result for a symmetrical GaN HEMT as proposed in [Paper B].

Chapter 3 begins with a discussion on the nonlinear operation of a transistor. Thereafter, how to build a nonlinear model from the small-signal parameters is discussed. A number of available nonlinear current models are presented including a new current expression to model the symmetrical GaN HEMTs presented in [Paper C]. Further on, the use of one charge expression to model the reactive part of a symmetrical transistor as proposed in [Paper A] is also described. Thereafter, a number of model validation techniques are briefly reviewed.

Trapping effects in transistors are discussed in Chapter 4 with a focus on GaN HEMTs. A number of trap models including the proposed model in [Paper D] are presented outlining their strengths and weaknesses. An analysis of a field-plated GaN device using the proposed trap model is presented in [Paper E] in order to identify the parameters for scalable models.

Finally, Chapter 5 summarizes the important conclusions from the work presented in earlier chapters. It also provides recommendations on how the empirical models can be further improved for future research into micro- and millimeter-wave wireless technologies and utilized in developing next-generation wireless applications.

# Chapter 2

# Small-Signal FET Model

## Linear Model and Parameter Extraction Techniques

Transistors are the building blocks for active microwave circuits like amplifiers, oscillators, mixers, frequency multipliers etc. The behavior of a transistor is inherently nonlinear. However, if the excitation is small enough, linear approximation can be used to define the operation of a transistor around an operating point (or bias point). This approximation can be modeled by an equivalent circuit consisting of linear elements like resistors, capacitors, inductors, voltage-controlled current sources (VCCSs), etc. The linear equivalent circuit is called the small-signal model. There are two important benefits of the small-signal models. First, the small-signal behavior can be easily measured by commonly available measurement setups like a vector network analyzer (VNA). This makes the availability of the measurements for the model extraction easy to obtain. Second, the small-signal model at different bias points forms a basis for the empirical nonlinear models, as will be described in Chapter 3. Moreover, the small-signal models are a good approximation for the transistor when used with small excitation. Therefore, they can be directly used to predict the transistor behavior in the design and analysis of applications like small-signal amplifiers, low-noise amplifiers, etc.

This chapter presents an overview of the small-signal model and its extraction procedure for a field-effect transistor (FET). The chapter begins with a brief discussion on the small-signal approximation of the transistor behavior and the derivation of the ideal small-signal model in Section 2.1. Thereafter, the widely used small-signal model and its extraction technique are discussed in Section 2.2 and 2.3, respectively. A brief discussion on the unique physical feature and operation of the symmetrical transistors is given in Section 2.4. In Section 2.5, a new symmetrical small-signal equivalent circuit is presented to model symmetrical devices. This is followed by a discussion on the required modification in the extraction procedure for the symmetrical model in Section 2.6.

## 2.1 FET operation under small excitations

A FET operates using a combination of a vertical and a horizontal electric field controlled by the gate-source and drain-source voltages respectively. The current flows from the drain to the source terminal when a drain-source voltage is applied. The current flows along a path called the channel as illustrated in Fig. 2.1. The physical thickness of the channel is fixed, but its electrical thickness is varied by the gate-source voltage. The channel conductivity is dependent on the electrical thickness [41]. Thus, a small change in the gate-source voltage causes a change in the channel conductivity leading to a large variation in the current flowing from the drain to source terminals. Although the channel properties depend on the FET technology, the transistor operation is more or less similar irrespective of the technology. Therefore, the small-signal models discussed in this chapter can be used for all FET transistor technologies.

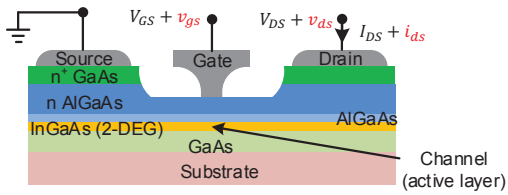



Figure 2.1: Illustration of the small-signal operation of a GaAs pHEMT. The small change in the gate-source voltage ($v_{gs}$) changes the number of carriers in the channel by ($q$) and the current flowing through the channel by ($i_{ds}$).

The drain-source current through a transistor depends on both the applied gate-source and drain-source voltages. This current-voltage relationship can be safely assumed to be both continuous and infinitely differentiable and is defined by a function $f : \mathbf{R^2} \rightarrow \mathbf{R}$ as:

$$I_{ds}\left(V_{gs}, V_{ds}\right) = f\left(V_{gs}, V_{ds}\right) \tag{2.1}$$

The function $f\left(V_{gs}, V_{ds}\right)$ in (2.1) can be any function (linear or nonlinear) dependent on the two bias voltages. Taylor series expansion can be used to find the current and voltage relationship around an operating point $(V_{GS}, V_{DS})$ is given by

$$\begin{aligned} I_{ds}\left(V_{gs}, V_{ds}\right) = f\left(V_{GS}, V_{DS}\right) &+ \left(V_{gs} - V_{GS}\right) \frac{\partial f\left(V_{gs}, V_{ds}\right)}{\partial V_{gs}}\bigg|_{V_{GS}, V_{DS}} \\ &+ \left(V_{ds} - V_{DS}\right) \frac{\partial f\left(V_{gs}, V_{ds}\right)}{\partial V_{ds}}\bigg|_{V_{GS}, V_{DS}} \\ &+ \frac{1}{2!}\Bigg(\left(V_{gs} - V_{GS}\right)^2 \frac{\partial f^2\left(V_{gs}, V_{ds}\right)}{\partial V_{gs}^2}\bigg|_{V_{GS}, V_{DS}} \\ &\quad + 2\left(V_{gs} - V_{GS}\right)\left(V_{ds} - V_{DS}\right) \frac{\partial f^2\left(V_{gs}, V_{ds}\right)}{\partial V_{gs} V_{ds}}\bigg|_{V_{GS}, V_{DS},} \\ &\quad + \left(V_{ds} - V_{DS}\right)^2 \frac{\partial f^2\left(V_{gs}, V_{ds}\right)}{\partial V_{ds}^2}\bigg|_{V_{GS}, V_{DS}}\Bigg) + \cdots \end{aligned} \tag{2.2}$$

The higher order terms in (2.2) can be neglected for small excitations. Therefore, the drain-source current $i_{ds}$ around any given DC operating point $(V_{GS}, V_{DS})$ can be approximated by a linear function as

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) &= I_{ds}(V_{gs}, V_{ds}) - f(V_{GS}, V_{DS}) \\ &= \left.\frac{\partial f(V_{gs}, V_{ds})}{\partial V_{gs}}\right|_{V_{GS}, V_{DS}} (V_{gs} - V_{GS}) \\ &\quad + \left.\frac{\partial f(V_{gs}, V_{ds})}{\partial V_{ds}}\right|_{V_{GS}, V_{DS}} (V_{ds} - V_{DS}) \\ &= g_m(V_{GS}, V_{DS}) \cdot v_{gs} + g_{ds}(V_{GS}, V_{DS}) \cdot v_{ds} \qquad (2.3a) \end{aligned}$$

$$\text{where} \qquad v_{gs} = V_{gs} - V_{GS} \qquad \text{and} \qquad v_{ds} = V_{ds} - V_{DS}. \qquad (2.3b)$$

This gives a small-signal representation of the current expression with one current source ($g_m$) and conductance ($g_{ds}$) at the operating point $(V_{GS}, V_{DS})$. The small-signal equivalent circuit for the drain-source current in (2.3a) is illustrated in Fig. 2.2.

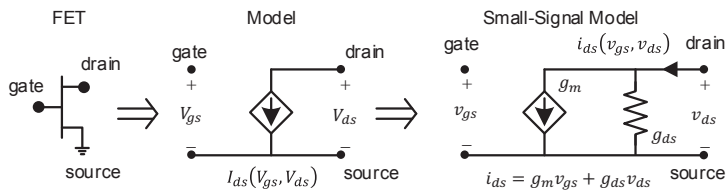



Figure 2.2: A FET where the drain-source current is represented by a nonlinear function $f(\bullet)$ (center) and an ideal small-signal representation (right). $i_{ds}$ is the net current flowing through the drain terminal.

### Ideal transistor example

The analysis used to identify the small-signal expression for the drain-source current in (2.3) can also be used for the gate-source current to fully describe the two-port behavior. Therefore, a two port node admittance matrix can be built for an ideal transistor shown in Fig. 2.2 and is given by

$$\begin{bmatrix} i_{gs} \\ i_{ds} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ g_m & g_{ds} \end{bmatrix}}_{\mathbf{Y}_{\mathbf{int}}^{\mathbf{ideal}}} \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix}. \qquad (2.4)$$

The node admittance matrix ($\mathbf{Y}_{\mathbf{int}}^{\mathbf{ideal}}$) in (2.4) is directly related to the scattering matrix parameters (S-parameters). The relation between node admittance matrix and S-parameters is given by [42]

$$\mathbf{S} = (\mathbf{Y_0} + \mathbf{Y})^{-1} (\mathbf{Y_0} - \mathbf{Y}) \qquad (2.5)$$

where $\mathbf{S}$ is the S-parameter matrix, $\mathbf{Y}$ is the admittance matrix and $\mathbf{Y_0}$ is the diagonal matrix of port admittances. The ease of measuring S-parameters at RF frequencies and their conversion using (2.5) allow the extraction of model parameters of the small-signal equivalent circuit using analytical techniques.

## 2.2 Commonly used small-signal model

The voltage-controlled current source shown in Fig. 2.2 is the most important element of the transistor model. The VCCS models the amplification or control of the RF signal flowing through a transistor. However, a transistor also consists of parasitics along with the VCCS which influence the electrical response. Therefore, the ideal model (see Fig. 2.2) is not sufficient to predict the electrical behavior of a transistor. Hence, an extensive equivalent circuit is considered to model the observed small-signal behavior at any operating point. The equivalent circuit consists of two parts: (a) intrinsic, and (b) extrinsic. The intrinsic part represents the active area of a transistor and the related parameters are bias-dependent in nature. The extrinsic part, however, denotes the connection to the active area and the related parameters are bias-independent in nature. In this section, the commonly used small-signal equivalent circuit for FETs is discussed.

### 2.2.1 Intrinsic small-signal model

A transistor channel in the active area is surrounded by many physical features which change the frequency response of the transistor. The channel itself is a collection of charges (electrons/holes) in the active layer (see Fig. 2.1). Therefore, capacitances $C_{gs}$ and $C_{gd}$ represent the formation of the channel (the VCCS and conductor shown in Fig. 2.2) in the active layer. A capacitor $C_{ds}$ represents the depletion region between the drain and source nodes. Fig. 2.3 illustrates a commonly used intrinsic model for a FET which is valid up to very high frequencies (e.g. up to 110 GHz in [43]). The transcapacitance $C_m$ models the delay in the response of the channel current to the gate-source voltage [21]. This model along with some variations has been extensively used in previous modeling and circuit design work [29, 43–56].

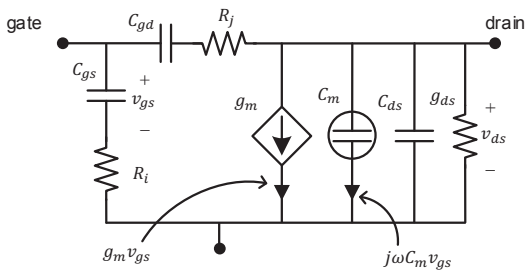



Figure 2.3: The intrinsic small-signal FET model [43].

The small-signal model shown in Fig. 2.3 is given by the intrinsic admittance relation between the small-signal gate-source and drain-source currents and voltages as

$$\begin{bmatrix} i_{gs} \\ i_{ds} \end{bmatrix} = \underbrace{\begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ g_m + j\omega C_m - Y_{gd} & Y_{ds} + Y_{gd} \end{bmatrix}}_{\mathbf{Y_{int}}} \begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix} \tag{2.6}$$

where

$$Y_{gs} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_i} \tag{2.7a}$$

$$Y_{gd} = \frac{j\omega C_{gd}}{1 + j\omega C_{gd} R_j} \tag{2.7b}$$

$$Y_{ds} = j\omega C_{ds} + g_{ds}. \tag{2.7c}$$

The admittance relation in (2.6) is used to analytically calculate the values of the model parameters, and will be discussed later in Section 2.3.

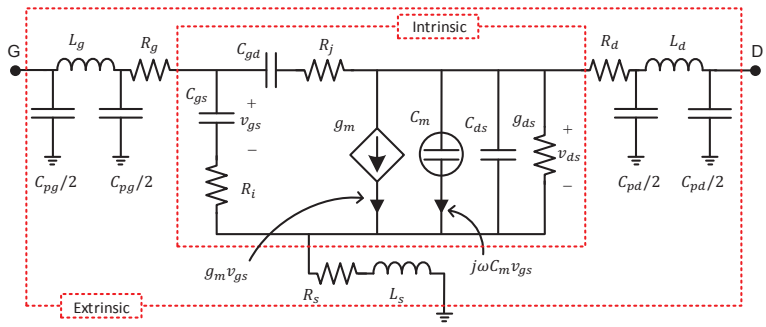



Figure 2.4: The traditional small-signal model of a common source field-effect transistor containing 16 parameters and the extrinsic and intrinsic reference planes. The intrinsic part represents the active area and the extrinsic part represents the connection to the former.

### 2.2.2 Extrinsic parameters

The 16-parameter model illustrated in Fig. 2.4 shows both the intrinsic and extrinsic small-signal model parameters. The extrinsic parameters represent the connection from the external contacts (or probe pads) to the active intrinsic device. Several variations have been proposed for the extrinsic model. Some variation of the extrinsic network depends on the pad structure [44,53,57–59], whereas other variations depend on the package used in the transistor [60,61].

## 2.3 Small-signal model parameter extraction

The small-signal properties of a transistor can be directly measured using a vector network analyzer (VNA). The two-port admittance parameters can then be computed using (2.5), which are then used to extract the small-signal model parameters. There exists two different methods of extraction: (a) direct extraction and (b) optimizer based extraction, which are briefly explained in this section.

### 2.3.1 Direct Extraction

The direct extraction method is based on the direct determination of a parameter value at a specific frequency or an averaged value over a frequency

range [59]. The method uses reverse analytical calculations to obtain the model parameter values from the admittance parameters [43,44,62,63], where the latter can be directly obtained from the measured S-parameters using (2.5). In this method first the extrinsic parameters are extracted and de-embedded, followed by the extraction of the bias-dependent intrinsic parameters.

### Extrinsic parameters

The extrinsic parameters need to be extracted and deembedded from the measurements in order to get the behavior of the intrinsic device. The direct extraction technique uses cold-FET (zero drain-source voltage) measurements under two sets of conditions [43, 44, 59, 64, 65]. The two chosen conditions enable simplification of the small-signal equivalent circuit models as shown in the Fig. 2.5. The subthreshold condition is used to determine the pad-capacitances ($C_{pg}$ and $C_{pd}$), whereas, the forward gate bias condition is used to determine other extrinsic parameters shown in Fig. 2.4.

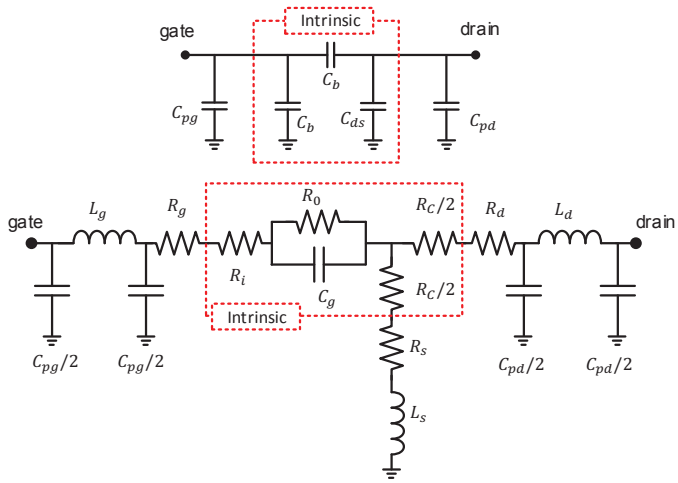



Figure 2.5: Small-signal equivalent circuit in the subthreshold condition $V_{ds} = 0$ V, $V_{gs} \ll V_{\text{threshold}}$ (top) used for the gate and drain pad capacitances extraction and the forward gate bias condition $V_{ds} = 0$ V, $V_{gs} \gg 0$ V (bottom) used for the extraction of other extrinsic parameters.

By first extracting the extrinsic parameters allows their effect to be deembedded from the network response of the intrinsic device [44]. The deembedding of extrinsic parameters shifts of reference plane from the extrinsic nodes to the intrinsic nodes as illustrated in Fig. 2.4.

### Intrinsic parameters

The intrinsic parameters of the commonly used small-signal model (see Fig. 2.3) are extracted directly from the deembedded network response using the admittance relation of the equivalent circuit [43]. The effect of the intrinsic parameters $R_i$ and $R_j$ mainly appear at very high frequencies, and therefore they are often neglected [50]. The admittance relation $\mathbf{Y_{int}}$ in (2.6) therefore

gets simplified to

$$\mathbf{Y_{int}} = \begin{bmatrix} j\omega\left(C_{gs}+C_{gd}\right) & -j\omega C_{gd} \\ g_m + j\omega\left(C_m - C_{gd}\right) & g_{ds} + j\omega\left(C_{ds}+C_{gd}\right) \end{bmatrix}. \tag{2.8}$$

The parameter values are calculated using the reverse analytical technique at each of the measured bias points, and will be later used to build a nonlinear model in Chapter 3.

### 2.3.2 Optimizer based extraction

While the direct extraction method is extensively used, higher modeling consistency can be achieved by optimizer based extraction methods [66–72]. A robust model parameter extraction and sequential model building method is presented in [67], where the model is built from a basic structure. The parameter extraction technique in [68] is based on optimization with bidirectional search with multiplane (extrinsic and intrinsic reference planes shown in Fig. 2.4) data fitting. Some methods use decomposition based optimization, where a new set of linearly independent artificial parameters are created from existing ones to extract weaker dependencies [69–72]. In [70–72], a sequential single parameter optimization technique is used which is robust against local minima. The optimization order for the sequential single parameter optimization technique is determined by the relative influence of the model parameters on the error function being minimized.

## 2.4 Symmetry in device and operation

The first field-effect transistor developed in 1952 by Shockley was symmetric around the gate [73]. The gate in the transistor is equidistant from the drain and source terminals as illustrated in Fig. 2.6. Commonly available transistors today continue to be symmetrical, except for the transistors used for high power applications [6, 74]. The benefit of the symmetry is that the transistor remains the same even when its drain and source terminals are interchanged. Although such transistors can be used in all of the circuit blocks illustrated in Fig. 1.1, switches and resistive mixers are the applications where the symmetry best can be utilized to simplify modeling and parameter extraction [49].

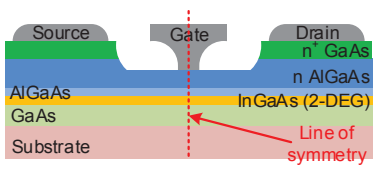



Figure 2.6: An illustration of symmetry in GaAs pHEMTs typically used in switch (and resistive mixer) circuits.

Fig. 2.7 shows an illustration of a FET operating in shunt configuration in a switch and a resistive mixer. Transistors used in switch and resistive mixer circuits are biased at zero volt at the drain ($V_{DS} = 0$ V) [75–79]. Therefore, the RF swing present in the drain terminal drives $V_{ds}$ to both the positive and

negative values over an RF cycle as illustrated in Fig. 1.2. Many models do not consider the operation in the negative $V_{ds}$ region, and therefore can not be used to design circuits (e.g. [29,80,81]). However, some models do consider the operation in the negative $V_{ds}$ region (e.g. [49, 82]). The available symmetrical models simply mirror the nonlinear current expression from the positive to the negative $V_{ds}$ region and they are discussed in Chapter 3. However the small-signal model used for the transistors, which has more or less remained the same since it was first reported in [83], can be simplified using the symmetry [Paper A].

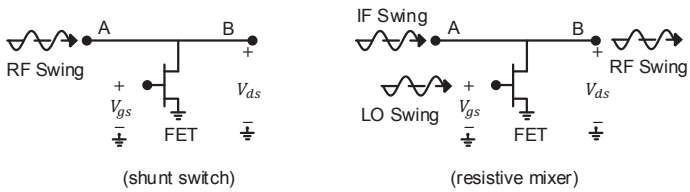



Figure 2.7: A FET operating in shunt configuration in a switch application.

## 2.5 Symmetrical intrinsic model

For a symmetrical device, the symmetry is observed along the gate as illustrated in Fig. 2.6. Hence for a three-terminal device, the two independent voltage set ($V_{gs}$, $V_{ds}$) does not make the use of the inherent symmetries and makes it difficult to simplify the model. The symmetry of a FET can be utilized by the selection of ($V_{gs}$, $V_{gd}$) as a set of two independent voltages, since the drain and source terminals are equivalent and mirror to each other [49]. Therefore, one can expect to see symmetries when the drain and source terminal are mirrored i.e. $V_{gs}$ and $V_{gd}$ are interchanged. To illustrate the symmetry in ($V_{gs}$, $V_{gd}$) bias grid, the measured drain-source current contours are shown in Fig. 2.8. The inverted symmetry between the upper left ($V_{gs} > V_{gd}$ or $V_{ds} > 0$ V) and lower right ($V_{gs} < V_{gd}$ or $V_{ds} < 0$ V) regions in $I_{ds}$ clearly shows the benefit of using the symmetrical bias grid.

In ($V_{gs}$, $V_{gd}$) control voltage set, the intrinsic parameters like ($C_{gs}$, $C_{gd}$) and ($R_i$, $R_j$) in Fig. 2.3 are interchanged whenever the drain and source terminal (or $V_{gs}$ and $V_{gd}$) are interchanged. Furthermore, the control voltage must be taken across $C_{gs}$ as well as $C_{gd}$ in order to preserve the symmetry in the VCCS. Therefore, the current source $g_m$ (see Fig. 2.3) is divided into two independent VCCS controlled by $v_{gs}$ and $v_{gd}$ respectively as [Paper A]

$$i_{ds}^{+} = g_m^{+} \cdot v_{gs} \tag{2.9a}$$

$$i_{ds}^{-} = g_m^{-} \cdot v_{gd} \tag{2.9b}$$

where

$$g_m^{+} = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{gd}=\text{const}} \tag{2.10a}$$

$$g_m^{-} = \left.\frac{-\partial I_{ds}}{\partial V_{gd}}\right|_{V_{gs}=\text{const}}. \tag{2.10b}$$

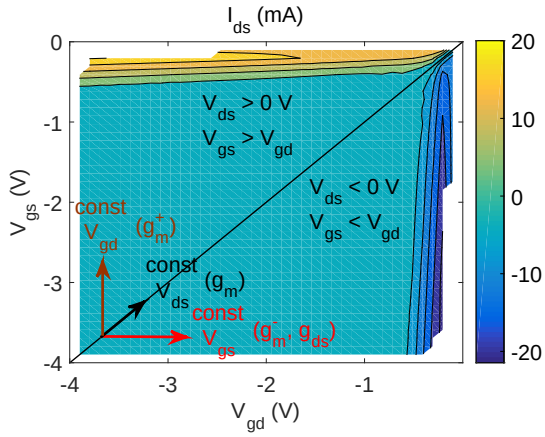



Figure 2.8: Contour plot of the drain-source current of a symmetrical GaAs FET, illustrating the direction of current derivatives for parameters $g_m$, $g_{ds}$, $g_m^+$ and $g_m^-$.

Thus, $g_m^+$ and $g_m^-$ line up with the symmetry of the device observed in the $(V_{gs}, V_{gd})$ bias grid, see Fig. 2.8. Moreover, since the FET is a three terminal device, the two current-sources $i_{ds}^+$ and $i_{ds}^-$ are sufficient to model the small-signal resistive current, thereby making $g_{ds}$ redundant. The same reasoning is applied to $C_m$ and $C_{ds}$, which are replaced by $C_m^+$ and $C_m^-$ to build the symmetrical small-signal model shown in Fig. 2.9 [Paper A]. Thus in the new model, all the intrinsic parameters exist in pairs and their derivatives align to the set of control voltages $(V_{gs}, V_{gd})$.

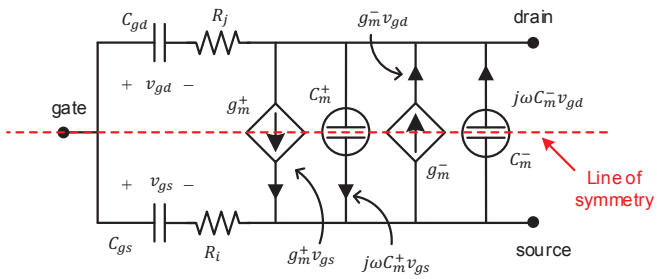



Figure 2.9: The symmetrical intrinsic equivalent circuit model for containing two pair of VCCS ($g_m^+$, $g_m^-$), and transcapacitances ($C_m^+$ and $C_m^-$) controlled by $v_{gs}$ and $v_{gd}$.

For the symmetrical equivalent circuit shown in Fig. 2.9, the admittance relation is given by

$$\mathbf{Y}_{\mathbf{int}}^{\mathbf{sym}} = \begin{bmatrix} j\omega(C_{gs}+C_{gd}) & -j\omega C_{gd} \\ j\omega(C_m^+ - C_{gd} - C_m^-) + g_m^+ - g_m^- & j\omega(C_{gd}+C_m^-) + g_m^- \end{bmatrix} \tag{2.11}$$

where $R_i$ and $R_j$ are neglected since their effects appear mainly at higher frequencies [50]. The equivalent circuit model in Fig. 2.3 and Fig. 2.9 represent the same active area, therefore, (2.8) and (2.11) give the relation between the

model parameters according to

$$g_m^- = g_{ds} \tag{2.12a}$$
$$g_m^+ = g_{ds} + g_m \tag{2.12b}$$
$$C_m^- = C_{ds} \tag{2.12c}$$
$$C_m^+ = C_{ds} + C_m. \tag{2.12d}$$

Thus, the proposed model parameters can be directly calculated from the existing model parameters.

## 2.6 Extraction of symmetrical intrinsic model

Symmetry in the device and the equivalent circuit model, shown in Fig. 2.6 and 2.9 respectively, also simplifies the parameter extraction procedure. The procedure using direct and optimizer based extraction is briefly explained in this section.

### 2.6.1 Direct extraction

The extraction of the symmetrical model parameters follows similar procedure as described in Section 2.2.2. As discussed in the previous section, the interchange of the drain and source terminals mirrors $C_{gs}$ and $C_{gd}$ as shown in Fig. 2.10. The extracted $g_m$ (and $C_m$) of the existing model shown in Fig. 2.10 also exhibits an inverted symmetry similar to the current contours (see Fig. 2.8). However, $C_{ds}$ (and $g_{ds}$) does not exhibit any feature related to the symmetry of the device.

The extracted symmetrical model parameters are shown in Fig. 2.11. It is evident that each of these parameters appear in pairs and are mirrors to each other along $V_{ds} = 0$ V. Thus, the parameters of the proposed model can be mirrored whenever the drain and source terminals (or $V_{gd}$ and $V_{gs}$) are interchanged. This essentially means that either the number of required measurement points or the number of parameters to be extracted can effectively be halved.

### 2.6.2 Optimizer based extraction

The advantages of the symmetrical intrinsic model are exploited using the optimization based parameters extraction technique in [70–72]. The intrinsic parameters at any bias point ($V_{gs} = x,\ V_{gd} = y$) are optimized together with its mirrored bias point ($V_{gs} = y,\ V_{gd} = x$) [Paper B]. The error function being minimized in the optimization process has contributions from both the regions with equal weights. Due to the symmetry, only four of the eight intrinsic parameters of the symmetrical model are extracted for a commercial GaN HEMT in [Paper B]. The modeling error ($\epsilon$) defined as

$$\epsilon = \sum_{j=1}^{2}\sum_{k=1}^{2} \frac{1}{\max |S_{jk}|^2} \sum_{i=1}^{N} \left| S_{jk}(\omega_i) - S_{jk}^{\mathrm{mod}}(\omega_i) \right|^2 \tag{2.13}$$

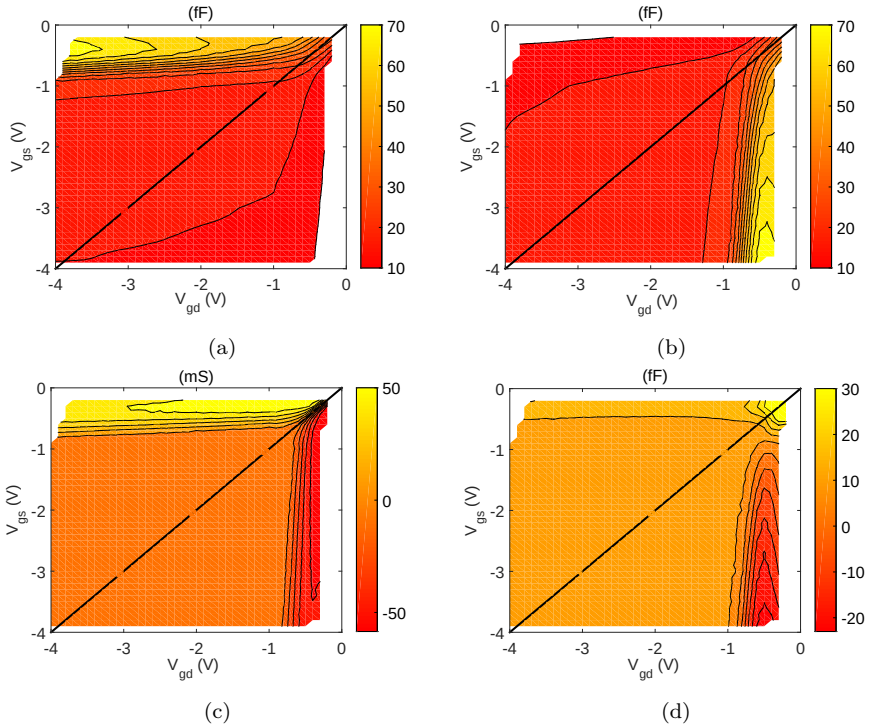



Figure 2.10: The bias dependence of the extracted intrinsic model parameters (a) $C_{gs}$ (fF), (b) $C_{gd}$ (fF), (c) $g_m$ (mS), and (d) $C_{ds}$ (fF) for the commercial GaAs HEMT used in [Paper A].

is compared for the direct and optimizer based extraction for the symmetrical model. Fig. 2.12 shows an overall improvement in the modeling error is achieved when the symmetry is used to simplify the model parameter extraction procedure.

## 2.7 Summary

This chapter has concentrated on the small-signal transistor model and its extraction procedure. It is shown that the small-signal equivalent circuit model can be simplified to reflect the symmetry of the device. The simplification allows a reduction in the number of measurements required or the intrinsic parameters to be extracted by half, while increasing the accuracy of the model for a symmetrical device.

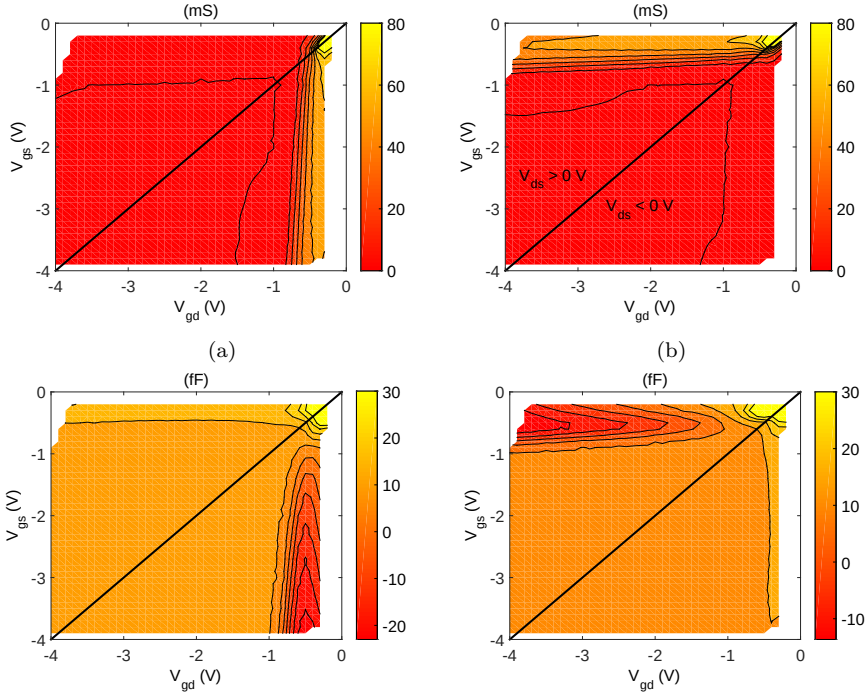



Figure 2.11: The bias dependence of the extracted symmetrical intrinsic model parameters (a) $g_m^-$ (or $g_{ds}$) (mS), (b) $g_m^+$ (mS), (c) $C_m^-$ (or $C_{ds}$) (fF), and (d) $C_m^+$ (fF) for the commercial GaAs HEMT used in [Paper A]. The parameters $C_{gs}$ and $C_{gd}$ are shown in Fig. 2.10.

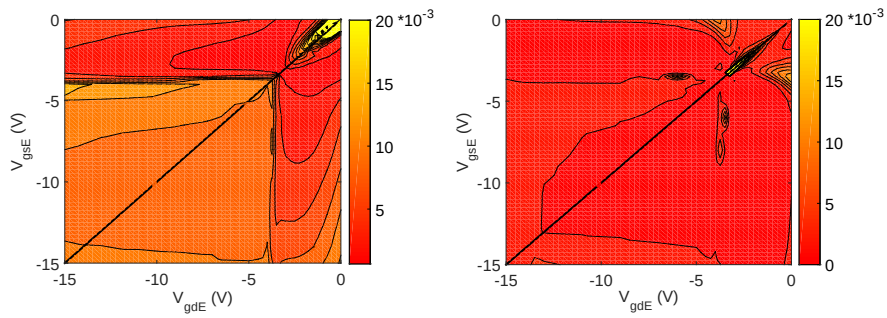



Figure 2.12: The modeling error $\epsilon$ given by (2.13) for the direct extraction (left) and the modified optimizer based extraction (right) for the GaN DUT used in [Paper B]. $V_{gsE}$ and $V_{gdE}$ are the gate-source and gate-drain voltages measured at the extrinsic plane of references.

# Chapter 3

# Nonlinear Transistor Model

### Bias-Dependent Current and Charge Relations

It has been discussed in the previous chapter that the transistor operation around an operating point can be approximated by a linear expression. However, the approximation requires the excitation signal to be small enough to neglect the higher order derivatives in (2.2). Beyond that range of excitation, the operation of a transistor is nonlinear due to its inherent physical behavior. While it may seem that the nonlinear behavior of a transistor is unnecessary and must be minimized, it is of utmost importance in circuits like mixers and frequency multipliers. Furthermore, modern communication systems use advance modulation schemes which require accurate nonlinear models to predict the output signals of a transistor.

This chapter presents an overview of the nonlinear transistor models and their extraction procedure. The chapter begins with a brief explanation on the source of nonlinear behavior of a field effect transistor in Section 3.1. This is followed by a discussion on building a nonlinear current model based on the extracted small-signal parameters in Section 3.2. Some of the existing current models for GaAs and GaN HEMTs will also be presented in this section. In Section 3.3, a brief discussion is presented on how to model the charge to correctly predict the reactive currents in a transistor. It is also shown that modeling a single charge expression is sufficient to predict the reactive currents in a symmetrical transistor. This is followed by a brief description of a self-heating model in Section 3.4. Furthermore, different measurements used for the model validation is presented in Section 3.5.

## 3.1 Transistor operation and source of nonlinearity

The operation of a FET as explained in Chapter 2 gives a simplified operation under small excitation signals. However, FETs are nonlinear electrical devices and the origin of their nonlinear behavior is illustrated for a junction-FET operation shown in Fig. 3.1 [41]. The channel is kept fully open by grounding the gate-source voltage ($V_{gs}$) (for depletion-mode transistors). $I_{ds}$ is low for small values of $V_{ds}$, therefore the thickness of the depletion region near the

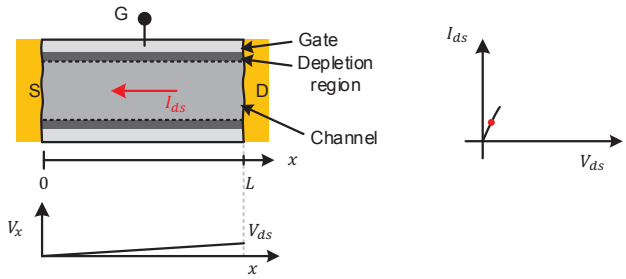



Figure 3.1: An illustration of channel and voltage variation along the channel for a junction-FET and a small drain-source current.

source and drain are similar as illustrated in Fig. 3.1. With an increase in the current, the voltage $V_x$ near the drain end of the channel is larger than the voltage at the source end. Since the depletion region depends on the gate-to-channel potential, the shape of the depletion region changes as illustrated in Fig. 3.2(a). With an increase in the applied $V_{ds}$, the depletion region widens,

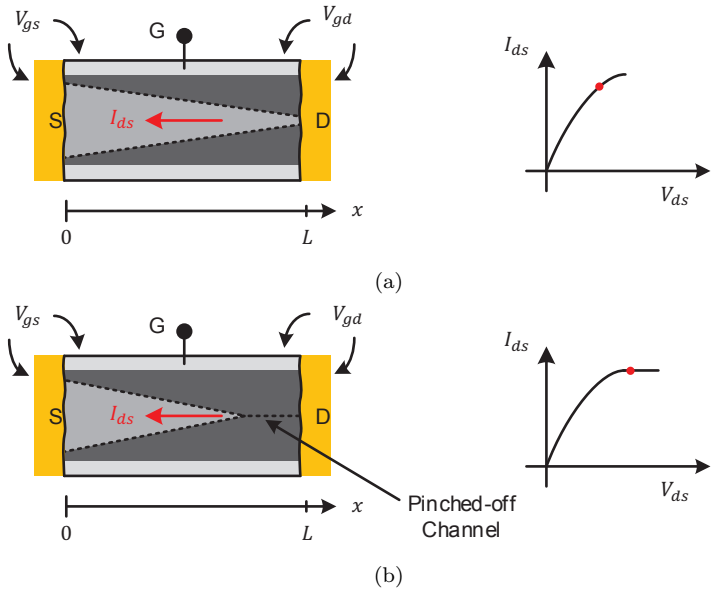



Figure 3.2: Illustration of variation of depletion region in the channel of a junction-FET with zero gate-source bias and (a) near current saturation, and (b) beyond current saturation [41].

intruding the channel near the drain end. Thus, the effective channel area is constricted as shown in Fig. 3.2(a). With further increase in the drain-source bias, the channel gets completely encroached as shown in Fig. 3.2(b). In this situation, the current through the channel cannot increase and gets saturated. The electrons from the channel are swept away towards the drain by the electric field-present in the depletion region.

From the brief description present above, the observed current-voltage (IV) behavior of a transistor is obviously nonlinear. The estimation of the IV relationship of a FET under nonlinear operation is often simplified by assuming

that the saturation current beyond pinch-off[1] remains fairly constant. The *Gradual channel approximation* (GCA) is used to calculate the current-voltage relationship until the full constriction of the channel at the drain end [73]. According to the GCA, it is required that the rate of variation of the lateral field along the channel must be smaller than the rate of variation of the vertical field, and the change in channel potential must be gradual as a function of position. While the GCA is a good starting point, many of the modern FETs have extremely short channel lengths, and therefore, the aforementioned requirement is often not met. Hence, empirical methods are used to model the IV-characteristics.

## 3.2 Nonlinear current model

The nonlinear expression for the current is directly related to the small-signal parameters according to (2.3a). Therefore, the bias-dependent behavior of the parameters is utilized to build the nonlinear empirical expressions for the resistive part of the drain-source current ($I_{ds}$) according to

$$\left.\frac{\partial I_{ds}\left(V_{gs},V_{ds}\right)}{\partial V_{gs}}\right|_{V_{GS},V_{DS}} = g_m\left(V_{GS},V_{DS}\right) \tag{3.1a}$$

$$\left.\frac{\partial I_{ds}\left(V_{gs},V_{ds}\right)}{\partial V_{ds}}\right|_{V_{GS},V_{DS}} = g_{ds}\left(V_{GS},V_{DS}\right). \tag{3.1b}$$

Referring back to Chapter 2 for symmetrical transistors, the drain-source current is related to the derivatives in (2.10) according to

$$\left.\frac{\partial I_{ds}\left(V_{gs},V_{gd}\right)}{\partial V_{gs}}\right|_{V_{GS},V_{GD}} = g_m^{+}\left(V_{GS},V_{GD}\right) \tag{3.2a}$$

$$\left.\frac{\partial I_{ds}\left(V_{gs},V_{gd}\right)}{\partial V_{gd}}\right|_{V_{GS},V_{GD}} = -g_m^{-}\left(V_{GS},V_{GD}\right). \tag{3.2b}$$

Therefore, the current model shall be such that its derivatives should fit the extracted small-signal parameters according to (3.1) or (3.2).

A number of empirical current expressions are available to model the nonlinear drain-source current. The models are dependent on the transistor technology and observed IV-characteristics. Some of them are discussed below.

### Curtice quadratic model

This is one of the first MESFET current model suggested by Curtice [45]. The current expression is given by

$$I_{ds} = \begin{cases} \beta_1\left(V_{gs}-V_{T0}\right)^2\left(1+\lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right) & \text{if } V_{ds}>0, \left(V_{gs}-V_{T0}\right)>0 \\ \beta_1\left(V_{gs}-V_{T0}\right)^2\left(1+\lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right) & \text{if } V_{ds}<0, \left(V_{gd}-V_{T0}\right)>0 \\ 0 & \text{otherwise} \end{cases}. \tag{3.3}$$

[1] Pinch-off denotes the constriction of the channel by the depletion region.

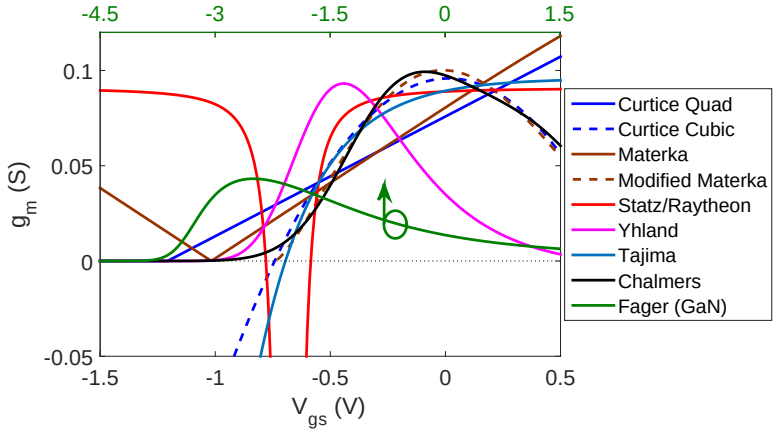



Figure 3.3: Illustration of the transconductance (derivative of drain-source current versus gate-source voltage) for different models at $V_{ds} = 2$ V. The top x-axis is used to illustrate the Fager et. al. model [81]. The parameter values used for different models are listed at the end of the chapter in Table 3.1.

The model is quite simple with only four parameters. However, it is not possible to achieve a good fit to the device behavior as the transconductance ($g_m$) predicted by the model has an unrealistic linearly increasing behavior as shown in Fig. 3.3.

### Curtice cubic model

The cubic model by Curtice is an improvement to the quadratic model for MESFETs [46]. Similar to the previous case, this model is also simple with a better transconductance behavior compared to the quadratic model. However, there is an unrealistic negative transconductance below the threshold voltage predicted by the model as shown in Fig. 3.3. The drain-source current is given by

$$I_{ds} = \begin{cases} \left(A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3\right) \tanh\left(\gamma V_{ds}\right) & \text{if } V_{ds} \geq 0 \\ 0 & \text{if } V_{ds} < 0 \end{cases} \tag{3.4a}$$

$$\text{where } V_1 = V_{gs}\left[1 + \beta\left(V_{dso} - V_{ds}\right)\right]. \tag{3.4b}$$

### Materka model

The Materka model is also designed for MESFETs [85] and is given by

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tanh\left[\frac{\alpha V_{ds}}{V_{gs} - V_p}\right] \tag{3.5a}$$

$$V_p = V_{p0} + \gamma V_{ds}. \tag{3.5b}$$

The model also shows difficulties in modeling the transconductance similar to the Curtice models as illustrated in Fig. 3.3.

### Modified Materka model

The modified Materka model is also designed for MESFETs [86] and is given by

$$I_{ds} = I_{dss}\left(1 + S_S\frac{V_{ds}}{I_{dss}}\right)\left(1 - \frac{V_{gs}}{V_{po} + \gamma V_{ds}}\right)^{(E+K_E V_{gs})} \cdot \tanh\left[\frac{S_L V_{ds}}{I_{dss}\left(1 - K - gV_{gs}\right)}\right]. \tag{3.6}$$

The model has significantly improved performance above the threshold voltage as shown in Fig. 3.3. However, the transconductance is not real below threshold voltage due to the presence of logarithmic term with the argument $[1 - V_{gs}/(V_{po} + \gamma V_{ds})]$ in the derivative of the current expression.

### Statz/Raytheon model

The Statz/Raytheon model in [87] is a MESFET model where the hyperbolical tangent function on $V_{ds}$ is not used unlike the previously shown current expressions. It was proposed to save computation time. However, this feature is not so important today when there is a significant improvement in the computational capacity. The model current is given by

$$I_{ds} = \begin{cases} \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)}\left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right](1 + \lambda V_{ds}) & \text{if } 0 < V_{ds} < 3/\alpha \\ \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)}(1 + \lambda V_{ds}) & \text{if } V_{ds} \geq 3/\alpha \end{cases}. \tag{3.7}$$

The proposed model is simple and has only five parameters. The transconductance in Statz/Raytheon model similar to previously described models is unrealistic as shown in Fig. 3.3.

The TriQuint's Own Model (TOM) is a variation of the Statz/Raytheon model wherein the exponent in the square-law term $(V_{gs} - V_T)^2$ is changed to an adjustable model parameter [88, 89]. The current expression is given by

$$I_{ds} = \begin{cases} I_d\left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right](1 + \lambda V_{ds}) & \text{if } 0 < V_{ds} < 3/\alpha \\ I_d & \text{if } V_{ds} \geq 3/\alpha \end{cases} \tag{3.8a}$$

$$I_d = \frac{\beta\left(V_{gs} - V_T\right)^Q}{1 + \delta V_{ds}\beta\left(V_{gs} - V_T\right)}. \tag{3.8b}$$

The TOM model, similar to the Statz/Raytheon model, has issues around the threshold voltage which is clearly shown in Fig. 3.3.

### Tajima model

The Tajima model uses an exponential function instead of the tangent hyperbolic function [90]. The current is defined as

$$I_{ds} = I_{d1} I_{d2} \tag{3.9a}$$

$$I_{d1} = \frac{1}{k}\left[1 + \frac{V'_{gs}}{V_p} - \frac{1}{m} + \frac{1}{m}\exp\left\{-m\left(1 + \frac{V'_{gs}}{V_p}\right)\right\}\right] \tag{3.9b}$$

$$I_{d2} = I_{dsp}\left[1 - \exp\left\{-\frac{V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}}\right)^2 - b\left(\frac{V_{ds}}{V_{dss}}\right)^3\right\}\right] \tag{3.9c}$$

$$k = 1 - \frac{1}{m}\left[1 - \exp(-m)\right] \tag{3.9d}$$

$$V_p = V_{po} + pV_{ds} + V_\phi \tag{3.9e}$$

$$V'_{gs} = V_{gs} - V_\phi \tag{3.9f}$$

The model has similar features like the Curtice Cubic model. The transconductance becomes negative below the threshold voltage as shown in Fig. 3.3.

### Chalmers model

The Chalmers model is one of the first empirical models able to predict the transistor performance for a wide range of operation [29]. The model in its simplest form is expressed as

$$I_{ds} = I_{pk}\left[1 + \tanh(\psi)\right]\left(1 + \lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right) \tag{3.10a}$$

$$\psi = \sum_{n=1}^{N} P_n \left(V_{gs} - V_{pk}\right)^n \tag{3.10b}$$

The Chalmers model does not have any strange behavior (e.g. negative or complex transconductance) as observed in the previously discussed models, see Fig. 3.3. Over the years, the model has also been improved for higher accuracy by including higher order terms in $\psi$, and $V_{ds}$ dependence on the shift of the peak of the maximum transconductance ($V_{pk}$) [80, 91]. The model has been extensively used for GaAs, SiC (Silicon Carbide), InP (Indium Phosphide), GaN MESFETs and HEMTs. The Chalmers model is also developed for the symmetrical transistors, where the current expression is also valid for the negative $V_{ds}$ region [82].

### Yhland model

Another symmetrical model was reported by Yhland et. al. [49] targeting the resistive mixer operation regime. The model is based on the assumption that the intrinsic transistor is symmetrical around the gate with respect to the source and drain. Unlike previously described models, the drain-source current in [49] is a function of the gate-source and gate-drain voltages. The current expression is given by

$$I_{ds} = g\left[f_1\left(U^+_{gd}, U^+_{gs}\right) f_2\left(V_{gs} - V_{gd}\right) - f_1\left(U^-_{gs}, U^-_{gd}\right) f_2\left(V_{gd} - V_{gs}\right)\right] \tag{3.11}$$

where

$$f_1(x,y) = [1+ax]\left[1-\tanh\left(e^{-b(y+c)}\right)\right] \tag{3.12a}$$

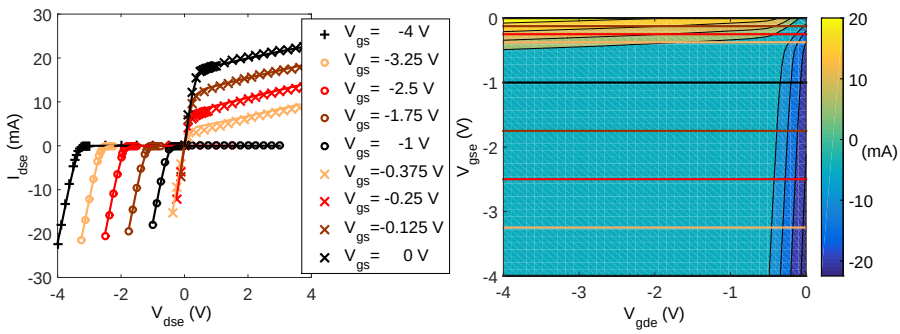
$$f_2(z) = 1-\tanh\left(e^{-dz}\right). \tag{3.12b}$$

The first part of (3.11) dominates for $V_{ds} > 0$ V, whereas the second part dominates for $V_{ds} < 0$ V. $(U_{gd}^+, U_{gs}^+)$ and $(U_{gd}^-, U_{gs}^-)$ define the coordinate system rotated by the angle $\phi$ relative to the $(V_{gd}, V_{gs})$ coordinate system in the counter-clockwise and clockwise directions respectively, as

$$\begin{bmatrix} U_{gd}^+ \\ U_{gs}^+ \end{bmatrix} = \begin{bmatrix} \cos(\phi) & \sin(\phi) \\ -\sin(\phi) & \cos(\phi) \end{bmatrix} \begin{bmatrix} V_{gd} \\ V_{gs} \end{bmatrix} \tag{3.13a}$$

$$\begin{bmatrix} U_{gd}^- \\ U_{gs}^- \end{bmatrix} = \begin{bmatrix} \cos(\phi) & -\sin(\phi) \\ \sin(\phi) & \cos(\phi) \end{bmatrix} \begin{bmatrix} V_{gd} \\ V_{gs} \end{bmatrix}. \tag{3.13b}$$

The model in [49] is used for modeling the symmetrical GaAs HEMT in [Paper A]. The agreement between the measured and modeled IV-characteristics is shown in Fig. 3.4(a) and the contour plot in $(V_{gd}, V_{gs})$ coordinate system is shown in Fig. 3.4(b).




(a) (b)

Figure 3.4: Yhland symmetrical current model for the GaAs DUT showing (a) comparison of measured(marker) versus modeled(-) I-V characteristics, (b) contour plot of $I_{ds}$ with constant $V_{gs}$ sweeps in the left figure drawn in corresponding colors in the extrinsic bias grid [Paper A].

### Fager model

The current model in Fager et. al. [81] has been developed for laterally diffused metal oxide semiconductor (LDMOS) transistors. The model has also been used for GaN transistors [32, 92]. The current expression is built on the transconductance characteristics which can be divided into four distinct regions, i.e. sub-threshold, quadratic, linear and compression. The model

expressions are given as

$$V_{gs1} = V_{gs} - V_t \tag{3.14a}$$

$$V_{gs2} = V_{gs1} - \frac{1}{2}\left(V_{gs1} + \sqrt{\left(V_{gs1} - VK\right)^2 + \triangle^2}\right) \tag{3.14b}$$

$$V_{gs3} = VST \ln\left(1 + e^{V_{gs2}/VST}\right) \tag{3.14c}$$

$$I_{ds} = \left\{\frac{\beta V_{gs3}^2}{1 + \frac{V_{gs3}^{\text{plin}}}{VL}}\right\} \cdot \left\{(1 + \lambda V_{ds})\right\} \cdot \left\{\tanh\left(\frac{\alpha V_{ds}}{V_{gs3}^{\text{psat}}}\right)\right\}. \tag{3.14d}$$

Equation (3.14a) models the threshold voltage and (3.14c) and the square term in (3.14d) model the transconductance in the subthreshold and quadratic regions. The denominator in the first term in (3.14d) controls the transition from the quadratic to the linear region. The compression region is modeled by saturating $V_{gs}$ at a constant voltage $VK$ and according to (3.14b). Some of these parameters may not necessarily be a constant and are made a function of the applied voltages and temperature [81].

### Fager Symmetrical Model

The model in [81] is only valid for $V_{ds} \geq 0$ V and does not model the transistors in the negative $V_{ds}$ region. Therefore, the model is modified to reflect the symmetry and operation of GaN transistors in switch circuits in [Paper C]. The modified current expression is given by

$$I_{ds}^{\text{sym}}\left(V_{gs}, V_{gd}\right) = \frac{1}{2}\left[I_{ds}\left(V_{gs}, V_{gs} - V_{gd}\right) - I_{ds}\left(V_{gd}, V_{gd} - V_{gs}\right)\right] \tag{3.15}$$

where

$$I_{ds}\left(V_{gs}, V_{ds}\right) = \left\{\frac{\beta V_{gs3}^2}{1 + \frac{V_{gs3}^{\text{plin}}}{VL}}\right\} \cdot \left\{(1 + \lambda V_{ds})\right\} \cdot \left\{1 + \tanh\left(\frac{\alpha V_{ds}}{V_{gs3}^{\text{psat}}}\right)\right\} \tag{3.16a}$$

$$V_{gs2} = V_{gs1} - \frac{\phi}{2}\left(V_{gs1} + \sqrt{\left(V_{gs1} - VK\right)^2 + \triangle^2}\right). \tag{3.16b}$$

The modification in the third term in (3.16a) allows the expression to model the current correctly around $V_{ds} \sim 0$ V. Whereas, the parameter $\phi$ added in (3.16b) controls the amount of saturation in the gate-source voltage in the positive $V_{ds}$ region and the gate-drain voltage in the negative $V_{ds}$ region.

### Jardel model

There is another current expression valid for symmetrical GaN HEMTs reported by Jardel et. al. in [93]. The current expression in [93] does not have a hyperbolic tangent dependence on $V_{ds}$ unlike [49, 82], [Paper C]. The model contains nested asymptotic functions to accurately model higher order harmonics for a transistor in the operating condition as a switch [93].

## 3.3 Nonlinear charge model

Modeling the nonlinear charges along with the resistive current in a transistor is critical to accurately predict the bias dependent S-parameters, harmonic and intermodulation distortion, adjacent channel power ratio (ACPR) etc. [94]. In general, the contribution of the charge to the current at node $i$ is expressed as [21, eq. 5.9]

$$I_i(t) = \frac{dQ_i\big(V_1(t), V_2(t)\big)}{dt} \tag{3.17}$$

where $V_1(t)$ and $V_2(t)$ are the two independent intrinsic voltages of a three terminal device. Either the capacitances or the charge as a function of applied voltages can be used to model the reactive currents in (3.17). However, it is important to consider the charge conservation according to

$$\frac{\partial^2 Q_i}{\partial V_1 \partial V_2} = \frac{\partial^2 Q_i}{\partial V_2 \partial V_1} \tag{3.18}$$

where $i$ can be replaced by $g$ or $d$ for the gate or drain terminals, respectively. The charge expression can be modeled directly from the extracted small signal capacitances by a path independent line integral when (3.18) is satisfied [21]. The integral is expressed as

$$Q_i = \int\limits_{\text{contour}} C_{i1} dV_1 + C_{i2} dV_2 \tag{3.19}$$

where $C_{ij} = \partial Q_i / V_j$. Modeling the charge expressions for the terminals automatically satisfies the condition in (3.18). This is not the case if developing a model directly from the small-signal capacitances.

### 3.3.1 Charge model expressions

Different empirical expressions for the charge are commonly not identified by any name, unlike the current models. However, they are an essential part of the transistor model. The empirical charge expressions model the bias dependent extracted intrinsic small-signal capacitances. For example, the Curtice quadratic [45] and cubic [46] models use the same charge model, which consists of a constant $C_{ds}$ and two expressions $Q_{gs}$ and $Q_{gd}$ representing $C_{gs}$ and $C_{gd}$, respectively [95, 96]. The Chalmers model, on other hand, is formulated with three choices, either fixed capacitances, nonlinear capacitance expressions, or nonlinear charge expressions, which can be used together with the current model [97]. The symmetrical model in [49] consists of three fixed capacitances. Like the current, nonlinear charge modeling can also be simplified by incorporating the symmetry around the gate.

### 3.3.2 Symmetry in charge model

The gate and drain charge functions $Q_g(V_{gs}, V_{ds})$ and $Q_d(V_{gs}, V_{ds})$ are typically used to define the reactive currents in a nonlinear transistor model. However, since the drain and source terminals of a symmetrical device are a

mirror of each other, it is advantageous to instead model the drain charge $Q_d^{\text{sym}}\big(V_{gs}(t), V_{gd}(t)\big)$ and the source charge $Q_s^{\text{sym}}\big(V_{gs}(t), V_{gd}(t)\big)$. Using (3.17), the reactive currents at the source and drain terminals are given by

$$\begin{bmatrix} I_s(t) \\ I_d(t) \end{bmatrix} = \begin{bmatrix} dQ_s^{\text{sym}}/dt \\ dQ_d^{\text{sym}}/dt \end{bmatrix} = \begin{bmatrix} \partial Q_s^{\text{sym}}/\partial V_{gs} & \partial Q_s^{\text{sym}}/\partial V_{gd} \\ \partial Q_d^{\text{sym}}/\partial V_{gs} & \partial Q_d^{\text{sym}}/\partial V_{gd} \end{bmatrix} \begin{bmatrix} dV_{gs}(t)/dt \\ dV_{gd}(t)/dt \end{bmatrix}. \tag{3.20a}$$

Thus, the partial derivatives of the charges at the source and drain ports are computed as

$$\left.\frac{\partial Q_s^{\text{sym}}}{\partial V_{gs}}\right|_{V_{gd}=\text{const}} = -C_{gs} - C_m^+; \qquad \left.\frac{\partial Q_s^{\text{sym}}}{\partial V_{gd}}\right|_{V_{gs}=\text{const}} = C_m^- \tag{3.21a}$$

$$\left.\frac{\partial Q_d^{\text{sym}}}{\partial V_{gd}}\right|_{V_{gs}=\text{const}} = -C_{gd} - C_m^-; \qquad \left.\frac{\partial Q_d^{\text{sym}}}{\partial V_{gs}}\right|_{V_{gd}=\text{const}} = C_m^+ \tag{3.21b}$$

where $C_{gs}$, $C_{gd}$, $C_m^+$ and $C_m^-$ correspond to the small signal model parameters defined in Section 2.5. Using the symmetry observed in Fig. 2.11, the partial derivatives of $Q_s^{\text{sym}}$ and $Q_d^{\text{sym}}$ according to (3.21) are symmetrical. Therefore, the charge functions are also symmetrical according to

$$Q_s^{\text{sym}}(V_{gs}, V_{gd}) = Q_d^{\text{sym}}(V_{gd}, V_{gs}). \tag{3.22}$$

Consequently, it is sufficient to model either $Q_s^{\text{sym}}$ or $Q_d^{\text{sym}}$ to define the reactive part of the intrinsic device. Thus, compared to modeling the gate and drain charges independently, as in the traditional models, the symmetry simplifies the modeling procedure with only one charge expression needed [Paper A].

For the exemplified GaAs HEMT in [Paper A], the source charge expression is built from existing expressions and is given by

$$\begin{aligned} Q_s^{\text{sym}}(V_{gs}, V_{gd}) = &\underbrace{f(V_{gs}, V_{gd}) + C_{gs0} \cdot V_{gs}}_{\text{[98, eq. (13)]}} + \underbrace{f(V_{gd}, V_{gs}) + C_{gd0} \cdot V_{gd}}_{\text{[98, eq. (14)]}} \\ &+ \underbrace{Q_d(V_{gs}, V_{gd})}_{\text{[56, eq. (A-2)]}} \end{aligned} \tag{3.23}$$

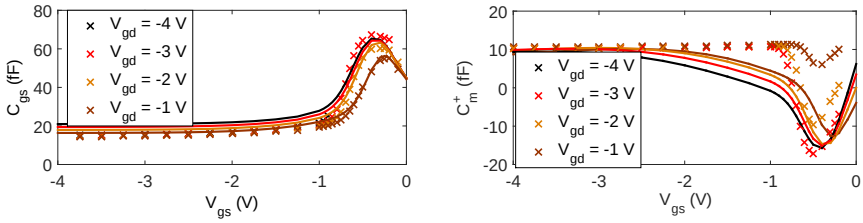
where

$$f(V_a, V_b) = C_0 \cdot \left[ V_a + C_f \cdot \log\left(\cosh(S_g \cdot W\left(V_a, V_b\right))/S_g\right) - \underbrace{R(V_a)}_{\text{[81, eq. (7)]}} \right] \tag{3.24}$$

$$W\left(V_a, V_b\right) = V_a - \eta \cdot V_a \cdot V_b - D_c \cdot \tanh\left(D_k \cdot V_b\right) \tag{3.25}$$

$$R(V_a) = (a_1/m_2) \cdot \ln\left(1 + \mathrm{e}^{m_2 \cdot (V_a - V_r)}\right). \tag{3.26}$$

The drain terminal charge is then calculated according to (3.22). The parameters of the nonlinear charge model for the GaAs DUT were extracted by manual fitting to the extracted small-signal intrinsic capacitances. Fig. 3.5 shows the modeled capacitances using a common charge expression (3.23) used




(a) (b)

Figure 3.5: Comparison of (a) $C_{gs}$ versus $V_{gs}$ and (b) $C_m^+$ versus $V_{gs}$ between the extracted small-signal capacitances (×) and modeled capacitances (-) obtained using charge expression in (3.23) [Paper A].

for the GaAs HEMT. Even though some mismatch is observed in $C_m^+$ at high ($V_{gs}$, $V_{gd}$), it can be concluded that a common charge function is sufficient to define the complete nonlinear model shown in Fig. 3.6.

A nonlinear current model together with the charge expression and extrinsic parameters form an important part of the transistor model. A schematic of the model is illustrated in Fig. 3.6.

## 3.4 Self-heating model

The current in a transistor is also affected by thermal effects [99]. It is therefore important to model the self-heating effects. There exist different models to accurately predict the thermal response of a transistor [100–105]. In all of the exemplified models in the appended papers, [Paper A]-[Paper E], a simple RC-circuit based thermal equivalent circuit is used to model the channel temperature as illustrated in Fig. 3.6 [105]. A manual fitting parameter ($a_T$) is added to model the effect of the channel temperature on the current according to

$$I_{ds}\left(V_{gs}, V_{ds}, T\right) = I_{ds}^{\text{Core}}\left(V_{gs}, V_{ds}\right) \cdot \left[1 - a_T\left(T - T_A\right)\right] \tag{3.27}$$

where $I_{ds}^{\text{Core}}\left(V_{gs}, V_{ds}\right)$ is the current model extracted from the measurements at the ambient temperature of $T_A$. The simple RC-circuit based model is used to put more focus on the other aspects of modeling highlighted in the respective paper.

Along with the thermal effects, transistors are also affected by trapping due to which the high-frequency operation deviates from the dc-IV characteristics. The trapping effects and the associated models are discussed in detail in Chapter 4.

## 3.5 Model validation

The complete model is validated using various small- and large-signal measurements of the transistor. A good agreement of the model behavior with the measurements generates a good confidence in the reliability of the model.

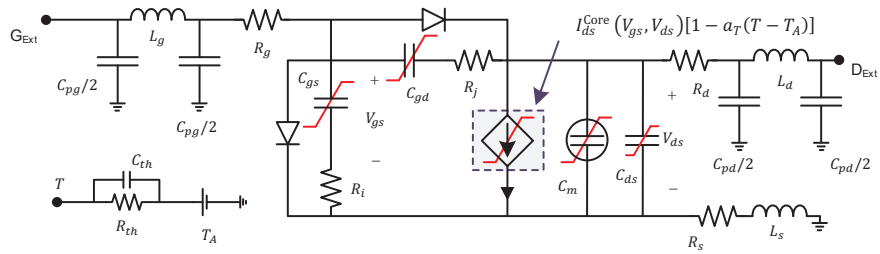



Figure 3.6: An illustration of the transistor model with the extrinsic parameters, current-source, nonlinear capacitances modeled by the charge expression and the thermal equivalent circuit.

### 3.5.1 dc-IV characteristics

Validating dc-IV characteristics give confidence on the dc (or steady state) performance of a transistor. This can be important to determine the validity of the current-voltage relationship predicted by the model. Fig. 3.7 shows a comparison between the measured and modeled dc-IV characteristics showing a good agreement.

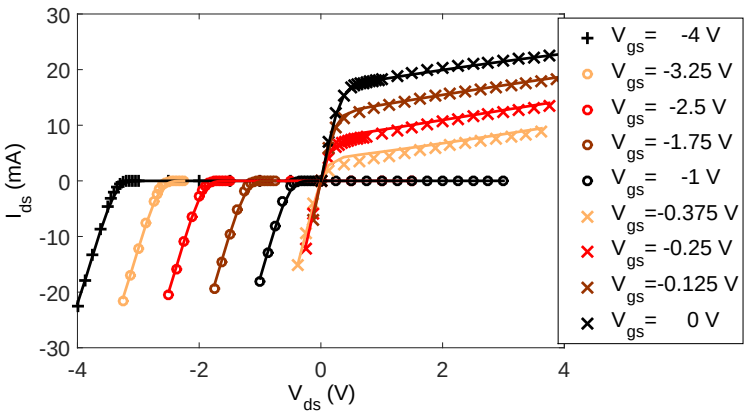



Figure 3.7: Comparison of measured (marker) and modeled (-) dc-IV characteristics of the GaAs HEMT used in [Paper A].

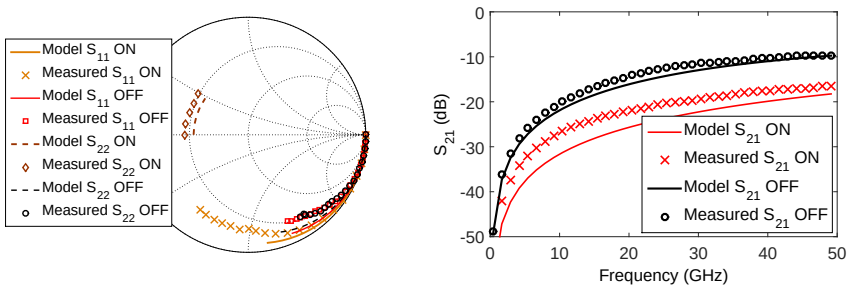
### 3.5.2 Pulsed-IV characteristics

Similar to dc-IV characteristics, pulsed-IV characteristics are also used to determine the validity of the current-voltage relationship. Pulsed-IV measurements are used for the extraction and validation under the minimal effect of self-heating and trapping, which both can cause inaccuracy in the IV-model [106]. Pulsed-IV measurements have been extensively used for characterization, extraction and validation of the trap models, and will be discussed later in Chapter 4.

### 3.5.3 Small-signal operation

Small-signal behavior of a transistor can be readily measured using a vector network analyzer (VNA), giving the scattering matrix parameters (S-parameters). The S-parameters not only gives information about the linear operation of a transistor but also allows a rough tracing of the output signal waveform. Therefore, a comparison with the measured S-parameters forms one of the basic model validation methods for RF operation.

In [Paper A], the transistor is intended to be operated as a switch in either ON or OFF state. Therefore, for the small signal verification, $V_{ds}$ bias is kept fixed at 0 V while $V_{gs} = 0$ V for the ON state and $V_{gs} = -4$ V for the OFF state. Measured and simulated S-parameters are compared and shown in Fig. 3.8. The mismatch is observed in the phase of $S_{11}$ in the ON state indicates a mismatch in $C_m^+$, see Fig. 3.5(b). Hence, further improvements are required in the charge model to correctly predict the extracted small-signal capacitances.




(a) (b)

Figure 3.8: Measured(×-ON, ∘-OFF) and modeled(-) S-parameters (a) $S_{11}$ and $S_{22}$, (b) $S_{21}$ of the GaAs HEMT used in [Paper A] from 100 MHz to 50 GHz at ON and OFF-state of a switch.

### 3.5.4 Load-pull measurements

Unlike S-parameters, pulsed- or dc-IV measurements, validation with load-pull measurements show the worthiness of the model for realistic RF applications. The transistor performance depends on the bias, input power, source and load terminations. Therefore, it is necessary to validate the model under such conditions. The measurement setup consists of a large-signal network analyzer (LSNA) which is capable of multi-harmonic measurements. The setup shown in Fig. 3.9 is used to emulate the operation of a transistor in a real high power shunt switch operation. The drain-source bias is kept fixed at 0 V volts while the gate-source voltage is set at 0 V for the ON state and −2.5 V for the OFF state. The DUT is excited with RF signal at the drain terminal similar to shunt switch operation and the incident and reflected waves are measured at both the drain and gate terminals.

To predict the harmonic response of the model in a CAD simulation, it is important to emulate the correct harmonic terminations observed by the transistor during the measurements. Therefore, the measured incident waves

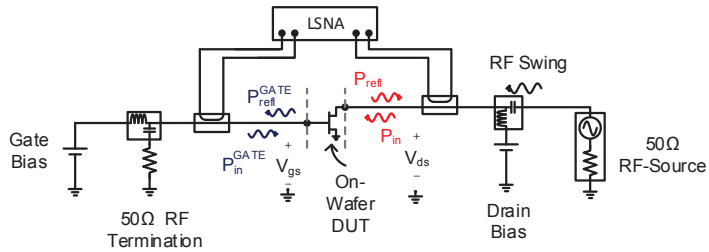



Figure 3.9: Large signal measurement setup with a large-signal network analyzer (LSNA), signal source and on-wafer transistor with 50 Ω RF termination at gate [107]. The reference plane of measurement is at the probe tips. The incident waves ($P_{in}^{GATE}$, $P_{in}$) and the reflected waves ($P_{refl}^{GATE}$, $P_{refl}$) are measured by the LSNA. Another variation of the load-pull measurement setup is used in [Paper D], where the load seen by the transistor is changed using a IQ modulator.

at the fundamental and the higher harmonic frequencies are injected in the respective ports during the model simulations. At low frequencies, the harmonics are generated mainly by the nonlinear current source, while at higher frequencies, the harmonics are also dependent on the reactive currents generated by the nonlinear charge model. Therefore, to validate the current and charge model, the simulated and measured reflected power are compared for varying incident RF power at 600 MHz and 16 GHz, respectively.

Fig. 3.10 shows the comparison between the simulated and measured harmonics at the ON state of the shunt switch. The good agreement in Fig. 3.10(a) validates the nonlinear current model and in Fig. 3.10(b), it validates the nonlinear charge model for the GaAs pHEMT. At power levels below the noise floor of the measurement setup, the measured noise is injected into the model causing the noisy response. This injected noise through the incident waves used as model excitation, also influences the phase of the reflected wave at higher harmonics. Therefore, the phase of the measured and simulated reflected wave at the fundamental frequency of the measurements are compared in Fig. 3.10(c) showing good agreement. Thus, the validation using both small- and large-signal measurements confirm the accuracy of the model and the overall symmetrical modeling procedure proposed in [Paper A].

## 3.6 Summary

This chapter has concentrated on nonlinear current and charge modeling along with model validation techniques. It is shown that the symmetry allows the modeling of the reactive currents using a single charge expression. This can help in simplifying the model extraction procedure. While the transistor model consists of extrinsic parameters along with nonlinear current and charge expressions, transistors are also affected by thermal effects (briefly discussed in this chapter) and trapping (to be discussed in detail in Chapter 4). Hence, a complete model would require all these effects to be taken into the account.

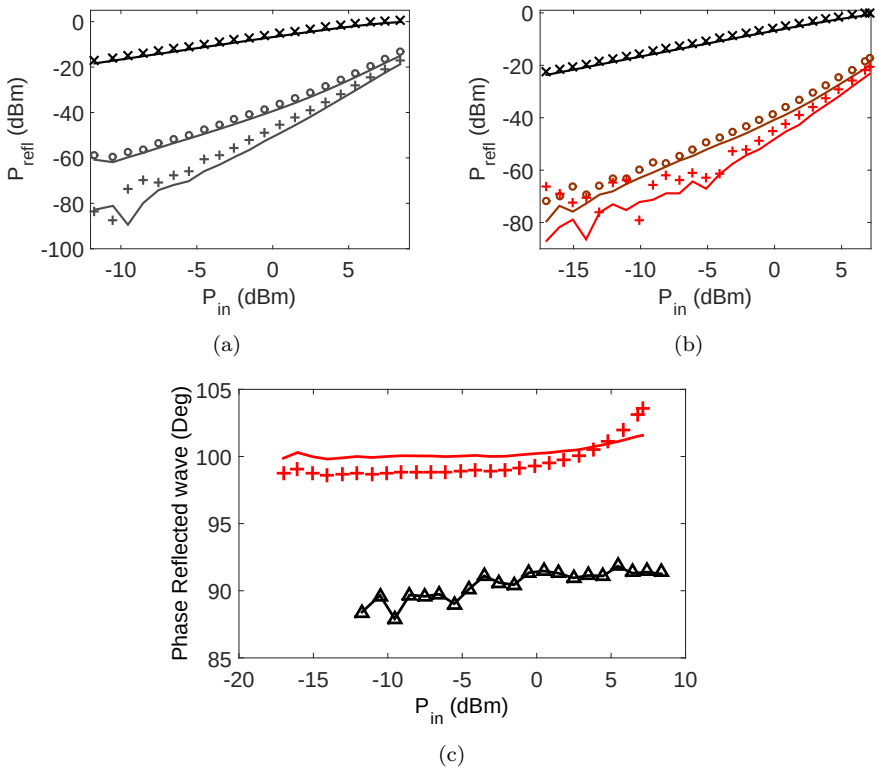



Figure 3.10: Comparison between magnitude of the measured (×: fundamental frequency, ∘: second harmonic, +: third harmonic) and modeled (-) reflected versus incident power at the drain of the DUT at (a) 600 MHz, (b) 16 GHz at the ON state ($V_{gse} = 0$ V, $V_{dse} = 0$ V), (c) comparison between the measured (△: 600 MHz, +: 16 GHz) and modeled (-) phase of the reflected wave ($P_{refl}$) at the drain port for the fundamental frequencies. For the OFF-state large-signal validation, see Fig. 14 in [Paper A].

Table 3.1: List of model parameters values used from [84] for the illustration of the current expressions in Fig. 3.3.

| Curtice quadratic model parameters | | | |
|---|---|---|---|
| $\beta_1$ | $V_{T0}$ | $\lambda$ | $\alpha$ |
| 0.0273 | -1.207 | 0.0754 | 2.265 |

| Curtice cubic model parameters | | | | | | |
|---|---|---|---|---|---|---|
| $A_0$ | $A_1$ | $A_2$ | $A_3$ | $V_{dso}$ | $\beta$ | $\gamma$ |
| 0.046 | 0.096 | 0.0024 | -0.056 | 2 | 0.008 | 1.7 |

| Materka model parameters | | | |
|---|---|---|---|
| $I_{dss}$ | $V_{po}$ | $\alpha$ | $\gamma$ |
| 0.041 | -1 | 2.31 | -0.0085 |

| Modified Materka model parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{dss}$ | $V_{po}$ | $\gamma$ | $E$ | $K_E$ | $S_L$ | $K_G$ | $S_S$ |
| 0.0347 | -0.587 | -0.076 | 1.64 | -0.752 | 0.0924 | -0.508 | 0.0052 |

| Statz/Raytheon model parameters | | | | |
|---|---|---|---|---|
| $\beta$ | $V_t$ | $b$ | $\alpha$ | $\lambda$ |
| 0.768 | -0.585 | 10.27 | 2.704 | 0.107 |

| Tajima model parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{dss}$ | $V_{dss}$ | $V_{po}$ | $V_\phi$ | $a$ | $b$ | $p$ | $m$ |
| 0.109 | 0.467 | 0.639 | 0.7 | 0.376 | -0.088 | 0.028 | 5.417 |

| Chalmers model parameters | | | | | | |
|---|---|---|---|---|---|---|
| $I_{pk}$ | $V_{pk}$ | $P_1$ | $P2$ | $P_3$ | $\alpha$ | $\lambda$ |
| 0.045 | 0.048 | 1.87 | -0.49 | 1.62 | 2.05 | 0.066 |

| Yhland model parameters | | | | | |
|---|---|---|---|---|---|
| $a$ | $b$ | $c$ | $d$ | $g$ | $\phi$ |
| -0.08 | 3.3 | 0.41 | 10 | 0.056 | 2.4 |

| Fager model parameters | | | | |
|---|---|---|---|---|
| $V_t$ | $VK$ | $\triangle$ | $VST$ | $p$lin |
| -3.45 | 1.4 | 2.15 | 0.15 | 1 |
| $\beta$ | $VL$ | $\lambda$ | $\alpha$ | $p$sat |
| 0.14 | 0.7 | 0.003 | 3.1 | 1.1 |

# Chapter 4

# Dispersion in Transistor

### Source, Effects and Models

Transistors are found to have trapping effects which deviate the high frequency operation from the dc-IV characteristics. Trapping effects are also called frequency dispersion [108], current slump [109], current compression [110], power slump [111], knee walk-out [112], kink effect [113], gate lag [114], and drain lag [115]. The trapping effects are caused by the capture and emission of electrons (and/or holes) at energy levels within the bandgap. The charging and discharging of these traps depend on the their location in the energy band. The trapped charges modulate the number of carriers in the 2-DEG, thereby changing the electrical characteristics of a transistor. The presence and identification of traps in GaAs transistors have been extensively studied [116]. Unlike GaAs transistors, trapping effects are more pronounced in GaN HEMTs due to high surface charge densities, high concentration of threading dislocations, the lattice mismatch with the substrate, etc., [117]. Therefore, the focus of this chapter will be on GaN HEMTs. Moreover, the trapping effects induce similar effects on the electrical characteristics of both GaN and GaAs devices. Hence, the trap models discussed in this chapter can be applied to GaAs, GaN, and other similar field-effect transistors.

Trapping in FETs is triggered by the electric field in the device [118]. The electric field in the device is also influenced by the field-plates (FPs), where the latter are used to reduce the peak electric field in order to increase the breakdown voltage [6, 119]. Apart from reducing the number of trapped electrons due to reduced peak electric field, FPs also change the distribution of the trapped electrons. Therefore, there is a relation between field-plates and the trapping effects in HEMTs.

In this chapter, an overview of the modeling of trapping effects is presented. The chapter begins with a discussion on the origin of traps in Section 4.1. This is followed by the description of the physical process of trapping and emission of electrons in the traps in Section 4.2. In Section 4.3, the effects of traps on the electrical characteristics of a transistor are discussed. Later on, an overview of the available empirical trap models is presented in Section 4.4. In Section 4.5, a new Shockley-Read-Hall (SRH) theory based model with effective back gating potential is discussed. The trap model addresses the influence of the trapped charges on the current (or the number of carriers) in

2-DEG due to the distributed nature of the former. This is followed by the validation of the proposed model. In Section 4.8, the influence of field-plate is investigated using the proposed model to distinguish the former's effect on the trap model parameters, and to open a scope for scalable trap models.

## 4.1 Physical Origins of Traps

One of the sources of traps are the crystal defects which introduce energy levels in the band gap [120]. The trap identification in GaN HEMTs are found to be more difficult than GasAs transistors due to the varying material qualities and growth process [121], higher trap densities due to lattice-mismatch and surface states [21, 122], and higher electric field enabling mechanisms like the Poole-Frankel effect [123].

Traps can be divided into two groups depending on their location in a transistor: (a) surface traps and (b) buffer traps.

### 4.1.1 Surface traps

Surface traps appear near the AlGaN surface as shown in Fig. 4.1. The source of surface states has been suggested to be the ambient water molecules bonding to the AlGaN surface at the room temperature [124]. Surface traps are linked to gate-lag effects, which can be reduced by passivation of these surface states. Thermal annealing is one such method to remove the water (and related molecules). Another effective method of surface passivation is by deposition of a layer of $SiN_x$ on the AlGaN surface. This method has shown drastic improvements in reducing the surface trapping in transistors [125–127].

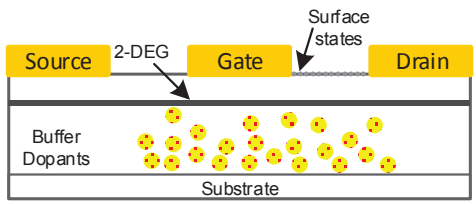



Figure 4.1: Cross-section of HEMT showing location of surface states and buffer dopants which contribute to buffer traps.

### 4.1.2 Buffer traps

The source of buffer traps are the crystal defects in the buffer due to lattice mismatch, threading defects, nitrogen (N) vacancies, etc. Higher crystal quality is achieved for the GaN buffer grown on SiC substrate. However, the two materials have different lattice constants. Therefore, a thin AlN nucleation layer and thick GaN buffer are added between the substrate and the HEMT structure to overcome the lattice mismatch [128].

Apart from the improvements in growth technique of GaN on SiC that have made it possible to obtain high-quality crystals, high carrier confinement close to AlGaN/GaN interface is important to improve pinch-off and reduce

short channel effects [129]. This is done by adding deep acceptor dopants, e.g. carbon (C) [130], magnesium (Mg) [131], iron (Fe) [132], during the growth of the buffer. These dopants, shown in Fig. 4.1, help in creating a high resistive buffer which improves the RF performance of the GaN HEMTs. While buffer dopants are necessary to ensure high carrier confinement, the former also show a strong correlation to dispersive effects [130, 133–135]. This makes it necessary to understand the trapping mechanism and its effects on the transistor operation.

## 4.2 Capture and emission process of electrons

Trap levels are essentially energy levels in the band gap which capture electrons (and/or holes) from either the conduction or the valence band as shown in Fig. 4.2. Thus, there exist four competing processes for charge transfer

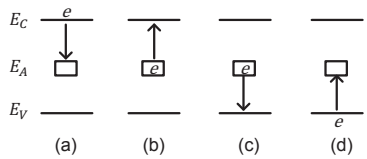



Figure 4.2: Four electron capture and emission processes from a trap level to conduction and valence band respectively. The arrow shows the direction of movement of an electron [136].

between the trap level and the valence or conduction band. These capture and emission processes can be described by the SRH statistics [136, 137]. For a deep acceptor level trap interacting with the conduction band, the rate of electron-density increase ($R_{cn}$) and decrease ($R_{en}$) due to electron capture and emission, respectively, are given by [136–139]

$$R_{cn} = c_n n(N_A - n_A) \tag{4.1a}$$

$$R_{en} = e_n N_C n_A \tag{4.1b}$$

where $n$ is the concentration of free electrons in the conduction band, $c_n$ is the rate of electron capture, $n_A$ is the density of filled trap states, and $N_A$ is the total density of trap states. $e_n$ and $N_C$ in (4.1b) are the rate of electron emission and effective density of states in the conduction band. Under thermal equilibrium, the electron emission is balanced by the capture. Therefore, $c_n$ and $e_n$ are related to each other as given by [136, eq. (2.9)]

$$\frac{e_n}{c_n} = \exp\left(\frac{E_A - E_C}{k_B T}\right) \tag{4.2}$$

where $E_A$, $E_C$ are energy levels of the acceptor state and the conduction band, respectively. $k_B$ and $T$ in (4.2) are Boltzmann constant and temperature, respectively. Using (4.1) and (4.2), the net rate of electron accumulation in the acceptor trap is given by

$$\frac{dn_A}{dt} = R_{cn} - R_{en} = \omega_T \left[(N_A - n_A)\exp\left(\frac{F_I - E_A}{k_B T}\right) - n_A\right] \tag{4.3}$$

where

$$n = N_C \exp\left(\frac{F_I - E_C}{k_B T}\right) \tag{4.4a}$$

$$\omega_T = c_n N_C \exp\left(\frac{E_A - E_C}{k_B T}\right) = \sigma_n \upsilon_n N_C \exp\left(\frac{E_A - E_C}{k_B T}\right) \tag{4.4b}$$

$\sigma_n$ and $\upsilon_n$ in (4.4) are the capture cross-section and the thermal velocity of the electrons. Over the typical operating temperatures, the thermal velocities of electrons and conduction band densities are proportional to $\sqrt{T}$ and $T^{\frac{3}{2}}$, respectively [140]. Thus, $\omega_T$ is of the form

$$\omega_T = AT^2 \exp\left(\frac{E_{act}}{k_B T}\right) \tag{4.5}$$

where $A$ is a constant and $E_{act}$ is the activation energy for the trap energy level. Such a dependence of $\omega_T$ on temperature ($T$) in (4.5) comes from the Arrhenius law given by

$$e_n = \frac{1}{\tau_{emission}} = AT^2 \exp\left(\frac{E_{act}}{k_B T}\right). \tag{4.6}$$

From the above analysis, three important observations can be made. The first observation is that the net capture or emission processes are first order differential equations with exponential solutions according to (4.3). The second observation is that the nature of exponential behavior is dependent on the applied voltage conditions due to the term $(F_I - E_A)$ in (4.3) [138, 140]. The third important observation is that the net capture or emission processes are strongly dependent on temperature according to (4.5) [136–138]. Together, these three properties essentially dictate the trapping effects which change the electrical characteristics of a transistor.

## 4.3 Effect of traps on transistor electrical characteristics

The trapping effects manifest themselves in transistor behavior such as knee-walkout effects [112] current suppression [110], kink effect [113], etc., as illustrated in Fig. 4.3. These effects deviate the high frequency operation from dc-IV characteristics leading to a reduced gain and output power. Trapping effects can also be observed in the drain-source current transients [141]. Fig. 4.4 shows an illustration of the measured drain-source current after a step change in the applied drain-source voltage. The exponential recovery observed in the current is often related to trapping effects. Similar effects are also observed in the associated gain of the transistor [139]. The recovery in the drain current can have multiple transients associated with single or multiple trap energy levels [135, 142]. The deviations caused due to trapping in transistors can lead to a significant mismatch between the designed and measured performance of the circuits containing them.

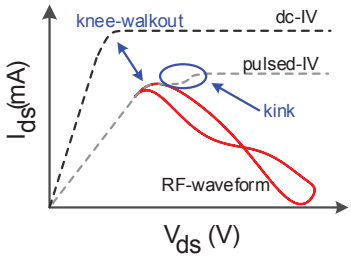



Figure 4.3: An illustration of the knee-walkout and kink effect observed in the pulsed-IV characteristics from a high trapping quiescent conditions.

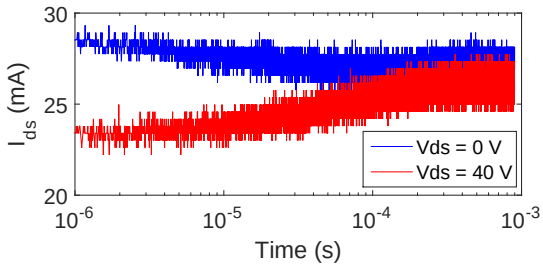



Figure 4.4: Measured drain-source current transient for a step change in the drain-source voltage from 0 V and 40 V to 30 V across a commercial GaN transistor used in [Paper D]. The gate-source voltage is set to −2.5 V.

## 4.4 Modeling Trapping Effects

Trap models are necessary in order to take into account the trapping effects, and predict the correct behavior of a transistor in order to take their full advantage in RF circuits. There can be many ways to distinguish different trap models, e.g. linear vs. nonlinear models, RC (resistive-capacitive) vs. non-RC models, delay vs. virtual gate potential/drain current implementations, etc. In this thesis, the trap models are looked as a two step procedure. The first step is to model the trapping effects, and the second step is its implementation in the transistor model. Based on these two steps (effect and implementation), trap models can be divided into four different categories:

- RC-branch delay implemented in the applied voltages;
- RC-branch delay implemented using a virtual gate;
- RC-branch delay implemented using an effective drain-source current;
- SRH-theory based models implemented using a virtual gate.

### 4.4.1 RC-branch delay in the applied voltages

Delay based trap models were initially designed to model the drain-lag effects. These models take into account the difference between the output conductance extracted from the small-signal RF characteristics and the dc (or low

frequency) IV measurements. The difference in the two measurements are typically used to extract the trap model parameters. Transient measurements are used to estimate the time-constant related to the trap, which is then used to set the capacitance values in the RC-branch. Some examples for this type of trap models are given below.

### Camacho et. al. model

The output impedance dispersion in [143] is typically modeled by introducing a low frequency RC-branch between the drain and source nodes of the transistor as shown in Fig. 4.5. Thus, the output impedance in saturation region and at low frequencies can be given by

$$Z_d(f) \simeq R_{ds}\left(\frac{1+j\omega C_T R_T}{1+j\omega C_T\left(R_T+R_{ds}\right)}\right). \tag{4.7}$$

Therefore, the low frequency (dc) impedance is observed as $Z_d(f=0) \simeq R_{ds}$. Whereas, the impedance at microwave frequencies beyond $f \gg 1/R_T C_T$ is observed as $Z_d(f) \simeq R_T R_{ds}/(R_T+R_{ds})$. This explains how the single RC-branch delay models like [143] predict the trap behavior in a transistor.

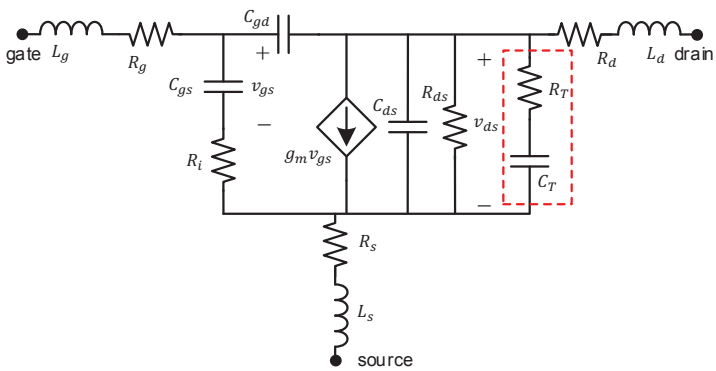



Figure 4.5: Trap model represented by RC-network as illustrated in [143].

### Golio et. al. model

The equivalent circuit model in Golio et. al. [144] replicates both the output and transconductance dispersion unlike the model in [143]. The model is illustrated in Fig. 4.6. The output impedance for the model is given by

$$Z_d(f) = \frac{R_{ds}\left(1+j\omega C_T R_T\right)}{1+j\omega C_T\left(R_T+R_{ds}+g_{mT}R_T R_{ds}\right)}. \tag{4.8}$$

The modeled output resistance and transconductance vary from the dc conditions to the microwave frequencies. At the two extremes, they are given by

$$Z_d(f=0) = R_{ds} \tag{4.9a}$$

$$Z_d(f\to\infty) = \frac{R_{ds}R_T}{R_{ds}+R_T+g_{mT}R_TR_{ds}} \tag{4.9b}$$

$$g_{m,\mathrm{NET}}(f=0) = g_m \tag{4.9c}$$

$$g_{m,\mathrm{NET}}(f\to\infty) = g_m - g_{mT} \tag{4.9d}$$

where $g_{mT}$ and $g_{m,\mathrm{NET}}$ are the transconductance due to the trapping effects and the net transconductance due to both the gate-source voltage and trapping, respectively. These models, e.g. [143,144], are used due to their relatively simple topologies and parameter extraction processes. Such models are mostly used under small-signal operating conditions due to the limitations in the voltage and temperature operating range of the model.

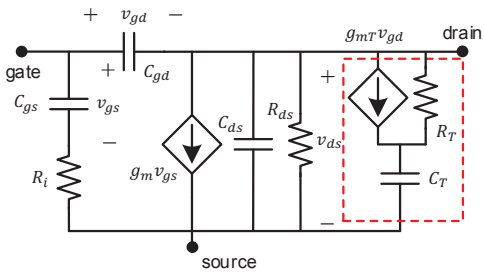



Figure 4.6: Trap model using RC-network with VCCS controlled by the drain-gate voltage as illustrated in [144].

### 4.4.2 RC-branch delay implemented using a virtual gate

The trapping effects can also be viewed as an additional virtual gate in a transistor. Therefore, the trapping behavior can be modeled by a subcircuit and implemented into a transistor model through the addition of a virtual gate [145–150]. Similar to the previous models, the trap model parameters are extracted from the difference between the measured dc-IV and S-parameters.

#### Jeon et. al. model

The trap model in [147] uses two RC-branches to implement gate and drain delay as shown in Fig. 4.7. The two voltage controlled voltage sources (VCVS) implement the delay into the effective gate-source voltage, where the latter is given by

$$V_{gs}^{\mathrm{Eff}} = V_{GS} + \alpha_1\left(V_{ds}(t) - V_{DS}\right) + \alpha_2\left(V_{gs}(t) - V_{GS}\right). \tag{4.10}$$

The effective gate voltage is then used to determine the drain-source current flowing through FET2 as

$$I_{ds}(t) = f\left(V_{gs}^{\mathrm{Eff}}, V_{ds}(t)\right) \tag{4.11}$$

where $f(\bullet)$ describes the dc drain-source current. In (4.10), $\alpha_1$ and $\alpha_2$ are output conductance and transconductance dispersion parameters, respectively. $R_3$, $R_4$ and $C_2$ determine $\alpha_1$ and the transition frequency of output impedance dispersion. Similarly, $R_1$, $R_2$ and $C_1$ determine $\alpha_2$ and the transition frequency of the transconductance dispersion. In the circuit shown in Fig. 4.7, the conduction path for the drain and gate currents are through FET2 and FET1, respectively. The drain current and gate current path in FET1 and FET2, respectively, are disabled.

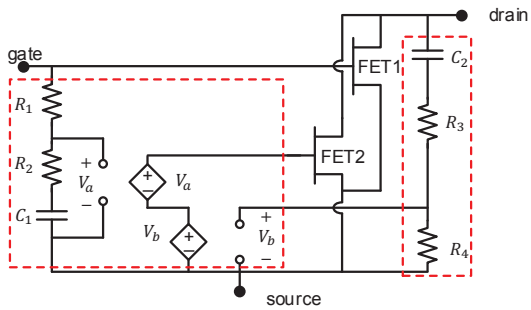



Figure 4.7: Trap model using two RC-networks creating the effective gate-source voltage as illustrated in [147].

### Matsunaga et. al. model

Another very similar implementation is reported in [149]. There exist two low frequency RC-branches to model the gate and drain delay, and a VCVS to implement the combined effect into the applied gate-source voltage. The use of an RC-branch in the trap models in [147,149] ensure that the time-constants of the electron capture and release processes are fixed.

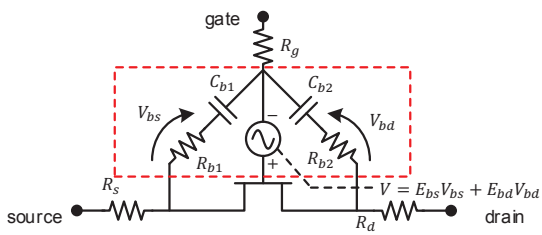



Figure 4.8: Trap model using two RC-network creating the effective gate-source voltage as illustrated in [149].

### Jardel et. al. model

Some models distinguish the fast capture and slow emission processes using two separate RC-branches. The trap model in [151] is shown in Fig. 4.9. Two resistances placed in each path have very different values ($R_{fill} \ll R_{empty}$). The diode is used to differentiate the two processes, and selects one over another depending on the applied voltage conditions. This allows the model to

take into account the asymmetry between charging and discharging of traps. In Fig. 4.9, the left part of the equivalent circuit incorporates the equivalent charge of traps represented by a capacitor. The right part of the circuit treats the trap voltage to modify the gate-source voltage for the current source in order to implement the trapping effects in the transistor model. The model parameters are extracted from the transient and dc-IV measurements [151]. Furthermore, the RC-network time-constant related to the charging of traps is typically set to a small value ($\tau_{fill} < 50$ns), whereas the RC-network time-constant for the discharging path is extracted from the drain-source current transient measurements.

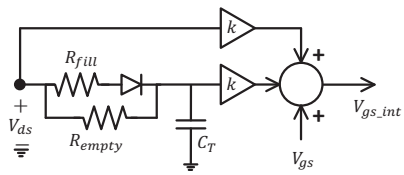



Figure 4.9: Trap model using RC-network with a diode distinguishing the capture and emission processes as illustrated in [151].

### 4.4.3 RC-branch delay implemented using an effective drain-source current

Similar to the effective gate-source voltage, delay circuits can also be used to implement the difference in the drain-source current. The models in [152–154] use error correcting terms in the drain-source current expression to implement the trapping effects in the transistor. The model parameters are typically extracted using a fitting procedure based on a large number of pulsed- and dc-IV measurements.

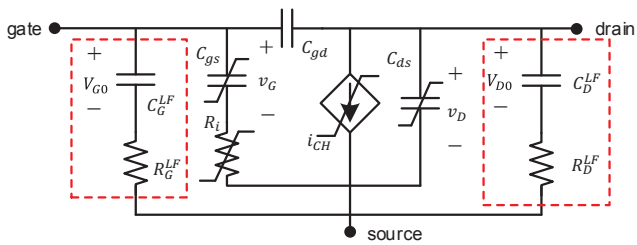



Figure 4.10: Trap model using two RC-branches as illustrated in [153].

#### Filicori et. al. model

The Filicori et. al. model implementation is illustrated in Fig. 4.10, where the capacitances $C_G^{LF}$ and $C_D^{LF}$ model the charge trapping [153]. The resistive-capacitive branches in the equivalent circuit model the delay time-constants. The drain-source current $i_{CH}$ is defined as a function of both instantaneous

and mean conditions as

$$i_{CH} = F\left(v_G, v_D, V_{G0}, V_{D0}, \theta_0\right). \tag{4.12}$$

The expression is linearized under the assumption that the trapping effects are not strong enough to involve nonlinear effects. Therefore, (4.12) is simplified as

$$\begin{aligned} i_{CH} = {} & F^*_{dc}\left[v_G, v_D\right] + f_\theta\left[v_G, v_D\right]\left[R_\theta\left(P_0 - P^*_0\right) + \theta_C - \theta^*_C\right] \\ & + f_G\left[v_G, v_D\right]\left(v_G - V_{G0}\right) + f_D\left[v_G, v_D\right]\left(v_D - V_{D0}\right) \end{aligned} \tag{4.13}$$

where

$$f_G = -\left.\frac{\partial F}{\partial V_{G0}}\right|_* \tag{4.14a}$$

$$f_D = \left.\frac{\partial F}{\partial V_{D0}}\right|_* \tag{4.14b}$$

$$F^*_{dc} = \left.F\right|_* + f_G\left(V^*_{G0} - v_G\right) + f_D\left(V^*_{D0} - v_D\right) \tag{4.14c}$$

In (4.12), $V_{G0}$, $V_{D0}$, $\theta_0$ are the mean gate-source, drain-source voltages and channel temperature respectively. The four functions $F^*_{ds}$, $f_\theta$, $f_G$, and $f_D$ in [153] are identified from a model fitting procedure. A least squares algorithm is therefore used with a large number of static and dynamic measurements performed for different quiescent bias conditions. It is important to note that (4.13) is a first order approximation assuming that the dynamic effects due to the traps and the dynamic heating are not strong. In some cases, the resistor in the LF-RC branch is replaced by a nonlinear current source expanding the flexibility in the correction term [155, 156]. The drain-source current is then expressed as

$$I_{ds} = I_{ds,DC}\left(V_{gs}, V_{ds}\right) + f_{\text{correction}}\left(V_{gs}, V_{ds}\right) \cdot \left(V_{ds} - V^{\text{LF}}_{ds}\right) \tag{4.15}$$

where $f_{\text{correction}}(\bullet)$ represents the nonlinear correction term in (4.15). The correction term can be extracted from pulsed-IV measurements [154], and modeled by nonlinear expressions [156] or lookup tables [157]. The error correction term based models in [153,154] are used due to their relative simplicity in terms of extraction of parameters from the pulsed-IV measurements. The models show good accuracy in predicting both the small signal and pulsed-IV measurements.

### Leoni et. al. model

Another RC-branch subcircuit based trap model is presented in [158]. The equivalent circuit is similar to [151] in using diodes to distinguish charging and discharging of traps. However, unlike [151], trapping effects observed in [158] shows that the change in drain-source current is linearly dependent on the drain-gate voltage, whereas the trap related time-constants are approximately constant over wide range of the drain-gate voltage. Therefore, the drain-source

current is modeled as

$$I_{ds} = I_{DS}\left(V_{gs}, V_{ds}\right)\left[1 - \sum_{J=1,2,3}\left(\alpha_J \cdot V_{DG}^{\mathrm{OFF}} + \beta_J\right) \cdot \left\{1 - \exp\left(\frac{-t_{\mathrm{OFF}}}{\tau_C^J}\right)\right\} \cdot \exp\left(\frac{-t}{\tau_C^J}\right)\right] \tag{4.16}$$

where $\alpha_J$ and $\beta_J$ are fitting constants. The decrease in the drain current is implemented using a VCCS controlled by a time-dependent drain-gate voltage $V'_{dg}$ , where the latter is generated by the trap circuit shown in Fig. 4.11. The three sets of double RC-branches with diodes in the trap equivalent cir-

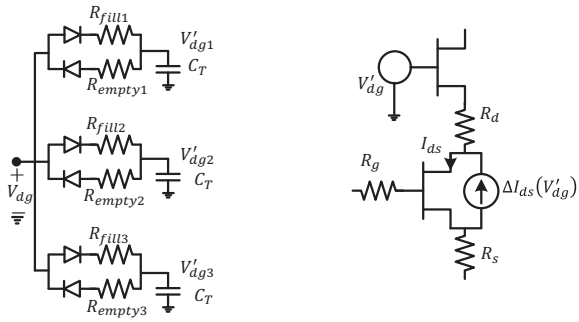



Figure 4.11: Trap model using multiple sets of RC-networks and implemented at VCCS and additional transistor to model the drain-current suppression and increase in the access resistance respectively, as illustrated in [158].

cuit represent three trapping/emission time-constants. Furthermore, the increase in the access resistance is modeled by a FET operating in the linear region. The trap model represented in Fig. 4.11 can also be transformed into a nonlinear RC-branch to represent a large-signal behavior with variable electron emission time-constants. Under such conditions, the change in the emission time-constant can be represented using variable resistor as $R_{empty,i} = \tau_0 \exp(\gamma V_{GS} + \delta V_{DS})$, where $\tau_0$, $\gamma$ and $\delta$ are fitting constants.

### 4.4.4 SRH theory-based models implemented using a virtual gate

The models discussed in the previous sections were based on the observed trapping behavior of a transistor. The exponential nature of the behavior allowed the use of RC-branch which is often sufficient to model the effects. Trapping effects are, however, strongly influenced by temperature. Therefore, the use of an RC-branch can often restrict the validity of the model to a limited region of operation. Unlike the error correction based models in [153, 154], SRH-theory based models closely follow physics, thereby having much wider range of validity in terms of voltage and temperature. The SRH theory-based models can also be viewed as temperature dependent nonlinear RC-circuit based models. These models tend to have higher accuracy in predicting the trapping behavior in a transistor operation.

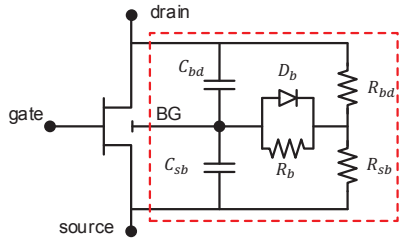



Figure 4.12: Trap model as illustrated in [159].

### Kunihiro et. al. model

One of the first large-signal trap models including the thermal effects was proposed by Kunihiro et. al. in [159]. The trap model is based on the SRH-theory, where the time-dependent expression for the trap charge is given by

$$\frac{d\Delta Q_B}{dt} = -J_S \left[\exp\left(\frac{e\Delta Q_B}{C_B k_B T}\right) - 1\right] - \frac{\Delta Q_B}{R_B C_B} \tag{4.17}$$

The two terms in (4.17) represent the electron capture and emission processes from the traps. The expression (4.17) can be described by currents through a diode and a resistor, respectively, which charge and discharge the traps represented by the back-gate capacitance $C_B$ as shown in Fig. 4.12. The back-gate capacitance is given by $C_B = C_{BD} + C_{BS}$ and the back-gate terminal charge is given by $Q_B$. The related back-gate voltage $V_B$ is then added to the threshold voltage of the main current source which emulates the effects of traps on the number of carriers and therefore, the current in 2-DEG according to

$$V_{th} = V_{th0} - \gamma V_B \tag{4.18}$$

where $\gamma$ here is the back-gating transconductance parameter and represents the ratio of real-front gate and pseudo-back gate distances. The term $J_S$ in (4.17) is of the similar form as the Arrhenius law in (4.6)

$$J_S = AT^2 \exp\left(-\frac{E_C - E_T}{k_B T}\right). \tag{4.19}$$

Therefore, the temperature effects of trapping are automatically incorporated into the model. The presented model is shown to predict both the output conductance dispersion and the thermal effects under both small-signal and large-signal conditions. The model parameters in [159] are typically calculated from the physical parameters of the device, which might not be easily available.

### Rathmell et. al. model

Another model has been developed based on SRH statistical theory, where the trapping process explained in Section 4.2 is modeled using two anti-parallel VCCSs [138]. The trap current formulation is given by

$$i_T = \omega_T C_T \left[(V_0 - v_T) - v_T \exp\left(\frac{v_I}{k_B T}\right)\right] \tag{4.20}$$

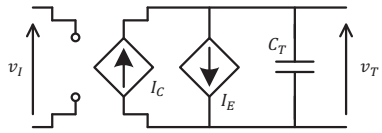



Figure 4.13: Trap model as illustrated in [138].

where $i_T$ is the net trapping current, $\omega_T$ is trap frequency, $v_I$ and $v_T$ are the trap model input and output potential. $V_0$ is the maximum trap potential under a fully ionized trap state, and it is negative for hole trapping at an acceptor level, and positive of electron trapping at a donor level. The trap current is represented by an equivalent circuit shown in Fig. 4.13. The two parts of the expression in (4.20) represent the emission and capture of electrons in the traps respectively, and are shown by two VCCSs in Fig. 4.13. Under steady-state conditions with no net capture or emission of electrons (or holes), $i_T = 0$ in (4.20). Thus, the relationship is derived between the input and output trap potential as

$$v_T = \frac{V_0}{1 + \exp\left(\frac{v_I}{k_B T}\right)}. \tag{4.21}$$

Furthermore, the characteristic frequency of the trapping effect on the current is given by

$$\omega = -\frac{1}{C_T}\frac{d}{dv_T} i_T = \omega_T \left[1 + \exp\left(\frac{v_I}{k_B T}\right)\right]. \tag{4.22}$$

The behavioral description of the relationship between the terminal potentials ($V_{gs}$ and $V_{ds}$) and the trap input potential ($v_I$) is given by

$$v_I = \alpha V_{gs} + \gamma V_{gd} - \phi \tag{4.23}$$

where $\alpha$, $\gamma$ and $\phi$ are fitting parameters. The trap potential $v_T$ is added to the applied gate-source voltage to implement the trapping effects into FETs similar to [159] as

$$I_{ds}(V_{gs}, V_{ds}, v_T, T) = f\left(V_{gs} + v_T, V_{ds}, T\right). \tag{4.24}$$

The model in [138] can predict the trapping characteristics such as kink effect, shift in the threshold voltage, change in the drain and source access resistance of the transistor etc. [160]. Furthermore, both electron and hole trapping processes in a single trap energy level have also been considered to create a comprehensive model [161]. The model parameters can be extracted from the drain-source current transient measurements [138].

SRH-theory based models are closely related to the capture and emission processes of electrons (or holes) [138, 159]. Therefore, the models have much wider voltage and temperature operational limit and can be used to predict the large-signal behavior under different operating conditions of a transistor.

## 4.5 Trap potential interaction with 2-DEG in a FET

Due to the non-accessibility of the trap terminal, the trap potential is often characterized or analytically computed from the drain-source current. Under isothermal conditions, a small change in the current in (4.24) is given by

$$\Delta I_{ds}(V_{gs}, V_{ds}, v_T, T) = g_m \Delta V_{gs} + g_m \Delta v_T + g_{ds} \Delta V_{ds}. \tag{4.25}$$

If the transistor is pulsed to the same $V_{gs}$ and $V_{ds}$ from two different $v_T$, eq. (4.25) is further simplified as

$$\Delta I_{ds}(V_{gs}, V_{ds}, v_T, T) = g_m \Delta v_T. \tag{4.26}$$

Thus, the change in $I_{ds}$ should be proportional to $g_m$. However, the measurements shown in Fig. 4.14 indicates a 50% change in $\Delta I_{ds}$ as opposed to merely 10% change in $g_m$ when $V_{ds}$ is varied from 4 V to 14 V. Thus, an offsetting $V_{gs}$ with $v_T$ according to (4.24) is not sufficient to accurately model the effects of traps in a large voltage operating range.

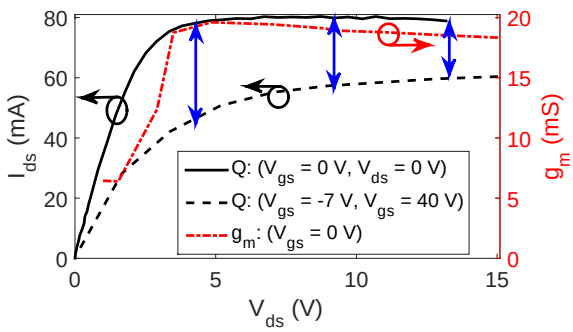



Figure 4.14: PIV measurement of $2 \times 50\mu$m GaN device from two different quiescent points ($V_{gs} = 0$ V, $V_{ds} = 0$ V) and ($V_{gs} = -7$ V, $V_{ds} = 40$ V)and small-signal transconductance (gm) along $V_{gs} = 0$ V. Arrows represent the amount of current suppression due to the change in quiescent bias point at three different $V_{ds}$.

The deep acceptor dopants required for the high resistive buffer have a non-uniform doping/distribution profile as illustrated in Fig. 4.1 [130,139]. A non-uniform distribution of the traps in the buffer provides a good balance between the current collapse and buffer leakage [162]. Therefore, the location of the traps and trapped electrons are most likely non-uniformly distributed in the buffer, unlike the electrons at the gate-interface. Such a distribution leads to a different interaction between the trapped electrons and the 2-DEG compared to the electrons at the gate-interface or the related $V_{gs}$. Therefore, the trap potential used in [138] can not be directly added to the gate-source voltage as described by (4.24). This is the reason why the difference in the relative change in $g_m$ and $\Delta I_{ds}$ is observed in Fig. 4.14.

Similar implementations are also observed in the models in [144,163]. Some models, e.g. [147–149,151,153,154,158,159] can also be observed to differentiate $V_{gs}$ and $v_T$ using a factor on the trap potential, or on the trap related current

in the respective models. The trap models in [147, 148] have a scaling factor allowing them to predict response under small-signal operation. For large-signal operations, nonlinear functions are used to create the error correction terms to predict the drain-source current in the models in [153,154]. Similarly, an amplification factor which is a function of the drain-source current is used in the model in [151]. The model in [159] has a back-gate transconductance factor multiplied with the trap (back-gating) potential, which is then added in the threshold voltage of the transistor model. This transconductance factor can be made nonlinear not only to distinguish the effect of $v_T$ from $V_{gs}$, but also to increase the voltage range of the transistor operation.

For the model in [138], the trap potential and $V_{gs}$ is differentiated by introducing a modulation factor in (4.24) according to [Paper D]

$$I_{ds}\left(V_{gs}, V_{ds}, v_T, T\right) = f\Bigg(V_{gs} + \underbrace{\alpha\left(V_{gs}, V_{ds}\right) \cdot v_T\left(V_{gs}, V_{ds}, T\right)}_{v_T^{\mathrm{Eff}}}, V_{ds}, T\Bigg). \quad (4.27)$$

Here, $\alpha$ is a function of the instantaneous $V_{gs}$ and $V_{ds}$, and $v_T^{\mathrm{Eff}}$ is the effective trap potential. The implementation according to (4.27) allows $\alpha$ to be extracted from pulsed-IV measurements using analytical techniques described later in this section.

The effect of $\alpha$ on $I_{ds}$ can be illustrated by looking at the change in the drain-source current due to the trap potential $v_T$ as shown in Fig. 4.14. For easier understanding, the function $f(\bullet)$ in (4.27) can be factorized according to

$$I_{ds}\left(V_{gs}, V_{ds}, v_T, T\right) \approx f_G(V_{gs} + \alpha v_T) f_D(V_{ds}) f_T(T) \quad (4.28)$$

where $f_G(\bullet)$, $f_D(\bullet)$ and $f_T(\bullet)$ represent the current dependence on the vertical electric-field through $V_{gs}$ and $v_T$, horizontal electric-field through $V_{ds}$ and temperature ($T$) respectively. If the isothermal conditions are assumed for a minimal change in the threshold voltage, a small variation in the drain-source current in (4.28) is given by

$$\begin{aligned}\Delta I_{ds}\left(V_{gs}, V_{ds}, v_T, T\right) &\approx f_D f_T \left(\frac{\partial f_G}{\partial V_{gs}}\Delta V_{gs} + \frac{\partial f_G}{\partial v_T}\Delta v_T\right) + f_G f_T \frac{\partial f_D}{\partial V_{ds}}\Delta V_{ds} \\ &\approx f_D f_T f_G' \left[\left(1 + \frac{\partial \alpha}{\partial V_{gs}} v_T\right)\Delta V_{gs} + \alpha \Delta v_T\right] \\ &\quad + f_T \left(f_G f_D' + f_D f_G' \frac{\partial \alpha}{\partial V_{ds}} v_T\right)\Delta V_{ds} \end{aligned} \quad (4.29)$$

where $f'(x) = \partial f(x)/\partial x$. For a small change in $v_T$, (4.29) gets simplified to

$$\begin{aligned}\Delta I_{ds}\left(V_{gs}, V_{ds}, v_T, T\right) &\approx \underbrace{f_D f_T f_G'}_{g_m}\Delta V_{gs} + \underbrace{f_D f_T f_G'}_{g_m}\alpha \Delta v_T + \underbrace{f_T f_G f_D'}_{g_{ds}}\Delta V_{ds} \\ \Rightarrow \quad \Delta I_{ds} &= g_m \Delta V_{gs} + g_m \alpha \Delta v_T + g_{ds}\Delta V_{ds}. \end{aligned} \quad (4.30)$$

Therefore, the change in $I_{ds}$ behavior due to two different $v_T$ related to the quiescent points as observed in Fig. 4.14 can be approximated by

$$\Delta I_{ds} = g_m \alpha \Delta v_T \quad (4.31)$$

where $\alpha$ modulates the transconductance $g_m$. This modulation factor along with the parameters of the trap model in [138] are extracted from the pulsed-IV and drain-source current transient measurements [Paper D].

## 4.6 Extraction procedure for the trap model in [Paper D]

The parameter extraction procedure for the trap model in [Paper D] involves three steps. The steps are briefly explained below, however for the detailed procedure, kindly refer to [Section IV, Paper D].

### (a) Extracting core-current model parameters

The first step is to extract the *core current model* ($I_{ds}^{\text{Core}}(V_{gs}, V_{ds})$) with the minimal effects of trapping and temperature. Therefore, pulsed-IV characteristics from the quiescent point $V_{gs} = V_{ds} = 0$ V are used to model the core current as the associated trap potential ($v_T$) is low in the absence of any electric-field [55, 142, 164–166]. The drain-source current transient measurements is used to identify the trap related time-constants. The latter is then used to determine the pulse-profile for the IV-measurements [Paper D].

The measured pulsed-IV characteristics can then be used to fit a current expression depending on the type of HEMT used to obtain $I_{ds}^{\text{Core}}(V_{gs}, V_{ds})$. For the symmetrical GaN HEMT used in [Paper D], the current expression in [Paper C] is used.

### (b) Extracting trap model parameter $v_T^{\text{Eff}}$

The next step is to estimate $v_T^{\text{Eff}}$ in (4.27). $v_T$ and $\alpha$ can then be extracted from $v_T^{\text{Eff}}$ for measurements where the conditions for $v_T$ and $\alpha$ can be differentiated. The double-pulse measurement technique proposed in [167] is one such method where $v_T$ and $\alpha$ can be associated to the pre- and measure-pulse conditions respectively. This method is useful in the presence of faster trap transients.

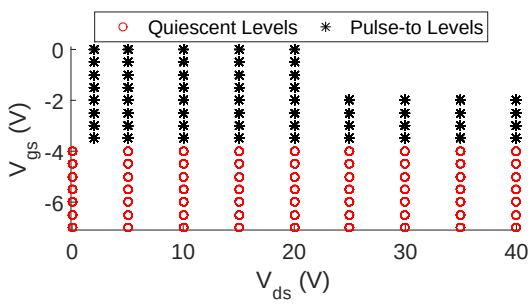



Figure 4.15: Selected pulse-to and quiescent voltage levels to extract the trap potential $v_T$ and modulating factor $\alpha$. The pinch-off of the GaN DUT is approximately $-3.9$ V.

Another simpler procedure to extract the parameters from pulsed-IV measurements is proposed in [Paper D]. Under the proposed procedure, it is important that the traps have negligible transients during the pulse in the mea-

surements used for extraction. The pulsed-IV measurements are performed from $n$ pulse-to and $m$ quiescent levels. The pulse-to points are in the active area, whereas the quiescent points are in the pinch-off region as shown in Fig. 4.15. $v_T^{\text{Eff}}$ is then estimated from the difference between the measured pulsed-IV current and the *core current* as

$$v_{T,(i,q)}^{\text{Eff}} = \arg\min_x \Big| I_{ds}^{\text{Core}}\left(V_{gs,(i)} + x, V_{ds,(i)}\right) - I_{ds}^{\text{Meas}}\left(V_{gs,(i)}, V_{ds,(i)}, V_{gs,(q)}, V_{ds,(q)}\right) \Big| \tag{4.32}$$

where $i$ and $q$ represent the pulse-to and quiescent voltage levels, respectively. Here, $v_{T,(i,q)}^{\text{Eff}}$ is the effective trap potential required to align the current model to the measured level within the pulse, and is given by

$$v_{T,(i,q)}^{\text{Eff}} = \alpha_{(i)} \cdot v_{T,(q)}. \tag{4.33}$$

Thereafter, the values of $\alpha_{(i)}$ and $v_{T,(q)}$ are obtained by minimizing the difference between the extracted $v_T^{\text{Eff}}$ in (4.32) and (4.33) as

$$\epsilon = \sum_{q=1}^{m}\sum_{i=1}^{n} \left| \alpha_{(i)} \cdot v_{T,(q)} - v_{T,(i,q)}^{\text{Eff}} \right|. \tag{4.34}$$

The trap transients are negligible during the measurements. The extracted $v_{T,(q)}$ is therefore used to estimate the $v_{I,(q)}$ according to

$$v_{I,(q)} = kT \ln\left(\frac{V_0}{v_{T,(q)}} - 1\right) \tag{4.35}$$

**(c) Extracting trap model parameter $\omega_T$**

The trap model parameter $\omega_T$ in [Paper D] is estimated from the extracted time-constant of the trapping effects observed in the drain-source current transient measurements. The transient response to a step change in $V_{ds}$ from 0 V to 20 V and 30 V is illustrated in Fig. 4.16.

$\omega_T$, together with the $\alpha$ and $v_I$ modeled using empirical expressions, are then implemented into the transistor current as shown in Fig. 4.17. The overall equivalent circuit for the transistor model is among the most complete presented. It implements nonlinear dc, RF, trapping and thermal effects.

## 4.7 Validation of the proposed trap model

The proposed model exemplified using a GaN transistor in [Paper D] is intended for nonlinear application (e.g. power amplifier). Therefore, apart from the dc- and pulsed-IV measurements, the model is validated with transient and load-pull measurements. The dc-IV characteristics of the model are compared to the measured behavior in Fig. 4.18(a). There is a good overall agreement in the response of the model. Furthermore, Fig. 4.18(b) shows a good agreement of the modeled and measurement pulsed-IV response for the DUT in

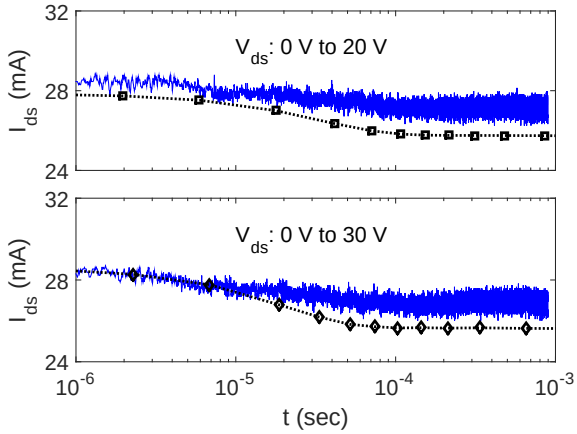



Figure 4.16: Comparison of the measured (−) and modeled (marker) transient response when the drain-source voltage across the DUT is stepped from 0 V to 20 V (top) and 30 V (bottom) respectively. The gate-source bias is fixed at −2.5 V.

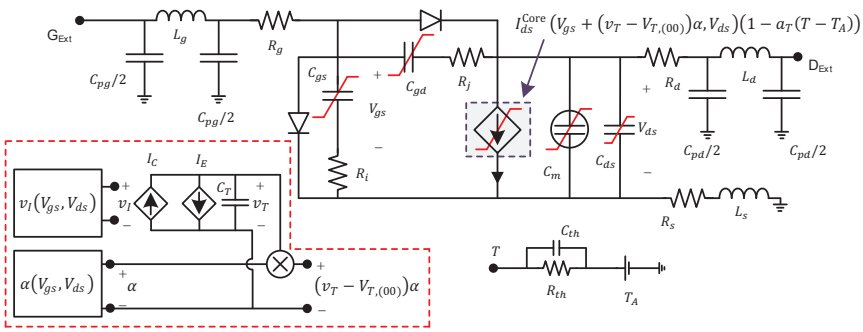



Figure 4.17: Transistor model in [Paper D] showing the extrinsic parameters, nonlinear capacitances modeled by the charge expressions, gate-diodes, an RC-branch thermal model on bottom right, and the trap model with the modulating factor $\alpha$ on bottom left. The VCCS implements the trapping effects $(v_T - V_{T,(0,0)}\alpha$ through $V_{gs}$, and the thermal effects in the *core current* model.

[Paper D]. The traps not just modulate the current in the 2-DEG, but also the resistivity of the drain and source access regions outside the influence of the gate contact. This, in turn, modulates the on-resistance and consequently a deviation in the knee region is observed in Fig. 4.18(b) [21].

The transient response of the model is already shown in Fig. 4.16, where the model is in correspondence to the measured behavior. The nonlinear characteristic of the model is validated with load-pull measurements where the load seen by the transistor is fixed at 10Ω and 500Ω. The transistor is excited with 2 GHz RF signal and calibrated incident and reflected waves at the gate and drain terminals are measured at the 1 dB compression point of the transistor. The model is then excited using the measured incident waves as described in Section 3.5, (for complete detail, refer to [Paper D, Section V]). Fig. 4.19 shows a comparison between the measured and modeled response of the transistor. The comparison reveals a good correspondence between the measured

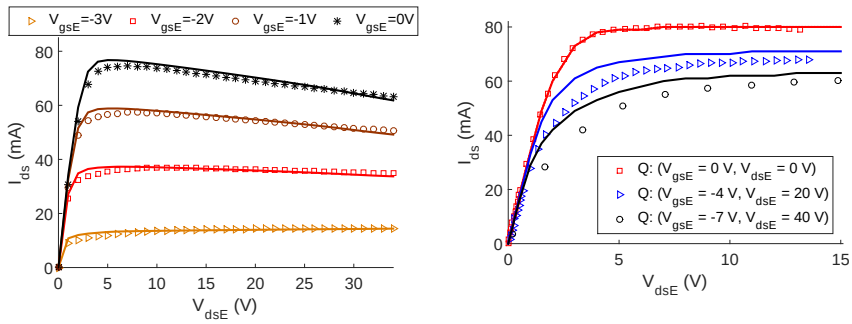



Figure 4.18: Comparison between the measured (marker) and modeled (-) (a) dc-IV characteristics, and (b) pulsed-IV characteristics from three different quiescent points.

and modeled response with the known discrepancy in the knee region.

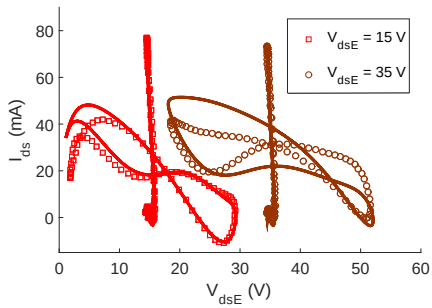



Figure 4.19: Comparison between the measured (marker) and modeled (-) (a) transient response to a stepped change in $V_{ds}$ with the gate-source bias fixed at $-2.5$ V, and (b) current-voltage waveforms at two different operating points ($V_{gsE} = -3$ V, $V_{dsE} = 15,\ 35$ V), where the impedance seen by the DUT is fixed at 10Ω and 500Ω.

## 4.8 Trapping Effect in field-plated (FP) devices

Field-plates (FPs) are used to increase the breakdown voltage of a transistor. These additional metallic structures, connected either to the gate or source metal contact, reduce the peak electric-field and increase the voltage operating range of a transistor [6,119]. The change in the electric-field due to the presence of the field-plate also changes the electron and ionized trap density profile in the buffer of the device [118]. Fig. 4.20 illustrates the ionized trap density profile in the buffer. The change in the ionized trap density profile from a non-field-plated to a field-plated device also reshapes how the trapped electrons modulate the number of carriers and the current in the 2-DEG. Such details are often studied with TCAD based physical models of a HEMT. However, TCAD based models can only be used if the information about the fabrication process of the device is available.

The empirical trap model in [Paper D] differentiates the trap potential

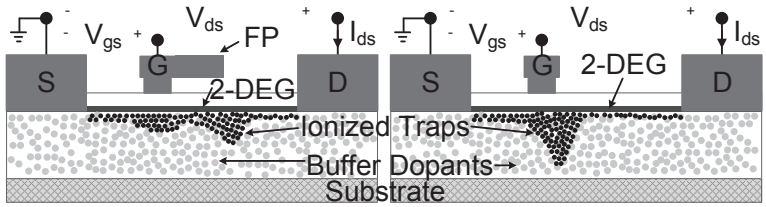



Figure 4.20: The cross-section of a FP (left) and non-FP (right) device showing typical distribution of ionized trap density in the buffer [118].

and the modulation factor. These parameters are related to the number of trapped electrons and their effect on the modulating the number of carriers in the 2-DEG, respectively. Therefore, the proposed trap model can be used to investigate the influence of addition of field-plates on the trapping effects. Hence, the parameters for the proposed trap model are extracted and compared for commercial GaN HEMTs with and without field-plates in [Paper E].

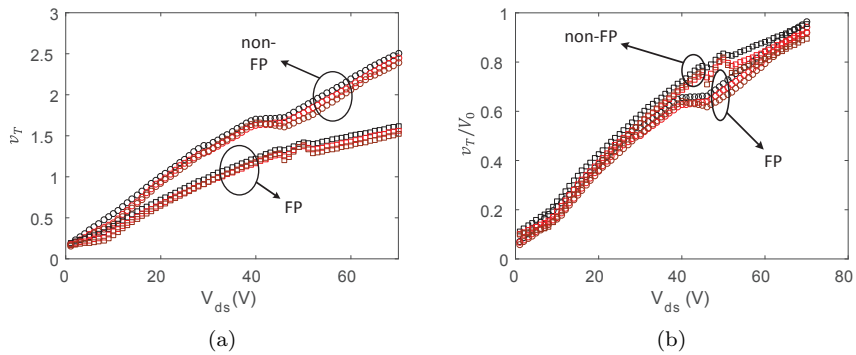



Figure 4.21: Comparison between the extracted trap parameters for the FP: □, non-FP: ○ devices for three different quiescent gate-source voltages (black: $V_{gs} = -6.5$ V, red: $V_{gs} = -5.5$ V, brown: $V_{gs} = -4.5$ V) : (a) $v_T$ vs. $V_{ds}$, and (b) $v_T/V_0$ vs. $V_{ds}$ [Paper D].

Fig. 4.21 compares the extracted trap potential for a commercial GaN HEMT with and without the field-plate. A higher trap potential is observed for the device without the field-plate. This is due to the higher peak electric-field injecting the electrons deeper into the buffer layer where trapping centers are present. However, the ratio of the trap potential to the maximum trap potential shown in Fig. 4.21(b) is observed to be similar for both the devices. Thus the ratio of the number of the trapped electrons to the number of available trap centres are similar in both devices. This clearly indicates that the trapping is essentially dependent on how deep the electrons are pushed into the buffer. Therefore, this can be linked to the peak electric-field in the device [Paper E].

Apart from the electric-field, field-plates also reshape the profile for electron and ionized trap density [118]. Compared to the device without the field-plate, the trapped electrons are closer to the 2-DEG and laterally more dispersed in the buffer between the gate and drain in the device with the field-plate. The distribution of trapped electrons (ionized traps) is illustrated in Fig. 4.20.

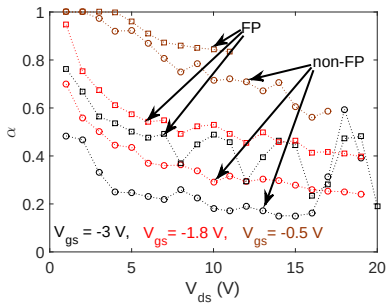



Figure 4.22: Comparison between the extracted modulation factor for the FP: □, non-FP: ○ devices for three different pulse-to gate-source voltages (black: $V_{gs} = -3$ V, red: $V_{gs} = -1.8$ V, brown: $V_{gs} = -0.5$ V) [Paper D].

It can be observed that the trapped electrons have a larger area available for influence and proximity to the 2-DEG for the field-plated device. These conditions make the 2-DEG more sensitive to the trapped electrons for the device with the field-plate. Hence, a higher modulation factor for the trap model in [Paper D] is observed as shown in Fig. 4.22.

The trapping effect is a product of both the trap potential and the modulation factor ($\alpha \cdot v_T$) as in (4.27). Therefore, the behavior observed in Fig. 4.21 and Fig. 4.22 indicate a clear trade-off between the two trap model parameters. Such a trade-off can not necessarily be observed in the comparison of the IV-characteristics [Paper E]. The observed trade-off is an interesting finding which requires further investigation to assess the benefit of field-plate with respect to the trapping effects. It appears that the benefit of the lower trap potential is counteracted by the increased modulation of the carriers in the 2-DEG by the trapped electrons. This prompts towards an investigation of optimized field-plate designs where an improved transistor performance is achieved with a lowered trap potential and not so significant rise in the modulation factor. Furthermore, the comparison of parameters of the trap model identifies the parameters to be further investigated for the development of a scalable trap model for varying field-plate dimensions.

## 4.9 Summary

This chapter has concentrated on the trapping effects and their models. A new model is proposed to take account of the distribution of the trapped electrons. Furthermore, the proposed model parameters are investigated for a field-plated device, which is attempt to take a first step towards a trap model scalable with respect to the field-plate dimensions.

# Chapter 5

# Conclusions and Future Work

## Conclusions

This thesis aims to simplify and improve FET models and their extraction procedures. It is by incorporating information about the device physics (e.g. symmetry, trapping theory) the accuracy and simplicity of empirical models can be improved. This is important since development of new products relies on accurate models and few design iterations.

For the microwave switches and resistive mixers wherein symmetrical devices are used, a new equivalent circuit was proposed in [Paper A]. The proposed model reduces the number of measurements required for the extraction of its parameters [Paper A]. The small-signal model parameter extraction procedure for the proposed model was further improved by using an optimizer based extraction along with the symmetry [Paper B]. It was shown that the extraction of only four out of the eight intrinsic parameters was sufficient when the measurements in both the positive and the negative drain-source voltage regions were used for a symmetrical transistor.

The symmetry in the extracted parameters for the proposed model was translated into the symmetry in the nonlinear model. This translation of symmetry allowed the reactive currents in the device to be modeled by a single common charge expression. Hence, the use of one charge expression simplified the nonlinear model [Paper A]. Furthermore, for GaN HEMTs, a new symmetrical current expression was developed in [Paper C] based on an existing model.

GaN HEMTs are ideal choice for high power RF applications due to a unique combination of high electron mobility and high breakdown electric field. However, they are also prone to trapping. The influence of the potential generated by the trapped electrons on the current in the 2-DEG is different from the gate-source voltage. Therefore, a new trap model was proposed in [Paper D] wherein, a modulation factor was introduced to distinguish the influence of trap potential. A parameter extraction procedure based on pulsed-IV measurements was also outlined for the trap model in [Paper D]. The field-plates used in transistors to suppress the peak electric-field also change the

number and distribution of the trapped electrons. Therefore, the proposed trap model was used to investigate trapping effects in the presence of field-plate [Paper E]. The investigation revealed that the proximity of the trapped electrons to the buffer, and the larger area available to interact with the 2-DEG increased the influence of trapped electrons on modulating the current in the 2-DEG in the presence of field-plate. The investigation also reveals the parameters to be invested further to build a trap model scalable with respect the field-plate dimensions.

The thesis has presented a built up for a transistor model covering from the small-signal, large-signal and trap model, and their parameter extraction procedure. This work aims to simplify the modeling procedure while improving the accuracy of the models. Simpler models with improved accuracy will assist circuit designers to harness the full potential of the transistor technology with first-time success. Thus, in turn, reducing the product development time and fueling the rapid growth in the wireless systems.

## Future Work

During the work with this thesis, several interesting topics for future work have emerged and are hereby listed:

- Improved charge models for symmetrical transistors.
  - Further work is required to improve the charge model developed for both GaAs and GaN DUTs. A common charge expression also opens up the possibility of modeling the nonlinear reactive part of a symmetrical device with fewer parameters.
- Symmetrical models for transistors in other technologies.
  - Except for transistors used in high power RF applications, commonly available transistors are symmetrical. Hence, the symmetrical model and the modeling procedure described in this thesis can be extended to other FET technologies.
- Trap model with multiple time-constants or activation energies.
  - Trapping often presents multiple time-constants and activation energies. Therefore, an accurate model must also consider the different time-constants as their individual effects would be dependent on the operating conditions such as temperature and applied voltages.
- Field-plate modeling.
  - Field plates in high power RF transistors disturb the intrinsic symmetry. Hence an investigation and comparison between intrinsic model parameters extracted for a symmetrical device, asymmetrical device with and without field-plates in the same technology would be interesting. This will give an insight on whether or not the field-plated transistors can be modeled using a symmetrical intrinsic core with a linear or nonlinear parameter corresponding to the effect of field-plates present in the device.

- Trap model scalable with field-plate dimension.
  - The investigation of the trap model parameters in [Paper E] indicates the model parameters which depend on the field-plate. Further investigations would open a scope to build a scalable trap model dependent on the length of the field-plate in a transistor.
- Models to evaluate process changes and materials.
  - Empirical models incorporated with physical information can also be used to evaluate how different GaN processing and material variations affect circuit behavior, as the process changes can be identified in the physical information embedded in the model.

# Acknowledgments

I would like to take this rare opportunity to express my gratitude to all the people who have been instrumental throughout my journey.

I want to begin with thanking Prof. Herbert Zirath, Prof. Jan Grahn, and my supervisors Prof. Christian Fager, Asst. Prof. Mattias Thorsell and Dr. Klas Yhland for their guidance throughout my work. I consider myself really lucky to be supervised by Christian and Mattias who through their guidance and encouragement sustained and nurtured my enthusiasm towards research. The discussions with Christian have often left me awed at his wide scope of experience and knowledge. Working with Mattias, especially in the lab, has been equally interesting where he taught me a whole lot about the minute details of measurements.

My research would not have been possible without the cooperation of my colleagues. I would like to thank all the personnel at MEL, especially Koen, Hans, Niklas, Dan, Iltcho, Vessen and Piotr with whom I have learned a lot through the discussions. I would also like to thank my friends whom I met and interacted with during my Ph.D. - César, Christer, Dhecha, Helena, Henric, Marcus, Mohammed, Mustafa, Olle, Paul, Sona, and many more. Seb, Will and Can, it was fun sharing the office and getting into some really random topics for discussion. The office and your company would be one of the first things I will miss outside Chalmers. I wish you and every one of my colleagues the very best in your future endeavors. I would also like to thank the industrial partners for interesting discussions, ideas and feedback.

Had it not been my Master's thesis supervisors, I probably would not have pursued Ph.D. Therefore, I would like to thank Prof. Animesh Biswas from IIT Kanpur and Prof. Danielle George from the Univ. of Manchester for opening the gate of a completely different world to me. I would also like to thank them for not letting me become another Software Engineer. I would also like to thank my tutor and teacher (late) Y. Bobby for encouraging me throughout my life.

I would also like to thank my family, my parents Sri Bineshwar Prasad and Smt. Savita Devi, my sisters Sweta and Smita, brother-in-laws Ranvijay and Rahul, who have always been a source of strength for me. A special mention for my sister Smita who decided that I should be sent to a boarding school at the age of eight, and that decision has been a turning point in my life. I want to take this opportunity to thank my (late) grandparents and the rest of my family. I have also been lucky to have found an equally loving family, and I would like to thank my parent-in-laws Sri Murli Manohar Baranwal and Smt. Anju Rani, sister-in-laws Saumya, Neha and Ankita, brother-in-laws Vineet

and Nitin for all the love and constant support they have given me. However, I will wait to thank Ankita until she files my income tax return!

The sparkle in the eyes of kids is the one thing that inspires me the most. I thank you Agastya, Ananya, Shlok, Shobhit, Vatsal and Vihaan for being an integral part of my life. You all have a special place in my heart and it will only grow bigger. Your playfulness always make me cherish my childhood. Thank you for reminding me that *there is a child in me still and sometimes not so still.*

Ph.D. has been a journey that I would never forget. Life during this journey for me has been like a box of chocolates. With each moment, there were quite many bittersweet surprises. However, none of them would have made any sense to me without a perfect partner. Thank you Sneha for being there with me. It is during the hard times one realizes how important it is to have a wonderful partner. And every time I would hear or use *Dr.* in my name, it will be a reminder of your selfless efforts which can not be expressed or described in words. Therefore, I dedicate this title to you my love.

Thank you Ashwini, Ayushi, Bala, Bhushan, Divya, Gyan, Haritha, Keerti, Prasanna, Praveen, Ritu, Shweta K., Shweta G., Siva, Srikar, Sumedh and Yogesh for being my family away from home. You all have made me experience different cultures and flavours from India drawing me closer to home.

And last but not the least, I would like to thank my friends from college Ammu, Azad, CDKey, Chauhan, DJ, Golu, Jaini, JB, Maate, Modi, Pappa, Peekay, Reddy, Sahoo, Sanki, Tingu, and Wind Singh. Sorry for ditching many of your plans, missing your marriage ceremonies. I truly understand now that *life happens to you when you are busy making other plans.* However, let us now plan and go for the trip that we all used to discuss.

While the list of people I feel compelled from within to thank is long, my limitations as a human being sadly makes this list not entirely exhaustive. I am really sorry to all of you (my extended family members, teachers and friends from school and college, colleagues, friends I met in Sweden and many more...) who do not find a special mention in here. I, however, as a person, am honoured to share a moment (or many) with you. I would like to thank you for the interactions, which however small, has definitely made an impact on my life.

*It has been said that something as small as the flutter of a butterfly's wing can ultimately cause a typhoon halfway around the world. - Chaos Theory*

This research has been carried out in the GigaHertz Centre in joint projects financed by the Swedish Governmental Agency of Innovation Systems (VINNOVA), Chalmers University of Technology, RISE (previously SP Technical Research Institute of Sweden), ComHeat Microwave AB, Ericsson AB, Infineon Technologies AG, Mitsubishi Electric Corporation, NXP Semiconductors BV, Saab AB, SweGaN AB and United Monolithic Semiconductors.

# Bibliography


[1] R. L. Ross, S. P. Svensson, and P. Lugli, *Pseudomorphic HEMT Technology and Applications*. Springer Science & Business Media, 2012, vol. 309.

[2] H. Störmer, R. Dingle, A. Gossard, W. Wiegmann, and M. Sturge, "Two-dimensional Electron Gas at a Semiconductor-Semiconductor Interface," *Solid state communications*, vol. 29, no. 10, pp. 705–709, 1979.

[3] M. A. Khan, J. Kuznia, J. Van Hove, N. Pan, and J. Carter, "Observation of a Two-dimensional Electron Gas in Low Pressure Metalorganic Chemical Vapor Deposited GaN-Al x Ga1- x N Heterojunctions," *Applied Physics Letters*, vol. 60, no. 24, pp. 3027–3029, 1992.

[4] A. Anwar, S. Entwistle, and C. Taylor, "Strategy Analytics Insight Current Status & Future Prospects for GaAs," 2004.

[5] A. Wakejima, K. Ota, K. Matsunaga, and M. Kuzuhara, "A GaAs-based Field-Modulating Plate HFET with Improved WCDMA Peak-Output-Power Characteristics," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1983–1987, 2003.

[6] S. Karmalkar and U. K. Mishra, "Enhancement of Breakdown Voltage in AlGaN/GaN High Electron Mobility Transistors Using a Field Plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, 2001.

[7] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. DenBaars, and U. Mishra, "High Breakdown GaN HEMT with Overlapping Gate Structure," *IEEE Electron Device Letters*, vol. 21, no. 9, pp. 421–423, 2000.

[8] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN-GaN HFET with a Field Modulating Plate," *IEEE Electron Device Letters*, vol. 24, no. 5, pp. 289–291, 2003.

[9] S. Karmalkar, M. S. Shur, G. Simin, and M. A. Khan, "Field-Plate Engineering for HFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2534–2540, 2005.

[10] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF Power Devices and Amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.

[11] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1764–1783, 2012.

[12] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs - An Overview of Device Operation and Applications," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1022–1031, 2002.

[13] E. Johnson, "Physical Limitations on Frequency and Power Parameters of Transistors," in *1958 IRE International Convention Record*, vol. 13. IEEE, 1966, pp. 27–34.

[14] J. E. Fisher and I. Bahl, *Gallium Arsenide IC Applications Handbook*. Elsevier, 1995.

[15] T. Kikkawa, "Recent Progress and Future Prospects of GaN HEMTs for Base-Station Applications," in *Compound Semiconductor Integrated Circuit Symposium, 2004. IEEE*. IEEE, 2004, pp. 17–20.

[16] K. Joshin, T. Kikkawa, S. Masuda, and K. Watanabe, "Outlook for GaN HEMT Technology," *Fujitsu Sci. Tech. J*, vol. 50, no. 1, pp. 138–143, 2014.

[17] Kazukiyo Joshin, Toshihide Kikkawa, Satoshi Masuda, Keiji Watanabe, "Outlook for GaN HEMT Technology," 2014. [Online]. Available: https://www.fujitsu.com/global/documents/about/resources/publications/fstj/archives/vol50-1/paper21.pdf

[18] P. Waltereit, W. Bronner, R. Quay, M. Dammann, M. Cäsar, S. Müller, R. Reiner, P. Brückner, R. Kiefer, F. Van Raay *et al.*, "GaN HEMTs and MMICs for Space Applications," *Semiconductor Science and Technology*, vol. 28, no. 7, p. 074010, 2013.

[19] K. Kikuchi, M. Nishihara, H. Yamamoto, T. Yamamoto, S. Mizuno, F. Yamaki, and S. Sano, "An 8.5–10.0 GHz 310 W GaN HEMT for Radar Applications," in *Microwave Symposium (IMS), 2014 IEEE MTT-S International*. IEEE, 2014, pp. 1–4.

[20] S. Yoshida, M. Tanomura, Y. Murase, K. Yamanoguchi, K. Ota, K. Matsunaga, and H. Shimawaki, "A 76 GHz GaN-on-Silicon Power Amplifier for Automotive Radar Systems," in *Microwave Symposium Digest, 2009. MTT'09. IEEE MTT-S International*. IEEE, 2009, pp. 665–668.

[21] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear Transistor Model Parameter Extraction Techniques*. Cambridge University Press, 2011.

[22] M. Henini and M. Razeghi, *Optoelectronic Devices: III Nitrides*. Elsevier, 2004.

[23] A. Vais, "Physical Simulation of GaN based HEMT," Master's thesis, Chalmers University of Technology, 2012.

[24] E. W. Faraclas and A. Anwar, "AlGaN/GaN HEMTs: Experiment and Simulation of DC Characteristics," *Solid-state electronics*, vol. 50, no. 6, pp. 1051–1056, 2006.

[25] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of Surface Defect Charge at AlGaN-GaN-HEMT Upon Schottky Gate Leakage Current and Breakdown Voltage," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 159–164, 2005.

[26] UC Berkeley Device Group, "Models - BSIM Group." [Online]. Available: http://bsim.berkeley.edu/models/

[27] R. Van Langevelde and F. M. Klaassen, "An Explicit Surface-Potential-Based MOSFET Model for Circuit Simulation," *Solid-State Electronics*, vol. 44, no. 3, pp. 409–418, 2000.

[28] A. Dasgupta, S. Ghosh, Y. S. Chauhan, and S. Khandelwal, "ASM-HEMT: Compact Model for GaN HEMTs," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on.* IEEE, 2015, pp. 495–498.

[29] I. Angelov, H. Zirath, and N. Rosman, "A New Empirical Nonlinear Model for HEMT and MESFET Devices," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2258–2266, 1992.

[30] K. Shirakawa, M. Shimizu, Y. Kawasaki, Y. Ohashi, and N. Okubo, "A New Empirical Large-Signal HEMT Model," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 4, pp. 622–624, 1996.

[31] Y. Chen, D. Ingram, H. Yen, R. Lai, and D. Streit, "A New Empirical IV Model for HEMT Devices," *IEEE microwave and guided wave letters*, vol. 8, no. 10, pp. 342–344, 1998.

[32] P. M. Cabral, J. C. Pedro, and N. B. Carvalho, "Nonlinear Device Model of Microwave Power GaN HEMTs for High Power-Amplifier Design," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2585–2592, 2004.

[33] M. Miller, T. Dinh, and E. Shumate, "A New Empirical Large Signal Model for Silicon RF LDMOS FETs," in *Wireless Applications Digest, 1997., IEEE MTT-S Symposium on Technologies for.* IEEE, 1997, pp. 19–22.

[34] L.-S. Liu, "An Improved Empirical Large-Signal Model for the GaAs- and GaN-based HEMTs," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 21, no. 3, pp. 343–352, 2011.

[35] D. E. Root, S. Fan, and J. Meyer, "Technology Independent Large Signal Non Quasi-Static FET Models by Direct Construction from Automatically Characterized Device Data," in *Microwave Conference, 1991. 21st European*, vol. 2. IEEE, 1991, pp. 927–932.

[36] M. F. Barciela, P. Tasker, M. Demmler, and E. Sanchez, "A Simplified Nonquasi-Static Table based FET Model," in *Microwave Conference, 1996. 26th European*, vol. 1. IEEE, 1996, pp. 20–23.

[37] J. Xu, D. Gunyan, M. Iwamoto, A. Cognata, and D. E. Root, "Measurement-based Non-quasi-static Large-Signal FET Model using Artificial Neural Networks," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. IEEE, 2006, pp. 469–472.

[38] J. Wood, P. H. Aaen, D. Bridges, D. Lamey, M. Guyonnet, D. S. Chan, and N. Monsauret, "A Nonlinear Electro-Thermal Scalable Model for High-Power RF LDMOS Transistors," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 2, pp. 282–292, 2009.

[39] L. Zhang and M. Chan, "Artificial Neural Network Design for Compact Modeling of Generic Transistors," *Journal of Computational Electronics*, pp. 1–8, 2017.

[40] D. E. Root, "Future Device Modeling Trends," *IEEE Microwave Magazine*, vol. 13, no. 7, pp. 45–59, 2012.

[41] B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*. Prentice-Hall, 2005.

[42] D. M. Pozar, *Microwave engineering*. John Wiley & Sons, 2009.

[43] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate Small-Signal Modeling of HFET's for Millimeter-wave Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 3, pp. 432–437, 1996.

[44] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 7, pp. 1151–1159, 1988.

[45] W. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 5, pp. 448–456, May 1980.

[46] W. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 33, no. 12, pp. 1383–1394, 1985.

[47] S. A. Maas and D. Neilson, "Modeling MESFETs for Intermodulation Analysis of Mixers and Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 12, pp. 1964–1971, 1990.

[48] W. Curtice, J. Pla, D. Bridges, T. Liang, and E. Shumate, "A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF LDMOS FETs," in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 2. IEEE, 1999, pp. 419–422.

[49] K. Yhland, N. Rorsman, M. Garcia, and H. Merkel, "A Symmetrical Nonlinear HFET/MESFET Model Suitable for Intermodulation Analysis of Amplifiers and Resistive Mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 1, pp. 15–22, 2000.

[50] C. Fager, L. Linner, and J. Pedro, "Optimal Parameter Extraction and Uncertainty Estimation in Intrinsic FET Small-Signal Models," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 12, pp. 2797–2803, 2002.

[51] M. Wren and T. J. Brazil, "Enhanced Prediction of pHEMT Nonlinear Distortion Using a Novel Charge Conservative Model," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, vol. 1. IEEE, 2004, pp. 31–34.

[52] A. Jarndal and G. Kompa, "A New Small-Signal Modeling Approach Applied to GaN Devices," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 11, pp. 3440–3448, 2005.

[53] A. E. Parker and S. J. Mahon, "Robust Extraction of Access Elements for Broadband Small-Signal FET Models," in *Microwave Symposium, 2007. IEEE/MTT-S International*. IEEE, 2007, pp. 783–786.

[54] W. Choi, G. Jung, J. Kim, and Y. Kwon, "Scalable Small-Signal Modeling of RF CMOS FET Based on 3-D EM-based Extraction of Parasitic Effects and its Application to Millimeter-wave Amplifier Design," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3345–3353, 2009.

[55] G. Callet, J. Faraj, O. Jardel, C. Charbonniaud, J.-C. Jacquet, T. Reveyrand, E. Morvan, S. Piotrowicz, J.-P. Teyssier, and R. Quéré, "A New Nonlinear HEMT Model for AlGaN/GaN Switch Applications," *International Journal of Microwave and Wireless Technologies*, vol. 2, no. 3-4, pp. 283–291, 2010.

[56] S. Takatani and C.-D. Chen, "Nonlinear Steady-State III–V FET Model for Microwave Antenna Switch Applications," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4301–4308, 2011.

[57] R. Minasian, "Simplified GaAs MESFET Model to 10 GHz," *Electronics Letters*, vol. 13, no. 18, pp. 549–551, 1977.

[58] T.-H. Chen and M. Kumar, "Novel GaAs FET Modeling Technique for MMICs," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1988. Technical Digest 1988., 10th Annual IEEE*. IEEE, 1988, pp. 49–52.

[59] M. Berroth and R. Bosch, "Broad-Band Determination of the FET Small-Signal Equivalent Circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 7, pp. 891–895, 1990.

[60] M. Thorsell, "Design and Characterization of a 2-Stage Silicon Carbide MESFET Amplifier," Master's thesis, Chalmers University of Technology, 2007.

[61] M. Ferndahl, C. Fager, K. Andersson, P. Linner, H.-O. Vickes, and H. Zirath, "A General Statistical Equivalent-Circuit-Based De-Embedding Procedure for High-Frequency Measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 12, pp. 2692–2700, 2008.

[62] E. Arnold, M. Golio, M. Miller, and B. Beckwith, "Direct Extraction of GaAs MESFET Intrinsic Element and Parasitic Inductance Values," in *Microwave Symposium Digest, 1990., IEEE MTT-S International*. IEEE, 1990, pp. 359–362.

[63] M. Berroth and R. Bosch, "High-Frequency Equivalent Circuit of GaAs FETs for Large-Signal Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 39, no. 2, pp. 224–229, 1991.

[64] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, "A New and Reliable Direct Parasitic Extraction Method for MESFETs and HEMTs," in *Microwave Conference, 1993. 23rd European.* IEEE, 1993, pp. 451–453.

[65] P. M. White and R. M. Healy, "Improved Equivalent Circuit for Determination of MESFET and HEMT Parasitic Capacitances from "Coldfet" Measurements," *IEEE microwave and guided wave letters*, vol. 3, no. 12, pp. 453–454, 1993.

[66] F. Lin and G. Kompa, "FET Model Parameter Extraction Based on Optimization with Multiplane Data-Fitting and Bidirectional Search - A New Concept," *IEEE Trans. Microw. Theory Techn.*, vol. 42, no. 7, pp. 1114–1121, 1994.

[67] J. Bandler, S. Chen, S. Ye, and Q. Zhang, "Robust Model Parameter Extraction Using Large-Scale Optimization Concepts," in *IEEE 1988 Int. Microwave Symposium Digest*, 1988, pp. 319–322.

[68] F. Lin and G. Kompa, "Efficient FET Model Parameter Extraction Using Multi-Plane Data-Fitting and Bidirectional Search Technique," in *Microwave Symposium Digest, 1993., IEEE MTT-S International.* IEEE, 1993, pp. 1021–1024.

[69] A. D. Patterson, V. F. Fusco, J. McKeown, and J. Stewart, "A Systematic Optimization Strategy for Microwave Device Modelling," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 3, pp. 395–405, 1993.

[70] C. Van Niekerk and P. Meyer, "A New Approach for the Extraction of an FET Equivalent Circuit from Measured S-Parameters," *Microwave and Optical Technology Letters*, vol. 11, no. 5, pp. 281–284, 1996.

[71] C. van Niekerk and P. Meyer, "Performance and Limitations of Decomposition-Based Parameter Extraction Procedures for FET Small-Signal Models," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 11, pp. 1620–1627, 1998.

[72] C. Van Niekerk, P. Meyer, D.-P. Schreurs, and P. B. Winson, "A Robust Integrated Multibias Parameter-Extraction Method for MESFET and HEMT Models," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 5, pp. 777–786, 2000.

[73] W. Shockley, "A Unipolar "Field-Effect" Transistor," *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365–1376, 1952.

[74] K. Asano, Y. Miyoshi, K. Ishikura, Y. Nashimoto, M. Kuzuhara, and M. Mizuta, "Novel High Power AlGaAs/GaAs HFET with a Field-Modulating Plate Operated at 35 V Drain Voltage," in *Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International.* IEEE, 1998, pp. 59–62.

[75] K. Chang, B. Epstein, E. Denlinger, and P. Gardner, "Zero Bias GaInAs MISFET Mixers," in *Microwave Symposium Digest, 1989., IEEE MTT-S International*. IEEE, 1989, pp. 1027–1030.

[76] K. Yhland, "Resistive FET Mixers," Ph.D. dissertation, Chalmers University of Technology, 1999.

[77] M. Thorsell, M. Fagerlind, K. Andersson, N. Billstrom, and N. Rorsman, "An X-band AlGaN/GaN MMIC Receiver Front-End," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 1, pp. 55–57, 2010.

[78] S. A. Maas, "A GaAs MESFET Mixer with Very Low Intermodulation," *IEEE Trans. Microw. Theory Tech.*, vol. 35, no. 4, pp. 425–429, 1987.

[79] M. D. Hodge, R. Vetury, J. Shealy, and R. Adams, "A Robust AlGaN/GaN HEMT Technology for RF Switching Applications," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE*. IEEE, 2011, pp. 1–4.

[80] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the Chalmers Nonlinear HEMT and MESFET Model," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 10, pp. 1664–1674, 1996.

[81] C. Fager, J. Pedro, N. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 12, pp. 2834–2842, Dec 2002.

[82] I. Angelov, V. Desmaris, K. Dynefors, P. Nilsson, N. Rorsman, and H. Zirath, "On the Large-Signal Modelling of AlGaN/GaN HEMTs and SiC MESFETs," in *Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005. European*. IEEE, 2005, pp. 309–312.

[83] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and Noise Properties of Gallium Arsenide Microwave Field-Effect Transistors," *Advances in electronics and electron physics*, vol. 38, pp. 195–265, 1975.

[84] L. Bengtsson, *Nonlinear Transistor Models for Microwave and Millimeterwave Circuits*, ser. Technical report L - School of Electrical and Computer Engineering, Chalmers University of Technology. , no: 220. Department of Microwave Technology, Chalmers University of Technology,, 1996, 50 s.

[85] Keysight Technologies, "Materka GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=5692606

[86] ——, "Modified Materka GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=10745514

[87] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET Device and Circuit Simulation in SPICE," *IEEE Trans. Electron Devices*, vol. 34, no. 2, pp. 160–169, 1987.

[88] Keysight Technologies, "TriQuint Scalable Nonlinear GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=10745300

[89] A. J. McCamant, G. D. McCormack, and D. H. Smith, "An Improved GaAs MESFET Model for SPICE," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 6, pp. 822–824, 1990.

[90] Y. Tajima, B. Wrona, and K. Mishima, "GaAs FET Large-Signal Model and its Application to Circuit Designs," *IEEE Trans. Electron Devices*, vol. 28, no. 2, pp. 171–175, 1981.

[91] I. Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman, V. Desmaris, M. Sudow, and H. Zirath, "Large-Signal Modelling and Comparison of AlGaN/GaN HEMTs and SiC MESFETs," in *Microwave Conference, 2006. APMC 2006. Asia-Pacific.* IEEE, 2006, pp. 279–282.

[92] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "Modeling GaN: Powerful but Challenging," *IEEE Microwave Magazine*, vol. 11, no. 6, pp. 82–96, 2010.

[93] O. Jardel, G. Callet, C. Charbonniaud, J. Jacquet, N. Sarazin, E. Morvan, R. Aubry, M.-A. D. F. Poisson, J.-P. Teyssier, S. Piotrowicz *et al.*, "A New Nonlinear HEMT Model for AlGaN/GaN Switch Applications," in *Microwave Integrated Circuits Conference, 2009. EuMIC 2009. European.* IEEE, 2009, pp. 73–76.

[94] D. E. Root, "Nonlinear Charge Modeling for FET Large-Signal Simulation and its Importance for IP3 and ACPR in Communication Circuits," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, vol. 2. IEEE, 2001, pp. 768–772.

[95] Keysight Technologies, "Curtice Quadratic GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=10745648

[96] ——, "Curtice Cubic GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=10745707

[97] ——, "Angelov Nonlinear GaAsFET Model." [Online]. Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=5692701

[98] C.-J. Wei, Y. A. Tkachenko, and D. Bartle, "An accurate large-signal model of gaas mesfet which accounts for charge conservation, dispersion, and self-heating," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 11, pp. 1638–1644, 1998.

[99] M. Thorsell, *Nonlinear Characterisation and Modelling of Microwave Semiconductor Devices.* Department of Microtechnology and Nanoscience, Microwave Electronics, Chalmers University of Technology, publisher=GigaHertz Centre, Chalmers University of Technology,,

place=Göteborg, year=2011, series=Technical report MC2 - Department of Microtechnology and Nanoscience, Chalmers University of Technology, no: 200, Doktorsavhandlingar vid Chalmers tekniska högskola. Ny serie, no: 3260, note=136,.

[100] S. McAlister, J. Bardwell, S. Haffouz, and H. Tang, "Self-Heating and the Temperature Dependence of the dc Characteristics of GaN Heterostructure Field Effect Transistors," *Journal of Vacuum Science & Technology A*, vol. 24, no. 3, pp. 624–628, 2006.

[101] M. Thorsell, K. Andersson, H. Hjelmgren, and N. Rorsman, "Electrothermal Access Resistance Model for GaN-based HEMTs," *IEEE Trans. ED*, vol. 58, no. 2, pp. 466–472, 2011.

[102] J. Joh, J. A. Del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, "Measurement of Channel Temperature in GaN High-Electron Mobility Transistors," *IEEE Trans. ED*, vol. 56, no. 12, pp. 2895–2901, 2009.

[103] Y.-R. Wu and J. Singh, "Transient Study of Self-Heating Effects in AlGaN/GaN HFETs: Consequence of Carrier Velocities, Temperature, and Device Performance," *Journal of Applied Physics*, vol. 101, no. 11, p. 113712, 2007.

[104] A. E. Parker and J. G. Rathmell, "Broad-Band Characterization of FET Self-Heating," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 7, pp. 2424–2429, 2005.

[105] Hewlett Packard, "High Frequency Transistor Primer Part III," 1998. [Online]. Available: http://www.hp.woodshot.com/hprfhelp/4_downld/lit/other/primer3.pdf

[106] C. Baylis and L. Dunleavy, "Understanding Pulsed IV Measurement Waveforms," in *Electron Devices for Microwave and Optoelectronic Applications, 2003. EDMO 2003. The 11th IEEE International Symposium on.* IEEE, 2003, pp. 223–228.

[107] M. Thorsell and K. Andersson, "Fast Multiharmonic Active Load–Pull System with Waveform Measurement Capabilities," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 1, pp. 149–157, 2012.

[108] E. Kohn, I. Daumiller, P. Schmid, N. Nguyen, and C. Nguyen, "Large Signal Frequency Dispersion of AlGaN/GaN Heterostructure Field Effect Transistors," *Electronics Letters*, vol. 35, no. 12, pp. 1022–1024, 1999.

[109] L. Eastman, "Results, Potential and Challenges of High Power GaN-Based Transistors," *physica status solidi (a)*, vol. 176, no. 1, pp. 175–178, 1999.

[110] C. Nguyen, N. Nguyen, and D. Grider, "Drain Current Compression in GaN MODFETs under Large-Signal Modulation at Microwave Frequencies," *Electronics Letters*, vol. 35, no. 16, pp. 1380–1382, 1999.

[111] A. Nakajima, H. Takayanagi, K. Itagaki, and K. Horio, "Analysis of Drain Lag and Current Slump in GaN-based HEMTs and MESFETs," in *Signals, Systems and Electronics, 2007. ISSSE'07. International Symposium on*. IEEE, 2007, pp. 193–196.

[112] S. J. Doo, P. Roblin, G. H. Jessen, R. C. Fitch, J. K. Gillespie, N. A. Moser, A. Crespo, G. Simpson, and J. King, "Effective Suppression of IV Knee Walk-out in AlGaN/GaN HEMTs for Pulsed-IV Pulsed-RF with a Large Signal Network Analyzer," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 681–683, 2006.

[113] A. Thomasian, N. Saunders, L. Hipwood, and A. Rezazadeh, "Mechanism of Kink Effect Related to Negative Photoconductivity in AlGaAs/GaAs HEMTs," *Electronics Letters*, vol. 25, no. 11, pp. 738–739, 1989.

[114] S.-H. Lo and C.-P. Lee, "Analysis of Surface State Effect on Gate Lag Phenomena in GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 9, pp. 1504–1512, 1994.

[115] J. Kuzmik, J.-F. Carlin, M. Gonschorek, A. Kostopoulos, G. Konstantinidis, G. Pozzovivo, S. Golka, A. Georgakilas, N. Grandjean, G. Strasser *et al.*, "Gate-lag and Drain-lag Effects in (GaN)/InAlN/GaN and InAlN/AlN/GaN HEMTs," *physica status solidi (a)*, vol. 204, no. 6, pp. 2019–2022, 2007.

[116] M. Rocchi, "Status of the Surface and Bulk Parasitic Effects Limiting the Performances of GaAs IC's," *Physica B+ C*, vol. 129, no. 1-3, pp. 119–138, 1985.

[117] R. Quay, *Gallium Nitride Electronics*. Springer Science & Business Media, 2008, vol. 96.

[118] N. Noda, R. Tsurumaki, and K. Horio, "Analysis of Lags and Current Collapse in Field-Plate AlGaN/GaN HEMTs with Deep Acceptors in a Buffer Layer," *Physica Status Solidi (c)*, vol. 13, no. 5-6, pp. 341–344, 2016.

[119] M. Kaddeche, A. Telia, and A. Soltani, "Study of Field Plate Effects on AlGaN/GaN HEMTs," in *International Conference on Microelectronics - ICM*, Dec 2009, pp. 362–365.

[120] W. Saito, T. Noda, M. Kuraguchi, Y. Takada, K. Tsuda, Y. Saito, I. Omura, and M. Yamaguchi, "Effect of Buffer Layer Structure on Drain Leakage Current and Current Collapse Phenomena in High-Voltage GaN-HEMTs," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1371–1376, 2009.

[121] S. Pearton, J. Zolper, R. Shul, and F. Ren, "GaN: Processing, Defects, and Devices," *Journal of applied physics*, vol. 86, no. 1, pp. 1–78, 1999.

[122] J. Ibbetson, P. Fini, K. Ness, S. DenBaars, J. Speck, and U. Mishra, "Polarization Effects, Surface States, and the Source of Electrons in

AlGaN/GaN Heterostructure Field Effect Transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, 2000.

[123] O. Mitrofanov and M. Manfra, "Poole-Frenkel Electron Emission from the Traps in AlGaN/GaN Transistors," *Journal of Applied Physics*, vol. 95, no. 11, pp. 6414–6419, 2004.

[124] F. Gao, D. Chen, H. L. Tuller, C. V. Thompson, and T. Palacios, "On the Redox Origin of Surface Trapping in AlGaN/GaN High Electron Mobility Transistors," *Journal of Applied Physics*, vol. 115, no. 12, p. 124506, 2014.

[125] S. Binari, K. Ikossi-Anastasiou, J. Roussos, D. Park, D. Koleske, A. Wickenden, and R. Henry, "GaN Electronic Devices for Microwave Power Applications," in *Proc. Int. Conf. GaAs Manufacturing Technology*, 2000, pp. 201–204.

[126] E. M. Chumbes, J. A. Smart, T. Prunty, and J. R. Shealy, "Microwave Performance of AlGaN/GaN Metal Insulator Semiconductor Field Effect Transistors on Sapphire Substrates," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 416–419, 2001.

[127] T. Huang, A. Malmros, J. Bergsten, S. Gustafsson, O. Axelsson, M. Thorsell, and N. Rorsman, "Suppression of Dispersive Effects in AlGaN/GaN High-Electron-Mobility Transistors using Bilayer SiNx Grown by Low Pressure Chemical Vapor Deposition," *IEEE Electron Device Letters*, vol. 36, no. 6, pp. 537–539, 2015.

[128] T. W. Weeks Jr, M. D. Bremser, K. S. Ailey, E. Carlson, W. G. Perry, and R. F. Davis, "GaN Thin Films Deposited via Organometallic Vapor Phase Epitaxy on A (6H)-SiC (0001) using High-temperature Monocrystalline AlN Buffer Layers," *Applied physics letters*, vol. 67, no. 3, pp. 401–403, 1995.

[129] M. Uren, K. Nash, R. Balmer, T. Martin, E. Morvan, N. Caillas, S. Delage, D. Ducatteau, B. Grimbert, and J. De Jaeger, "Punch-through in Short-channel AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395–398, 2006.

[130] S. Gustafsson, J.-T. Chen, J. Bergsten, U. Forsberg, M. Thorsell, E. Janzén, and N. Rorsman, "Dispersive Effects in Microwave AlGaN/AlN/GaN HEMTs with Carbon-doped Buffer," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2162–2169, 2015.

[131] Y. Wang, N. Yu, D. Deng, M. Li, F. Sun, and K. M. Lau, "Improved AlGaN/GaN HEMTs grown on Si substrates by MOCVD," in *Laser Physics and Laser Technologies (RCSLPLT) and 2010 Academic Symposium on Optoelectronics Technology (ASOT), 2010 10th Russian-Chinese Symposium on.* IEEE, 2010, pp. 68–71.

[132] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "Growth of Fe Doped Semi-insulating GaN by Metalorganic Chemical Vapor Deposition," *Applied Physics Letters*, vol. 81, no. 3, pp. 439–441, 2002.

[133] V. Desmaris, M. Rudzinski, N. Rorsman, P. Hageman, P. Larsen, H. Zirath, T. Rodle, and H. Jos, "Comparison of the DC and Microwave Performance of AlGaN/GaN HEMTs Grown on SiC by MOCVD with Fe-doped or Unintentionally Doped GaN Buffer Layers," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2413–2417, 2006.

[134] M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Chini, A. Pantellini, C. Lanzieri, A. Nanni, G. Meneghesso, and E. Zanoni, "Buffer Traps in Fe-doped AlGaN/GaN HEMTs: Investigation of the Physical Properties Based on Pulsed and Transient Measurements," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4070–4077, 2014.

[135] O. Axelsson, S. Gustafsson, H. Hjelmgren, N. Rorsman, H. Blanck, J. Splettstoesser, J. Thorpe, T. Roedle, and M. Thorsell, "Application Relevant Evaluation of Trapping Effects in AlGaN/GaN HEMTs with Fe-doped Buffer," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 326–332, 2016.

[136] W. Shockley and W. Read Jr, "Statistics of the Recombinations of Holes and Electrons," *Physical review*, vol. 87, no. 5, p. 835, 1952.

[137] R. N. Hall, "Electron-Hole Recombination in Germanium," *Physical review*, vol. 87, no. 2, p. 387, 1952.

[138] J. G. Rathmell, A. E. Parker *et al.*, "Circuit Implementation of a Theoretical Model of Trap Centres in GaAs and GaN Devices," in *Microelectronics: Design, Technology, and Packaging III, Proceedings of SPIE Conference on Microelectronics, MEMS and Nanotechnology*, vol. 6798, no. 1–11, 2007, p. 67980R.

[139] O. Axelsson, "Characterization of Trapping Effects, Robustness and Linearity in GaN HEMTs for High Power and Low Noise Microwave Amplifiers," Ph.D. dissertation, Chalmers University of Technology, 3 2016.

[140] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John wiley & sons, 2006.

[141] S. C. Binari, P. Klein, and T. E. Kazior, "Trapping Effects in GaN and SiC Microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048–1058, 2002.

[142] O. Jardel, F. De Groote, T. Reveyrand, J.-C. Jacquet, C. Charbonniaud, J.-P. Teyssier, D. Floriot, and R. Quéré, "An Electrothermal Model for AlGaN/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2660–2669, 2007.

[143] C. Camacho-Penalosa and C. Aitchison, "Modelling Frequency Dependence of Output Impedance of a Microwave MESFET at Low Frequencies," *Electronics Letters*, vol. 21, no. 12, pp. 528–529, 1985.

[144] J. M. Golio, M. G. Miller, G. N. Maracas, and D. A. Johnson, "Frequency-Dependent Electrical Characteristics of GaAs MESFETs," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1217–1227, 1990.

[145] M. Lee and L. Forbes, "A Self-Backgating GaAs MESFET Model for Low-Frequency Anomalies," *IEEE Trans. Electron Devices*, vol. 37, no. 10, pp. 2148–2157, 1990.

[146] S. U. Zaman, A. E. Parker *et al.*, "Modelling Electron Trapping Effects on Gate Lag in Field Effect Devices," in *Workshop on applications in Radio Science, Leura, Australia, Union Radio Science International, Commission C*, 2006, pp. 15–16.

[147] K.-i. Jeon, Y.-s. Kwon, and S.-c. Hong, "A Srequency Dispersion Model of GaAs MESFET for Large-Signal Applications," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 78–80, 1997.

[148] A. Santarelli, F. Filicori, G. Vannini, and P. Rinaldi, "'Backgating' Model Including Self-Heating for Low-Frequency Dispersive Effects in III-V FETs," *Electronics Letters*, vol. 34, no. 20, pp. 1974–1976, 1998.

[149] N. Matsunaga, M. Yamamoto, Y. Hatta, and H. Masuda, "An Improved GaAs Device Model for the Simulation of Analog Integrated Circuit," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1194–1199, 2003.

[150] A. E. Parker and D. J. Skellern, "A Realistic Large-Signal MESFET Model for SPICE," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 9, pp. 1563–1571, 1997.

[151] O. Jardel, F. De Groote, C. Charbonniaud, T. Reveyrand, J.-P. Teyssier, R. Quere, and D. Floriot, "A Drain-Lag Model for AlGaN/GaN Power HEMTs," in *Microwave Symposium, 2007. IEEE/MTT-S International*. IEEE, 2007, pp. 601–604.

[152] F. Filicori, G. Vannini, A. Mediavilla, and A. Tazon, "Modelling of Deviations Between Static and Dynamic Drain Characteristics in GaAs FETs," in *Microwave Conference, 1993. 23rd European*. IEEE, 1993, pp. 454–457.

[153] F. Filicori, G. Vannini, A. Santarelli, A. M. Sanchez, A. Tazon, and Y. Newport, "Empirical Modeling of Low-Frequency Dispersive Effects Due to Traps and Thermal Phenomena in III-V FET's," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 12, pp. 2972–2981, 1995.

[154] A. Jarndal, B. Bunz, and G. Kompa, "Accurate Large-Signal Modeling of AlGaN-GaN HEMT Including Trapping and Self-Heating Induced Dispersion," in *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on*. IEEE, 2006, pp. 1–4.

[155] T. J. Brazil, "A Universal Large-Signal Equivalent Circuit Model for the GaAs MESFET," in *Microwave Conference, 1991. 21st European*, vol. 2. IEEE, 1991, pp. 921–926.

[156] T. Fernandez, Y. Newport, J. M. Zamanillo, A. Tazon, and A. Mediavilla, "Extracting a Bias-Dependent Large Signal MESFET Model from Pulsed I/V Measurements," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 3, pp. 372–378, 1996.

[157] A. Raffo, A. Santarelli, P. Traverso, M. Pagani, F. Palomba, F. Scappaviva, G. Vannini, and F. Filicori, "Improvement of PHEMT Intermodulation Prediction Through the Accurate Modelling of Low-Frequency Dispersion Effects," in *2005 IEEE MTT-S International Microwave Symposium Digest.* IEEE, 2005, pp. 465–468.

[158] R. Leoni, M. S. Shirokov, J. Bao, and J. C. Hwang, "A Phenomenologically Based Transient SPICE Model for Digitally Modulated RF Performance Characteristics of GaAs MESFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 6, pp. 1180–1186, 2001.

[159] K. Kunihiro and Y. Ohno, "A Large-Signal Equivalent Circuit Model for Substrate-Induced Drain-Lag Phenomena in HJFETs," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1336–1342, 1996.

[160] S. A. Albahrani and A. E. Parker, "Classification of Trapping Characteristic in HEMTs," in *Microwave Integrated Circuits Conference (EuMIC), 2010 European.* IEEE, 2010, pp. 178–181.

[161] S. A. Albahrani, A. Parker, and M. Heimlich, "Circuit Model for Single-Energy-Level Trap Centers in FETs," *Solid-State Electronics*, vol. 126, pp. 143–151, 2016.

[162] C. Tang and J. Shi, "Influence of Acceptor-like Traps in the Buffer on Current Collapse and Leakage of E-mode AlGaN/GaN MISHFETs," *Semiconductor Science and Technology*, vol. 28, no. 11, p. 115011, 2013.

[163] S. D. Nsele, L. Escotte, J. Tartarin, S. Piotrowicz, and S. L. Delage, "Broadband Drequency Dispersion Small-Signal Modeling of the Output Conductance and Transconductance in AlInN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1372–1378, 2013.

[164] J. Rodriguez-Tellez, T. Fernandez, A. Mediavilla, and A. Tazon, "DC and Pulsed IV Characteristics of GaAs MESFET Devices," *Microwave Journal*, vol. 43, no. 5, pp. 328–328, 2000.

[165] J.-W. Lee and K. J. Webb, "A Temperature-Dependent Nonlinear Analytic Model for AlGaN-GaN HEMTs on SiC," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 1, pp. 2–9, 2004.

[166] S. Lai, C. Fager, D. Kuylenstierna, and I. Angelov, "LDMOS Modeling," *IEEE Microwave Magazine*, vol. 14, no. 1, pp. 108–116, 2013.

[167] A. Santarelli, R. Cignani, G. P. Gibiino, D. Niessen, P. A. Traverso, C. Florian, D. M.-P. Schreurs, and F. Filicori, "A Double-Pulse Technique for the Dynamic I/V Characterization of GaN FETs," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 132–134, 2014.