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Technical Report No. MC2-366
ISSN 1652-0769

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Chalmers Reproservice
Göteborg, Sweden October 2017

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Abstract

In order to push the upper frequency limit of high speed electronics further, thereby extending the range of applications, new device technologies and materials are continuously investigated. The 2D material graphene, with its intrinsically extremely high room temperature charge carrier velocity, is regarded as a promising candidate to push the frequency limit even further. However, so far most fabrication processes unintentionally introduce impurities at the interface between graphene and adjacent materials, which affect the performance. Additionally, due to the lack of a band gap, the important power gain parameter, the maximum frequency of oscillation ($f_{\max}$), is not impressively high.

In this thesis, results of the studies of the effect of impurities on charge transport in a graphene field effect transistor (GFETs) are presented. This study was performed was done by, firstly, setting up a semi-empirical model describing the influence of impurities, i.e., interface states on capacitance and transfer characteristics at low electric fields and, secondly, by developing a method for studying the limiting mechanisms of the charge carrier velocity in the graphene channel at high electric fields.

It was found that uncertainties in the material parameters of graphene, such as the Fermi velocity, hamper the possibility to find the correct mobility value by direct measurements on a GFET. Furthermore, it was shown that remote optical phonons limit the saturation velocity and charge carriers emitted from interface states at high fields are preventing the current to saturate and, hence, restricting $f_{\max}$.

By studying the effects and the limitations set by impurities and other parasitic effects in the GFET it is possible to clarify strategies for further development of GFETs towards reliable performance and higher $f_{\max}$. As is shown in this work, it is necessary to develop a fabrication process which results in clean interfaces and adjacent materials with higher optical phonon energies than today.

Keywords: graphene, field-effect transistors, microwave devices, saturation velocity, traps, impurities, remote phonons, carrier transport, electron and hole mobility

List of publications

Appended papers

Paper A **M. Bonmann**, A. Vorobiev, J. Stake, and O. Engström. 'Effect of oxide traps on channel transport characteristics in graphene field effect transistors.' *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **35**, 01A115 (2017), doi:10.1116/1.4973904

Paper B **M. Bonmann**, M. A. Andersson, A. Vorobiev, and J. Stake. 'Charge carrier velocity in graphene field-effect transistors.' under review in *Applied Physics Letters.*

Other papers and publications

Paper a X. Yang, **M. Bonmann**, A. Vorobiev, and J. Stake. 'Characterization of Al_2O_3 gate dielectric for graphene electronics on flexible substrates.' *2016 Global Symposium on Millimeter Waves (GSMM) & ESA Workshop on Millimetre-Wave Technology and Applications*, IEEE (2016). doi:10.1109/GSMM.2016.7500326.

Nomenclature

$a_{\text{c-c}}$	≈ 1.42 Åcarbon-carbon bond length
a_{o}	lattice constant
a_1, a_2	primitive vectors
A, B	in-equivalent atom sites
c_{o}	$\approx 3 \times 10^8$ m/s speed of light in vacuum
C_{ds}	stray capacitance between electrodes
C_{g}	gate capacitance
C_{gd}	gate-drain capacitance
C_{gs}	gate-source capacitance
C_{int}	interface capacitance
C_{ox}	oxide capacitance
C_{pg}	gate pad capacitance
C_{pd}	drain pad capacitance
C_{q}	quantum capacitance
C_{t}	total capacitance
e	$\approx 1.602 \times 10^{-19}$ C elementary charge
e_{n}	tunneling emission and capture rates
E	energy
E_{g}	energy bandgap
E_{F}	Fermi level, chemical potential
$f_{\text{T-int}}$	intrinsic transit frequency
$f_{\text{max-int}}$	intrinsic maximum frequency of oscillation
$f(E, E_{\text{F}})$	Fermi-Dirac distribution
g_{ds}	drain conductance
g_{m}	intrinsic transconductance
$g_{\text{m,ext}}$	terminal transconductance
h	Planck constant
$\hbar$	reduced Planck constant
h_{21}	short circuit current gain
I_{d}	drain current
J	current density
k_{x}, k_{y}	coordinate components of the wave vector
k	Boltzmann constant
l	mean free path
l_{a}	ungated access length
L	gate length
$L_{\text{d}}, L_{\text{s}}, L_{\text{g}}$	lead inductances
m^*/m_{e}	electron effective mass
n	charge carrier concentration
n_{g}	charge carrier concentration by Eq. 4.8
n_{e}	concentration of electrons
n_{h}	concentration of holes

n_0	residual charge carrier concentration
n_{imp}	charged impurity concentration
N_{ia}	acceptor-like interface state density
N_{id}	donor-like interface state density
N_{int}	interface state density
Q_{g}	charge in graphene
Q_{int}	interface charge
Q_{ox}	oxide charge
R_1, R_2, R_3	nearest neighbour vectors
R	measured resistance
R_{c}	metal-graphene contact resistance
R_{C}	$= R_{\mathrm{d}} + R_{\mathrm{s}}$ contact resistance as in Paper A
R_{d}	drain resistance
R_{g}	gate resistance
R_{i}	charging resistance
R_{s}	source resistance
S, S_{12}, S_{21}	S-parameter matrix, S-parameter matrix elements
T	temperature
T_{F}	Fermi temperature
t_{ox}	oxide thickness
U	unilateral power gain
v	velocity
v_{drift}	drift velocity
v_{F}	$\approx 10^6$ m/s Fermi velocity
v_{sat}	saturation velocity
V_{ch}	channel potential
V_{dir}	voltage at Dirac point
V_{ds}	drain voltage
V_{g}	gate voltage
W	gate width
γ	neares neighbour overlap
ε	electric field
ϵ_0	vacuum permittivity
ϵ_{ox}	relative dielectric permittivity
κ	thermal conductivity
μ_0	low-field mobility
ρ	resistivity
σ	conductivity
t, t_{eff}	scattering time, effective scattering time
τ_{int}	intrinsic delay time
τ_{pad}	pad delay time
τ_{tot}	total delay time
Φ_{ms}	work function difference
ω	angular frequency

Abbreviations

Al_2O_3	aluminium oxide
ALD	atomic layer deposition
CMOS	complementary metal-oxide-semiconductor
CNT	carbon nano tube
CVD	chemical vapour deposition
DOS	density of states
FET	field effect transistor
GaAs	gallium arsenide
GaN	gallium nitride
GFET	graphene field effect transistor
h-BN	hexagonal boron nitride
HEMT	high electron mobility transistor
IF	intermediate frequency
InAs	indium arsenide
InP	indium phosphide
$LiNbO_3$	lithium niobium oxide
MESFET	metal-semiconductor field effect transistor
MOSFET	metal oxide semiconductor field effect transistor
PET	polyethylene terephthalate
SiC	silicon carbide
SiO_2	silicon oxide
RF	radio frequency
THz	terahertz

Contents

Chapter 1

Introduction

Today, electronic devices, such as computers, tablets, radios and mobile phones, are part of our everyday lives. The elementary components of all electronic devices are solid-state transistors. For example, solid-state transistors switch between on and off states in the logical circuit of computers, and they serve as amplifiers in the receiver and transmitter circuitry of mobile phones. Since the first bulky transistor was demonstrated in 1947 by Shockley, Bardeen and Brattain, new technologies have been developed aiming for smaller and faster transistors. Regarding computers, the so-called Moore's law is frequently cited, which is the observation that the number of transistors on an integrated circuit doubles approximately every two years [1].

There is a vast amount of applications in the microwave (200 MHz to 300 GHz) and terahertz (300 GHz to 10 THz) regions of the electromagnetic spectrum. Applications in the microwave region range from communications to radar, GPS and many more. The field of terahertz (THz) frequencies is mostly limited to space applications, such as remote sensing and spectroscopy [2], because water in the earth atmosphere strongly attenuates THz radiation [3]. However, the application of THz in imaging systems for security [4], in diagnostic tools in medicine and life sciences [5] and in high-speed communication networks [6] has recently explored, thereby calling for faster transistors.

The first transistor was based on the semiconductor material germanium. Today, transistors based on silicon are the most common. The material is inexpensive, and the technology is very mature. Other successful transistor technologies are high-electron-mobility transistors (HEMTs) based on gallium arsenide (GaAs) [7] or indium phosphide (InP) [8]. Scaling of transistor dimensions has been a useful approach to increase the frequency, but at some point the fundamental scaling limit will be reached. Therefore, new technologies and materials with higher charge carrier velocities have to be found to continue the journey towards higher frequencies.

In 2004, Novoselov *et al.*[9] presented the field effect in graphene, thereby demonstrating that graphene can be fabricated. The 2D material graphene was first theoretically described in 1947 [10], but it was believed to be unstable. Since then, different methods have been employed to synthesise graphene: mechanical exfoliation [11], chemical vapour deposition [12], and intercalation on silicon carbide [13]. After graphene was successfully obtained by mechanical exfoliation, researchers proceeded to successfully apply the same method to bulk crystals of, for example, boron nitride (BN), molybdenum disulphide (MoS_2) and niobium triselenide ($NbSe_2$). The most interesting material in the context of graphene is hexagonal boron nitride since it is atomically flat and matches the graphene lattice very well. By sandwiching graphene flakes between two layers of h-BN, the high mobility in graphene is preserved [14]. In general, the stacking of different 2D materials provides the opportunity to explore a large variety of new applications, such as supercapacitors, photoconductors, p–n junctions, or low-dimensional magneto-optical nanostructures and

materials with multifunctional properties [15].

Graphene is unique in that it combines high room-temperature charge carrier velocity, high thermal conductivity, mechanical strength, bendability and transparency in a single material. Therefore, graphene has attracted considerable interest from the research community. The extremely high charge carrier mobility at room temperature [16] and the ease by which two-dimensional graphene can be included into already existing fabrication processes has made it a promising candidate as a channel material in field-effect transistors. The drawback of graphene is its lack of a bandgap. Therefore, it is not possible to efficiently use graphene in logic circuits. Rather, research focuses on applications on the analog side. Even in these applications, a bandgap would be desirable to obtain current saturation, as in the semiconductor pendant. Current saturation is a favourable state to obtain a transistor with a good power gain. Attempts to introduce a bandgap in graphene have been conducted, but opening a bandgap is accompanied by a strong decrease in charge carrier mobility and thus has not been considered a useful approach [17].

Power gain and current gain are important parameters in a transistor amplifier. The figures of merit related to the power and current gain are the maximum frequency of oscillation ($f_{\max}$) and the transit frequency (f_{T}), respectively. Graphene field-effect transistors (GFETs) perform well in terms of f_{T} (intrinsic f_{T}=427 GHz [18]) but in terms of $f_{\max}$ they cannot compete with state-of-the-art transistors based on other material systems, such as InAs PHEMTs with $f_{\mathrm{T}} = 644\,GHz$, $f_{\max} = 681\,GHz$ [19], GaAs mHEMT with $f_{\mathrm{T}} = 688\,GHz$, $f_{\max} = 800\,GHz$ [20], and InP HEMT with $f_{\max} = 1\,THz$ [8]. Recently, the performance of GFETs was increased by a clean self-aligned process up to an intrinsic $f_{\max}$=200 GHz [21, 22] on silicon carbide. When comparing the performance of GFETs it is important to distinguish between extrinsic and intrinsic parameters. The intrinsic values are obtained by de-embedding the measurements to exclude the effects of the parasitic capacitance, resistance, and inductance associated with the contact pads of the transistors [18].

A clean fabrication process and high-quality interfaces between graphene and adjacent materials are needed for good and reliable performance of GFETs. It has been shown that super-clean suspended graphene can actually reach the theoretically predicted mobility limit [23], but as soon as graphene comes into contact with another material, its mobility degrades severely due to the inclusion of impurities and remote phonons [24, 25]. In GFETs, there is at least one substrate-graphene interface involved, when the transistor is backgated, and even two interfaces have to be considered for a top-gated GFET. Additionally, due to impurities in the oxide and due to adsorbates at unprotected areas, the typical transfer and the capacitance versus gate voltage characteristics exhibit hysteresis [26]. This is caused by charge transfer in and out of interface states associated with impurities.

Therefore, it is important to study the effect of impurities on the charge transport in GFETs as is done in this work. In Paper A, a model was developed to describe how oxide traps affect the capacitance and transfer characteristics, and in Paper B, a method is demonstrated by which the effect of impurities on carrier velocity at high fields can be studied.

1.1 Thesis outline

The following chapters place the appended papers in a broader context. The thesis begins with a description of the electrical properties of graphene in Chapter 2, followed by an outline of the fabrication steps and characterisation techniques of graphene field-effect transistors in Chapter 3. Subsequently, the charge carrier transport dependence on temperature, charge carrier concentration and impurity concentration is discussed in Chapter 4. Then, the content of the appended papers is summarised in Chapter 5, and finally, the thesis ends with conclusions and a future outlook in Chapter 6.

Chapter 2

Properties of graphene for FET applications

The band structure and electrical properties of a monolayer of graphite, i.e., graphene, first theoretically described in 1947 by P.R. Wallace *et al.* [10]. However, it was not until 2004 that graphene was separated from graphite by K. S. Novoselov *et al.* [9] and its thermodynamic stability along with the electric field effect in graphene could be proven. The interesting electronic properties of graphene can be understood based on its physical configuration, which is described in this chapter. Furthermore, this chapter presents short descriptions of its thermal and optical properties.

2.1 Crystal structure and electronic band structure

Graphene is composed of a single layer of carbon atoms that are arranged in a hexagonal lattice. A carbon atom has four valence electrons. The orbital model of the carbon atoms in graphene is shown in Fig. 2.1(a). This figure illustrates where electrons are allowed to be localised in the atom. In graphene, the s2 orbital of the carbon atom is hybridised with the $2p_x$ and $2p_y$ orbitals to three sp2 orbitals that are equally spaced in the x-y-plane by an angle of 120°. The sp2 orbitals form strong covalent σ bonds between the carbon atoms with a carbon-carbon bond length of approximately $a_{\text{c-c}} \approx 1.42\,\text{Å}$, which leads to the hexagonal arrangement as shown in Fig. 2.1(b) and explains the mechanical strength of graphene. The third $2p_z$ orbital forms out-of-plane π bonds with the neighbouring carbon atoms, which allows electrons to move rather freely across the graphene sheet and is responsible for the notable electronic properties of graphene.

The lattice structure of graphene can be described by its primitive unit cell, which is indicated by the dashed parallelogram in Fig. 2.1(b). The basis of the unit cell is two inequivalent atom sites denoted as A and B. By repeating the unit cell along the primitive vectors $a_1 = (\sqrt{3}a/2, a/2)$ and $a_2 = (\sqrt{3}a/2, -a/2)$, where $a = \sqrt{3}a_{\text{c-c}}$ is the lattice constant and $a_{\text{c-c}} \approx 1.42\,\text{Å}$ is the carbon-carbon bond length, the entire graphene lattice is formed. From the description of the physical graphene lattice it is possible to find the electronic band structure, which describes the allowed energy states versus the momentum of the electrons in the graphene lattice. This is performed by solving the Schrödinger equation in a periodic structure [27]. A useful method to find an approximate analytic expression for the dispersion relation is the nearest-neighbor tight-binding model (NNTB) assuming electron-hole symmetry [28, 29]. The NNTB model assumes that the band structure can be found by the sum over the wave functions of the electrons at every atomic site, calculating the wave function assuming the atom to be isolated. An overlap integral is calculated by only taking the nearest neighbours into account, for example, for

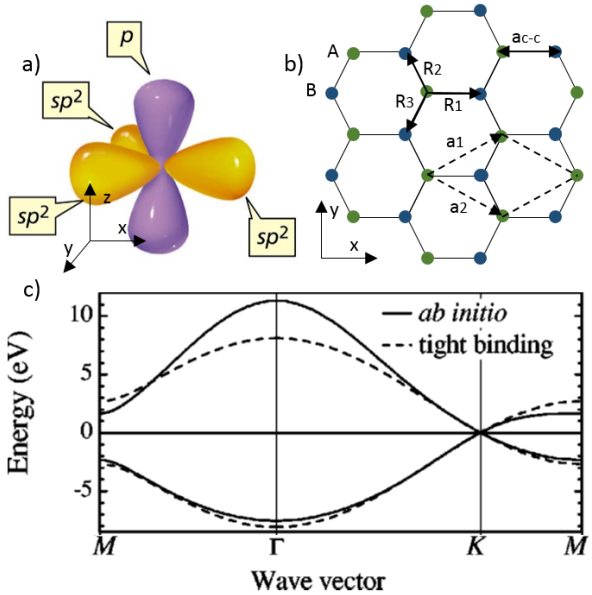

Figure 2.1: a) Orbital model of a carbon atom, [31]. b) The graphene lattice. The two inequivalent atom sites A (green dots) and B (blue dots) form the basis of the primitive unit cell indicated by the parallelogram (dashed lines). a_1 and a_2 are the primitive unit vectors (dashed arrows). R_1, R_2 and R_3 describe the separation between atom site A and its nearest-neighbour atoms. $a_{\text{c-c}} \approx 1.42$ Å is the carbon-carbon bond length. c) Comparison of the energy-momentum dispersion of ab initio calculations and the nearest-neighbour tight-binding approximation; adapted from [30].

an A atom this would be B atoms located at $R_1 = (a/\sqrt{3}, 0)$, $R_2 = (-a/2\sqrt{3}, -a/2)$ and $R_3 = (-a/2\sqrt{3}, a/2)$ relative to A.

The assumption of electron-hole symmetry allows us to neglect the contribution of the overlap integral and the approximate dispersion relation is found to be

$$E(k)^{\pm} = \pm\gamma\sqrt{1 + 4\cos\Big(\frac{\sqrt{3}a}{2}k_{\text{x}}\Big)\cos\Big(\frac{a}{2}k_{\text{y}}\Big) + 4\cos^2\Big(\frac{a}{2}k_{\text{y}}\Big)}, \tag{2.1}$$

where γ (typically between 2.7-3.1 eV) is the nearest neighbour overlap found by fitting Eq. 2.1 to ab initio calculations of the band structure at low energies (at the K point), as shown in Fig. 2.1(c) [29, 30]. k_{x} and k_{y} are the coordinate components of the wave vector. The + and - signs denote the signs for the conduction (π^*) and valence (π) bands, respectively. The dispersion relation centred at the K point can be further simplified to the linear relation (Fig. 2.2(a))

$$E(k)^{\pm} = \pm\hbar v_{\text{F}}\sqrt{k\text{x}^2 + k\text{y}^2}, \tag{2.2}$$

where $\hbar$ is the reduced Planck's constant and $v_{\text{F}} = 3\gamma a_{\text{c-c}}/2 \approx 10^6$ m/s$\approx c_0/300$, is the Fermi velocity, where c_0 is the speed of light in vacuum. Theoretically, the maximum

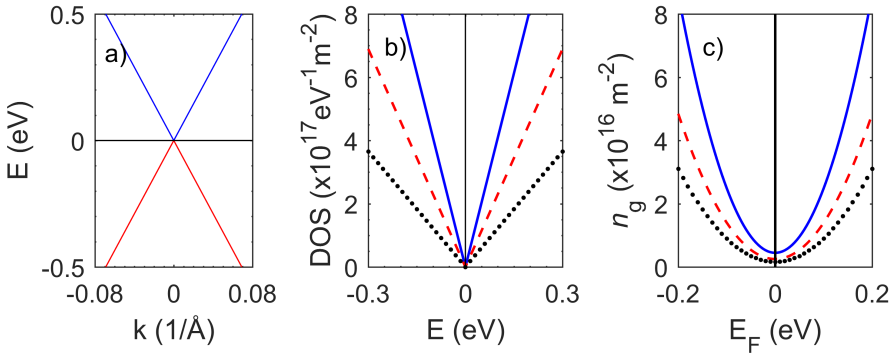

Figure 2.2: a) Linear dispersion relation of graphene using the approximation of Eq. 2.2. b) Density of states (DOS) and c) total charge carrier concentration for different Fermi velocities: $v_{\mathrm{F}} = 0.6$(solid line), 0.8 (dashed line), 1 (dotted line) $\times 10^6$ m/s.

charge carrier velocity at room temperature and at low charge carrier densities reduces to $v \approx 0.4 \times 10^6$ m/s due to acoustic phonon scattering. This will be further discussed in Chapter 4. The room temperature velocity in graphene is still greater than that in other semiconductor materials, which in combination with its unique combination of high thermal conductivity and mechanical properties motivates the interest for using graphene in high-frequency devices. The material properties of graphene and other common semiconductor materials are compared in Table 2.1. The given values of thermal conductivity, mobility, and saturation velocity might vary in the literature depending on the measurement conditions.

The dispersion relation of conventional semiconductor materials, such as silicon and gallium arsenide, is approximated by a parabolic function. In graphene, the dispersion relation is linearly approximated, and the electron states are described by the Dirac equation, similar to weightless particles. This is the reason why the cone-like shape of the energy band structure is called a Dirac cone, and the point where the valence and conduction bands touch ($E = 0\,\mathrm{eV}$) is called the Dirac point.

Properties	Graphene	Si	GaAs	GaN	InAs	InP
E_{g} (eV)	0	1.12	1.42	3.44	0.35	1.34
$m*/m_{\mathrm{e}}$	0 @V_{Dir}	0.98	0.06	1.5	0.02	0.08
μ (cm^2/V· s)	200000	1450	900	9000	33000	5400
v_{sat} ($\times 10^7$ cm/s)	5	1	0.7/2.7	1.4	0.9	0.7
κ (W/cm· K)	10-50	1.3	0.6	1.3	0.3	0.7

Table 2.1: Comparison of graphene properties at $T = 300\,\mathrm{K}$ with conventional semiconductors. E_{g} is the energy bandgap, $m*/m_{\mathrm{e}}$ is the electron effective mass, μ is the mobility, v_{sat} is the saturation velocity, and κ is the thermal conductivity [16, 32–37].

2.2 Charge carrier statistics

From the dispersion relation, the density of states (DOS) can be derived, which is the density of available states per energy interval. For graphene, the DOS has the following form [29]:

$$g(E) = \frac{2}{\pi(\hbar v_{\mathrm{F}})^2}|E|. \tag{2.3}$$

The DOS is inversely proportional to the square of the Fermi velocity. This involves a strong influence on the DOS when the Fermi velocity varies slightly, as shown in Fig. 2.2(b). It has been shown that the permittivity of the substrate on which graphene is placed influences the Fermi velocity [38]. This also entails a variation in the charge carrier concentration for varying Fermi velocity (Fig. 2.2(c)) since the DOS together with the Fermi-Dirac distribution

$$f(E_{\mathrm{F}}) = \frac{1}{1 + e^{(E-E_{\mathrm{F}})/kT}}, \tag{2.4}$$

where E_{F} is the Fermi energy, k is the Boltzmann constant and T is the temperature, is used to calculate the charge carrier concentration in the graphene sheet. For a given temperature and position of the Fermi level, the Fermi distribution describes the probability that an electron occupies an available energy state. The charge carrier concentrations of electrons, $n_{\mathrm{e}}(E_{\mathrm{F}})$, and holes, $n_{\mathrm{h}}(E_{\mathrm{F}})$, are derived as

$$n_{\mathrm{e}}(E_{\mathrm{F}}) = \int_0^\infty g(E)f(E, E_{\mathrm{F}})dE \tag{2.5}$$

and

$$n_{\mathrm{h}}(E_{\mathrm{F}}) = \int_{-\infty}^0 g(E)(1 - f(E, E_{\mathrm{F}}))dE. \tag{2.6}$$

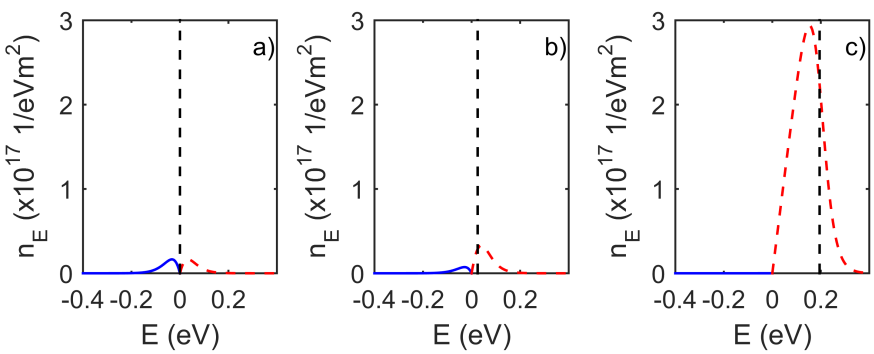

Figure 2.3: Charge carrier concentration of holes (solid line) and electrons (dashed line) for different positions of the Fermi level as indicated by the vertical dashed line.

The total charge carrier concentration $n_g(E_F)$ is given by the sum of electrons and holes:

$$n_g(E_F) = n_e(E_F) + n_h(E_F). \tag{2.7}$$

The total charge is given by the difference between electrons and holes times the elementary charge:

$$Q_g(E_F) = e(n_h(E_F) - n_e(E_F)) = -e \cdot \mathrm{sign}(E_F)\frac{4\pi E_F^2}{(hv_F)^2}. \tag{2.8}$$

For $E_F = 0\,\mathrm{eV}$, the density of occupied states per unit volume and energy (n_E) for holes and electrons is the same as that shown in Fig. 2.3(a). The area below the curves is equal to the charge carrier concentrations of electrons and holes derived by Eqs. 2.5 and 2.6. As soon as the Fermi level is shifted to more positive energies, the charge carrier concentration will be dominated by electrons (Fig. 2.3(b-c)). The position of the Fermi level is tuned by either doping graphene with impurity atoms or via the field effect by electrical gating [9].

2.3 Quantum capacitance

The quantum capacitance [39] needs to be considered in systems with a low density of states, such as two-dimensional materials and the inversion layer in a MOS transistor. In a parallel plate capacitor with a metal-insulator-metal configuration, the capacitance per unit area can be calculated from the geometric dimension using the simple expression

$$C_{ox} = \frac{\epsilon\epsilon_0}{t_{ox}}, \tag{2.9}$$

where ϵ_{ox} is the relative dielectric permittivity, ϵ_0 is the vacuum permittivity and t_{ox} is the thickness of the insulator. However, if one of the metal plates is replaced by a material with a low density of states, then the total capacitance (C_t) will be reduced due to the quantum capacitance (C_q) acting in series with the geometrical capacitance:

$$C_t = \frac{C_{ox} \cdot C_q}{C_{ox} + C_q}. \tag{2.10}$$

In the case that one of the capacitances is substantially lager than the other capacitance, the total capacitance can be approximated by the smaller capacitance, for example, when

$$C_q \gg C_{ox} \rightarrow C_t \approx C_{ox}. \tag{2.11}$$

Due to the low density of states in graphene, a small shift in the Fermi level noticeably changes the charge carrier concentration. C_q is defined as the derivative of the total charge (Q_g) in graphene with respect to the local electrostatic channel potential $V_{ch} = E_F/e$, and for pristine graphene, it can be expressed as follows [40, 41]:

$$C_q = \frac{\partial Q_g}{\partial V_{ch}} = \frac{8\pi e^2 kT}{(hv_F)^2} ln\Big[2 + 2\cosh\Big(\frac{E_F}{kT}\Big)\Big]. \tag{2.12}$$

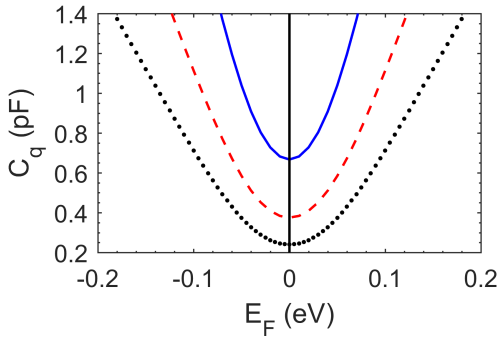

Figure 2.4: Calculated quantum capacitance using Eq. 2.12 for different Fermi velocities $v_F = 0.6$ (solid line), 0.8 (dashed line), 1 (dotted line) $\times 10^6$ m/s.

Again, the Fermi velocity enters the expression in the denominator and results in a reduction of C_q for larger values of v_F, as shown in Fig. 2.4.

During the fabrication process of graphene field-effect transistors, graphene is typically sandwiched between a substrate and a top-gate dielectric, and impurities are unintentionally introduced. Charged impurities introduce potential fluctuations across the graphene sheet, and the quantum capacitance can be modelled assuming a Gaussian distribution of the potential [42].

Since the quantum capacitance is directly related to the density of states, any distortion of the ideal graphene lattice that influences the electronic properties will affect the quantum capacitance. Distortions can be generated by doping with impurity atoms, by forming of nanoribbons (graphene strips with a width of a few nanometres) or by inducing strain [43–46].

2.4 Thermal and optical properties of graphene

Graphene has a strong anisotropy in thermal transport. In-plane thermal conductivity is very high due to the strong covalent σ bonds. Typically, the thermal conductivity in suspended single-layer graphene has values in the range $(1 - 5.30) \times 10^3$ W/m·K [32, 47]. The high in-plane thermal transport is beneficial for transistors; however, the thermal connection between graphene and the contact materials is a weak point [48] that needs to be carefully engineered. Graphene absorbs 2.3% of incident visible light [49]. For being atomically thin, this is a high fraction, but graphene is still transparent, which makes it interesting for the development of transparent, stretchable electrodes [50, 51].

Chapter 3

GFETs for RF applications

This chapter addresses the operating principle of field-effect transistors in general and the distinguishable features of graphene field-effect transistors (GFETs) that are associated with graphene-specific properties. Furthermore, the design and fabrication of GFETs is presented. Then, the figures of merit for RF transistors and the challenges when using graphene as a channel material are discussed.

3.1 Field-effect transistors

3.1.1 Operating principle of FETs

Field-effect transistors (FETs) are active electronic components that can be found in any electrical device. The name field-effect transistor arises from the utilisation of the field effect in this type of transistor. The field effect entails the modulation of the electrical conductivity between a drain and source terminal through the application of an out-of-plane electric field on the gate terminal. An in-plane electric field between the source and the drain drives the charge carriers along the channel [52]. The conductivity in the channel is either modulated by altering the channel height or by changing the charge carrier concentration in the channel. Junction field-effect transitors (JFETs) and metal-semiconductor field-effect transistors (MESFETs) belong to the former group, whereas in metal-oxide-semiconductor field-effect transistors (MOSFETs), high-electron-mobility transistors (HEMTs) and graphene field-effect transistors (GFETs), the carrier concentration is changed. In GFETs, it is even possible to change the majority charge carrier type in the channel because there is no bandgap in graphene.

There is a vast range of applications for transistors. The switching property of transistors is used in digital electronics, e.g. computers, whereas the amplifying property is used in receivers and transmitters. Furthermore, transistors are used in frequency multipliers, mixers, and detectors. The most commonly used transistor is the MOSFET. Over the past years, the gate length of MOSFETS has been continuously reduced to reach higher operating speeds. However, the scaling of the MOSFET technology is about to reach its limits. Therefore, the high charge carrier mobility and high saturation velocity in graphene have attracted attention for using graphene as a potential channel material in FETs. However, graphene has no bandgap. It is not possible to turn off a GFET, which makes it inapplicable for switching applications, where a high ratio between the on and off currents ($I_{\mathrm{ON}}/I_{\mathrm{OFF}}$) and a very small leakage current I_{OFF} are needed. For analog applications, power amplification at high frequencies is important, which requires the output current to saturate. To achieve current saturation a bandgap material is preferable. Attempts were made to induce a bandgap in graphene, but when inducing a bandgap,

the carrier mobility rapidly decreases. In conclusion, in terms of mobility and for a given bandgap, graphene does not offer a distinct advantage over conventional semiconductors [53]. Current saturation can also be achieved when the velocity of the charge carriers saturates [54]. This work considers the development of this approach.

Currently, a niche of GFET-based applications that does not directly require amplification, is under extensive development (mixers, power detectors and so forth [28, 55, 56]).

3.1.2 FET dc characteristics

The current density (J) in the channel of a field-effect transistor is determined by how many and how fast charge carriers can travel across the channel. The current density is expressed as

$$J = env_{\text{drift}}, \tag{3.1}$$

where e is the elementary charge, n is the charge carrier concentration, and v_{drift} is the charge carrier drift velocity. The charge carrier concentration n is modulated by the out-of-plane electric field, whereas the charge carrier drift velocity depends on the in-plane electric field between the source and drain. The field-dependent drift velocity is commonly modelled as follows [57]:

$$v_{\text{drift}} = \frac{\mu_0 \varepsilon}{(1 + (\mu_0 \varepsilon / v_{\text{sat}})^{\gamma})^{1/\gamma}}, \tag{3.2}$$

where ε is the in-plane electric field, μ_0 is the low-field mobility, v_{sat} is the saturation velocity of the charge carriers, and γ is a fitting parameter. At low electric fields the expression can be approximated by

$$v_{\text{drift}} \approx \mu_0 \varepsilon. \tag{3.3}$$

At high fields, the drift velocity saturates and approaches v_{sat}.

The direct current (dc) performance of FETs is characterised by measuring the drain and the gate currents under different bias conditions. The results are commonly presented in form of output characteristics (drain current versus drain voltage) and transfer characteristics (drain current versus gate voltage). The gate current is the leakage current through the gate and the drain current is the current through the channel. The applied gate voltage (V_{g}) and the drain voltage (V_{ds}) determine the strength of the out-of-plane and in-plane electric fields, respectively. The output and transfer characteristics of an ideal long-channel MOSFET can be modelled by the gradual channel approximation assuming uniform doping of the substrate [52, 58]. The ideal MOSFET characteristics are shown in Fig. 3.1 together with the characteristics of a typical GFET. It is apparent that the dc characteristics of the two devices differ significantly. As shown in Fig. 3.1(a), for the conventional semiconductor FETs, the drain current saturates at high drain voltages (high electric fields). The current saturation in semiconductor FETs is caused by velocity saturation and pinch-off of the channel. In contrast, a saturation plateau in the output characteristics of GFETs can be observed only for a small voltage range. The plateau is obtained in a condition where the in-plane and out-out-plane electric fields add up to

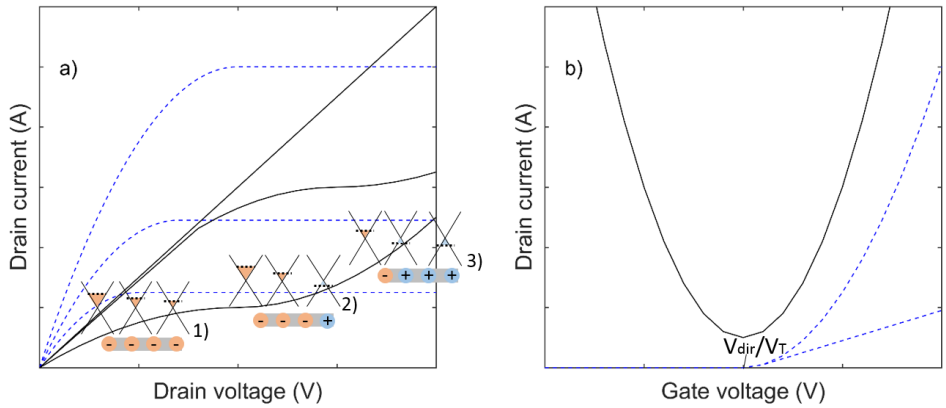

Figure 3.1: Typical a) output characteristic and b) transfer characteristic for semiconductor FETs (dashed lines) and GFETs (solid lines). 1)-3) illustrate the Dirac cone and the local position of the Fermi level within the graphene channel with $V_{\mathrm{g}} > 0$ and $V_{\mathrm{ds}} < 0$ with the source on the left-hand side and the drain on the right-hand side.

an effective electric field that moves the Fermi level to the Dirac point. Recalling the content of Chapter 2, this is the point where the charge carrier concentration reduces to a minimum. Because graphene has no bandgap, a further increase of the in-plane electric field changes the charge carrier type and the concentration of the charge carrier type in the channel. Therefore, the current continues increasing instead of saturating. Paper B discusses the issue of current saturation in GFETs in detail.

Another difference between GFETs and semiconductor analogies is shown in Fig. 3.1(b). The drain current of a semiconductor FET reduces to approximately zero below the threshold voltage (V_{T}). In contrast, the drain conductance in a GFET has a minimum at the Dirac voltage (V_{Dir}) and increases symmetrically around it. It is not possible to turn off a GFET due to the lack of a bandgap in graphene.

3.1.3 RF figures of merit of FETs

To benchmark analog radio frequency (RF) applications the important figures of merit are the maximum frequency of oscillation (f_{max}) and the transit frequency (f_{T}). The maximum frequency of oscillation is the frequency at which the unilateral power gain U is unity, and the transit frequency is the frequency at which the short-circuit current gain h_{21} is unity (0 dB). f_{max} and f_{T} of a device are estimated from S-parameters measured by a vector network analyser, calculating and extrapolating U and h_{21} to 0 dB using the fact that they roll off at a slope of -20 dB/dec with frequency. The expressions for f_{max} and f_{T} are derived from small-signal analysis of a linear two-port network. The unilateral gain is calculated in terms of the measured scattering parameter matrix S by [59]

$$U = \frac{|S_{12} - S_{21}|^2}{\det[\mathbf{1} - \mathbf{SS^*}]}. \tag{3.4}$$

When the input and output impedances are equal and real the short-circuit current gain can be expressed via S-parameters as follows [60]:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{3.5}$$

3.2 Graphene field-effect transistors

3.2.1 GFET layout and fabrication

The layout of the graphene field-effect transistor used in this work is shown in Fig. 3.2. The micrograph shows the top view on a double-finger GFET. The metal pads for probing the GFET constitute the largest part. The right-hand schematic shows a magnification of the actual gate-stack structure. The important layout parameters are the gate length L, the gate width W, the oxide thickness t_{ox} and the un-gated access length l_a between the gate and the source/drain contacts. The most general fabrication steps of a GFET are illustrated in Fig. 3.3. The process might vary from case to case. First, graphene needs to be transferred onto a substrate. The substrate is most commonly silicon covered by a 90 or 300 nm thick oxide layer (SiO_2). In this work, silicon, lithium niobate ($LiNbO_3$) and plastic (PET) were used as substrates. Second, a e-beam lithography is used to define the position of the transistor and to form the graphene mesa. The graphene mesa is defined by the size of the transistor channel plus the graphene area needed to apply the source/drain contacts. The graphene outside the active area is etched by oxygen plasma. In the next step, the source/drain contacts are patterned by e-beam lithography and 1 nm Ti/25 nm Pd/100 nm Au is deposited by e-beam evaporation followed by standard lift-off. In the next step, the Al_2O_3 gate oxide is deposited. To ensure good adhesion of the gate oxide, a seed layer is required. The seed layer is applied by e-beam evaporation of 1 nm Al followed by oxidation in air. This process is repeated 2-4 times. Then, atomic layer deposition of Al_2O_3 is perforemed until the required oxide thickness is obtained. After the deposition of the gate oxide, another e-beam lithography step is performed to form the 10 nm Ti/500 nm Au or 250 nm Al/10 nm Ti/50 nm Au gate contact. In the last step, the contact pads are formed using an e-beam lithography step and e-beam evaporation of

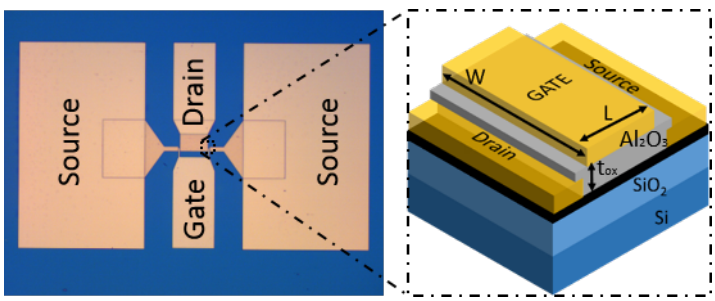

Figure 3.2: Layout of a GFET. The micrograph shows the top view of a GFET. The schematic is a magnification of the gate-stack structure.

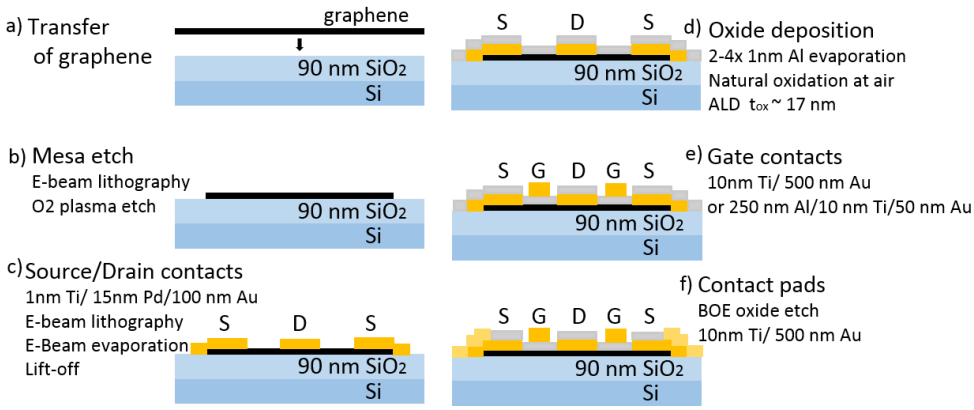

Figure 3.3: Fabrication steps of a GFET. a) Graphene is transferred onto a substrate. b) The graphene mesa is patterned by e-beam lithography. Graphene outside the active area is etched by oxygen plasma. c) E-beam lithography is used to define the areas for the source and drain contacts. E-beam evaporation followed by lift-off is used to apply the 1 nm Ti/15 nm Pd/100 nm Au contacts. d) Al_2O_3 is formed by 2-4 times of applying a 1 nm layer of Al by e-beam evaporation followed by oxidation in air. Then a 17 nm thick Al_2O_3 is applied using atomic layer deposition. e) A third e-beam lithography step followed by e-beam evaporation of 10 nm Ti/500 nm Au or 250 nm Al/10 nm Ti/50 nm Au and lift-off is needed to form the gate contact. f) Finally, the contact pads are formed in a final e-beam lithography step and e-beam evaporation of 10 nm Ti/500 nm Au.

10 nm Ti/500 nm Au. The silicon and lithium niobate samples were fabricated according to Fig. 3.3, whereas the order and number of the processing steps for the PET sample were slightly changed. For the PET sample, the graphene was tranferred and then immediately covered by a protective Al_2O_3 layer, which was formed from the natural oxidation of 2x1 nm evaporated Al. Then, the graphene mesa is formed. In the next step, the drain and source contacts and contact pads are patterned together, and in the final step, the gate oxide and gate contact plus contact pad are formed.

3.3 Synthesis of graphene

Originally, graphene was obtained by **mechanical exfoliation** from graphite using adhesive tape [9]. Graphite consists of stacked layers of graphene that adhere to each other by van der Waals forces. Using adhesive tape and repeatedly folding and unfolding the tape, the graphene layers can be detached from each other, until only one layer of graphene remains.

Following the first mechanical exfoliation of graphene, other synthesis processes have been developed. Graphene can be grown by **chemical vapour deposition (CVD)** on a catalyst material (most commonly copper) [61]. Another technique is the formation

of graphene by **intercalation on a silicon carbide crystal (SiC)**. This is performed under ultrahigh vacuum and at high temperatures, which are sufficient to sublimate silicon from the surface and leave the carbon-rich surface layer to transform to graphene [62]. Furthermore, graphene can be obtained by **liquid exfoliation** from graphite powder in a solvent using ultrasonication or sheer forces applied by a mixer to separate the graphene sheets [63, 64].

The graphene quality in terms of mobility is the highest in mechanically exfoliated graphene. However, only a limited number of small-sized graphene flakes can be fabricated at a time using this method. The mechanical exfoliation method has been optimised to obtain flake sizes of up to 500 μm [65]. Considering the combination of price for large-scale production and quality CVD graphene isthe most promising. CVD graphene can be grown at large scalea and then be transferred onto arbitrary substrates. The bottleneck is to developing a clean transfer method that results in an ultra-clean and atomically flat graphene layer that does not exhibit wrinkles or holes. The graphene used in this work is grown by CVD.

3.3.1 Raman spectroscopy

Raman spectroscopy is a fast and nondestructive characterisation tool that provides structural and electronic information about graphene sheets. Raman spectroscopy is often used after transferring CVD graphene from the copper foil onto the substrate to identify the graphene quality. The shape, intensities and positions of the characteristic peaks in the Raman spectrum povide information about any structural damage, unwanted dopants or chemical modifications of the graphene [66]. As shown in Fig. 3.4(a,top), the G peak and 2D peak are always present in the characteristic Raman spectrum. If defects are present, then the D peak and D' peak will appear in the spectrum (Fig. 3.4(a,bottom)). The ratio

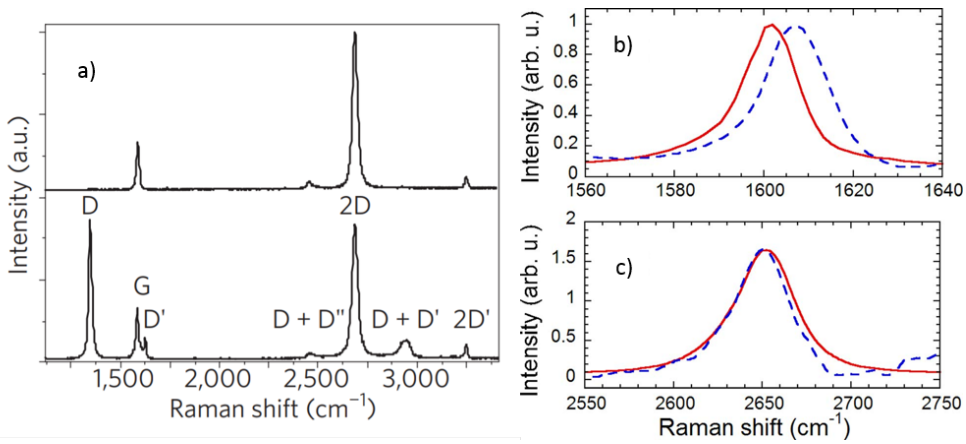

Figure 3.4: a) Raman spectra of pristine (top) and defective (bottom) graphene [66]. Raman spectra of the G peak b) and the 2D peak c) of graphene on SiO_2 (solid lines) and on $LiNbO_3$ (dashed lines) [67].

of the intensities of the G and the 2D peaks, or the full-width at half-maximum of the 2D peak, is often used to estimate the number of layers of graphene. Another peak that is related to interlayer coupling and that can be used to estimate the number of graphene layers is the C peak; however, this peak is not shown in Fig. 3.4. Figure 3.4,(b-c) shows the G peaks (b) and 2D peaks (c) of graphene on the SiO_2 (solid lines) and on $LiNbO_3$ (dashed lines) substrates used in this work. The intensity ratios are approximately 1.7 on both substrates. The different G peak positions indicate a slightly higher residual charge carrier concentration in graphene on the $LiNbO_3$ substrate.

3.3.2 Characterisation of the gate oxide

After fabricating the GFETs it is important to characterise the gate oxide. A high-quality oxide is important for good device performance. The effect of imperfections in the oxide on the transport characteristics will be discussed in Chapter 5 and Paper A.

A commonly used method is analysing capacitance versus gate voltage (C-V) measurements at different frequencies or temperatures to find relevant material parameters, such as the gate dielectric thickness, the dielectric constant, the oxide charge, and the doping profile of the substrate. C-V measurements are a good tool for characterising interfaces between materials and to find the interface state density [68]. Charge carriers moving in and out of interface states contribute to the total capacitance as an in-parallel acting capacitance. When measuring the capacitance at low frequencies, all interface states contribute to the total capacitance; at higher frequencies, the trapping-detrapping cannot follow the voltage variations fast enough, and the contribution of the interface capacitance is negligible. From the difference between the total capacitance at low and high frequencies, estimates of the interface state density can be made.

Another method for characterising a gate oxide is presented in Paper a. Dedicated parallel-plate capacitor test structures are characterised, using graphene on polyethylene terephthalate (PET) as a bottom electrode and gold as a top electrode. A source meter is used to measure the leakage current, and a LCR meter is used to measure the capacitance and the loss tangent. The analysis allows for finding the dielectric constant of the oxide and for determining the origin of losses.

To obtain further insights into the origin, distribution, and capture and emission rates of interface states, various analysis methods are available, such as conductance measurements [69], capacitance frequency spectroscopy [70], and multiparameter admittance spectroscopy [71].

3.3.3 High-frequency performance of GFETs

An important tool for modelling the RF performance of FETs, including GFETs, is the small-signal equivalent circuit with lumped elements as shown in Fig. 3.5. In small-signal modelling, the amplitude of the signal is assumed to be small enough such that the behaviour of the elements can be linearised around the bias point. In contrast, large-signal modelling requires consideration of non-linearities when a large signal is applied to describe the behaviour of the transistor. When all the elements of the small-signal equivalent circuit of a transistor are known, the resulting transistor model can be used for simulating

a full circuit.

The elements in the small-signal equivalent circuit correspond to actual physical effects in the transistor and can be extracted using S-parameter measurements at each applied bias of interest [72, 73]. The small-signal equivalent circuit consists of intrinsic and extrinsic elements. The intrinsic elements, which are shown in the dashed square in Fig. 3.5, are the gate-source and gate-drain capacitances (C_{gs} and C_{gd}) and the charging resistance for the gate-source capacitance (R_{i}). The extrinsic elements are the parasitic drain, source and gate resistances (R_{d}, R_{s} and R_{g}); the stray capacitance between electrodes (C_{ds}); the pad capacitances (C_{pg} and C_{pd}); and the bond and lead inductances (L_{d}, L_{s} and L_{g}).

Furthermore, the current source $g_{\mathrm{m}}V_{\mathrm{gi}}$ and the drain conductance $g_{\mathrm{ds}} = 1/r_{\mathrm{ds}}$ are part of the intrinsic device, where g_{m} is the intrinsic transconductance and g_{ds} is the drain conductance. The intrinsic transconductance is defined as the derivative of the drain current (I_{d}) with respect to the intrinsic gate voltage (V_{gi}):

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gi}}}\right|_{V_{dsi}=\mathrm{const.}}. \tag{3.6}$$

The drain conductance is the derivative of the drain current with respect to the intrinsic drain voltage (V_{dsi}):

$$g_{\mathrm{ds}} = \left.\frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{dsi}}}\right|_{V_{gi}=\mathrm{const.}}. \tag{3.7}$$

Meanwhile, the terminal transconductance is the derivative of the drain current with respect to the externally applied gate voltage (V_{g}):

$$g_{\mathrm{m,ext}} = \left.\frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{g}}}\right|_{V_{ds}=\mathrm{const.}}. \tag{3.8}$$

The intrinsic and extrinsic figures of merit , $f_{\mathrm{T\text{-}int}}$, $f_{\mathrm{max\text{-}int}}$ and f_{T}, f_{max}, respectively,

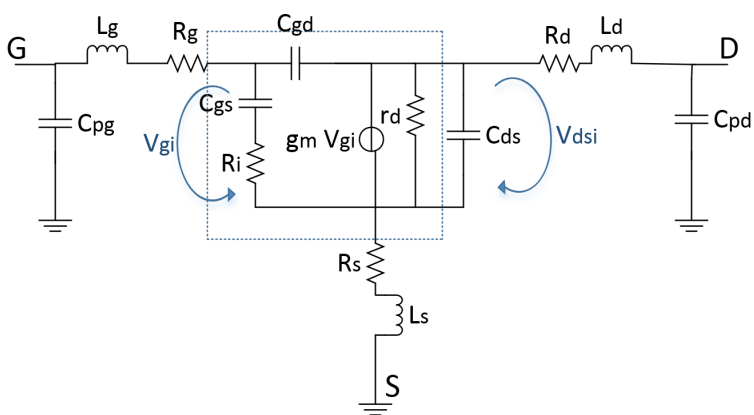

Figure 3.5: A small-signal equivalent circuit of a typical FET; adapted from [72].

can be approximated in terms of the small-signal equivalent circuit elements as [17, 74]

$$f_{\text{T-int}} = \frac{g_{\text{m}}}{2\pi(C_{\text{gs}} + C_{\text{gd}})}, \tag{3.9}$$

or expressed as the inverse of the transit time of charge carriers under the gate

$$f_{\text{T-int}} = \frac{1}{2\pi\tau}, \tag{3.10}$$

$$f_{\text{max-int}} = \frac{g_{\text{m}}}{4\pi C_{\text{gs}}} \times \frac{1}{\sqrt{g_{\text{ds}} R_{\text{i}}}}, \tag{3.11}$$

$$f_{\text{T}} = \frac{g_{\text{m}}}{2\pi(C_{\text{gs}} + C_{\text{gd}})} \frac{1}{1 + g_{\text{ds}}(R_{\text{s}} + R_{\text{d}}) + \frac{C_{\text{gd}} g_{\text{m}}(R_{\text{s}} + R_{\text{d}})}{C_{\text{gs}} + C_{\text{gd}}}}, \tag{3.12}$$

$$f_{\text{max}} = \frac{g_{\text{m}}}{4\pi C_{\text{gs}}} \frac{1}{\sqrt{g_{\text{ds}}(R_{\text{i}} + R_{\text{s}} + R_{\text{g}}) + g_{\text{m}} R_{\text{g}} \frac{C_{\text{gd}}}{C_{\text{gs}}}}}. \tag{3.13}$$

Apparently, the values of the circuit elements are defined by the design of the transistor, and thus, f_{T} and f_{max} can be optimised by a careful transistor design. In general, g_{m} should be as high as possible, and all the other elements should be minimised.

To obtain high f_{T}, the resistances R_{d} and R_{s} need to be reduced [75]. In this work, the drain and source resistances are considered to be equal due to the symmetric layout of the GFETs. Additionally, the resistances consist of the metal-graphene contact resistance R_{c} and the access resistance of the channel R_{ac}; accordingly, $R_{\text{d}} = R_{\text{s}} = R_{\text{c}} + R_{\text{ac}}$. The access resistance is the resistance of the ungated channel region. R_{ac} can be reduced by shortening the access length, by using self-aligned structures [76] or by employing side contacts [14]. Furthermore, the extrinsic fringing field capacitances can be decreased by optimising the oxide thickness [77]. However, when the oxide thickness is reduced, the

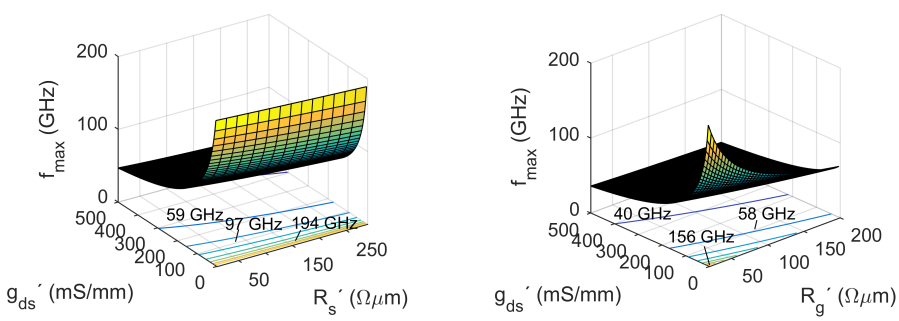

Figure 3.6: a) Effect of R'_{s} and g'_{ds} on f_{max} and b) effect of source resistance normalised to gate width R'_{g} and g'_{ds} on f_{T} calculated using Eq. 3.13 and Eq. 3.12, respectively, with parameters extracted from the devices described in Paper B.

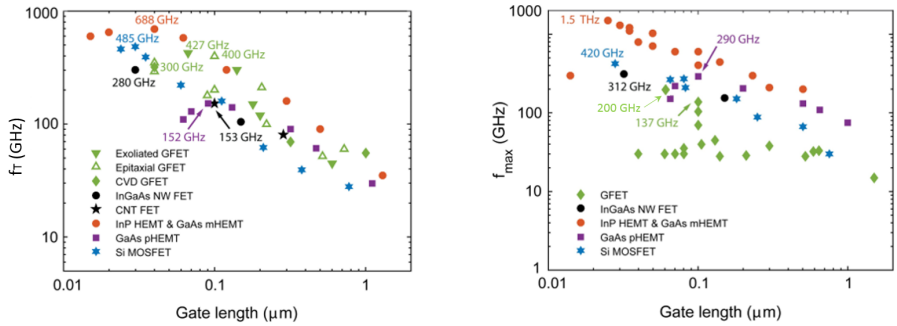

Figure 3.7: State-of-the-art de-embedded a) f_T and b) f_{max} for HEMTs, Si CMOS, CNT [8, 17] and NW FETs [81, 82] compared to intrinsic GFETs [17, 18, 21, 22, 83, 84]; adapted from [85].

non-linear voltage-dependent quantum capacitance can no longer be neglected, which might set an inherent limit on the transistor performance [78]. f_{max} is mostly limited by the high drain conductance g_{ds} due to the lack of current saturation. The current in GFETs does not saturate via pinch-off, since graphene has no bandgap. Rather than pinch-off, the charge carrier type will change within the channel from one type to the other when the in-plane electric field is strong enough [79]. Another path to achieve current saturation is via velocity saturation, which is further discussed in Chapter 5.

Figure 3.6 shows the effects of the source and gate resistances and of the drain conductance on f_{max} evaluated using Eq. 3.13. The source and gate resistances are normalised to the gate width (R'_s, R'_g), and the drain conductance is normalised with respect to the gate length (g'_{ds}). g_m is found from de-embedded f_T of the transistor described in Paper B and using Eq. 3.9. The transistor in Paper B has a channel length of $L = 1\,\mu$m, a channel width of $W = 20\,\mu$m, Al_2O_3 as the gate oxide with a thickness of $t_{ox} = 18$ nm and a relative dielectric permittivity of $\epsilon_{ox} = 7.5$. The capacitances are approximated to be $C_{gs} = C_{gd} = C_{ox} \times W \times L/2$. As shown in Fig. 3.6(a), a lower drain conductance will result in a significant improvement of f_{max}, when R_s is kept constant. The reduction of R_s at a constant g_{ds} has less influence. Regardless, the contact resistance should be as small as possible since simulations of the drain current have shown that the contact resistance can shadow the current saturation effect in the transistor [80]. Thus, reducing of the contact resistance enhances the device performance. Figure 3.6(b) shows the dependence of f_{max} on the normalised gate resistance R'_g and drain conductance g'_{ds}. As shown, reductions in both g'_{ds} and R'_g while the other variable is kept constant improves f_{max}.

3.3.4 State-of-the-art RF GFETs

Figure 3.7 summarises the state-of-the-art $f_{T\text{-int}}$ and $f_{max\text{-int}}$. The graphs show that GFETs compete well with other transistor technologies when comparing f_T at similar gate lengths. An $f_{T\text{-int}}$ of 427 GHz was achieved in GFETs with a gate length of L =67 nm

using bilayer graphene on a silicon carbide (SiC) substrate [21]. However, GFETs perform quite poorly in terms of $f_{\max}$. This poor performance is due to the lack of a bandgap and the poor current saturation, which lead to a high drain conductance. Some research groups recently achieved improved $f_{\text{max-int}}$ of 105 GHz and 200 GHz for GFETs with gate lengths of $L = 100\,\text{nm}$ and $L = 60\,\text{nm}$, respectively [22, 83], with an extrinsic $f_{\max} = 106\,\text{GHz}$ for the GFETs with $L = 60\,\text{nm}$ [22]. In the former case, the research group used bilayer graphene on a SiC substrate and in the second case, CVD graphene transferred onto a SiO_2 substrate was used. A self-aligned fabrication process was used in both cases, thereby reducing the access length and hence the source resistance. Additionally, the transfer procedure of CVD graphene was improved, which protects the graphene from organic contamination.

The theoretically achievable intrinsic high-frequency performance limit of a top-gated GFET has been estimated to be approximately $f_{\text{T-int}}$=640 GHz at a channel length of 100 nm and approximately 3.7 THz at a channel length of 20 nm [86].

Chapter 4

Carrier transport in the GFET channel

The particular properties of graphene are its high charge carrier mobility and velocity. In this chapter, the dependencies of mobility and velocity on electric field strengths, temperatures, impurity concentrations and charge carrier concentrations for different scattering mechanisms, which are relevant for the analysis of the effect of impurities on charge transport in Chapter 5, are discussed. In literature there are different models available to explain conductivity or current measurements and the results and explanations differ depending on the calculation methods used and the considered scattering mechanisms.

4.1 Scattering, carrier mobility and velocity

The charge carrier mobility μ defines the relationship between the charge carrier drift velocity v_{drift} and the in-plane electric field ε. Different scattering mechanisms dominate under different bias conditions. Therefore, it is necessary to distinguish between transport under low electric fields and under high electric fields. The transfer characteristics discussed in Paper A and in Chapter 5 are conducted at low electric fields, while the analysis of the velocity in GFETs in Paper B is relevant for amplifier applications at high electric fields. Electric fields, where a linear relationship between electric field and drift velocity (Eq. 3.3) is a valid approximation, are understood to be low electric fields and the mobility is assumed to be independent of the electric field. Under higher electric fields, the velocity saturates and the mobility starts to be field dependent. Because of this differentiation, the low-field mobility is used as a quality parameter when GFETs are characterised under low fields, and the saturation velocity is used under high fields.

Experimentally, the dependences of conductivity, mobility, or resistivity of the temperature, the charge carrier concentration, and the electric field are often investigated to determine which are the dominating and limiting scattering mechanisms. The conductivity σ, mobility μ and resistivity ρ are related as follows:

$$\sigma = en\mu = 1/\rho. \tag{4.1}$$

The knowledge of the limiting scattering mechanism is used to decide which are the necessary steps to achieve a better device performance.

4.1.1 Scattering mechanisms

The mobility is proportional to the effective scattering time $\mu \propto t_{\text{eff}}$, which is the time that a mobile charge carrier can travel through an atomic lattice before it is

scattered. Therefore, the mobility can be considered as a measure of how easily the charge carriers can move. Scattering of charge carriers in the graphene lattice can occur via different mechanisms, which are categorised into intrinsic and extrinsic scattering. Whereas extrinsic scattering can be minimized by careful device design and an appropriate fabrication technology, intrinsic scattering is inherent to the graphene lattice and sets an upper limit on the achievable performance of GFETs. Intrinsic scattering is due to lattice vibration, i.e., optical and acoustical phonons, and scattering between charge carriers within graphene. Extrinsic scattering mechanisms are scattering at neutral and charged impurities, scattering at defects and remote phonon scattering at adjacent materials. Each scattering mechanism has its specific scattering time t, which typically depends on temperature T, charge carrier concentration n, concentration of charged impurities n_{imp}, and the electric field.

The measurements of the GFETs studied in this work were conducted at room temperatures. Additionally, they have generally a high charged impurity concentration n_{imp}. Therefore the most relevant scattering mechanisms at room temperature are acoustic phonon scattering with the scattering time inversely proportional to the temperature and charge carrier concentration [87, 88],

$$t_{\mathrm{AP}} \propto \frac{1}{T \cdot n}, \tag{4.2}$$

optical phonon scattering where the scattering time is inversely proportional to the charge carrier concentration,

$$t_{\mathrm{OP}} \propto \frac{1}{n}, \tag{4.3}$$

remote phonon scattering with an inverse proportionality to the square root of the charge carrier concentration,

$$t_{\mathrm{ROP}} \propto \frac{1}{\sqrt{n}}, \tag{4.4}$$

and long-range charged impurity scattering

$$t_{\mathrm{imp}} \propto \frac{1}{\sqrt{n_{\mathrm{imp}}}}. \tag{4.5}$$

When several scattering mechanisms are active at the same time they are approximated in an effective scattering time using Matthiessen's rule [89]:

$$\frac{1}{t_{\mathrm{eff}}} = \frac{1}{t_1} + \frac{1}{t_2} + ... + \frac{1}{t_{\mathrm{n}}}. \tag{4.6}$$

Resistivity vs temperature and charge carrier concentration has been studied by Ref. [16]. Intravalley optical phonon scattering was considered to be negligible due to the high phonon energy of $\omega^{g}_{\mathrm{OP}} \approx 200\,\mathrm{meV}$. However, the measured resistivity vs temperature curves cannot be explained by a model considering intravalley acoustic phonon scattering alone. The measured resistivity (ρ) diverges from a linear behaviour for $T > 150 - 200\,\mathrm{K}$. Therefore, remote interface polar optical phonon scattering is introduced as an additional scattering mechanism [16]

$$\rho(V_{\mathrm{g}}, T) = \rho_0(V_{\mathrm{g}}) + \rho_{\mathrm{A}}(T) + \rho_{\mathrm{rps}}(V_{\mathrm{g}}, T), \tag{4.7}$$

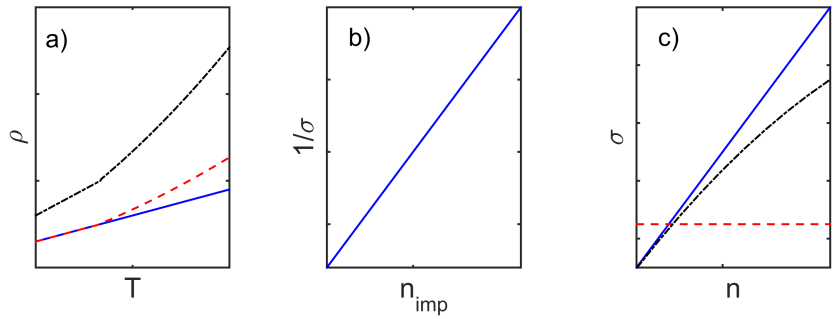

Figure 4.1: a) Qualitative resistivity versus temperature for different charge carrier concentration for acoustic phonon scattering (blue solid line) and combined with remote phonon scattering (red dashed and black dashed dotted). The charge carrier concentration is smaller for the dashed dotted line. b) Qualitative conductivity dependence on charged impurity concentration at low temperatures and $V_g \approx V_{Dir}$; c) Qualitative conductivity dependence on charge carrier concentration for long-range Coulomb scattering (blue solid line), for short-range scattering (red dashed line) and for combined (black dashed dotted line) scattering at low temperatures and $|V_g| > V_{Dir}$.

where $\rho_0(V_g)$ is the residual resistivity, ρ_A is the resistivity due to acoustic phonons, and ρ_{rps} is the remote phonon scattering. The qualitative dependence of acoustic-limited and remote phonon-limited resistivity versus temperature is shown in Fig. 4.1(c). However, it has also been shown that it is not fully correct to add up the resistivities assuming Matthiessen's rule as done in Eq. 4.7 [90]. Additionally, in the theoretical description of long-range Coulomb scattering, there is a temperature-dependent screening factor, entailing a temperature dependency of the Coulomb scattering, which needs to be considered along with phonon scattering.

4.1.2 Residual charge carrier concentration

Close to the Dirac point, the minimum conductivity depends on the charged impurity concentration. The higher the charged impurity concentration, the higher the conductivity minimum because the charged impurities induce potential fluctuations across the graphene sheet, which lead to the formation of electron-hole puddles, as has been observed by a scanning single-electron transistor shown in Fig. 4.2. The relation between the concentration of charged impurities n_{imp} and residual charge carrier concentration n_0 is found using a self-consistent approximation of the screening between impurities and carriers [24]. At low temperatures ($T \approx 20\,\mathrm{K}$), the measured dependence between conductivity on residual charge carrier concentration, conductivity minima width and the shift of the Dirac point have been well described by the self-consistent approximation [16]. With a higher charged impurity concentration, the conductivity minima width and the shift of the Dirac point increase. Although the conductivity minima increases, the conductivity

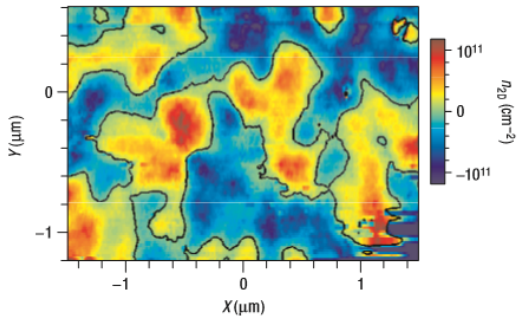

Figure 4.2: Colour map of the spatial concentration variations in a graphene flake extracted from surface potential measurements. The blue regions correspond to holes, and the red regions correspond to electrons. The black contour lines mark the zero concentration contour; adapted from [91].

for $|V_g| > V_{Dir}$ decreases with higher charged impurity concentrations as $\sigma \propto n/n_{imp}$ because the mobility is reduced by charged impurity scattering (Fig. 4.1(b)).

Because long-range scattering is generally the dominant scattering mechanism in fabricated GFETs, the conductivity measurements at low temperatures, exhibit a linear dependence with carrier concentration, as qualitatively illustrated in Fig. 4.1(c).

In cases where the concentration of charged impurities is low, the conductivity exhibits a sub-linear behaviour with a crossover from long-range to short-range dominant scattering when moving from lower to higher charge carrier concentrations [92].

4.1.3 Other scattering mechanisms

In general, graphene is not atomically flat but exhibits ripples because it adjusts to the substrate morphology or releases strain. Depending on its physical origin, scattering at ripples can mimic short-range scattering [93, 94].

Furthermore, it was shown that vacancies in the graphene sheet, which are identified by large D peaks in the Raman spectrum, are the origin for strong resonant scattering, which has the same dependencies as the long-range Coulomb scattering [95, 96].

In suspended graphene, out-of-plane (flexural) phonon modes are the main limiting factor of the mobility [97].

4.1.4 Ballistic transport

The scattering time relates to the mean free path l, which is the distance that a charge carrier can travel before it is scattered. When the mean free path is much smaller than the channel length $l \ll L$ it is appropriate to consider diffusive transport. The condition $l \gg L$ is called ballistic transport. Ballistic-like transport can be obtained in devices with high-quality graphene and short gate length. For a device with the dimensions $L \times W =$ $0.5\,\mu\text{m} \times 1.4\,\mu\text{m}$, the maximum ballistic mobility is $\approx 280000\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ at the charge carrier concentration $n \approx 4 \times 10^9\,\text{cm}^{-2}$ [98]. Furthermore, ballistic transport has been

observed at room temperature over a distance of 1 μm in Hall bar structures with graphene encapsulated in hexagonal boron nitride with $n \approx 10^{11}\,\mathrm{cm}^{-2}$ and $\mu > 100000\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ [99].

However, for the mobilities and gate lengths of the transistors considered in this work it is sufficient to assume diffusive transport. The fabrication process of GFETs unintentionally introduces impurities at the interfaces between the graphene layer and the adjacent substrate and the gate dielectric. Inevitably, these impurities act as scattering centres and shorten the scattering length.

4.1.5 Estimating mobility in graphene

Different mobility definitions and corresponding methods are available for estimating the mobility in graphene. The most commonly used methods are

- the **Hall effect mobility**, which requires the fabrication of so-called Hall bars or van der Pauw structures. These structures are used to measure the resistivity and the Hall coefficient of a sample. Thus, the mobility value can be separated from the $n \cdot \mu$ product in the resistivity expression.

- the **effective mobility** $\mu = \sigma/ne$. The mobility is found from a conductivity measurement vs drain voltage, followed by dividing the measured conductivity by the charge carrier concentration estimated from the approximation

$$n_\mathrm{g} \approx \frac{|V_\mathrm{g} - V_\mathrm{Dir}|C_\mathrm{ox}}{e}, \tag{4.8}$$

  when $V_\mathrm{g} > V_\mathrm{Dir}$ and $C_\mathrm{q} \gg C_\mathrm{ox}$. When $C_\mathrm{q} \gg C_\mathrm{ox}$ the gate capacitance per unit area can be approximated as $C_\mathrm{g} \approx C_\mathrm{ox}$.

- the **field-effect mobility**. The field-effect mobility is defined as the slope of the conductivity curve $\mu = \frac{1}{C_\mathrm{g}} \frac{d\sigma}{dV_\mathrm{g}}$.

- fitting of a resistance model to measured transfer characteristics of a transistor [100].

It is important to note which method is used to extract the mobility because the found mobilities are not necessarily comparable. Mobility degrades during fabrication and the mobility measured on complete GFETs is lower than that by the Hall effect since graphene is exposed to different external factors during the fabrication of specific test structures.

4.1.6 High-field transport

As discussed above, the saturation velocity (v_sat) is a more adequate parameter to describe transport at high fields. The saturation velocity can be found by fitting the field-dependent velocity model, Eq. 3.2, to the measured velocity versus electric field curves and using the low-field mobility μ, the saturation velocity v_sat and γ as fitting parameters.

Measurements show that the velocity in GFETs decreases with increasing temperature and increasing charge carrier concentration [101]. A number of different theoretical approaches exist to explain the high-field behaviour. The theoretically achievable saturation velocity is between 0.2 and $0.8v_{\mathrm{F}}$ depending on the calculation method, the considered scattering mechanisms, and substrate [25, 88, 102, 103]. Typically, at low fields, the charged impurity scattering is the dominant scattering mechanism, but impurity scattering does not significantly affect high-field transport according to Refs. [88, 103, 104], whereas in Ref. [87] a strong effect of charged impurity scattering is predicted.

The dependence of the saturation velocity on charge carrier concentration and temperature is quite well described by simplified models for the remote-phonon-scattering-limited saturation velocity model [25, 88, 101]

$$v_{\mathrm{sat}}(n,T) = \frac{2}{\pi}\frac{\omega_{\mathrm{OP}}}{\sqrt{\pi n}}\sqrt{1-\frac{\omega_{\mathrm{OP}}^2}{4\pi n v_{\mathrm{F}}^2}\frac{1}{N_{\mathrm{OP}}+1}} \quad \text{or} \quad v_{\mathrm{sat}} \approx \frac{2}{\pi}\frac{\omega_{\mathrm{OP}}}{\sqrt{\pi n}}, \tag{4.9}$$

where $\hbar\omega_{\mathrm{OP}}$ is the optical phonon (OP) energy, and $N_{\mathrm{OP}} = 1/[exp(\hbar\omega_{\mathrm{OP}}/kT) - 1]$ is the phonon occupation.

However, it is argued that a combination of remote phonon scattering and self-heating needs to be taken into account, where the self-heating effect depends on the choice of substrate and its thermal conductivity [88, 103].

Other simulations assume increasing impurity scattering with increasing carrier concentration, since the applied gate voltage will fill interface traps, charge them and thus introduce more scattering centres or that local potential scattering (atomic scale defect scattering and dislocation scattering) explains the dependence of saturation velocity on charge carrier concentration at high fields [105, 106].

Chapter 5

Effects of impurities on transport characteristics

The performance of GFETs is affected by impurities at the interfaces between the graphene layer and the adjacent material layers. The topic of this chapter is the study of the effect of impurities on transport characteristics, which is the main work of this thesis. The study of the effect of impurities is performed using a semi-empirical model, which allows us to see how interface states contribute to the total capacitance with an interface capacitance and thereby affect the voltage dependencies of the gate capacitance and gate resistance curves. Additionally, a method was developed using high-frequency and dc measurements followed by delay-time analysis to study the saturation velocity in GFETs.

5.1 Hysteresis in C-V and transfer characteristics

Figure 5.1 shows a typical measured gate-source capacitance versus gate voltage (C-V) and a drain resistance versus gate voltage (R-V) characteristics of a GFET. The measured resistance is the sum of the contact resistance, the access resistance and the channel resistance. To be able to observe the capacitance minimum in the C-V characteristic, it

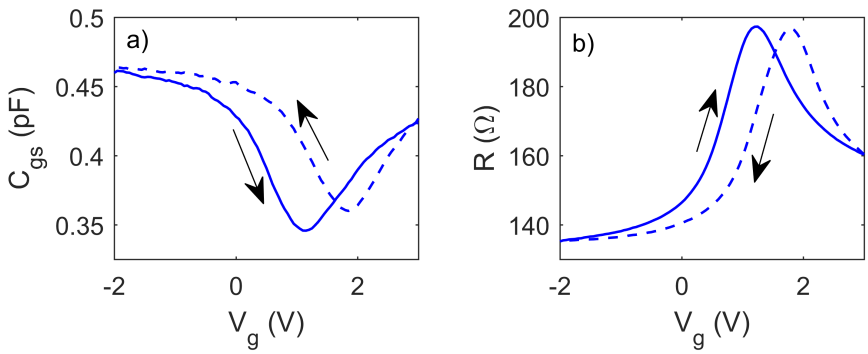

Figure 5.1: a) Gate-source capacitance versus gate voltage and b) resistance versus gate voltage for a GFET fabricated on PET with a gate length of $L = 1\,\mu$m, gate width of $W = 2 \times 30\,\mu$m (two-finger gate) and 15 nm Al_2O_3 gate oxide. Solid lines are forward sweeps of the gate voltage $V_g = -2$ to 3 V, and dashed lines are backward sweeps $V_g = 3$ to -2 V.

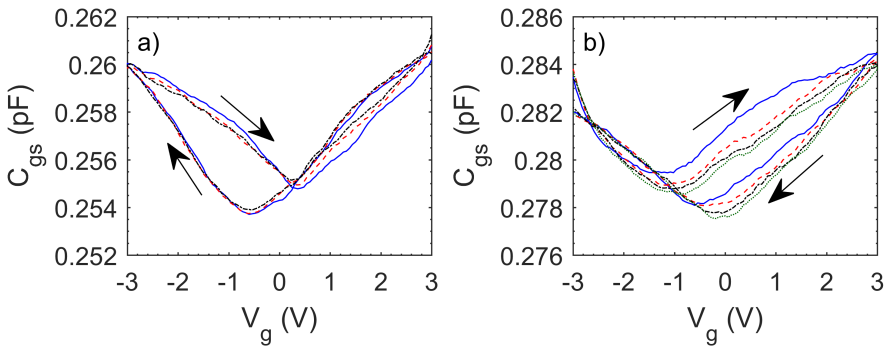

Figure 5.2: C-V characteristics of a GFET on $LiNbO_3$ with a) gate voltage sweeps repeated immediately and b) holding the gate voltage at $V_g = 1\,V$ for 10 minutes after every sweep. Solid line - first sweep; dashed line - second sweep after 10 minutes; dashed dotted line - third sweep after 20 min; and dotted line - fourth sweep after 30 min.

is necessary to use a non-conducting substrate, such as PET, $LiNbO_3$ or sapphire. On silicon, the gate capacitance is overshadowed by the large parasitic capacitance of the contact pads (Fig. 3.2). For this reason, the measurement results presented in Fig 5.1 are from a GFET on a PET substrate.

There are two observations that can be frequently made in the presented C-V and R-V characteristics. The first is that the forward and backward sweeps ($V_g = -2$ to $3\,V$ and $V_g = 3$ to $-2\,V$, respectively) in the C-V and R-V characteristics do not coincide; rather, they exhibit hysteresis. The second is that there is an asymmetry between the hole branch and the electron branch of the R-V characteristic as shown in Fig. 5.1(b). For $V_g < V_{Dir}$, the majority charge carriers are holes, and for $V_g > V_{Dir}$, the majority charge carriers are electrons. The asymmetry in R-V characteristics is explained by two mechanisms.

The first is due to the change in R_d and R_s due to formation of p-n junctions between the n-type gated channel and the p-type ungated regions at $V_g > V_{Dir}$ [107, 108].

Second, assuming charged impurity scattering to be the dominant scattering mechanism, the scattering cross sections for holes and electrons are different, and thus the ratio between the mobility values of holes and of electrons can be as high as ≈ 2. [109].

The hysteresis appears in two different ways, depending on the sweep rate and temperature of the system. An increase in the minimum capacitance gate voltage during the back sweep can be explained by charge carriers being trapped in the gate oxide and/or in adsorbents on graphene [26]. In this thesis, both traps and adsorbents are denoted as impurities. A negative shift in the minimum capacitance gate voltage is due to capacitive gating. Fully covering graphene by a high-quality protective oxide layer helps to work against hysteresis. Thereby, the device performance can be stabilised for weeks [110]. This fabrication step is not conducted for devices in this work, since a relatively thin gate oxide is needed to allow for top-gating the device.

If no conservation measures are undertaken, with ageing or stressing the gate oxide

with a gate voltage will lead to the C-V and R-V characteristics changing in shape, and shifting the position of the Dirac point. As shown in Fig. 5.2(a), the capacitance curves are reproducible when the gate voltage sweeps are repeated immediately after each other. In contrast, when the gate voltage is swept after keeping the gate voltage at a constant $V_g = 1\,\mathrm{V}$ for 10 minutes, the measured minimum capacitance is decreasing and the minimum capacitance voltage is increasing, as shown in Fig. 5.2(b).

Clearly, the instability of the GFETs is a challenge. To be useful in commercial applications, the devices need to reproducibly provide the same output at the same bias conditions used.

5.2 Oxide traps and impurities

The schematic of traps, i.e., energy states between the conduction and valence bands of the oxide that are available for charge carriers in graphene, is illustrated in Fig. 5.3. There are different types of traps depending on their energy levels and physical location in the oxide [111]. A-type and b-type traps are so-called interface traps/interface states, which originate from impurities or dangling bonds at the interface. The difference between a-type and b-type interface states is in the energy level. A-type interface states are likely to trap and de-trap charge carriers, whereas b-type interface states are too high or too low in energy to contribute to the fast trapping dynamics. However, both types of traps contribute to charged impurity scattering. C-type traps are commonly oxygen vacancies that lay in the bulk oxide. Fast interface traps, which can follow the accurrent when conducting the C-V measurement at typical frequencies of approximately 1 MHz, contribute with an interface capacitance, whereas slower traps are responsible for the shift of the capacitance minimum and resistance maximum between the forward and backward sweeps.

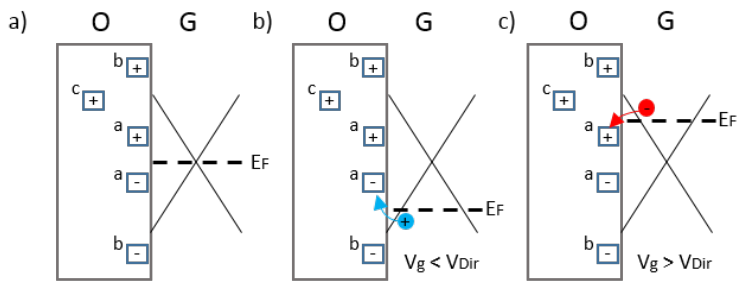

Figure 5.3: a) Schematic of different types of traps within the band diagram of an oxide (O) and graphene (G) system. A-type traps lay close to the oxide/graphene interface at relatively low energy levels. B-type traps are positioned close to the interface but have much higher or much lower energy levels than a-type traps. C-type traps lay deep in the bulk oxide [111]. b) Emptying and c) filling of traps when $V_g < V_{\mathrm{Dir}}$ and $V_g > V_{\mathrm{Dir}}$, respectively.

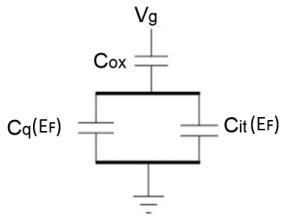

Figure 5.4: Equivalent circuit of the total gate capacitance. C_{ox} is the oxide capacitance, C_{q} is the quantum capacitance, and C_{int} is the interface capacitance.

5.3 Effect of impurities on C-V and transfer characteristics

5.3.1 C-V model

The following model is described in more detail in Paper A. The existence of interface states accompanied by the trapping and de-trapping dynamics of charge carriers at the graphene/oxide interface requires including an interface capacitance C_{int} in parallel to the quantum capacitance C_{q} in the equivalent circuit model of the total capacitance, as shown in Fig. 5.4. The total capacitance can be calculated from

$$C_{\mathrm{t}} = \frac{C_{\mathrm{ox}}(C_{\mathrm{int}} + C_{\mathrm{q}})}{C_{\mathrm{ox}} + C_{\mathrm{int}} + C_{\mathrm{q}}}, \tag{5.1}$$

where

$$C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}\epsilon_0}{t_{\mathrm{ox}}}, \tag{5.2}$$

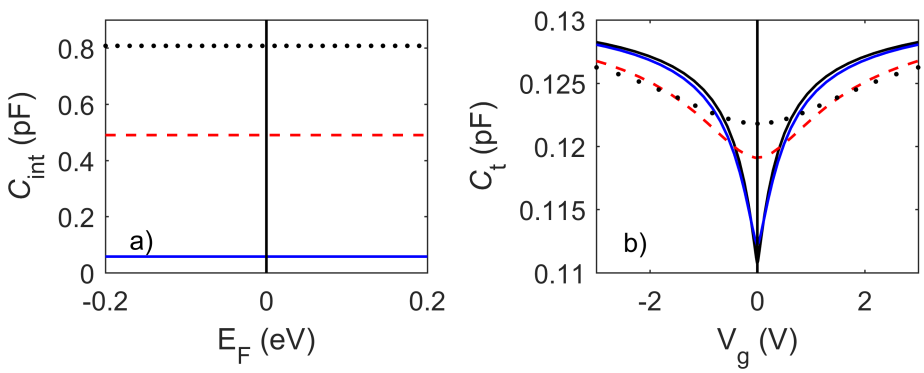

Figure 5.5: a) Interface capacitance and b) total capacitance for different interface state densities $N_{\mathrm{int}} = (0, 0.02, 0.17, 0.28) \times 10^{18}\,\mathrm{m}^{-2}\mathrm{eV}^{-1}$ (solid black line, solid blue line, red dashed line, black dotted line).

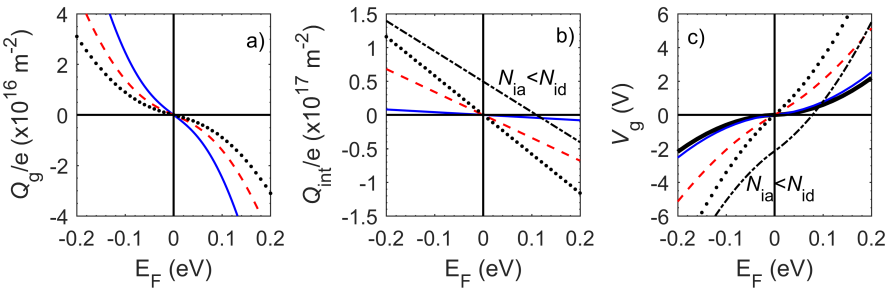

Figure 5.6: a) Charge concentration in graphene ($Q_g = e(n_h - n_e)$) versus Fermi level (E_F) for different Fermi velocities $v_F = (0.6, 0.8, 1) \times 10^6$ m/s (solid line, dashed line, dotted line). b) Interface charge concentration versus Fermi level and c) gate voltage versus Fermi level for different interface state densities $N_{int} = (0, 0.02, 0.17, 0.28) \times 10^{18}$ m^{-2}eV^{-1} (solid black line, solid blue, dashed line, dotted line) and for $N_{ia} < N_{id}$ (dashed dotted line).

$$C_q = \frac{8\pi kT}{(hv_F)^2} ln\Big[2 + 2\cosh\Big(\frac{E_F}{kT}\Big)\Big], \tag{5.3}$$

and

$$C_{int} = \int_{-\infty}^{\infty} \chi_{int} dE, \tag{5.4}$$

where χ_{int} is the capacitance density per energy and area unit. χ_{int} can be derived in [71] from

$$\chi_{int} = \frac{e^2}{kT} \frac{N_{id} + N_{ia}}{2} \frac{2e_n^2}{4e_n^2 + \omega^2} f(1 - f), \tag{5.5}$$

where ω is the measurement frequency, e_n is the tunnelling emission and capture rates of charge carriers, and N_{id} and N_{ia} denote the donor-like and acceptor-like interface state densities, respectively. For the devices discussed in Paper A, it was sufficient to approximate the interface state densities to be constant with energy $N_{int} = N_{id} = N_{ia}$.

A higher interface state density results in a larger interface capacitance, as shown in Fig. 5.5(a), and a broadening of the total capacitance curve versus gate voltage (Fig. 5.5(b)). This result is explained by the relation between the gate voltage and the Fermi level given by

$$V_g(E_F) = \Phi_{ms} - \frac{Q_{ox} + Q_g(E_F) + Q_{int}(E_F)}{C_{ox}} + \frac{E_F}{e}, \tag{5.6}$$

where Φ_{ms} is the work function difference between the gate metal and graphene and is assumed to be negligibly small, Q_{ox} is the oxide charge attributed to c-type bulk traps and is approximately constant, Q_g is the charge in graphene given by Eq. 2.8 in Chapter 2, and Q_{int} is the interface charge:

$$Q_{int} = \int_{E_F}^{\infty} e \cdot N_{id} - \int_{\infty}^{E_F} e \cdot N_{ia}. \tag{5.7}$$

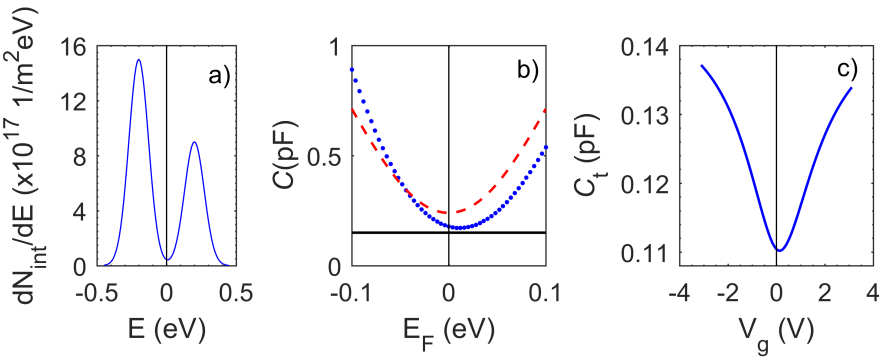

Figure 5.7: a) Gaussian interface state density distribution. b) Quantum capacitance (dashed line), interface capacitance for the interface state density distribution in (a) (dotted line), and oxide capacitance (solid line). c) The total capacitance of the capacitance in (b) calculated using Eq. 5.1.

Q_g depends on the value of the Fermi velocity (Fig. 5.6(a)), and Q_{int} depends on the interface state densities, as in Fig. 5.6(b). The dependence of V_g versus E_F and different interface state densities is shown in Fig. 5.6(c). For a greater interface state densities, the gating effect is reduced. This means that to achieve the same shift of the Fermi level, a higher gate voltage needs to be applied when the interface state density is greater. This entails broadening the capacitance in Fig. 5.5(b), and also the resistance curve. Broadening of the resistance curve with increasing residual charge carrier concentration was confirmed by the 2D to G peak intensity ratio in the Raman spectrum [67, 112].

Figure 5.7 illustrates how the interface state density distribution affects the shape of the total capacitance, assuming that the interface state density distribution for the donor-like and acceptor-like interface states is Gaussian, as shown in Fig. 5.7(a), rather than having a constant distribution. The quantum capacitance, the interface capacitance for the interface state density distribution in Fig. 5.7(a) and the oxide capacitance are shown in Fig. 5.7(b). The interface capacitance is not constant, and its minimum is shifted away from $E_F = 0$. This affects the shape of the total capacitance versus gate voltage shown in Fig. 5.7(c). The curve is not symmetric around the minimum and is shifted away from $V_g = 0$.

5.3.2 R-V model

The resistance is modelled as

$$R(V_g) = R_C + \frac{L}{W}\frac{1}{e(\mu_h(n_h + n_0/2) + \mu_e(n_e + n_0/2))}, \tag{5.8}$$

where $R_C = R_d + R_s$. In Paper A and Paper B, R_C is denoted as contact resistance. L is the gate length; W is the gate width; μ_e and μ_h are the hole and electron mobilities; n_e and n_h are the hole and electron carrier concentrations calculated from Eqs. 2.5 and 2.6,

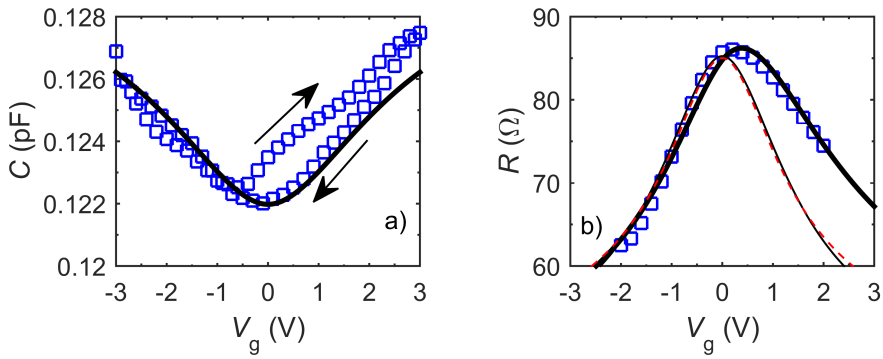

Figure 5.8: Fit (solid bold line) of model to measured (squares) a) capacitance-gate voltage and b) resistance-gate voltage characteristics. In (b), the fitting results of Eq. 5.8 using equal hole and electron mobilities (solid slim line) are compared to the commonly used model [100] that does not consider interface states (dashed lines); adapted from Paper A.

respectively; and n_0 is the residual charge carrier concentration as discussed in the low-field transport section in Chapter 4.

The basic steps to fit the capacitance model and resistance model are as follows:

i) The capacitance model (Eq. 5.1) is fitted to the C-V measurement using the interface state density as a fitting parameter, where the relation between the gate voltage and rhe Fermi level is defined by Eq. 5.6.

ii) The resistance model (Eq. 5.8) is fitted to the measured R-V curve, and the resistance R_C, the mobility and the residual charge carrier concentration are used as fitting parameters.

As shown in Fig. 5.8, the model fits the measurements well using the fitting parameters in Table 5.1. Note that there are a number of assumptions that need to be made, which significantly influence the extracted mobility and residual charge carrier concentration values.

First, the Fermi velocity is not exactly known, but it strongly affects the calculation of quantum capacitance, the density of states and thereby the charge carrier concentration and eventually the mobility values, as well as the interface state density and residual charge carrier concentration, as clearly shown in Table. 5.1. Second, it is assumed that charged impurity scattering, i.e., Coulomb scattering, is the dominant scattering mechanism, and

v_F (m/s)	$N_{int} \times 10^{18}$ (m^{-2})	$n_0 \times 10^{16}$ (m^{-2})	μ_h (cm^2/Vs)	μ_e (cm^2/Vs)
0.6	0.29	0.6	2050	950
0.8	0.28	0.4	3100	1600
1.1	0.25	0.28	4900	2600

Table 5.1: Fitting parameters of Eqs. 5.1 and 5.8 to the measured capacitance and resistance characteristic in Figs. 5.8(a) and (b), respectively, adapted from Paper A.

	with interface states	without interface states
$n_0 \times 10^{16}$ (m^{-2})	0.2	2.4
μ ($\mathrm{cm}^2/\mathrm{Vs}$)	2400	650

Table 5.2: Comparison of fitting parameters of the model using Eqs. 5.1 and 5.8 with and without interface states; adapted from Paper A.

thus, the mobility is independent of the charge carrier concentration. Third, the contact resistance is assumed to be constant and independent of the applied gate voltage. Fourth, the interface state density could have any other distribution that results in fitting the measured capacitance. Since the interface state density is high and this leads to only a small shift of the Fermi level, the approximation of a constant interface state distribution within this small energy interval is appropriate. Fifth, the tunnelling emission and capture rates of charge carriers was set high such that all interface states contribute to the interface capacitance.

These assumptions are numerous, and additional characterisation methods should be considered to decrease the uncertainties. There are several such interface state density characterisation methods mentioned in Ref. [111]. The advantage of the method presented here is that all information is obtained from GFET measurements, and no additional structures, such as Hall bars, are needed.

If the found values of the mobility and rhe residual charge carrier concentration using the method presented here are compared to a commonly used method [100], the results differ quite considerably. The mobility values can differ up to a factor of two and the residual charge carrier concentration can differ by a factor of 10 (Table 5.2).

The discrepancy can be explained by the fact that in the commonly used model [100], interface states and capacitance measurements are not taken into account. Commonly, the charge carrier concentration is calculated from Eq. 4.8 ($n_\mathrm{g} = C_\mathrm{ox}|V_\mathrm{g} - V_\mathrm{Dir}|/e$), without considering charge carriers that are captured in oxide traps (n_int)

$$n_\mathrm{g} + n_\mathrm{int} = \frac{C_\mathrm{ox}(V_\mathrm{g} - V_\mathrm{Dir})}{e}. \tag{5.9}$$

In this way, the charge carrier concentration is overestimated, thereby leading to an underestimation of the mobility, since it is the product of mobility and charge carrier concentration that determines the resistivity (Eq. 4.1; $1/\rho = \sigma = en\mu$). Additionally, by using Eq. 4.8 the predicted charge carrier concentration at $(V_\mathrm{g} - V_\mathrm{Dir}) = 0\,\mathrm{eV}$ is $n_\mathrm{g} = 0\,\mathrm{m}^{-2}$, while Eq. 2.7 predicts $n_\mathrm{g} = n_\mathrm{th}$, the thermally generated charge carriers. Therefore, the n_0 used for fitting is different in both approaches.

5.4 Effect of impurities on carrier velocity in GFETs

One set of representative output and transfer characteristics of the GFETs studied in Paper B is shown in Fig. 5.9. The slope, and the minimum current shift and width in the transfer characteristic depend on the charged impurity concentration and is shown for two devices in Fig. 5.9(a). Furthermore, it is shown that the output current clearly does not saturate.

The velocity of charge carriers in the channel of GFETs can be studied by delay-time analysis followed by applying analytical models of the field-dependent and phonon-limited carrier velocity, Eq. 3.2 and Eq. 4.9. The velocity models are discussed in Chapter 3 and 4. Delay-time analysis is used to separate the parasitic, extrinsic and intrinsic delay times. Here, the aim is to extract the intrinsic delay-time τ_{int} since it is directly related to the carrier velocity as

$$v = \frac{L}{\tau_{\text{int}}}, \tag{5.10}$$

when the GFETs are biased in the unipolar regime (Fig. 5.9(b)), i.e., [113]

$$V_{\text{d,int}} < V_{\text{d,sat}} = |V_{\text{g}} - V_{\text{Dir}}| + en/C_{\text{g}}, \tag{5.11}$$

where $V_{\text{d,int}} = \varepsilon_{\text{int}} \times L$ and n is the charge carrier concentration.

5.4.1 Delay-time analysis

The delay-time analysis was developed based on the methodologies in [74, 77, 114]. The total delay is the sum of the intrinsic delay, the time that the charge carriers need to travel across the channel according to Eq. 5.10, the extrinsic delay, due to contact resistances and the parasitic delay associated with the gate pad capacitance:

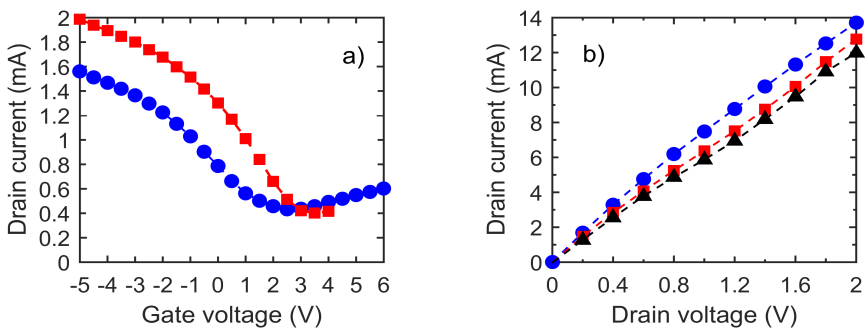

Figure 5.9: a) Output and b) transfer characteristics of GFETs. a) Drain current I_{ds} versus drain voltage V_{ds} for V_{g}= (-4,-2,+1) V (circles,squares,triangles). b) I_{ds} versus gate voltage V_{g} for two different devices at $V_{\text{ds}} = -0.1$ V.

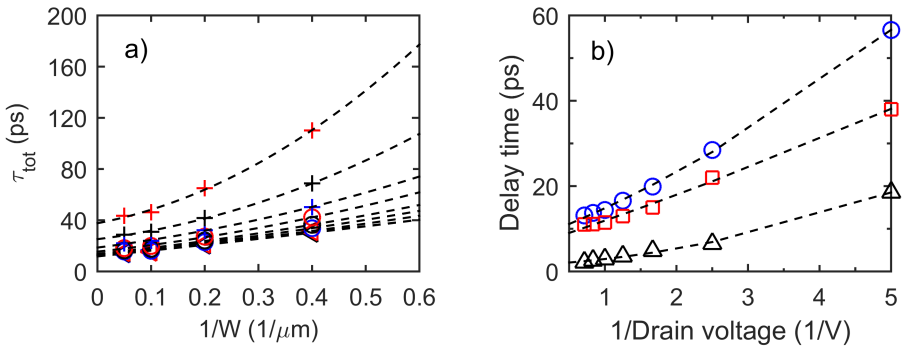

Figure 5.10: a) Delay-time versus the reciprocal of the gate width for drain bias from top to bottom $V_{ds} = 0.2$ to 2 V in steps of $\Delta V_{ds} = 0.2$ V. b) Measured delay-time τ_{tot} (open circles), delay-time minus gate pad delay $\tau_{tot} - \tau_{pad}$ (open squares) and gate pad delay τ_{pad} (open triangles) versus reciprocal of the drain-source voltage.

$$\begin{aligned}\tau_{tot} &= \frac{1}{2\pi f_{T,ext}} = \tau_{int} + \tau_{ext} + \tau_{pad} \\ &= \tau_{int}\left(1 + \frac{R_C}{R - R_C}\right) + \frac{C \cdot W \cdot L}{2} R_C + \frac{C_{pg}}{g_{m,ext} W}. \end{aligned} \tag{5.12}$$

$g_{m,ext}$ is the terminal transconductance. The resistance. R_C is extracted by a commonly used method of fitting the resistance model to measured data [67, 100]. Due to the bias condition according to Eq. 5.11 the charge carrier concentration in the channel can be approximated to be equally distributed, and therefore, $C_{gs} = C_{gd} = C_{ox} \cdot W \cdot L/2 = C_g \cdot W \cdot L/2$. The influence of the interface capacitance associated with interface states and quantum capacitance are not taken into account. The delay time attributed to the gate pad capacitance τ_{pad} is

$$\tau_{pad} = \frac{C_{pg}}{g_{m,ext} W}. \tag{5.13}$$

In the paper B, τ_{pad} is estimated by using its dependence on the gate width and by using data from measurements on transistors with similar n_0, the same gate length $L = 1\,\mu$m, but with different gate widths $W = 2.5, 5, 10$ and $20\,\mu$m. The extrinsic delay-time versus the reciprocal of the gate width is extrapolated to infinite gate width $1/W = 0$ as shown in Fig. 5.10(a). The delay-time at this point can be treated as having no contributions from τ_{pad}. This is performed for all drain biases. τ_{pad} versus drain bias is found by subtracting τ at $1/W = 0$ from the measured delay-time τ_{tot}, as shown in Fig. 5.10(b). As soon τ_{pad} is found, all parameters that are needed to calculate the intrinsic delay-time (τ_{int}) according to Eq. 5.12 are known.

τ_{int} is used to calculate the intrinsic transit frequency:

$$f_{T,int} = \frac{1}{2\pi\tau_{int}}. \tag{5.14}$$

In Fig. 5.11(a) the measured and intrinsic transit frequencies are compared. The measured transit frequency is lower due to the contribution of the extrinsic and parasitic parts. Furthermore, the transit frequency is lower for higher residual charge carrier concentrations. From $f_{\mathrm{T,int}}$, the charge carrier velocity is found using Eq. 5.10, and the field-dependent velocity model, Eq. 3.2, is fitted to the measurement to find v_{sat}. Figure 5.11(b) shows the measured charge carrier velocity versus intrinsic electric field in the channel, $\varepsilon_{\mathrm{int}}$, where

$$\varepsilon_{\mathrm{int}} = -\frac{V_{\mathrm{ds}}}{L}\Big(1 - \frac{R_{\mathrm{C}}}{R}\Big), \tag{5.15}$$

together with the fit of the model. To study the limiting scattering mechanisms, we employ a simplified model of the saturation velocity limited by phonon scattering (Eq. 4.9) for the involved materials using surface OP energies of the SiO_2 substrate $\hbar\omega_{\mathrm{OP}} = 55\,\mathrm{meV}$ [115] and the Al_2O_3 gate dielectric $\hbar\omega_{\mathrm{OP}} = 87\,\mathrm{meV}$. The carrier concentration is determined from the measured output characteristic

$$n = \frac{L}{We\mu_{\mathrm{T}}}\frac{1}{R - R_{\mathrm{C}}}, \tag{5.16}$$

with $\mu_{\mathrm{T}} = \frac{L}{\tau_{\mathrm{int}}\varepsilon_{\mathrm{int}}}$. Matthiessen's rule is applied to find an effective saturation velocity:

$$\frac{1}{v_{\mathrm{sat}}^{\mathrm{eff}}} = \frac{1}{v_{\mathrm{sat}}^{\mathrm{G}}} + \frac{1}{v_{\mathrm{sat}}^{\mathrm{SiO2}}} + \frac{1}{v_{\mathrm{sat}}^{\mathrm{Al2O3}}} + \frac{1}{v_{\mathrm{sat}}^{\mathrm{n0}}}. \tag{5.17}$$

The best estimate of $v_{\mathrm{sat}}^{\mathrm{eff}}$ compared to the measured velocity yields the combination of SiO_2 phonons and graphene phonons (dashed line in Fig. 5.11). Adding $v_{\mathrm{sat}}^{\mathrm{Al2O3}}$ underestimates the saturation velocity. Self-heating is neglected since the current does not decrease at high fields. In Fig. 5.11(c), the saturation velocity found by using the field-dependent velocity model, Eq. 3.2, is plotted against the residual charge carrier concentration. There appears to be a trend towards lower saturation velocities for higher residual charge carrier concentrations. However, for the ratio of the saturation velocity from Eq. 3.2 and Eq. 5.17 with $v_{\mathrm{sat}}^{\mathrm{G}}$ and $v_{\mathrm{sat}}^{\mathrm{SiO2}}$, the dependence on n_0 disappears. The decrease in velocity can be explained by a higher charge carrier concentration in the channel induced by the emission of charge carriers from traps at high fields. An indication for the emission of charge carriers at high fields is shown in Fig. 5.11(d). Figure. 5.11(d) shows that there is a correlation between n_0 and the charge carrier concentration at the same intrinsic electric field and at $|V_{\mathrm{g}} - V_{\mathrm{Dir}}| = 4.7\,\mathrm{V}$ for all devices.

The results indicate how the power gain of GFETs can be improved. The quality of the gate oxide/graphene interface needs to be enhanced to reduce the impurity concentration and the emission of charge carriers, which prevent the current from saturating via velocity saturation. Additionally, replacing the substrate and gate material with materials that have higher phonon energies, e.g., hexagonal boron nitride, increases the intrinsic transit frequency.

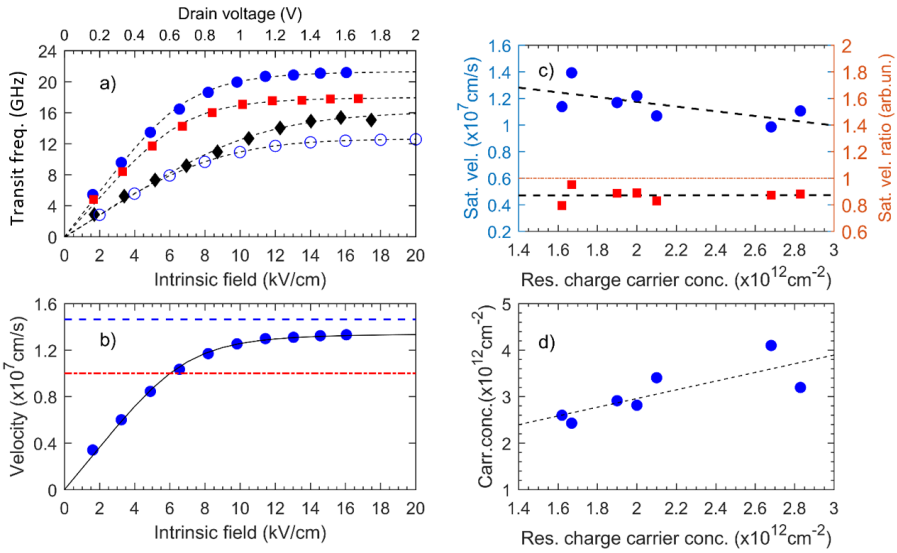

Figure 5.11: a) Intrinsic transit frequency vs electric field in the channel for devices with $n_0 = (1.7, 1.9, 2.8) \times 10^{12}\,\mathrm{cm}^{-2}$ (circles,squares,diamonds) at $V_\mathrm{g} = -2\,\mathrm{V}$. The extrinsic transit frequency vs drain voltage for the device with $n_0 = 1.7 \times 10^{12}\,\mathrm{cm}^{-2}$ is indicated in the same graph by open circles. Dashed lines are polynomial fitting curves and serve as a guide for the eye. (b) Carrier velocity for the device with $n_0 = 1.7 \times 10^{12}\,\mathrm{cm}^{-2}$ calculated using Eq. 5.10 and fitted by the empirical expression of Eq. 3.2 (solid line) using $\gamma = 3$, $\mu_0 = 1920\,\mathrm{cm}^2/\mathrm{Vs}$ and $v_\mathrm{sat} = 1.4 \times 10^7\,\mathrm{cm/s}$ vs electric field in the channel. The effective saturation velocities calculated using Eq. 5.17 for graphene with SiO_2 OPs (dashed) and graphene with SiO_2 and Al_2O_3 OPs (dashed-dotted) are also shown. c) Saturation velocity calculated using Eq. 3.2 (circles) and its ratio to effective saturation velocity calculated using Eq. 5.17 counting graphene with SiO_2 OPs (squares) vs residual charge carrier concentration ($n_\mathbf{0}$). d) The charge carrier concentration vs. n_0 at $E_\mathrm{int} = 1.5\,\mathrm{V}/\mu\mathrm{m}$ and $|V_\mathrm{g} - V_\mathrm{Dir}| = 4.7\,\mathrm{V}$.

Chapter 6

Conclusions and future outlook

In this work, the effects of impurities on charge carrier transport in graphene field-effect transistors were studied by *i)* developing a semi-empirical capacitance and resistance model, which addresses interface charge and corresponding interface capacitance, and *ii)* by introducing a method to study the limiting mechanisms of the charge carrier velocity.

The model showed that a constant interface capacitance increases the minimum capacitance value and broadens both the capacitance curve and the resistance curve due to a reduced gating effect. Interface capacitance values are found by fitting the capacitance model to measured capacitance characteristics. The charge carrier concentration can be calculated by using the relationship between the applied gate voltage and the Fermi level position. The charge carrier concentration is then used in the resistance model, which is fitted to the resistance-gate voltage measurement using the mobility, the residual charge concentration and the resistance as fitting parameters. The comparison between the presented model and a similar commonly used resistance model, which does not include interface states, shows that ignoring interface states leads to an underestimation of the mobility. Additionally, the model was used to analyse how different values of the Fermi velocity influence the extracted values of the mobility and the interface state density. It was shown, that the results are strongly affected by small uncertainties in the Fermi velocity, which is influenced by the dielectric constant of the substrate.

Several assumptions were made when developing the model. The interface state density distributions are assumed to be constant, the tunnelling capture and emission rates are assumed to be high, the charged impurity scattering is assumed to be the dominant scattering mechanism, and the contact resistance is assumed to be constant while sweeping the gate voltage. Although it is advantageous to be able to conduct a characterisation on a full transistor layout without the need for designated test structures, it is advisable to have independent measurements to reduce the number of assumptions.

Thus far, only the forward gate voltage sweep can be accurately described by the model. For the future, it is planned to include different time constants for the capture and emission rates of the charge carries to obtain a more complete picture of the charge transport.

Since the hysteresis effect in graphene devices is a common feature, it is necessary to understand and model this effect. An appropriate model of the hysteresis effect can be added to any other device model, for example, a detector model, to study the implications of hysteresis on these types of graphene devices.

The limiting factors of the charge carrier velocity in top-gated GFETs were studied, using the method developed in this work, by applying delay-time analysis to the measured transit frequencies of transistors with different residual charge carrier concentrations. The transit frequencies were calculated from RF S-parameter measurements. Additionally, dc transfer and output characteristics were measured. The transfer characteristic was used to

find the contact resistance and the residual charge carrier concentration, and the output characteristic was used to find the charge carrier concentration. The delay-time analysis separates the intrinsic delay time from the extrinsic delay and the gate-pad-induced delay. The intrinsic transit time is directly related to the transit time of the charge carriers under the gate and is inversely proportional to the charge carrier velocity. A field-dependent velocity model was applied to find the saturation velocity, which was then compared to the effective saturation velocities of different material combinations calculated by a remote phonon-limited saturation velocity model. The analysis shows that the saturation velocity is limited by remote phonons in graphene and SiO_2. Impurities contribute indirectly to the velocity limitation by emitting charge carriers at high fields and increase the total charge carrier concentration, which enters the remote phonon-limited saturation velocity model in denominator.

Future work will address improving the performance of GFETs, mainly in terms of the maximum frequency of oscillation. It is necessary to obtain hig-quality interfaces between graphene and the adjacent materials to keep the interface state density as small as possible and thereby minimise hysteresis and charge carrier emission at high fields. Achieving this condition could pave the way towards current saturation via velocity saturation and thus higher $f_{\max}$. Furthermore, a substrate with relatively high phonon energy needs to be chosen to increase the saturation velocity. Replacing Al_2O_3 and SiO_2 by hexagonal boron nitride in addition to a clean GFET fabrication process with self-aligned structures is a promising approach to achieve this goal.

Chapter 7

Summary of appended papers

Paper A

Effect of oxide traps on channel transport characteristics in graphene field-effect transistors

In this work, the effect of oxide traps on the charge transport in GFETs was studied by including an interface capacitance and interface charge in the capacitance-gate voltage and resistance-gate voltage models. It was shown that a higher interface state concentration increases the total capacitance and decreases the gating effect, thus broadening the measured characteristics. With the help of the model, it is possible to find the interface state density, the mobility, the contact resistance, and the residual charge carrier concentration. Furthermore, it is possible to study the effect of uncertainties on the extracted values. If oxide traps, i.e., interface states, are neglected, then the mobility values are underestimated. Additionally, the value of the Fermi velocity strongly influences the extracted mobility.
My contribution: Measurements, modelling, interpretation, writing the article.

Paper B

Charge carrier velocity in graphene field-effect transistors

In this work, a method was developed to analyse the limiting mechanisms of the charge carrier velocity in GFETs. The analysis of the saturation velocity is of particular interest since drain current saturation via velocity saturation is a possible approach to achieve higher $f_{\max}$. The S-parameters of transistors with different residual charge carrier concentrations were measured, and the respective transit frequencies for different bias conditions of V_{g} and V_{ds} were found. At the same time, the dc current was measured to calculate the charge carrier concentration. The transit frequencies were used for delay-time analysis to estimate the intrinsic transit frequency, which is directly related to the velocity of the charge carriers. Using a field-depended velocity model and a phonon-limited saturation velocity model, we found that phonons in SiO_2 and graphene are limiting the saturation velocity. The phonon-limited saturation velocity is inversely proportional to the charge carrier concentration. Additionally, it was shown that a higher impurity concentration leads to a higher charge carrier concentration in the channel due to the emission of charge carriers from traps at high fields., thereby contributing to a reduced saturation velocity.
My contribution: Measurements, modelling, interpretation, writing the article.

ACKNOWLEDGEMENTS

Hereby, I want to express my sincere gratitude to a number of people which supported me and are still supporting me on my path towards the PhD degree.
Thank you to Jan Stake, the head of the Terahertz and Millimetre wave Laboratory (TML), to employ me and giving me the chance to make this experience.
Furthermore, I would like to thank Andrei Vorobiev, my supervisor, for always being available for discussions and giving advice.
A big thank you to all my office mates and ex office mates, Andrey Gerneralov, Xinxin Yang, Mohammad Assad, and Michael Andersson, for the pleasantly shared time.
I also would like to thank the rest of the TML laboratory and all my colleagues on the sixth floor of MC2 for being a nice group to have around.
In addition, a thank you to Dr. Johan Liu, Yifeng Fu, Per Hyldgaard, Zhibin Zhang for the ongoing collaboration. I am thankful to Antonio Lombardo and the Graphene Centre for exchanging ideas, to Daniel Neumaier for supplying material and valuable knowledge, and to Olof Engström for a fruitful collaboration.
I am grateful to the cleanroom staff for your all the help and the support.
I would also like to thank Jasper Ruhkopf and Max Lemme for supporting my measurements at the University of Siegen, and Samina Bidemshkipour for the support during device fabrication.
Above all I am extremely thankful to my family, Vedad, and my friends for always being there for me in good and in bad times.

This work was supported in part by the Swedish Research Counsel (VR) under Grant Nos. 2012-4978 and 2014-5470, in part by the Swedish Foundation for Strategic Research (SSF) under Grant No. SE13-0061, and in part by the EU FET Graphene Flagship Project.

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