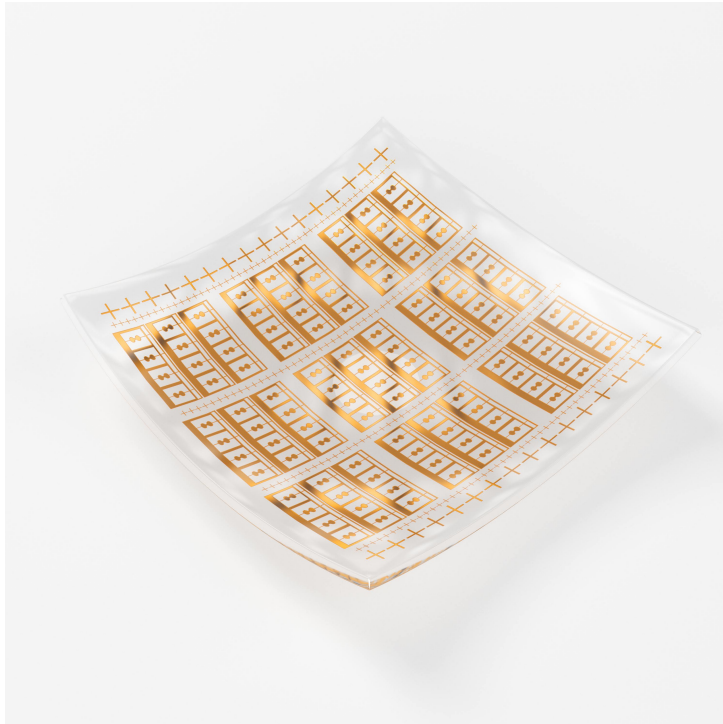




CHALMERS



Graphene FET terahertz detectors on flexible substrates

XINXIN YANG

Terahertz and Millimetre Wave Laboratory
Microtechnology and Nanoscience - MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2017

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因为我热爱 所以我存在
I love, therefore I am.

Abstract

Terahertz (THz) science and technology have developed rapidly over the past decades, extending the THz application areas from spectroscopy and earth and space sciences to communications, biomedicine and security sensing. Many of these emerging applications require shape-conforming, light-weight and low-cost detectors rather than existing solid-state detection technology. Graphene, which possesses impressive electrical and mechanical properties, is a promising material for enabling flexible devices at THz frequencies.

This thesis reports on the modelling, design, fabrication and characterisation of graphene THz detectors on plastic substrates. These detectors are based on field-effect transistors (FETs) fabricated using chemical vapour deposition (CVD)-grown graphene and integrated with split broadband bow-tie antennas.

A fabrication process has been developed to achieve high-performance THz detectors on plastic substrates. Since the properties of the dielectric film on graphene are very sensitive to the growth conditions, parallel-plate capacitor test structures on graphene on flexible substrates are fabricated for characterising the electrical properties of the dielectric films.

THz power detection in the frequency range from 330 GHz to 500 GHz at room temperature is demonstrated. The devices operate well above the cutoff frequency of the transistors. At room temperature, the voltage responsivity is above 2 V/W, and the noise-equivalent power (NEP) is below 3 nW/ $\sqrt{\text{Hz}}$ at 487 GHz.

The effects of bending strain on the dc characteristics, voltage responsivity and NEP of these detectors have been investigated. The mechanical studies reveal robust detector performance with tensile strain more than 1% with a corresponding bending radius of 7 mm.

This work provides an important route towards high-performance, low-cost THz flexible technology for future niche applications, such as wearable smart electronics, imaging systems, and communications.

Keywords: Graphene, 2D materials, field-effect transistors, THz detectors, sensors, flexible electronics, plastic substrates.

List of publications

Appended papers

This thesis consists of an extended summary and the following appended papers:

[A] **Xinxin Yang**, Andrei Vorobiev, Andrey A. Generalov, Michael A. Andersson, and Jan Stake, “A flexible graphene terahertz detector”, *Applied Physics Letters*, vol. 111, no. 2, pp. 021102-1–021102-4, July 2017. DOI:10.1063/1.4993434

[B] **Xinxin Yang**, Marlene Bonmann, Andrei Vorobiev, Jan Stake, “Characterization of Al_2O_3 gate dielectric for graphene electronics on flexible substrates”, in 2016 Global Symposium on Millimeter Waves (GSMM), Espoo, Finland, 2016. DOI: 10.1109/GSMM.2016.7500326

Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping with appended papers, or due to contents not related to the thesis.

[a] Andrey A. Generalov, Michael A. Andersson, **Xinxin Yang**, Jan Stake, “Optimization of THz graphene FET detector integrated with a bowtie antenna” in 10th European Conference on Antennas and Propagation (EuCAP), Davos, Switzerland, 2016.

[b] Andrey A. Generalov, Michael A. Andersson, **Xinxin Yang**, Andrei Vorobiev, and Jan Stake, “A 400-GHz graphene FET detector”, accepted by *IEEE Transactions on Terahertz Science and Technology*, vol. 7, no. 5, pp. 614-616, July 2017. DOI: 10.1109/TTHZ.2017.2722360

Abbreviations

AFM atomic force microscope. 8

ALD atomic layer deposition. 25, 27

BOE buffered oxide etch. 22, 23

CL conversion loss. 12

CMOS complementary metal-oxide-semiconductor. 23

CNT carbon nanotube. 5

CVD chemical vapour deposition. 2, 8, 21, 23, 37

EBL electron-beam lithography. 21, 22

FET field-effect transistor. 2, 8, 12, 21, 37

GB grain boundary. 8

GFET graphene field-effect transistor. 2, 3, 7, 9–13, 15–17, 24, 25, 27, 29, 35, 36

h-BN Hexagonal boron nitride. 36

HEMT high-electron-mobility transistor. 1

HOPG highly oriented pyrolytic graphite. 23

IoT Internet of things. 1, 36

LTPS low-temperature polycrystalline silicon. 5

MOSFET metal-oxide semiconductor field-effect transistor. 1

NEP noise equivalent power. 1, 2, 12, 17, 29, 32, 35

NW nanowire. 5

PAR polyarylate. 4

PDMS polydimethylsiloxane. 4, 6

PEN polyethylene naphthalate. 4

PET polyethylene terephthalate. 2, 4, 10, 21, 23, 24, 29, 31

PI polyimide. 4, 6

PMMA polymethyl methacrylate. 6, 24

PTFE polytetrafluoroethylene. 29, 31

SBD Schottky-barrier diode. 1, 2

THz Terahertz. 1, 2, 12, 16, 17, 19, 21, 27, 29, 32, 35, 36

Notations

C_o	capacitance of outer capacitor. 26
E	electric field. 7
I_{THz}	dc current response. 17
L	gate length. 7
L_a	access gap between gate and source/drain. 24
M_s	mismatch factor. 16, 17
$P_{\text{in,int}}$	power absorbed in intrinsic part of device. 16
R_{ipd}	parallel dielectric resistance of inner capacitor. 26
R_{ipl}	parallel leakage resistance of inner capacitor. 26
R_n	minimum noise temperature. 13
R_{opd}	parallel dielectric resistance. 26
R_{opl}	parallel leakage resistance. 26
R_D	parasitic source resistance. 7, 24
R_{Sh}	sheet resistance. 24
R_S	parasitic drain resistance. 7, 24
$R_{\text{v,int}}$	intrinsic voltage responsivity. 16
T	temperature. 17
T_{min}	minimum noise temperature. 13
T_n	noise temperature. 13
T_0	room temperature. 13
T_D	equivalent drain noise temperature. 13
T_G	equivalent gate noise temperature. 13
T_{gl}	glass transition temperature. 5, 21
V_{THz}	dc voltage response. 17
W	gate width. 7

Z_0 reference impedance. 13
 Z_a antenna impedance. 17
 Z_{in} intrinsic input impedance. 17
 Γ_{opt} optimum source reflection coefficient. 13
 Γ_s source reflection coefficient. 13
 μ carrier mobility. 7, 30
 σ conductivity. 7
 ε_r relative permittivity. 6
 a distance between two carbon atoms. 7
 f_T transit frequency. 11, 12
 f_{max} maximum frequency of oscillation. 11, 12
 g_{ds} intrinsic drain conductance. 12
 g_m intrinsic transconductance. 12
 h_{21} current gain. 11
 k_B Boltzmann constant. 17
 n carrier density. 7
 n_0 carrier density at Dirac point. 7, 30
 n_G carrier density induced by gate voltage. 7
 q electron charge. 7
 v_{drift} carrier drift velocity. 7

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Chapter 1

Introduction

Terahertz (THz) waves are part of the electromagnetic spectrum between microwaves and the optical region, and are loosely defined as the frequency range from 0.3 to 10 THz.¹ Over the past few decades, THz science and technology have attracted considerable interests in applications such as astronomical observation, noninvasive biomedical imaging, nondestructive inspection and security screening.^{2,3} In addition, THz signals can be the carriers for ultrahigh-speed wireless communications. In recent years, wireless data traffic has substantially increased due to the increasing demand for high-speed wireless communications anywhere and at any time. In particular, Internet of things (IoT), which connects all objects in sensory and intelligent manners, is greatly expanding the wireless connectivity market. In the coming age of IoT, rigid and bulky electronics are not in compliance with the complex surfaces, irregular contours, and soft tissues of natural living species. Hence, there is a need for flexible THz electronics.

Graphene, which possesses outstanding electrical and mechanical properties, is a promising candidate for high-frequency flexible electronics. Specifically, as the first real two-dimensional material, graphene has the ability to reversibly undergo high strains and strain rates. These properties promise to revolutionize many applications ranging from solar cells⁴ and photodetectors⁵ to mixers,⁶ sources⁷ and modulators⁸ in the THz frequency range. Furthermore, due to the remarkable progress in the development of plastic materials, graphene devices can be fabricated on plastic substrates for flexible electronics, such as graphene flexible sensing/communication systems with advantages including shape-conforming ability, light weight and low cost^{9,10}.

THz power detectors are key components in THz detection systems. The noise equivalent power (NEP) corresponding to the lowest detectable power is an important figure of merit for such detectors. For comparison, the estimated NEP values of different detectors operating at room temperature are shown in Fig. 1.1. Both Schottky-barrier diode (SBD)s and transistors can be used in THz detection at room temperature. In 2013, R. Han et al. fabricated SBD detectors with the measured minimum $\text{NEP} \approx 29 \text{ pW}/\sqrt{\text{Hz}}$ at 860 GHz.¹¹ Transistors based on different materials can also be used for broadband THz detection and can be directly tuneable by changing gate bias. These materials include Si, GaAs/AlGaAs, InGaP/InGaAs/GaAs, and GaN/AlGaN.^{11–16} In the frequency range from 100 to 200 GHz, Si metal-oxide semiconductor field-effect transistor (MOSFET) THz detector can reach NEP of $15 \text{ pW}/\sqrt{\text{Hz}}$.¹² In 2017, H. Qin et al.¹⁷ develop GaN/AlGaN high-electron-mobility transistor

(HEMT) detector with the minimum NEP of $30 \text{ pW}/\sqrt{\text{Hz}}$ at 900 GHz.

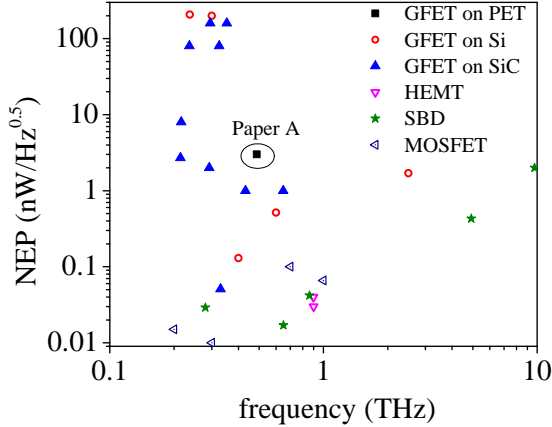


Figure 1.1: Comparison of estimated NEP for GFET detector in [Paper A] and literatures^{7,17–21} to other kind of detectors: SBD,^{22,23} HEMT,^{11,16,24} and MOSFET.^{12–15}

In 2012, L. Vicarelli et al.¹⁹ demonstrated the first field-effect transistor (FET) THz detector based on exfoliated graphene on Si/SiO₂ substrate. The values of the NEP are approximately $200 \text{ nW}/\sqrt{\text{Hz}}$ and $30 \text{ nW}/\sqrt{\text{Hz}}$ for monolayer and bilayer devices, respectively. Nevertheless, the area of high-quality exfoliated graphene from natural graphite is limited to hundreds of micrometres squared and is thus not scalable to meet the requirements of high-volume manufacturing. In 2014, A. Zak et al.¹⁸ developed the first chemical vapour deposition (CVD) graphene FET THz detector with an estimated NEP of $515 \text{ pW}/\sqrt{\text{Hz}}$. Currently, the minimum NEP of a graphene THz detector is achieved by a graphene field-effect transistor (GFET) on SiC substrate.¹⁷ Although the GFET detectors have lower sensitivity than that of SBD detectors and transistor detectors now, GFETs have shown great potential as sensitive THz detectors. Furthermore, taking advantages of graphene with excellent mechanical properties, GFET are expected to play an important role in the development of flexible THz technology.

In this thesis, GFET THz detectors on flexible substrates are demonstrated in the following six chapters. Chapter 2 presents an overview of flexible electronics, graphene properties and GFET characteristics. Chapter 3 provides the detailed description of a GFET THz detection model and the design of antennas and detectors. Chapter 4 describes the processes for fabricating GFET detectors on polyethylene terephthalate (PET) substrates. Chapter 5 discusses the measurement setup and the dc and THz characterisation results. Chapter 6 summarises the results of this thesis and provides a future outlook.

Chapter 2

Graphene flexible high-frequency electronics

Graphene combines high carrier mobility and saturation velocity, ultra-thin thickness, and outstanding flexibility and stretchability, which are attractive properties for flexible high-frequency electronics. This chapter provides an overview of flexible electronics and the fundamental electrical and mechanical properties of graphene. In addition, the figures of merit and noise performance of GFETs are discussed.

2.1 Flexible electronics

Flexible electronics that are capable of undergoing mechanical deformations without losing functionality have been rapidly developing over the past two decades.²⁵ Due to their excellent features, including wearability, biocompatibility, light weight and low cost, flexible electronics have already been successfully used in a wide range of applications, such as displays, solar cells, medical sensors, and communication and wireless systems.^{26, 27}

2.1.1 Fabrication technology for flexible electronics

Flexible electronics can be produced by transferring or bonding normal rigid devices to flexible substrates.²⁵ The advantage of this approach is that it provides high-performance devices. However, the processes of this approach are generally complex and expensive, and the fragile nature of rigid substrates (e.g. Si, GaAs or glass wafers) imposes limitations on the flexibility and lifetime of the devices. With the development of polymer technology, direct fabrication on flexible substrates is rapidly encroaching into the realm of the transfer approach. In recent years, increasingly more researchers have concentrated on direct fabrication using direct and innovative techniques to reduce fabrication costs and improve throughput. Based on the fabrication technique, flexible electronics can be divided into two basic categories: solid-phase and liquid-phase approaches.

Liquid-phase approaches

Semiconductor materials in a solution are deposited onto flexible substrates by liquid-phase approaches, including gravure/inkjet printing, spin coating and so forth. Semiconducting inks are generally prepared using purification, dispersion and separation processes. Thus, this approach could be suitable for high-throughput and large-area manufacturing. However, liquid-phase fabrication may inevitably induce many charge traps caused by the chemical solvents used, non-uniformity of semiconductor layers produced by the surface tension of liquids, and structural defects produced during the fabrication processes.

Solid-phase approaches

For solid-phase fabrication, semiconductor materials supported on solid and rigid wafers are placed onto flexible substrates. The subsequent processes include forming the source, drain and gate electrodes; insulator; and contact windows. N. Petrone et al.^{28–30} fabricated CNT or graphene transistors on various substrates, such as flexible plastic and paper.

2.1.2 Materials for flexible electronics

The development of high-frequency flexible electronics requires materials to combine outstanding electronic performance with the ability to withstand high levels of strain. The basic building blocks for electronic components are substrates, conductors, semiconductors and dielectrics. Many research efforts have been devoted to developing flexible materials in each of these categories.

Substrates

The materials for flexible substrates can generally be grouped into three categories: plastic films, metal foils and fibrous materials (e.g. paper and textiles). As the most common flexible substrates, plastic films include PET, polyethylene naphthalate (PEN), polydimethylsiloxane (PDMS), polyimide (PI), and polyarylate (PAR). The properties of plastic film vary greatly from material to material. In general, plastic films are relatively inexpensive and lightweight. The material properties of commonly used plastic films are listed in Table 2.1. Metal foils, such as stainless steel, titanium and copper foils, have excellent electrical and thermal properties. However, compared to plastic films, these foils tend to be more expensive and less flexible. In addition, paper, clothing or other textiles can also be used as flexible substrates for low-cost or wearable electronics.

Conductors

Metals that withstand modest bending-mode deformations are the best known electrical conductors. However, metal films are mechanically inadequate in

Table 2.1: Material properties of flexible substrates used for GFETs.^{31–33}

Property	PEN	PET	PI	PDMS
Young's modulus (MPa)	620	$\sim 3 \times 10^3$	4×10^3	0.36-0.87
Density (g/cm ³)	1.36	1.38	1.42	0.97
Relative permittivity (ϵ_r)	3.2-3.4	2.9	~ 3.5	2.3-2.8
Glass transition temperature (T_{gl}) (°C)	155	81	300-410	N/A
Thermal conductivity (W/mK)	0.15	~ 0.2	~ 1	0.15
Electrical resistivity (Ωcm)	1×10^{15}	1×10^{17}	1.5×10^{17}	4×10^{13}

applications that require large-scale bending,^{34–36} which has led to the development of alternative materials. With electrically conducting fillers such as metals, carbon nanotubes or other nanowire (NW)s,³⁷ polymeric materials can also be used as conductors. Polymeric conductors tend to have considerably lower electrical conductivity and stability than metallic conductors.³⁸ In addition, networks of NWs, carbon nanotube (CNT)s³⁰ or graphene flakes are also used to form strain-tolerant conducting films.

Semiconductors

Semiconductors, which dominate the electrical properties of integrated devices, are used extensively in electronic circuits. Most of the approaches used for flexible conductors can also be adapted to form flexible semiconductors, such as organic semiconductors,³⁷ hydrogen-terminated amorphous silicon (a-Si:H), low-temperature polycrystalline silicon (LTPS), semiconducting metal oxides, NWs,³⁹ CNTs, and graphene. In terms of properties, organic semiconductors are inexpensive and highly flexible, but they have a limited carrier mobility of less than 100 cm²/Vs. a-Si:H has modest properties in terms of carrier mobility and flexibility. LTPS has a high mobility but low flexibility. Semiconducting metal oxides with rare earth elements are expensive. CNTs and graphene possess excellent electrical and mechanical properties. In particular, graphene prepared using a technical method for wafer scalability shows the highest mobility of above 10,000 cm²/Vs on plastic films and is able to survive mechanical tensile strains of up to 200%. Graphene-based transistors are becoming increasingly more attractive in the pursuit of novel flexible high-frequency electronics.

Dielectrics

For high-speed and low-voltage transistors, dielectrics with a high relative permittivity (ϵ_r) and thin thickness are needed.⁴⁰ However, due to the presence of a leakage current between the source and gate, an ultrathin dielectric does not possess a good insulator property. The ceramic oxides (e.g. SiO_2) and the high- κ dielectrics (e.g. Al_2O_3 , HfO_2 , TiO_2 , and ZrO_2) developed for conventional rigid electronics generally achieve impressive electronic performance. However, these dielectric materials can only be used in applications that require modest flexibility. If large stretchability is necessary, polymeric dielectrics such as PDMS, polymethyl methacrylate (PMMA) or PI are generally obtained by spin coating, casting or printing at room temperature.^{41–43} In addition, hybrid dielectrics that include both high- κ oxides and polymers have also been demonstrated, with excellent mechanical flexibility, large dielectric constant, and low leakage current.⁴⁴

2.2 Graphene properties

Novoselov and Geim were awarded the 2010 Nobel Prize in physics for their pioneering research on graphene, a two-dimensional sheet of carbon atoms arranged in a honeycomb lattice.⁴⁵ The impressive electrical and mechanical properties of graphene have opened up new horizons for flexible high-frequency electronics.⁴⁶

2.2.1 Electrical properties

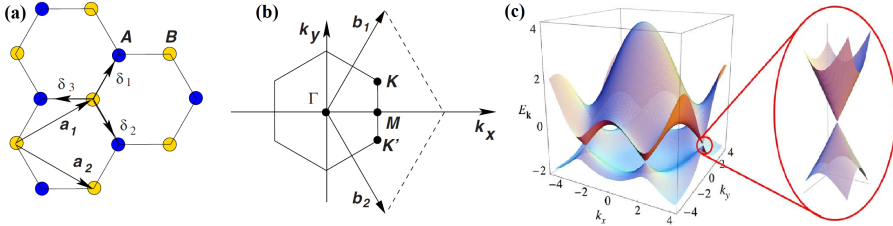


Figure 2.1: Graphene honeycomb lattice structure (a), Brillouin zone (b) and band structure (c).⁴⁷

In 1947, Wallace first analysed the band structure of monolayer graphene by using the tight-binding approach.⁴⁸ The graphene honeycomb lattice structure composed of carbon atoms can be viewed as two interpenetrating triangular lattices, as shown in Fig. 2.1. Considering both the nearest- and next-nearest-neighbour atoms in graphene, the energy bands derived from the tight-binding Hamiltonian are

$$E_{\pm}(\mathbf{k}) = \pm t \sqrt{3 + f(\mathbf{k})} - t' f(\mathbf{k}) \quad (2.1)$$

where $f(\mathbf{k}) = 2 \cos(\sqrt{3}k_y a) + \cos(\sqrt{3}k_y a/2) \cos(3k_x a/2)$, $a = 1.42 \text{ \AA}$ is the distance between two carbon atoms, and $t = 2.8 \text{ eV}$ and $t' = 0.1 \text{ eV}$ are the nearest-neighbour and next nearest-neighbour hopping energies, respectively. The band structure of large-area graphene is shown in Fig. 2.1 (c). The valence and conduction bands are cone shaped and meet at the K points of the Brillouin zone. The mobility and the saturation velocity describe the carrier transport in low and high electric fields, respectively. The linear dispersion relationship close to one of the Dirac points indicates two-dimensional massless electrons in graphene, which represents the origin of the superior carrier mobility in ideal graphene. The carrier mobility in suspended monolayer graphene is greater than $200,000 \text{ cm}^2/\text{Vs}$ at 5 K, which allows for accessing the intrinsic transport properties of graphene.⁴⁹ However, a substrate and a gate dielectric are typically required in real applications. The presence of charge carrier scattering limits the electron mean free path and leads to degradation of the mobility, which is a major barrier in the development progress of graphene. The maximum values of carrier velocity for graphene devices are approximately $4 \times 10^7 \text{ cm/s}$, compared with values of $2 \times 10^7 \text{ cm/s}$ for GaAs and 10^7 cm/s for silicon. In addition, the velocity in graphene at high fields does not drop as drastically as in the III-V semiconductors,⁵⁰ which represent a new class of electronic devices.

In the low field, the carrier drift velocity is linear in field strength with the carrier mobility, $v_{\text{drift}} = \mu E$. There are three common approaches to measure or extract the carrier mobility in graphene:

- Hall mobility. The Hall mobility is measured using the Hall effect in Hall bar or van der Pauw structures.
- Effective mobility. The effective mobility is defined as $\mu = \sigma/(nq)$, where σ is the conductivity and n is the carrier density estimated via the gate capacitance and voltage.
- Field-effect mobility. The field-effect mobility is defined by the slope of the conductivity curve $\mu = d\sigma/dV_{\text{GS}}/C_{\text{G}}$. In GFETs, a semi-empirical model is widely used for evaluation of the field-effect mobility by fitting the model to the measured total device resistance.

$$R_{\text{tot}} = R_{\text{S}} + R_{\text{D}} + \frac{L}{Wq\mu\sqrt{n_0^2 + n_{\text{G}}^2}}, \quad (2.2)$$

where R_{S} and R_{D} are the source and drain resistances, respectively; q is the electron charge; μ is the carrier mobility; L and W are the gate length and width, respectively; and n_0 is the carrier density at the Dirac point. n_{G} is the carrier density induced by the gate voltage, which can be obtained from the following equation: $V_{\text{G}} - V_{\text{Dir}} = en_{\text{G}}/C_{\text{G}} + \hbar v_{\text{F}} \sqrt{\pi n_{\text{G}}}/q$,⁵¹ where V_{Dir} is the gate voltage at the Dirac point.

2.2.2 Mechanical properties

The mechanical properties of graphene are controlled by the characteristics of ideal pristine crystal lattices and structural defects such as grain boundaries. Lee et al.⁵² conducted the first systematic experimental analysis of the elastic properties and intrinsic strength of free-standing monolayer graphene membranes by nanoindentation in an atomic force microscope (AFM). The Young's modulus and third-order elastic stiffness of monolayer graphene are 1.0 TPa and -2.0 TPa, respectively. Brittle fracture of graphene occurs at a critical stress equal to its intrinsic strength of 130 GPa.⁵² Furthermore, graphene sheets can sustain stretching as large as 20%. These values are considerably larger than those of all other materials, which stimulates great interest in applying graphene for various applications.

In recent years, large-area polycrystalline graphene sheets grown using CVD have been widely used. As unavoidable structural elements in polycrystalline graphene, grain boundary (GB)s influence the mechanical properties of graphene. The nanoindentation experiments with CVD graphene membranes showed that the intrinsic strength of CVD graphene is approximately 35 GPa,⁵³ which is considerably lower than the intrinsic strength (130 GPa) of pristine graphene. This result is explained by Ruiz Vargas et al. by assuming the presence of nanovoids at real GBs, which significantly decrease the strength characteristics of graphene.⁵³

2.2.3 Optical properties

The optical properties of graphene are determined by the direct interband electron transitions, which can be modulated by an external gate field.⁵⁴ Thus, the transition and absorption coefficients of monolayer graphene are 97% and 2.3%, respectively, independent of the wavelength.⁵⁵ The graphene-light interaction is strong. Monolayer graphene can absorb the same amount of 1.55 μm light as a 20 nm thick film of InGaAs.⁵⁶ The electron-hole pairs generated by photoexcitation in graphene can be separated by built-in electric fields of metal/graphene contacts, which can be used as the basis of graphene photodetectors.^{5,57}

2.3 Graphene field-effect transistors

For high-frequency electronics, FETs should respond quickly to variations in the gate voltage, which requires short gate lengths and high-speed carriers in the channel. Unfortunately, scaling of the gate length to smaller values introduces many problems, such as degradation of the gate control electrostatic profile in the channel, drain-induced barrier lowering, impaired drain-current saturation and threshold-voltage roll-off.⁵⁸ These problems can be countered by increasing the doping density in the channel and using ultra-thin body channel FETs. The first approach leads to a mobility reduction due to increased

impurity scattering. For the second approach, a FET with a thin barrier and a thin gate-controlled region will be robust against short-channel effects.

Graphene with its purely two-dimensional structure could help the microelectronics industry continue down-scaling, which is one of the attractive features of graphene for use in transistors. Moreover, the impressive graphene carrier transport properties (e.g. high carrier mobility and saturation velocity at room temperature and sub-THz transit frequency at moderate channel lengths) offer attractive prospects for high-frequency applications.⁵⁹ Due to its exceptional electronic properties and outstanding mechanical performance, graphene is a promising material for use in flexible and transparent FETs.

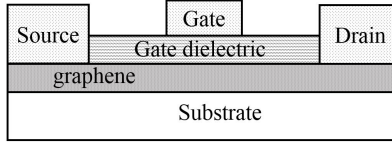


Figure 2.2: Device schematic of a GFET.

A schematic of a GFET with the source, drain, and gate terminals is shown in Fig. 2.2. The operation of GFETs relies on controlling the drain current by the gate voltage.

Compared with traditional semiconductor transistors, GFETs have ambipolar field-effect characteristics, as shown in Fig. 2.3. Both the carrier density and the type of carrier in the graphene channel are governed by the potential differences between the channel and the gate. Large positive and negative gate voltages promote an n-type channel and a p-type channel, respectively, which leads to the two branches of the transfer characteristics separated by the Dirac point. The position of the Dirac point is defined by charged impurities in the dielectric and at the interface between the dielectric and graphene.

2.3.1 Small-signal equivalent GFET circuit

Depending on the magnitude of the time-varying terminal voltage signals, the dynamic operation of GFETs can be classified as large-signal nonlinear operation and small-signal linear operation. The small-signal equivalent circuit provides only limited information, but it allows modelling S-parameters, calculating figures of merit and estimating the noise performance of GFETs in an easy way. However, it is not suitable for characterising power transistors, which is nonlinear operation. The large-signal equivalent circuit of GFETs for THz power detection will be demonstrated in the following chapter.

As shown in Fig. 2.4, the conventional small-signal equivalent circuit can be divided into two parts: the intrinsic elements (marked by a dashed rectangle) and the extrinsic elements. The intrinsic elements include g_m , C_{GS} , C_{GD} , C_{DS} , R_{DS} and R_i , and the extrinsic elements include L_G , R_G , C_{PG} , L_D , R_D , C_{PD} , L_S and R_S . The values of the equivalent circuit elements can be derived from

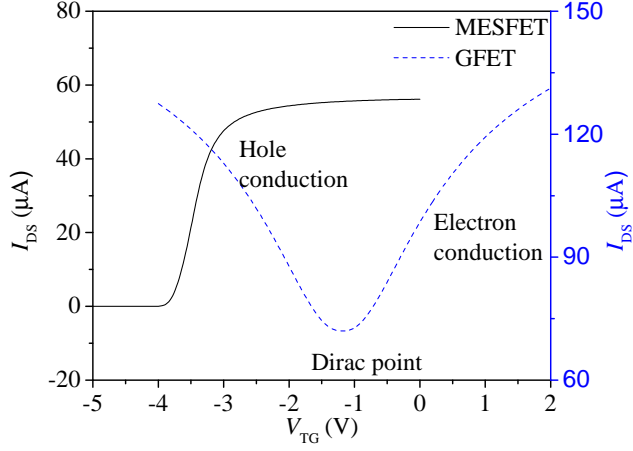


Figure 2.3: MESFET and GFET transfer characteristics.

measured S-parameters through fitting techniques. Since the circuit is based on the hybrid- π model, the Y-parameters of the circuit can be derived as follows:⁶⁰

$$Y_{11} = \frac{R_i C_{GS}^2 \omega^2}{D} + j\omega \left(\frac{C_{GS}}{D} + C_{GD} \right), \quad (2.3)$$

$$Y_{12} = -j\omega C_{GD}, \quad (2.4)$$

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{GS} \omega} - j\omega C_{GD}, \quad (2.5)$$

$$Y_{22} = g_d + j\omega C_{GD}, \quad (2.6)$$

where $D = 1 + R_i^2 C_{GS}^2 \omega^2$.

The measured and modelled S-parameters of a GFET on PET without bias in the frequency range of 0.1 to 20 GHz are shown in Fig. 2.5. The extracted parameters of a GFET found by de-embedding the S-parameters and cross-checked by fitting the dc transfer characteristics are shown in Table 2.2. Because the device layout is symmetric, R_S and R_D are considered to be equal.

Table 2.2: Extracted parameters of a GFET.

L (μm)	W (μm)	C_{GS} (fF)	C_{DS} (fF)	$R_S = R_D$ (Ω)	R_i (Ω)	g_m (mS)
1.8	20	24	25	100	3	2.1

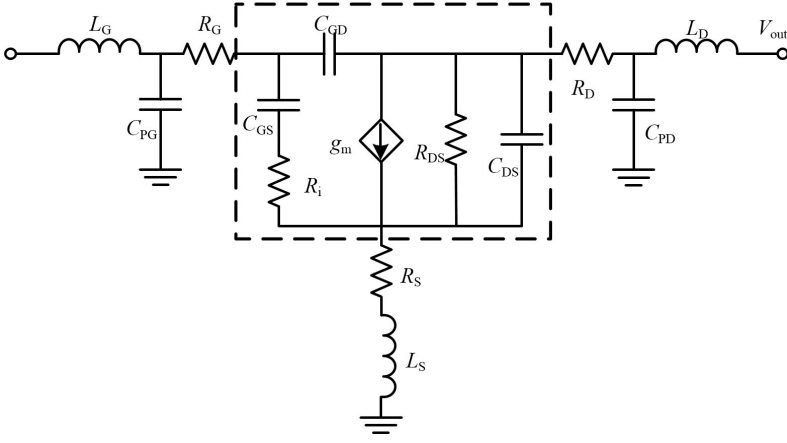


Figure 2.4: Small-signal hybrid- π equivalent circuit of a GFET.

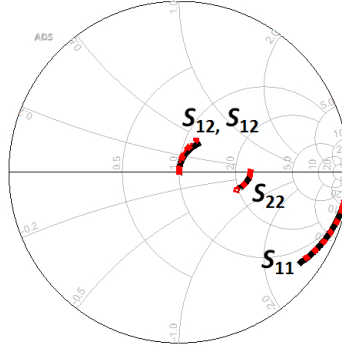


Figure 2.5: Measured and modelled GFET S-parameters from 0.1 to 20 GHz at the bias point of $V_{GS} = 0$ V and $V_{DS} = 0$ V.

2.3.2 Figures of merit

Extracting the small-signal parameters of GFETs allows calculating the figures of merit, which can be used to conduct performance comparisons. The transit frequency (f_T) and maximum frequency of oscillation (f_{max}) are two important performance metrics of high-frequency GFETs.

f_T is the frequency where the magnitude of the small-signal current gain (h_{21}) rolls off to unity. The current gain is defined as the ratio of the small-signal output current to the input current of the transistor and can be derived from measured S-parameters as follows.

$$h_{21} = \frac{i_2}{i_1} = \frac{y_{21}}{y_{11}} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \quad (2.7)$$

Based on the small-signal equivalent circuit from Fig. 2.4, f_T can be

written as⁴⁰

$$f_T \approx \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})[1 + g_{ds}(R_S + R_D)] + C_{GD}g_m(R_S + R_D)}, \quad (2.8)$$

where $g_m = dI_D/dV_{GSi}$ is the intrinsic transconductance which is determined by the gate capacitance and n_0 . $g_{ds} = dI_D/dV_{DSi}$ is the intrinsic drain conductance. Therefore, the optimisation of f_T involves increasing g_m and minimising the gate capacitance and contact resistance. Additionally, the minimisation of other parasitic capacitances is necessary. Currently, the highest experimental f_T value reported for a GFET is 427 GHz with a 60 nm gate length and SiC substrate.⁶¹

f_{max} is the frequency where the maximum unilateral power gain (U) goes to unity. Thus, f_{max} is the maximum frequency at which the transistor still provides a power gain. f_{max} can be written as⁴⁰

$$f_{max} \approx \frac{g_m}{2\pi(C_{GS} + C_{GD})} \frac{1}{\sqrt{4g_{ds}(R_S + R_G + R_i) + 4g_m R_G \frac{C_{GD}}{C_{GS} + C_{GD}}}}. \quad (2.9)$$

The majority of high-frequency applications require a high f_{max} , which characterises the amplifying ability of the FET. However, due to the zero band gap in monolayer graphene, f_{max} is very low since there is no drain current saturation and hence high g_{ds} . The bandgap can be engineered, for example, in graphene nanoribbons or in bilayer graphene by applying an out-of-plane electric field. However, the mobility in graphene decreases with the bandgap even faster than that in the semiconductors.⁶²

Another direction is the development of millimetre wave and THz devices, which are still exploiting the advantages of the unique graphene properties but do not require graphene transistors working in the amplification mode. The most interesting types of such devices are millimetre wave GFET mixers and GFET THz power detectors. The main parameters of the mixers are conversion loss, or conversion gain, proportional to the on-off ratio of the drain resistance. For the detector, it is the voltage responsivity (proportional to the derivative of the drain conductance) and NEP. It can be shown that conversion loss (CL) and NEP are inversely proportional to the mobility; hence, the devices can exploit the intrinsically high graphene carrier velocity. This is why the topic of the present thesis is developing GFET THz power detectors.

2.3.3 Noise

Noise is an important parameter in electronic devices, particularly in the areas of small-signal detection and low-noise amplifiers. In GFETs, the main noise sources include thermal noise, shot noise, and $1/f$ noise. The thermal noise arises from the thermal agitation of the charge carriers, which is unavoidable in any electronic system.⁶³ The shot noise originates from the discrete nature of the electric charge, and it is negligible with a low or zero-drain-source bias.⁶⁴

For high-frequency operation, $1/f$ noise is at a low level, and the thermal noise dominates the performance of GFETs.⁶⁵ Thus, the noise of GFETs can be expressed through the noise temperature (T_n),⁶⁶

$$T_n = T_{\min} + \frac{4T_0 R_n |\Gamma_s - \Gamma_{opt}|^2}{Z_0(1 - |\Gamma_s|^2)|1 + \Gamma_{opt}|^2}, \quad (2.10)$$

where Z_0 is the reference impedance and T_0 is room temperature. Γ_s is the source reflection coefficient. And Γ_{opt} is the optimum source reflection coefficient, where $T_n = T_{\min}$ is obtained. T_{\min} is the minimum noise temperature. R_n is the noise resistance quantifying the sensitivity to increased noise temperature with $\Gamma_s \neq \Gamma_{opt}$. $T_{\min} \approx f/f_T \sqrt{(R_S + R_G + R_i)T_G g_{ds} T_D}$ is the minimum noise temperature, where T_D and T_G are equivalent drain and gate noise temperatures, respectively.⁶⁷ Therefore, one can improve the noise level by increasing the carrier mobility, saturation velocity, and f_T . Furthermore, thermal noise can be minimised by reducing the contact resistance.

Chapter 3

GFET THz detector modelling and design

Sine the first GFET THz detector was demonstrated in 2012,¹⁹ the physical model constructed from the plasma-wave theory by Dyakonov–Shur have been reported. However, it is difficult to implement the overdamped plasma model in circuit simulators, and it can not provide a reasonable agreement with the measurement results. Instead, the electrical nonlinear model for GFET THz detection is analysed and discussed in this chapter. In addition, the antenna simulation results are provided, which are important for optimising the performance of THz detectors.

3.1 Electrical nonlinear model for GFET THz detection

The electrical nonlinear model is based on the large-signal equivalent circuit of a GFET detector, as shown in Fig. 3.1.⁶⁸ The bias dependence of the intrinsic capacitors is included, which is important when the reactive currents become non-negligible at high frequencies.

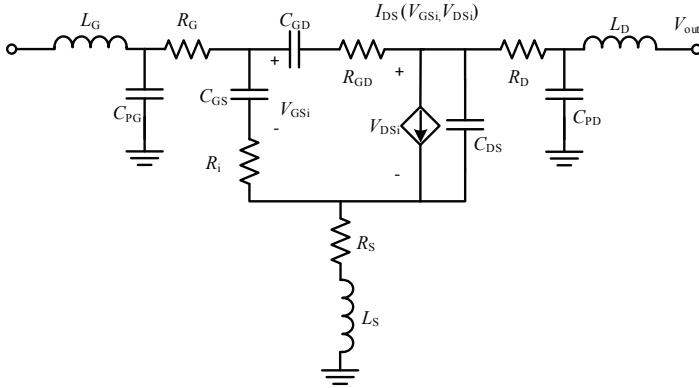


Figure 3.1: Large-signal GFET model. The intrinsic elements are bias dependent.⁶⁸

Because the GFET has two control voltages, the small-signal drain-to-source current (i_{ds}) is a function of the gate-source voltage (v_{gs}) and the drain-source (v_{ds}) voltage and can be expressed by the Taylor series as (limited to 2 orders)^{68,69}

$$i_{ds}(v_{gs}, v_{ds}) = g_{m1}v_{gs} + g_{ds1}v_{ds} + g_{m2}v_{gs}^2 + g_{ds2}v_{ds}^2 + g_{11}v_{gs}v_{ds}, \quad (3.1)$$

The coefficients of the Taylor series at the bias point (V_{GS} , V_{DS}) obtained from the derivatives of the drain-source current I_{DS} can be expressed as

$$g_{mx} = \frac{1}{x!} \frac{\partial^x I_{DS}}{\partial V_{GS}^x} \bigg|_{V_{DS}}, \quad (3.2)$$

$$g_{dsx} = \frac{1}{x!} \frac{\partial^x I_{DS}}{\partial V_{DS}^x} \bigg|_{V_{GS}}, \quad (3.3)$$

$$g_{xy} = \frac{1}{x!y!} \frac{\partial^{x+y} I_{DS}}{\partial V_{GS}^x \partial V_{DS}^y}. \quad (3.4)$$

Upon THz irradiation with a frequency of ω ,

$$v_{gs} = v_{THz} \cos(\omega t), \quad (3.5)$$

$$v_{ds} = \alpha v_{THz} \cos(\omega t + \theta), \quad (3.6)$$

where α is the amplitude ratio of v_{ds} to v_{gs} and θ is the phase difference between them. v_{THz} is the input THz voltage which is determined by the antenna coupling and the impedance matching between the GFET and the antenna.

The dc current response generated by the even-order non-linearity can be expressed as

$$I_{THz} = \frac{1}{2} (g_{m2} + \alpha^2 g_{ds2} + 2\alpha \cos \theta g_{11}) v_{THz}^2. \quad (3.7)$$

Since the dc voltage response and dc current response are connected by channel resistance as follows,

$$V_{THz} = I_{THz} R_{DS}, \quad (3.8)$$

the intrinsic voltage responsivity $R_{v,int}$ is defined by⁷⁰

$$R_{v,int} = \frac{V_{THz}}{P_{in,int}}, \quad (3.9)$$

where $P_{in,int}$ is the power absorbed in the intrinsic part of device. Under general impedance conditions the voltage responsivity is reduced as quantified by the mismatch factor M_s as bellow.

$$R_v = R_{v,int} (1 - |\frac{Z_{in} - Z_a}{Z_{in} + Z_a}|^2), \quad (3.10)$$

where Z_{in} is the intrinsic input impedance of device and Z_a is the impedance of the antenna.

The estimated NEP defined by the thermal noise can be expressed as⁷⁰

$$\text{NEP} = \frac{\sqrt{4k_B T R_{\text{DS}}}}{R_v}, \quad (3.11)$$

where k_B is the Boltzmann constant and T is the absolute temperature.

Similar to the f_T and f_{max} of a GFET derived from the small-signal circuit, the derivation of a 3-dB frequency of halved voltage responsivity from the large-signal circuit is,⁶⁸

$$f_{3\text{dB}} \approx \frac{1}{2\pi C_{\text{GS}} \sqrt{R_{\text{DS}} R_s}}. \quad (3.12)$$

3.2 Detector topology

As shown in Fig. 3.2, there are four possible topologies of a GFET THz detector. For topology (a), the THz signal is coupled to the gate only ($v_{\text{ds}} = 0$). Thus, the THz response depends on g_{m2} , which is very low without source-drain bias. For topology (b), the THz signal is applied to the drain only ($v_{\text{gs}} = 0$). Therefore, the THz response relies on g_{ds2} . However, due to zero bandgap, a GFET has linear output characteristics with $g_{\text{ds2}} \approx 0$. Consequently, the THz response is also very low. For topologies (c) and (d), the THz signal is coupled to both the gate and drain through a capacitor. Therefore, all second-order terms become important in Eq. (3.1). Since both g_{m2} and g_{ds2} are almost 0, g_{11} is the main parameter for THz detection, and this topology generates a higher current than the other topologies.

Since g_{11} is proportional to the aspect ratio (W/L), the wider transistor with the minimum allowed gate length can maximise I_{THz} . However, this cannot increase the V_{THz} based on Eq. 3.8. In reality, NEP is a more important figure of merit for choosing the device dimension. Considering the frequency-dependent of NEP,⁶⁸ a GFET with shorter gate length and narrower gate width show better noise performance.

3.3 Antenna design

An antenna that improves the coupling efficiency between the antenna and THz radiation is one of the key parts of GFET THz detectors. Fig. 3.3 (a) shows the layout of a bow-tie antenna. The pads for the gate and drain are located at the two ends of the bow-tie antenna. According to the electrical nonlinear model, the THz voltage responsivity is reduced as quantified by the impedance mismatch factor M_s between the GFET and the antenna. The factor can be optimised by adjusting the impedance of the antenna, the ratio of L/W , and the gate bias voltage. In this work, the bow-tie antenna was

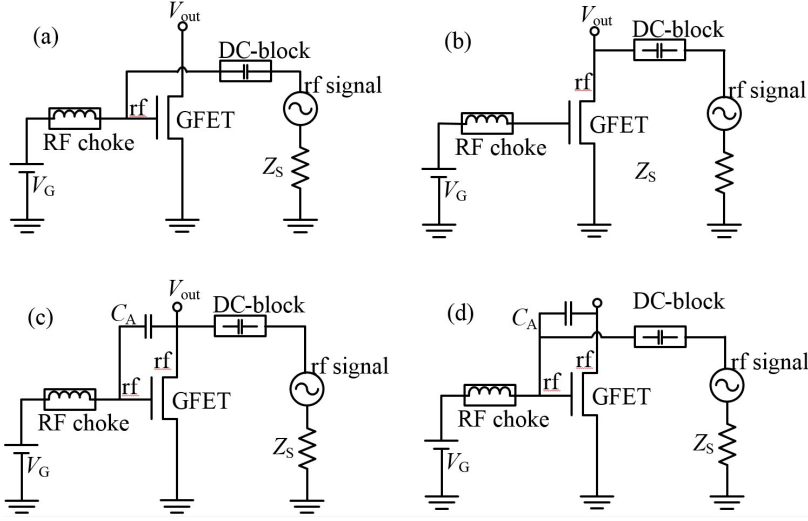


Figure 3.2: Three possible topologies of GFET detector with (a) $v_{gs} = v_{THz} \cos(\omega t)$ and $v_{ds} = 0$, (b) $v_{gs} = 0$ and $v_{ds} = v_{THz} \cos(\omega t)$, (c) $v_{gs} = v_{THz} \cos(\omega t)$ and $v_{ds} = \alpha V_{THz} \cos(\omega t + \theta)$, (d) $v_{ds} = v_{THz} \cos(\omega t)$ and $v_{gs} = \alpha v_{THz} \cos(\omega t + \theta)$.

simulated by using HFSS. The simulated antenna reflection coefficients at the gate-source port are shown in Fig. 3.3 (b). This figure implies that the antenna radiates best at 487 GHz, where $S_{11} = -17$ dB. Furthermore, if the antenna bandwidth is defined as the frequency range where S_{11} is less than -10 dB, then the bandwidth would be more than 50 GHz.

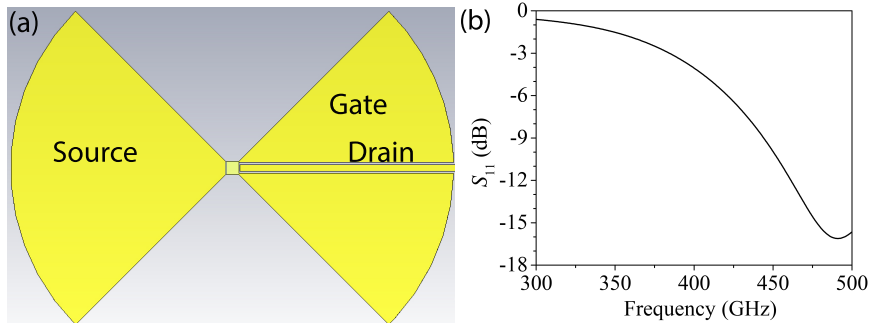


Figure 3.3: Bow-tie antenna layout (a), and its reflection coefficient at the gate-source port (b).

As one of the fundamental antenna parameters, directivity of an antenna is equal to the ratio of the radiation intensity in a given direction from the

antenna to the radiation intensity averaged over all directions. Larger values of directivity imply a more focused antenna. The simulated antenna directivity at 487 GHz is shown in Fig. 3.4. The maximum directivity is 2.3 dB. An efficient method for increasing the antenna directivity is to place the antenna on a dielectric lens. The simulated antenna directivity of a hyperhemispherical silicon lens-coupled bow-tie antenna is shown in 3.4. The maximum directivity increases from 2.3 dB to 19 dB.

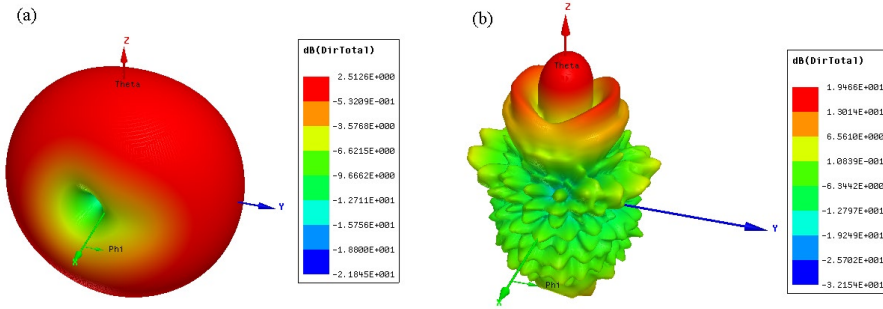


Figure 3.4: HFSS simulated directivity of the bow-tie antenna (a) and the bow-tie antenna with Si lens(b).

3.4 Detector optimisation

As shown in Fig. 3.5, four different types of THz detectors are fabricated to unveil the detection physical mechanism for an optimised detector design. The insets are enlarged views of the central active regions. The main characteristics of these detectors are described below.

- Detector-a, used in Paper A. Asymmetric design of drain and gate is conducive to the asymmetric THz distribution in the electron channel which is essential for the enhancement of response.
- Detector-b. Compared to detector-a, part of antenna connected to the gate are replaced by the connection of drain. The capacitance between gate and drain is less.
- Detector-c. Symmetric design of drain and source should result in reduced THz response.
- Detector-d. Detector with three gates are used for analysing the effect of p-n junction in graphene channel on the THz response.

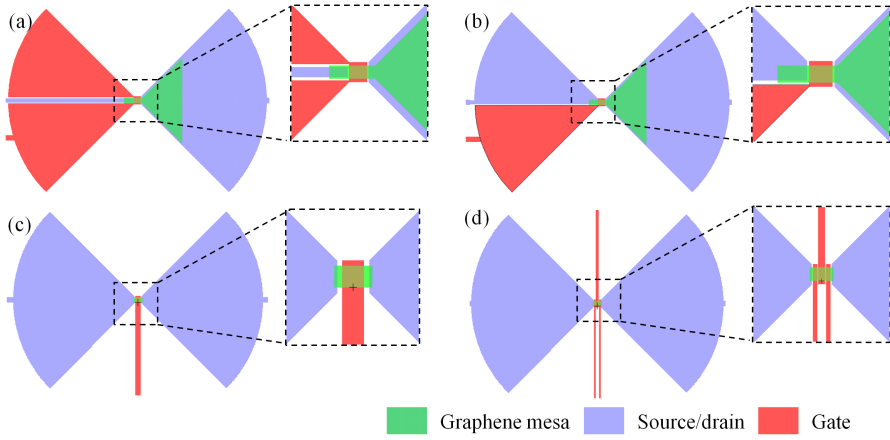


Figure 3.5: Four different types of THz detectors: detector-a (a); detector-b (b); detector-c (c); detector-d (d).

Chapter 4

Device fabrication

To achieve high-performance THz detectors, in addition to the rational design, state-of-the-art processing technologies are also required. In this chapter, the processes for fabricating graphene THz detectors on plastic substrates are introduced, and the fabrication techniques with emphasis on properties of three critical interfaces are discussed. These interfaces include the interface between graphene and the substrate, the interface between graphene and the metal (ohmic contact), and the interface between graphene and the gate dielectric. High quality of these interfaces is necessary for realising high-performance THz detectors.

4.1 Fabrication process flow

Compared to the normal rigid substrates(e.g. Si, GaN, and glass), there are several limitations during the fabrication of devices on PET. One of the limitations is the processing temperature. The glass transition temperature (T_g) for crystalline PET is 81 °C.³² Thermally induced crystallization occurs when the PET is heated above T_g . Thus, the annealing process or baking the resist at high temperature cannot be used in the fabrication process of flexible THz detectors. In addition, because PET is insulating, charges occurring during electron-beam lithography (EBL) cannot be appropriately discharged from the substrate and may distort the structures. This problem can be eliminated if a conductive layer is applied on the e-beam resist prior to EBL.

As shown in Fig. 4.1, in this work standard fabrication process has been modified with the aim to achieve low-resistance ohmic contacts and graphene with a low residual carrier concentration, which is required for high-performance flexible detectors. The effect of the residual charge carrier concentration on the GFET THz detector performance is discussed in Paper A. The graphene layer was covered by a protective layer to prevent any liquids from coming into contact with the graphene in the FET channel during the next steps for a cleaner gate dielectric/graphene interface and a lower residual carrier density. Furthermore, the fabrication of the gate dielectric, electrodes and pad contact are combined in one step to reduce number of processing steps. The detailed process parameters are listed in Appendix A and the details of processing steps shown in Fig. 4.1, are listed below.

- Graphene on PET substrate. The graphene in this work was grown by CVD on copper foils and transferred onto PET substrates.

- **Protective layer.** The deposition by e-beam evaporation and natural oxidation in air of a 1 nm Al layer was repeated 2 times to achieve a uniform dielectric layer as the protective layer. This layer allows avoiding any undesired impurities introduced into graphene during the fabrication processes.
- **Mesa isolation.** Patterns of graphene channels were defined by EBL. The protective layer was etched by buffered oxide etch (BOE) solution and followed by etching graphene using oxygen plasma.
- **Ohmic contact.** Source/drain electrodes were patterned by EBL followed by the e-beam deposition of Ti/Pd/Au (1 nm/ 15 nm/ 180 nm) and the standard lift-off process.
- **Gate dielectric and gate electrode.** Gate electrodes were patterned by EBL. The e-beam evaporation and oxidation in air of a 1 nm Al layer was repeated five times to achieve a uniform gate dielectric layer. In the last step, Al/Au (150 nm/ 80 nm) was subsequently deposited by e-beam evaporation and lifted off for the gate electrodes and pad contacts.

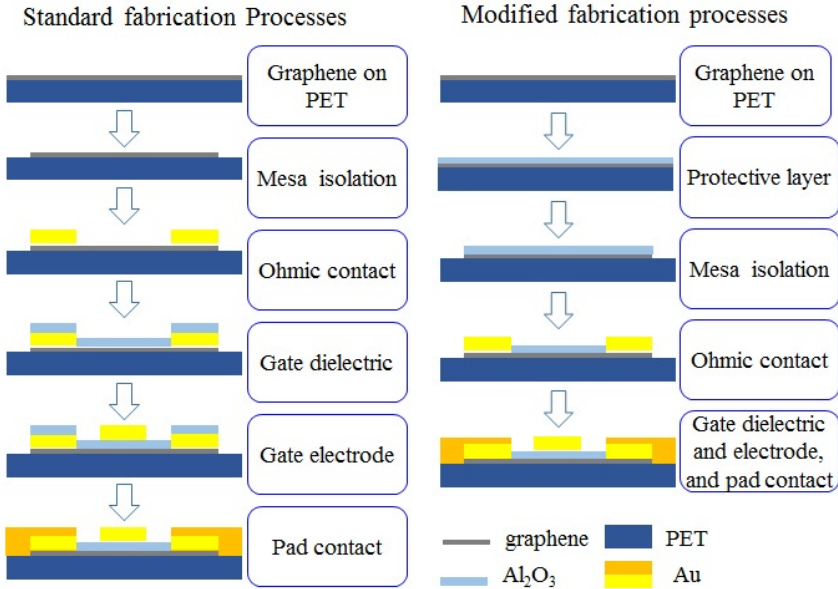


Figure 4.1: Schematics of the fabrication processes for GFET THz detectors.

4.2 PET substrate

PET is insoluble in water, in BOE and in many common organic solvents, which is a necessary property for the use as a substrate in electronics. The material properties of PET are shown in Table 2.1. Theoretical model of van der Waals interaction⁷¹ predicts that the surface roughness of the substrate can affect the adhesion of the graphene layers. To understand and characterise the interfacial adhesion of graphene on PET substrates, it is essential to characterise the surface roughness. As shown in Fig. 4.2, the surface roughness of the PET is considerably larger than that of the Si/SiO₂ (300 μm /300 nm) substrate. Thus, the adhesion of graphene on PET is potentially less than that on Si/SiO₂, which requires development of more gentle fabrication processes to avoid graphene disintegration.

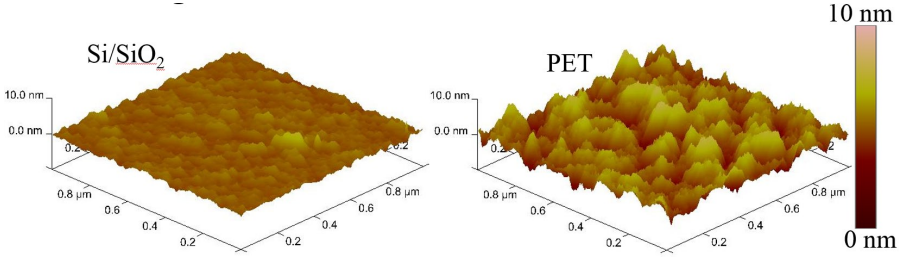


Figure 4.2: Atomic force microscope (AFM) images of the Si/SiO₂ substrate (left) and the PET substrate (right).

4.3 Graphene growth and transfer

There are three major approaches to obtain high-quality graphene sheets: mechanical exfoliation of highly oriented pyrolytic graphite (HOPG), epitaxial growth on SiC substrates, and CVD on metal foils. For commercial viability, low-cost and scalable large-area synthesis is necessary. Thus, mechanical exfoliation using adhesive tapes is clearly not an option. The CVD graphene can be transferred onto any substrate and integrated into standard complementary metal-oxide-semiconductor (CMOS) processes, which is crucial for the commercial realisation of graphene-based flexible electronics. Recent work has demonstrated techniques to grow single-crystal graphene domains with a lateral size of 0.3 mm in only 5 s.⁷²

In this work, the graphene was grown on copper foil using a CVD system.⁷³ The synthesis process can be described as follows:

- Pretreatment. The copper foil was pre-cleaned in acetic acid, acetone, isopropanol and deionised water to remove native oxides and organic contaminants.

- Annealing. After loading into the chamber, the copper foil was annealed at 1050 °C to optimise the surface morphology (e.g. the roughness, orientation and grain size).
- Growth. H₂ and CH₄ were introduced into the chamber to synthesise graphene on the copper foil.
- Cooling down and unloading the sample.

After growing graphene on copper foils, there must be a reliable method for transferring graphene onto PET substrates. The graphene was transferred onto PET by the bubble approach^{74,75} using the following steps:

- A PMMA layer was spin coated onto the graphene/copper. Then the PMMA/graphene/copper stack was cured at 180 °C on a hotplate for 10 min.
- An electrolytic cell was filled with a 0.2 M NaOH solution as the electrolyte. The PMMA/graphene/copper stack was used as the cathode, while a platinum foil was used as the anode. By applying a voltage source, the water reduction reaction can evolve to produce H₂. The PMMA/graphene layer was delaminated from the copper foil as a result of the formation of a large number of H₂ bubbles at the interface between the graphene and copper foil.
- To remove ionic, atomic metal and organic contaminants, the PMMA/graphene layer was rinsed in dilute SC-2 (20:1:1 H₂O/H₂O₂/HCl), SC-1 (20:1:1 H₂O/H₂O₂/NH₄OH) and deionised water.⁷⁶ Then, the graphene/PMMA was transferred onto the PET substrate, and the PMMA was removed using acetone.

4.4 Ohmic contact

To minimise the parasitic resistances in graphene devices, highly conductive ohmic contacts are necessary. In a symmetric GFET, the parasitic source and drain resistances (R_S and R_D) are equal and can be expressed as a sum of the metal-graphene ohmic resistance R_c and the access resistance,

$$R_S = R_D = R_c + R_{sh} \frac{L_a}{W}, \quad (4.1)$$

where R_{sh} is the graphene sheet resistance and L_a is the access gap between the gate and the source/drain. To decrease the parasitic resistance, one can adjust the values of L_a and W . However, in most cases, these values are limited by the fabrication process and the structure of the devices.

On the other hand, R_c can be reduced by using contact metals with high work functions. Fig. 4.3 shows values of R_S from the fitting of the transfer

characteristics of GFETs by Eq. 2.2.⁵¹ The GFETs were fabricated with ohmic contacts of Ti/Pd/Au (1 nm/ 15 nm/ 180 nm) or Ti/Au or (10 nm/ 150 nm). For monolayer graphene, metals in contact with graphene can shift the Fermi level below the electrodes in graphene. This results in the formation of an interface dipole layer due to charge transfer because of the low density of states in graphene. A consequence of this interface dipole formation is the typically observed asymmetry between the hole and electron contact resistance in graphene devices.

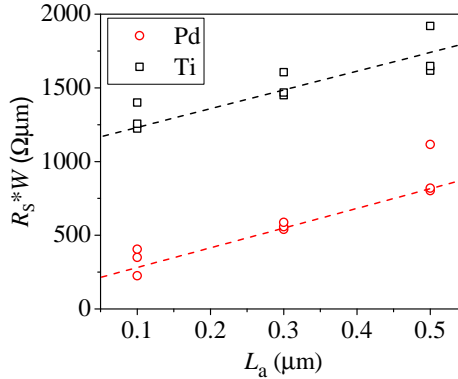


Figure 4.3: Extracted R_s with graphene-Pd and graphene-Ti contacts as a function of L_a .

4.5 Gate dielectric

To ensure the high performance of THz detectors and to reduce the leakage current, a uniform and manufacturable gate dielectric film with good electrical properties is needed. However, defect-free graphene is hydrophobic and inert, and there are no dangling bonds on its surface. Thus, it is difficult to directly deposit polar thin film gate dielectrics (e.g. Al_2O_3 , HfO_2 and SiO_2) on graphene. To solve this problem, a thin inert buffer layer or seed layer followed by atomic layer deposition (ALD) of the main dielectric film^{51,77} is widely used. However, the properties of the gate dielectric film on graphene are very sensitive to the growth conditions. Thus, techniques to characterise the electrical properties of the dielectric film on graphene are very important.

In this work, parallel-plate capacitor test structures were fabricated and characterised to evaluate the electrical properties of the dielectric film [paper B]. Fig. 4.4 (a) and (b) show the top and cross-sectional views of the test structure. The equivalent circuit of the structure based on the parallel capacitance model⁷⁸ is shown in Fig. 4.4 (c). To measure the series resistance of graphene R_s under the same conditions as the capacitance measurement, we use the same

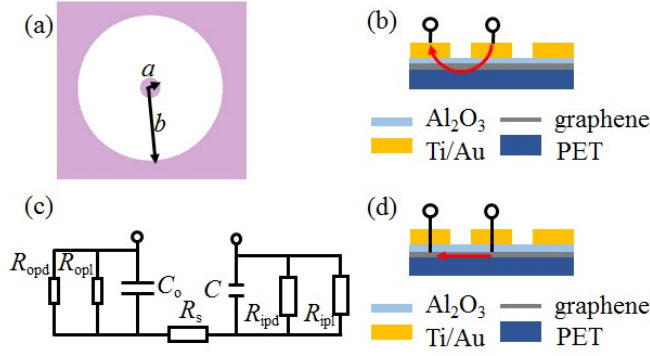


Figure 4.4: (a) Top and (b) cross sectional view of the test structure; (c) the equivalent electrical circuit of the test structure; (d) the cross sectional view of the short structure.[paper B]

probe to punch through the dielectric, as shown in Fig. 1 (d). Because the area of the outer electrode is much larger than that of the inner electrode, the capacitance of the outer capacitor (C_o) is much larger than that of inner (C). Similarly, both the parallel leakage resistance (R_{opl}) and the parallel dielectric resistance (R_{opd}) of the outer capacitor are much smaller than that of the inner. So C_o , R_{opl} and R_{opd} are negligible. R_{ipl} and R_{ipd} are the parallel leakage resistance of the inner capacitor and the parallel dielectric resistance of the inner capacitor, respectively.

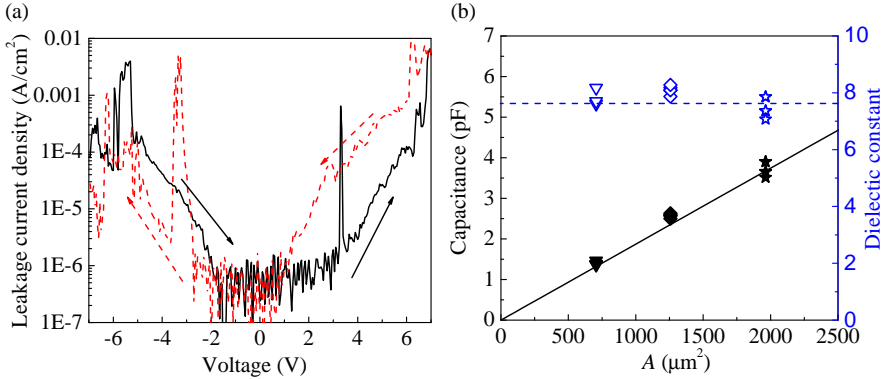


Figure 4.5: (a) Leakage current density of a test structure versus applied voltage. The arrows denote the different sweeping directions. (b) Capacitance (solid symbols, left axes) and dielectric constant (open symbols, right axes) versus area of the inner electrode. The solid line is modeled capacitance curve with $\epsilon_r = 7.6$. The dash line is $\epsilon_r = 7.6$. [Paper B]

The test structures were characterised at dc and 1 MHz frequency. As shown in Fig. 4.5 (a), the leakage current is less than $100 \mu\text{A}/\text{cm}^2$ when the gate voltage is 5 V, which is negligible compared to drain current in GFETs and photocurrent in GFET THz detectors.¹⁹ The breakdown electric field is about 5 mV/cm, which is similar to reported Al_2O_3 ALD films on silicon.⁷⁹ The measured capacitance versus area of the inner electrode is shown in Fig. 4.5 (b). The dielectric constant calculated from the measured capacitance is approximately 7.6, which is comparable with the bulk material properties. This confirms the good quality of the dielectric and allows for applying it as a gate dielectric in GFETs on plastic substrates. In addition, the results and analysis in Paper B indicate that the measured loss tangent is governed mainly by the dielectric loss in Al_2O_3 and can be associated with charged defects.

Chapter 5

Detector characterisation

This chapter provides the details of the measurements and characterisations of the GFET THz detectors. The detectors are characterised at room temperature with different bending strains, including the transfer characteristics, gate voltage tuned THz responsivity, NEP, and THz responsivity versus frequency.

5.1 DC characterisation

5.1.1 Measurement setup

To investigate the effect of the bending strain on the detector performance, the set of detectors on the PET substrate was attached to a polytetrafluoroethylene (PTFE) Teflon fixture which has a convex cylindrical surface with the cylinder axis perpendicular to the length of the bow-tie antenna, as shown in Fig. 5.1. In this configuration, the detector was located on the outer surface of the bent substrate; hence, it experienced tensile strain in the direction perpendicular to the cylinder axis and corresponding compressive strain along the cylinder axis due to the Poisson effect. The dc measurements were performed using microprobes for electrical contacts and a Keithley 2604B sourcemeter.

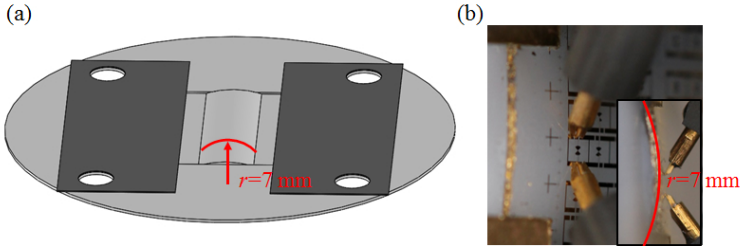


Figure 5.1: (a) Schematic of the PTFE Teflon fixture; (b) photographs of the detector under test with a bending radius of $r = 7 \text{ mm}$, which corresponds to a strain of $\varepsilon = 1.3\%$. The inset shows the corresponding side view.

5.1.2 Transfer characteristic

Fig. 5.2 shows the conductance of the detector versus the gate-source voltage with different bending strains of $\varepsilon = 0\%$, 0.9% and 1.3% . The V_{Dir} of the

detector increases with the strain, which is in qualitative agreement with the results presented in Ref. 28,29. This is attributed to changes in device electrostatics caused by changes in mobile trapped charges in the gate dielectric and at the graphene-dielectric interface as the substrate is bending.²⁸ In particular, it is shown that the trap activation energy level can be affected by the stress.⁸⁰

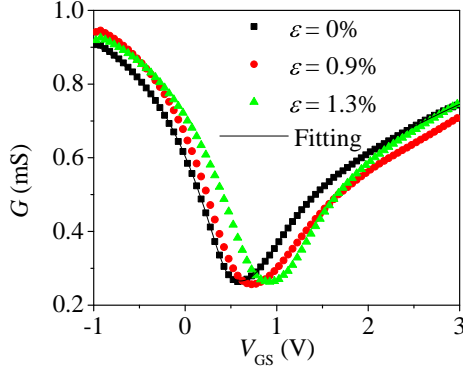


Figure 5.2: The conductance of the detector as a function of V_{GS} at $V_{DS} = 0.5$ mV with different strains of 0%, 0.9% and 1.3%. The solid line is the fitting results without strain. [Paper A]

Based on the fitting of the transfer characteristics by Eq. 2.2,⁵¹ the residual carrier density and contact resistance can be extracted from dc measurements. The average values of μ and n_0 with different strains are summarised in Table 5.1. Because the deviations of the mobility with the strain in the studied range are less than the uncertainty produced by the fitting model⁸¹, the values of mobility do not reveal a clear dependence on the strain.

Table 5.1: Extracted parameters of the detector.

Bending Radius (mm)	Strain	n_0 (cm^{-2})	μ_e (cm^2/Vs)	μ_h (cm^2/Vs)	$R_{c,e}$ (Ω)	$R_{c,h}$ (Ω)
∞	0%	6.7	2010	3000	1250	660
10	0.9%	8.0	2100	1900	1240	500
7	1.3%	7.6	2200	2000	1100	650

5.2 THz detection in a free space

5.2.1 Measurement setup

The THz source was composed of a WM-2.2 VDI's THz extender driven by an Agilent HP 83650A signal generator with 30 dB sine-wave modulation at 333 Hz. Microprobes are used for electrical contacting of detectors. The rectified voltage response was measured using an SR830 lock-in amplifier. As shown in Fig. 5.3 (a), the THz power was transmitted by a WR-2.2 horn antenna, collimated, prefocused by two identical PTFE Teflon lenses with a 75 mm focal length, and finally focused by a hyper-hemispherical high-resistivity silicon lens with a 5 mm diameter. The set of detectors on the PET substrate was attached to the PTFE Teflon fixture (as shown in Fig. 5.1) placed at the backside of the silicon lens, which was fixed at the centre of an x-y stage. Perpendicular movement of the PTFE fixture along the optical axis of the setup allowed the detector position to be adjusted with respect to the beam focus and enabled selection of the device under test among the detector set. For calibration, the total available THz power (P) was measured using an Erickson calorimetric power metre at the waveguide flange of the extender on which the horn antenna is mounted.

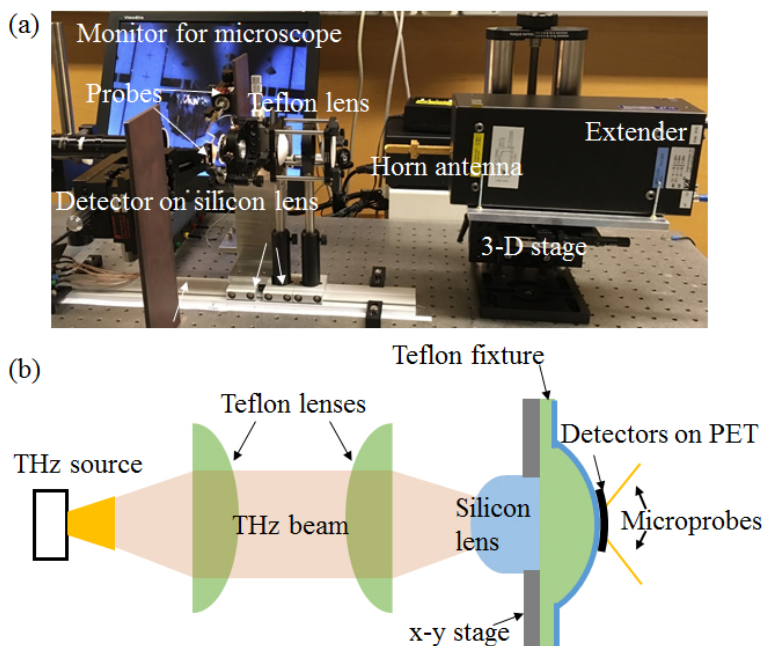


Figure 5.3: (a) Photograph and (b) schematic drawing of far-field measurement setup for THz characterisation. The figure is for reference only, not in actual scale.

5.2.2 Responsivity and NEP

Fig. 5.4 (a) shows the measured voltage responsivity versus the gate voltage at 487 GHz with different strains. The solid line in Fig. 5.5 (a) represents the simulation results at $\varepsilon = 0\%$ based on the electrical nonlinear model described in Chapter 3. As the gate voltage increases, the measured responsivity varies from negative to positive, which is consistent with the modelled responsivity. However, the amplitude of the modelled responsivity is 10 times larger than that from the measurements. This result occurs because the voltage responsivity calculated using Eq. 3.9 is underestimated, since it does not take into account power reduction factors including the power losses in the the experimental setup, limited detector antenna gain, and impedance mismatch between the antenna and transistor^{23, 82–84}.

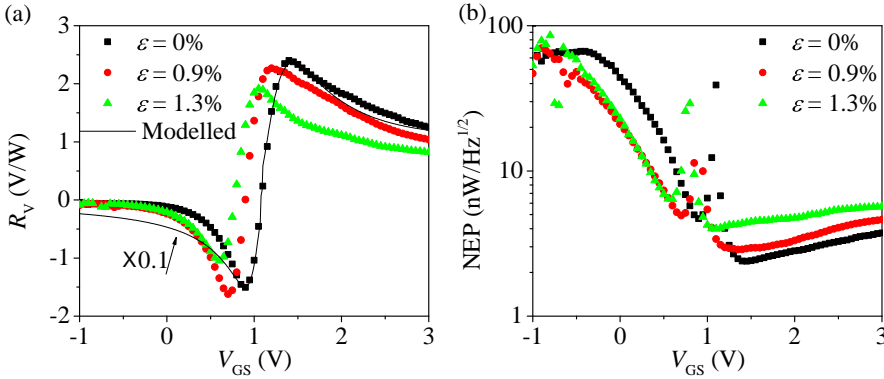


Figure 5.4: The measured voltage responsivity (a) and the estimated NEP (b) as a function of V_{GS} at 487 GHz with different strains of 0%, 0.9% and 1.3%. The solid line is the modelled results without strain. [Paper A]

Figs. 5.4 (b) shows the estimated NEP of the detector as a function of V_{GS} with different strains. The minimum NEP value without bending is less than $3 \text{ nW}/\sqrt{\text{Hz}}$ at $V_{GS} = 1.45 \text{ V}$ in the n-type gated channel. As the strain increases from 0% to 1.3%, the minimum NEP increases from $2.4 \text{ nW}/\sqrt{\text{Hz}}$ to $4 \text{ nW}/\sqrt{\text{Hz}}$, which is reversible and without permanent damage. This reflects the excellent mechanical properties of graphene. Physical models explaining effects of the bending strain on the THz detector performance are discussed in details in Paper A.

5.2.3 The frequency dependence of responsivity

Fig. 5.5 (a) and (b) show the voltage responsivity as a function of frequency at $V_{GS} = 1.4 \text{ V}$ without and with strains (0.9% and 1.3%), respectively. Because of the increase in the transmitting and detector antenna gains and better

conjugate impedance matching at the higher frequencies^{68, 82–84}, the voltage responsivity generally increases with frequency. The reproducible deviations around the average values are caused by the standing waves in the optical setup⁸². Note that the measured data do not clearly show any effects of applied strain on the antenna parameters.

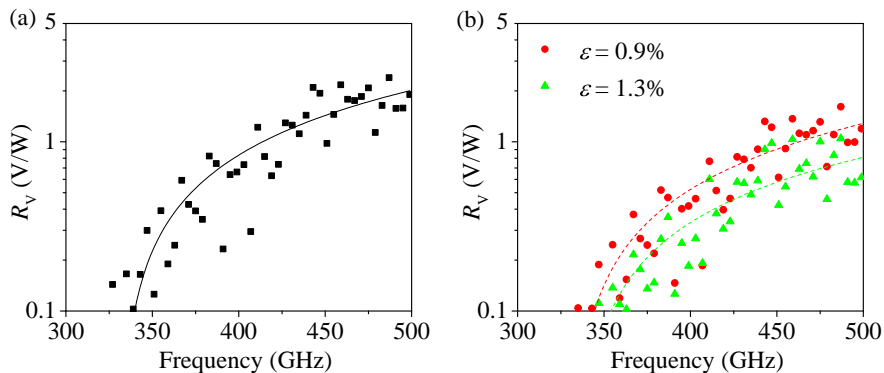


Figure 5.5: The measured voltage responsivity as a function of frequency at $V_{GS} = 1.4$ V without strain (a) and with strains of 0.9% and 1.3% (b). The lines are the fitting results. [Paper A]

Chapter 6

Conclusions and future work

6.1 Conclusions

THz radiation lying in the frequency range between infrared and microwaves can be exploited in various applications. The unique electronic properties and outstanding mechanical properties of graphene make it a promising material for future flexible THz applications. This thesis aims to develop sensitive room-temperature bendable THz detectors based on antenna-coupled GFET. Furthermore, this work provides an important route towards high-performance and low-cost THz flexible technology. The following results and conclusions are obtained:

- The electrical nonlinear circuit model for GFET THz detection is discussed and analysed. The model indicates that the V_{GS} -dependent response is proportional to the field-effect factor dG_{DS}/dV_{GS} , which is consistent with the measurement results.
- The fabrication process of THz detectors on plastic substrates has been developed. Moreover, parallel-plate capacitor test structures on graphene on flexible substrates are fabricated for characterising the electrical properties of the gate dielectric films.
- A high-efficiency asymmetric split bow-tie antenna is designed and simulated. The antenna is placed on a hyperhemispherical silicon lens to improve the directivity.
- Broadband GFET THz detectors on plastic substrates have been designed, fabricated, and characterised. The THz responses with different strains and different frequencies have been measured at room temperature. The underestimated voltage responsivity reaches 2 V/W , and the estimated NEP is less than $3 \text{ nW}/\sqrt{\text{Hz}}$. The responsivity only has a small reduction with increasing strain, which demonstrates the robustness of the detector.

6.2 Future work

The future work is to distinguish and separate the contributions of different mechanisms to the THz response in the graphene field-effect detection, including accurate de-embedding of external circuit elements and detailed investigation

of the GFET performance and characteristics over a wide frequency range. Furthermore, the future work will focus on the optimisation of the THz detectors and can be divided into 4 parts.

- One-dimensional electrical contact. Three-dimensional metal electrodes can be connected to the two-dimensional graphene layer along the one-dimensional graphene edge for carrier injection to reduce the contact resistance and increase the response.
- Hexagonal boron nitride (h-BN)/graphene/h-BN van der Waals heterostructures. There is a large density of charge traps and defects in the Al_2O_3 gate dielectric or at the interface of Al_2O_3 /graphene. In addition, the PET substrate with a high surface roughness can limit the carrier mobility by scattering charge carriers in graphene. The two-dimensional h-BN with an ultra-flat surface and free of dangling bonds and charge traps can be an ideal material for the dielectric and substrate to reduce the charge scattering and improve the carrier mobility.
- Plasmon resonant THz detection. With increasing carrier mobility, when the plasma resonance condition is met, GFETs can exhibit a sharp resonance response to the THz signal at the plasma oscillation frequencies. The responsivity of such devices may greatly exceed the responsivity of non-resonant detectors.
- Hemispherical THz electronic eye camera. Similar to the structure of biological eyes, a hemispherical THz detector array with simple imaging optics can provide a wide field of view and low aberrations, which is difficult to achieve using exiting technologies on rigid substrates.

In conclusion, this thesis shows that graphene is a promising material for future THz technology. This is an important step towards integrated low-cost wearable THz sensors, which can become an important part of IoT.

Appendix A

Recipe of GFET THz detectors on PET

The fabrication steps assume the CVD graphene is transferred onto the FET substrate.

1. Protective layer

- Evaporate 1 nm Al, oxidise at room temperature, repeat 2 times.

2. Alignment marks

- Spin coat e-beam resist MCC NANO Copolymer EL10 at 3000 rpm during 60 s for 400 nm thickness.
- Soft bake in oven at 110 °C for 10 min.
- Spin coat e-beam resist AR-P 6200.13 diluted 1:2 in anisole at 3000 rpm during 60 s for 95 nm thickness.
- Soft bake in oven at 110 °C for 10 min.
- Evaporate 20 nm Cr.
- E-beam expose pattern proximity corrected using BEAMER at 100 kV/ 10 nA with a dose of 295 $\mu\text{C}/\text{cm}^2$.
- Remove Cr by chromium etchant diluted 1:2 in deionized water, then rinse off with deionized water, blow-dry by N_2 .
- Develop AR-P for 45 s in n-Amylacetate, blow-dry by N_2 .
- Develop copolymer for 2 min in MIBK:IPA 1:1, blow-dry by N_2 .
- Etch Al_2O_3 by buffered oxide etch for 10 s, rinse off with deionized water.
- Etch graphene by oxygen plasma at 50 W RF power and 50 mTorr pressure for 10 s.
- Evaporate 1 nm Ti/ 50 nm Au.
- Lift-off in acetone for 1 h at room temperature, rinse by IPA and deionized water, N_2 blow dry.

3. Mesa isolation

- Spin coat the negative e-beam resist maN 2401 at 3000 rpm during 60 s for 100 nm thickness.
- Soft bake in oven at 110 °C for 3 min.

- Spin coat Espacer 300Z at 1500 rpm during 60 s for 100 nm thickness.
- Soft bake in oven at 110 °C for 3 min.
- E-beam expose pattern proximity corrected using BEAMER at 100 kV/ 2 nA with a dose of 285 $\mu\text{C}/\text{cm}^2$.
- Remove Espacer with deionized water, then rinse off with deionized water.
- Develop for 30 s in MF-CD-26, rinse by deionized water, blow-dry by N_2 .
- Etch Al_2O_3 by buffered oxide etch for 10 s, rinse off with deionized water.
- Etch graphene by oxygen plasma at 50 W RF power/ 50 mTorr pressure for 10 s.
- Strip resist in acetone for 1 h at room temperature , rinse by IPA and deionized water, blow-dry by N_2 .

4. Ohmic contact

- Spin coat e-beam resist MCC NANO Copolymer EL10 at 3000 rpm during 60 s for 400 nm thickness.
- Soft bake in oven at 110 °C for 10 min.
- Spin coat AR-P 6200.13 resist diluted 1:2 in anisole at 3000 rpm during 60 s for 95 nm thickness.
- Soft bake in oven at 110 °C for 10 min.
- Evaporate 20 nm Cr.
- E-beam expose pattern proximity corrected using BEAMER at 100 kV/ 10 nA with a dose of 295 $\mu\text{C}/\text{cm}^2$.
- Remove Cr by chromium etchant diluted 1:2 in deionized water, then rinse off with deionized water, blow-dry by N_2 .
- Develop AR-P for 45 s in n-Amylacetate, blow-dry by N_2 .
- Develop copolymer for 2 min in MIBK:IPA 1:1, blow-dry by N_2 .
- Etch Al_2O_3 by buffered oxide etch for 10 s, rinse off with deionized water.
- Evaporate 1 nm Ti/ 5 nm Pd/ 100 nm Au.
- Lift-off in acetone for 1 h at room temperature, rinse by IPA and deionized water, blow-dry by N_2 .

5. Gate dielectric and electrodes

- Spin coat e-beam resist MCC NANO Copolymer EL10 at 3000 rpm during 60 s for 400 nm thickness.

- Soft bake in oven at 110 °C for 10 min.
- Spin coat AR-P 6200.13 resist diluted 1:2 in anisole at 3000 rpm during 60 s for 95 nm thickness.
- Soft bake in oven at 110 °C for 10 min.
- Evaporate 20 nm Cr.
- E-beam expose pattern proximity corrected using BEAMER at 100 kV/ 10 nA with a dose of 295 $\mu\text{C}/\text{cm}^2$.
- Remove Cr by chromium etchant diluted 1:2 in deionized water, then rinse off with deionized water, blow-dry by N_2 .
- Develop AR-P for 45 s in n-Amylacetate, blow-dry by N_2 .
- Develop copolymer for 2 min in MIBK:IPA 1:1, blow-dry by N_2 .
- Evaporate 1 nm Al, oxidise at room temperature, repeat 4 times.
- Evaporate 1 nm Ti/ 150 nm Al/ 2 nm Ti/ 150 nm Au.
- Lift-off in acetone for 1 h at room temperature, rinse by IPA and deionized water, blow-dry by N_2 .

Summary of appended papers

Paper A

A flexible graphene terahertz detector

We present the first flexible THz detector based on a CVD graphene field-effect transistor fabricated on a plastic substrate. We have investigated the effects of bending strain on DC characteristics, voltage responsivity and NEP of the detector, and the results reveal its robust performance.

My contributions: Designed, fabricated and characterised the devices, and analysed the results and wrote the paper.

Paper B

Characterization of Al_2O_3 gate dielectric for graphene electronics on flexible Substrates

Here, we have fabricated and characterised parallel-plate capacitor test structures consisting of 35 nm thick Al Al_2O_3 dielectric film and with graphene as bottom electrode on polyethylene terephthalate (PET).

My contributions: Designed, fabricated and characterised the devices, and analysed the results and wrote the paper.

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