

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

**CARBON BASED MATERIALS SYNTHESIS AND
CHARACTERIZATION FOR 3D INTEGRATED
ELECTRONICS**

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Carbon Based Materials synthesis and characterization for 3D Integrated Electronics
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Abstract

3D IC packaging technology extends Moore's law and shifts the IC field into a new generation of smaller, but more powerful devices. Interconnection and thermal management as two critical parts of 3D IC integration packaging, are facing harsh challenges due to the miniaturization of IC devices. This thesis focuses on improving the heat dissipation effect and interconnect performance for 3D IC integration packaging by developing carbon based nanomaterials.

Thermal management has been identified by the semiconductor industry as one of the major technological bottlenecks to hinder the further miniaturization of 3D IC devices, particularly in high power devices. The first part of thesis presents a comprehensive thermal management solution including nanocomposite thermal interface material (Nano-TIM), hexagonal boron nitride (hBN) heat spreader and graphene-CNT (G-CNT) hybrid heatsink to address heat issue existing in high power IC devices. To decrease the thermal interface resistance, a smart Nano-TIM is developed through combining a silver-coated nanofiber network and an indium matrix. The matrix contributes to the heat conduction, while the nanofiber network defines the geometry and improves the mechanical performance. The thermal and mechanical performance of Nano-TIM is demonstrated in die attach applications in IC packaging. In addition to improve thermal interface resistance by Nano-TIM, an hBN heat spreader was synthesized by liquid exfoliation method to spread and dilute the heat energy generated in power chip for further cooling. This spreader potentially broadened the heat spreader application scenario in IC packaging due to its insulating performance. Moreover, in order to dissipate heat energy from IC microsystem, a 3D carbon based heat sink consisted of CNTs and graphene was synthesized using CVD method. The carbon based heat sink combining 1D CNTs with 2D graphene extended the excellent thermal property to three dimensions through covalent bonding.

In the second part of thesis, it is devoted to the development of CNT-based through silicon vias (TSVs) for interconnects in 3D IC packaging. Vertically aligned carbon nanotubes (VA-CNTs) with different structures were synthesized by the thermal chemical vapor deposition (TCVD) method. In order to address the incompatibility with IC manufacturing processes and relatively lower electrical conductivity than metal, a series of processes including tape assisted transfer, filling solder balls into hollow structures and electroplating Cu into CNTs bundles were developed. Accordingly, different types of CNT-based TSVs were fabricated: densified VA-CNT TSV, VA-CNT-Solder TSV and VA-CNT-Cu TSV. The electrical conductivity performance of the TSVs was measured using the four-probe method. Among these different kinds of TSVs, VA-CNT-Cu TSV exhibits the best conductivity, around the same order of magnitude as copper. Meanwhile, the CTE of this kind of TSV is as low as that of silicon substrate, which can effectively decrease thermal stress of the interface between via and substrate. In addition, to broaden the TSV application scenario, a flexible CNT interconnect system was integrated to demonstrate potential carbon based application in future wearable microelectronics.

In addition, CNT-G material was developed for carbon based supercapacitors application, thanks to the huge surface area and high electrical conductivity of the CNT-G hybrid material. The results indicate a superior rate capability of the CNT-G material. This carbon hybrid material exhibited a great promise for supercapacitor applications particularly in high current density.

In summary, integrating the Nano-TIM, heat spreader and G-CNT heatsink together offered a comprehensive thermal management solution for 3D IC microsystem using carbon based materials. Carbon based TSV technology further shortens interconnection path and enhanced 3D IC integration. To some extent, these findings offer a potential solution for the further miniaturization of 3D IC microsystem.

Keywords: TIM, VA-CNTs, VA-CNT-Cu, VA-CNT-Solder, TSV, G-CNT, 3D IC integration, thermal resistance, electrical resistivity, graphene.

To My family, especially Ting

List of appended papers

Paper A

Mechanical and thermal characterization of a novel nanocomposite thermal interface material for electronic packaging

Shuangxi Sun, Si Chen, Xin Luo, Yifeng Fu, Lilei Ye, Johan Liu

Microelectronic Reliability, published online 4th November 2015. DOI: 10.1016/j.microrel.2015.10.028

Paper B

Tape-assisted transfer of carbon nanotube bundles for through-silicon-via applications

Wei Mu, Shuangxi Sun, Di Jiang, Yifeng Fu, Michael Edwards, Yong Zhang, Kjell Jeppson, Johan Liu

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Paper C

A Flexible and Stackable 3D Interconnect System using Growth-Engineered Carbon Nanotube Scaffolds

Di Jiang, Shuangxi Sun, M. Edwards, K. Jeppson, Nan Wang, Yifeng Fu, Johan Liu

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Paper D

A vertically-aligned CNT-Cu nanocomposite material for through-silicon-via interconnects

Shuangxi Sun, Wei Mu, Michael Edwards, Davide Mencarelli, Luca Pierantoni, Yifeng Fu, Kjell Jeppson, Johan Liu

Nanotechnology, vol. 27, no. 33, p. 335705, 2016

Paper E

Cooling hot spots by hexagonal boron nitride heat spreaders

Shuangxi Sun, Jie Bao, Wei Mu, Yong Zhang, Yifeng Fu, Lilei Ye, Johan Liu

The Proceeding - Electronic Components and Technology Conference, 2015, vol. 2015–July, pp. 1658–1663.

Paper F

Controllable and fast synthesis of bilayer graphene by chemical vapor deposition on copper foil using a cold wall reactor

Wei Mu, Yifeng Fu, Shuangxi Sun, Michael Edwards, Lilei Ye, Kjell Jeppson, Johan Liu

Chem. Eng. J., vol. 304, pp. 106–114, Nov. 2016.

Paper G

Covalent bonding improved thermal transport at CNT-graphene interface

Shuangxi Sun, K. Majid Samani, Yifeng Fu, Tao Xu, Lilei Ye, Maulik Satwara, Kjell Jeppson, Torbjörn Nilsson, Litao Sun, Johan Liu

Under review by ACS Appl. Mater. Interface, May. 2017.

Paper H

A seamless CNT and graphene hybrid supercapacitor

Shuangxi Sun, Qi Li (Equal first author), Yifeng Fu, Per Lundgren, Peng Su, Peter Enoksson, Johan Liu

In Manuscript, 2017.

Other contributions that are not included in the discussion due to being out of the scope of this thesis

- 1 O. Cometto, Majid K. Samani, Bo Liu, Shuangxi Sun, Siu Hon Tsang, Johan Liu, Kun Zhao, Edwin H.T. Teo, "Control of Nanoplane Orientation in voBN for High Thermal Anisotropy in a Dielectric Thin Film: A New Solution for Thermal Hotspot Mitigation in Electronics," *ACS Appl. Mater. Interfaces*, vol. 9, no. 8, pp. 7456–7464, Mar. 2017.
- 2 J. Daon, S. Sun, D. Jiang, G. Cibien, E. Leveugle, C. Galindo, A. Ziaei, L. Ye, Y. Fu, J. Bai, and J. Liu, "Electrically conductive thermal interface materials based on vertically aligned carbon nanotubes mats," in *2014 20th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014, pp. 1–4.
- 3 J. Daon, S. Sun, D. Jiang, E. Leveugle, C. Galindo, S. Jus, A. Ziaei, L. Ye, Y. Fu, J. Liu, and J. Bai, "Chemically enhanced carbon nanotubes based Thermal Interface Materials," *presented at the THERMINIC 2015 - 21th International Workshop on Thermal Investigations of ICs and Systems, Proceedings, 2015*.
- 4 K Jeppson, J Bao, S Huang, Y Zhang, S Sun, Y Fu, J Liu, "Hotspot test structures for evaluating carbon nanotube microfin coolers and graphene-like heat spreaders," presented at the IEEE International Conference on Microelectronic Test Structures, 2016, vol. 2016–May, pp. 32–36.
- 5 Yong Zhang, Shirong Huang, Nan Wang, Jie Bao, Shuangxi Sun, Michael Edwards, Xuan Fu, Wang Yue, Xiuzhen Lu, Yan Zhang, Zhichao Yuan, Haoxue Han, Sebastian Volz, Yifeng Fu, Lilei Ye, Kjell Jeppson, Johan Liu, "2D heat dissipation materials for microelectronics cooling applications," presented at the China Semiconductor Technology International Conference, CSTIC, 2016.
- 6 Di Jiang, Shuangxi Sun, Wei Mu, Yifeng Fu, Johan Liu "Carbon nanotube/solder hybrid structure for interconnect applications," presented at the Proceedings of the 5th Electronics System-Integration Technology Conference, ESTC 2014, 2014.
- 7 Y. Fu, W. Mu, S. Sun, N. Wang, S. Huang, and J. Liu, "Post-growth processing of carbon nanotubes for interconnect applications - a review," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, 2016, pp. 1–6.
- 8 Dongsheng Zhang, Jiawen Liu, Shuangxi Sun, Shirong Huang, Jie Bao, Ning Wang, Johan Liu, Xiuzhen Lu, "Thermal properties of TIM using CNTs forest in electronics packaging," presented at the 2016 17th International Conference on Electronic Packaging Technology, ICEPT 2016, 2016, pp. 1355–1359.
- 9 Wei Mu, Josef Hansson, Shuangxi Sun, Michael Edwards, Yifeng Fu, Kjell Jeppson, Johan Liu "Double-Densified Vertically Aligned Carbon Nanotube Bundles for Application in 3D Integration High Aspect Ratio TSV Interconnects," presented at the Proceedings - Electronic Components and Technology Conference, 2016, vol. 2016–August, pp. 211–216.

Abbreviations

CNT	Carbon nanotube
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
DRIE	Deep reactive ion etching
EDX	Energy dispersive X-ray spectroscopy
ENIG	Electroless nickel immersion gold
G-CNT	Graphene and CNT hybrid structure
hBN	Hexagonal boron nitride
IC	Integrated circuit
IHS	Integrated heat spreader
Nano-TIM	Nanocomposite thermal interface material
SEM	Scanning electron microscope
TCR	Thermal coefficient of resistance
TCVD	Thermal chemical vapor deposition
TIM	Thermal interface material
TSV	Through silicon via
VA-CNT	Vertical aligned carbon nanotube
3D	Three dimensional

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Chapter 1

1. Introduction

1.1 Background

Over the past few decades, the rate of progress in the semiconductor industry has roughly followed Moore's law, determined by Gordon Moore in 1965 [1]. Dating back over the past 30 years, the quantity of transistors has dramatically increased from thousands to billions in just a single microchip. This is why a desktop computer a decade ago has the same or even less functions than a current smart phone. However, the amount of energy consumer by mobile phone is much smaller than a computer. More importantly, this kind of high-integrated microchip has brought digital electronics including cellphone, iPad, Kindle and Tablet into our life, totally changing our daily lifestyle. Fig. 1.1 shows that increased integration degree in technology has brought human from desktop internet era to mobile internet era (MonolithIC 3D Inc. Report). This is due to both academia and industry keeping up with Moore's law and the ability of semiconductor manufacturer to advance technology.

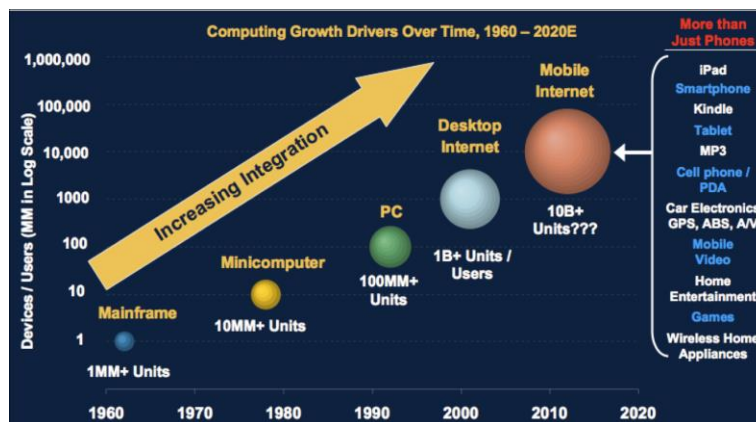


Fig. 1.1. The development trend of digital electronics devices from 1960 to 2020.

However, over the past five years the performance of microchip has been fallen behind the exponential growth that Moore predicted. International Technology Roadmap for Semiconductor (ITRS) reported that the pace of advancement and the miniaturization trend of manufacturing size has slowed down since reaching 14 nm in 2013, as shown in Fig 1.2. Gordon Moore himself also foresaw that the rate of progress of semiconductor development would eventually reach saturation [2]. The reasons for falling behind Moore's law are mainly from two aspects, which are the fundamental limit and engineering manufacture limit respectively. For the fundamental limit, if the microprocessors feature size decreases to 4 nm, as is

scheduled to occur in around 2020, then transistor performance will be substantially affected by quantum tunneling [3]. For the engineering limit, there are obstacles in the integrated circuit (IC) manufacturing process, where accuracy at the 4 nm scale is a huge challenge. In order for Moore's law to continue, the semiconductor industry has invested many efforts in IC packaging. In order to integrate so many transistors in the microchip, IC manufacturer invented three-dimensional IC (3D IC) concept to continue the trend of faster and smaller IC products.

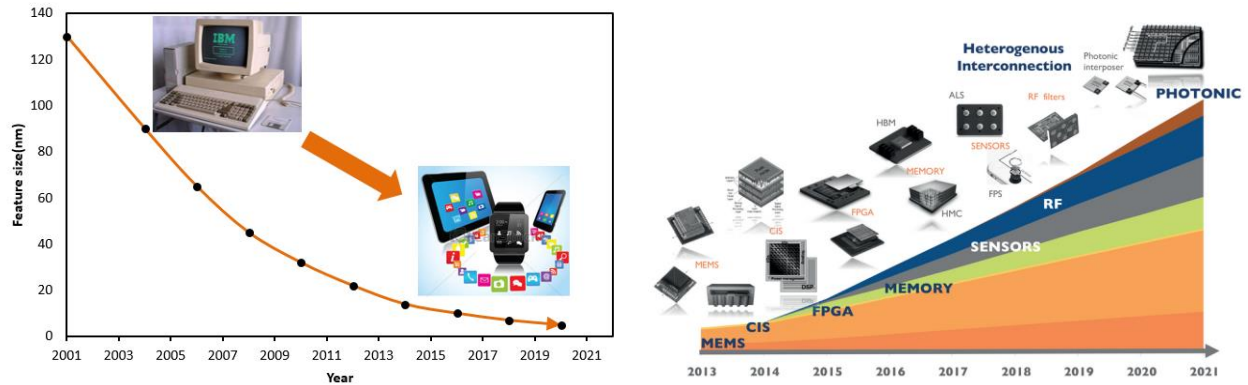


Fig. 1.2. Left diagram shows the decrease in feature size with respect to time [4]; Right diagram describes the 3D IC market distribution from 2013 to 2021.

3D IC is an integrated circuit manufactured by stacking silicon wafers and/or dies and interconnecting them vertically using through-silicon via (TSVs) so that they behave as a single device to achieve performance improvements at reduced power and smaller footprint than conventional two dimensional processes [5]. As shown in Fig 1.2, 3D IC packaging technology is becoming more and more important in the future microelectronics field. The market for 3D IC technology is expanding at a 22% compound annual growth rate. The growth is mainly driven by increased adoption of 3D IC devices in more and more fields including 3D memories with high performance computing, RF field, sensor filed like finger print sensor and photonic devices with high-end graphics. However, generally speaking, every new technology emerging in the market always brings some new issues in this field. The 3D IC packaging is not an exception. Because 3D IC packaging realizing higher density IC devices, thermal issue will be one of big challenges to manage to keep the devices working under an acceptable temperature. Another key technology to realize communication between chips in 3D IC is the TSV technology. High performance and smaller size interconnect is extremely important in the very limited silicon area. In this thesis, we mainly focus on improving heat dissipation and the performance of interconnects in 3D IC packaging to address these two challenges in developing this new IC packaging technology, as shown in Fig. 1.3.

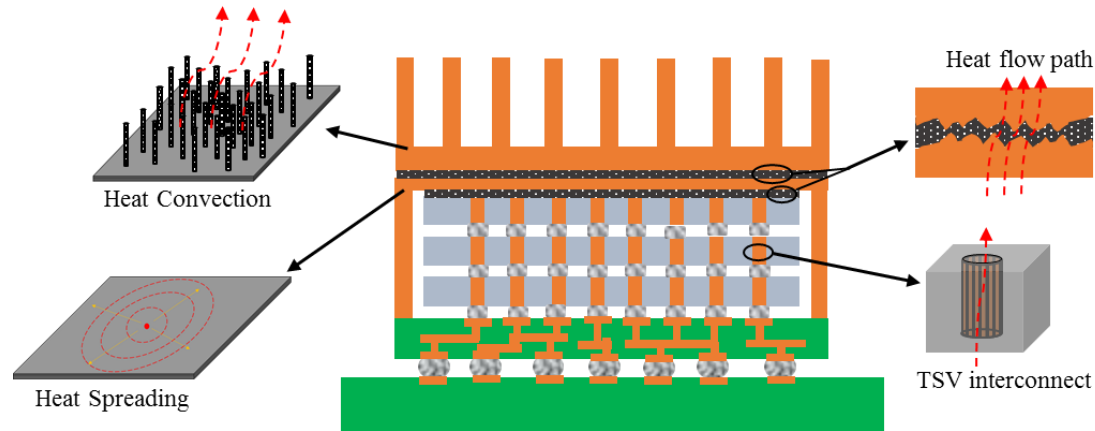


Fig. 1.3. The scheme of a typical 3D IC integration packaging.

1.11 Thermal Management in 3D IC packaging

The trend of microelectronics system is towards to smaller size, higher integration density and more functionality [6]. A billion of transistors and CMOS cells are designed on centimeter sized chips [7]. Therefore, large amount of thermal energy will be generated in a limited space when a chip with billions of cells is in operation. For instance, the laser devices and systems which are used as power sources for fiber communication can generate heat flux up to 1000 W/cm^2 in less than 0.5 mm^2 area. LED devices also lead to high heat intensity between 300 and 600 W/cm^2 due to the high power loading in a small area. Moreover, if the power cannot be distributed uniformly on the chip, hot spots will be formed in a certain area of the chip, where tremendous power densities can be reached during the operation of the devices [8], [9]. Hot spots can be formed easier when the chip thickness is decreased [10]. Unfortunately, the hot spot will cause many problems in electronic devices, including fractures of circuits, delamination, melting, creep, corrosion, electro-migration and even combustion of packaging materials [11]. In other words, high temperature leads to the overheating of specific areas in electronic devices, which lowers the performance, and reliability of the devices. Therefore, it is of strategic importance that heat dissipation is well managed and controlled. In fact, poor thermal management solution is restricting the growth and further development of electronics systems according to the report of the industry consortia iNEMI and ITRS [12],[13]. Particularly in higher power electronics, the chips are often stacked or connected in parallel in a multichip module. As 3D IC chip solutions are incorporated into more and more applications, the urgent demand for efficient thermal management will push the fast development of heat dissipation technologies including using new material like carbon based material.

The methodologies of thermal management for 3D IC packaging can be categorized into passive cooling and active cooling. For active cooling methodologies, there are several approaches including using fans, thermal exchangers, low power loading and integrating thermoelectric material on the microchip for cooling

[14]. In contrast, passive methodologies strongly rely on material performance such as the heat sink material, heat spreader material and thermal interface material (TIM). In this thesis, we mainly focus on passive cooling material application in 3D IC packaging.

1.12 Interconnect in 3D IC packaging

As previously mentioned, 3D IC technology is one of the main driving forces for the continuous down scaling of the IC devices [15] [16]. There are many interconnection technologies such as wire bonding, edge connect and capacitive or inductive coupling method to fabricate 3D-IC devices [17][18]. However, the most key technology for enabling 3D-IC package is through-silicon via (TSV) technology which acts as paths for signal exchange and power delivery between the stacked chips [19][20]. TSV technology has allowed great progress in reducing signal delay, enhancing the IC integration and decreasing the overall packaging volume [21]. Thus, the development of this technology is accelerating the miniaturization of 3D-IC devices as well as integration of I/O systems.

The filling materials used in the silicon via determine the key performance of TSVs. There are various materials that have been used for the TSV, such as tungsten (W) [22], copper (Cu) [23], and a Ag/polypyrrole composites [24]. The copper is the most commonly used filling material for TSV due to its excellent electrical conductivity and low process costs. However, the main limiting factor for Cu-TSV technology is the large difference in the coefficient of thermal expansion (CTE) between Cu and Si, which results in mechanical stress in the TSV and the surrounding Si [25]. In addition, the electro-migration and skin effects also limit the application of Cu TSV in high frequency application [26]. Moreover, it is currently not technologically possible to use Cu for high aspect ratio via structures [27]. However, CNT is the other potential filling material for TSV to address the problems encountered by Cu, since Carbon Nanotubes (CNTs) have very low thermal expansion coefficients [28], joule heating [29] and do not fail at high current densities due to electro-migration [30]. More importantly, CNTs can achieve high aspect ratios needed to continue 3D IC device miniaturization trends [31]. In addition, CNT bundles also exhibited excellent flexibility performance, which can be able to use in flexible electronics for interconnect [32]. Thus in this thesis, we will work on CNT based TSV to replace metal for 3D IC interconnect.

1.13 Supercapacitors

Over the past ten years, the market of portable electronic devices and electric vehicles is expanding in a high speed. Consequently, energy storage devices with high energy density and high power density are becoming urgent demand. Although Li-ion batteries have exhibited a good energy performance in many electronic devices [33]–[37], the power performance is still not sufficient for many related applications due to the inherent limitation of Li-ion battery [38], [39]. It usually takes a long time to discharge and recharge, which seriously affects their ability to deliver power. However, supercapacitors are now attracting a lot of

attention due to the fact that most researchers believe that supercapacitors will be a critical enabling technology for much stricter application like the internet of things device. Actually the supercapacitors indeed can offer quite a lot of unique performances like pulse power supply, long cyclic life, combination of high power and high energy. In this thesis, a carbon hybrid material in supercapacitor application will be presented.

1.2 Scope and Outline

This thesis addresses integration of carbon-based material into 3D IC microsystem to meet current challenges of interconnect technology and thermal management. In this thesis, a few integration processes were developed for the realization of carbon-based material for interconnect and heat dissipation application. These include growth, densification, transfer, electroplating and integration of carbon based materials. These basic processes were also combined with 3D IC packaging process for applications as: (1) thermal management solution including thermal interface material, micro heat sink and heat spreader; (2) through silicon via for interconnect; (3) carbon hybrid supercapacitors.

Chapter 2 mainly introduces the basics of carbon materials such as carbon nanotube and graphene. The structure and properties of carbon materials was simply reviewed, particularly in heat dissipation and interconnect field. Additionally, the potential application in 3D IC microsystem was briefed in this section. Chapter 3 presents the results on the fabrication, characterization and heat dissipation effect of thermal management material, which included thermal interface material, micro heat sink and heat spreader. Firstly, a novel nanocomposite thermal interface material (Nano-TIM) based on metallic indium in a silver-coated nanofiber network was developed and characterized in the first section. For dissipating heat energy into ambient air from IC chip, a micro heat sink was fabricated using CNT and graphene hybrid material for heat dissipation application in the IC chip level. In the third section, we focused on addressing the hot spot issue existing in the IC chip by developing the hexagonal boron nitride (hBN) heat spreader that was fabricated using liquid phase exfoliation method.

Chapter 4 is devoted to the development of CNT based material for TSV interconnection in IC packaging. In the first section, synthesis processes such as the densification and transfer process used for CNTs are illustrated. In order to improve the TSV performance, densified CNTs TSV, CNT-Solder TSV and CNT-Cu TSV are each developed, evaluated and demonstrated in the 3D IC stacked chip microsystem. Due to the flexibility of CNTs, the flexible CNT-metal TSV was also demonstrated in the flexible and stretchable electronics devices.

In chapter 5, we developed a controllably aligned CNTs and graphene-based film hybrid structure to use as supercapacitors electrode. This pillared CNT-G hybrid material was synthesized using chemical vapor

deposition. The atomic structure of covalently bond was characterized by high-resolution transmission electron microscopy (TEM). The performance of this CNT-G hybrid supercapacitor was investigated. Chapter 6 concludes the thesis and gives a brief outlook.

Chapter 2

2. Carbon Materials

Nanostructured carbon materials have attracted more and more attentions due to their excellent performance in many fields such as high thermal conductivity, excellent electrical conductivity, flexible mechanical performance, high current carrying capability etc [40]–[42]. Due to various allotropes, nanostructured carbon material is a big family that comprise zero-, one-, two-, and three-dimensional materials such as fullerene, carbon nanotubes (CNT), graphene, diamond and porous carbon respectively. In this chapter, we focus on studying carbon nanotubes and graphene basic properties and their potential applications in the microelectronics.

2.1 Carbon Nanotube

Carbon nanotubes (CNT) were first discovered in 1991 by Iijima [43], which opened up a new era in materials science. Simply speaking, CNT can be considered as a long hollow tube with the walls consisted of one-atom-thick carbon layer, called monolayer graphene now. CNT can be categorized by the wall number like single-walled CNT rolled by single layer of graphene. Multi-walled CNT is rolled up by multi-layer graphene. In addition, CNT can be classified into different types by the way of graphene rolling, which can be represented by a pair of indices (n, m). Based on the combination of n and m , the CNT can be categorized zigzag, armchair and chiral CNT. From the perspective of CNT property, nanotubes can also divide into metallic CNT and semiconducting CNT. The specific structures of different type of carbon nanotubes are illustrated in Fig. 2.1. The electrical, thermal and mechanical properties of the CNT, considering its use as an interconnect and thermal management material, are discussed as follows.

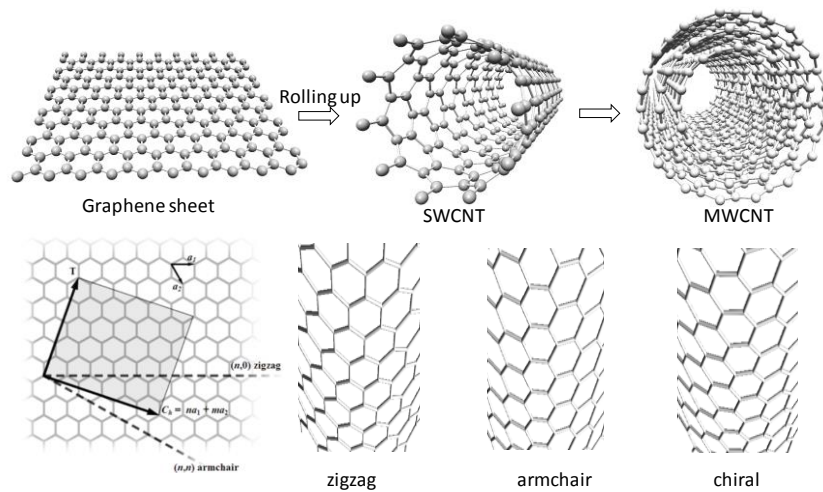


Fig. 2.1. The different structure of CNTs

Electrical performance

The electrical properties of SWCNTs are strongly dependent on the chirality (n, m) and the diameter of nanotubes [44]. If the chirality (n, m) can satisfy $n - m = 3i$, where i is an integer, this CNT will be the metallic nanotubes where the electrons can transport in the metallic way. Otherwise, the CNTs will exhibit semiconductor behavior with a band gap which is roughly inversely proportional to the tube size [40], [45], [46]. Based on the statistical results in mass scale growth, the metallic CNTs can occupy one third of all produced CNTs, while two thirds are semi-conductive. For single-walled CNTs, the electrical resistivity of individual CNTs can be as low as $10^{-6} \Omega \cdot \text{cm}$ due to ballistic conductions [47], [48]. As to multiwall CNTs, the electrical resistivity can reach to $3 \times 10^{-5} \Omega \cdot \text{cm}$ [49], [50]. Moreover, if the length of a conductive CNT is shorter than its electron mean free path, a quantum effect will be behaved [51]. In addition, CNTs also have a very strong capability to carry high current density as high as 10^9 A/cm^2 [49], [52], which is three orders of magnitude higher than that of copper. Additionally, CNTs also are with very low-level joule heating effect and less susceptible to electro-migration [29], [30].

Thermal performance

Carbon nanotube like graphene is an excellent thermal conductor material due to its unique structure. Thermal transport in CNT is mainly conducted by the intrinsic properties of the strong sp^2 lattice, rather than by phonon scattering on boundaries or by disorder, giving rise to extremely high K values [53]–[56]. According to previous theoretical results, the thermal conductivity of CNTs can be ranged from ~ 3000 to $\sim 6600 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ using different simulation method [57]–[59]. Meanwhile, many experimental data were also reported in the past ten years. Commonly quoted values for individual CNT are $\sim 3000 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ for MWCNT [53] and $\sim 3500 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ for SWCNT [54] at room temperature. However, it has to be noted that crystallographic defects strongly influence the final thermal transport capability of CNTs. Particularly in large-scale defects as stone wales defects, it leads to strong phonon scattering and gets a big reduction of thermal conductivity in consequence [60]. Table 2.1 shows the specific thermal performance of CNTs measured by different methods in the past years.

Table 2.1: The thermal conductivity of carbon nanotubes

Sample	K ($\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$)	Method	Comments	Refs
MWCNT	>3,000	Electrical; micro-heater	Individual; diffusive; suspended	[53]
SWCNT	~3,500	Electrical self-heating	Individual; boundary	[54]
SWCNT	1,750–5,800	Thermocouples	Bundles; diffusive	[61]
SWCNT	3,000–7,000	Electrical; micro-heater	Individual; ballistic; suspended	[62]
CNT	1,100	Electrical; micro-heater	Individual; suspended	[63]
CNT	1,500–2,900	Electrical	Individual	[64]
CNT	~6,600	Theory: molecular dynamics	$K_{\text{CNT}} < K_{\text{G}}$	[57]
CNT	~3,000	Theory: molecular dynamics	Strong defect dependence	[65]
SWCNT	~2,500	Theory: Boltzmann transport equation	$K_{\text{CNT}} < K_{\text{G}}$	[58]
SWCNT	~7,000	Theory: molecular dynamics and Boltzmann transport equation	$L > 20 \text{ nm}$	[59]

Mechanical performance

It is well known that CNT is the strongest material yet discovered in the world, due to the strong covalent sp^2 bonds between the carbon atoms. A lot of measurement methods such as atomic force microscope (AFM) [66], electromechanical resonant vibrations [67] and observations in transmission electron microscope [68], were developed to measure the Young's modulus and mechanical strength. Most of results claimed that the Young's modulus of CNTs could be able to reach to TPa level ranged from 0.41 TPa to 4.15 TPa. Normally speaking, the mechanically strength of CVD-CNT is usually lower than arc-CNT, which is possibly because of more defects introduced during CVD growth [66], [69]. In addition, coefficient of thermal expansion of CNT is close to zero, which can largely reduce thermal stress occurred at the interface between CNT and silicon ($2.6 \times 10^{-6} \text{ K}^{-1}$) in the IC application compared to copper ($16 \times 10^{-6} \text{ K}^{-1}$) and aluminum ($23.6 \times 10^{-6} \text{ K}^{-1}$). Moreover, the CNT is also very flexible and resilient, indicating intrinsic advantage in wearable and flexible electronics application[32], [70].

2.2 Graphene

In this section, some basics of graphene material is introduced. Regarding graphene application in the microelectronics system, monolayer graphene, bilayer graphene and graphene based film are mostly investigated by worldwide researchers due to their respective unique performance. The Fig 2.2 showed the schematic structures of graphene material.

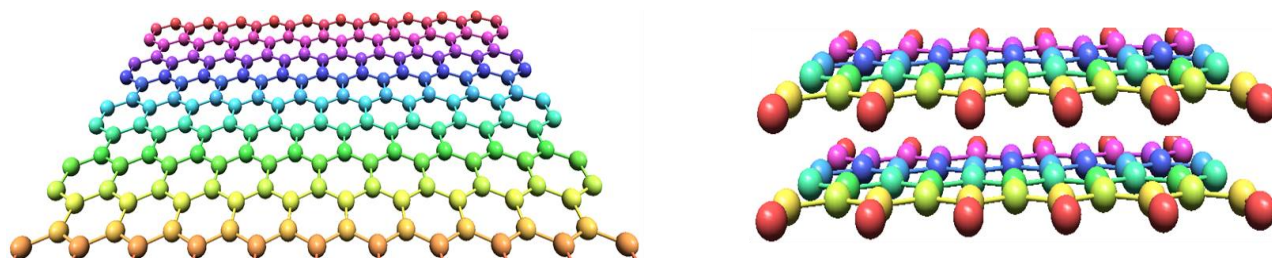


Fig 2.2: Schematic structures of graphene and bilayer graphene.

Monolayer graphene

Graphene is a two-dimensional material consisting of a single layer of sp^2 -hybridized carbon atoms arranged in a hexagonal structure [41]. It is the first 2D atomic crystal material known by human. Many extreme properties combined on this just one-atom thin graphene. Its room-temperature electron mobility can reach to $2.5 \times 10^5 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ [71], which already attracts a lot of transistor research work using graphene [72]–[76]. Graphene also exhibits excellent mechanical properties such as a Young's modulus of 1 TPa [77], the intrinsic strength of 130 GPa [77] and flexural rigidity of $3.18 \text{ GPa} \cdot \text{nm}^3$ [78]. Moreover, super high thermal conductivity (above $3000 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$) were experimentally measured through different methods by researchers [79]. This extreme thermal property triggered many graphene thermal applications in the high power IC field [80]–[82]. In addition, the optical absorption of the graphene is just $\sim 2.3\%$ over the visible spectrum [83], which combined with its high electrical conductivity [84], could result in transparent conductive electrodes applications [85]–[87].

Bilayer graphene

Bilayer graphene is basically a kind of material consisting of two layers of graphene. Commonly, bilayer graphene is categorized into AB-stacked structure and AA-stacked structure. AB-stacked bilayer graphene means that half of atoms lie directly over the center of a hexagonal of the lower graphene layer and another half of atoms locate over an atom from below layer [88]. Other type is AA-stacked structure where the two layers are exactly aligned each other [89]. For AB-stacked bilayer graphene, the band structure is very interesting. Its band gap is zero just like monolayer graphene when it is pristine form. But the non-zero band gap can be induced by electrical-displacement field [90], [91]. This unique property could be potentially used to develop nanoelectronics devices such as field-effect transistor-based switches and pseudo-spintronics [92].

Graphene Based Film

Graphene based film (GBF) is a film, which consists of a few graphene layers by stacking together in order, as shown in Fig. 2.3. Graphene based film is usually obtained from graphene oxide (GO) film through high temperature reduction [87], [93]–[95] or chemically reduction [96]–[98]. As to GO film, the GO dispersion can be prepared using Hummer's method [99] and then be infiltrated by vacuum to get the film [100]. Graphene based film exhibits outstanding properties as monolayer graphene, particularly in the area of thermal performance and electrical conductivity. Table 2.2 lists the recent research work on investigating thermal performance of graphene by different method. For instance, Zhang et al. [100] claimed that the thermal conductivity of GBF can reach to around $1200 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$, which is several times higher than copper and aluminum. Moreover, Chen et al. [101] reported a super high electronic conductive film ($\sim 3112 \text{ S} \cdot \text{cm}^{-1}$) through reduction of GO film by electrical current-induced annealing treatment. Besides these excellent thermal and electrical performances, more importantly it is a freestanding film with a strong mechanical performance, which means that it is much easier to be handled compared to monolayer graphene in many applications.

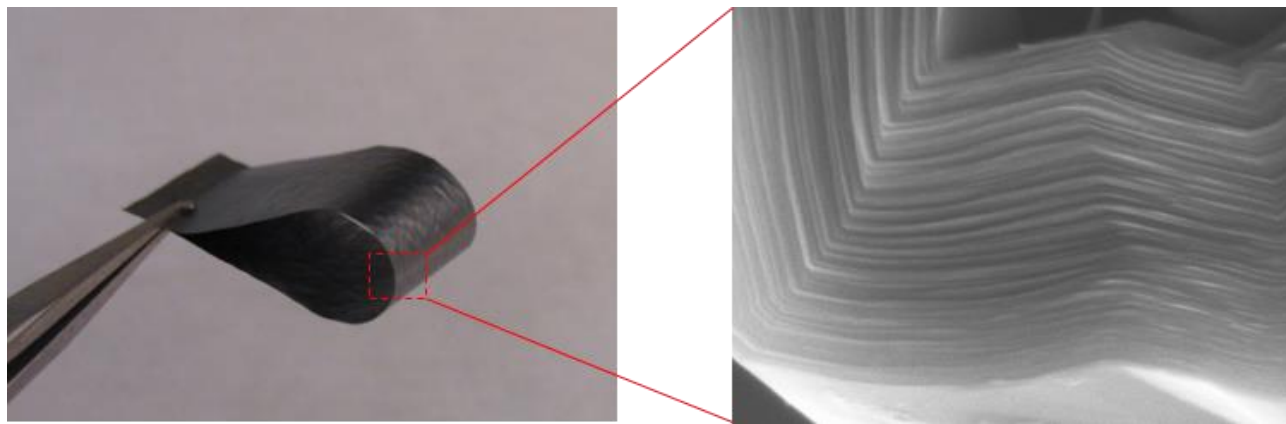


Fig 2.3: The structure of graphene based film.

Table 2.2: The thermal conductivity of graphene material.

Sample	K (W mK ⁻¹)	Method	Comments	Refs
Graphene	~2,000–5,000	Raman optothermal	Suspended; exfoliated	[56]
FLG	~1,300–2,800	Raman optothermal	Suspended; exfoliated; $n = 4-2$	[102]
Graphene	~2,500	Raman optothermal	Suspended; CVD	[103]
Graphene	1,500–5,000	Raman optothermal	Suspended; CVD	[104]
Graphene	600	Raman optothermal	Suspended; exfoliated; $T \approx 660$ K	[105]
FLG ribbon	1,100	Electrical self-heating	Supported; exfoliated; $n < 5$	[99]
Graphene	600	Electrical	Supported; exfoliated	[100]
GBF	~1200	Laser flash	Graphene film; thickness: ~30um	[100]
G paper	~1500	Electrical self-heating	Graphene paper; Ball-milling exfoliated	[101]

2.3 Applications in 3D IC packaging

Thanks to the extraordinary properties of CNT and graphene as described in previous sections, many research works are concentrated on the CNT and graphene applications, particularly in the area of thermal management and interconnect. The specific applications are introduced in the following sections.

2.3.1 Carbon material for thermal management application

Since high capability of thermal transport in CNT and graphene was demonstrated, more and more researchers are trying to use these high thermal conductive materials into 3D IC field where there is urgent requirement on heat dissipation. A comprehensive thermal management solution using passive cooling method for IC packaging includes thermal interface material, heat spreader and heat sink. Due to graphene's high in-plane thermal conductivity and fantastic 2D structure, graphene and graphene based films have been widely investigated for using as heat spreader [80]–[82], [108]–[112]. Balandin et al. presented that thermal management of GaN transistors can be substantially improved via introduction of alternative heat dissipation channels implemented by few-layer graphene [82]. Hao et al. showed that the hot spot temperature can be lowered by ~ 28 °C through chemically bonding the graphene based film on top of thermal test chip [100]. Some simulation work also demonstrated that the graphene based film have a potential for hot spot removal and the effect of heat dissipation will be more pronounced as number of transistors increases [113]. Due to high thermal conductivity in one dimensional direction and flexibility of aligned CNTs, it is more suitable to be used as TIM for improving thermal interface resistance. Many work

have therefore been done including utilize CNTs as fillers for composite TIM [114], [115], pure vertically aligned CNTs film TIM [116], [117] and CNT-metal matrix TIM [118]. For effectively resolving the contact issue between metal surfaced and vertically aligned multiwall CNT arrays, Kaur et al. published some related work in Nature Communication where they got a sixfold reduction of thermal interface resistance by bridging the interface with short, covalently bonded organic molecules [119]. Due to large surface area ratio of CNT forest, potential CNT based heat sink application were also studied in IC heat dissipation field. For instance, Fu et al. presented that a water-assisted CNT microfin on-chip cooling solution can effectively cool down high power chip ($\sim 1000 \text{ W}\cdot\text{cm}^{-2}$) by several 10°C [120]. Huang et al. demonstrated that cooling effect of CNT based heat sink were very related to length and arrangement of CNTs [121]. In recent years, graphene-CNT hybrid structures for thermal management have recently gained much attraction [122]–[127]. Through molecular dynamics simulations (MDS) large heat dissipation capability of this hybrid materials has been theoretically verified by some researchers [27][29][30]. Thermal transition junction between the CNT and the graphene film dominate the thermal resistance of such hybrid structure materials [31][32].

2.3.2 Carbon material for interconnect application

As mentioned in the previous sections, CNT and graphene both has extreme high electrical conductivity and extreme current carrying capacity. In addition, due to their inherent nanostructure, they are able to achieve nanoscale or finer interconnect. All of their advantages for interconnect trigger many related applications in 3D IC microsystem. For instance, CNTs have been proposed as promising candidate materials to build next generation interconnects in miniaturized electronics, as both on-chip and off-chip interconnects [132]–[136]. The lower resistivity of pure CNT interconnect can be as low as $\sim 10^{-6} \Omega\cdot\text{m}$, which still does not excel that of metals such copper. In order to further reduce resistivity of CNT based interconnect, CNT-metal composite materials were developed for interconnect. Subramanian et al. [137] synthesized a novel CNT-Cu composite film using electroplating, and showed a hundredfold increase in ampacity compared with Cu. Feng et al. [138] developed a fabrication method where copper was electroplated through a tungsten seed layer onto as-grown CNTs inside a blind via to fabricate CNT-Cu TSVs. Except CNT-based interconnect applications, graphene also make many researchers interested in studying its potential interconnect in IC packaging [139]. Due to its transparency, it is also widely used as transparent conductors [42], [140]–[142]. Kin et al. demonstrated that the graphene based transparent interconnect exhibited competent performance for application in LED field [143]. Taking advantage of graphene's unique band structure, graphene based transistor also become another hot topic [74]. For example, Liao et al. claimed a self-aligned high-speed graphene transistors or circuit were successfully demonstrated in high-speed and high-frequency electronics [144].

Chapter 3

3. Carbon based material for Thermal management application in 3D IC packaging

In this chapter, we mainly focus on studying thermal management application for high power chip in 3D IC packaging. As mentioned in the previous chapter, thermal issue has already become one of the bottlenecks for miniaturization of IC devices. Thus, this chapter investigates some new high thermal conductive carbon based material for thermal management applications. As shown in Fig. 3.1, a comprehensive thermal management solution for high power IC chip will be presented in this chapter.

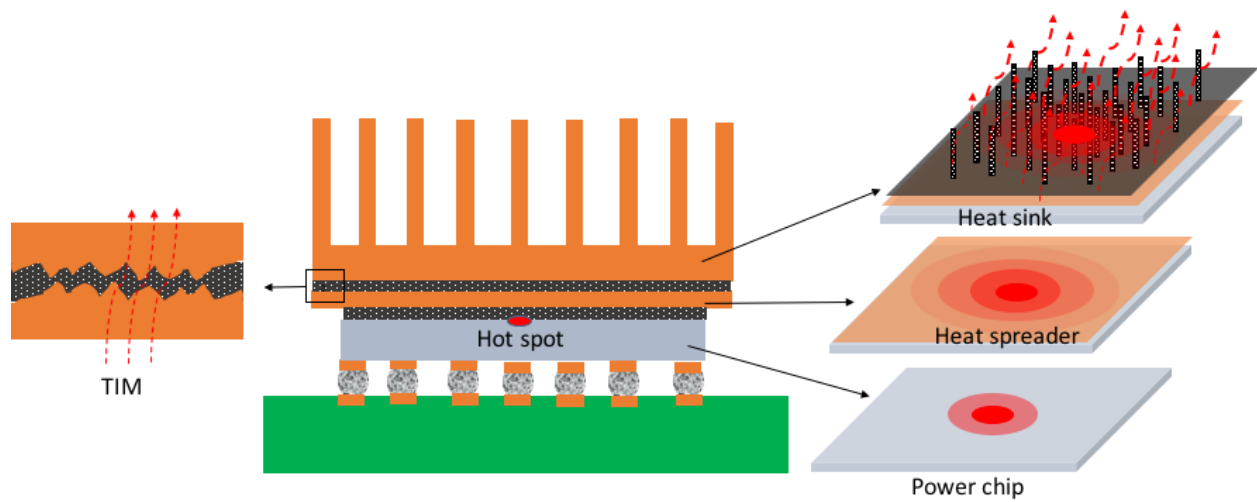


Fig. 3.1. Thermal management solution for high power chip.

3.1 A Novel nanocomposite thermal interface material (Nano-TIM) for heat dissipation

In microelectronics packaging, it is important to keep the integrated circuit junction temperature (T_j) as close as possible to the ambient temperature (T_a). Since the temperature drop ΔT from the junction temperature to the ambient can be written

$$\Delta T = R_{\text{thermal}} Q \quad (2.1)$$

where R_{thermal} is the thermal resistance and Q is the heat flux, it is important to keep the thermal resistance as low as possible. Thus, to keep the thermal resistance along the paths as small as possible is critical for the performance of an IC package. A typical layout of 3D IC package is outlined in Fig. 3.2 to illustrate the heat flow paths. For this IC packages the main heat flow path is typically from power chip to the top heat

sink. Thus, the two thermal interface materials between the circuit and the heat sink mainly limit thermal resistance from junction-to-ambient. In this thesis, a novel nanocomposite thermal interface material for efficient 3D IC packaging has been proposed and evaluated as described in the appended paper A.

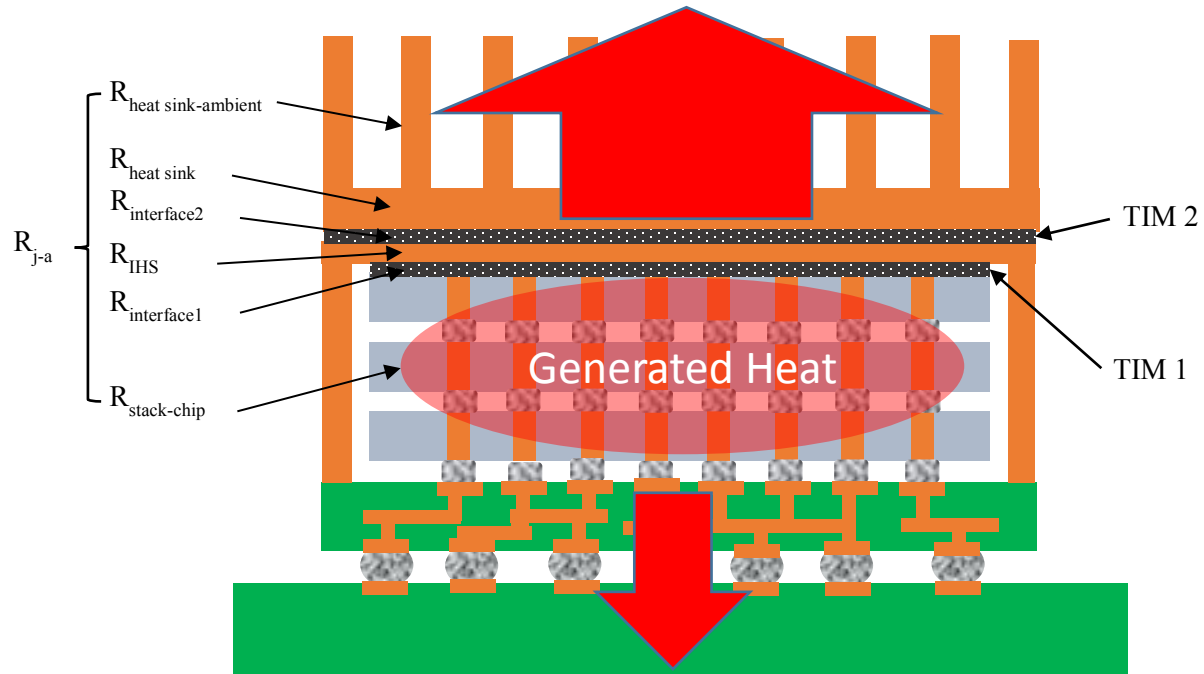


Fig. 3.2. Typical 3D IC packaging and the heat flow paths of IC device.

The main role of the thermal interface material is to fill the air voids and gaps, which inevitably arise at the interface between two surfaces due to surface roughness and the relative asperity. As can be seen in Fig. 3.3, the thermal interface resistance can be decreased considerably if the high resistance air gap is replaced by a low resistance thermal interface material.

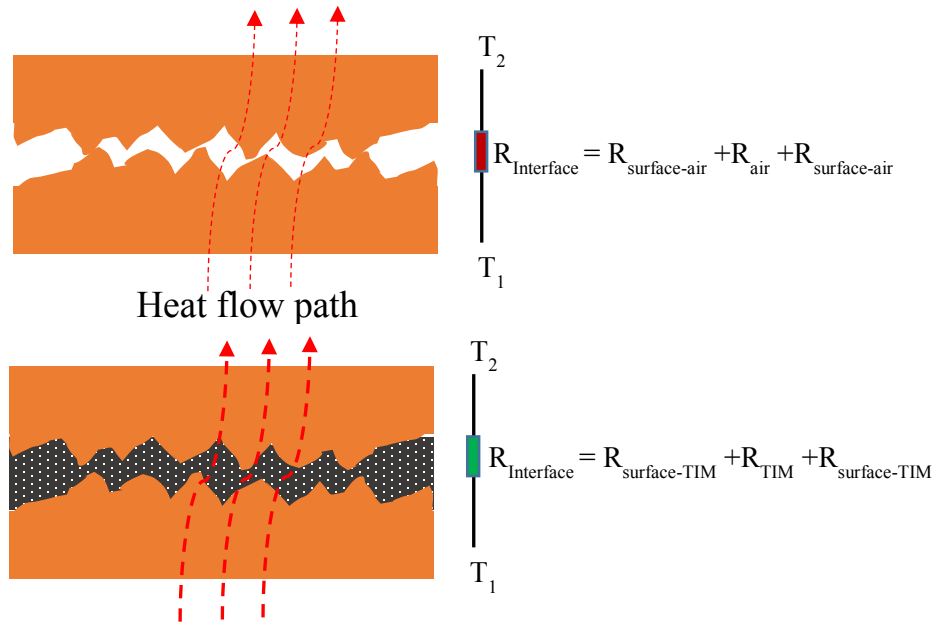


Fig. 3.3: Schematic of the thermal resistance across interface with and without TIM.

The current trends of developing new TIMs are focused on the nanocomposite materials, such as embedding carbon nanotubes [145]–[147] and silver nanowire arrays in a polymer matrix [148], due to the unique properties of nanomaterials on surface area, defects, mechanical, electrical, and thermal performance. Meanwhile, the improvement and characterization of traditional TIMs, including solder-based TIMs [149] and phase-change materials [150], are also an important topic in the thermal management field. The researchers have developed several metal based nano-fiber matrix composite TIMs for heat dissipation in the electronics packaging. Zhang et al. reported the performance of indium-tin-bismuth alloy based nano-fiber composite TIMs used as a phase-change material [151]. However, phase-change TIM material can easily be oxidized and corroded at the elevated temperature cycles [152]. Zandén et al. studied the thermal performance and reliability of tin-silver-copper based nano-polymers composite in a die attachment [153]. Murugesan et al. developed carbon fiber based tin-silver-copper alloy matrix composite TIM for thermal management of high power electronics [154]. However, this kind of solder based nanocomposite TIM has to be soldered onto the substrate at around 220 °C which possibly brings a risk of reliability of some temperature sensitive device [155].

In the novel nanocomposite thermal interface material proposed in this thesis section, we have chosen indium as the base material of the TIM to exploit the high thermal conductivity and low melting temperature of the metal [156]. However, pure indium is easily deformed due to its low yield strength and its tendency of flowing out during die attach process [157]. Addressing the weaknesses of indium, a novel

nanocomposite thermal interface material (Nano-TIM) based on metallic indium in a silver-coated polyimide (PI) network was developed. The polymer network defines the geometry of the thermal interface material, such as its shape and bond line thickness. The metallic part is responsible for heat transfer.

3.1.1 Fabrication of the Nano-TIM

The detailed processes for fabricating this Nano-TIM is described in paper A. In short, the polymer network matrix is electrospun and then infiltrated with indium after surface modification where the fibers are coated with silver. A silver-coated polyimide network and a piece of the final Nano-TIM are shown in Fig. 3.4. The detailed structures of the polyimide nanofibers network before and after surface modification by coating silver are shown in Fig. 3.5.

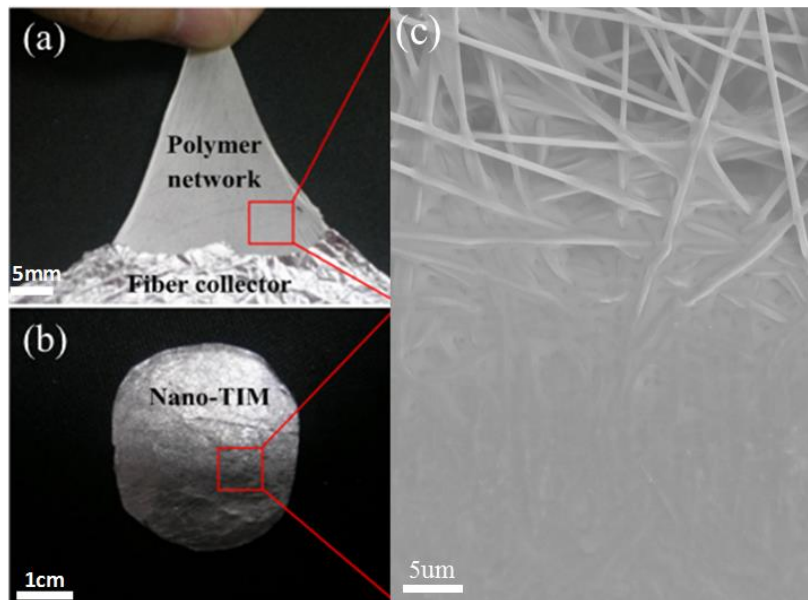


Fig. 3.4. (a) Polyimide network formed with electrospinning process; (b) a piece of Nano-TIM fabricated with infiltration process; (c) SEM image of nanofiber network after partly metal infiltration. (From Paper A)

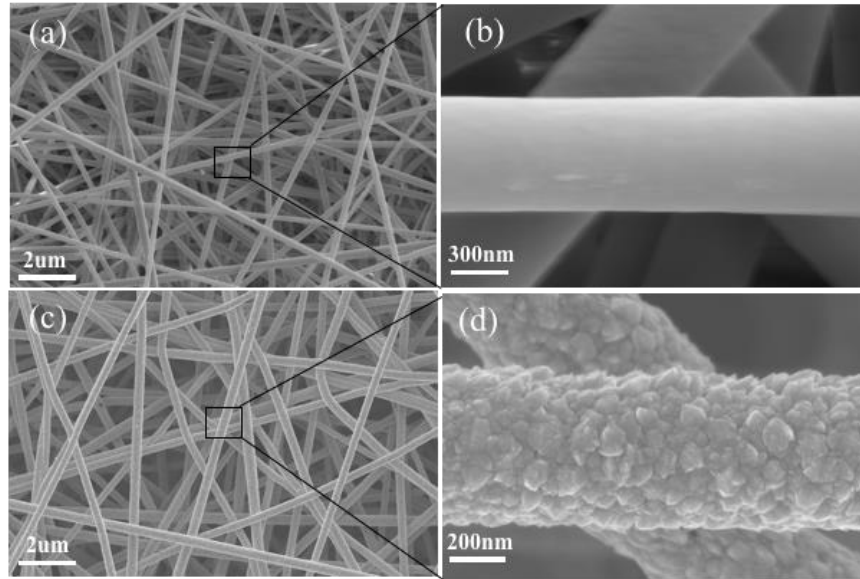


Fig. 3.5. (a) and (b) show pristine polyimide nanofibers network formed through electrospinning process; (c) and (d) show the nanofibers network with Ag nanoparticles coating after surface modification. (From paper A)

In order to study the inner structures of the Nano-TIM by scanning electron microscopy, a number of cross-section samples were prepared using a pure indium TIM sample as a reference. Pure indium at the interface between the copper pads with an electroless nickel immersion gold (ENIG) is shown in Fig. 3.6 (a). Some Si pieces are found in the indium matrix. These Si pieces come from the Si chip used during the cross-section polishing process. The Si pieces were polished off the Si chip and embedded in the soft indium. In Fig. 3.6 (b), the polymer fibers can be observed in the indium matrix. There are no visible voids that can be seen in Fig. 3.6 (b), indicating the porous polymer network has been completely filled with indium after the infiltration process. Fig. 3.6 (c) shows an image of Nano-TIM with high magnification. In Fig. 3.6 (c), each fiber is tightly covered by the indium matrix. In general, the porous fibers network is extremely difficult to be fully wetted and filled by liquid indium due to the inert nature of PI and the small gap between the fibers as shown in Fig. 3.6 (e). However, in this Nano-TIM, the surface of the fibers has been coated by silver, which significantly improves the wettability of liquid indium to the surface. For all nanofibers observed, each individual nanofiber was tightly surrounded by indium under the help of the silver particle as shown in the representative image given in Fig. 3.6 (d). As a result, the liquid indium can successfully infiltrate the fiber network by using high pressure in the infiltration process.

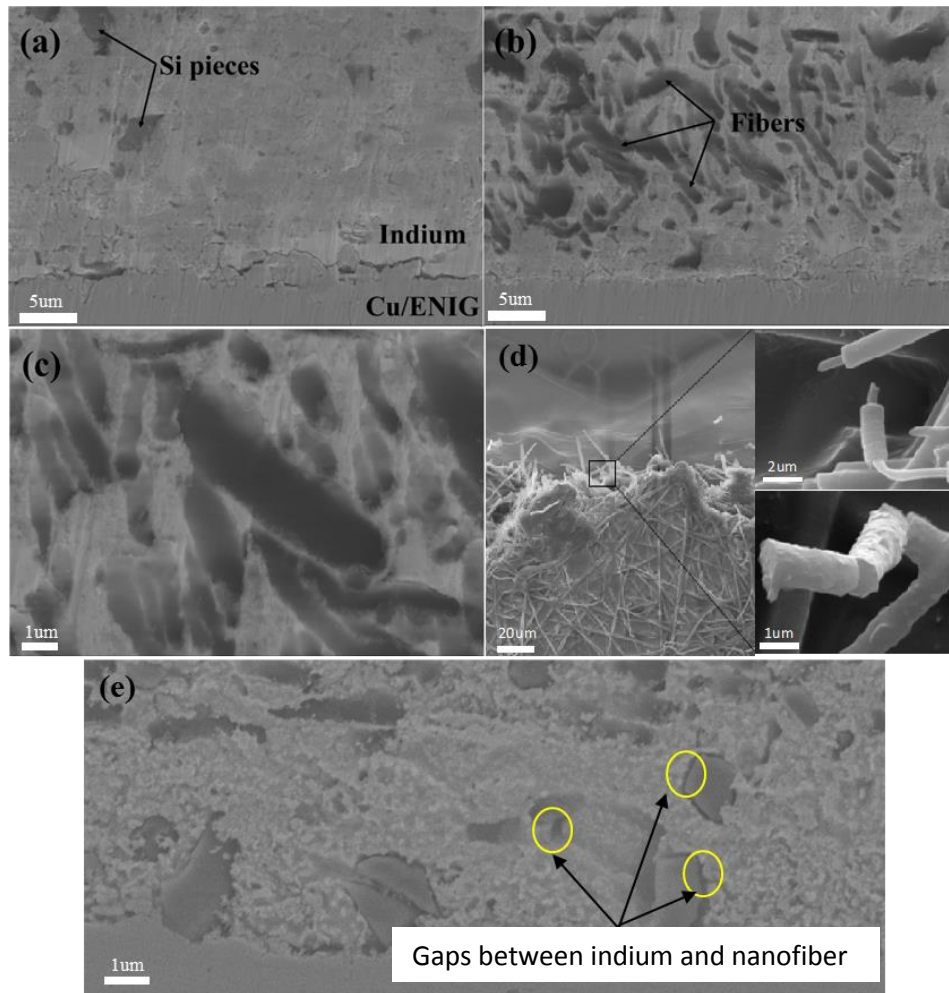


Fig. 3.6. Cross-sections of (a) pure indium and (b) Nano-TIM with Cu/ENIG pad; (c) high magnification image of the Nano-TIM; (d) shows the inner structure of Nano-TIM after damage; (e) shows the interface status between indium and the nanofiber without silver coating. (From paper A)

3.1.2 Performance evaluation of the Nano-TIM

As described in detail in paper A, the novel nanocomposite thermal interface material was evaluated by shear test, thermal resistance measurements, and thermal infrared camera tests. The schematic structures of the shear test setup and the thermal interface resistance measurements are shown in Fig. 3.7, and the results of these test are shown in Fig. 3.7 (c) and (d). These figures show the results obtained from the novel Nano-TIM in comparison to the results obtained for pure indium TIMs. The results show that the average shear strength of Nano-TIM is higher than that of pure indium, which could be attributed to the reinforcement effect of silver-coated PI fibers. For the thermal resistances, that of the novel Nano-TIM is only slightly larger

than that of a purely metallic indium TIM, 2.1 and 1.7 $\text{K} \cdot \text{mm}^2 \cdot \text{W}^{-1}$, respectively. The results indicate that the polymer network has no significant negative influence on the thermal conductivity of the Nano-TIM material.

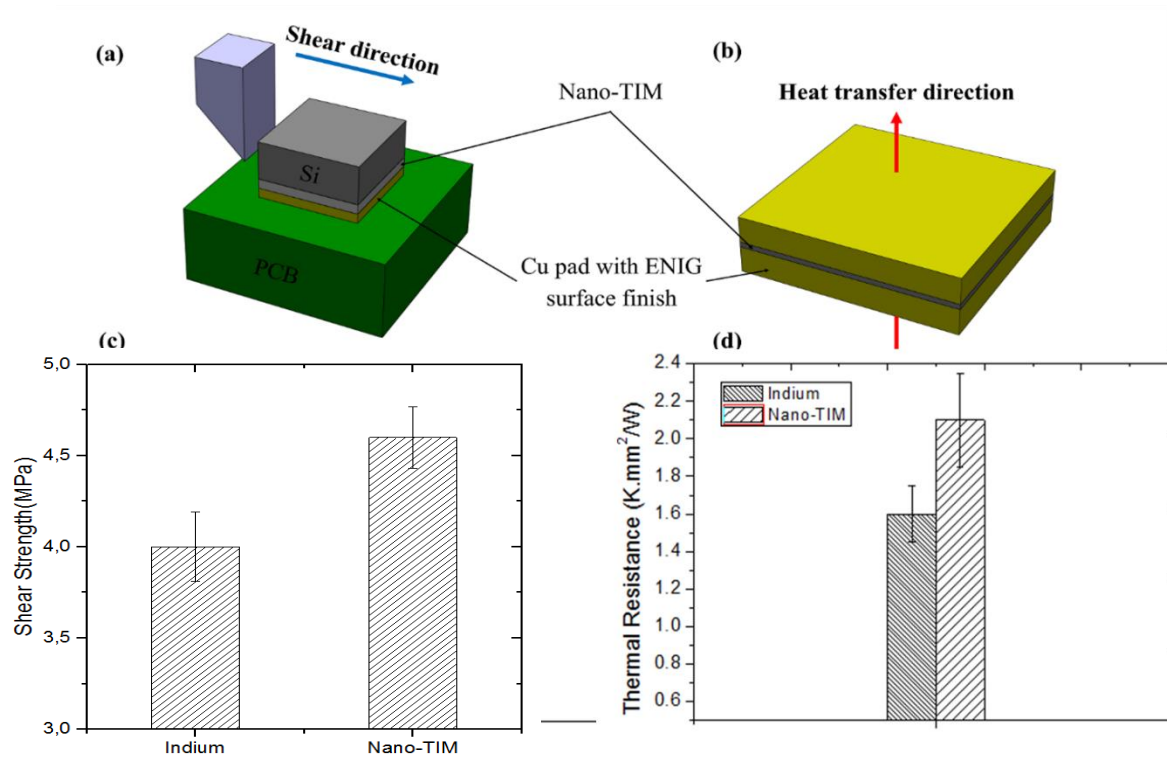


Fig. 3.7. Sample structures for (a) shear test and (b) thermal interface resistance measurement. Results of (c) shear test and (d) thermal interface resistance measurement. (From Paper A)

The dislocation motion in the Nano-TIM can be impeded by the silver-coated fibers limiting any crack initiation and propagation during the shear test and therefore increases the shear strength of the Nano-TIM compared to the pure indium TIM. To verify this hypothesis, the fracture surface after the shear test was also studied. The fracture surface of both samples shown in Fig. 3.8 are composed of dimples, but the

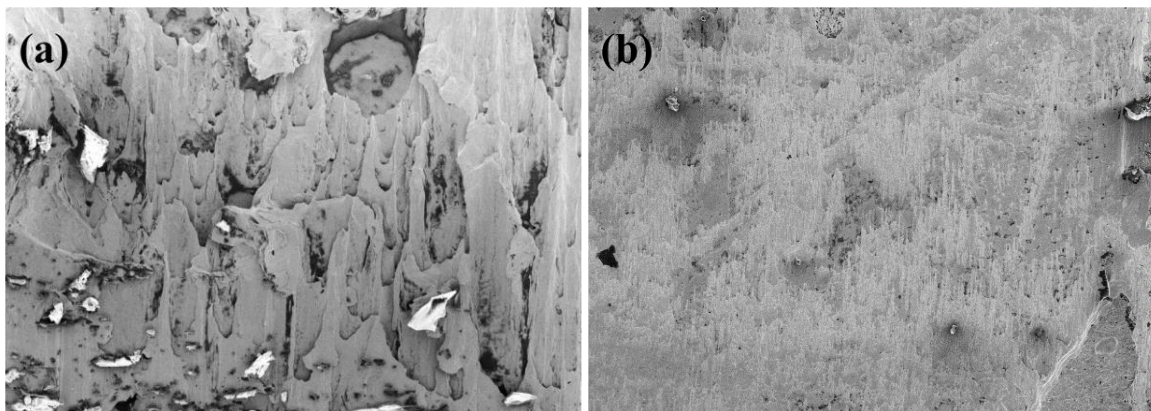


Fig. 3.8. Fracture surface of pure indium (a) and Nano-TIM (b) after shear test. (From paper A)

microstructure of the Nano-TIM is much finer than that of pure indium and with smaller dimple sizes. This fine microstructure of the fracture surfaces of Nano-TIM could be caused by the fiber network which separates the large indium matrix to small areas. This finer microstructure of fracture surface of Nano-TIM directly justified that the nanofibers do limit the crack initiation during the shear test.

The heat dissipation effect of the Nano-TIM for die attach applications was investigated by using a thermal infrared camera. The test setup is shown in Fig. 3.9 where a hot spot power chip was attached onto a copper heat sink with TIM materials by using the same process as in the shear tests. An infrared camera was used to capture the temperature profiles of the power chip with 10 W loading. The results obtained are shown in Fig. 3.10. While the sample without any thermal interface material showed a much higher hot spot temperature (30 °C), the two samples with indium and the novel Nano-TIM showed almost the same thermal behavior as captured from the temperature profiles.

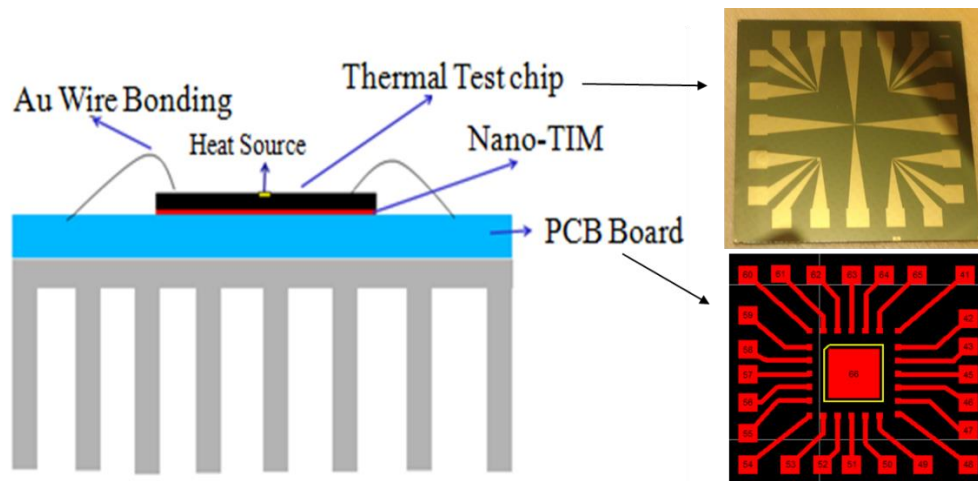


Fig. 3.9. Infrared camera setup for heat distribution analysis. (From paper A)

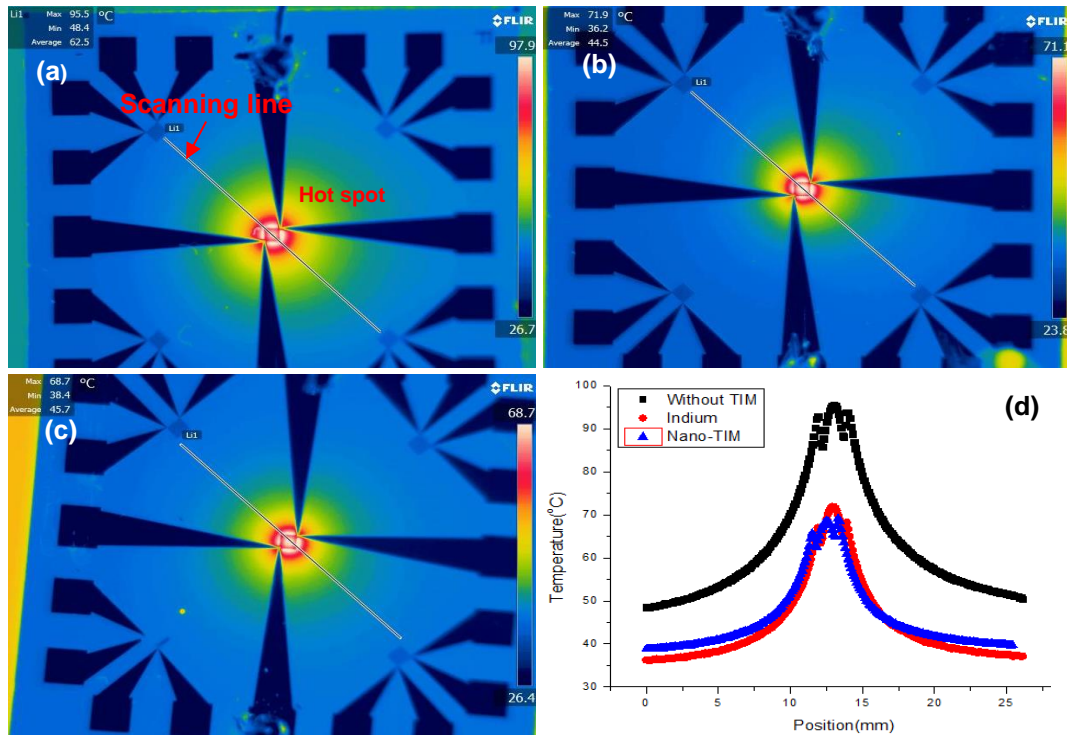


Fig. 3.10. IR test results: temperature distribution of the chip (a) without TIM, (b) with pure indium, and (c) with the Nano-TIM; (d) Temperature distribution along the line direction shown in Fig. 3.10 (a, b, c). (From Paper A)

3.1.3 Reliability test of the Nano-TIM

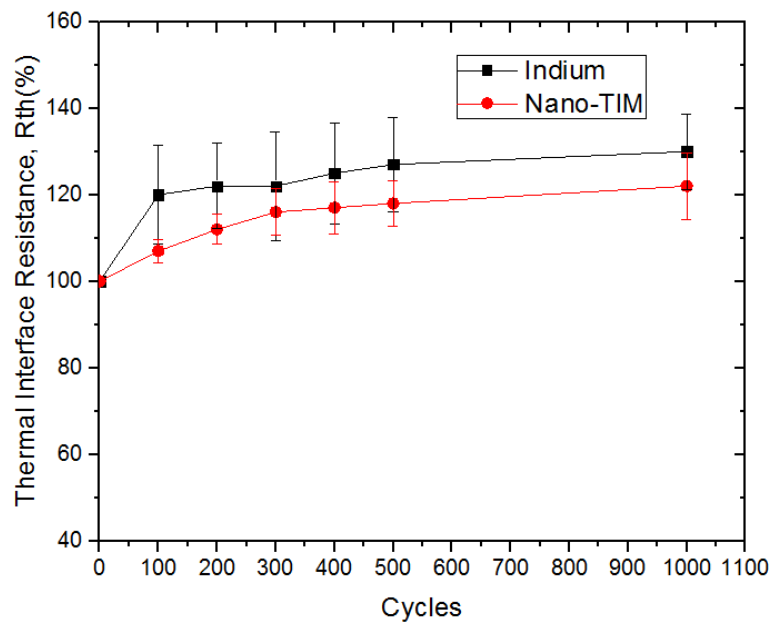


Fig. 3.11. Thermal interface resistance measurement after 100, 200, 300, 400, 500, and 1000 temperature cycles. (From paper A)

In order to evaluate the change in thermal performance and long-term reliability of the Nano-TIM, we carried out thermal cycling under harsh conditions while periodically monitoring the change in thermal resistance. The details of the thermal cycling are found in paper A, but the results after 100, 200, 300, 400, 500, and 1000 cycles are shown here in Fig. 3.11. The results presented in Fig. 3.11 gives a comparison between the pure indium TIM and the novel Nano-TIM. The thermal resistances of both materials increase with time in almost the same manner. This increase of the thermal interface resistance may be attributed to the formation of small cracks in the TIM structures caused by the harsh cycling conditions. Our conclusion is that the bonding quality of the Nano-TIM is as high as for a pure indium TIM even after 1000 cycles.

3.2 CNT-Graphene hybrid material for heat dissipation application

Carbon nanotubes (CNT) and graphene are the most representative carbon materials due to their extraordinary thermal performance [158]. The CNT high heat conductivity and graphene has made them hot subjects for research investigations in [159]–[168]. In particular, functionalized CNT arrays can effectively enhance the thermal transport at the interface between CNT and targeted surface and to some extent solve the problem of the small contact areas of individual CNT. However, this one dimensional (1D) thermal transfer cannot effectively decrease the heat density due to weak thermal conductivity and poor contact of CNT in the radial direction [169]. On the other hand, although 2D carbon materials like graphene can be able to dilute the heat density to a certain extent [170], graphene cannot provide as huge surface areas for convection as 1D CNT structures. Moreover, the cross-planar thermal conductivity of few-layer graphene is only around $0.7 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ [171]. To curb these CNT drawbacks and graphene in heat dissipation applications, covalently bonded graphene-CNT hybrid structures have recently gained much attraction [122]–[127]. However, most investigations are just theoretical predictions of the potentially large heat dissipation capability of such materials [121][122]. Through molecular dynamics simulations (MDS) it has been shown that the thermal transition junction between the CNT and the graphene film dominate the thermal performance of such hybrid structure materials [124][165]. However, experimental investigations of the heat conduction between 1D CNT and 2D graphene films are still essentially absent due to the difficulties in both fabricating the material and experimentally measuring these contact resistances. Thus, few studies have experimentally demonstrated the heat dissipation performance of this kind of hybrid structures for thermal management applications. In this section, a freestanding hybrid material was developed for thermal management applications consisting of an array of multiwall carbon nanotubes (MWCNT) covalently bonded on the graphene based film. The pillared G-MWCNT hybrid material was obtained through chemical vapor deposition to grow MWCNT on the surface of the graphene. The atomic structure of covalently bond was analyzed by transmission electron microscopy (TEM). The thermal properties of the G-MWCNT structure have been characterized by the joule heating method [173]. In

particular, the thermal junction resistance between the one-dimensional carbon nanotubes and the two-dimensional graphene was investigated through the pulsed photothermal reflectance (PPR) technique [230] [231]. Our results show that thermal junction resistance is effectively decreased when the two materials are joined with covalent bonds. In addition, we developed a thermal test chip to demonstrate the heat dissipation effect in the application.

3.2.1 Synthesis of graphene material

This section presented graphene synthesis on copper foil. In this fabrication, 50 μm thick copper foils with a purity $> 99.995\%$ (from Advent research materials Ltd) were used as the catalyst substrates for graphene growth. Prior to loading the copper foil into the CVD chamber, the trimmed copper foil was cleaned by acetone and isopropanol to remove any organic contamination, whereafter the thin oxide surface layer was removed by acetic acid for 5 minutes.

After the copper foil was suspended above the graphite heater held by an alumina frame, the bell jar was immediately pumped down to 0.1 mbar. The temperature of the graphite heater was ramped up to 800 $^{\circ}\text{C}$ at a rate of 300 $^{\circ}\text{C}/\text{min}$ in an argon or argon/hydrogen atmosphere. Hereafter, the automatic heating was stopped, and the temperature was slowly raised manually until hotspots, which indicated that the copper foil was very close to its melting point of 1060 $^{\circ}\text{C}$. Once the hotspot was visible on the surface of the copper foil, the heating power was decreased and the temperature held at around 1000 $^{\circ}\text{C}$. When the temperature stabilized, the copper foil was annealed for 5 minutes in hydrogen to completely remove any native oxide. Finally, the carbon feedstock, 5 % of methane in argon, was introduced into the chamber for initiating the growth. After completing growth, the chamber temperature was decreased to below 100 $^{\circ}\text{C}$ before the graphene film synthesized on the copper foil was taken out. A typical growth procedure with the two-step temperature ramp-up, a five minute anneal, a fifteen-minute growth, and the final chamber cool-down is shown in Fig. 3.12.

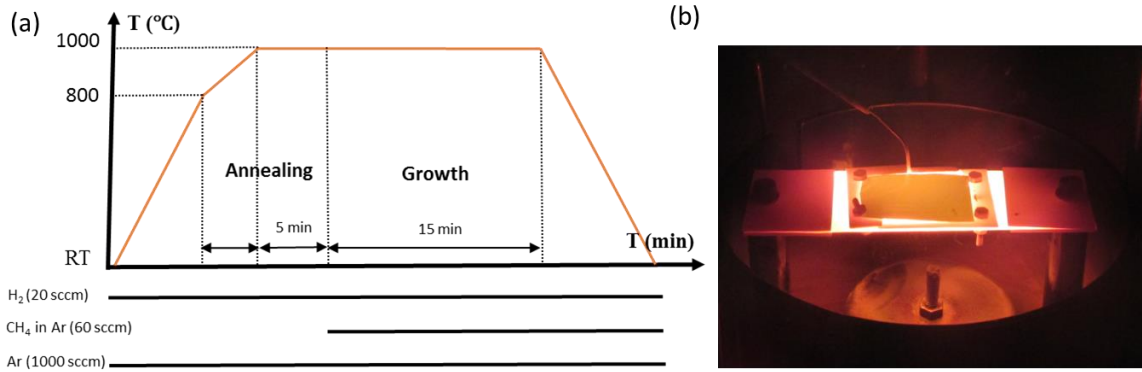


Fig. 3.12. The process flowchart for bilayer graphene growth (a) and a close-up of the experimental set-up during graphene growth on copper in the cold wall reactor (b). (From paper F)

By using a low-pressure cold-wall CVD reactor, the deposition of graphene on copper foil was found not necessarily to be a self-limiting process. The appearance of graphene adlayers is independent of the ratio between the hydrogen and methane flow rates, but rather related to the growth time. As long as the growth time was long enough, graphene adlayers always formed as shown by the top row SEM micrographs in Fig. 3.13. The difference between the process runs was the ratio between the flow rates of methane and hydrogen, and the higher the hydrogen flow rate the longer before the adlayers appear. In Fig. 3.13 (a) and (b) adlayers were already visible after two minutes, while they were not visible for the high hydrogen flow rate shown in Fig. 3.13 (c). Here, it took 50 minutes before any adlayers appeared, as shown Fig. 3.13 (d), demonstrating that a high hydrogen flow hinders growth. In order to determine the exact number of graphene layers, samples (b) and (c) were transferred onto Si/SiO₂ substrates for AFM characterization. The result of the AFM analysis of sample (b) is shown in Fig. 3.13 (e), (f) and (g), while the result of sample (c) is shown in Fig. 3.13 (h) and (i). From Fig. 3.13 (i) the height difference between first layer graphene and bare silicon dioxide surface is found to be around 0.64 nm, which confirms the existence of patches of monolayer graphene [176]. From Fig. 3.13 (f) and (g) the 0.64 nm monolayer thickness is confirmed along the blue line in figure (e), while an adlayer thickness of 0.34 nm is confirmed along the red line in Fig. 3.13 (e).

Based on the AFM analysis of the surface topography, the difference between bare copper, monolayer and bilayer graphene could be distinguished from the contrast differences on the SEM micrographs as shown on the top row of Fig. 3.13. Graphene wrinkles were also observed, and we believe they are formed during cooling due to the different thermal expansion coefficients of graphene and copper [177]. However, no wrinkles can be observed on the bare copper area, so this feature can be used to indicate whether the first graphene layer covers the entire copper surface. As shown in Fig. 3.13 (b) and (e) after two minutes of

graphene growth, some carbon clusters (indicated by red arrows) were observed. However, these clusters gradually disappeared as the growth process continued. Bointon et al. [178] claimed that, in cold-wall CVD, graphene growth is initialized from coated carbon films, and that these carbon films progressively evolve into islands, or patches, of graphene. Even though our observation of carbon clusters is consistent with the findings of Bointon et al., graphene synthesis still follows the common stages of nucleation, expansion and coalescence.

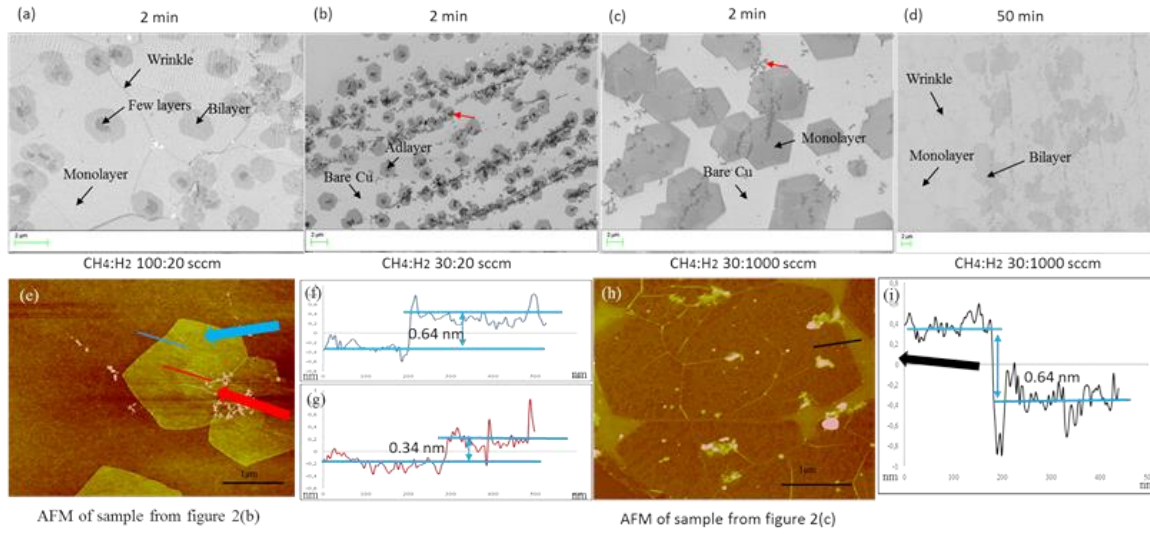


Fig. 3.13. SEM micrographs of graphene on copper foil samples (top row), (a - d), AFM height estimations across mono- and bilayer graphene edges after patches being transferred to SiO_2/Si substrates (bottom row), (e - i). (From paper F)

TEM observations and selected area electron diffraction (SEAD) examinations were further carried out to determine the thickness and evaluate the quality of as-grown graphene sample from Fig. 3.14. Folded graphene layers can be clearly observed suspended above the copper grid under low magnification as Fig. 3.14 (a) indicates. While a bilayer graphene edge can be identified from the high magnification TEM image shown in Fig. 3.14 (b), the SEAD pattern shown in Fig. 3.14 (c) reveals a set of 6-fold symmetry arrangement of carbon atoms. In addition, the intensities of outer diffraction are twice as strong as that of the inner diffraction as Fig. 3.14 (d) displays, indicating the formation of AB-stacked bilayer graphene. These observations are in line with the results of the Raman spectroscopy. It should be noted that the SEAD pattern of mis-oriented bilayer graphene was also occasionally observed, showing two sets of diffraction spots with a 28.9° rotation as Fig. 3.14 (e) shows. It also should be noted that the mis-oriented bilayer graphene with a twist angle 28.9° was the most often observed type in the measurement.

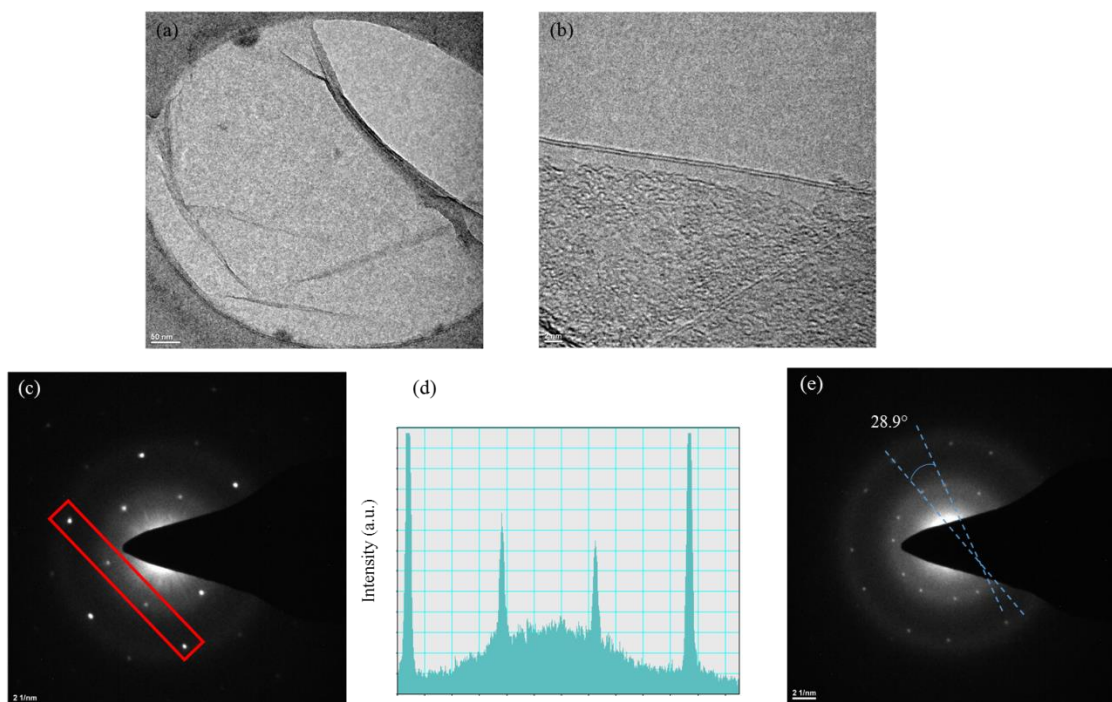


Fig. 3.14. Bright field (a) low-resolution TEM micrograph of graphene on copper grid, and (b) high-resolution TEM micrograph of bilayer graphene. (c) Typical SEAD patterns of the as-grown bilayer graphene shown in (a). (d) Intensity profiles along the selected spots in (c). (e) SEAD patterns of the mis-oriented bilayer graphene with a 28.9° rotation. (From paper F)

3.2.2 Synthesis of Graphene-CNT hybrid material

After investigating graphene growth, this section demonstrates CNT growth on the graphene by CVD method. A schematic illustration of the synthesis process of this hybrid material is shown in Fig. 3.15. The starting material obtained from the Panasonic Co. was a graphite film consisting of a number of stacked layers of graphene. The surface of this graphite film was prepared for CNT growth by deposition of a 2 nm iron film and on top of that a 3 nm thick layer of alumina (Al_2O_3) was deposited in situ by electron-beam evaporation. Here, the iron served as a catalyst for MWCNT growth while the alumina layer served to facilitate the formation of top grown MWCNT [124]. MWCNT array were synthesized on the surface of the graphene film through CVD. After loading the film the chamber was pumped down to below 0.1 mbar before an 837 sccm flow of H_2 was input. Thereafter, the substrate heater was ramped up to 500°C at a rate of $300^\circ\text{C}/\text{min}$, and when this intermediate temperature was reached the heater was maintained at this temperature for 3 minutes for reducing the catalyst [179]. The heater temperature was then rapidly increased to 720°C , while carbon feedstock acetylene at a rate of 240 sccm was introduced into the chamber for

several minutes for allowing the CNT array to grow from the surface of the G film. Since the process is a top-growth process, the iron catalyst and the 3 nm Al_2O_3 layer are separated from the surface of the film during growth ending up at the top of the MWCNT array. A plasma etch treatment was used to remove the Al_2O_3 layer because of its poor thermal conductance. After etch, a freestanding hybrid film with G-CNT covalent bond was obtained.

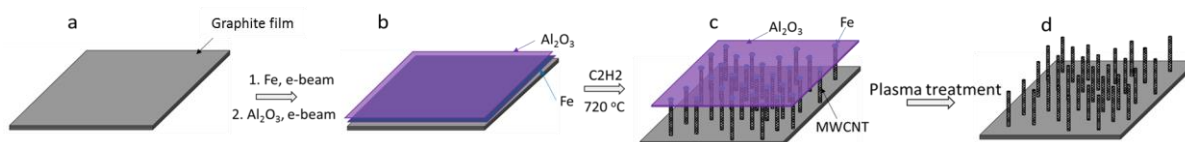


Fig. 3.15. Schematic illustration of the synthesis of the G-MWCNT hybrid material. (a) The graphite film was starting material. (b) Surface of the film covered with thin iron and alumina layers in preparation for CNT growth. (c) Growth of a vertical multiwall CNT array from the surface of the film lifting the iron and alumina layers. (d) Top alumina layer removed by plasma etch. (From paper G)

The freestanding G-MWCNT hybrid film prepared as described in Fig. 3.15 consists of an MWCNT array covering the surface of the film. The quality and structure of the MWCNT array is examined using SEM. Some of the resulting SEM images are shown in Fig. 3.16. Fig. 3.16(a) shows the flexible G film before CNT growth, while the same film after MWCNT growth is shown in Fig. 3.16(b). The color change of the top surface due to the uniform MWCNT array is clearly observed. In the SEM inset of Fig. 3.16(a) the multilayer graphene structure is visible, while in the SEM inset of Fig. 3.16(b) the vertically aligned CNT are observed. A top view of the MWCNT array is shown in the SEM image of Fig. 3.16(c). The top view shows that the MWCNT carpet was split into different islands, hundreds of micrometer in size, which is not different from normal MWCNT growth [180]. The gap between islands was formed already in the initial stage when the Al_2O_3 layer was split so that the carbon feedstock gas could reach the iron catalyst. From the heat dissipation perspective, this kind of MWCNT porous structure is preferred to enhance the thermal convection effect. Furthermore, a plasma etching treatment was introduced to remove the thin Al_2O_3 layer to further facilitate the heat convection as shown in Fig. 3.16(g). In order to check the quality of the MWCNTs and their interface between the G film and MWCNT, high-resolution SEM pictures are captured, as shown in Fig. 3.16(d-f). From the cross-sectional view of the MWCNT shown in Fig. 3.16 (d) the MWCNT height grown on top of the G film could be estimated to above $10\text{ }\mu\text{m}$. In addition, most of the CNT appear vertically aligned. A number of bright areas can be observed, some of the marked by an orange dish line, and they indicate the Al_2O_3 layer remaining on top of the catalyst according to the tip growth ‘Odako’ mechanism [181]. Since the MWCNT form by tip growth, the iron catalyst covered by the Al_2O_3 layer was lifted up by MWCNT during the growth. We believe this indirectly prove that the MWCNT have

a stable and strong bonding to the multilayer graphene at the bottom. Without such strong bonds to the G film, the CNT would easily lay down horizontally instead of the vertically aligned growth shown in Fig. 3.16(e).

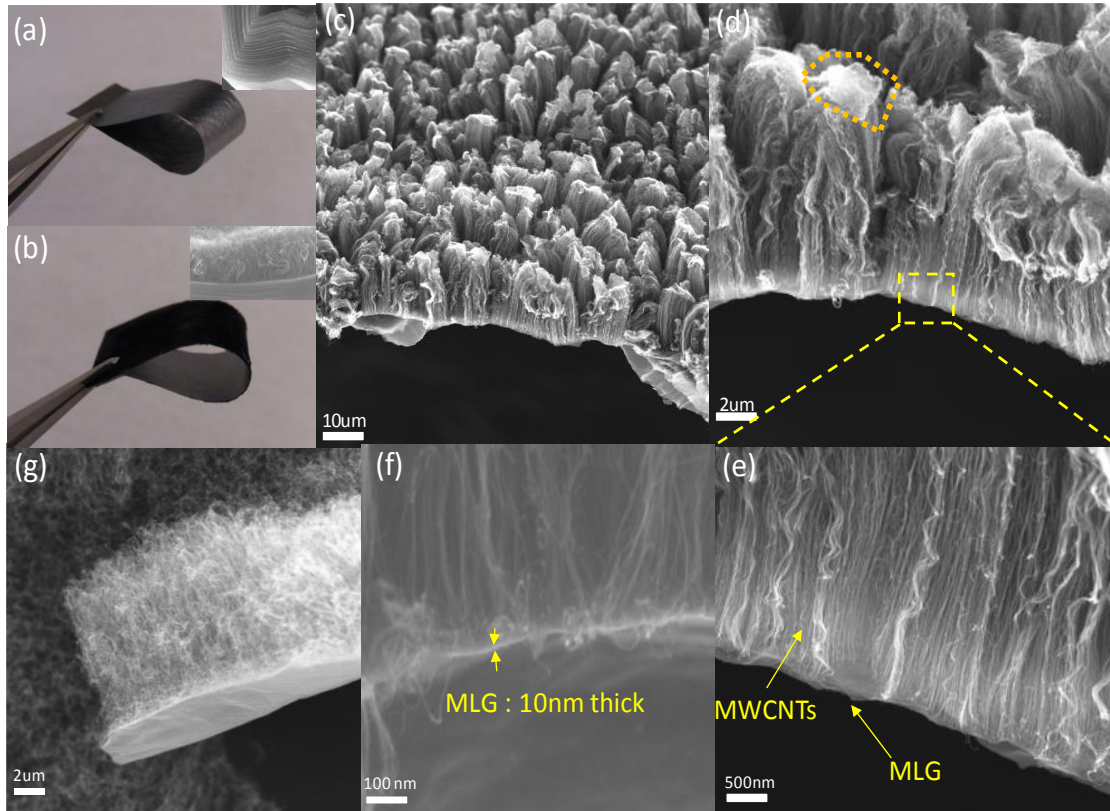


Fig. 3.16. SEM characterization of MWCNT grown on G. (a) The freestanding GBF with stacked layer structure. (b) The freestanding GBF-CNT hybrid film. (c) The overall CNT-G hybrid structure from top view was captured by SEM. (d-f) Several ten micrometer thick of vertically aligned MWCNT directly grow on the tens of nanometer thick G. 3 nm thick alumina layer was lifted up by CNT in the orange marked area. (g) The alumina layer lifted up by CNT was removed using plasma. (From paper G)

In order to investigate the junction structure between CNTs and graphene, the G-MWCNT material was analyzed by TEM. Some detailed results of typical CNTs grown under these conditions are shown in Fig. 3.17. In Fig. 3.17(a), a number of randomly distributed MWCNTs grown on the film can be observed. Moreover, most CNTs are multiwall structures with the diameter of 10 to 20 nm, as shown in Fig. 3.17 (b). Compared to SWCNT-monolayer graphene synthesized in [124], multilayer graphene seems tend to grow multiwall CNT structure. In addition, a number of multiwall ring-like structures can be observed on the graphene film as shown in Fig. 3.17(c) and (d). According to previous reports [25][40], these ring-like structures is an indication of covalent bonds between the CNTs and the multilayer graphene film. Besides

that, the lateral layers inside the root junction of the CNT was also detected in Fig. 3.17(c), which implied that the CNTs are open-ended at the bottom. This result is consistent with theoretical prediction [23][26][41] that one indication of forming covalent bonds with graphene was open-ended CNT at the bottom. Furthermore, the cross-sectional views in Fig. 3.17(e) show how the CNTs have grown from the surface of the multilayer graphene film with covalent bonds. In Fig. 3.17(e) the yellow dashed lines mark the direction of the carbon shells, while the yellow arrow shows the transition shells from the CNTs to the graphene. This indicate that the outermost several shells of CNT is covalently bonded to the multilayer graphene plane. In order to further observe the detailed atomic structure of the MWCNT and planar graphene transformations, high-resolution TEM image, Fig. 3.17(f), was FFT treated to obtain atomic structure as showed in Fig. 3.17(g) and (h). It can be seen that each white dot representing an aromatic ring was orderly arrayed until the walls of MWCNT. The FFT pattern in the upper-right inset shows the six-fold crystal symmetry structure of graphene. However, there some aromatic rings nearby the shells of CNTs, as marked in red arrow, were distorted. That could be due to their out-of-plane orientations from 2D planar graphene. These distorted rings could be the seven-edge rings as reported by previous theoretical work [23][26][41] to form stable G-CNT carbon structure. Taken all the indications together, the graphene and CNTs hybrid structure through covalent bonds was confirmed.

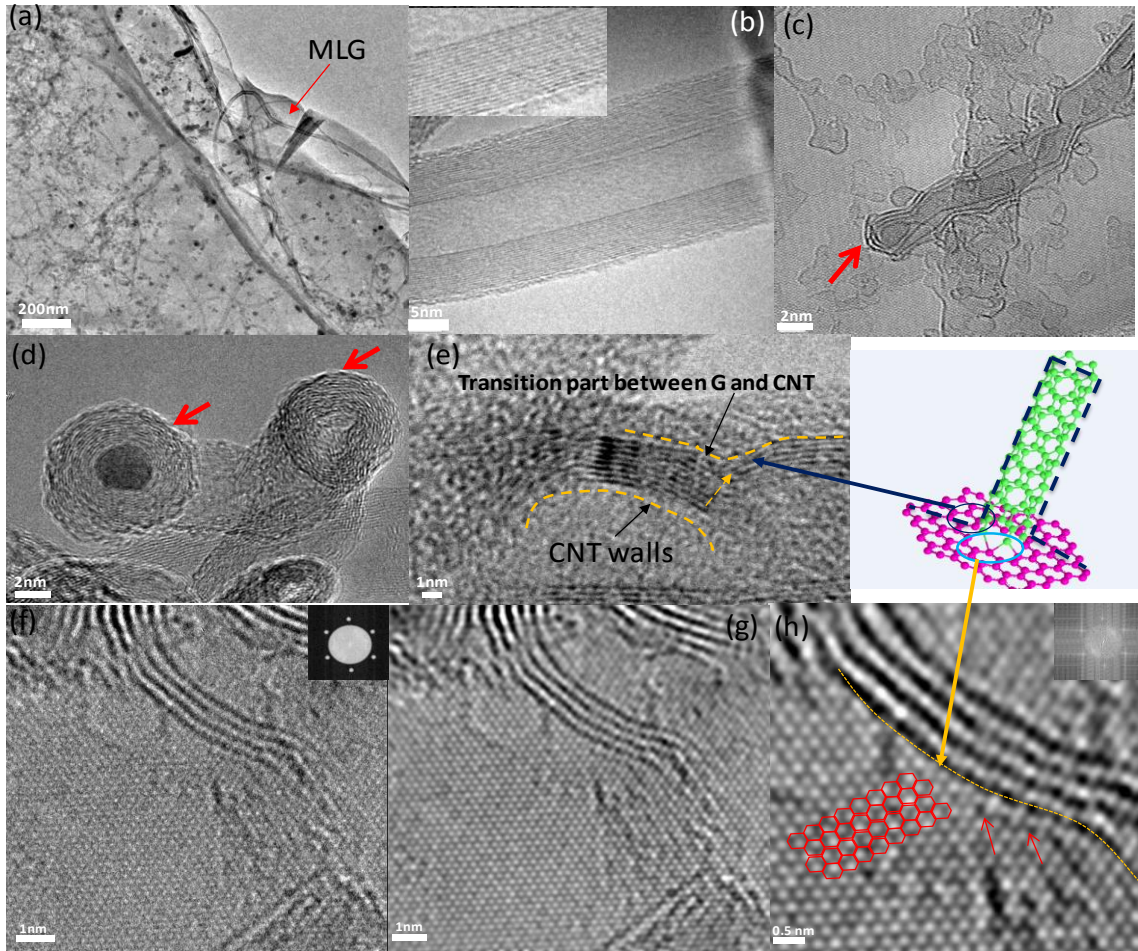


Fig. 3.17. TEM characterization of MWCNT grown on G film. (a) It shows the overall structure of G with MWCNT. (b) This image shows the multiwall structure and diameter of one single MWCNT grown on the G. (c) It characterized the MWCNT root region as marked by red arrow. Additional shells are found on the root. (d) This shows the ring like nanostructure of MWCNT grown on the G. (e) The continuous walls from a MWCNT to graphene was detected with high resolution TEM. (f) The raw high-resolution TEM images show the CNT-G junction. (g,h) The high-resolution images after applying a filter to the FFT of raw image (f). (From paper G)

3.2.3 Thermal Performance characterization of CNT-Graphene hybrid material

To evaluate the thermal performance of the G-MWCNT material acting as a heat sink, the test structure described in Fig. 3.18 was used. First, the test chip was calibrated to obtain the temperature versus resistance calibration curves. Calibration was carefully done with the test chip placed in a thermal chamber and its resistance measured at a number of temperature settings after temperature steady state was reached. As shown in Fig. 3.18(e) the relationship between temperature and resistance shows good linearity, with a

temperature sensitivity coefficient of about $4\text{ }^{\circ}\text{C}/\Omega$. By monitoring the resistance versus the power, dissipated in the hotspot resistor, temperature versus power density curves can be obtained and the heat dissipation performance of the heat sink material be evaluated.

First of all the hotspot temperature curves were plotted for bare chips. As shown in Fig. 3.18(f) the hotspot temperature increased from room temperature to above 100°C when the power density was increased from 0 to $900\text{ W}/\text{cm}^2$. As a reference, chip one was covered with G films without MWCNT and the chip two was covered with the G-MWCNT hybrid material. The application of both materials had a clear cooling effect as shown in the graph of Fig. 3.18(f). As a comparison between the two materials with and without MWCNT, it can be monitored that at a power density of $800\text{ W}/\text{cm}^2$ that for the chips without CNT the temperature decreased $6\text{ }^{\circ}\text{C}$ and for the chips with the G-MWCNT hybrid material the temperature decreased $10\text{ }^{\circ}\text{C}$. These experiments show that the G film serves to effectively spread the thermal energy from the hotspot due to its high lateral thermal conductivity. However, the surface area is still limiting the heat dissipation by convection to the ambient. In contrast, the G-MWCNT structure with vertically aligned CNT is shown to effectively enhance heat convection since the numerous carbon nanotubes function as micro heat sinks improving the heat dissipation.

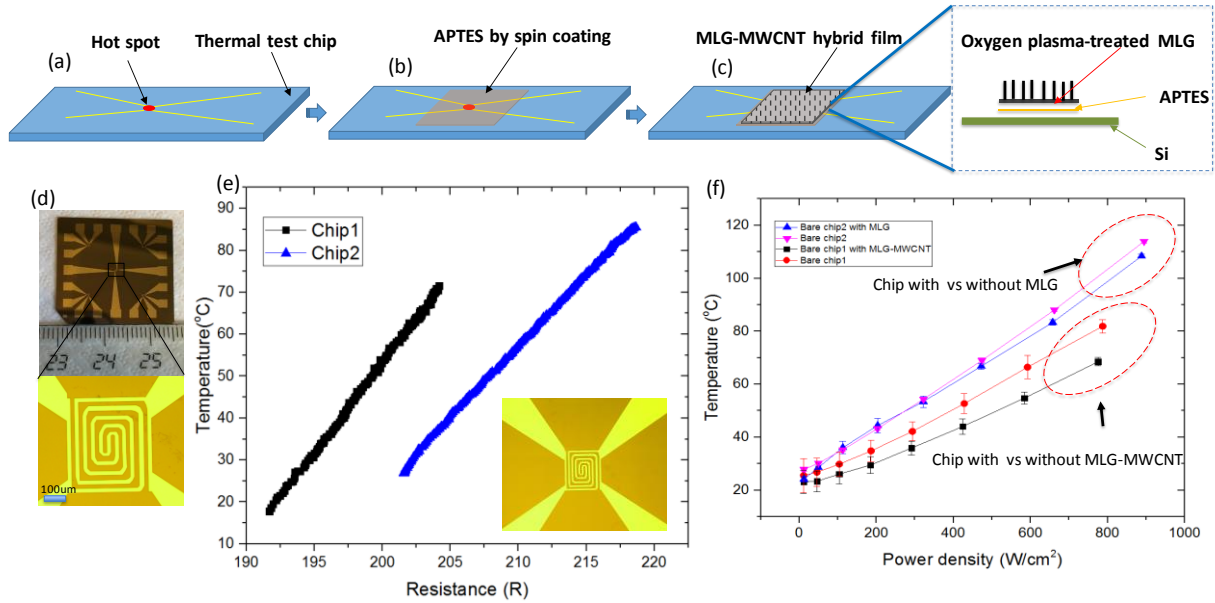


Fig. 3.18. Heat dissipation capability was demonstrated through thermal test chip. (a) Thermal test chip with the hot spot was fabricated through a series of lithography process. (b) A thin layer of APTES was spin-coated on the central part of chip. (c) The G-MWCNT film was spin-coated on the top of hot spot via APTES for improving thermal boundary resistance. (d) The thermal test chip has a micro-heater&sensor to be seen as a hot spot in the central part of chip. (e) The calibration curve of thermal test chips shows a linear relationship between resistance and temperature. The inset image of figure (e) is the hot spot structure from top view. (f) The temperature of hot spot under different power density was respectively measured to make a comparison between chips with and without G and between chips with and without G-CNT. (From paper G)

In order to further verify the performance improvements provided by adding the MWCNT array on top of the freestanding G film, the so-called Joule heating method [173] was used to measure the temperature distribution along the sample mounted as a bridge between two copper electrodes. The experimental setup of the Joule heating measurements is shown in Fig. 3.19(a) and (b). In this setup, the two ends of the sample were attached to the two copper electrodes by solder paste. The sample was then electrically self-heated by a current passing through the bulk of the sample. Two types of samples were tested, one type where the freestanding G film was not covered by CNT, and one type where it was covered by MWCNT. As shown by the images captured by the infrared camera, the temperature distribution always showed its maximum at the middle of the bridge because of symmetry reasons. According to the previous reports [173], the difference in temperature between the middle of the sample and its end terminals can be used to estimate the lateral thermal conductivity of the film. Here, the lateral conductivity of a multilayer graphene film was found to be as high as 1600 W/m·K. It indicated that the G film has strong heat spreading capability.

However, this film does not have good heat convection effect due to limited specific area ratio. According to the results of Fig. 3.19(e), the maximum temperature of the G film was always higher than that of G-MWCNT film when the same power was dissipated in the sample. The extra cooling effect is from the enhanced heat convection of the MWCNT array with high specific area. Moreover, the temperature differences were increased with the higher power. That was attributed to that higher temperature lead to stronger heat convection with ambient air. We also use finite element model simulation to further verify this result. The simulation results as seen in Fig. 3.20 were showing a good agreement with experimental work. The results of these experiments and simulations indicate that the G-MWCNT film was quite effective as a micro heat sink. Taking advantage of the large surface area to volume ratio and the high thermal conductivity of the CNT, the heat generated by the power dissipation in the sample was effectively transported to the individual CNT through the low thermal contact resistance of the covalent bonds to the G film.

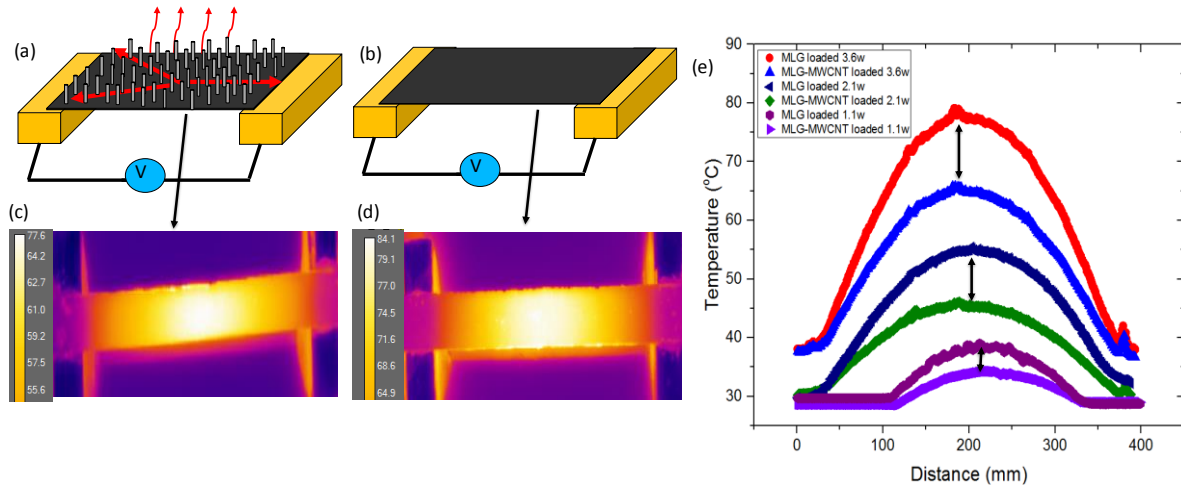


Fig. 3.19. (a) and (b) GBF-CNT and GBF strips are heated up through joule heating effect after loading the same power. (c) and (d) show the temperature distribution of the samples loaded with 3.5W using IR camera. (e) The temperature distribution curves under different power are shown in this figure. (From paper G)

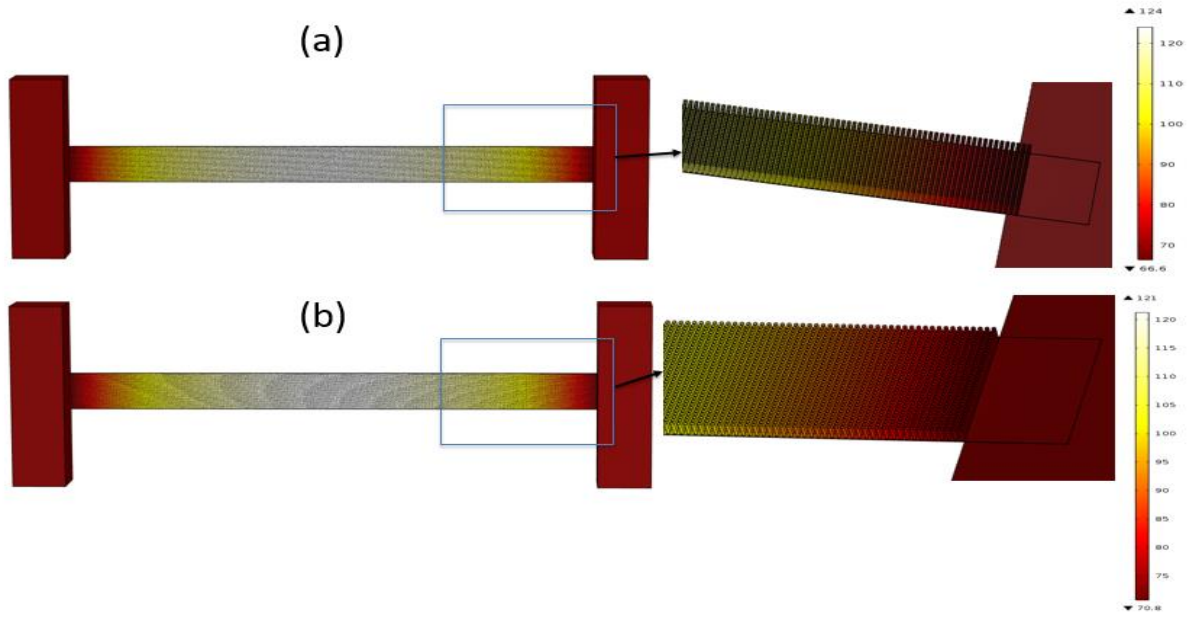


Fig3.20. (a) The Finite element model of G-MWCNTs without covalently bonds was simulated and the temperature distribution was obtained. (b) The temperature distribution of the model of G-MWCNTs with covalently bonds is shown in this image.

One critical factor when it comes to the thermal performance of this G-MWCNT hybrid structure for dissipating heat is the thermal contact resistance between the bottom film and the vertically-aligned CNT. This bottom junction could easily become the thermal bottleneck limiting the heat dissipation from the film to the CNT. The limiting phonon scattering is much larger at the junction due to the media change in dimensionality along the phonon path, which could lead to a mismatch of phonon spectra along the path of phonon transportation [131]. Some simulation work investigating the thermal performance of the junction between single-wall CNT and graphene has been reported in literature [130], [160], [162], [170], but to our knowledge there are no experimental reports on the junction between multi-wall CNT and graphene. Therefore, we found it is quite significant to measure the thermal junction resistance in the one dimensional CNT and two-dimensional graphene hybrid application.

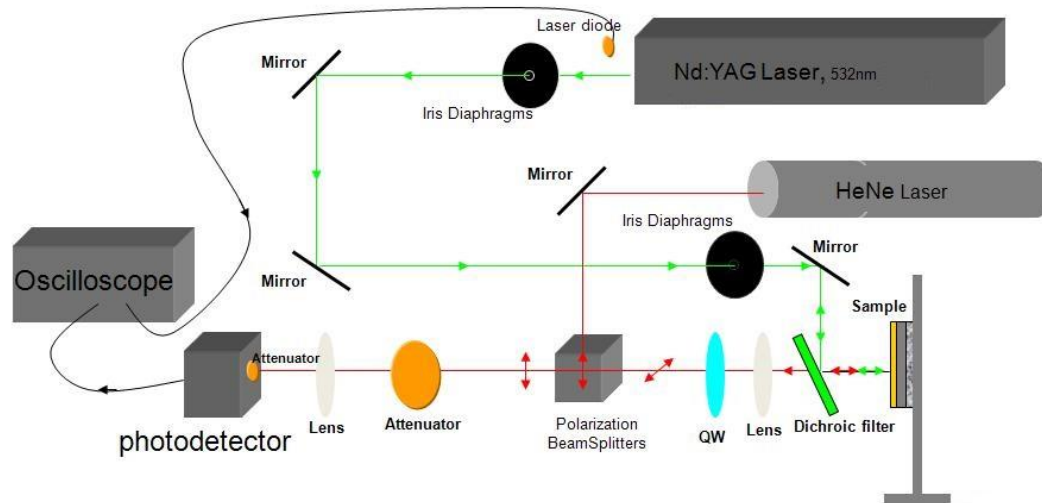


Fig. 3.21. Schematic diagram of PPR experiments.

In this work, the pulsed photothermal reflectance method (PPR) was used to measure the thermal junction resistance of our samples [174], [175]. PPR was first used to measure the thermal conductivity of SiO₂ thin film [184], since then it has been widely used to exam the thermal properties of thin films [185], [186]. Fig. 3.21 shows the setup of the pulsed photothermal reflection measurement used in this study. As shown in Fig. 3.22 (a) and (b), a 300 nm thick TiN layer was deposited on the surface of CNT to enhance the heat absorption. In these measurements, the sample was first excited by a Nd:YAG laser pulse as shown in Fig. 3.22 (c). This pulse first causes a fast rise of the surface temperature followed by a temperature relaxation. The change of surface temperature was monitored by a probe laser, the beam of which reflects from the surface of the sample. Since the relaxation time is governed by the thermal properties of the underlying layers and the thermal interface resistance between the underlying layers, the thermal properties of the underlying materials can be obtained from the experimental temperature profile by fitting the data to a theoretical heat conduction model. Two sets of samples were fabricated for these tests. One set of samples with covalent bonding between the film and the CNT and one set of samples without covalent bonds obtained by normal CNT growth were fabricated as respectively shown in Fig. 3.22 (a) and (b). Some typical plots of the normalized surface temperature versus time obtained by the probing laser are shown in Fig. 3.22(f). Obviously, the surface temperature of G-MWCNT samples was attenuated much faster than the normal CNT growth samples. By fitting the experimental data to the heat conduction model, the two thermal contact resistances R_1 and R_2 between the TiN film and the CNT, and between the CNT and the graphene film, respectively, can be extracted. This is shown in Fig. 3.22 (g). The extracted contact resistance R_1 between the TiN metal film and the CNT is found to be almost the same for both sets of samples, $\sim 10^{-6}$ m²K/W. However, for the contact resistance R_2 between the CNT and the graphene, there was an extreme decrease

from 7.5×10^{-7} to 9×10^{-10} $\text{m}^2\text{K/W}$. This thousandfold decrease of the contact resistance when the van der Waal contact was replaced by a covalently bonded junction is consistent with MD simulation work on sp^2 covalent bonds [130], and has now for the first time been experimentally verified. Although the extracted contact resistance is still one order of magnitude larger than the ideal theoretically predicted value of the resistance of a sp^2 covalent junction due to defects, it can be claimed that sp^2 covalent bonds were indeed formed at the junction when the CNT were grown on the graphene film. From the perspective of thermal transport, we found it is indirectly verified that the phonon spectra mismatch of a covalently bonded junction between dissimilar materials is much lower than for a van der Waal junction. Moreover, this lower mismatch degree of phonon spectra indeed bring higher thermal transport capability. As shown in Fig. 3.22 (h), the sample with covalently bonding lead to extra cooling effect as compared with the sample without covalently bonding under joule heating condition. This finding will be extremely important and significant for the lifespan of the IC device.

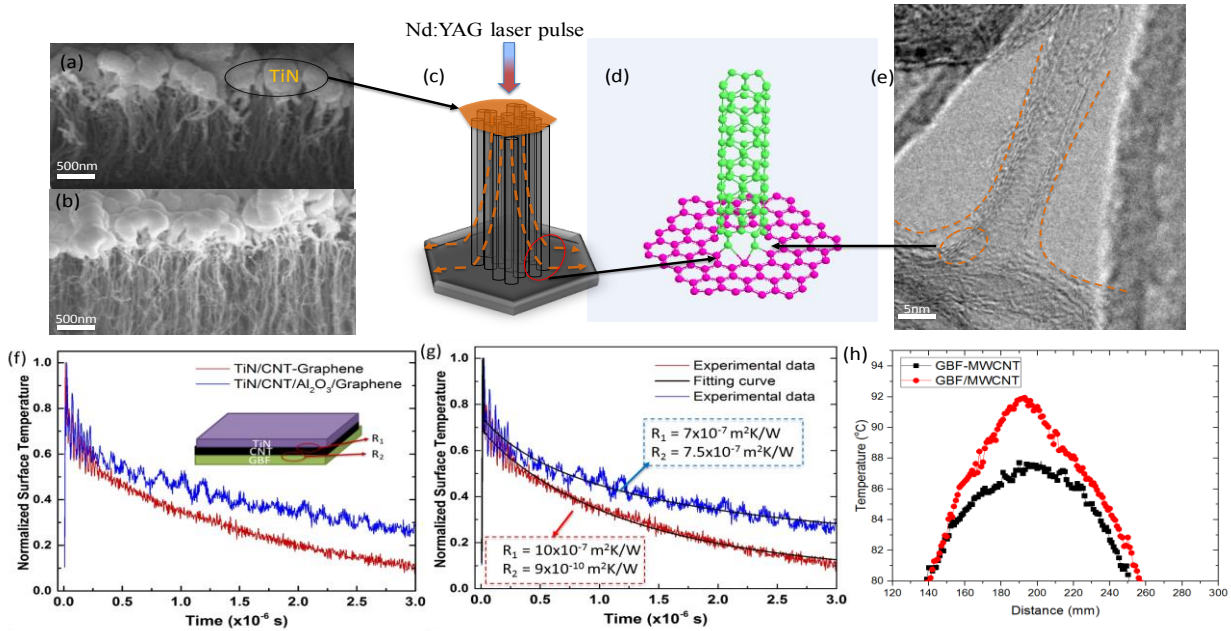


Fig. 3.22. (a) SEM image shows the MWCNT grown on G with covalent bond was covered by 300nm TiN through sputtering process. (b) show the reference sample without covalent bonds. (c) Schematic structure describes the specific structure used for PPR measurement. The laser pulse will come from the top surface of TiN. (d) and (e) shows the detailed structure of covalent bonding between MWCNT and G by TEM. The MWCNT shells are keeping continuous at the transition place of CNT and graphene. (f) and (g) figures illustrate the surface temperature's attenuation with time and thermal junction resistance was obtained through curve fitting. (h) shows the temperature distributions of the samples with/without covalent bonds under joule heating condition. (From paper G)

3.3 Boron Nitride based film for heat spreader application

Hotspot issue usually exists in the power chip due to uniform IC design in the silicon. It is very critical for the reliability of IC device. In order to solve this problem, various heat spreader materials have been developed. Some metallic materials such as copper and aluminum are widely used due to their high thermal conductivity. However, the thermal performance of metal films decreases dramatically when their thicknesses are reduced into nano-scale. It is attributed partly to the scattering of the conduction electrons from the film surfaces and partly to the scattering by lattice impurities and frozen-in structural defects in the films [187]. Therefore, metal materials would not be very compatible with the trend of thinner and smaller power devices. To address this problem, carbon based materials have been developed as heat spreaders in recent years, including graphene heat spreader [188], graphite film [189] and carbon nano-tube (CNT) cooler [190]. These new heat spreader materials show lightweight, small size and extremely high thermal conductivity. However, high electric conductivity of carbon-based materials also limit their application in the high power electronics. Two-dimensional hexagonal Boron Nitride (hBN) is a layered material with a wide band gap. It has many attractive properties such as large thermal conductivity and low dielectric constant which enable potential application in thermal management of electronics packaging [191]–[194]. Layered hBN material is referred to as “insulating white graphene”. Unlike CNTs or graphene, it is a layered material with a wide band gap (~ 5.9 eV) [195]. So it is an electrical insulator with a dielectric constant of 3-4 [196]. Meanwhile, this material shows high thermal conductivity. The thermal conductivity for hBN nano-ribbons can reach to 1700~2000W/mK [197]. Therefore, it could find applications in thermal management of high power electronics and displays where CNTs and graphene materials are not allowed. Many methods were developed to synthesize monolayer and multilayer hBN films for different application. The first method was mechanical exfoliating. Because of weak van der Waals force between layer and layer, h-BN films could be peeled off from bulk hBN crystal by micromechanical cleavage [196]. And Chemical liquid phase exfoliation method was also reported to be an efficient way to get few-layer h-BN films over small area [198]. The growth of large area, few-layer hBN films using chemical vapor deposition (CVD) on metallic substrates and transfer to other substrates has been reported in the past year [199]. However, the application of hBN as heat spreader has never been demonstrated. In this section, the application of hBN heat spreader prepared by liquid phase exfoliation will be demonstrated to solve hotspot issue in the power chip.

3.3.1 Fabrication of Boron Nitride based film

Here we outlined the fabrication process for hBN film by liquid phase exfoliation method as shown in Fig. 3.23. Firstly, hBN micro-powder was dispersed in isopropanol alcohol (IPA) with a concentration of

10mg/ml. IPA is a good solvent to exfoliate hBN material[198]. The dispersion was sonicated for 3h using Branson Model 450 ultrasonic disruptor. Then hBN solution was centrifuged at 2000rpm for 30 minutes. After that, the supernatant was decanted into the beaker. Because the hBN nano-sheets exfoliated from the hBN solution were very difficult to form a freestanding film, acetate cellulose solution was also prepared to mix with hBN solution together to solve this problem. Afterwards, this hybrid solution was sonicated for 15minutes. After sonication, uniform hybrid suspension was obtained. Thirdly, the hybrid solution was filtrated and hBN film attached on the filter paper was obtained. Then a little acetone was decanted onto the wet hBN film to dissolve the filter paper. After drying at room temperature, the freestanding hBN film was obtained.

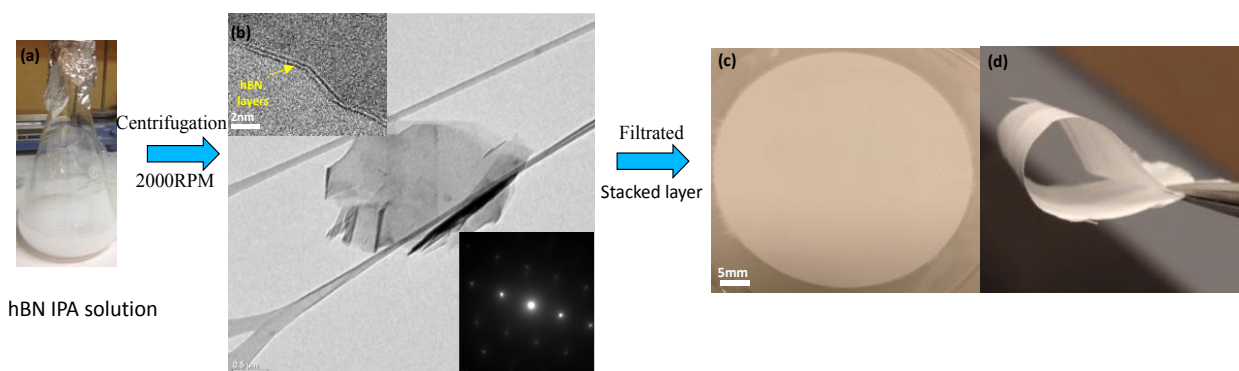


Fig. 3.23. Characterization of (a) hBN solution, (b) TEM pictures of 2D hBN sheets after centrifugation and (c) the freestanding hBN film after filtration. (From paper E)

3.3.2 Microstructure characterization

In general, it is difficult to fabricate freestanding pure hBN films due to their poor mechanical performance. However, Fig. 3.23 (c) shows the hBN films prepared in this paper are very flexible and uniform because of the addition of acetate cellulose [200]. Because the acetate cellulose excellent mechanical performance, it can enhance the strength of the hBN film as a glue by wrapping the 2D hBN sheets together. Moreover, there would be hydroxyl groups (-OH) and amino groups (-NH₂) on the edge of the hBN sheets. Meanwhile, the cellulose surface has many hydroxyl groups (-OH) and carboxyl groups (-COOH). Based on the principles of chemistry, the hydrobonding between acetate cellulose and the hBN sheets can possibly form. In order to examine the detailed structure of the hBN sheets after centrifugation, transmission electron microscopy (TEM) was used to measure the thickness and crystal structure. Fig. 3.24 shows the representative TEM images of various thicknesses of h-BN sheets. As shown in the Fig. 3.24 (a), the TEM image shows that thickness of this hBN sheet is just around 0.7 nm, which indicate two layers thick hBN sheets were attached on the TEM grid. The reason is that the thickness of one layer hBN is equivalent to one atom of hBN which is around 0.33nm [201]. Meanwhile, based on the number of lines at the folding

edge, we can also clearly and directly see the number of layer. The Fig. 3.24 (b) and (c) show the three layers and four layers of hBN sample respectively. Moreover, the both TEM images show that folding edges of different layers are parallel with each other. However, Fig. 3.24 (d) shows that some parts of the hBN atomic layers are aligned and some parts are randomly arranged. That's called fringe-like features, which could be either due to lattice fringes or wrinkles in the hBN layers or due to the fact that the c-axis orientation of the multilayer stacking is in the in-plane direction. If the lattice fringes lead to this feature shown in the multilayer sample, it indicates that this multilayer samples seems to be polycrystalline. Further, the selected area electron diffraction (SAED) of Fig. 3.24 (d) shows circular rings mixed with the individual spots. That means that some parts

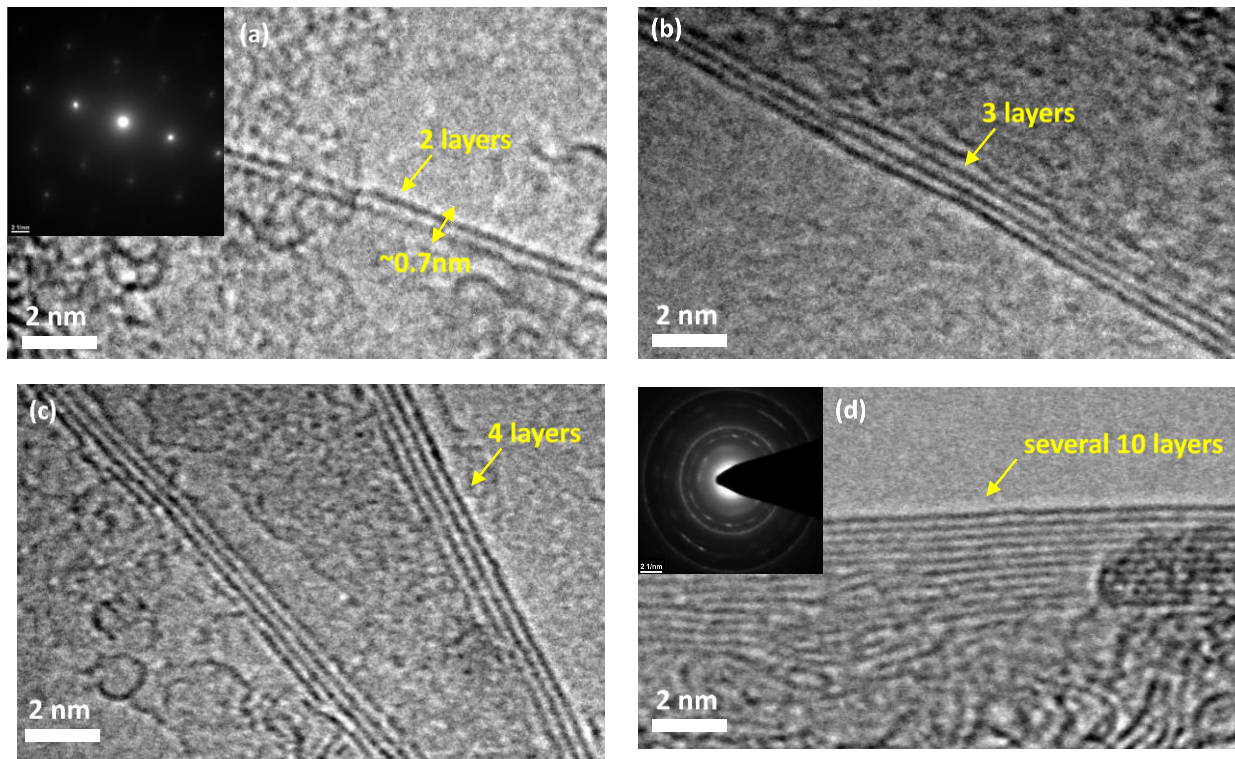


Fig. 3.24. TEM characterization of hBN sheets. (a) TEM images of 2 layers hBN sample, (b) 3 layers hBN sample and (c) 4 layers hBN samples at their folder edge; (d) above 10 layers hBN samples at their folder edge. (From Paper E)

of samples (d) have a polycrystalline structure. The edge of the sample Fig. 3.24 (d) also suggested that the crystallites of the several ten layers hBN stacks are randomly oriented, comparing with the aligned straight lines as shown in the Fig. 3.24 (a) and (b). The SAED pattern of the hBN sheet shown in these both samples, presents hexagonal symmetry of hBN, which imply that these samples have high quality [202].

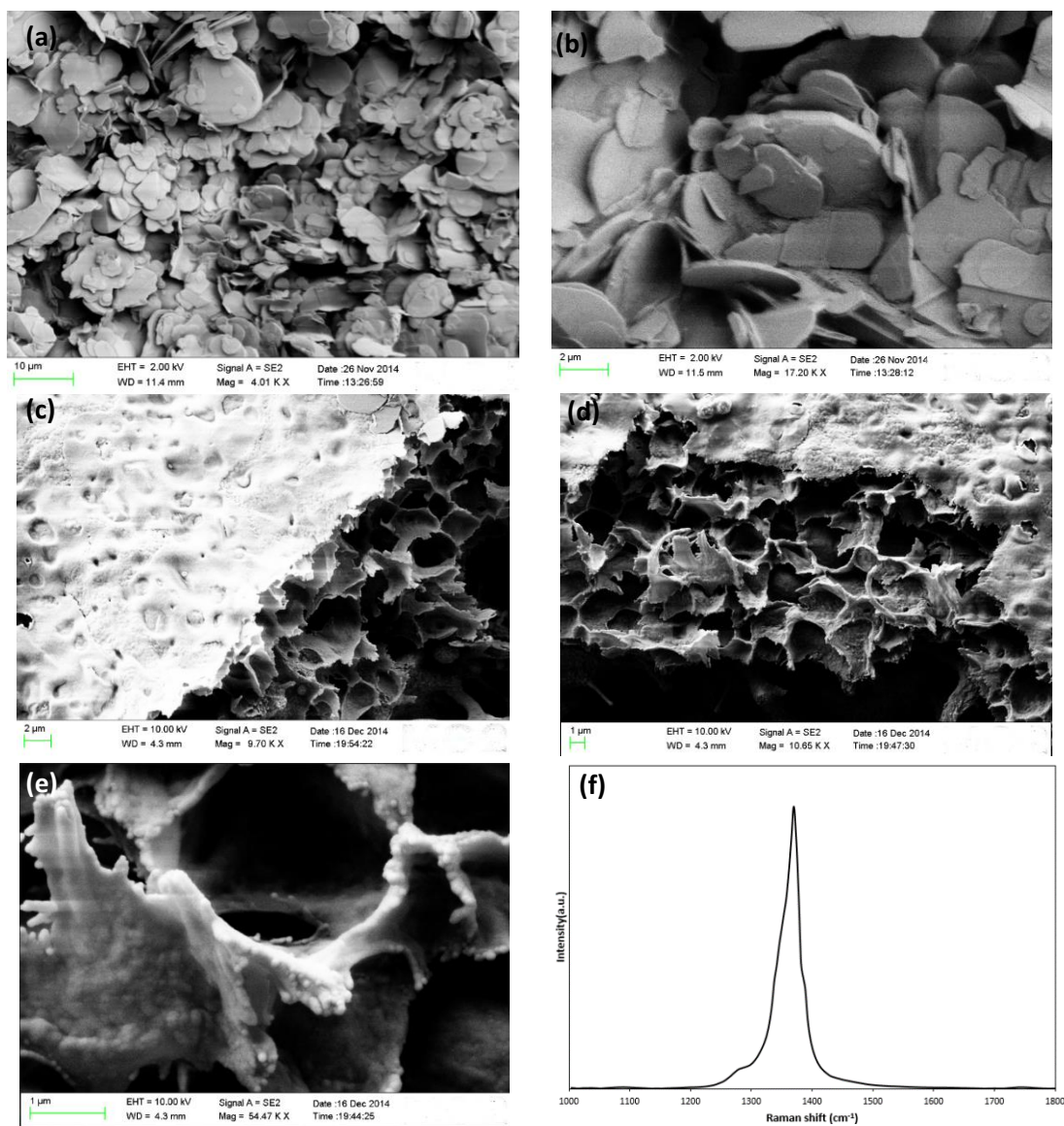


Fig. 3.25. (a)(b) Characterization of cross section of hBN film without acetate cellulose using SEM; (c) (d) SEM image of cross section of hBN film with acetate cellulose and (e) zoom-in the SEM image; (f) Raman diagram of hBN film surface (From paper E)

The SEM machine was employed for investigating the structure of the stacked layer film after infiltration. As shown in the Fig. 3.25 (a) and (b), the pure 2D hBN sheets are like random petals which can't agglomerate together. Therefore the pure stacked hBN sheets is difficult to form a freestanding film. The cross section of the hBN film with acetate cellulose was also observed using SEM, as shown in Fig. 3.25 (c) and (d). The 2D hBN sheets were tightly packed together to form a layered film structure. Based on Fig. 3.25 (f), the Raman peak of this film is located at around 1366 cm^{-1} , which means the film consists of layered hBN sheet [203].

3.3.3 Thermal performance characterization

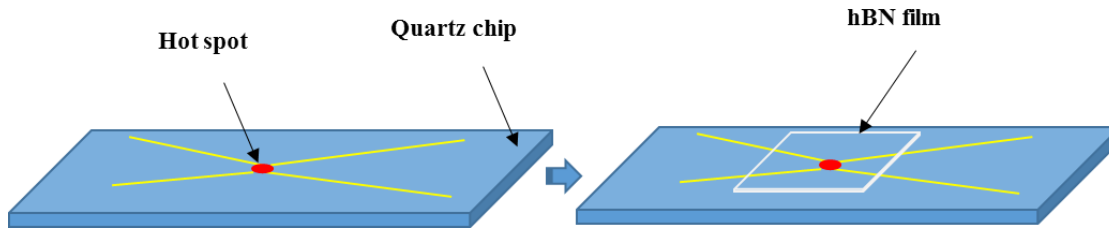


Fig. 3.26. The model of heat dissipation structure

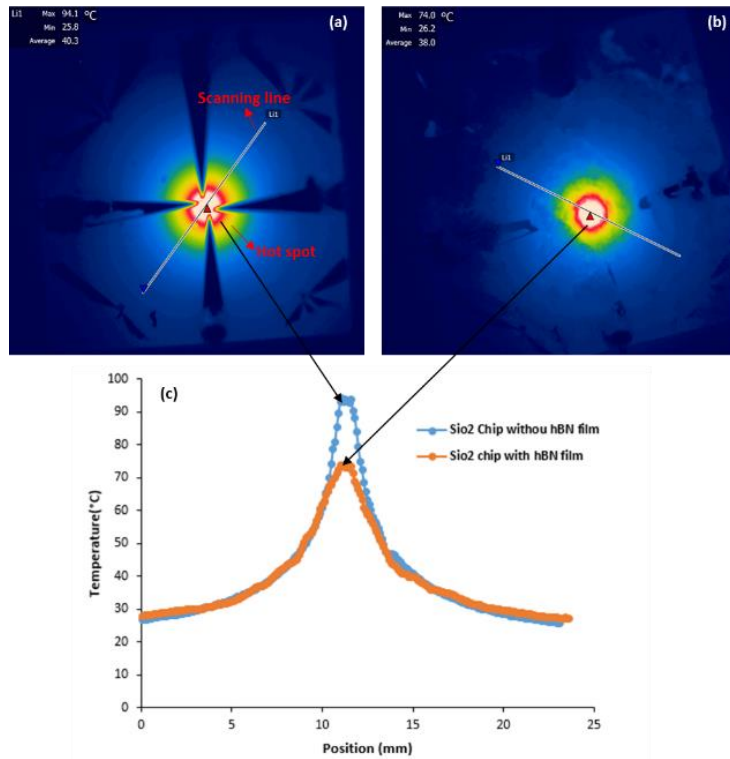


Fig. 3.27. (a) Temperature distribution of the power chip without hBN film; (b) Temperature distribution of the power chip with hBN film; (c) Temperature distribution along the line direction shown in the (a) and (b). (From paper E)

In order to study the thermal performance of the hBN film, a similar thermal test chip as used in previous section was employed. For measuring the heat dissipation effect of the hBN film, the thermal test chip with hot spot was tested by infrared camera. Fig. 3.27 (a) shows the temperature distribution on the chip without hBN film, while Fig. 3.27 (b) presents the temperature map on the chip with hBN film. The hot spot temperature without hBN heat spreader is about 20 °C higher than the one with hBN heat spreader. Meanwhile, the hot spot area is also much bigger on the chip with hBN heat spreader than the one without.

They both indicate that the hBN films can effectively weaken the hot spot effect. As shown in Fig. 3.27 (c), the temperature distribution of the sample with hBN film is much more uniform, compared to the sample without hBN film, which implicated that the hBN film can efficiently spread the hot spot thermal energy in plane direction. The experimental results have demonstrated the hot spot cooling effect of the hBN film as heat spreader. Furthermore, the cooling effect also is explained through the thermal transfer theory. The key point of this heat dissipation model is that the thin film is used to spread heat from the hot spot in the central part of the chip. The whole model was exposed in the atmospheric environment to have a natural convection. That means that the heat spreading resistance of the hot spot will directly influence the cooling effect of hot spot. According to the heat spreading resistance calculating theory mentioned in another paper [204], the below formula can be employed.

$$R = \frac{H}{k\pi\sqrt{a}}$$

Where k is the thermal conductivity, a is the heat source area, H is the spreading resistance factor and R is the thermal resistance. In addition, the excellent thermal conductivity of the layered hBN increased the k value in the denominator. Therefore, the heat spreading resistance can be substantially decreased accordingly.

Chapter 4

4. CNT based TSV for 3D IC packaging

While the previous chapter concerned a carbon based material for improving thermal management of electronic packaging, this chapter concerns the use of carbon nanotubes for electrical interconnect applications in 3D packaging of integrated circuits. As shown in Fig. 4.1, three applications concern the use of vertically aligned carbon nanotubes for replacing or enhancing copper in through-silicon-via applications, while the other application concerns the use of carbon nanotubes for flexible TSV applications in the flexible electronics.

Concerning the use of carbon nanotubes for through-silicon-via applications one problem is that the carbon nanotubes might have to be transferred from the wafer where they are grown at a temperature too high to be compatible with silicon IC technology. For this purpose, we have developed a simple and efficient tape-assisted method for transferring the carbon nanotube via bundles to the through-silicon-via wafer. For optimizing the electrical performance, a new carbon nanotube/solder hybrid structure material was developed for interconnect application. In order to further enhance electrical conductivity, thermal and mechanical properties of the through-silicon-via material, finally we proposed a nanocomposite material where vertically aligned carbon nanotubes are used to enforce the copper via material. Moreover, due to the flexibility of CNT material and the growing interest of flexible electronics, a flexible TSV application in a flexible 3D IC system was also demonstrated in this chapter.

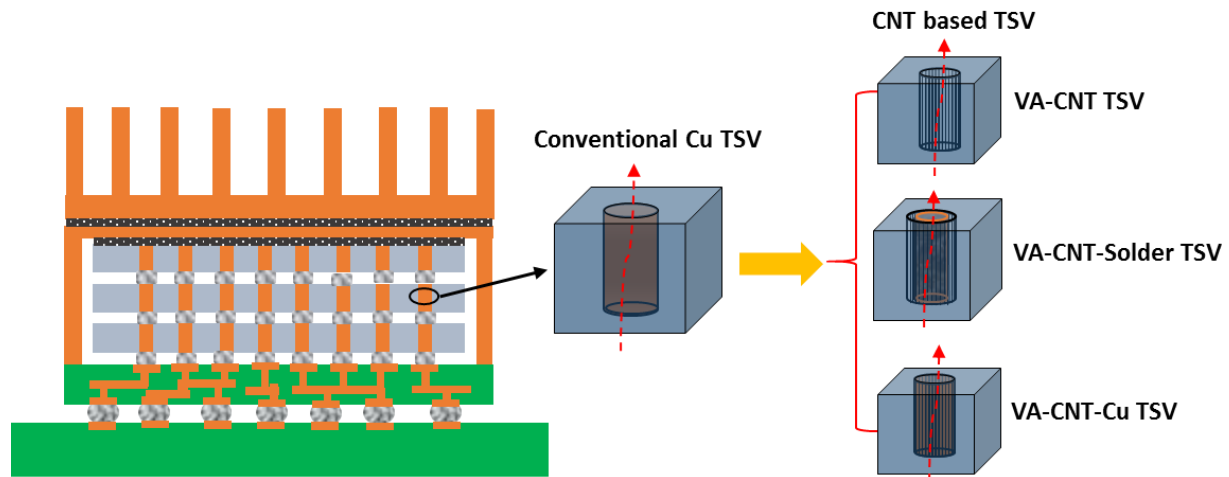


Fig. 4.1. The scheme structure of different types of TSV based on the 3D IC packaging.

In this chapter, some background information of the properties of vertically aligned carbon nanotubes is provided and the main findings presented in the four appended papers are summarized. As already stated

in chapter one of this thesis, conventional copper through-silicon-vias are faced with several obstacles including limited current carrying capability, low aspect ratio, CTE mismatch and electronic migration, which will hinder the miniaturization trend of future microelectronics packaging. Thus, CNT, representative of emerging material, is employed in this chapter to replace the metal for filling the TSV due to that CNT possesses many excellent performance such as low thermal expansion [28] low joule heating [29] and does not fail in high current density due to electromigration [30].

4.1 Synthesis of VA-CNTs

The physical properties of CNTs are strongly dependent on the way they are grown. Commonly there are three mostly used methods to grow CNTs, namely arc discharge [205], laser ablation [206] and chemical vapor deposition (CVD) [207]. Each method requires carbon feedstock and certain temperature conditions. Compared to the other two methods, CVD method is advantageous due to the high purity and excellent alignment of synthesized CNTs as well as good controllability and up-scalable production process. Moreover, the CVD method is most suitable for the patterning of desired interconnect layout. Therefore, all the synthesis of the VA-CNTs is conducted in a commercial low-pressure cold-walled CVD apparatus, named Black Magic II from Aixtron. The setup of the CNT CVD is illustrated in Fig. 4.2 (a). As shown in Fig. 4.2 (b), various gases are introduced into the chamber and distributed uniformly across the wafer on the graphite holder/heater by a gas shower header. A thermocouple sensor is attached to the graphite heater to monitor the wafer temperature and give feedback to the control system. The exhaust pipe is placed at the bottom of the chamber for maintaining a stable chamber pressure.

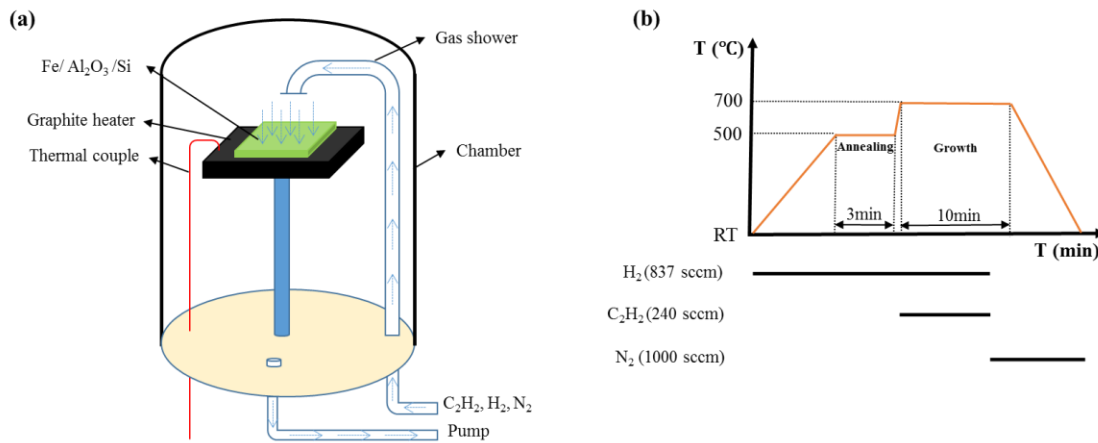


Fig. 4.2. (a) Illustration of the thermal LPCVD reactor, and (b) the CNT growth flow-chart.

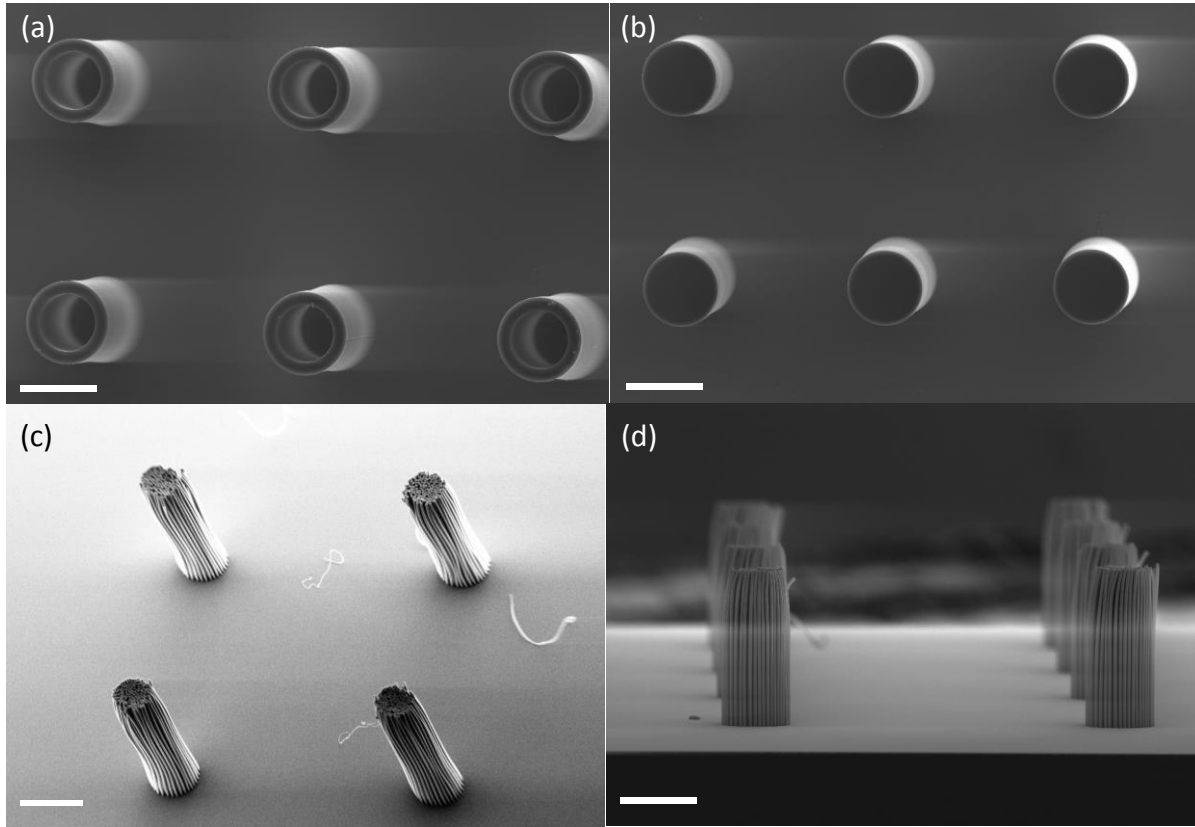


Fig. 4.3. The morphology of different structure of CNTs grown on silicon substrate. (a) Hollow structure; (b) pillar structure; (c) and (d) circular CNTs array. The scale bar is 200 μm .

Fig. 4.3 shows different structure of CNTs bundles, which are grown from lithography-patterned catalyst. All the CNTs are aligned in the vertical direction due to the crowding effect from neighboring CNTs[208], which is quite helpful to use as interconnect in the TSV application. Fig. 4.3 (a) presented a hollow structure consisted of VA-CNTs, which can be filled in by solder or other material to form a composite material, while CNTs pillar structure shown in Fig. 4.3 (b) can be further processed through densification process for interconnect. Fig 4.3 (c) and (d) show a circular CNT array consisting of hundreds of high-aspect-ratio CNT bundles, which create a chance to make metal more uniformly distributed among the CNTs by electroplating method.

4.2 VA-CNTs TSV for interconnect

The CNT's high electrical [209]/thermal [210] conductivity and resistance to electro-migration makes it a good fit for electronics that require high reliability. Thus, vertically aligned CNTs are regarded as a most promising TSV material [211] [212] [213] and as a possible future substitute for today's copper TSVs. However, the harsh condition of CNT growth is not compatible with IC manufacture process. Even though many attempts have been tried to synthesize CNT at low temperatures, the quality and density of CNTs grown at low temperatures is still an problem [214]. Therefore, post-growth CNT transfer becomes the obvious solution for getting around this issue. This section focused on using a novel tape assistant transfer method to fill VA-CNTs bundle into via for interconnect. Fig. 4.4 illustrated the process flow of developing VA-CNTs TSV for interconnect.

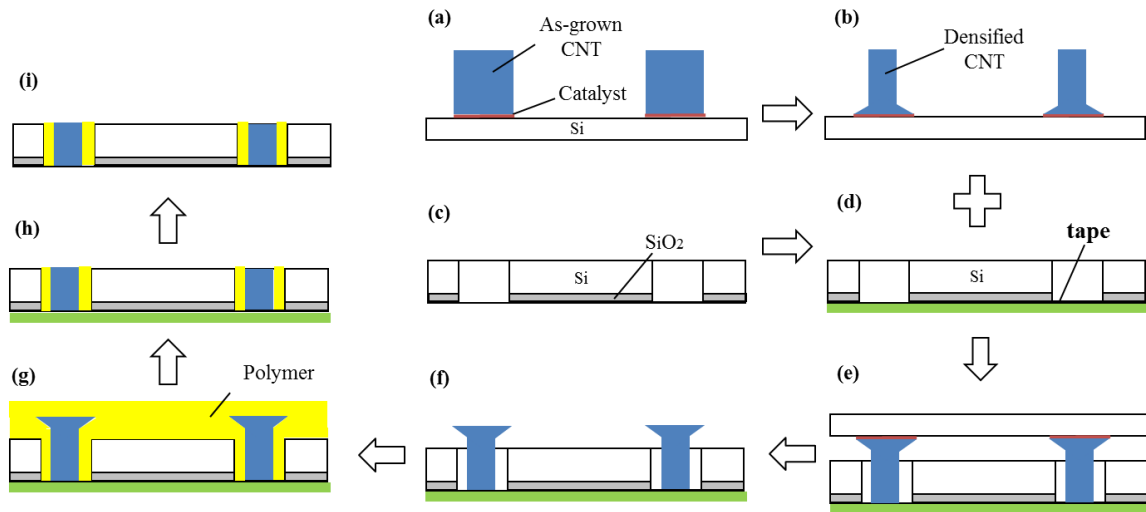


Fig. 4.4. Step-by-step schematic of the process for accomplishing CNT filled TSVs. (a) First, CNT bundles are synthesized by using CVD at a temperature of 700 °C. (b) Second, as-grown CNT bundles are densified using the paper-mediated densification method [15]. (c) In parallel to these steps, the target wafer/chip is prepared by deep reactive ion etching (DRIE) of the TSV openings. (d) A layer of adhesive tape is attached onto the front surface of the target wafer/chip. (e) Third, CNT bundles are transferred into the via openings and retained onto the adhesive tape by use of a flip-chip bonder. (f) Fourth, the donor wafer/chip is removed. (g) Fifth, a polymer resin is dispensed on the chip surface and cured. (h) Finally, the back surface of the wafer/chip is planarized through CMP and excessive polymer removed, where after the adhesive tape can be removed (i). (From paper B)

Densification and Transfer of CNT bundle

In order to enhance the electrical conductivity of CNT bundle, as-grown porous CNTs bundles were densified through paper-mediated controlled densification method [36]. After densification, a 20/100 nm Ti/Au sandwich layer was sputtered to cover the CNT bundle top surface to promote a complete transfer and to decrease the contact resistance. In parallel to preparing the CNT wafer for transfer, via openings with a diameter of 300 μm were etched in the target wafer through DRIE using a 400 nm SiO_2 layer as mask. The transfer process was carried out by a flip chip bonder machine (Fine Tech) and adhesive tape. Paper B has described the detailed transfer process.

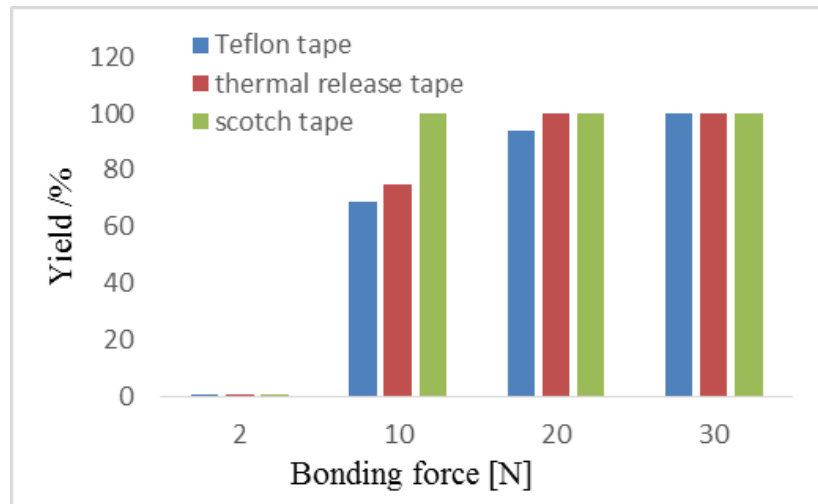


Fig. 4.5. Yield as a function of the bonding force. (From paper B)

As is summarized in Fig. 4.5, CNT transfer was not successful for any of the three tapes when only a low bonding force of 2 N was used. Increasing the bonding force to 10 N, the yield increased to 69%, 75% and 100% for the Teflon, thermal release tape, and Scotch tape, respectively. When a 20 N bonding force was used, the yield increased to 100% for both the thermal release tape and the scotch tape, the yield for the Teflon tape was about 94%. For a bonding force of 30 N, the transfer yield increased to 100% for all three tapes. The reason for the low transfer yield at low bonding forces, is likely due to the bonding strengths between carbon nanotubes and catalyst being larger than that of adhesive strength of the tape. Hence, when the donor chip is lifted, carbon nanotubes remain stuck onto the donor chip. For bonding forces of 10 N, the flatness of the adhesive became the main factor affecting the yield. For instance, Teflon tape is much thinner than the other two types of tapes, so it is not as flat as the other two tapes, and that was not compensated by its strong adhesive properties. The influence of tape flatness, was of less importance at higher bonding forces, the only disadvantage of the higher forces being that some CNT bundles endured a slightly axial deformation. However, when lifting away the donator chip, carbon nanotube bundles would retract, at least to some extent.

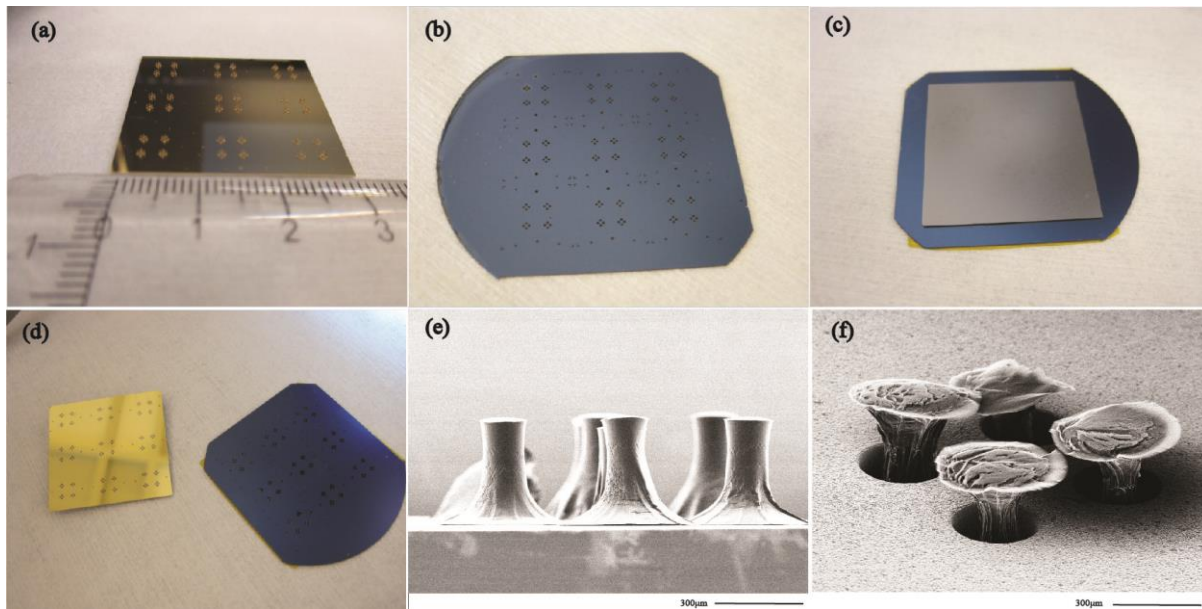


Fig. 4.6. Wafer scale CNT transfer by tape. (a) Photograph of the 2 inches' wafer with CNT bundles. (b) Photograph of a 2 inches' target wafer with via openings. (c) Photograph of the bonding. (d) Photograph of separation of CNT bundles wafer and tape adhered TSV wafer. (e) SEM of local CNT bundles on the donor wafer (f) SEM of local CNT bundles after transferring on the acceptor TSV wafer. (From paper B)

Based on the optimized transfer process, for the first time, wafer scale transfer of vertical CNT bundles as shown in Fig. 4.6 has been demonstrated. A set of 2 inch wafers, one with 144 CNT bundles and one with 144 via openings, was prepared as shown in Fig. 4.6 (a) and (b), respectively. For wafer scale CNT transfer process, the yield was up to 97%. Only five short CNT bundles on the edge of the donor wafer were lost, and the transfer yield was higher than previously reported for the method where indium was used as the transfer medium [29]. Since tape assisted CNT transfer can be achieved at room temperature within a couple of seconds by means of a flip-chip bonder, the transfer process is compatible with standard electronic packaging processes. Most importantly, the tape would prevent the front surface of wafer from any contamination during the following polymer filling process, meaning that no CMP process needs to be carried out on the front surface of wafer. It is expected that the transfer yield could be improved further, provided uniform wafer scale CNT bundles are obtained by utilizing a more advanced thermal controller, and wafer scale CVD equipment.

Filling CNT bundle into TSV and electrical characterization

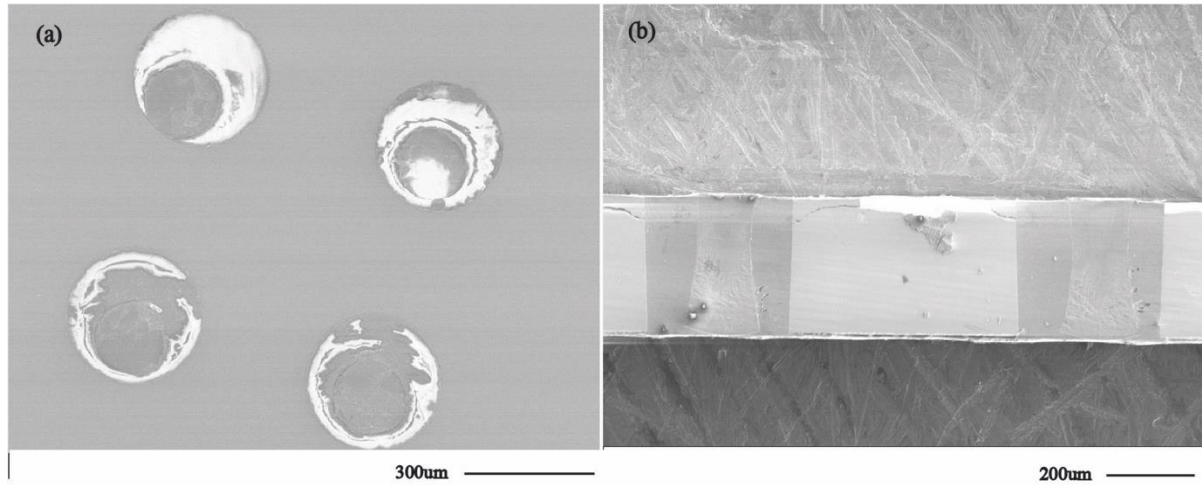


Fig. 4.7. (a) SEM of back surface of CNT TSV after CMP. (b) Cross section of epoxy filled CNT TSV.

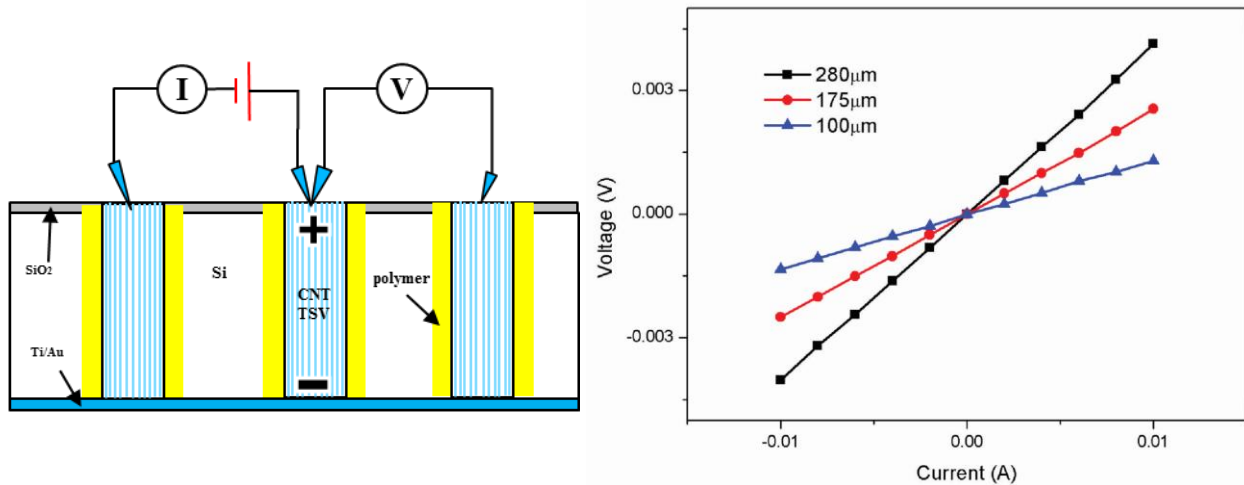


Fig. 4.8. Illustration of four-probe method for measuring the resistance of the middle CNT TSV and DC I-V response of a CNT-TSV of three different heights 100 μm, 175 μm and 280 μm as measured by the four-probe method. (From paper B)

In order to measure the electrical conductivity of the CNT vias, a sandwich layer of 20 nm titanium and 300 nm gold were sputtered onto the back surface of the sample. The configuration of the four-probe measurement setup for measuring the I-V characteristic of the middle CNT TSV is illustrated in Fig. 4.8. To separate the contact resistances from the bulk resistivity, measurements were performed on carbon nanotube TSVs of three different heights. The current/voltage characteristics from these measurements are

shown in Fig. 4.8. Good ohmic contact is indicated by the linear relationships between measured currents and voltages. On the average, the resistances of the three CNT vias of different heights of 100 μm , 175 μm and 280 μm , were 0.15 Ω , 0.25 Ω , and 0.4 Ω , respectively. By plotting the calculated resistances as a function of via heights, as shown in Fig. 4.9, the contact resistance was found to be almost negligible (<1 m Ω). This is consistent with previous results published by Lim et al.[215], and could be explained by titanium, as compared to gold, having a work function closer to that of the CNTs, and a better wettability to the CNTs.

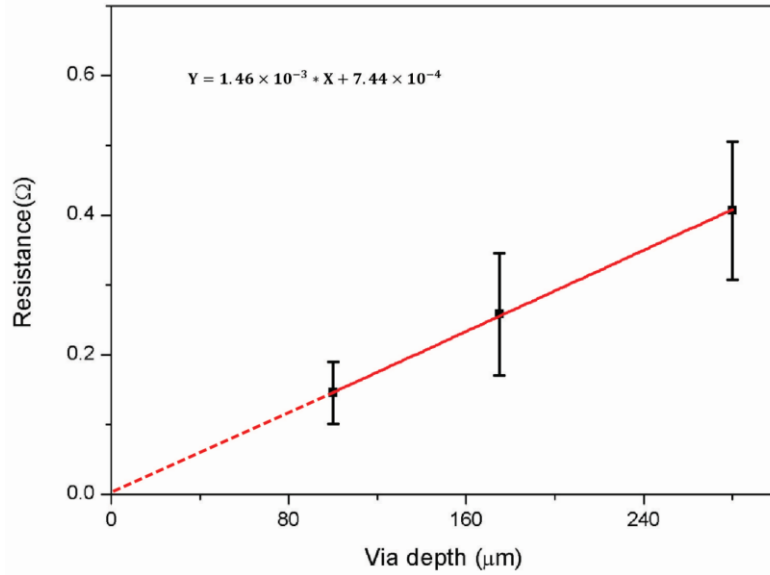


Fig. 4.9. Estimation of contact resistance based on resistances of different via depths.(From paper B)

4.3VA-CNT-Solder TSV for interconnect

Due to the difficulty to produce high quality CNT interconnects in a manufactory-friendly way [216], CNT-based interconnects have been suffering from relatively high electrical resistivity compared with conventional metal-based materials, i.e. Au, Cu, and SAC alloys. This section describes a fabrication process for a carbon nanotube (CNT)/Solder hybrid structure aiming to combine the merits of CNTs and solders.

Fig. 4.10 illustrates the fabrication process for the CNT/solder hybrid bump structure. Lithographically defined CNT moulds are grown by TCVD method up to hundreds of micrometer long. The CNT moulds are pre-densified before the solder spheres are filled. The densification process strengthens the pristine porous CNT forests and allows the CNTs to withstand the following solder filling and reflow process. After densification, the CNTs are sputter-coated with 10nm Ti/50nm Au layers for better wetting with the solder.

After that, the space inside the CNT moulds is filled up with SAC305 (96.5 % Sn, 3% Ag, and 0.5% Cu) solder spheres of around 10 μm in by simply sprinkling the spheres onto the sample. Excess spheres outside the hollow CNT moulds were shaken off the surface of the substrate. This CNT/Solder hybrid material is then reflowed. The reflow melts the small solder spheres into large single solder balls surrounded by densified CNT walls.

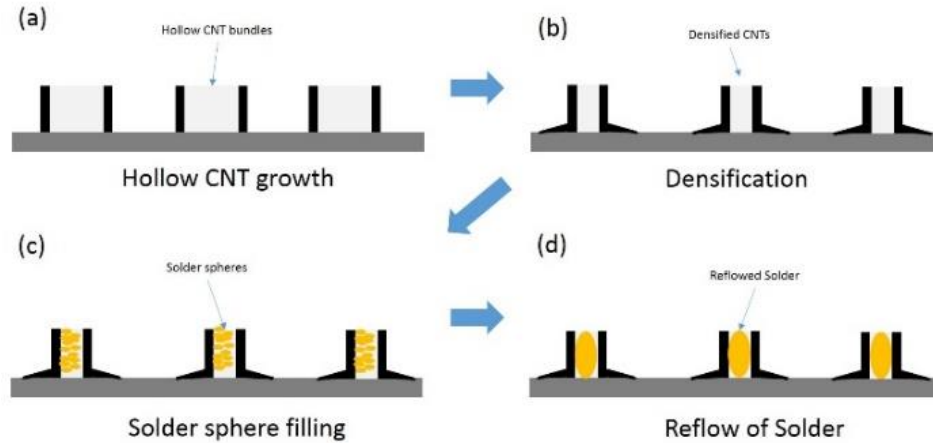


Fig. 4.10. Fabrication process for the CNT/Solder hybrid interconnect: (a) TCVD growth of hollow CNT bundles. (b) Densification of hollow CNT bundles. (c) Filling of solder sphere into CNT bundles. (d) Reflow of the solder spheres.

It is shown in Fig. 4.11 that after filling and reflowing the SAC spheres, the cylindrical CNT bundle was successfully filled with SAC solder. The diameter of the CNT mould after densification is around 200 μm and the thickness of the CNT wall is around 20 μm . The cross-section of the CNT mould after the solder filling is presented in Fig. 4.12. It is shown that the solder spheres were well suited inside the CNT mould. After the reflow process, the solder spheres melted down into a single solder ball. The densified CNT walls surrounding the solder ball remains intact after the whole processing including the rough polishing process. The highly porous, just grown, pristine CNT bundles [217] would not withstand the whole process unless densification process [218], [219] was made to make it strong enough. And the cross section picture of the reflowed solder spheres are shown in Fig. 4.12.

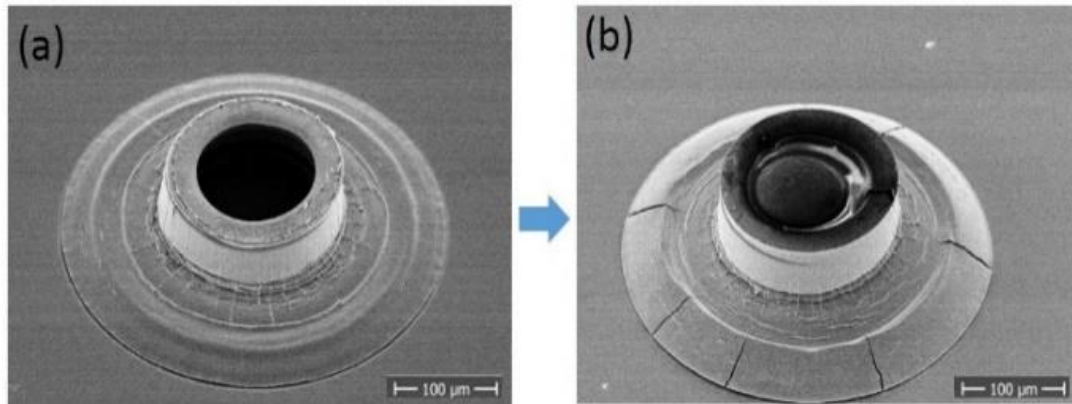


Fig. 4.11. (a) SEM picture of thermally grown and densified carbon nanotube mould with hollow structures. The space inside the hollow tube will be filled with Sn-Ag-Cu solder spheres. (b) SEM picture of densified CNT mould filled with SAC alloy sphere.

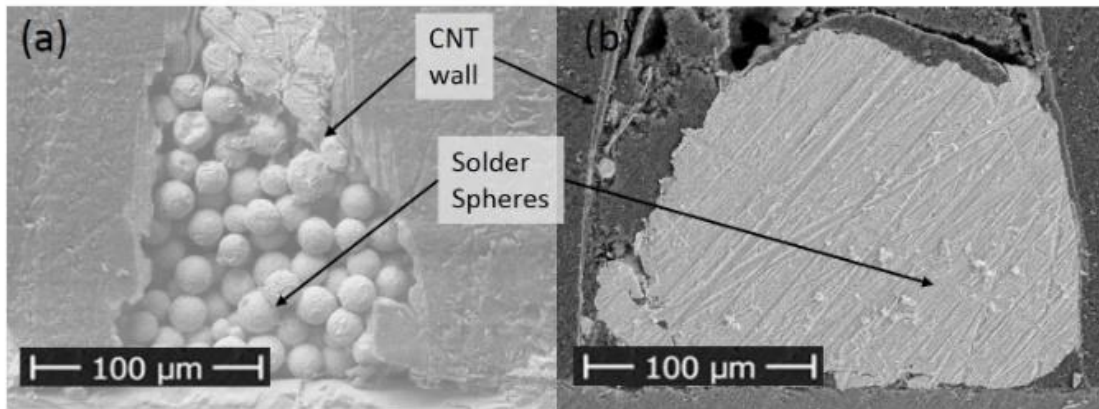


Fig. 4.12. SEM pictures of the cross section of (a) CNT/solder spheres before reflow. (b) CNT/solder sphere after reflow.

In order to study the electrical performance of the CNT/solder hybrid structure, four-probe measurement was carried out to characterize the DC resistance of such bump. Through the conducting indium substrate a direct current was applied on two of the bumps and the voltage drop on one bump was measured. The result of such a test is shown in Fig. 4.13 (b). As comparison, a densified and transferred hollow CNT bundle was also measured using the same method, and the result is presented in Fig. 4.13 (a). Both of the two measurements resulted in highly linear voltage-current dependency, which indicates good ohmic between the conducting materials. The resistance of the CNT bundle without solder filling is around 640 m Ω while the resistance of such a hybrid structure is around 100 m Ω . The resistance was reduced by almost 6 times with the addition of solder filling. It can be regarded as putting a solder resistor in parallel with the CNT bundles. In addition, the total resistance of such a hybrid structure can be approximated by:

$$\frac{1}{R_{total}} = \frac{1}{R_{CNT}} + \frac{1}{R_{solder}} \quad 4.1$$

It is clear that the solder filling greatly lower the resistance of such a CNT-based bump. However, due to the imperfect contact between the CNT, solder and the interfacing materials on the substrate, the measured total resistance has not matched that of a pure solder bump, where in this case should be around 60 mΩ if we approximate the bump as a cylinder with 200 μm in diameter and 150 μm in height.

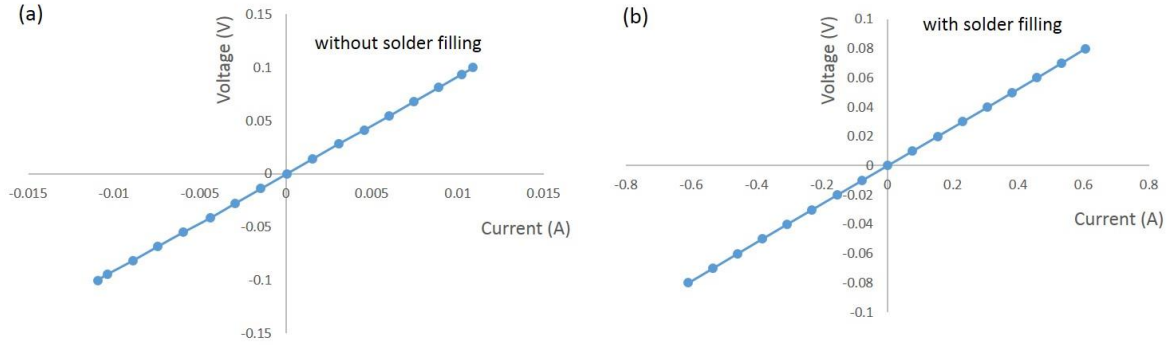


Fig. 4.13. (a) The I-V curve measured on one hollow CNT bundle without solder sphere filling. (b) The I-V curve measured on one sphere filled CNT/solder hybrid bump.

4.4 VA-CNT-Cu TSV for interconnect

According to the results of previous sections, the electrical resistivity of CNT TSVs is still several orders of magnitude higher than Cu TSVs due to their highly porous structure. Although vertically-aligned CNTs can be densified, the resistivity of the CNT TSVs is still two orders of magnitude higher than Cu [220][221]. For this reason, developing a novel composite TSV to address the current problems encountered by pure Cu or pure CNT TSV interconnections can potentially offer a significant breakthrough. A few works in the literature have reported that a CNT-Cu composite material could have several advantages over both pure Cu and densified CNTs. Molecular Dynamics simulation results predict that the addition of CNTs can dramatically decrease the skin effect of Cu [222] and has strong vdW interfacial bonding with Cu [223][224]. Subramanian et al [137] synthesize a novel CNT-Cu composite film using an electroplating method, where the film showed one hundred fold increase in ampacity when compared with Cu. However, this film was too thin to make a vertical interconnection through a silicon wafer. Feng et al [138] developed a fabrication method where Cu was electroplated through a tungsten seed layer onto as-grown CNTs inside a blind via to fabricate CNT-Cu TSV. However, the resistivity of this composite TSV was still two orders higher than Cu as only a limited amount of Cu plating occurred inside the as-grown CNTs. Additionally, the CNT growth temperature is too high for current device fabrication processes. Therefore, the main

challenge is to develop a novel process for synthesizing vertically-aligned CNT-Cu composites, which has the same order of magnitude resistivity as Cu and silicon-like CTE, for 3D-IC interconnect. In this section, a novel CNT-Cu composite TSV fabrication process was developed to address the problems encountered by current TSV technologies, as shown in Fig. 4.14.

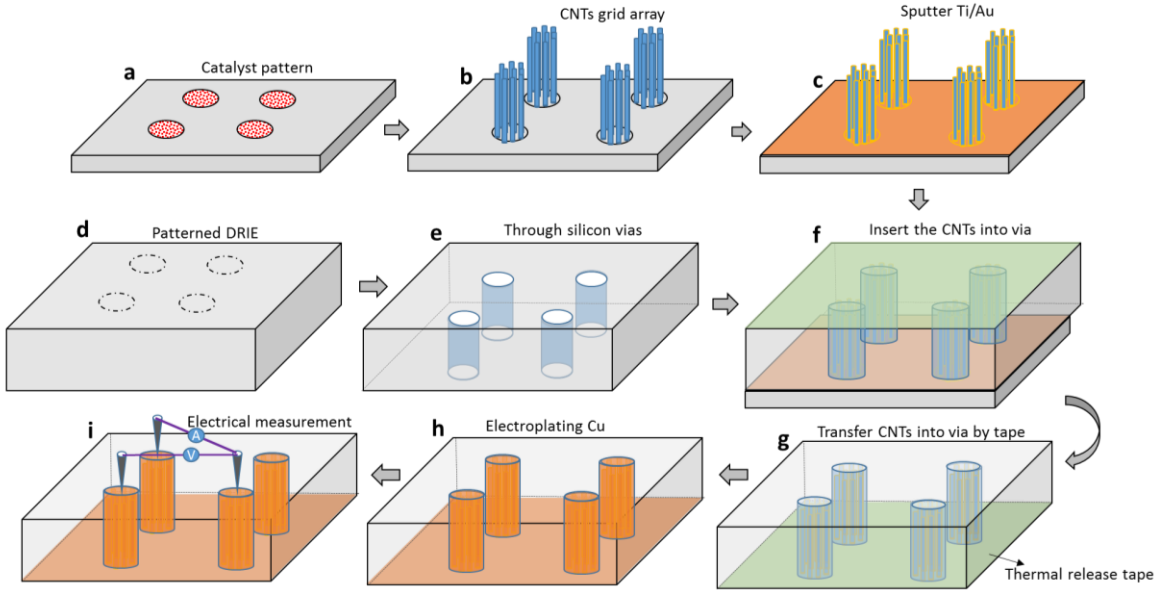


Fig. 4.14. Step-by-step schematic of the process for fabricating composite Cu-CNT TSVs. (a) Patterned catalysts are deposited by E-beam evaporation with the help of bi-layer photoresists. (b) CNTs array synthesized by using CVD at a growth temperature of 700°C. (c) Sputter 10nm Ti and 20nm Au onto the CNTs array. (d)(e) In parallel to these steps, the target Si wafer/chip with vias are prepared by deep reactive ion etching (DRIE). (f) Thermal release tape is attached onto the front surface of the target wafer/chip and CNTs array were transferred into the via and retained onto the adhesive tape using a flip chip bonder. (g) The donor wafer/chip is removed. (h) Cu is transferred into the vias by electroplating to form the composite CNT/Cu TSV. (i) Electrical performance was characterized by the four probe method. (From paper D)

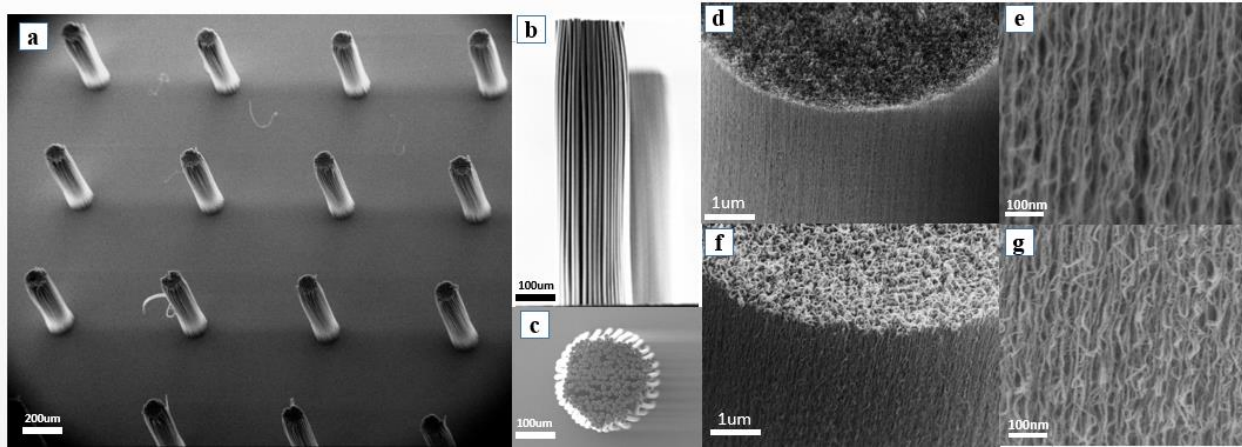
Morphology of CNTs and CNT-Cu material

Fig. 4.15. Aligned CNTs structure. (a) Uniform array of CNT bundles grown on the silicon chip; (b) One CNT bundle consisted of hundreds of small CNT bundles with an aspect ratio $\sim 300:1$; (c) Top view of one CNT bundle; (d,e) Zoom in image of one CNT bundle before sputtering Ti/Au; (f,g) Zoom in images of one CNT bundle after sputtering Ti/Au. (From paper D)

In order to fabricate vertically-aligned CNT-Cu TSV, the CVD method was used to synthesize high aspect ratio and aligned CNTs in a array. Scanning electron microscopy (SEM) images shown in Fig. 4.15 directly present the structure of CNTs at different processing stages. Fig. 4.15 (a) shows every CNT bundle and each CNT bundle consists of hundreds of individual CNTs, as shown in Fig. 4.15 (b). The aspect ratio of each individual CNTs can reach $\sim 300:1$. Importantly, the uniformity of CNTs array is good enough for interconnection applications. As shown from the top view in Fig. 4.15 (c), the high aspect ratio CNTs bundle looks straight and uniform in height, meaning that the transfer process was straight forward. The zoom in images given in Fig. 4.15 (d) and (e), demonstrate that every single CNT was vertically-aligned, which enhanced the electrical and thermal conductivity of TSV in the vertical direction [225]. The density of pristine CNTs calculated based on Fig. 4.15 (e) was in the order of 10^{11} cm^{-2} . Some papers reported that the density of a CNTs bundle can reach around 10^{12} cm^{-2} after densification [220][226]. However, the CNTs in this work were not densified as pristine CNTs were required for the nucleation steps inside of CNTs array afterwards. Fig. 4.15 (f) and (g) show the morphology of CNTs array after sputtering 10 nm Ti/20 nm Au. In contrast with CNTs before sputtering, slightly bigger diameter of CNTs and smaller gap between CNTs are observed in Fig. 4.15 (g), which indicate the Ti/Au layer continuously covers the surface of each individual CNT. Another important feature is that the overall structure of CNT array after the sputtering process remains porous, which means that Cu nucleation between the CNTs was possible. Here, the Ti layer

acts as a transition layer between carbon and the metals because it is more cohesive with respect to carbon than Au or Cu [227]. The gold layer is used as a seed layer for the later Cu electroplating process.

To realize the novel composite material with excellent electrical conductivity and mechanical performance simultaneously, a two-stage electroplating approach [137] was employed to plate the Cu into the CNTs array. Before electroplating, 10 nm Ti and 20 nm Au were sputtered respectively onto the surface of the samples as shown in Fig. 4.14 (c). There are two functions for this layer. First function is to enhance the wetting ability of CNTs to the Cu electroplating solution. Second function is to act as a conductive layer for the electroplating process. Then briefly, CNTs array was put in copper acetate (2.75 mM) electrolyte in acetonitrile under galvanostatic electric field to uniformly seed Cu into the CNT array. The sample was then put into the second aqueous electro-deposition plating setup to grow Cu seeds. For the first step, a very low current density of just 5 mA/cm², compared to standard 30 mA/cm², was used to ensure that Cu ion nucleation occurred slowly inside the CNT array. For the second step, the standard current density of 30 mA/cm² was used to complete the plating process. The fabrication of Cu-CNT composite TSVs with a uniform distribution of Cu was then completed.

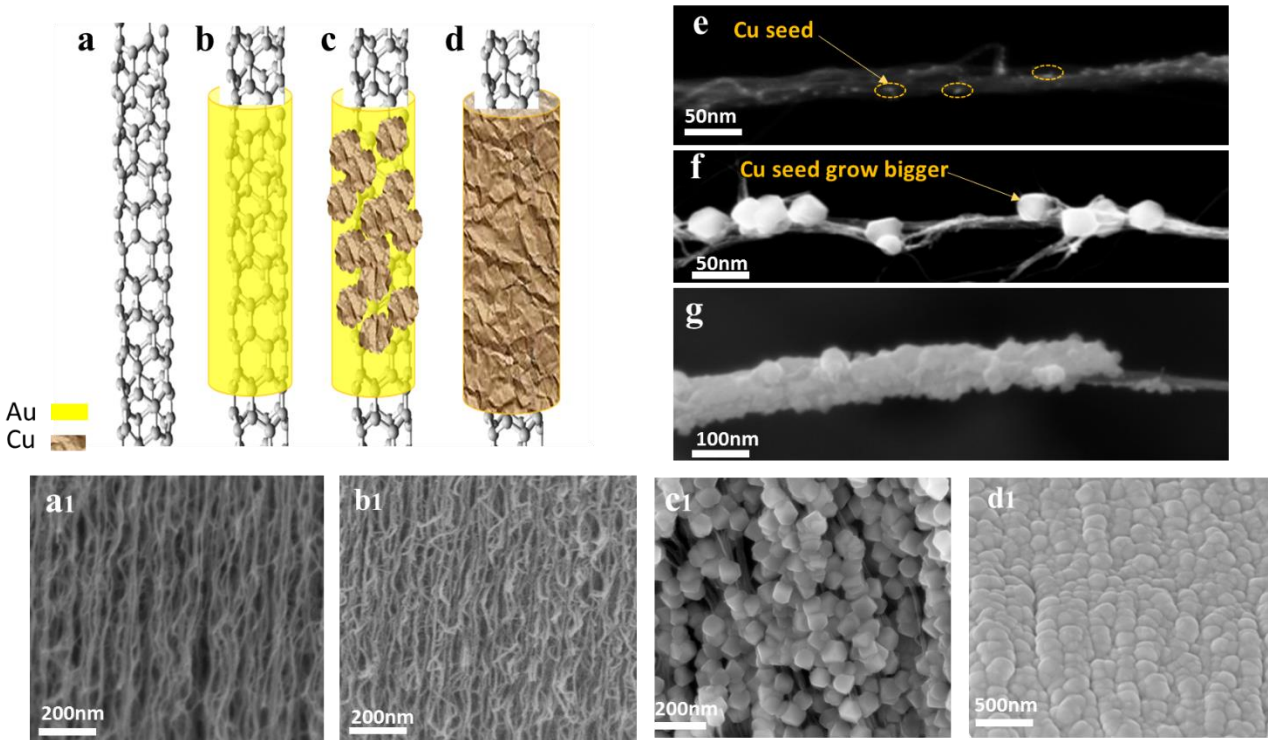


Fig. 4.16. (a-d). The schematic diagram from CNT to CNT-Cu composite; (a1-d1) Corresponding SEM images from aligned CNTs to CNT-Cu composite; (e) The surface morphology of CNTs in the early stage of electroplating; (f) Cu nucleating surrounding CNT in the second stage of electroplating. (g) Cu polycrystals tightly bonded with the CNT. (From paper D)

The different processing statuses of CNTs during electroplating are shown in Fig. 4.16. In the preliminary stage, there are many white dots appearing on the surface of CNTs as shown in Fig. 4.16 (e). This indicates that several Cu seeds have nucleated on the CNTs. Fig. 4.16 (f) shows that the seed gradually grew from 2-3nm to 50-60nm during the process, and a Cu crystal tightly intertwines each CNT through vdWs interfacial force [224]. This nucleation process can also be observed in the aligned CNTs as shown in Fig. 4.16 (c1). The structure looks like many chaplets where Cu crystals attached to the aligned CNTs, which illustrates that Cu was uniformly distributed along the aligned CNTs array. In Fig. 4.16 (d), polycrystalline Cu totally covers the whole CNT giving the composite nanowire a high conductivity capability. Corresponding to the schematic illustration of Fig. 4.16 (a-d), Fig. 4.16 (a1-d1) presents the different structure of the aligned CNTs array at each nucleation step in fabricating the CNT-Cu composite. As shown in Fig. 4.16 (d1), the coalesced polycrystalline Cu was successfully bonded to align CNTs resulting in stronger CNTs with a lower electronic resistance. The final CNTs/Cu composite structure seemed to consist of millions of composite nanowires as shown in Fig. 4.16 (d1). The whole structure becomes very condensed due to the electrostatic force between Cu crystal lattices.

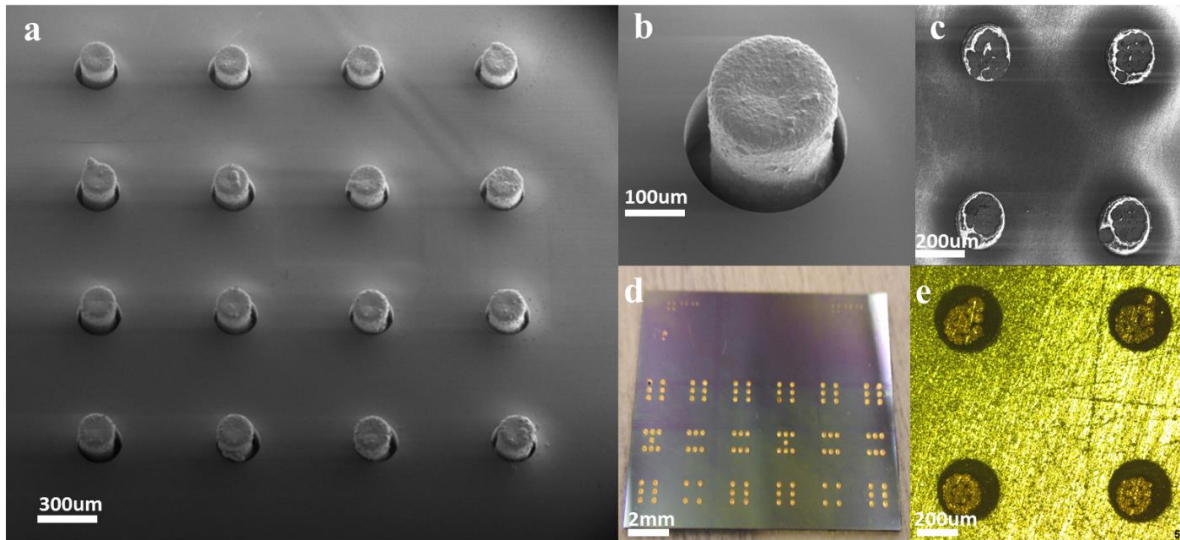
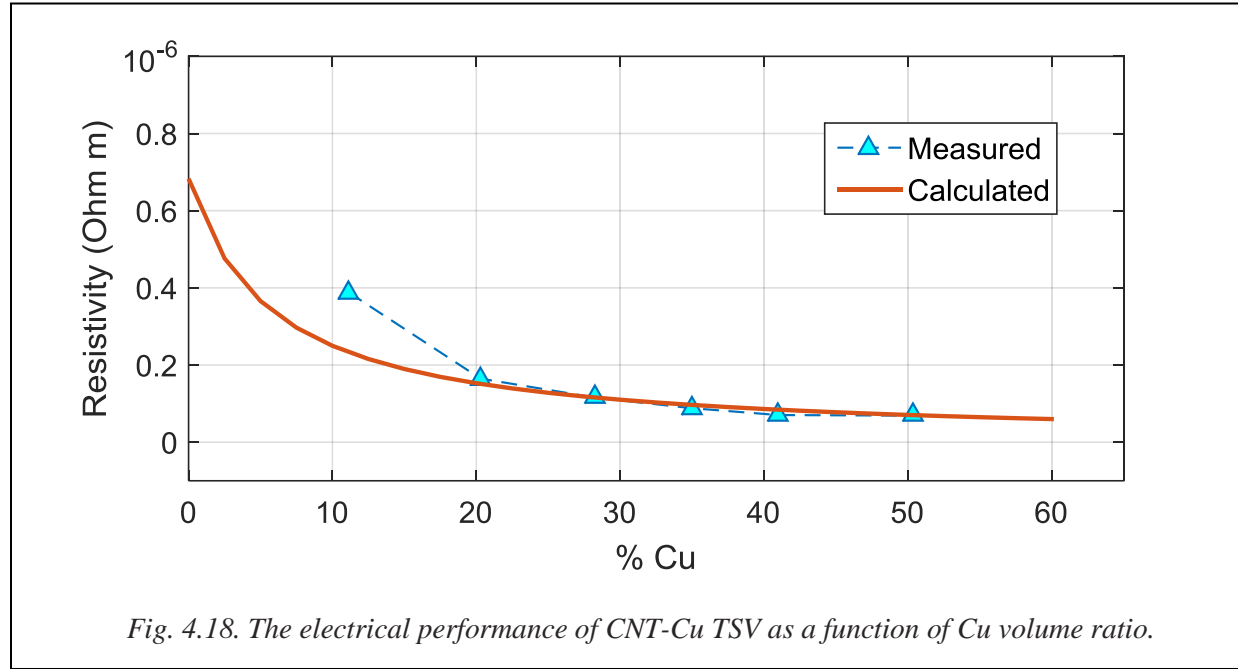


Fig. 4.17. (a) CNT-Cu composite structures inside the silicon vias; (b) Zoom in image of a CNT-Cu composite in the via; (c) the surface topography of CNT-Cu composite TSVs after polishing; (d) The completed test sample with CNT-Cu TSVs; (e) the optical microscope image at top surface topography of CNT-Cu composite TSVs after polishing. (From paper D)

The CNT-Cu bundles are assembled into the via openings using a flip-chip bonder. The situation after CNT transfer is shown in Fig. 4.17 (a), where the CNT-Cu arrays show high uniformity and high filling ratio. After copper electroplating, the CNTs still keep a vertically-aligned shape, as demonstrated in Fig. 4.17 (b),

which is important for obtaining a high electrical conductivity in the vertical direction. Through polishing the TSVs, Fig. 4.17 (c) and (e) show the on-site TSV status of the CNTs-Cu composite. The cross-sectional Fig. 4.17 (e), with a uniform copper colour distribution in the TSV, demonstrated that the Cu had fully penetrated the CNT array. A completed test sample is shown in Fig. 4.17 (d), where there were several tens of CNT-Cu TSVs in the $2 \times 2 \text{ cm}^2$ chip ready for electrical testing.

Performance evaluation of CNT-Cu TSV



The electrical performance of these composite TSVs with respect to different copper volume ratios is shown in Fig. 4.18, where the copper volume ratio is a function of the electroplating time. Initially, both the resistance and the resistivity decreased sharply as the volume ratio of copper increased. However, as more copper was electroplated into the structure, the trend of the resistance and resistivity of the composite TSV levelled off. The resistivity stabilized between 40% and 50% of its initial value, while the resistance decreased only slightly. This suggests that most of the copper was already deposited within the porous CNT bundles during the initial electroplating stage, thereby contributing to the sharp initial decrease. At a certain point, in this case at about 35% Cu volume ratio, further electrodeposition appears to coat only the outside of the CNT bundles, indicating that there will only be a limited improvement in the electrical conductance of the composite TSV [17]. In other words, the high concentrations of free electrons are mostly from the electrodeposited copper inside the CNT bundle. Correspondingly, CNTs offer a high mobility conductance channel to transport these free electrons with weaker scattering than copper [228]. The suggested composite

enhancement mechanism potentially explains why the electrical conductivity is of the same order of magnitude as for pure copper. But also, the potential for a localized charge exchange between the CNTs and the copper surface, raising the potential barrier at the interface, has the net effect of reducing the conductance with respect to pure copper [229]. In order to rationalize the experimental results, a theoretical model was built to analyze the results. As shown in Fig. 4.18, the theoretical model closely matches the experimental results. The difference between model and data for low copper concentrations can be explained by two concurring effects: i) the probability of copper is yet fully covering the CNT TSVs from top to bottom, ii) the mean free path of a CNT embedded in dense bundles being shorter than that of single CNTs due to them being in contact, as well as crossing and overlapping. The last point also applies to CNTs with no copper coverage (0%) and explains why the resistivity usually encountered in experiments are higher than expected from numerical simulations [31].

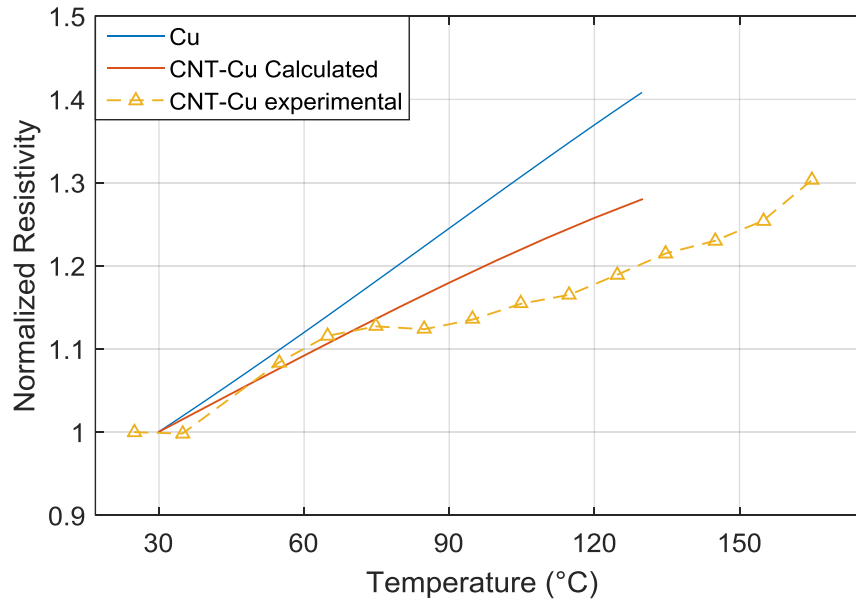


Fig. 4.19. Normalized Resistivity change with increasing temperature. (From paper D)

In general, the resistance of metals shows a strong dependence on temperature due to the random thermal motion of lattice atoms. The temperature coefficient of resistance (TCR) of copper at room temperature is about 3.9 %/°C [230], indicating that pure copper TSVs in high power applications will have increased power consumption due to a significant increase in the resistance. Fortunately, CNT-Cu composite TSVs show more stable performance with increasing temperature compared with pure copper. As shown in Fig. 4.19, the resistance of CNT-Cu TSVs increases less for increasing temperatures than for resistance of pure

copper for temperatures above 25°C, and in particular for temperatures above 50°C. The experimental results show good agreement with the theoretical model described in section S2 of the supplementary information. The gap between simulation and experiments at temperatures above 50°C can possibly be attributed to thermal strain in the composite nanomaterial. Based on the results in figure 6, the TCR of a CNT-Cu composite TSV for temperatures above 50°C was estimated to 2.1 %/°C, about half of that for pure Cu. This improvement is likely attributed to the CNT suppressing the increased self-motion of charged metallic atoms, particularly at higher temperatures [231], because the atomic diffusion activation energy of copper in CNT-Cu composites becomes larger than usual [137]. Therefore the scattering rate between electrons and charged particles decreases accordingly and, hence, result in a TCR less than that of copper.

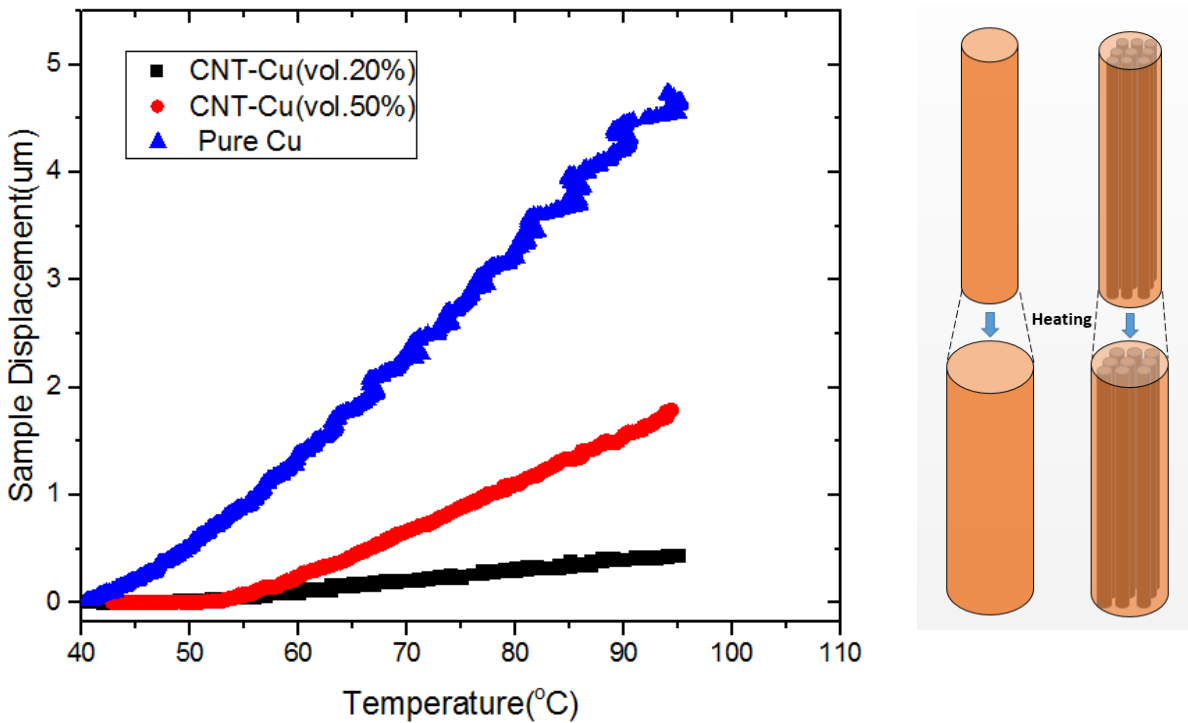
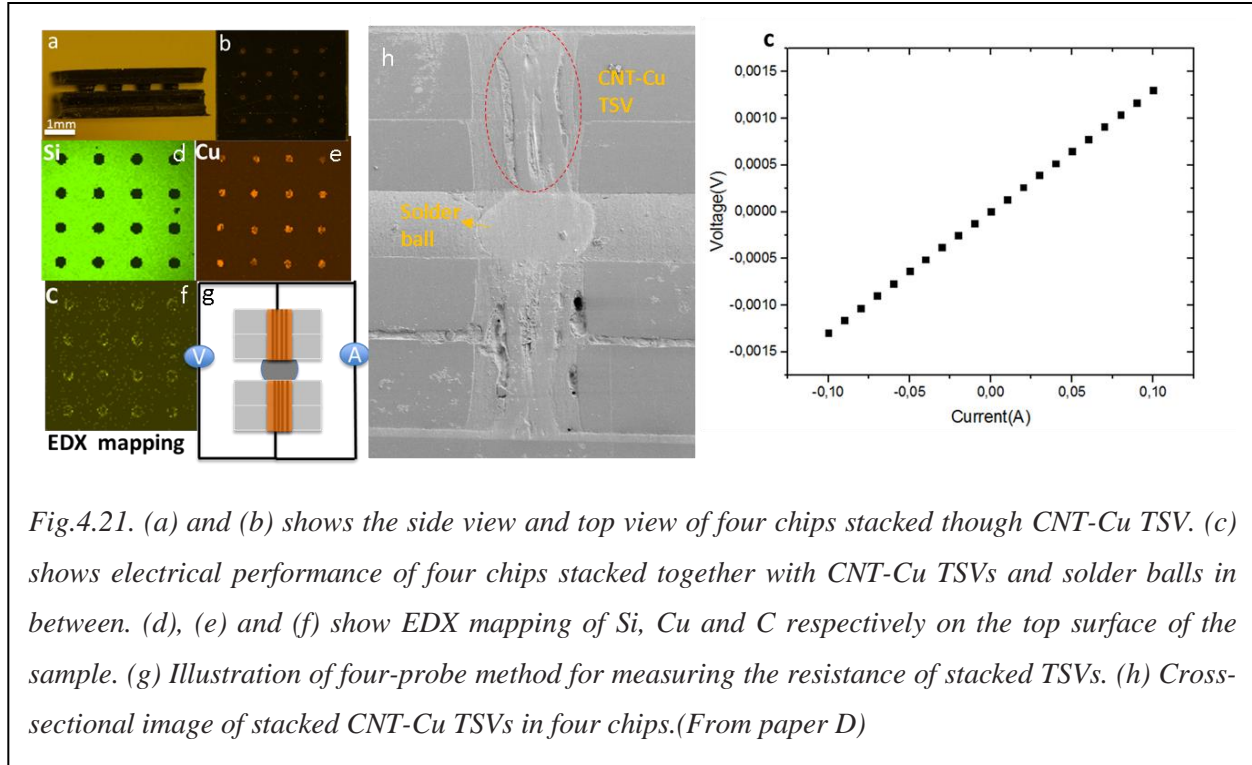


Fig. 4.20. Thermal expansion performance of CNT-Cu and pure-Cu TSVs at different temperatures.

Thermal expansion of TSVs is another key factor to be considered for the reliability of microelectronic devices. Fig. 4.20 shows the thermal expansion of the CNT-Cu composite at 20 and 50 vol% of copper, as well as for 100% pure copper. The thermal expansion of these three materials were measured by TMA displacement over a temperature range from 40°C to 100°C. The CNT-Cu (20 vol%) composite TSV expanded by a displacement of 0.5 μm, while the composite TSV with 50 vol% copper had expanded by 1.6 μm. The results obtained for CNT-Cu TSVs compare favourably with respect to pure Cu TSVs, which expanded by about 5 μm. Effectively, this indicates CTE reductions corresponding to 65% and 90% for nanocomposites with 20 and 50 vol% of copper, respectively. The CNTs seemingly absorbed the thermal expansion of the sample during heating, indicating that the CNT arrays can effectively restrain the thermal

expansion of the copper due to the flexibility of the CNTs [31]. On the other hand, the CNTs array isolated the continuous arrangement of copper grains, thereby effectively blocking any thermal movement of the copper lattice chain at high temperatures, which possibly weakens the thermal motion amplitude of the copper crystals. This would result in a reduction in the thermal expansion of the electroplated copper.

To demonstrate the applicability of CNT-Cu TSVs in microelectronics packaging, 2x2 chips connected by CNT-Cu TSVs were stacked together with solder balls, as shown in Fig 4.21(a). Fig 4.21(b) shows the top surface of the same stacked sample after surface polishing. Energy dispersive X-ray spectroscopy (EDX)



mapping of the top surface showed that copper (shown in orange) was evenly distributed across all composite vias. Fig 4.21 (h) shows a cross-sectional view of the inner structure of stacked composite TSVs after polishing. There is a good soldering joint between TSV and solder ball and a considerable amount of copper can penetrate the CNT bundles. The I-V characteristics in Fig 4.21 (c), shows good linearity after a series of assembly processes including reflow soldering. Based on calculations from the I-V curve, the resistance and resistivity of the stacked structure were determined as 12 mΩ and $4.19 \times 10^{-7} \Omega \cdot \text{m}$, respectively. Considering the solder ball resistance and the interfacial resistance between the TSV and the solder ball, the electrical performance is comparable with that of pure copper TSVs. In addition, the excellent electrical performance of the stacked sample demonstrates the strong applicability of this composite TSV for future high density 3D stacking of IC devices.

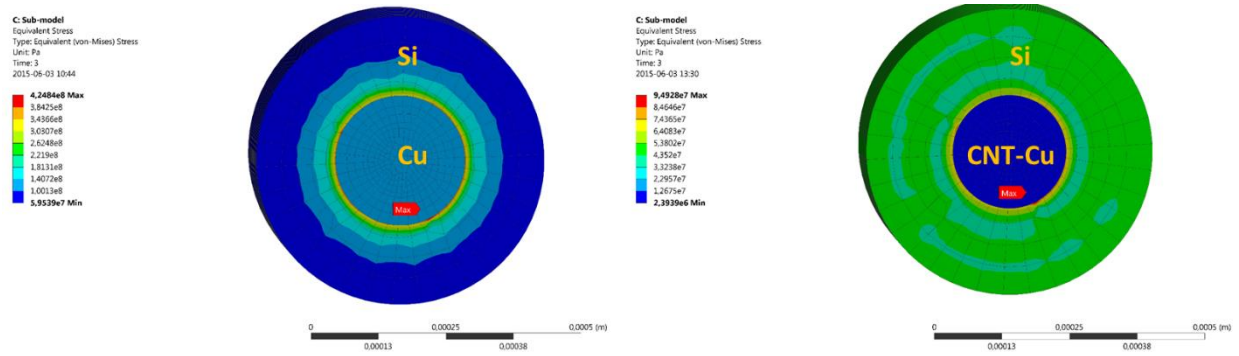


Fig. 4.22. Maximum stress comparison between CNT-Cu TSVs and Cu TSVs after two thermal cycles from -40°C to 115°C . (From paper D)

To demonstrate the potential improvements in reliability of a CNT-Cu TSV, a finite element simulation (ANSYS 16.0) was employed to estimate the stress distribution on a single layer of the test structure after two thermal cycles between -40°C and 115°C . The finite element model structure contained a 4×4 array of TSVs in a silicon chip, with a geometry similar to the one shown in Fig. 4.22 (a). The CTE and stress/strain measurements shown earlier in this work for a CNT/Cu composite with 20 vol% of copper were used as input values to the simulation model. The simulation results shown in Fig. 4.22 indicate that the maximum stress occurs at the TSV/silicon interface and was found to significantly decrease from 424.84 MPa for a pure copper TSV model to 94.93 MPa for a 20 vol% CNT/Cu composite TSV model. These findings suggest that CNT-Cu composite TSVs could potentially result in a massive improvement in reliability.

In summary, processing steps for fabricating a novel CNT-Cu composite TSV was developed for interconnection in 3D integrated device. This composite TSV combined Cu-like high electrical conductivity and CNT-like low CTE together. Moreover, this composite TSV also had a TCR that is half that of pure Cu. Shear testing indicated that the composite structure is very robust, with the CNTs adding extra mechanical support. A finite element model simulated the interfacial stress between TSV and silicon after two thermal cycles, where it shows a dramatic decrease in the stress on the silicon. As the material is a composite, the vol% of Cu has an impact on thermal, mechanical and electrical performance, meaning that designing the optimum structure is a matter of getting the best compromise between these competing needs. This composite TSV one of a selected group of materials that offers low resistivity and low CTE, perfectly suiting 3D interconnection applications in microelectronics devices.

4.5 Flexible TSV for interconnect

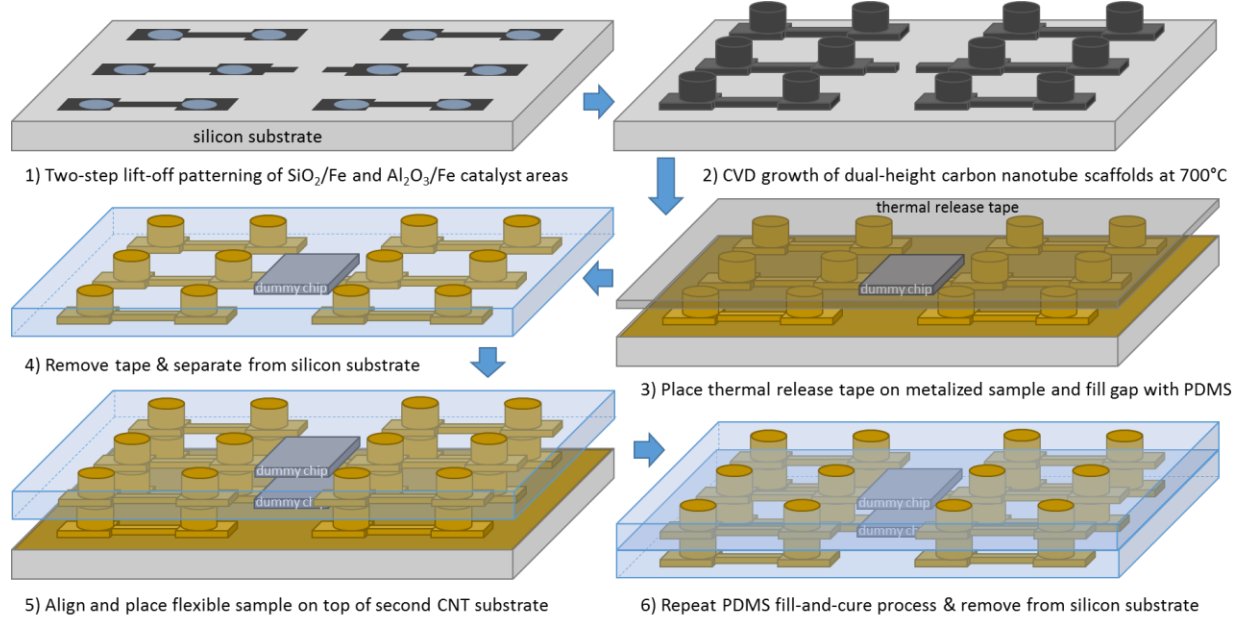
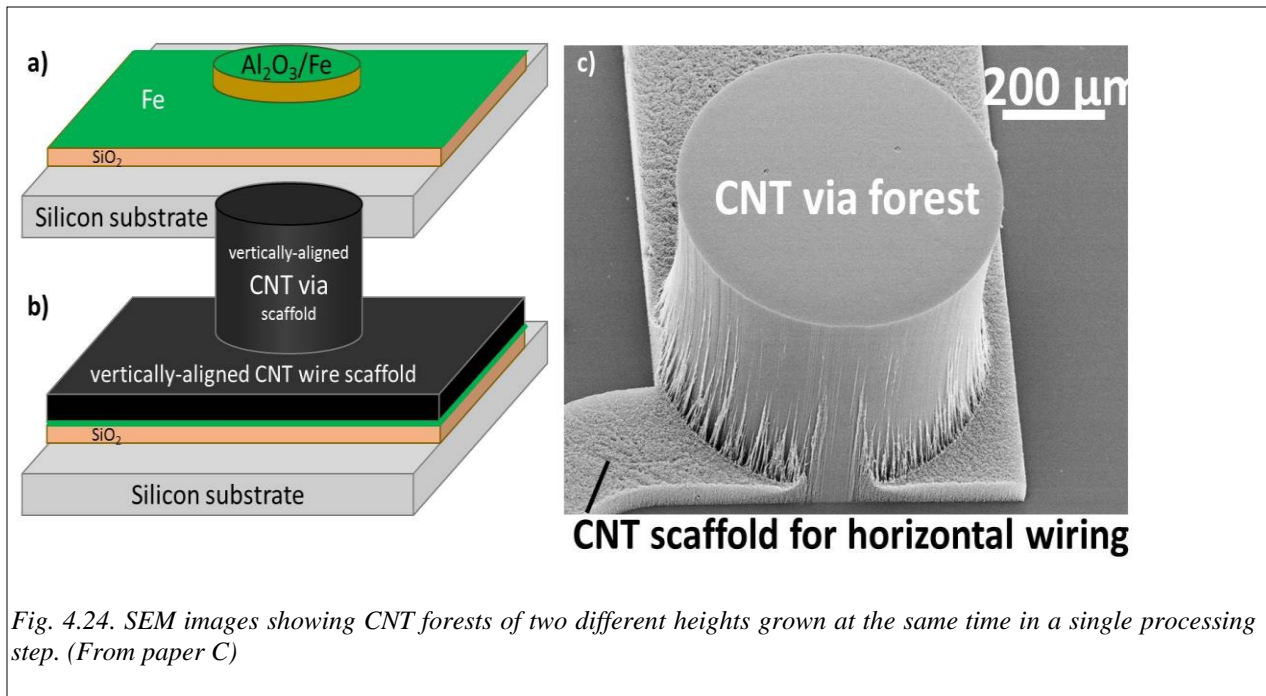


Fig. 4.23. Illustrations of the process flow for fabrication of the proposed 3D CNT scaffold-based interconnect. (From paper C)

In this section, the fabrication of the flexible and stackable 3D interconnect system is described. In this work, I mainly focused on investigating the CNT growth. An overview summary of the process flow is shown in Fig. 4.23. Firstly, 30 nm SiO_2 underlayer and 1 nm Fe catalyst, defining the horizontal wire patterns, were evaporated onto a silicon substrate. A second pattern defining the position of the vertical vias was fabricated with evaporated Al_2O_3 and Fe of 10 nm and 1 nm thick, respectively (Fig 4.23(1)). The CNT scaffolds were synthesized by thermal chemical vapor deposition method, at a maximum temperature of 700°C with C_2H_2 and H_2 as the gas feedstock [233]. The use of different underlayer materials (Al_2O_3 and SiO_2) resulted in CNT growth of different heights [234], hence separating the horizontal and vertical interconnects (Fig. 4.23(2)). This is the key feature of this work, which enabled the formation of both vertical, and horizontal interconnects at the same time. A multi-metal layer consisting of Ti and Au was sputtered onto the whole sample (Fig. 4.23(3)). The Ti layer served as contact and adhesion layer between the CNTs and the Au layer because of its reported high quality wetting to CNTs [235]. This multi-metal layer served as the main conductor for the electrons. Next, the sample was placed on a thermal release tape, with the tips of the vertical CNT vias in contact with the tape. PDMS solutions was then applied along the edges between the two substrates (Fig. 4.23(4)). The sample was then placed in a vacuum chamber at 10 mbar for 30 minutes, during which the PDMS was de-bubbled and driven by capillary force to fill the gap between the two substrates. Then the sample was heated up to 80°C to cure the PDMS, and then to 150°C to release the thermal tape. Finally, the CNT-growth substrate and the thermal tape were both removed,



leaving the PDMS layer consisting of both horizontal and vertical wire paths (Fig. 4.23(4)). Furthermore, the stacking of the layers was done by aligning and placing a second CNT-carrying silicon substrate onto the as-fabricated first layer interconnect (Fig. 4.23(5)). It is optional to use conductive adhesives for bonding, yet direct bonding is also possible as the CNT bundles are axially elastic. The PDMS flow-and-cure process was repeated to form a double layered 3D metal-CNT interconnect network within the completed PDMS substrate as shown in Fig. 4.23(6).

A SEM image showing the resulting vertically aligned multi-walled CNT forests of two different heights after growth, but before PDMS filling, was shown in Fig. 4.24 (c). The empty space provided by the 300 μm height difference between the two CNT forests provides room for thinned silicon chips while still leaving enough space for insulating the stacked interconnect layers from each other. A stacked flexible double-layer PDMS-embedded system with integrated silicon chips is shown in Fig. 4.25 (a). This figure also contains a cross-sectional inset showing two stacked CNT-metal via (bottom right).

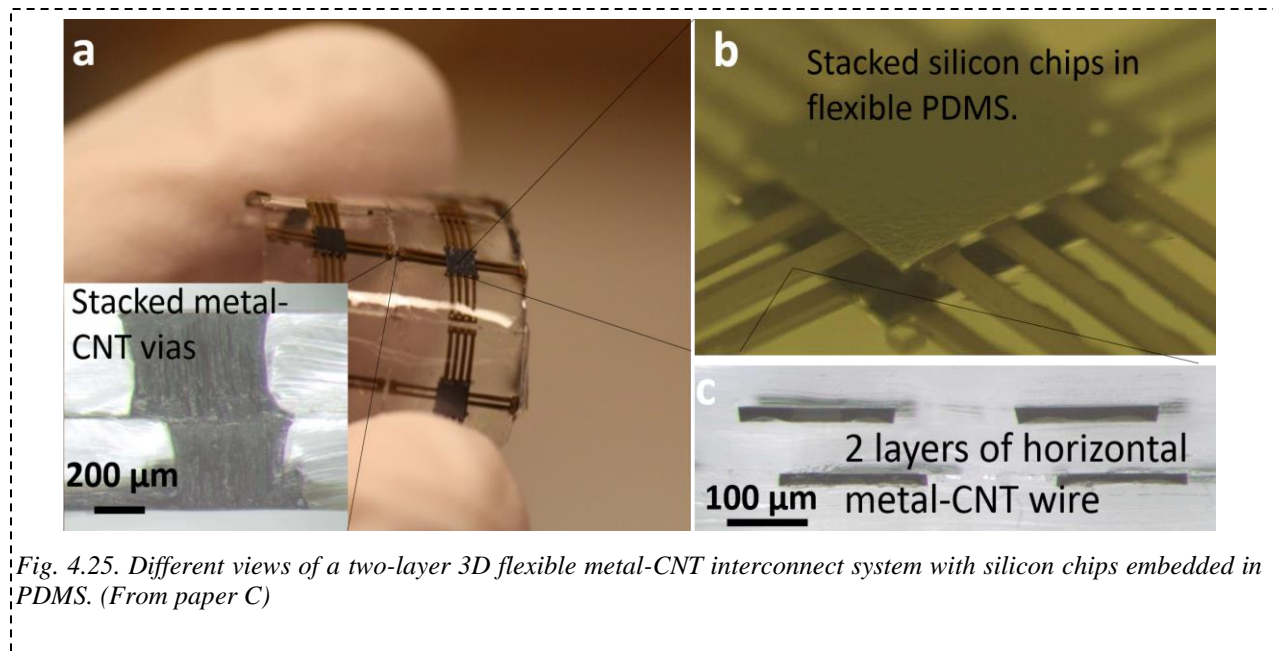


Fig. 4.25. Different views of a two-layer 3D flexible metal-CNT interconnect system with silicon chips embedded in PDMS. (From paper C)

As shown in Fig. 4.26 (a) linear IV curves were obtained indicating good ohmic contacts. The resistance of pristine CNT test structures before metallization was found to be 5 k Ω . Such high resistances are expected since the vertically aligned carbon nanotubes are not oriented in the direction of the current flow; hence their conductivity in the wire direction is quite low. However, their only purpose is to serve as flexible scaffolds for the horizontal metal wires, not to serve as conductors. For test structures covered with a 200 nm gold layer on top of the 20 nm titanium adhesion layer, a resistance of 30 Ω ($\pm 10\%$) was measured. Since the resistance of the vias themselves was found to be less than one ohm [21], the wire resistance corresponds to a sheet resistivity of 0.6 Ω /square which is not an unreasonable value. Due to the surface roughness of the CNT scaffolds on which the metal conductor was deposited, the sheet resistivity is not as low as for a similar gold wire deposited on the smooth surface of a SiO₂-capped silicon wafer. However, some of the deficiency caused by the surface roughness of the gold film is alleviated by the metalized sidewalls of the CNT scaffolds contributing to the conductance of the wire, thereby making the cross-sectional area of the 400 μ m wide horizontal wire 50% larger than indicated by its footprint. Considering the influence of the metalized sidewalls, the resistance measured corresponds to a resistivity of 18 $\mu\Omega$ -cm, a resistivity that is less than one order of magnitude larger than that of bulk gold (2.2 $\mu\Omega$ -cm). The conductance of the test structures as a function of the gold film thickness is shown in Fig. 4.26 (b). The linear trendline indicates that the conductance of the test structure increases linearly with its cross-sectional area.

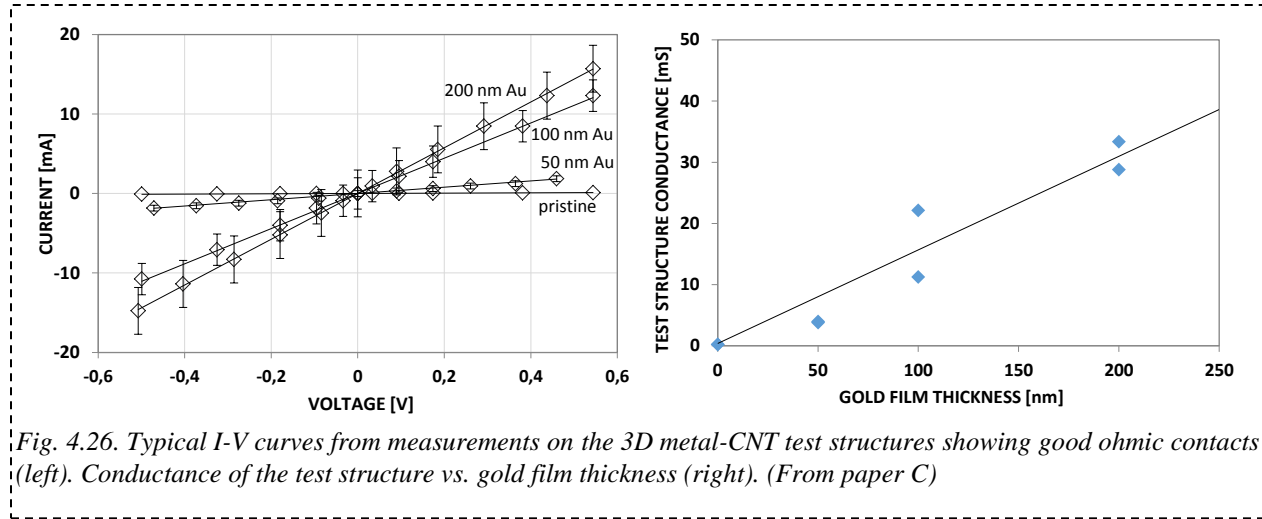


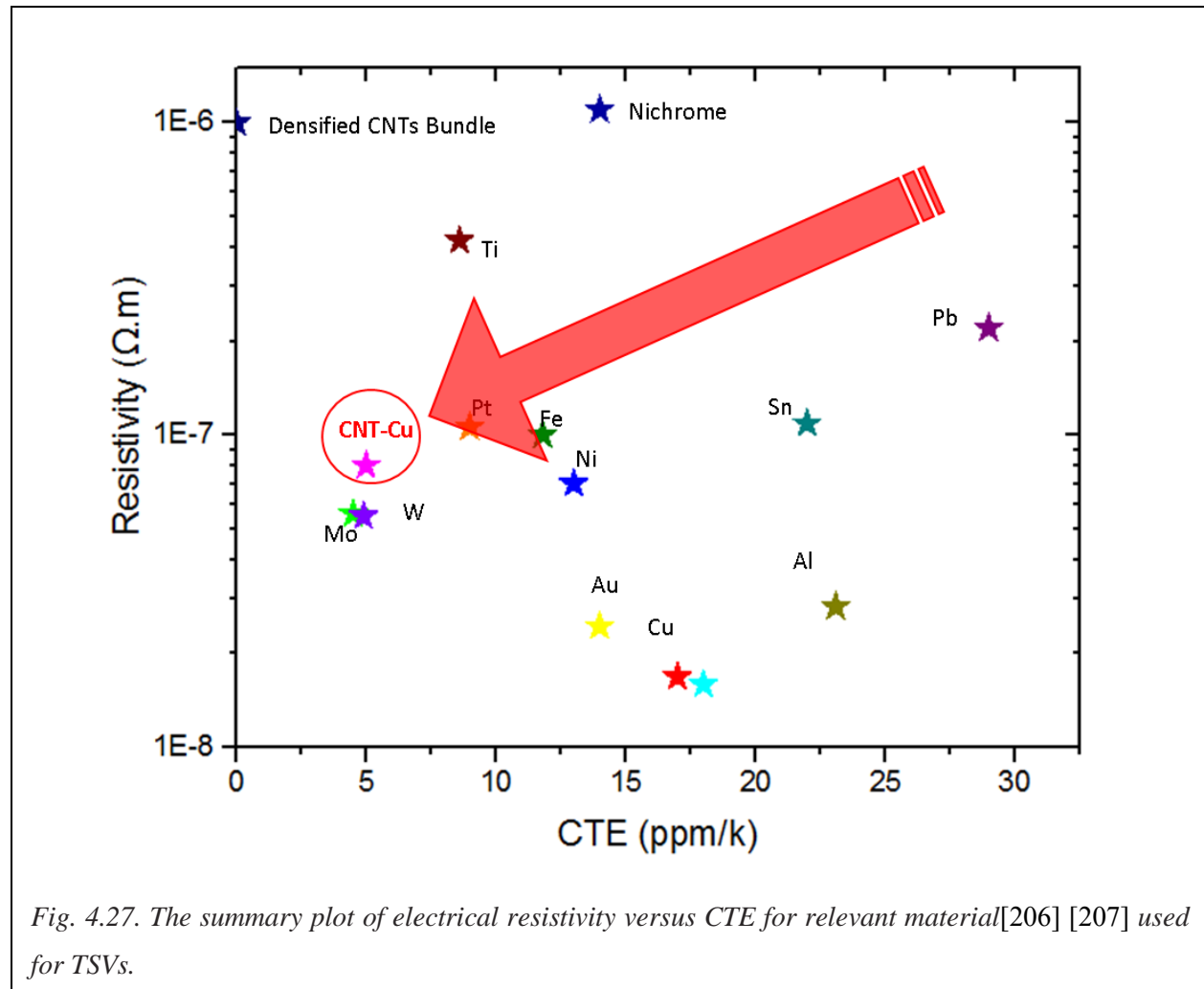
Fig. 4.26. Typical I-V curves from measurements on the 3D metal-CNT test structures showing good ohmic contacts (left). Conductance of the test structure vs. gold film thickness (right). (From paper C)

4.6 Summary and discussion

This chapter demonstrated different kinds of CNT based TSVs, which were VA-CNT TSV, VA-CNT-Solder TSV, VA-CNT-Cu TSV and flexible CNT TSV respectively. Among these four types of TSVs, the resistivity of flexible CNT TSV is the largest due to that its more complicated fabrication process possibly caused more defects of CNTs than others. However, it is the most flexible to fit wearable electronics in the future based on the fact that the CTE of CNT is almost zero at room temperature [236]. In contrast, VA-CNT-Solder is six times lower than VA-CNTs in term of resistivity, while its CTE might be the worst in these three kinds of TSV because of the structure of solder-filling hollow CNTs. The SAC solder after reflow process will become very stiff. However, CNT-Solder TSV manufacture process is much simpler than VA-CNT-Cu TSV fabrication process. Comparatively speaking, VA-CNT-Cu TSV possessed the best electrical conductivity, showing the same order as pure copper. Additionally, the CTE of VA-CNT-Cu TSV is closed to that of Si. Moreover, Subramanian et al reported that CNT-Cu composite material showed excellent ampacity [137]. Nevertheless, the fabrication process might be relatively more complicated than other three kinds of TSV. The specific value for every material is shown in table 4.1.

Table 4.1: The size, Resistance and Resistivity of these three CNT based material.

TSV type	VA-CNT	VA-CNT-Solder	VA-CNT-Cu	Flexible CNT TSV
Size(Diameter)	160 μm	200 μm	200 μm	600 μm
Resistance	$\sim 400 \text{ m}\Omega$	$\sim 100 \text{ m}\Omega$	$\sim 1 \text{ m}\Omega$	$\sim 1 \Omega$
Resistivity	$\sim 2\text{e}^{-5} \Omega\text{m}$	$\sim 5\text{e}^{-6} \Omega\text{m}$	$\sim 8\text{e}^{-8} \Omega\text{m}$	$\sim 3.7\text{e}^{-4} \Omega\text{m}$



For comparison, a summary of different filling materials [33–36] is given in Fig. 4.27 providing an overall view of the TSV field. As shown in figure 10, the CNT–Cu composite material and tungsten are occupying unique positions with low resistivity and CTEs. However, tungsten is very costly, and only used as via plugs between on-chip interconnect layers [241]. Overall, the CNT-Cu material represents the best combination of properties with high electronic conductivity and low CTEs for TSV interconnects.

Chapter 5

5. Carbon hybrid supercapacitors

Carbon based materials including activated carbon, carbon nanotube (CNT) and graphene, have been widely investigated in supercapacitors owing to their excellent physical and chemical properties. Activated carbon has a large surface area but low electrical conductivity due to its isolated carbon atoms structure. Owing to low cost, activated carbon is the most used as electrode for supercapacitors. However, considering its inherent structure drawback, its applications in high power density supercapacitors usually output a low specific capacitance per area [242], [243], which directly leads to limited capability in high power density supercapacitors. Compared to activated carbon, CNT and graphene both have super high electrical conductivity and excellent surface area, which has been reported by many reports [47], [48], [107], [244], [245]. However, if we separately use CNT and graphene respectively as electrode, their advantages will not fully be demonstrated due to two facts. One is that CNT network cannot perform a very high electricity as we expected in every individual CNT due to too many contact resistance existed in the CNT network. Another one is that graphene sheets usually tend to restack together in the fabrication process due to strong van der Waals interaction [246], which will lead to very limited surface area. Considering these two points, many researchers are trying to mix CNT and graphene together to use as electrode. For instance, some researchers used CNTs as effective spacers between graphene layers to improve capacitance [247]–[250]. X. Cui et al. [251] fabricated a graphene oxide and CNT composite film electrode for supercapacitors, which exhibited good capacitance. Z. Zhang et al. [252] combined CNTs with graphene nanosheets together to obtain 3D nanostructure with a promising surface area of $903 \text{ m}^2\text{g}^{-1}$. However, it seems seldom research on aligned CNTs grown on continuous graphene film with C-C covalent bond, which can significantly increase electrical conductivity compared to previous research work on this field. In this chapter, a controllably aligned CNTs and graphene-based film hybrid structure (CNT-G) was synthesized to be used as supercapacitors electrodes. This pillared CNT-G hybrid material was obtained using the same method as mentioned in chapter 3 to grow CNTs on the surface of graphene based film to form covalent bond. The atomic structure of covalent bond was characterized by transmission electron microscopy (TEM). The performance of CNT-G electrode supercapacitors was investigated. For demonstrating potential flexible supercapacitor application by CNT-G material, the capacitive behavior was also studied using solid electrolyte.

5.1 Carbon hybrid material characterization

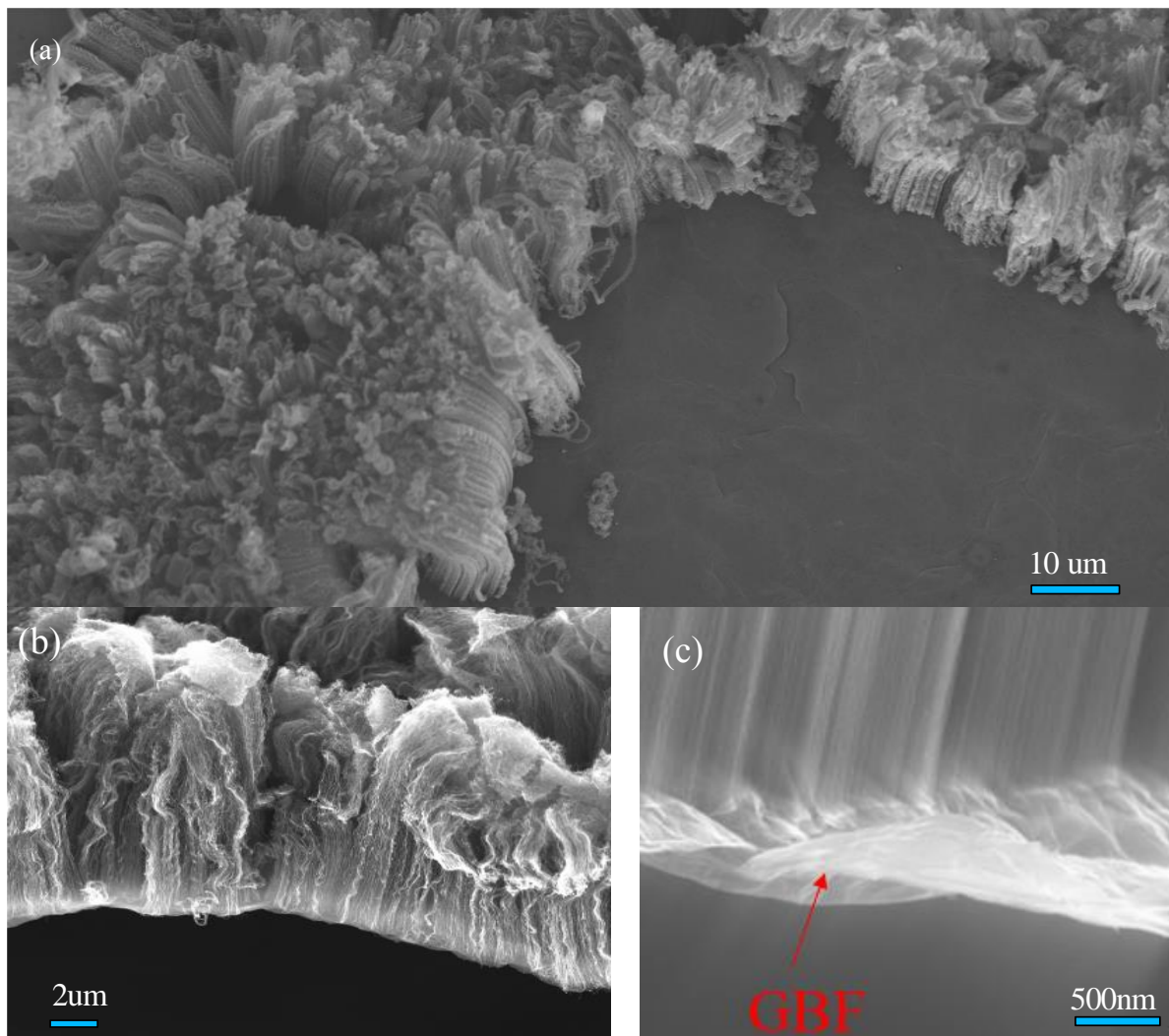


Fig. 5.1. SEM images of CNT-G hybrid materials. (a) The CNT-G hybrid structure was captured from top view. (b) The morphology of CNT-G hybrid material from cross-section view was showed in this image. (c) After zooming in small part of image (b), aligned CNTs grown on the thin graphene based film was clearly characterized.

Fig. 5.1(a) shows the surface morphology of CNT-G hybrid material after performing CNT growth from top view. We intentionally choose a region with both CNT growth part and only graphene based film part to conveniently make a comparison. There are some wrinkles formed on the surface, which is possibly attributed to solvent surface tension during fabrication and that graphene tends to minimize the total free energy[253]. However, these wrinkles seem not to restrict the CNT growth even though CNTs were not as straight as CNTs grown on the silicon substrate. As shown in the Fig. 5.1(b), uniform carpet-like CNTs

were grown on the graphene-based film. CNTs can still keep aligned with each other in a height of over 10 μm . In order to clearly check the quality of CNTs and interface between CNTs and graphene-based film, the root region of samples were zoomed in to be investigated by SEM, as shown in Fig. 5.1(c). It can be seen that CNTs were directly grown from graphene-based film in perpendicular angle without any interface layer between each other. In the electrical conductivity perspective, this hybrid structure, combined the high in-plane electrical conductivity of graphene and the high vertical electrical transport capability of CNTs, can potentially exhibit much better electrical performance compared the mechanically composite of CNT and graphene. Moreover, the surface area is also very plenty due to CNTs' porous structure. Furthermore, Fig.5.1 (d) showed that this hybrid structure could exist in the freestanding way, which indicate that this material could be more applicable because of easy handling.

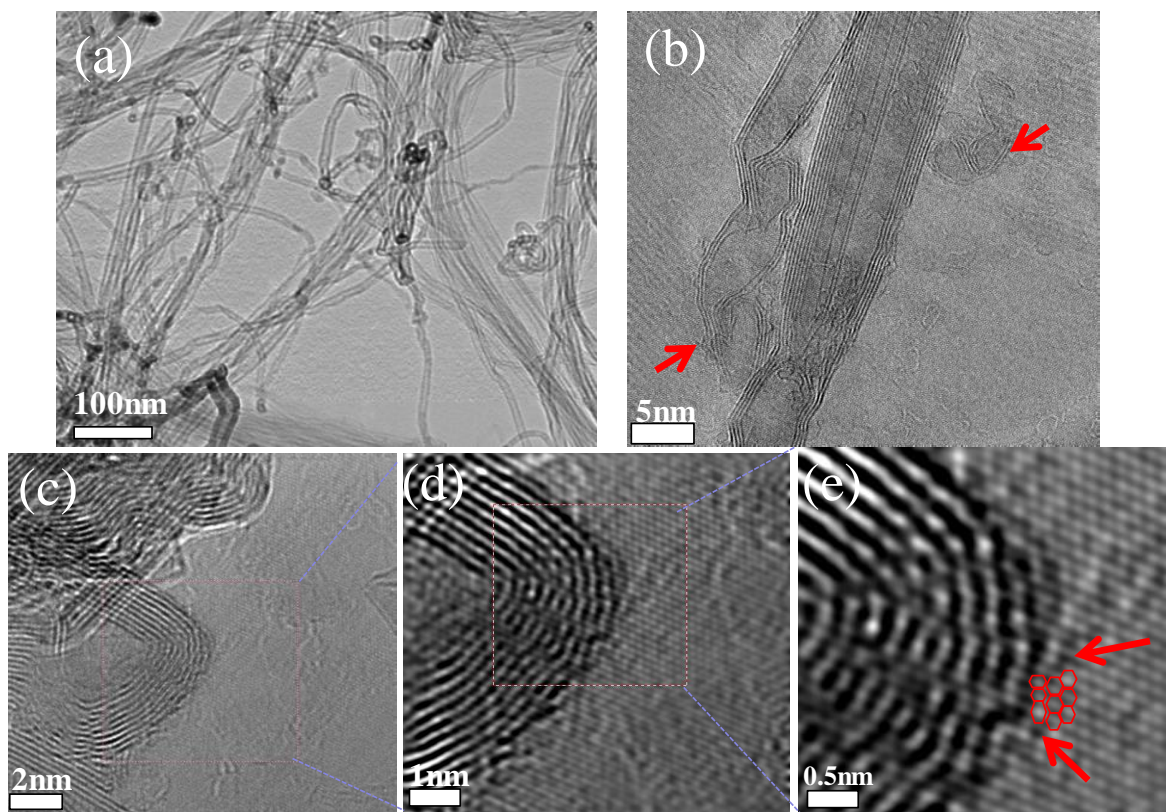


Fig. 5.2. TEM images of CNT-G hybrid materials. (a) and (b) show CNTs grown on graphene based film are multiwall structure with a diameter range of 5-10 nm. As seen in image (b) marked by red arrow, there are some ring-like inner shell structures, which are the root parts of CNTs.(c)-(e) investigated the transition part between CNT shells and graphene.

The interface between CNT and graphene is a key factor to influence the final electrical performance of this hybrid structure. Thus, in order to investigate the interface structure, TEM was used to monitor the nanostructure in atomic scale. As shown in Fig. 5.2(a) and (b), carbon nanotubes structure were clearly observed and multiwall structure with a diameter range of 5-10 nm was verified. Moreover, there are many ring-like structures arisen in the image (a), which cannot be monitored in the normal CNT growth. After zooming in some parts of image (a), we can see clearly that an inner ring-like shell positions inside CNT shells in the root region of CNTs. According to previous reports [124], [182], these ring-like structures can be seen as a typical characteristic of covalent bonds between CNTs and graphene. In order to obtain direct evidence, high-resolution TEM images were captured to analysis the transition part between CNTs and graphene. As shown in Fig. 5.2(d-e), we gradually zoomed in the interface until the atomic structure can be clearly observed. Each white dot representing an aromatic ring was orderly arrayed until the shells of CNTs. It can be seen a seamless connection between CNTs and graphene due to that there is not visible gap or crack at the interface except some black dots. The black dots could be due to that some aromatic rings nearby the shells of CNTs marked in red arrows was distorted because of their out-of-plane orientations from 2D planar graphene [122], [125], [183].

5.2 Electrochemical measurements

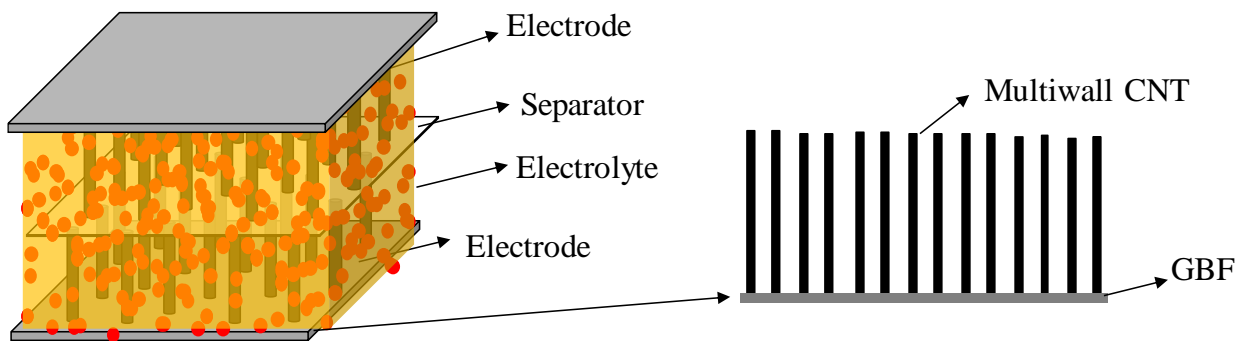


Fig. 5.3. Scheme of EDLC fabricated in this work. The current collector and electrode are prepared directly through the CVD growth.

Two-electrode electric double-layer capacitors (EDLC) were fabricated with the as-grown hybrid materials. The aligned CNT array was grown on the graphene-based film using CVD method as mentioned in the previous section. The EDLC device scheme is shown in Fig 5.3. Glass fiber was used as the separator. The electrolyte solution was 6 M KOH. The specific capacitance C_p was calculated from the CV curves using the following equation:

$$C_p = \frac{\int I dV}{mv\Delta V}$$

where I is the applied current, m is the mass of active electrode material, V is the potential scan rate, and ΔV is the potential range. The specific capacitance calculated from the charge and discharge line was based on the following equation:

$$C_p = \frac{I}{m(dV/dt)}$$

where I is the applied current, m is the mass of active electrode material, and dV/dt is the slope of the charge curve.

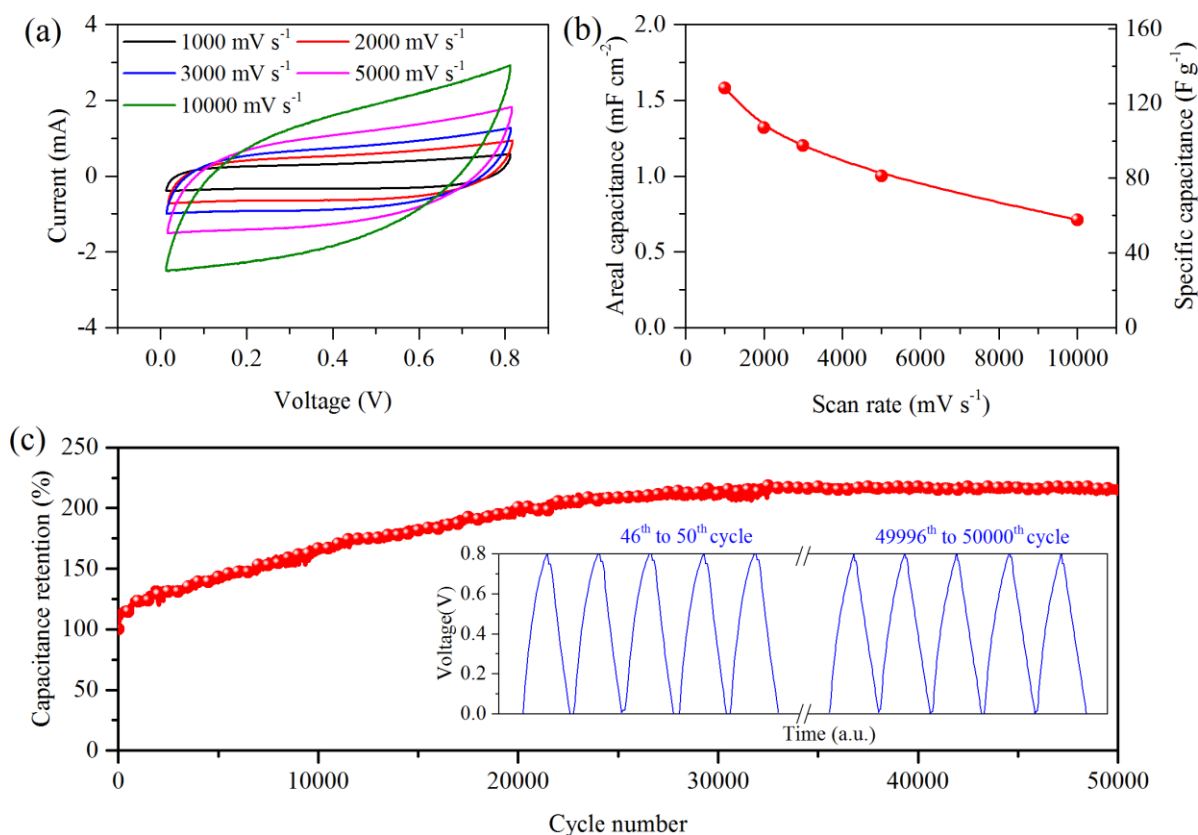


Fig. 5.4. CNT-G supercapacitor with 6 M KOH electrolyte (a) Cyclic voltammograms of CNT-G hybrid electrode at different scan rates. (b) The areal and specific capacitance of CNT-G hybrid samples at different scan rates. (c) Capacitance retention of CNT-G samples at a current density of 40 A g⁻¹. Inset shows the Galvanostatic charge/discharge (GCD) curves at specified cycle numbers.

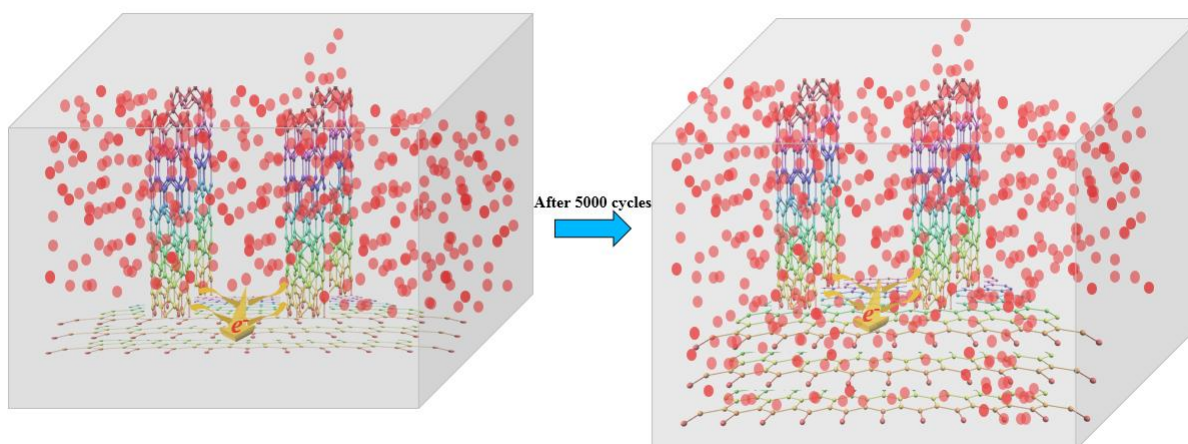


Fig. 5.5. The schematic illustration of the ion diffusion behavior and electron transfer path in CNT-G electrode before and after 50000 charging/discharging cycles.

As shown in Fig. 5.4(a), CNT-G sample exhibits the stable CV curves in quasi-rectangular shapes under different scan rates, even in 10000 mV s^{-1} , which indicates an ideal capacitive behavior. This excellent behavior could be due to the high conductivity and fast ion transport of the CNT-G hybrid samples. According to the CV analyses, the specific capacitance of CNT-G hybrid samples under various scan rates are shown in Fig. 5.4(b). The areal and specific capacitance is 1.6 F cm^{-2} and 168 F g^{-1} at a scan rate of 1000 mV s^{-1} . The device still delivers high values of 0.7 mF cm^{-2} and 58 F g^{-1} , respectively, at an extremely high scan rate of 10000 mV s^{-1} . The results indicate a superior rate capability of the CNT-G material, which could be attributed to high current carrying capability of graphene and CNT. We further investigated the stability of the samples by repeated charge/discharge cycles. In Fig. 5.4(c), it is interesting to be noted that the discharging capacity were gradually increasing with cycles by 100% before 20000 cycles. This significant increase in the first 20000 cycles could be attributed to electro-activation [254], [255], i.e. the increase of effective surface area as shown in Fig. 5.5. The graphene layers usually tend to restack together in the fabrication process due to strong van der Waals interaction [246]. However, this condense structure by van der Waals force will be interfered during charging and discharging energy cycles. The repeated charging cycles may generate heat expansion effect to enlarge the gap between different graphene layers, which indeed expand ion diffusion transport. Thus, the capacitance is increased at the first 20000 cycles. After that, the capacity curve with cycles tend to stabilize until 50000 cycles, which indicated the excellent electrochemical stability of the CNT-G sample.

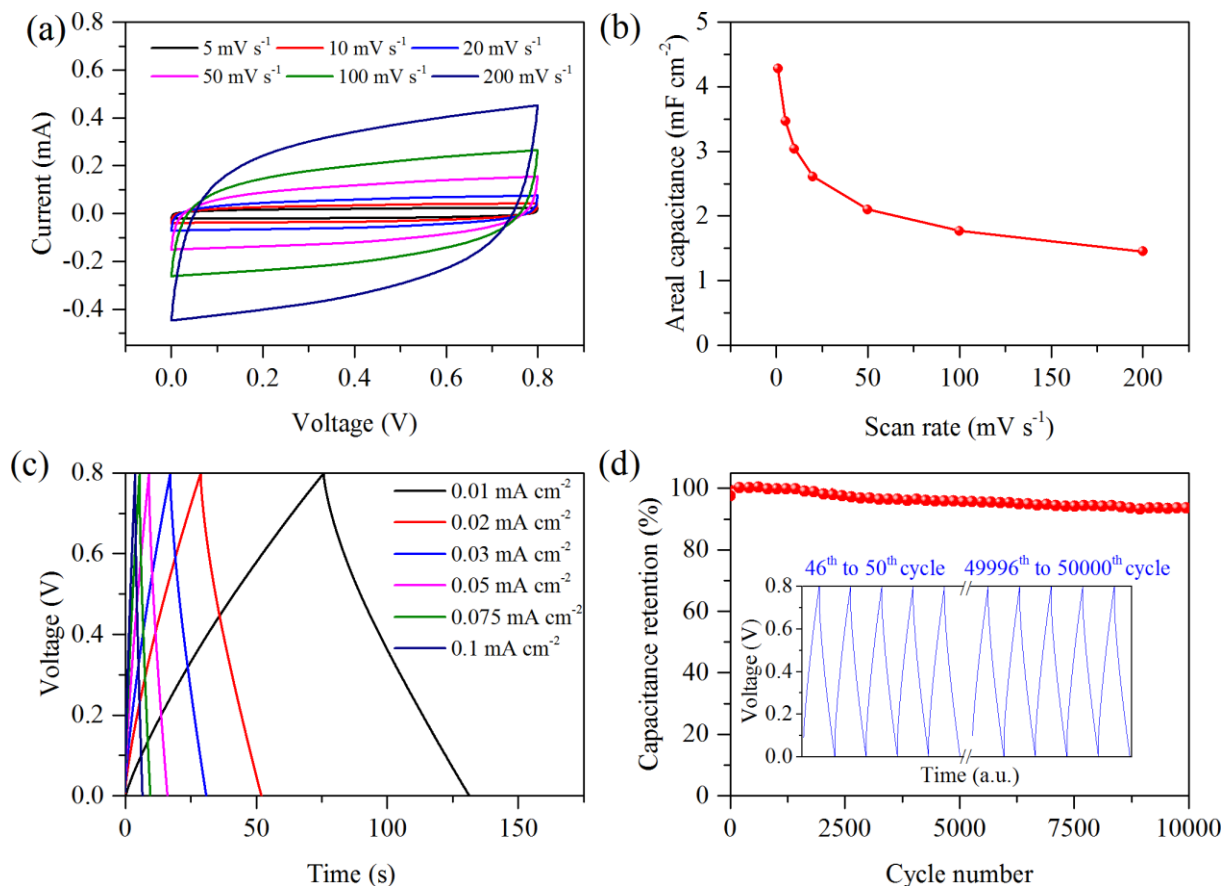


Fig. 5.6. CNT-G solid state supercapacitor with PVA/H₃PO₄ electrolyte: (a) Cyclic voltammograms of at different scan rates. (b) The areal capacitance at different scan rates. (c) Galvanostatic charge/discharge (GCD) curves at different current densities. (d) Capacitance retention at a current density of 0.1 mA cm⁻². Inset shows the GCD curves at specified cycle numbers.

The high conductivity and freestanding nature make CNT-G material promising for flexible energy storage devices. A prototype solid state supercapacitor was fabricated with PVA/H₃PO₄ electrolyte, and the device performance is displayed in Fig. 5.6. Despite of slow kinetics of gel electrolytes, the CNT-G solid state supercapacitor could sustain symmetric CV curves at relatively high scan rates (Fig. 5.6(a)). Areal capacitance is then calculated based on the enclosed area of each CV loops and the value against scan rate is plotted in Fig. 5.6(b). Areal capacitance drops quickly in the beginning from 4.3 mF cm⁻² when increasing the scan rate, and thereafter decreases slowly to 1.5 mF cm⁻² at 200 mV s⁻¹. In accordance with rectangular-like CV curves, the GCD profiles in Fig. 5.6(c) show symmetric and triangular features, indicating capacitive charge storage mechanism. The cycling test in Fig. 5.6(d) evidenced a rather high stability of the CNT-G solid state supercapacitor – capacitance retention (relative to the highest value) is 94% over 10000 cycles, and GCD curves show negligible change during the cycling test.

In summary, a freestanding controllably aligned multiwall CNT-G hybrid structure was developed through CVD process. The covalent bonds between CNTs and graphene was directly characterized in the atomic scale by high resolution TEM. This hybrid structure by covalent bonds enhanced the capability of electron transport in the material, which facilitate ion transport area in this hybrid structure. The great promise of CNT-G material in supercapacitor applications has been demonstrated. With 6 M KOH liquid electrolyte, the device showed capacitive behavior at an extremely high scan rate of 10000 mV s^{-1} and excellent stability over 50000 charging/discharging cycles. With PVA/ H_3PO_4 electrolyte, the CNT-G solid state supercapacitor delivered a high areal capacitance of 4.3 mF cm^{-2} and 94% capacitance retention over 10000 cycles. Further improvement can be performed by optimizing the density and height of CNT forest of the CNT-G material.

Chapter 6

6. Conclusion and Outlook

This thesis mainly focuses on heat dissipation and TSV interconnect of 3D IC integration through developing new nanoscale materials. In the heat dissipation part, a comprehensive thermal management solution including Nano-TIM, hBN heat spreader and G-CNT heat sink, was developed to dissipate high thermal energy generated by high power density IC chip. The Nano-TIM is able to decrease the thermal interface resistance at the interface between different blocks of 3D IC integration so that the junction temperature of IC device is in the acceptable range. The thermal and mechanical performances of this Nano-TIM were both evaluated in a typical sandwich structure. This Nano-TIM showed comparable thermal performance with indium and stronger mechanical performance than indium. Moreover, in order to alleviate hot spot effect and dilute heat density, the hBN heat spreader was developed through liquid exfoliation method. For demonstrating the performance in application, thermal test chip was employed and evaluated the hot spot cooling effect through IR measurement. In addition, the graphene and CNT hybrid heat sink was also developed to eventually dissipate thermal energy in IC system by heat sink convection so as to finally ensure the ideal life span of the IC device.

In the other part of interconnect, CNT-based material as a potential alternation to metal for TSV application was developed. In order to address the compatibility problem with IC manufacture process and relative lower electrical conductivity than metal, a series of processes including tape-assisted transfer, filling solder ball into hollow structure and electroplating Cu into CNTs bundles, were carried out and corresponding electrical performance was characterized and discussed. CNT-based TSVs exhibited excellent performance combining Cu-like high electrical conductivity and CNT-like low CTE together. Moreover, taking advantage of CNT intrinsic flexibility, a flexible 3D system based on CNT interconnect was successfully demonstrated, which implied that this flexible CNT interconnect process can potentially be a candidate in the wearable electronics device.

To take advantage of the huge surface area and high electrical conductivity of CNT-G hybrid material, CNT-G material in supercapacitor applications was developed and demonstrated. This sample showed capacitive behavior at an extremely high scan rate of 10000 mV s^{-1} and excellent stability over 50000 charging/discharging cycles.

Considering the astonishing miniaturization trend of 3D IC device, there are several aspects to be concerned in the future. For more efficient heat-dissipation, perfectly integrating different cooling mode and new cooling material into microelectronics system is still very challenging for IC industry even though every

individual cooling mode and new material can show excellent thermal performance in the laboratory. Regarding interconnect in 3D IC packaging, there is no doubt that carbon material has inherent advantages over metal for interconnect particularly in the nanoscale. However, to fully exhibit these advantages during the interconnect applications in IC device, we still need to solve many problems including too many defects introduced by integration process, complicated process and cost issues before achieving carbon based interconnect fabrication at industry level.

Nevertheless, it is expected that the work presented in this thesis can be able to provide valuable bricks, which can be put on the long way to carbon electronics era.

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