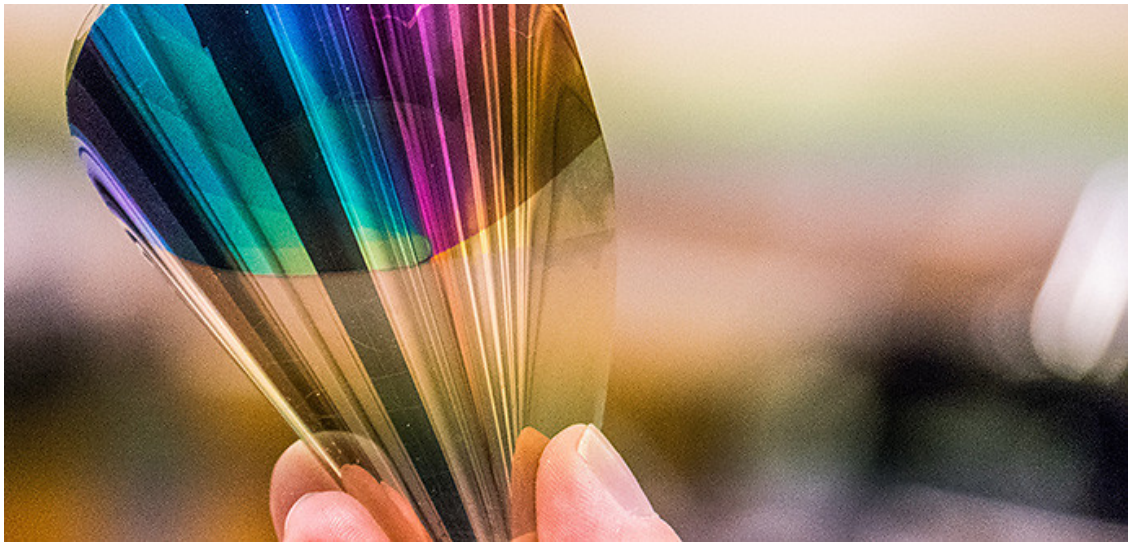

Display controller and circuit modeling for a new electronic paper display technology

Master's thesis in Embedded Electronic System Design

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Gothenburg, Sweden 2017

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Cover: The e-paper material that contains gold, silver and PET plastic and is less than a micrometer thin. ©Rdot AB

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Abstract

Reflective display technologies have gained popularity in recent years and have found use in many applications. As such, a lot of research has been conducted to find new such technologies and improve upon current ones. The Rdot display technology is an advancement on reflective electronic paper displays by adding natural color without compromising on image quality.

In this thesis the Rdot technology is evaluated and modelled electrically through an analog circuit simulations using discrete electronic components. These circuit models are compared with other similar circuits of similar technologies and it is determined whether it is possible to use similar driving schemes to drive a multi-pixel Rdot display. Timing and voltage information is also derived from the circuit simulations.

A digital display controller design is also proposed and realized on an FPGA, written in VHDL. The necessary digital components are noted and the system block diagram as well as the individual blocks with the signals between them are shown. In addition to the digital design, the necessary peripheral driving circuits and their configuration are described. It is noted that the use of DACs is obsolete in this design and the display can be driven with the same 1V source as the logic circuits.

Keywords: Rdot, reflective display, display controller, circuit modeling, FPGA

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Nikolaos Petrichos, Tomas Serti, Gothenburg, June 2017

Acronyms

AM Active matrix
ADE Analog Design Environment
CMOS Complementary metal oxide semiconductor
CRT Cathode ray tube
DAC Digital-to-analog converter
deMUX De-multiplexer
EPD Electrophoretic display
EWD Electrowetting display
FET Field-effect transistors
FPGA Field-programmable gate array
ITO Indium tin oxide
LCD Liquid crystal display
LED Light emitting diode
LUT Look-up table
MOSFET Metal oxide semiconductor FET
OLED Organic light-emitting diode
PM Passive matrix
QR-LPD Quick response liquid power display
RGB Red, Green, Blue
SMPS Switch mode power supply
TFT Thin-film transistor
VHDL VSHIC hardware description language
VHSIC Very high speed integrated circuit

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1

Introduction

For many decades, cathode ray tube (CRT) displays were dominating the display market, since they provided the best performance as a display technology. However, due to the significant advancement in VLSI technology in the last 3 decades and the large influx of small portable devices, liquid crystal display (LCD) technology quickly became the dominant technology for flat panel displays. In combination with thin-film transistor (TFT) technology development and the succesful integration of large-area microelectronics on glass, LCDs were used to create a large variety of smart digital devices, such as smartphones, smart-watches, smart-TVs etc.

With the advent of so many devices that could be used as replacement to conventional reading and record-keeping means, such as books and newspapers, paper consumption was expected to drop significantly. On the contrary, the introduction of computers and other digital media has led to an increase in paper usage for personal and professional purposes, since people prefer reading documents off paper rather than computer displays. Specifically, the increase of printing and writing paper production is shown in Fig. 1.1 for the years 1994-2006 [1].

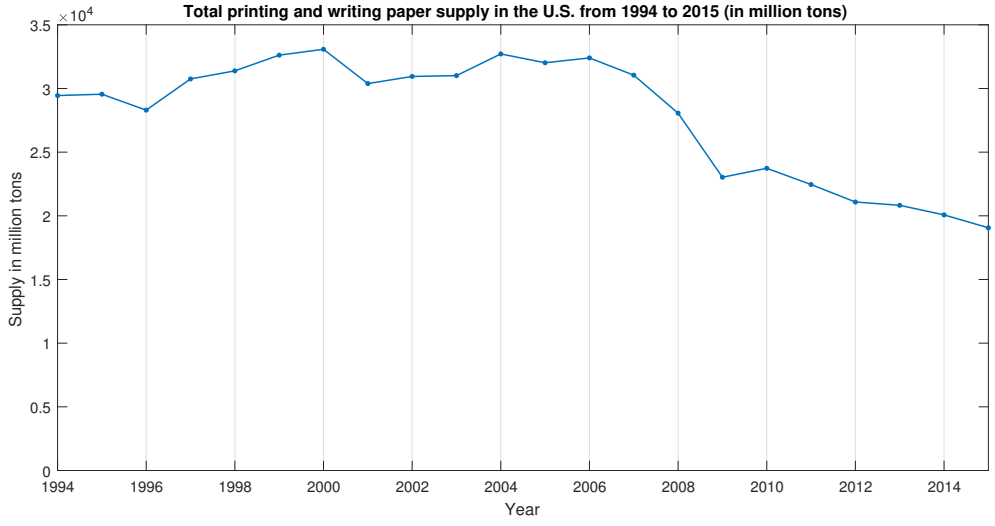


Figure 1.1: Total printing and writing paper supply in the U.S. from 1994 to 2015 [1].

The increase of paper consumption has driven researchers and engineers to create paper-like display materials and integrate them in modern electronic systems, with

the first commercial e-readers appearing in 2005 [2]. The introduction of reflective display devices in the market has led to a steady decline in reading and writing paper consumption, as shown in Fig. 1.1 for the years 2007-2015.

Following that, in the last decade, the efforts of all the competitors in the reflective display market have been to find display materials that have better quality, brightness, contrast ratio and full color capabilities. The current thesis focuses on the development of a display controller and control electronics for operating a new type of reflective display material, namely the Rdot display. In the next sections, previous work is referenced and compared with the aforementioned display material and the purpose of this thesis is motivated.

1.1 Electronic paper display technology

The majority of flat panel displays today use liquid crystal devices to operate. LCDs are built on a glass base and get illuminated from a backplane (usually LED), while the image is displayed by manipulating the polarization properties of the liquid crystals to filter the light accordingly [3]. LCD technology has advanced rapidly and modern displays can achieve very high color depth, contrast ratio and response times. They need to be refreshed constantly, though, in order to retain the image, in addition to wasting the power from the filtered light. They also introduce eye-strain for the user, since the image is constantly refreshed rather than being static. Transflective LCDs, which is a hybrid between transmitting and reflecting, have been developed [4], but they suffer from many of the same issues as regular LCDs.

Reflective displays operate by reflecting the ambient light instead of generating and filtering light. The majority of reflective displays make use of electrophoretic materials, which use microcapsules filled with a suspension of charged pigment particles and sandwiched between two electrodes. Depending on the voltage applied to the electrodes and their charge, the black and white particles change their position, showing different shades of grey [5]. There have also been several improvements on this technology with the most notable being the electrophoretic ink [6], which has been used in commercial products like the Amazon Kindle. Another display similar in structure is the quick response liquid power display (QR-LPD®), which uses a high fluidity material that combines the properties of a powder and a liquid and is higly sensitive to electricity [7].

After high-quality performance was achieved for colorless reflective displays, the desire for color-capable reflective displays increased. A few first attempts to realize that were done by using different color filter layers on top of the electrophoretic or the liquid-powder materials [8]. The quality of the image, especially brightness and constrast ratio, greatly suffer though from the use of filters since the only light source is ambient light.

In this thesis, the subject of work is a new type of electronic paper-thin display that uses ultrathin nanostructured plasmonic metasurfaces (silver, aluminum and gold) to reflect ambient light, while adjusting the electrical properties of a conducting

polymer on top to control the absorption and create a broad range of colors [9].This technology provides high polarization-independent resonant reflection (>90% in air), good constrast (30-50%), fast response times in the order of hundreds of milliseconds, ultra-low power consumption (<0.5 mW cm^{-2}) and long-term stability. This technology is based on several years of research at Chalmers University of Technology and patented by Rdot which is a Swedish incorporated venture backed start-up company [10].

1.2 Problem definition and motivation

In order to create the plasmonic display, the display material needs to connect with an electronic backplane that will control the charge around the electrodes. The backplane is usually a thin layer of transistors called thin-film transistors (TFT), which connects each pixel with peripheral driving circuits, in order to control the current moving through the pixels or the voltage applied to the electrodes. Since this plasmonic display is a new technology, no efforts for creating the accompanying electronic circuits have been made yet. This thesis is an attempt at developing appropriate control circuits to adjust voltage or current levels on the plasmonic material dynamically to produce different images.

1.3 Project goal

The goal of this project is to design a simple and reliable display controller in combination with the control electronic circuits for the Rdot display material. More specifically, the project can be divided into several tasks:

- Describe the display material properties and create an electrical circuit model that simulates its behavior as best as possible.
- Research and define required hardware to drive and operate the display based on available information.
- Design a system concept that implements both hardware description and electronic elements.
- Simulate the digital design and the circuit design.
- Derive conclusions about the feasibility of the chosen driving scheme and the derived values.

1.4 Scope limitations

Since the display technology is new and there is not much information about it yet available, several assumptions about its properties need to be made in order to develop a design and derive conclusions. There is neither a display provided yet by Rdot nor a working sample pixel out of the lab, which makes it impossible to derive concrete conclusions about the display properties. As such, it is a challenge to study the behavior of the technology and it has to be done by the limited information

available in the initial publication [9] and information that can be derived from other publications for the same or similar materials.

Furthermore, there is no specific TFT technology that is chosen to be integrated on the display or to match the display properties. The development of a TFT array and the in-depth analysis and comparison of available TFT technologies which suit the display material best is outside of the scope of this thesis. Generic TFT models will be used, found in the chosen circuit design and simulation programs. Complex TFT parameters and behavior will also be ignored during the analysis and simulation of the system. Only the fundamental properties of the TFT technology will be considered.

1.5 Outline of the thesis

This thesis is organized in three different parts; Chapters 2-3 are based on research and present the theory and background knowledge related to the technical field of the thesis. Chapter 4 describes the steps of the electrical modelling of the Rdot technology. Chapter 5 is focused on the development of the digital display controller. In the end, a summary and discussion conclude the thesis and some future work opportunities are explored.

Chapter 2 introduces the concept of reflective display technology and mentions briefly a few technologies already on the market, with their advantages and disadvantages. Afterwards, it introduces the Rdot technology, its structure and operating principles, as well as determining some of its properties that are relevant for this thesis.

Chapter 3 explains how different schemes can be used for addressing a display and which one is more relevant for this thesis. It also describes the different electronic components that are necessary for designing a working display system. The main component described is the TFT and its operating principles. The different DC/DC converter architectures are also explored, since different voltage levels are necessary in this design.

Chapter 4 is an analytical electrical modelling of different pixel configurations and sizes, mainly to show that the chosen driving scheme can work and to also find out about timing and voltage requirements.

Chapter 5 describes in detail how the display controller design is done, which digital components are used and in which way and the whole system design is shown.

Chapter 6 contains a summary of what has been described in the thesis, what the initial goals were and the deviations from them, and finally some discussion on how this technology can be used based on the findings from previous chapters.

Chapter 7 proposes some work that can be done in the future to expand upon this thesis.

2

Electronic reflective display technology

The reflective electronic paper display concept has in recent years become more well-known and a part of an active research. E-ink displays provided today in the market are mainly developed to generate black, gray and white colors in a more energy efficient way than LCD displays. The Rdot display material provides both colors and is power efficient and, since it is a new research topic, there is limited theory available about it, so research on similar kind of technologies(LCD, OLED and LED displays) has been made.

2.1 State of the art

Electronic paper(e-paper) displays are display units that are very much like the regular ink on paper. Unlike other display devices, the e-paper displays reflect light the same way as a newspaper does, which contributes to a more comfortable reading. There are different types of e-paper displays that have been developed over the years and some of them will be further explained in this section.

2.1.1 QR-LPD®

QR-LPD® is a paper-like display which uses electronic powder to provide images on the display. This powder is high-fluency and sensitive to electricity. The material is a combination of properties from powder and liquid. Some of the most important properties and advantages for this technology are image stability, high resolution, fast response, easy viewing and low power consumption[7].

The display material was developed by the Japanese company Bridgestone and it behaves like liquid despite its powdered form. The powder can be divided into two categories, white and black colored powder, where the former mentioned has a negative charge while the latter has a positive charge. These two powders are attracted to each other and make a gray mass. When the material is subjected to an electric force, the liquid-powder is moved and the white particles are drawn to the positive electrode while the black particles to the negative electrode.

As can be seen in Fig. 2.1, the structure of the technology is built upon the negatively charged white powders and positively charged black ones. They are located between two glass plates. Indium tin oxide(ITO), which has a good electrical conductivity

and optical transparency, is connected on the inside of the glass plates. To avoid the powder from mixing, a rib is used and the remaining part of the area is filled with air. The image to the left of Fig. 2.1 represents black appearance on the display while the one on the right represents white appearance on the display.

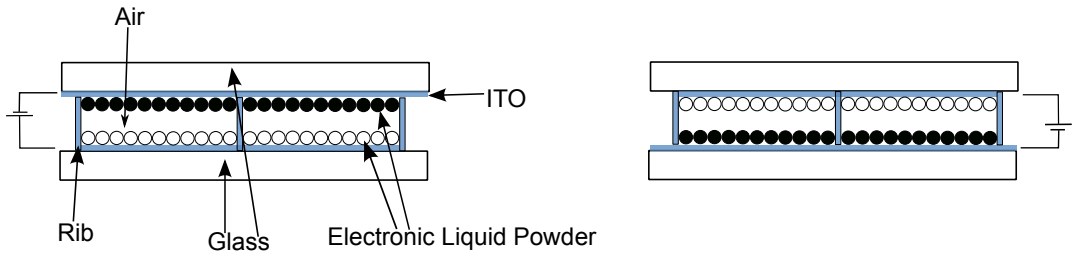


Figure 2.1: Structure of the QR-LPD[7]

The structure of the QR-LPD is very simple. The black powders, which are positively charged, will move to the top electrode and a black appearance will be showed during the time when a negative voltage is applied on the top ITO electrode. In the opposite way, when a positive voltage is applied, the white powders will move to the top electrode and a white appearance will be showed. Compared to an LCD display, this display does not require polarization, orientation or a reflective layer and it can still provide a clear image. This has to do with the good threshold characteristic of the electronic powder[7]. To change the orientation of the powder, though, requires very high potentials between the electrodes (up to 70V). This type of display can also only output black and white images, with some intermidiate greyscale images.

2.1.2 The electrophoretic display

Similar to the QR-LPD® display, the electrophoretic display(EPD) is constructed to look like real ink on paper. The display is associated with e-paper/e-reader applications due to its ability to show messages or images in all lighting environments and it provides good readability in direct sunlight [11].

The EPD is based on movement of electrically charged molecules or particles under force of an electric field. The technology utilizes colored micro-particles suspended in clear fluid[12]. It has a two-particle distribution, with black and white pigment particles located inside micro-encapsulated and electrically insulating oil. The micro-capsules are placed between a transparent top electrode and line electrodes at the bottom plate as in Fig. 2.2.

The black and white particles are transmitted to opposite faces and form a pixel on the display when a DC-voltage is applied over the two electrodes. When a positive voltage is applied at the bottom plate, the white particles are pushed to the surface and ambient light is reflected. The image contrast becomes sharper with more light shining on the display surface.

The EPD has the advantages of consuming little power, a good reflectivity and also a wide viewing angle[11]. Another important advantage is the bistable behavior

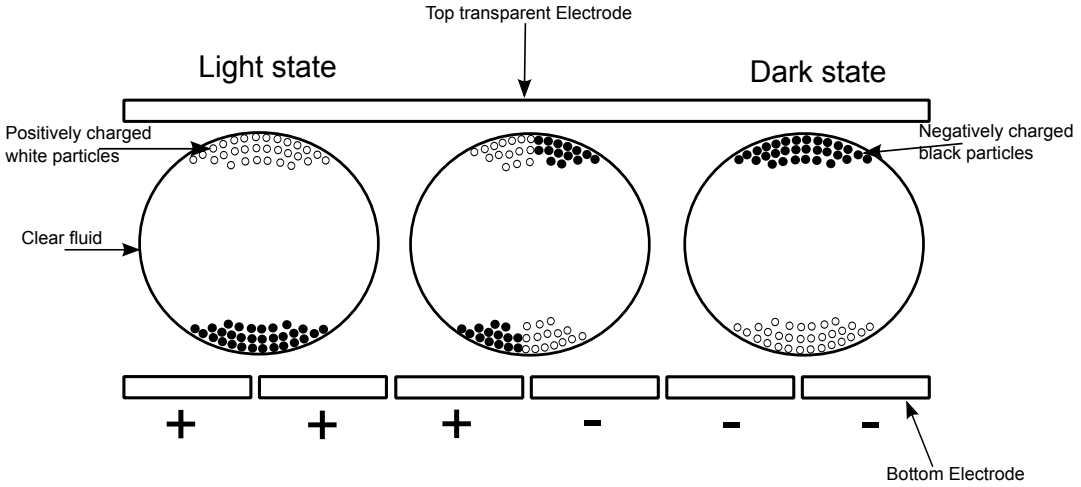


Figure 2.2: Structure of the electrophoretic display [13]

which means that an image will remain even if the driving voltage is removed and the power consumption will be dominated by how fast images are switching on the display. The power consumption is small in e-readers since the display is updated more slowly compared to general purpose displays which would have a larger power consumption due to the rapid update[11].

The EPD display has also some drawbacks such as to achieve gray levels with a high efficiency due to the bistable performance of the display. Since there are only black and white particles, it is hard to force the display to something different than white and black.

2.1.3 Electrowetting display

The electrowetting display(EWD) differs to other electronic paper displays when it comes to the material that is used for it. It is based on the controlling of oil and water with the help of an applied voltage. As can be seen in Fig. 2.3, the coloured oil is located between the water and hydrophobic insulator together with a transparent electrode[14].

The right image in Fig. 2.3 shows the case when a voltage V is applied between the water and transparent electrode which forces the oil to move to the side. How far it moves is dependent on the balance between electrical and capillary forces. The moving of the oil to the side leads to a slightly transparent pixel. The left image shows the case when no voltage V is applied which contributes to the oil forming a flat layer between the water and hydrophobic insulator, leading to a colored pixel.

The EWD has several advantages such as displaying video content in small pixels when the movement of the oil film is fast enough. The technology has also at least as good reflectively and contrast as other reflective displays. It has also a wide viewing angle. Comparing LCDs and the EWD with colour, the EWD has a reflectivity four times higher than the LCD[14].

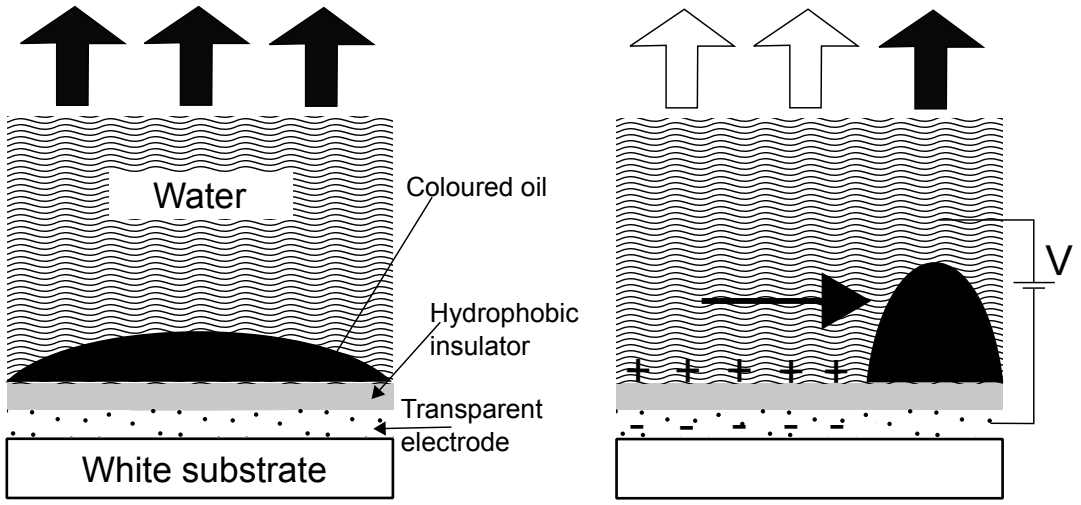


Figure 2.3: Structure of the electrowetting display[14]

There are also some drawbacks with the EWD such as the bad reflectivity of colour which has to do with use of RGB colour segmentation[14]. Another drawback is the decreased brightness of the pixels which occurs at low frequencies during the frame times. In other words, a reduction of oil contraction has a negative impact on the brightness, which means that the display needs a constant refresh to keep the image[15].

2.2 Structure of the Rdot display

The Rdot display uses thin metal layers in a configuration to create plasmonic metasurfaces to interact with ambient light [9]. A surface plasmon is a wave oscillation of electrons propagating along the surface of certain metals. Electromagnetic fields are created outside and inside the metal through the charge motion in the surface plasmon [16]. Under certain circumstances, the electrons oscillate at the same frequency as the light waves and this leads to interesting properties for the material, such as absorbtion, scattering and coupling of the incident light.

The display interacts with visible wavelengths using three solid films: Au(gold), AI_2O_3(aluminium oxide or alumina) and Ag(silver) (Fig. 2.4). A 150 nm silver film is first deposited on a glass or plastic substrate in order to provide high base reflection. On top of that, the alumina layer is deposited in order to tune the reflective color by Fabry-Pérot interference [17]. Different alumina thickness creates different colors. In order to create the three primary colors red, green and blue (RGB) the alumina thickness was found to be 48, 93 and 83 nm respectively [9]. A 20 nm gold film is deposited at the top with 150 nm nanoholes down to the alumina layer to complete the reflective layer. The gold layer is important to create coloration because of the very low absorption of silver in the visible spectrum, causing all the visible wavelengths to be reflected. The nanohole array is what enables the coupling to the surface plasmons and also provides strong resonant scattering (on the respective wavelength), thus strengthening the display colorization [9].

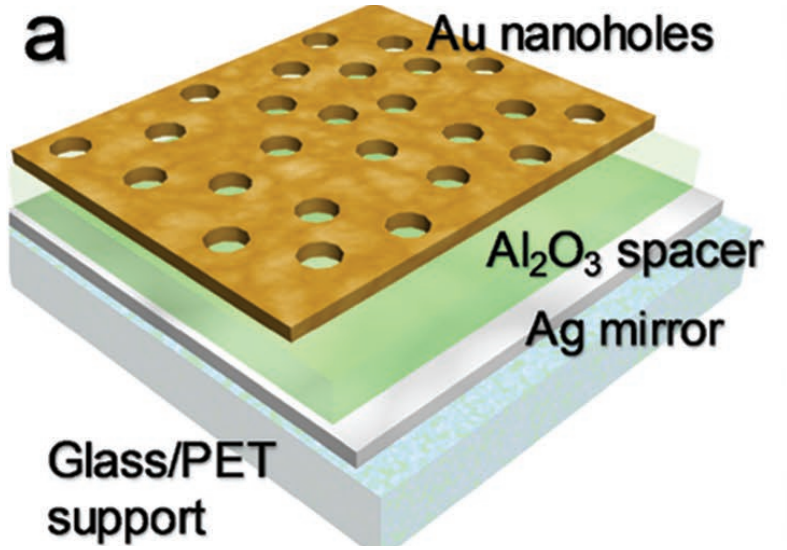


Figure 2.4: Schematic of the plasmonic metasurface [9].

In order to be able to switch colors on and off, the tunable optical absorption of conjugated polymers is utilized. The electrical and optical properties of the polymer are altered by applying voltage across it, in order to create an electric field. The polymer is sandwiched between the gold layer, which acts as an electrode, and a graphene or ITO covered plastic, which act as counter electrodes, creating a thin electrolyte layer in between, essentially operating similar to a capacitor. Colors are switched "on" in an electrolyte, reducing the polymer to its neutral state, altering its bandgap and leading to strongly reduced absorption [9]. The response time of the display, which is the time it takes for 90% intensity change, depends on the thickness of the polymer and was reported to be in the order of hundreds of milliseconds [9]. This indicates that the technology can be used for reading devices that display static images but not for animated images, since the required response time is less than 100 milliseconds. The contrast is also dependent on the polymer thickness and it has been demonstrated that the optimal contrast of the Rdot display is very similar to the printed paper.

Power consumption is also a significant advantage of the Rdot display over other similar technologies. In comparison to emissive displays (OLED, LED and CRT displays), the power consumption for this display is more than one order of magnitude lower and much less than that compared to electrophoretic displays [9]. This has to do with the thin polymer films but also since the ideal voltage used for switching the colors fully on is -0.9, -1.0 and -0.8 V for RGB respectively, which is significantly lower than other similar technologies. Furthermore, current monitoring has shown that a switching period of 10 s increases the power density (power over area) by less than a factor of three. Taking into account that this frequency assumption is pessimistic and that not all pixels will be fully active at all times, combined with the implementation of low power driving schemes, the actual power consumption of the metasurfaces is overestimated [9].

2.3 Polymers

The choice of polymer used for this technology affects significantly the properties of the display. Polymers are created through a chemical reaction of monomers, and these are in turn small molecular compounds. Polymers can be formed in two different ways, either that the monomers have reactive functional groups or double/triple bonds whose reaction leads to significant linkages between repeat units [18]. Conjugated polymers, in particular, have electrical and optical properties that make them relevant for use in the Rdot display. They are conductive under certain conditions, so they can be used as dielectric material, and their absorption changes with applied potential, so they can be deposited on top of the reflective metal layers and in between electrodes.

2.3.1 Polypyrrole

There are several different types of conductive polymers. During the first phase of development and testing for the Rdot display, the chosen polymer was polypyrrole, which is formed by the polymerization (process of reacting monomer molecules together in a chemical reaction to form polymer chains) of pyrrole. During this polymerization, each monomer provides two electrons for the bond formation but also one electron for every 4th ring for the oxidation of the polymer[19]. One of polypyrrole's most important characteristics is its controllable thickness and conductivity. The conductivity of the polymer is used to adjust the reflected light from the plasmonic metasurface while its thickness determines the response time of the intensity change for a specific wavelength[9].

All the assumptions and the analysis done in this thesis are based on a sample using polypyrrole films doped with sodium dodecylbenzenesulfonate (NaDBS) as an electrolyte. It has been determined that for optimal contrast a different polypyrrole thickness is required for each color, specifically 190, 260 and 110 nm for RGB respectively.

2.3.2 PEDOT and PProDOT

As already mentioned, there are different types of conductive polymers, each with different properties. From the different alternatives, two polymers have been tested and demonstrated better performance than polypyrrole: Poly(3,4-ethylenedioxythiophene), or PEDOT, and poly(3,4-propylenedioxythiophene), or PProDOT.

PEDOT is a conducting polymer with good electrochromic properties. Comparing to poly(thiophene), also called PT, PEDOT shows a more rapid switching but also a better balance at ambient and elevated temperatures[20].

One important characteristic of electrochromic polymers is the ability to show varying colors when they are held at different potentials. In order for the material to be useful in a display, such as the Rdot display, these kind of materials (polymers) need to show stability for a longer time, fast redox and as high as possible transmit-

tance factor (ΔT) between states (dark and light color), which is one of the most important parameters.

As already mentioned in this section, PEDOT exhibits a rapid switching and experiments in the lab have shown successful utilization of the benefits of PEDOT to synthesize many electrochromic polymers. The tests have also shown that, for a wavelength of 620 nm, PEDOT can be used in EC devices with ΔT of 45% which is good [20]. Further investigations have shown a way to improve the ΔT value of PEDOT by chemical derivatives. According to the experiments [20], the synthesized derivative with best qualities suitable for this purpose was PProDOT. PProDOT-Me_2 was according to experiments showing a transmittance of 78% between two states at a maximum wavelength(λ_{max}) of 578nm [20].

The polymer determined for the Rdot display is based on the parameters above, especially the high ΔT, which is an important factor for the display.

2.4 Display properties

Efforts have been made in this thesis to approximate and simulate the behavior of the display material. The Rdot display technology is new and as such there is a significant lack of information available for it in terms of its electrical properties. This information is important in order to design an active matrix driving circuit to drive the display effectively. Electrical characteristics and behavior is also necessary to realize the low power consumption potential of the technology while maintaining performance stability.

It has been shown (Fig. 2.5) that voltage is not linearly related to absorption and it can also reach saturation levels rapidly [9]. Different wavelengths (colors) have slightly different behavior to voltage changes, since the thickness of both the metasurface and the polymer differs. As mentioned already, for red and blue the absorption is minimal (saturates) at -0.8 and -0.9 V respectively, whereas for green it can still decrease with voltage below -1V. However, long exposure to voltages below -1V (or above 1V) can damage the metasurface irreversibly [9], so they are avoided.

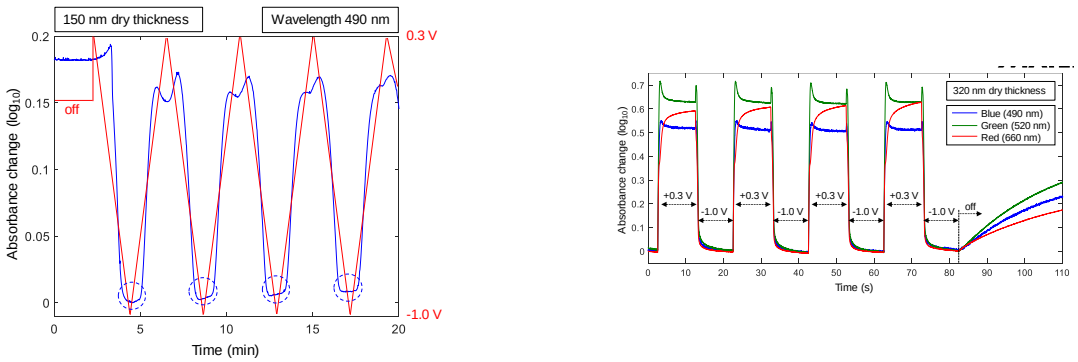


Figure 2.5: Absorbance change compared to voltage changes for different wavelengths [9].

One very important characteristic of the Rdot material is the electric current (I) going through it and how it relates with the voltage applied to it. Such a relation provides information about the resistivity of the material so it can be approximated by an RC circuit model. Cyclic voltammetry performed on a sample with an electrode area of 176 mm^2 shows the transient current when sweeping the voltage in a rate of 10 mV/s (Fig. 2.6) [9]. By extracting the data points from the voltammogram, it is possible to approximate a V-I curve, which is shown in Fig. 2.6, through the curve fitting tool in MATLAB. It becomes clear from the figure that the relation of voltage with current is not linear, so some non-linearities are expected also in the resistivity (voltage regions that it becomes unstable). This response is probably related to the capacitive properties of the material, since they introduce charge and discharge times, causing the V-I curve to be exponential instead of linear.

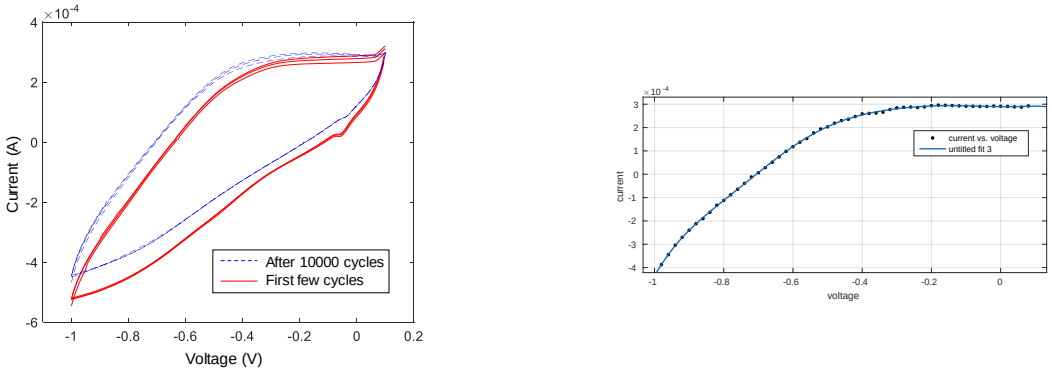


Figure 2.6: Voltammogram and the curve fitting of the data points in MATLAB [9].

The resistance of the material for different voltages can also be extracted by the V-I data, with $R = \frac{V}{I}$, and the plot of resistance versus voltage is shown in Fig. 2.7. The non-linear and the stable regions are marked. These regions provide information about which voltage levels will drive the display with stability in mind. For example, to drive this 176 mm^2 sample to minimum absorption levels, voltage should remain below -0.8V for at least a few seconds. Calculations about potential storage capacitor size in an AM-TFT cell can also be done with this information, though in case of such a large area sample it would not be efficient to use a capacitor to drive the material for seconds (that would require a very large capacitor).

Another important characteristic of the display is the power consumption, which can confirm some earlier assumptions. As stated earlier, power consumption for this technology is significantly lower compared to other similar technologies, so it would be safe to assume that the same driving schemes would work as well in operating this display. Especially for an active matrix TFT, using a storage capacitor of the same size as used in other similar displays should provide the same results. The power consumption was also calculated for the same sample [9] by integrating the current trace to get the average current during one cycle (Fig. 2.8. The increase in current is a result of switching voltage from -1V to +0.3V, which happened with a frequency of 10 seconds in this example. It should be noted that in reality an electronic paper

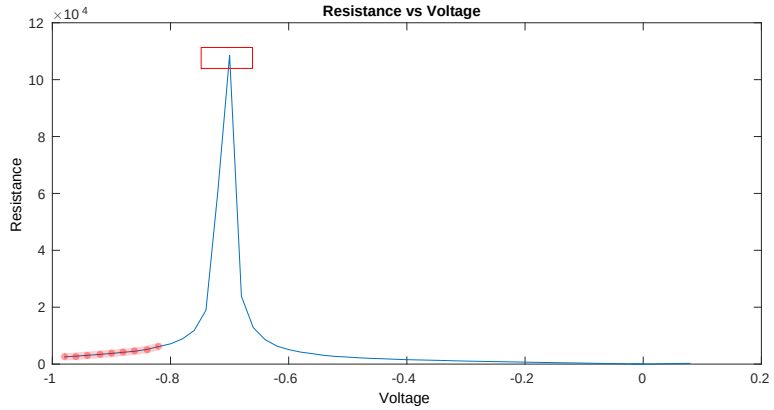


Figure 2.7: Resistance curve derived from the voltammogram data.

device would maintain a static image for the vast majority of the time and the switching would happen a lot less frequently, so this average power consumption is vastly overestimated. When the voltage is steady, there is a leakage or back current, which is 3 times smaller than the average current due to switching. This means that power consumption is also increased by a factor of three due to switching. Lower polymer thickness will provide reduced currents and as a result reduced power consumption. The energy density (energy over area) for one switch was calculated to be around 80 mJ/m^2, which indicates that for this sample the average current at -1V is around 1.4 mA (similar to the data from the voltammogram).

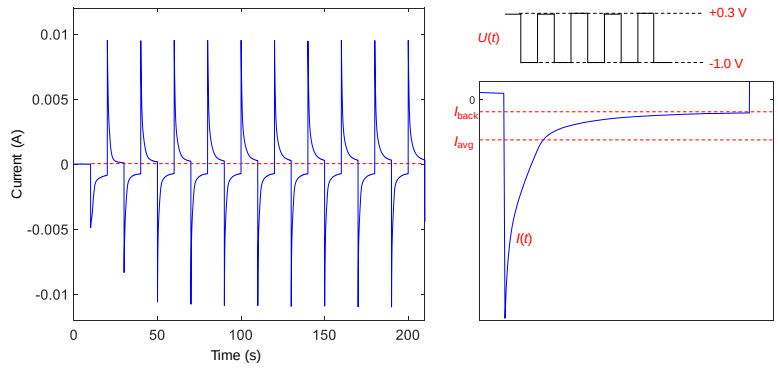


Figure 2.8: Current trace when switching the voltage and average current [9]

As mentioned earlier, the way the display is constructed, with two electrodes surrounding the doped polymer, each pixel has similarities to a capacitor. The capacitive load of the material is dependent both on the area of the metal electrode and the thickness of the polymer. Since specific thickness is required to produce each color, it is safe to assume that the thickness of the polymer will remain constant regardless of the area of the pixel. The parallel plate capacitance equation (2.1) is used to approximate the capacitance of the pixel:

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d}, \tag{2.1}$$

where ϵ_0 is the dielectric constant of free space, ϵ_r is the dielectric constant of the material separating the plates (electrodes), A is the area of the plates and d is the distance of the plates (thickness of material).

Since there is very limited information available for the dielectric properties of polypyrrole, especially when doped with various solvents, some assumptions must be made and the capacitance can only be approximated. The thickness of the used polypyrrole, either dry or doped, can be found by integrating the current through the electrode and measuring the accumulated surface charge density (C/m^2) on the electrode. For PPy(DBS), when the surface charge density was 50 mC/cm^2, the thickness was measured at 200nm [21]. It is important at this point to note that the thickness of PPy(DBS) increases when negative voltage is applied to it (as it is the case for Rdot). Accounting for these effects and determining exact properties of the display material is outside of the scope of this thesis, so the capacitive load will be roughly approximated and the thickness will be considered constant at 230nm, which is the dry polypyrrole (undoped) thickness for which the energy measurements were done. Based on these assumptions, the capacitance of the $176mm^2$ sample can be approximated at 10 µF, which should be expected from a sample of that size.

Another way of approximating the restistive and capacitive load of the sample is to look again at the current response at Fig. 2.8 and consider this as the current through a capacitor in a simple RC circuit. As explained, the Rdot sample can be described as a combination of a resistor and a capacitor, as shown in Fig. 2.9a. Here, R_{PPy} and C_{PPy} represent the resistance and the capacitance of polypyrrole respectively and R_{off} represents the resistance of the open switch (assumed infinite in this case). C_{PPy} can be approximated by closing the switch and measuring the charge/discharge time of the capacitor, i.e. the RC time constant τ. With the switch closed, it has a low resistance R_{on}, which is assumed to be significantly smaller than R_{PPy}. In that case, R_{PPy} will be ignored by the current and the equivalent circuit would be the one at Fig. 2.9b.

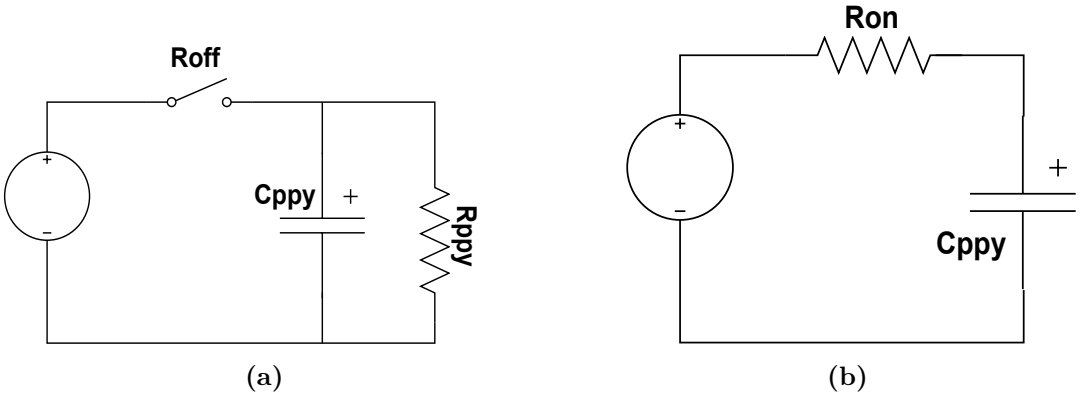


Figure 2.9: a)Open RC circuit of PPy sample. b)Closed RC circuit of PPy sample.

The discharge time of the capacitor can be considered as the time the current reaches the back current level at Fig. 2.8. The back current is the leakage current and its effect can be seen after the circuit has settled, which means that it is caused by the resistive path at R_{PPy}, so that level can be considered as 0 for the circuit before steady state. Based on all the assumptions above, R_{on} can be calculated from the maximum current at the applied voltage, $I_{max} = -0.01A$ at $V = -1V$, so $R_{on} = 100\Omega$. Since the voltage (or current) can never reach 0, but it is known that after 5τ the capacitor discharges by 99.3%, which is almost at the point where the current reaches the I_{back} level, then τ can be calculated by 2.2:

$$I(t) \cdot R_{on} = V_0(e^{-\frac{t}{5\tau}}), \tag{2.2}$$

for t = 10s. Since $\tau = \mathrm{RC}$, then $\mathrm{C_{PPy}}$ can be calculated from that to be around 500 µF, much larger than the value calculated earlier (10 µF). Since there is not enough information available to determine confidently which approach is the correct one, it is assumed that the larger capacitance is the correct one, because it is derived from data coming exclusively from the tests conducted on the Rdot sample. The resistance of the material, $\mathrm{R_{PPy}}$, can be calculated from the $\mathrm{I_{back}}$, since this leakage current can be seen after the capacitor is settled and the current only sees the resistive path. The total resistance is $R = R_{on} + R_{PPy} = \frac{V}{I_{back}}$, from which $\mathrm{R_{PPy}} = 2.027\,\mathrm{K}\Omega$. Of course, resistance and capacitance are inversely proportional to each other, since capacitance is proportional to area (as shown in 2.1) and resistance is inversely proportional to area, because $R = \frac{\rho L}{A}$, where L is the length of the resistor (in this case the thickness) and A is the area. This indicates that resistance and capacitance of the sample would scale linearly up and down respectively with size.

The properties mentioned in this section are only approximations and serve as a tool to model the behavior of the pixel and adjust the driving scheme and the electronics according to the needs of the display.

3

Display driver circuitry

3.1 Display addressing scheme

In order for the pixels to be controlled, they need to be connected to a voltage source. The method of applying voltage to pixels in an automated way is called addressing and there are three main types: direct addressing, passive matrix addressing and active matrix addressing.

3.1.1 Direct addressing

Direct addressing is the most intuitive method of controlling a display. In this method, the smallest element that can be controlled individually is called segment instead of pixel. Each segment is connected and controlled individually to the peripheral electronics and the segments are arranged in such a way as to be able to form the desired shapes and images. This method is usually used in small LCD displays, such as calculators and watches, in a 7-segment configuration, as shown in Fig. 3.1. Each segment requires its own individual input source, which makes multiplexing of data impossible. Due to that fact, direct addressing is a very slow method and spatially costly, as it requires individual wiring of every segment.

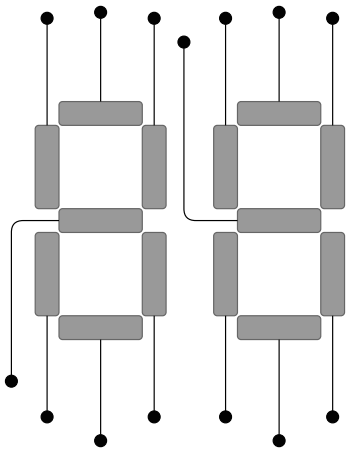


Figure 3.1: 7-segment arrangement using direct addressing.

3.1.2 Passive matrix addressing

In order to display more information, faster and with higher quality, more picture elements need to be employed. Due to the limitations of direct addressing, a multiplexing scheme is employed to achieve that. The segments are arranged into a pixel matrix configuration with M rows and N columns. This addressing scheme is called passive matrix (PM) addressing. All pixels in a row and all pixels in a column are multiplexed together and connected to one common electrode, which means the number of wires needed for controlling the panel is equal to the number of rows and columns (M+N wires). Fig. 3.2 shows the passive matrix configuration. As shown, only one row is active at any moment, activated by a pulse from the row driver. This activates all the pixels in that row, while the column driver sends the data waveforms to every column, charging the storage capacitor in each pixel at the crossings. By repeating this procedure, the whole display is addressed. Due to its simplicity and cost efficiency, this method is popular among LCDs and EPDs. But, it suffers from crosstalk between the pixels, since all pixels in a row are electrically related and a small dc voltage can be added to the pixel liquid crystal voltage from its neighbouring pixels [22]. Because the display used in the current project is very sensitive to voltage and has no threshold voltage, this crosstalk effect would cause low contrast ratio and would allow for only a small active region of operation.

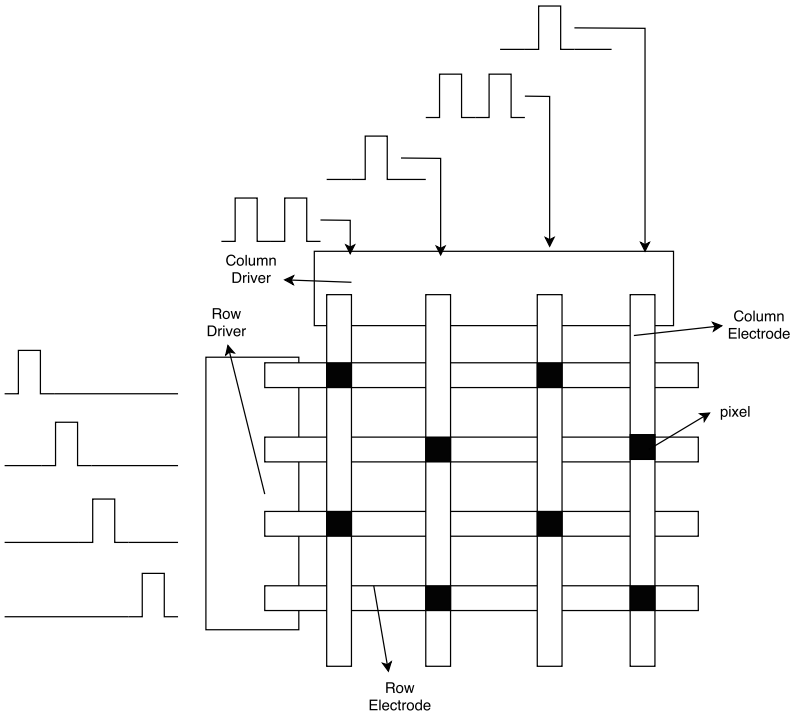


Figure 3.2: Passive matrix addressing scheme.

3.1.3 Active matrix addressing

Active matrix (AM) addressing is an improvement over the PM method to eliminate the crosstalk effect and allow for larger multiplexing capabilities. This is achieved

by introducing transistors in the cross points of the row and column lines that work as switches (Fig. 3.3). Usually, the transistor gate is connected to the row line and the transistor drain is connected to the column line. The row driver sends select pulses to each row separately and enables the transistor, while the column driver sends data voltage through the transistor to charge the storage capacitor. After the end of the select pulse, the row turns OFF and the pixel is isolated from its neighbouring pixels and the charge stored in the capacitor will be progressively used up by the pixel. For the display developed during this thesis work, AM addressing is preferred because of its robustness, speed and resistance to crosstalk.

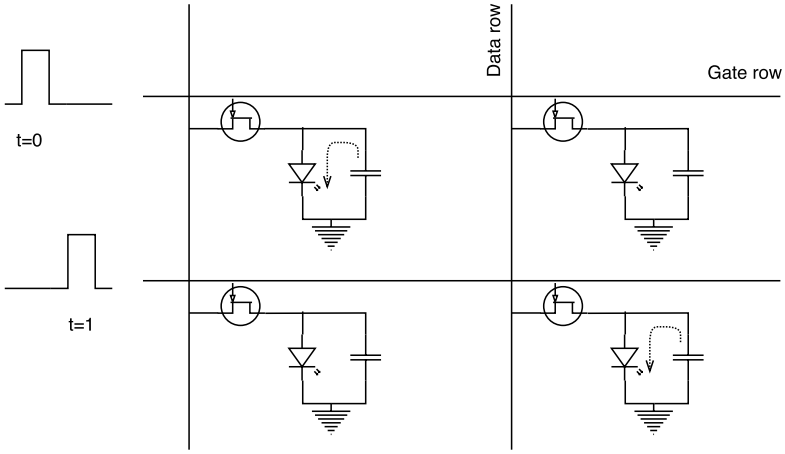


Figure 3.3: Active matrix addressing scheme [22].

3.2 Thin-film transistor

A thin-film transistor (TFT) is a type of field-effect transistors (FET) mainly used in large area and low temperature processing applications. A TFT has three terminals, i.e. gate, source and drain, and it is constructed using a conductive, semiconductive and dielectric layer configuration. This configuration enables the current flow between drain and source (I_{DS}) under certain conditions, i.e. voltage applied to the gate electrode is above (below) threshold for n-type (p-type) transistors.

The TFT is built similarly to the more widely used metal oxide semiconductor FET (MOSFET) but with a few key differences. The main difference between them is the slower carrier mobility, μ, of the TFT, making it have worse performance than the MOSFET, both in terms of conductance and switching speed [23]. In the case of flat panel displays, the key difference between TFT and MOSFET is the substrate. MOSFETs are made on silicon wafers and they have a non-trasparent silicon substrate electrode (*bulk* or *body*), in contrast to TFTs that have glass or plastic substrate (insulators), making them transparent [23].

There are two types of TFTs that are most commonly encountered: hydrogenated amorphous silicon (a-Si:H) [24] and polycrystalline silicon (poly-Si) [25]. Their main difference is poly-Si can provide both n-type and p-type devices, while a-Si:H can

only be n-type [22]. a-Si:H TFTs are easier to fabricate and bring higher yield, which makes their cost lower overall for large-sized panels [26], so they are the dominant TFT technology. Poly-Si TFTs, on the other hand, are more suitable for small-sized panels with a focus on quality, since they have higher carrier mobility and can provide higher and more stable driving current [26].

TFT operation is similar to MOSFET. When it behaves as an electrical switch, it operates in the linear (triode) region of the MOS transistor. The linear operating region is defined by two conditions, $V_{GS} > V_{th}$ and $V_{DS} \leq V_{GS} - V_{th}$, where V_{DS} is the voltage between the drain and source terminals, V_{GS} is the voltage between gate and source terminals and V_{th} is the threshold voltage of operation for the TFT. In the linear region the current between the source and the drain, I_{DS}, changes linearly with V_{DS} and it can be described as [27]

$$I_{DS} = \mu C_{OX}(\frac{W}{L})(V_{GS} - V_{th})V_{DS} \tag{3.1}$$

where μ is the carrier mobility, C_{OX} is the gate insulator capacitance per unit, W is the channel width and L is the channel length.

As shown in Eq. 3.1, the low mobility in a-Si:H requires increased aspect ratio (W/L) or higher (V_{GS}) in order to achieve a high enough (I_{DS}) to drive the display. Increasing the aspect ratio causes a reduction in image definition in traditional LCD technology, so higher driving voltage is usually chosen, typically in the range of 20V [23]. High (V_{th}) is also observed in a-Si:H TFTs ranging up to 5V. On the contrary, Poly-Si TFTs have larger OFF-currents and are typically driven to negative gate-source voltages in the range of -5V to -8V in order to minimize the leakage current condition.

The main task for the transistor is to act as a switch for each pixel in the display, in this project the active-matrix electronic paper display. Each pixel will be divided into three sub-pixels, which will individually produce the three main colors red, green and blue (RGB). Each of these sub-pixels is connected to a thin film transistor to control the voltage accross the electrode. (Fig. 3.4).

In the basic form of the active-matrix (AM) TFT, every sub pixel contains one capacitor and one transistor controlling the voltage across the capacitor. The size of the capacitor should be determined so it will be able to hold enough charge to keep the polymer in the same position the whole update time. See Fig. 3.5 for a circuit schematic of one sub-pixel.

3.3 DC/DC converter

One of the most important characteristics in a battery driven portable device such as a display is to maintain as low power consumption as possible. The pixel addressing to rows and columns for an active matrix TFT, such as in EPDs, often requires higher voltages for both negative and positive amplitudes[23]. One way to generate these high voltages and still keep the external supply as low as possible for the power

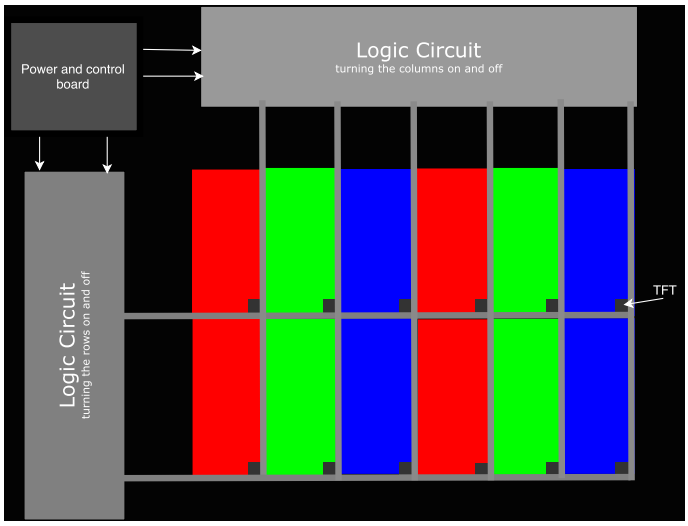


Figure 3.4: Four pixels containing RGB sub pixels with one TFT in each.

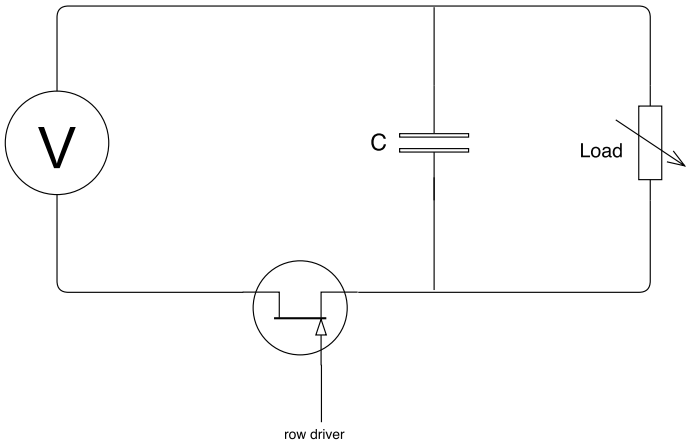


Figure 3.5: Circuit schematic of one sub-pixel.

consumption is to use a DC/DC-converter. There are different types of architectures for converters which will be further explained in the following sections.

3.3.1 Charge pump DC/DC converter

A charge pump is a DC/DC converter architecture based on the usage of switches(often diodes) and capacitors. It is an electronic circuit that converts input (supply) voltage to a DC output voltage that is many times higher. It can be used as both a negative(step-down) and positive(step-up) charge pump.

One of the most extensive charge pump architectures is the Dickson charge pump which is intended for low voltage purposes. The topology is made up by diodes which are inversely biased instead of switches, and capacitors (Fig. 3.6). As can be seen in the figure, the circuit is driven by a DC voltage, V_{in}, and it is also fed by two clock pulse trains, ϕ_1 and ϕ_1, which are in anti-phase.

The whole operation of the Dickson charge pump architecture starts from left to right according to Fig. 3.6. Diode one will charge capacitor one with the value from the input voltage when the clock pulse ϕ_1 is low, and as soon as the clock goes high, the top conducting plate of the capacitor one is charged up to two times the input voltage ($2V_{in}$).

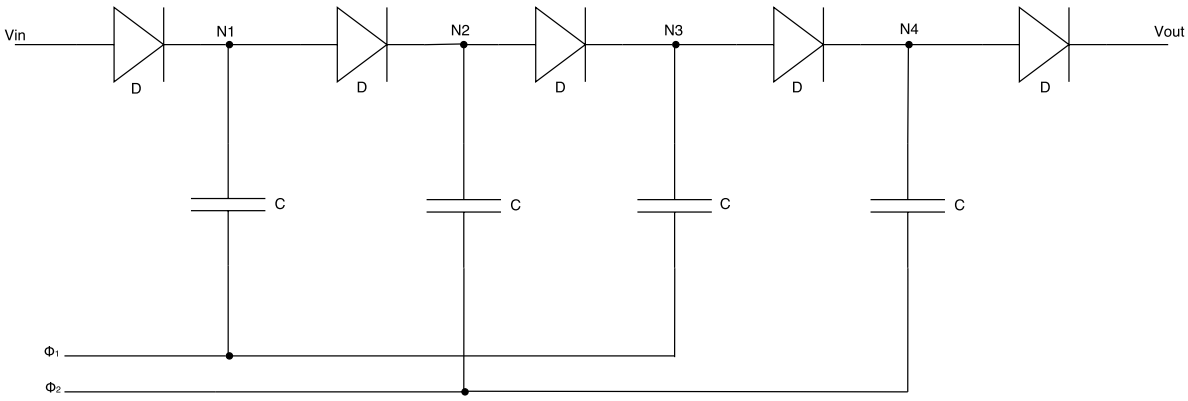


Figure 3.6: Dickson charge pump[28]

Thereafter, diode one is deactivated while diode two is active. This leads to a charge of capacitor two with the value of $2V_{in}$. During the next cycle, ϕ_1 is again low while ϕ_2 goes high, which leads to charging the top plate of capacitor two, to three times the input value ($3V_{in}$). Diode 2 is then turned off while diode three is turned on which leads to charging of capacitor three with a value of $3V_{in}$. This process is repeated until the end where charge is transmitted up through the chain[28]. Following equations describe the different parameters and their potential that can be reached during the operation of the charge pump topology:

The charge of the nodes is given by Equation 3.2[28]:

$$Q_N = V_{in}C \tag{3.2}$$

The diodes are reversed-biased and the maximum voltage potential that can be reached in the first node can be seen in Equation 3.3 [28]:

$$V_{N1max} = V_{in}\left(1 + \frac{C}{C + C_p}\right) \tag{3.3}$$

$$V_{N_1max} = 2V_{in}(if\ C_p << C)$$

The equation is the same for every node where the maximum voltage in every node increases accordingly if the components are considered as ideal. As described before in this section, there are both negative and positive charge pump stages. For a positive charge pump, the maximum voltage level that can be brought out from the circuit is dependent on the number of pump stages. See Equation 3.4[28].

$$V_{max} = nV_{in}\ (n = number\ of\ pump\ stages) \tag{3.4}$$

So for a 4-stage Dickson charge pump as in Fig. 3.6, the output voltage will be four times the input voltage.

The minimum voltage level that can be generated for a negative charge pump(inverting converter) can be seen in Equation 3.5.

$$V_{min} = -N(V_{cc}) \ (N = number\ of\ pump\ stages) \tag{3.5}$$

3.3.2 Switch mode power supply

The Switch Mode Power Supply(SMPS) is based on electromagnetic components such as inductors and transfomers storing and converting energy. The SMPS is mainly used in systems which require higher power conversion efficiency but also a high output power[28]. The system is made up of an inductor, a power switch and a diode which transfer the energy from input to the output.

The SMPS can be constructed as three different topologies such as a boost converter (output voltage higher than input supply), an inverting converter (output voltage with opposite polarity of input supply) and a buck converter (output voltage lower than the input power supply).

The boost converter as can be seen in Fig. 3.7, is made up of a switch, diode, inductor and filter capacitance. The input voltage V_{sup} represents the input DC supply and the output load is represented with a resistor R_{load}. The operation for the topology can be divided into two stages. In the first stage, when the switch is closed, electric energy is converted from the input voltage into magnetic energy which is stored in the inductor L. Current is flowing into the inductor and the magnetic energy will gradually increase over time. In the second stage, when the switch is open, the magnetic load which is stored in the inductor is converted back into electric energy and transmitted to the load together with the input voltage. This leads to an output voltage higher than the input voltage[28].

The buck converter, which has the purpose of generating an output voltage lower than the input voltage, contains the same components as the boost converter but in a rearranged configuration.

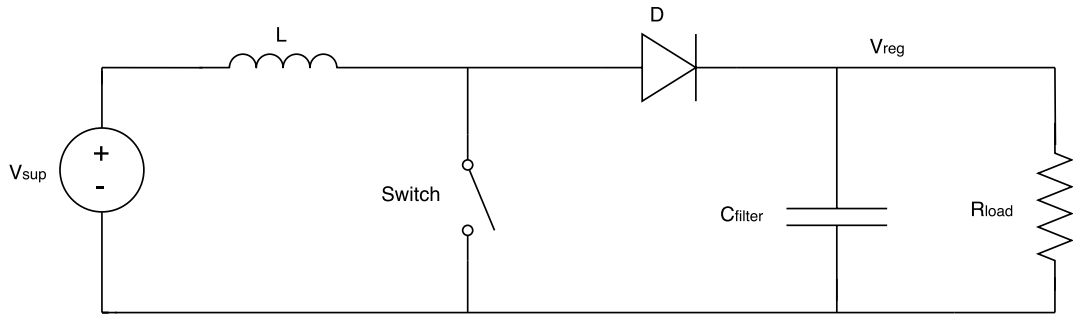


Figure 3.7: Switch mode power supply converter[28]

Two different types of DC/DC converters has been described in this section, the Dickson charge pump which is capacitor-based and the switch mode power supply which is inductor-based. Both of the technologies are intended to fulfill the task of

generating an output which is higher than the input or vice versa. But there are some drawbacks and benefits for both of them.

The capacitor-based converter (Dickson charge pump) contributes to more voltage and power loss compared to the inductor-based converter (SMPS)[28]. Therefore, charge pump converters are restricted to small size displays[23]. Since the driver being developed in this project is aimed to work for smaller displays as a first step, it would be easier to use a charge pump DC/DC converter. The number of pump stages would be easy to determine according to the desired output voltage that will drive the gate and data driver. Since the switch mode power supply is used in systems that require high power efficiency and a high output, it would be a better choice to use for a later iteration of the display.

3.3.3 High voltage level shifter

The main task for a level shifter is to convert an incoming signal, which has a lower voltage swing that what is desired, to an output signal with a higher voltage swing. This is very necessary and useful in this project since the TFT needs to be turned ON and OFF with a higher required voltage, commonly around ±15V[23].

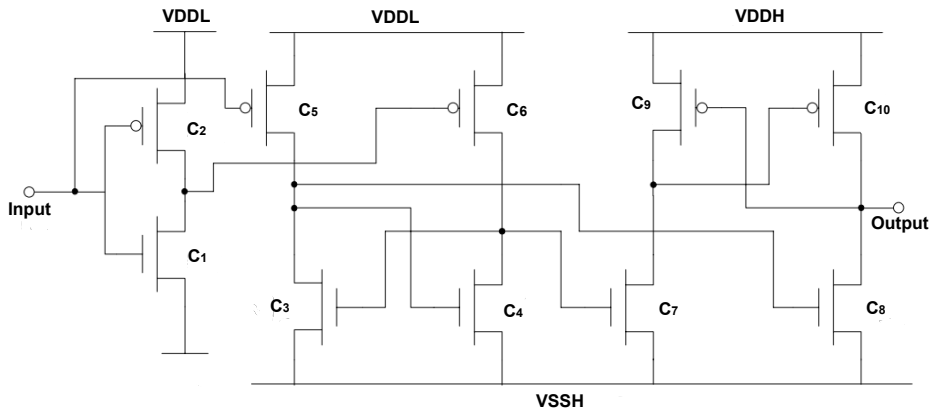


Figure 3.8: CMOS level shifter[23]

The CMOS level shifter is a common level shifter. It contains a CMOS inverter and two latches, as shown in Fig. 3.8. The first latch (C3-C6), supplied by VDDL-VSSH, is used for negative supply voltage where VDDL and VSSL represent the low voltages used for the digital logic. The second latch (C7-C10), supplied by VDDH-VSSH, is used for positive supply voltage and VDDH and VSSH represent the high driving voltages for the TFTs. The second latch can be directly driven by utilizing

the two outputs from the first latch without using any extra inverter. The level shifter is connected to the output buffer of the gate driver as a final step as can be seen in Fig. 3.9.

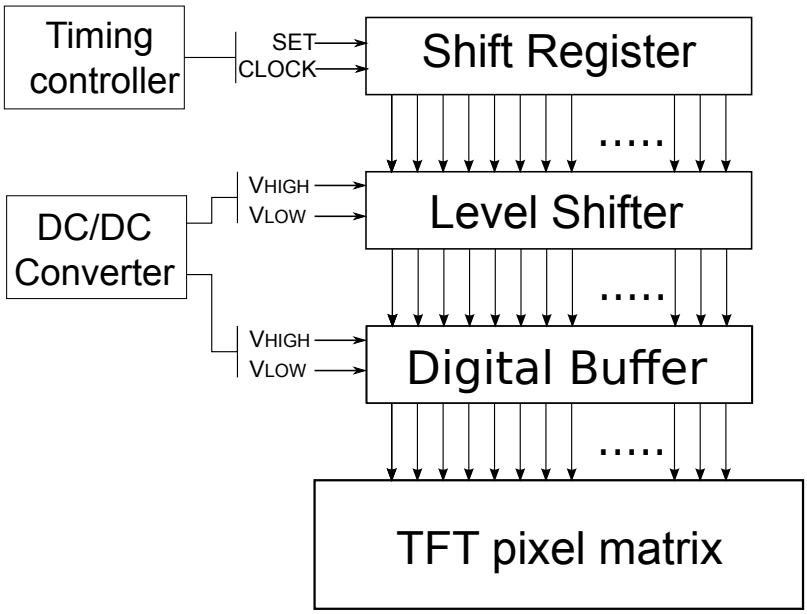


Figure 3.9: Block diagram of the gate driver[23]

3.3.4 Buffers

One major influence on displays these days is the display addressing which has a big impact on the image quality. The display addressing can be accomplished in different ways, but the most common ones, which are described previously on this chapter, are the passive and active matrix addressing.

In active matrix addressing, there are TFTs driven by voltage and their threshold voltage is critical. One of the disadvantages of using TFTs is the variation of the threshold voltage which is caused by random distribution of the grain boundaries in the poly-crystalline material of the TFT. These variation leads to dissimilarity of the brightness and color-scale of the sub-pixels. A way to avoid this kind of issues is to use an output buffer for the gate and data driver respectively in order to implement accurate voltages to the sub-pixels of the display despite the threshold voltage variations[29].

To be able to drive the output signals from the drivers with enough strength, an output buffer can be implemented. A single logic gate is not powerful enough to drive a large load at the output with enough speed. The output buffer can be designed in different ways. A simple but sufficient way to design and implement the buffer is to use inverter stages where the amount of parallel inverters on each stage increase, for example: 2, 4, 16 and 64, or a fan-out 4 delay metric which is the same for stages 4, 16 and 64. This type of output buffer minimizes the delay of the buffer

by increasing the inverters per stage and ensuring that each stage will have a load that can be driven with adequate speed.

The gate driver in this project includes a digital output buffer which has the function of improving the driving capability for the desired switching speed[23]. Buffers serve a more important part in high resolution and large-area displays. For the source driver, analog buffers are usually used to ensure voltage control for the display. However, decisions has been made to not use a digital to analog converter for the data driver since it does not require a high frequency update and analog data signals like in LCDs. Since the output of the data driver only needs a basic on and off regulation, a level shifter and output buffer configuration as shown in Fig. 3.9 can be also used for it.

4

Electrical modelling

Based on the information and the assumptions about the display properties and the TFT laid out in the previous sections, an effort has been made to create an electrical model of the whole TFT pixel, using an active matrix configuration. The purpose of this model is to provide an overview of the display's response to voltage changes and also to provide information about timing and power required to operate it. Cadence® Virtuoso® Analog Design Environment was used to design and simulate various pixel configurations. Specifically, the Cadence® Spectre® Circuit Simulator was used for SPICE-level simulation.

In every design many of the components were re-used. All the components used were taken from the *analoglib* library of Virtuoso®, just for simplicity. For voltage sources the components *vdc* and *vpulse* were used for DC and pulse voltage generation respectively. For resistances and capacitances the generic *res* and *cap* models were used. For the TFT, the built-in generic poly-Si TFT model from Rensselaer Polytechnic Institute (RPI) [30] was used, with default values.

The TFT channel width and length varied based on the size of the sample examined. The majority of the transistor parameter values have been chosen arbitrarily, since optimizing the TFT operation is outside of the scope of this thesis. One important parameter, which was taken into account, is the gate oxide thickness (T_{OX}), which affects the threshold voltage of the TFT. More specifically, with increasing thickness of the oxide semiconductor on the gate of the TFT, the threshold voltage level increases accordingly [31] and higher gate voltage is required to achieve the same drain current.

4.1 Simple EPD pixel

A first simulation was done for a simple active-matrix electrophoretic display (AM-EPD) cell described in [32] in order to determine the behavior of a typical EPD pixel and establish a reference for the Rdot pixel. As shown in Fig. 4.1, the TFT is controlled by a vpulse and enables the flow of current to the RC circuit. In this case, the resistor represents the load of the EPD cell and the capacitor is used as a storage capacitor. This particular EPD technology requires 15V/-15V to change state. The resistance value was 67.445 GΩ and the storage capacitance was 8.6 pF. The capacitance is chosen based on the time constant desired for the RC circuit. The potential across the resistor for a transient analysis of 1 s is shown in Fig. 4.2.

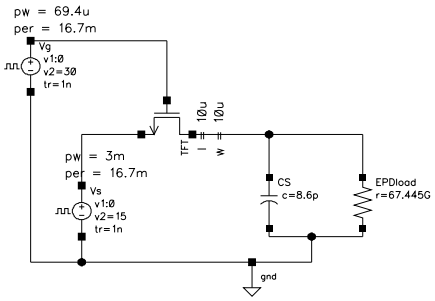


Figure 4.1: AM-EPD pixel schematic on Cadence Virtuoso.

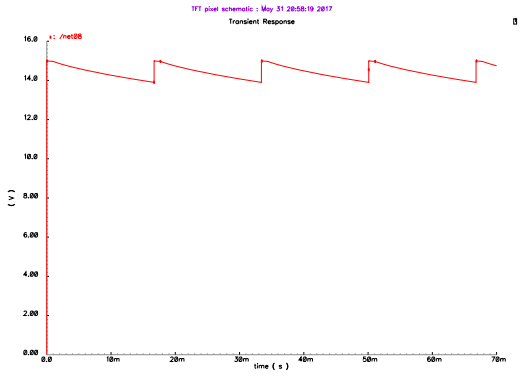


Figure 4.2: Voltage response for the AM-EPD pixel.

The gate pulse is 0.0694 ms long and it is supposed to charge the capacitor to a level where it can in turn maintain the voltage accross the resistor for 16.7 ms [32].

In this case, a very high gate voltage is needed to reach the required 15V potential. The TFT threshold voltage, resistance and size play a significant role for the performance of the circuit and its effects will be discussed later together with the simulation of the Rdot circuits. It is also shown in Fig. 4.2 that the capacitor discharges slowly and the voltage drops after the TFT is off. The point of this configuration is to maintain a voltage close enough to the desired voltage for the whole row-write time. In this case the voltage never drops below 14V (max is 15V) until the next time the row is activated. In this way, the addressing of all the rows can be done in significantly less time while also applying the required voltage for the required amount of time to change the state of the electrophoretic particles.

4.2 Rdot pixel for large size sample

Since most information available for the Rdot display is on large sample pixels (176 mm^2), the same size was used for the circuit simulation initially. Based on earlier assumptions, for a sample with an area of 176 mm^2 to be modeled as an RC circuit, with discrete components (resistor and capacitor), the resistance is approximately 2.027 KΩ (based on the average current and the energy density) and the capacitance of the sample has been calculated at approximately 500 µF. In Fig. 4.3, the corresponding pixel circuit is shown, designed based on the EPD cell earlier. In this case, since the material has such high capacitance, it has to be included in the model. Since the leakage is high for this large sized sample, it is not realistic to provide a constant voltage across it with only using a charged capacitor. Here, the TFT is connected to the ground instead of the source voltage, so the effect is going to be opposite (discharging when it is "on" and then maintaining low voltage).

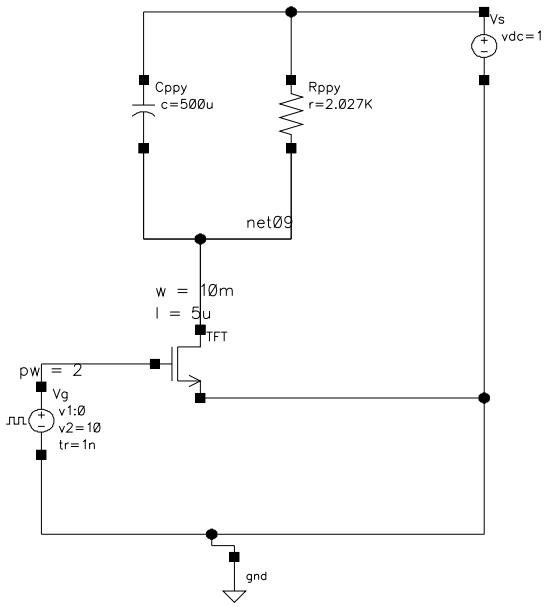


Figure 4.3: Rdot pixel schematic on Cadence Virtuoso for 176 mm^2 sample.

The voltage across the resistor can be seen in Fig. 4.4 and 4.5 for a transient analysis of 10 seconds. The TFT gate voltage pulse width was 2 sec and it was given at t = 1 sec. Two different gate voltages (V_g) were tested for the TFT. As described in section 3.2, due to their low mobility and high threshold voltages, the TFTs require gate voltage higher than the source voltage (around 5V) in order to be able to operate in the correct region. In addition to that, since the leakage of the material at this size is significant (very low resistance), the TFT channel width needed to be comparable in size, so that the channel ON resistance would be significantly smaller than the material resistance. This is the only case where the described model can work as intended and the assumptions made can be valid. The channel length was kept as short as possible (3 µm), since it affects the mobility, but the width was increased to 10 mm, which, in a real configuration, translates into several TFTs of smaller width in parallel.

Fig. 4.4 shows the response with a low V_g (5V higher than source voltage). The voltage drop is slow and the saturation happens at a quite high voltage level (around 200 mV) compared to the desired 0 V. Fig. 4.5 shows the response for high V_g (15V higher than source voltage). In this case it is obvious that the voltage drop is much faster and the saturation point is much closer to 0V. As indicated in section 3.2, there is a direct relation between I_{DS} and (V_{GS} - V_{th}), which means that for higher gate voltage the higher the current will saturate. Also, while the voltage on the observed node is dropping, V_{DS} is increasing, which is causing the transistor to not operate in the same region anymore. After these effects take place, a voltage division is created between the TFT resistance and the node resistance, determining the maximum voltage drop possible. Increasing V_{GS} essentially decreases the TFT resistance. It is generally advised to have one static voltage level for all the control TFTs (of the same layer), since there is a limited amount of logic voltages that can be used effectively. Based on these observations, it may be beneficial to use a higher

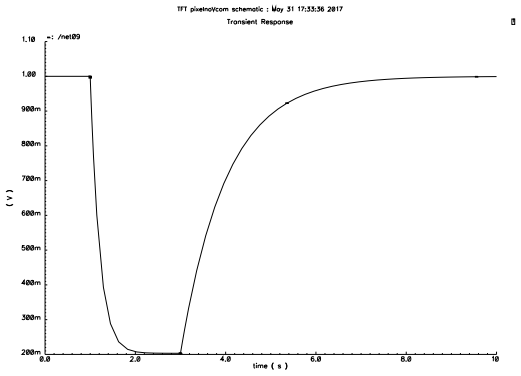


Figure 4.4: Voltage across the transistor for the large Rdot pixel for V_{GS}=10V.

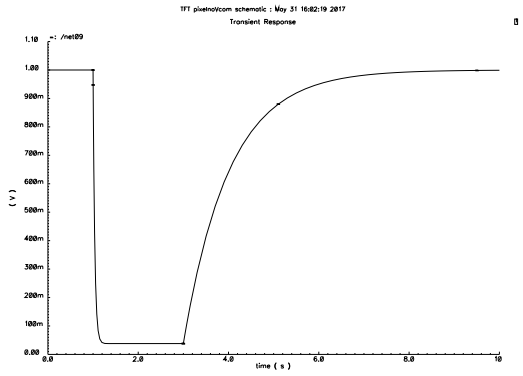


Figure 4.5: Voltage across the transistor for the large Rdot pixel for V_{GS}=25V.

source voltage in order to reach the desired voltage on the node (across the pixel). Choosing the appropriate voltage requires further experimentation on a real sample though, since higher voltages can damage the metasurface irreversibly.

The configuration at Fig. 4.3 requires either direct or passive matrix addressing, since the TFT needs to be on for the whole duration of the frame. Since the sample simulated is quite large for a typical display, it is unlikely that it will be used in a real application. The results seen here though indicate that for lower resolution displays using the Rdot technology, where the pixels will be in the millimeter range, similar timing will be required as well. In that case, a different configuration is proposed, to be used with an active-matrix addressing scheme, shown in Fig. 4.6.

Here, the TFT gate capacitance, modelled externally by a discrete capacitor, is used as a storage capacitor for the TFT gate. In practice, the first TFT, TFT-Gate, when "on", allows a small current to charge the gate capacitance of the second TFT, then quickly shuts off, which leaves this capacitance to maintain the voltage on the gate for longer time. The charge of the gate capacitance slowly leaks through the gate to the substrate, so this effect can only be maintained for a certain amount of time. The limitation with this technique is that the gate capacitance of the second transistor, C-Gate, needs to be significantly larger than the drain capacitance of the TFT-Gate, otherwise the TFT-Gate channel is turned on and high leakage is observed. Also, since the TFT capacitances are secondary parameters outside of the scope of this thesis, the exact phenomenon cannot be simulated, so a discrete capacitor is used instead.

The resulting voltage response on the node of interest (across the pixel) is shown in Fig. 4.7. The gate pulse width in this case was only 100 ms, more than enough to charge the capacitor and maintain a high enough voltage on the TFT gate in order to maintain a steady voltage across the pixel for several seconds. Further optimization

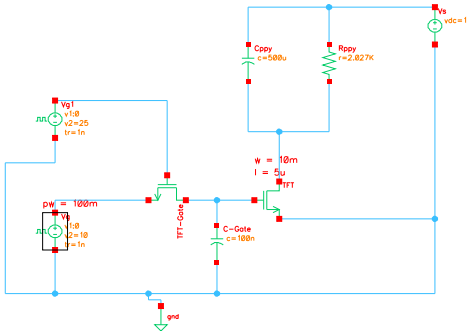


Figure 4.6: Schematic of large sample circuit with double TFT.

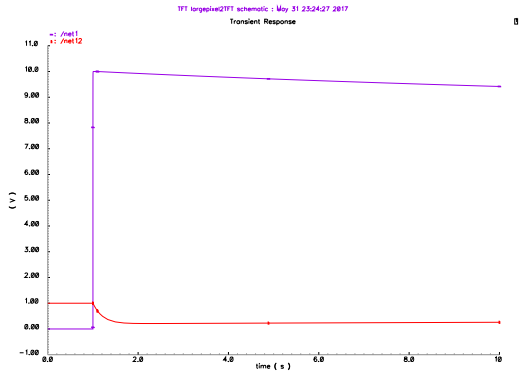


Figure 4.7: Simulation of the double TFT configuration. Voltage across the pixel is in red and at the TFT gate is in purple.

can be made on this configuration to find the ideal gate capacitance value to maintain the voltage level for at least 2 seconds, but it will not be examined at this point, as the purpose was to demonstrate that the AM driving scheme is possible even for larger pixel sizes.

4.3 Rdot small size pixel

Since the intention for the Rdot technology is to be used in real display applications, the pixel size should get smaller (sub-millimeter range). It is claimed that the Rdot technology can reach a density as high as 10000 dpi (dots per inch) [9], which would make the pixel area approximately $9\,\mu m^2$. Since the controller and the driver electronics have to be developed for an actual display, it is beneficial to model the small size pixel as well and observe its behavior.

After scaling the pixel size (area) down, its capacitance and resistance have to be scaled as well. For a $9\,\mu m^2$ Rdot pixel, $C_{PPy} = 25.6$ pF and $R_{PPy} = 39.639\,G\Omega$ approximately. The TFT size had to be scaled down accordingly, since it has to be significantly smaller in size than the pixel it controls. In this case, it was scaled down to $W = 1\,\mu m$ and $L = 500\,nm$, which would make the occupied area of the transistor (including the electrode area) almost a third of the pixel area. Since the RPI TFT model is not as modern, its behavior in such small sizes is unknown, so further experimentation is advised with more modern TFT models. This will not be done in this thesis, since it is outside of the scope. The circuit schematic for the small pixel is shown in Fig. 4.8.

The result of a transient analysis of 10 seconds is shown in Fig. 4.9a. The gate voltage pulse is only 1 ms short and is repeated after 5 sec. Fig. 4.9b shows the

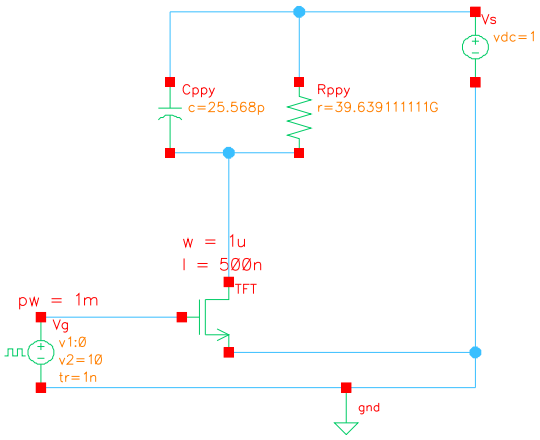
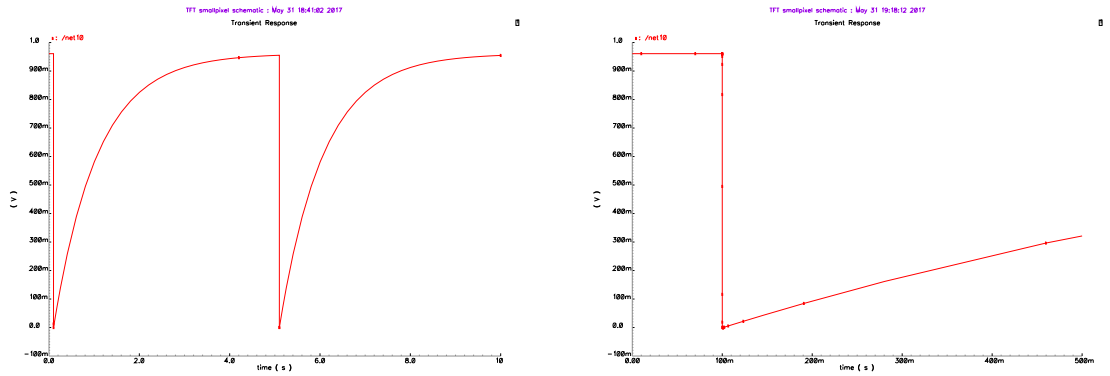


Figure 4.8: Rdot pixel schematic for minimum size pixel on Cadence Virtuoso.

voltage curve zoomed in at millisecond range. For a pixel of this size, the reported time from maximum to minimum absorption is less than 500 ms [9], as long as constant -1V is applied. As shown in Fig. 4.9b, the internal pixel capacitance is capable of storing enough charge to maintain 90% of the voltage difference for more than 100 ms. This indicates that no external storage capacitor is required for an AM driving scheme to be possible. The behavior is similar to the AM-EPD cell discussed earlier, which is known to work as intended. Based on that, it can be assumed that this model will also work as intended if a frame-write time of maximum 100 ms is chosen, so the voltage can be maintained near the desired level for as long as needed. These observations can provide critical information for the design of the display controller and the timing in which it needs to operate.



(a) **(b)**

Figure 4.9: a)Voltage across the resistor for the small Rdot pixel. b)Voltage curve zoomed in at millisecond scale.

5
Digital controller design

The Rdot display requires specific driving signals with appropriate power levels and timing so it can operate in a functioning manner. This chapter will discuss how the digital controller is design, which components are used and their function, how the appropriate voltage is fed from the driver electronics to the pixel and how the address timing of each pixel is controlled, in order to satisfy the requirements and constraints determined in the previous chapters.

5.1 Digital control units

This section covers necessary information about the code implementation for the display controller. The analog simulations of the Rdot display in section 4 showed that, with the provided information and with certain assumptions in mind, active matrix addressing is possible for this technology. The digital display controller was designed in parallel with the analog modelling, following the active matrix driving scheme and some initial conditions. More specifically, it is assumed here that any active matrix cell properties used in other similar technologies are sufficient for Rdot technology as well (such as storage capacitor and TFT sizes). Also, the maximum timing for a transition of a pixel from the lowest to the highest optical absorption level (white to black) and reverse (black to white) is assumed to be 500 ms. Furthermore, the display is considered to be bistable, meaning the pixels maintain their optical absorption levels when no voltage is applied (when the driver is "off"), whereas in reality, at the current technology state, the display requires a small periodic negative voltage in order to retain an image. A description of the components used in the controller is given and the operational scheme of the controller is explained.

5.1.1 De-multiplexer (deMUX)

The demultiplexer, referred to as demux from this point on, is a digital circuit that converts a single input data line into several individual output lines based on some conditions. For a number of n conditions or select lines, there are 2^n possible outputs. It can be used to transition from a serial data input to a parallel data output.

The main purpose of using a demux in this project is as a decoder. It receives the input of the system, which is a 10-bit binary word, and breaks it down into several different outputs to be used as inputs in other components. More specifically, the

10-bit input contains information bits about the desired color state of each sub-pixel and also some synchronization signals, such as vsync and hsync. The first 6 bits are used for color information (2 bits per color) and are translated into integer outputs to be used in the look-up tables. The rest of the bits are assigned to vsync, hsync and enable signals to help synchronize the controller with other systems.

5.1.2 Lookup table

A look-up table (LUT) is a structure used to replace the computational effort for a function. In digital logic in particular, a LUT is a component that can simulate any boolean function by storing its truth table. There are two ways to construct and operate a LUT: either with a decoder (static) or with D-latches (reconfigurable).

In this work, look-up tables are used in order to store the driving waveforms for the column drivers (data). Based on the received input from the system, a choice of Color State (CS) is done and the appropriate driving waveform is then accessed, represented by a digital voltage (1/0) on every consecutive frame (F1-10). Each frame represents a set amount of time, which is based on the display refresh rate and the number of fractions we want to divide it into. The driving waveform should be chosen in such a way as to average a specific voltage over one refresh cycle, in order to reach a specific color state. There is one LUT dedicated to each color in the system. The LUT presented on Table 5.1 is a simple early version of the final LUT, which will also include a third input metric (previous state) and possibly more color states and frames.

Table 5.1: Look-up table (LUT) configuration for driving the different color states.

	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
CS1	0	0	0	0	0	0	0	0	0	0
CS2	0	0	0	0	0	0	1	1	1	1
CS3	0	0	0	1	1	1	1	1	1	1
CS4	1	1	1	1	1	1	1	1	1	1

5.1.3 Gate driver

The main purpose of the gate driver, also referred to as the row driver, is to activate all the transistors in a single row of the active matrix array. The process of the driver can be described as a generation of a gate pulse that controls a specific row of pixels through the TFTs connected to each pixel on that row. By turning on and off the switch TFT device for each pixel, the pixels can be programmed.

The gate driver is implemented through a simple shift register as a first step where the length of the register depends on the amount of rows used for the display. A voltage level shifter is implemented as a second step with the purpose of shifting the voltage level for the interfacing between the gate driver and the rows. As a last step, buffers are used to drive the capacitive loads.

The shifted serial output is fed back to the input since continuous writing is desired. The concept of this register is to use a logic 1 that travels through the shift register meanwhile all other bits in the register are zero. This brings out the result of having only one line activated out of the total number of lines. The whole frame is scanned one line after the other by the gate driver.

5.1.4 Data driver

In addition to the gate driver, there is also a data driver whose purpose is to take care of the incoming data. It gathers the data serially and then forwards the correct digital data to the columns in the active matrix TFT.

The data driver is implemented through a shift register and output buffer. The purpose of the shift register is to serially shift in the input data bits and store them there. The register is a serial-to-parallel shift register which shifts in data corresponding to all column lines. The amount of bits stored in the register corresponds to the amount of columns used in the active matrix TFT. The data stored in the shift register are latched out in parallel to the output register when an update signal is set. This enables the driver to write data on a row while simultaneously shifting in new data for the next row.

The circuit part of the data driver, which is interfaced with the digital output register, needs structures to convert the digital information into actual voltages for the columns. This is usually achieved with individual digital-to-analog converters (DACs) at every column, since most displays have variable voltage levels. In the case of Rdot and this controller, the addressing is done in a digital way and various voltage levels are achieved through averaging of a DC voltage in a certain amount of time. As such, the electronic structure of the data driver can be similar to the gate driver, using a level shifter or a switch connected to the DC source of the system. An output buffer is also needed as a final step in order to be able to drive the large capacitive loads of the columns.

5.1.5 Timing control

One of the most important sub components within the display organization is the timing control which can be seen as the "brain" controlling the synchronization of the gate and data drivers using the synchronization signals *hsync* and *vsync*. These synchronization signals are used in the gate driver to determine when to select a new row, but also when to write and erase. For the data driver, they are used to indicate when to shift in and when to output data with correct timing.

5.2 Display module architectural design

This section covers the architecture of the display module on block level. The design of the display module will be described in a basic functionality through a system level block diagram together with the construction of the different parts in this block. After literature studies on similar technologies, assumptions and design concepts

have been made. The driving of the display is based on research of technologies using a TFT active matrix which can be adjusted and applied for this project. The design was made in VHDL with the main features for these components.

The intention with this circuit is to generate driving voltages with correct timing to change the pixels in the display and address the right data for these pixels. This section will describe the design methodology of the different blocks connected together. Since this is a simplified description of how the display can be driven, only the most important aspects on how to drive the display will be described.

5.2.1 System level block diagram

As mentioned earlier, the components are designed in VHDL using Modelsim. The different components were verified through simulations and tests for accurate operation. Through structural design, the gate driver is broken down to a gate unit which corresponds to one row. This unit is then copied to the amount of rows that were used for the display, which for a first test case is 10 rows, and the result is a complete gate driver.The same principle goes with the data driver where a data unit is constructed and copied the necessary amount of times (10 columns in the test case) which make up the whole data driver.

The display module can be controlled by a microcontroller unit but also by a Field-Programmable Gate Array(FPGA) which is used in this project. The main purpose of the FPGA board is to act like a communication interface to the display module and provide important parameters such as clock signal, power and image data. The image data will be located in a memory in the FPGA. A block diagram can be seen in Fig. 5.1.

The most important parts in this diagram are the gate and data drivers, the timing controller and the DC/DC-converter but also the common electrode driver (Vcom in Fig. 5.1). The common electrode is shared between all pixels on the display and it is the indium tin oxide (ITO) plane which is located at the top of the display. It is transparent and electrically conductive. The board has the responsibility of handling the incoming data from memory, providing it with the right timing (from the timing controller) to the data driver and also providing power for updating the display.

The whole operation for the image data bits to travel from memory until being translated to voltages for the pixels for a specific image can be described as following:

An image is converted into data bits and stored in the memory. When the operation starts, the data bits are transmitted into the FPGA and thereafter shifted into a demultiplexer(deMUX). The purpose of using a deMUX is to separate the bits according to the colors red, green and blue, see subsection 5.1.1 for more information about the deMUX.

Since the data columns of the active matrix TFT are receiving driving waveforms to generate the desired pixels, a lookup table(LUT) is needed. This is the next step in the operation where the bits for the different color data are transmitted to a

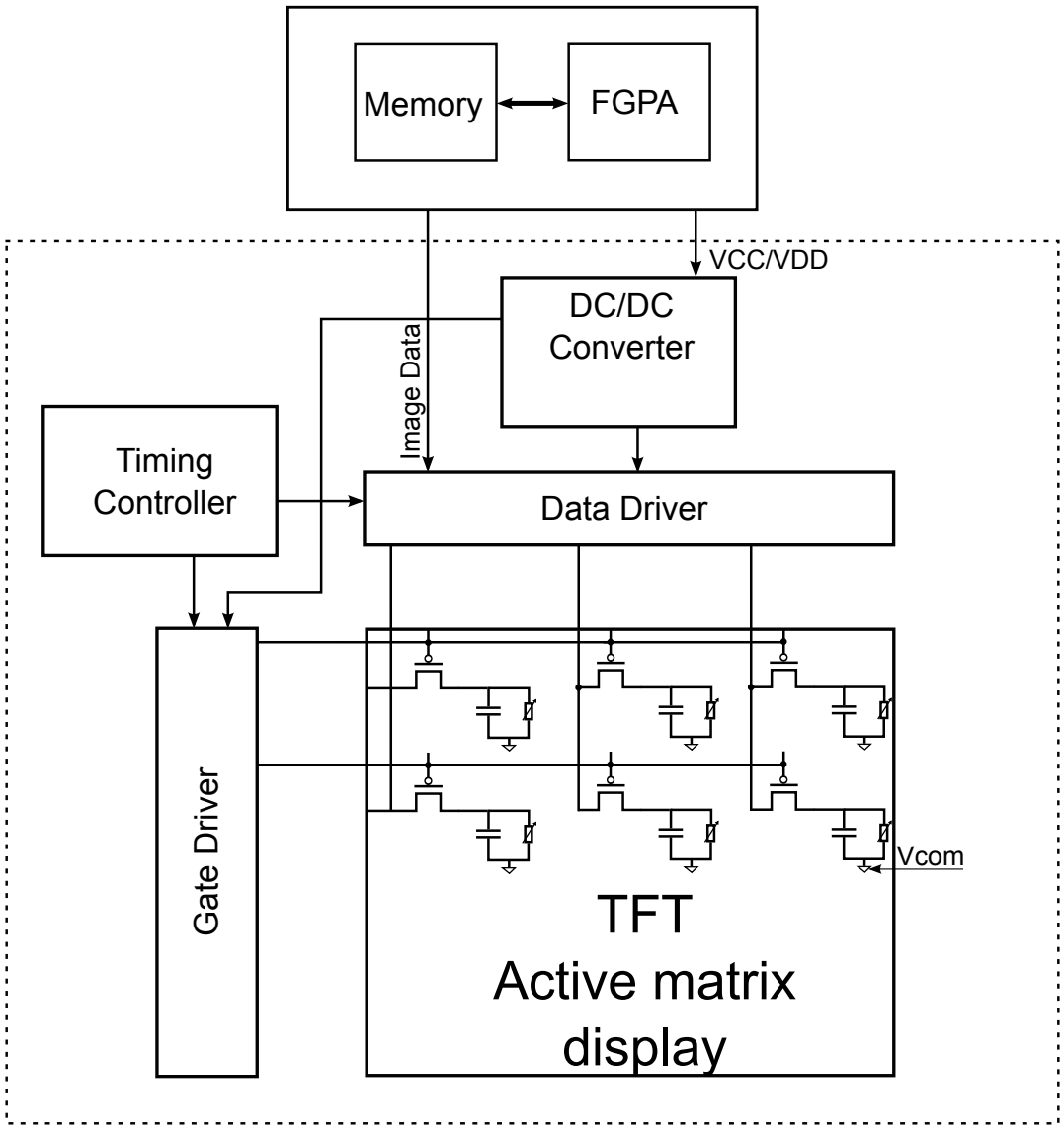


Figure 5.1: A block diagram of the system

LUT. The input to this component determines which color state should be chosen as a digital voltage(1/0) according to the selected driving waveform for that specific color state, see subsection 5.1.2.

The output from the LUT is connected to the data driver where serial-to-parallel shift registers are used to transmit the voltage information for each subpixel. There are three separate shift registers representing information for the RGB colors.

This data is handled by the data driver and its components, the color driver and data unit. The operation in this stage is controlled by the two synchronization signals, *hsync* and *vsync*. During every pixel clock cycle, a new desired voltage bit for a specific pixel is shifted into the shift register. When a whole row of pixels is filled, the register retains the data until the *hsync* signal is deactivated, at which point the shift register pushes the data to the output register, which in turn is connected with the columns. The data driver is then ready to start shifting in new data for the next

row, without disrupting the current output. At the same time, the contents of the gate driver's shift register are shifted by one bit, so a new row is activated. These outputs are synchronized (with *hsync*) in order to activate the TFT and provide the voltage data at the same time. A more detailed description of the data and gate drivers and their components can be seen in section 5.2.2.

The operation described above happens continuously until all the rows have been addressed. In the meantime, *vsync* stays high to indicate that one frame is being written. As soon as all the rows have been addressed, *vsync* goes low and a new frame starts. The timings for the operation can be seen in Fig. 5.2 where the top image shows data transmitted for one row during the activation of *hsync*. The bottom image shows the input data for all the rows on the display during the time when *vsync* is activated and *hsync* is activated for every row.

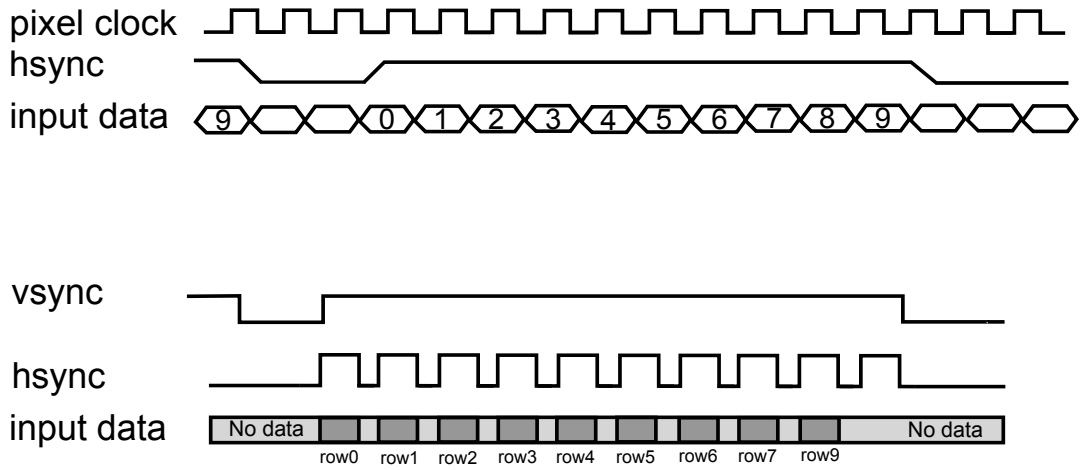


Figure 5.2: Horizontal and vertical timing properties

5.2.2 Design implementation for the display module

The different blocks in the display module with their inputs and outputs can be seen in Fig. 5.3. The source driver receives serial pixel data for the three subpixels(red, green and blue) which then need to be converted into positive or negative driving voltages dependent on the value of the data. This should then be the output to the columns for the TFT active matrix. The size of the display determines how many outputs should be connected to the columns. In this project, as a first test configuration, it has been decided to stick to a parallel output of 10 bits of data. This decision is made from the fact that the module should be working for test cases in the beginning and it would then be easier to implement a larger size. The data driver output can be seen in Fig. 5.3, where 10 output bits are located for each of the colors *red(R_out)*, *green(G_out)*, and *blue(B_out)*.

The gate driver has also only 10 bits of output(*Row_out*) which can be seen in Fig. 5.3. The gate and source drivers need to be synchronized and should be able to receive the hsync and vsync signals from the timing controller. Besides the

synchronization signals, they should also be able to take in the clock signal(pxl_clk), a common reset signal(Reset), an erase signal(erase) and a start pulse(start).

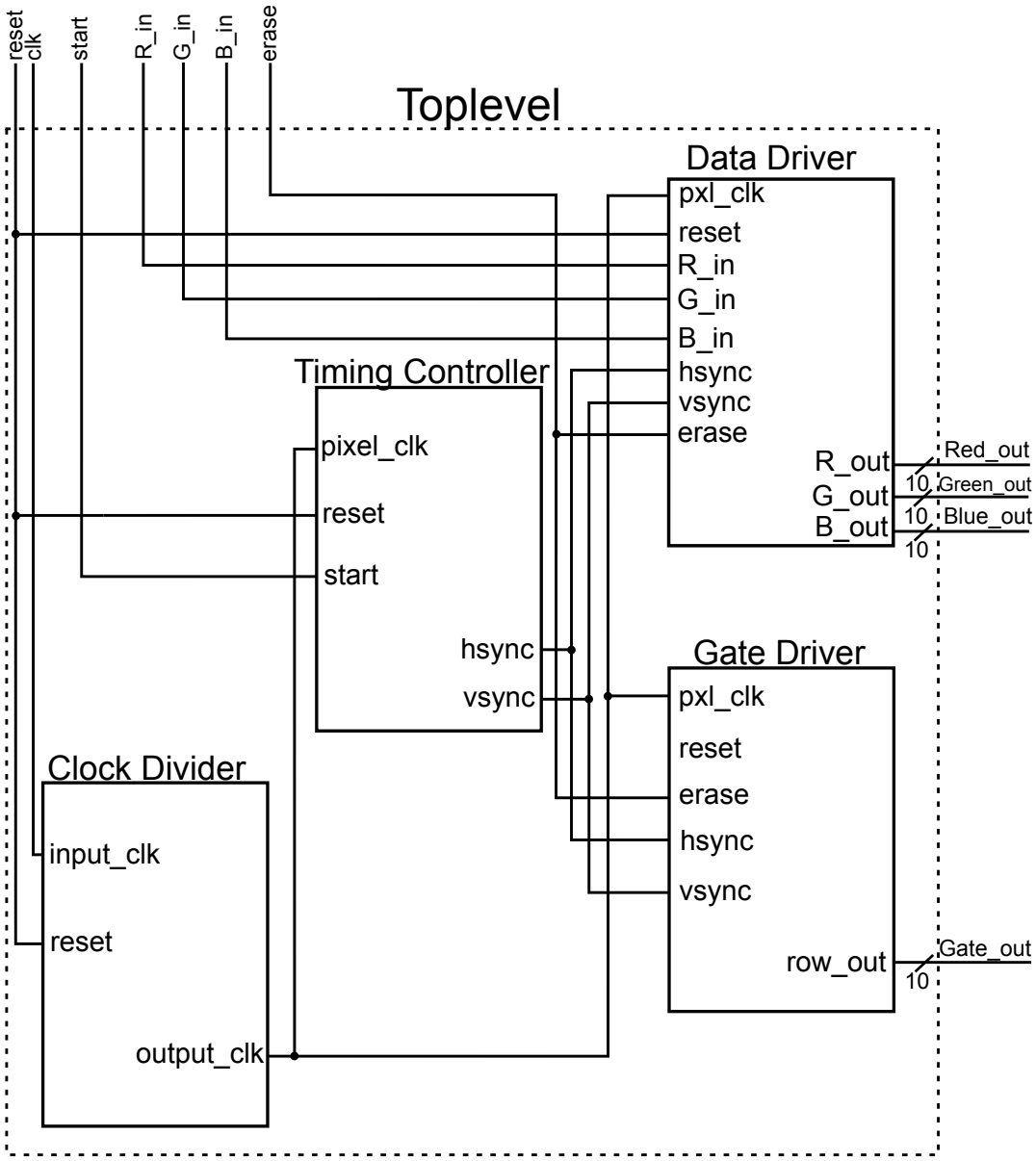


Figure 5.3: The toplevel schematic for the VHDL implementation

The timing controller has the responsibility of receiving the clock signal(pixel_clk) and the start signal(start) and output the synchronization signals(*hsync* and *vsync*) to the data and gate driver. It should be synchronized so every time the data driver is finished with outputting data to one column, the gate driver should advance to the next row.

5.2.3 Gate driver

The gate driver is one of the most important components in this design. The main purpose of the gate driver is to control the rows on the TFT active matrix. As

mentioned earlier in this section, there is only 10 bits out from the gate driver for testing purposes only. This can of course be changed easily in the code but as a first development stage, 10 rows has been selected as the number of rows. Fig. 5.4 shows a schematic of the design made in VHDL. As mentioned earlier, the gate driver is built up through a structural design which means that it is connected through different parts.

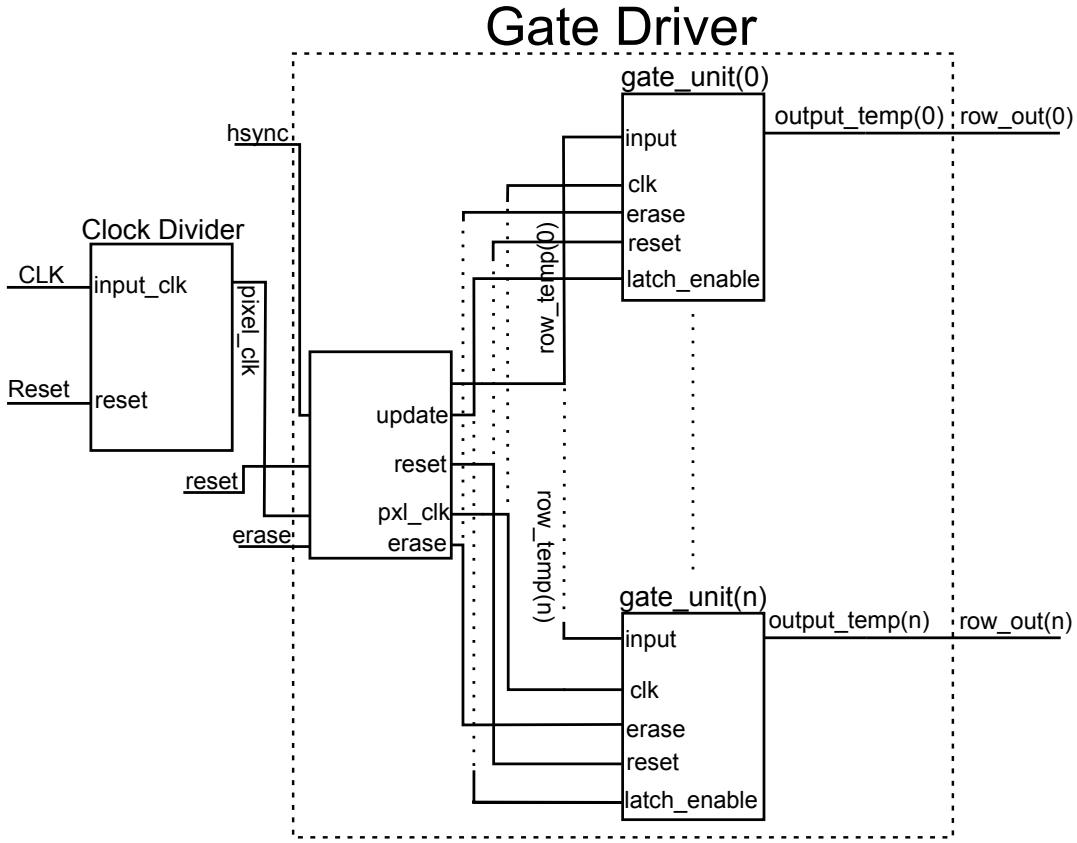


Figure 5.4: A schematic of the Gate Driver implemented in VHDL

The subcomponent for the gate driver is called gate unit. The gate driver uses the unit 10 times which corresponds to the 10 rows conected to it. In the Toplevel design, which is shown in Fig. 5.3, it can be seen that a clock divider is used as a component which generates a clock with lower frequency than the one used from the FPGA and the clock signal coming out from the component is called *pixel_clk*.

The different inputs and outputs are described below according to Fig. 5.4:

hsync:
The *hsync* input is one of the most important inputs to the gate driver since it controls the changing of rows. This signal is created in the timing controller and connected to the gate driver in the toplevel. The signal works like a clock and during the active cycle of it, all the data should be transmitted to the columns on the active row. When the signal is deactivated, a row shift should be made.

erase:
The *erase* input is a signal also generated in the toplevel. The signal has the purpose of erasing the display row. This is accomplished by erasing all the columns in every row starting from the top to the bottom.

update:
As the signal name describes, this is an update signal whose purpose is to update the driver and change to the next row. The signal is connected to the input signal *hsync* and the to the signal *latch_enable* on the data unit. When *hsync* is deactivated(signal is low), the update signal is activated which in other words means that a row change is done every time *hsync* goes low.

row_temp:
This is a 10 bit vector signal connected to the input of the gate units. The *input* signal on the gate units receives one bit at a time from the *row_temp* register and when the update signal is activated, it outputs the bit to the *output_temp* signal.

output_temp:
As previously described, the *output_temp* signal is the output from the gate units and it is a 10 bit vector. This signal is connected to the output from the gate driver called *row_out* which also is a 10 bit vector.

row_out:
Finally, the gate driver contains a 10 bit output vector called *row_out* which is used as an output from the whole system connected to the gates on the TFTs of the adressed row.

5.2.4 Data driver

The data driver is another one of the most important components in this design. The purpose of the color driver is to separate the three different RGB inputs and run them simultaneously. The data driver has the responsibility to transmit data to the columns on the TFT active matrix connected to the display. The data driver is written in VHDL as a structural design and it is composed of color drivers and data units as can be seen in Fig. 5.5. The color driver is implemented for the red, green and blue(RGB) color data and these are connected to one column each for each pixel (so each pixel has 3 subpixels). As described before in this section, the data driver output for the RGB colors is a 10 bit output vector. The decision for the vector size is based on the fact that it is easier to verify and test it as a first development step.

The clock divider in Fig. 5.5 works the same way as for the gate driver which was described in subsection 5.2.3. The data driver receives different inputs and they will be described below:

Red_in:
This is the input signal data for the red color which is shifted in serially to the data driver and it is connected to the *color_in* input on the color driver. The incoming

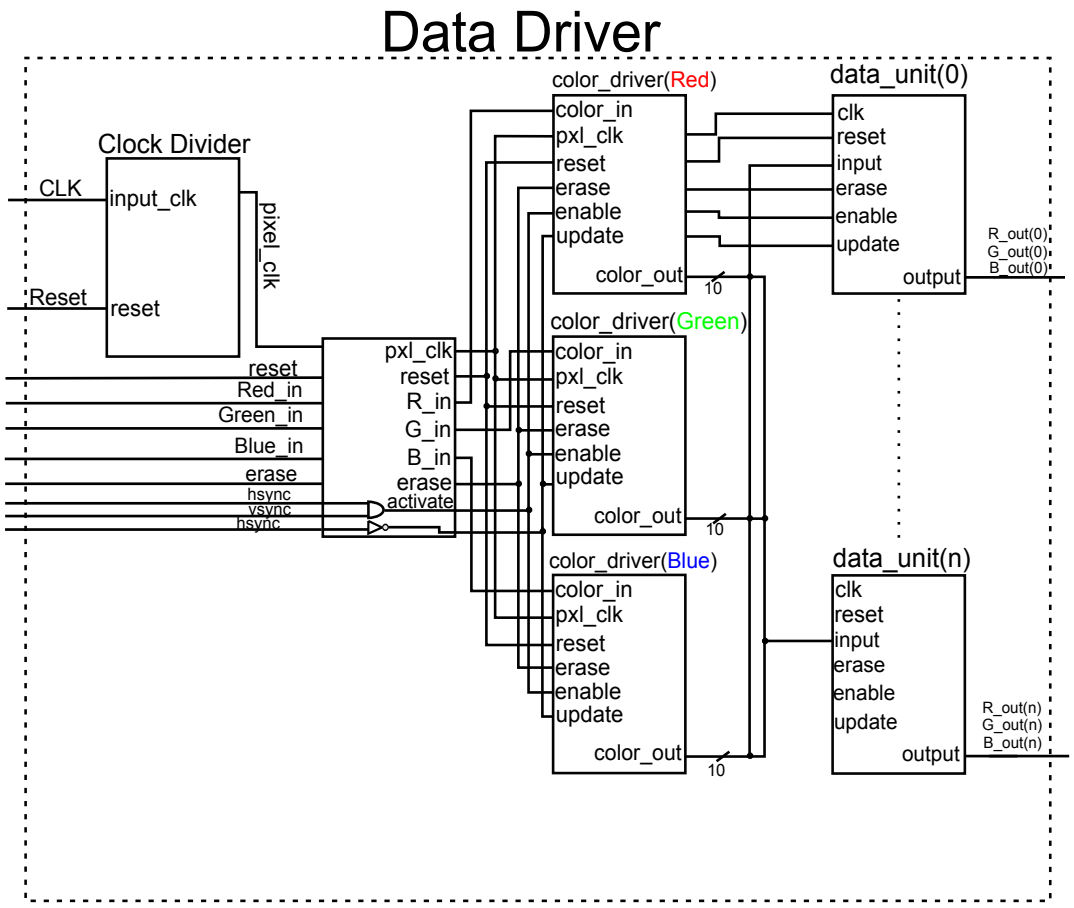


Figure 5.5: A schematic of the Data Driver implemented in VHDL

bits contain the data information and are later transmitted to the columns of the TFT active matrix. The same thing goes for the *G_in* and *B_in* signals which represent the green and blue color information respectively.

erase:
The erase input works the same way as for the gate driver. The purpose of this signal is to delete the data on every column on the display. If this signal is activated, all columns will be set to 1.

hsync and vsync:
The *hsync* and *vsync* input signals are two synchronization signals generated from the timing controller. They are really important for this design since they determine when to shift to next row but also when to shift in data to the driver. The two synchronization signals are connected to an AND gate as can be seen in Fig. 5.5. These signals are then connected to the *activate* signal. Both *hsync* and *vsync* need to be set to 1 for data to be shifted into the driver. *Vsync* should be set to 1 during the operation to fill up all columns in every row with data.

When *activate* is set to 1, which happens when *hsync* and *vsync* both are active, the enable signal input to the color driver shifts in the data. Thereafter, when *hsync* is

inactive, the update signal is set to one and data are shifted out in parallel to all columns.

It can be seen in Fig. 5.5 that the *hsync* input signal is also connected to a NOT gate and the update signal on the color driver. This results in the data being shifted to the output buffers when the *hsync* goes to a low state (so when the row changes). The reason why the driver is designed with two stages, one to shift in data and one to output data, is because the row should be addressed with new data without interrupting the operation to prepare the data for the next row. This, in turn, increases the addressing speed.

color_out:
color_out is a 10 bit output signal from the three different color drivers and each of them contains the data bits for a pixel. This signal is connected to the input signal named *input* on the data unit. During an operation when *enable* is set to one, one bit at a time is shifted in to the unit and shifted out parallel to a column as soon as *update* is activated, which also was describe above.

R_out:
The 10 bit outputs from the data driver are called *R_out*, *G_out* and *B_out*. These outputs are connected to the *output* signal in the data unit and the data are shifted out in parallel for the three colors to the columns. This happens during one cycle of *hsync* and when *vsync* is set to 1.

5.2.5 Timing controller design

The timing controller is intended to act as the "brain" which controls the gate and data driver. The controller uses the synchronization signals hsync and vsync. It is designed in VHDL and implemented in the FPGA. The design methodology is simple in this project since it is a first design stage for testing purposes but it can be even more developed for future work.

As can be seen in Fig. 5.6, the timing controller is very basic. It uses the downscaled clock from the component called clock divider as an input to the controller. By using counters and variables containing the row/columns sizes, it generates the two synchronization signals, *hsync* and *vsync* as an output.

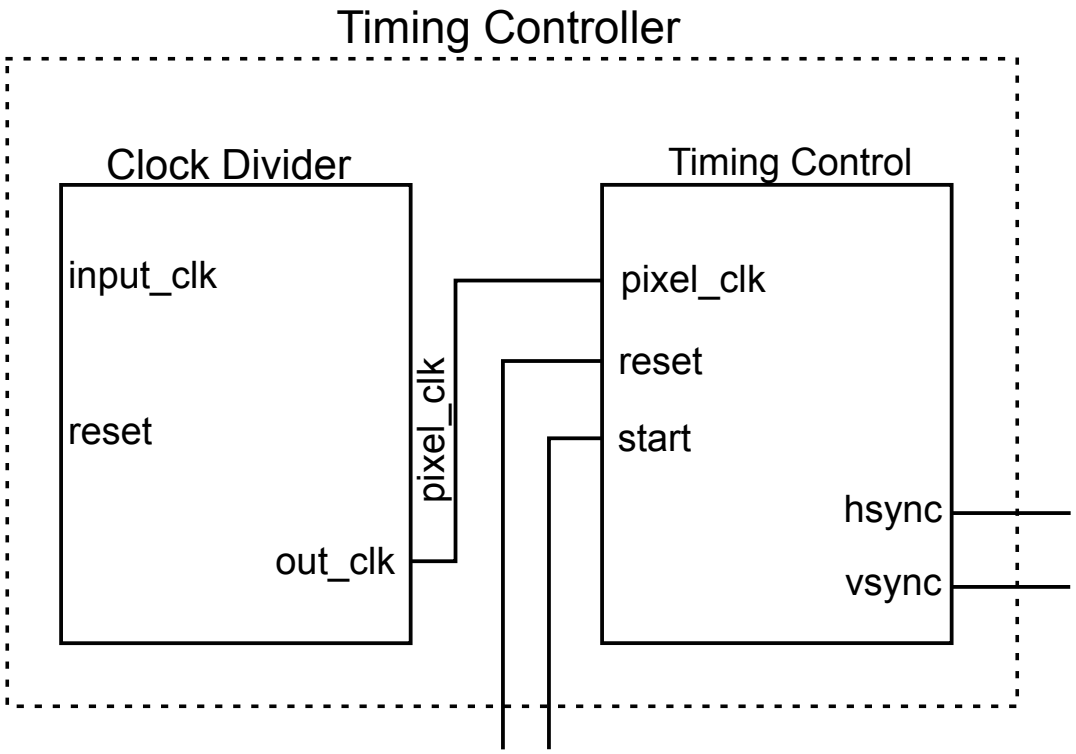


Figure 5.6: A schematic of the Timing Controller implemented in VHDL

6

Conclusion

6.1 Summary

The Rdot display technology has been introduced as an advancement over the monocolor and greyscale reflective display technologies that dominate the market at this time. The structure and operating principles of the Rdot display have been explained, followed by an analysis of its properties, with a focus on determining its electrical properties. Several assumptions had to be made based on the already available information and it was determined that this technology has relatively high leakage current (low resistivity per area unit) and large capacitance. It was decided that the best way to model an Rdot pixel, with the given information in mind, was with an RC circuit using discrete components, e.g. a capacitor and a resistor in parallel. This electrical modelling was done using Cadence® Virtuoso® ADE and running SPICE-level simulations. A simple circuit model of an EPD display was first simulated to set a reference point for the Rdot display simulations. Following that, both a large size and minimum size pixel of the Rdot technology were modelled as circuits and simulated and it was determined that both can be addressed with an active matrix configuration. Specifically for the minimum size pixel, its behavior was very similar to the reference EPD pixel and its capacitance was large enough to make the use of a storage capacitor obsolete. An important observation, though, is that this technology exhibits very high current leakage per unit of area, which translates to high power consumption.

Based on the information gathered from analyzing the display properties and running circuit simulations, a digital display controller concept was proposed and developed. A system description was laid out with all the blocks and components used and it was developed in VHDL. A short description of how the peripheral electronic circuits, namely the gate and data drivers, can be constructed was also given. Assuming the logic circuits are driven by 1V source, the data driver can directly drive the pixels without the need for a level shifter, since the required driving voltage is also 1V. Higher voltage is needed in the gate driver output, though, to drive the TFT gates. It was also explained how different grey levels can be achieved without the need for DACs at the driver output but by averaging a voltage through applying DC voltage on specific timeslots. Finally, the design implementation of the digital controller was described in detail, showing all the input and output signals and the operating principles. The design was also mapped and simulated on an FPGA.

6.2 Initial goals and deviations from the original plan

The goal of this project initially was to design a simple and reliable display controller in combination with the control electronic circuits for the plasmonic display material. The system should have been able to receive input from a computer or from an internal pattern generator with information about the displayed image, such as color levels of each pixel and synchronization signals. The controller should then have been able to choose the appropriate driving waveforms to control the voltage applied to the polymer in order to change the brightness of each color. At the end of this project it was expected to have demonstrated a proof of concept for the controller and the peripheral circuits to be able to control a multi-pixel display.

The initial main goal of this thesis was to develop a functional system consisting of two parts:

- The display controller, which handles the timing and would initially receive input from a bitmap stored in an internal pattern generator.
- The peripheral driving circuits connected to the TFT on the pixels that control the voltage to the polymer to create different colors.

A simple working prototype was also intended as an initial goal, since there was limited time and resources available. Finally, a sample that would be provided by Rdot was planned to be tested.

The RGB pixel developed by the company responsible for this thesis project was planned to be ready for testing. However, due to complications and delays in providing this pixel outside a lab environment, there has been no opportunity to work with it for this project. This was a big obstacle, since the only option left was to model the technology as a circuit instead and simulate its behavior. This of course leads to many assumptions and uncertainties. It also made it impossible for any kind of hardware implementation of the driving circuitry to be developed due to lack of time.

An electrical model was decided to be described, designed and simulated instead through a SPICE netlist or a circuit design tool. The electrical properties of the polymer electrode has been investigated and represented as a combination of discrete components. such as capacitors and resistors. The accurate simulation of one pixel's properties can allow of a larger scale simulation of several pixels. The initial goals for the digital display controller were, for the most part, achieved.

6.3 Discussion

One aspect of the Rdot technology that was observed in this thesis and can stir some discussion is the very high power consumption in combination with very high resolution capabilities. In the introduction of the initial publication of this technology [9] it is claimed that the power consumption is somewhere below $0.5\,\mathrm{mW/cm^2}$, which probably accounts for idle time as well. The average drawn current for one

switch for the 176 mm^2 sample was calculated at 1.4 mA, which would indicate a 1.4 mW for the same sample for one switch. But, since the leakage current is 3 times smaller than that, then the above estimation of power per area is feasible. This poses a big obstacle for the use of this technology in larger displays, since the overall power consumption would be much larger than other similar displays. Of course, it has to be noted that all these conclusions are based on only published results and assumptions made surrounding these. The company owning the technology is claiming that it can rival other reflective technologies and replace them in already existing applications.

Based on the observations in this thesis though, there can be a discussion on the applications of a display technology with extremely sharp resolution and high power consumption on a small area. In recent years there has been some research dedicated to creating micro-displays, that is displays at the size of a few millimeters. These displays can be used for near-eye display applications, e.g. as a part of smart glasses, or for augmented reality applications (which again are near-eye distance). There are already other technologies that ventured in this field of microdisplays, such as microOLED. A limitation for the Rdot technology to be used in some near-eye display applications could be its response time, which is not fast enough to display animated images at an acceptable framerate yet.

7
Future work

There are some improvements and further work that can be made for this project. One of them, which could be considered as one of the most important things, is to test the validity of the results for a specific pixel when it is ready to be brought out from the lab. As already stated in this report, the pixel has not been ready to be tested outside the lab together with the controllers and electronics.

The pixel can first be tested and verified together with the display controller where validity of the timing results would be the most important parameter to investigate. Since the pixel should be connected to a TFT according to the design in this project, testing and verification for the peripheral driving circuits together with the pixel should also be included as a future work.

Testing the whole system concept should be considered as a next step as soon as the multipixel display is available. The timing will here be more challenging since more pixels are considered to be driven simultaneously. The whole system should be working correctly with the synchronization signals controlling the writing of data to the columns of the display, when to select the next row and also when to delete an image. This should be done during a specific time interval.

In addition to testing the pixels, the peripheral hardware design connected to the controller is also considered to be tested and verified in the future. This can be verified through different measurements on the system and the validity of these results. A typical example of measuremnt would be to investigate the behaviour of the hardware components and see if it really works as intended.

Besides the previous mentioned future work that can be done, there are also more things that can be accomplished such as to simulate a more complex design in cadence using multiple iterations of the pixel cell. The controller functionality can also be further improved with other functions such as temperature sensors, detection of previous state etc.

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