850 nm hybrid vertical cavity laser integration for on-chip silicon photonics light sources

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Abstract: The realization of 850 nm hybrid III-V/dielectric VCSELs is reported in order to realize low power consumption integrated light sources for SiN waveguide circuits, which find applications both in short-reach optical communication and optical sensors.

OCIS codes: (130.0130) integrated optics; (140.7270) Vertical emitting lasers

1. Introduction

While silicon photonics is generally considered to be based on silicon-on-insulator (SOI) waveguide circuits, there is a growing interest in the use of SiN waveguide circuits at visible / near-infrared wavelengths (VIS/NIR), telecom/datacom wavelengths and mid-infrared wavelengths. These circuits can also be fabricated using the CMOS fabrication infrastructure and have a medium refractive index contrast, leading to relatively compact devices. In the near-infrared, the applications are mainly related to optical sensing and short-reach optical interconnects. These applications require the integration of near-infrared light sources on the SiN waveguide platform. For example, one can envision an optical sensor where a functionalized SiN ring resonator array is interrogated by a near-infrared laser source and silicon / GaAs photodetector array both integrated on the SiN waveguide circuits. In the context of short-reach optical communication one can envision a SiN optical interposer chip providing optical links between two neighbouring electronic ICs. Also in this case there is the need for the integration of large arrays of fast, low-power consumption near-infrared laser sources, while the optical detection can be realized inside the electronic ICs. Considering operation at 850 nm wavelength, GaAs VCSELs are nearly ideal sources, featuring high wall-plug efficiency and high bandwidth. In this paper we elaborate on a scalable method to integrate such laser sources on a SiN waveguide circuit.

2. Hybrid III-V/dielectric VCSEL structure

While one approach to integrate 850 nm VCSELs on SiN waveguide circuits is to flip-chip integrate finished VCSELs on diffractive grating couplers, such an approach is not scalable to large arrays, given the high alignment accuracy required in the placement and the complication of having to mount the VCSEL under an angle with respect to the surface normal. Therefore we adopted another approach: the heterogeneous integration through die-to-wafer bonding of III-V epitaxy comprising a half VCSEL structure, i.e. the *p*-type DBR, the multi-quantum well active region and an intra-cavity *n*-contact, on a silicon substrate comprising a dielectric DBR and a SiN waveguide layer, after which the VCSEL is processed lithographically aligned to the underlying SiN waveguide circuit, as shown in Fig. 1(a).

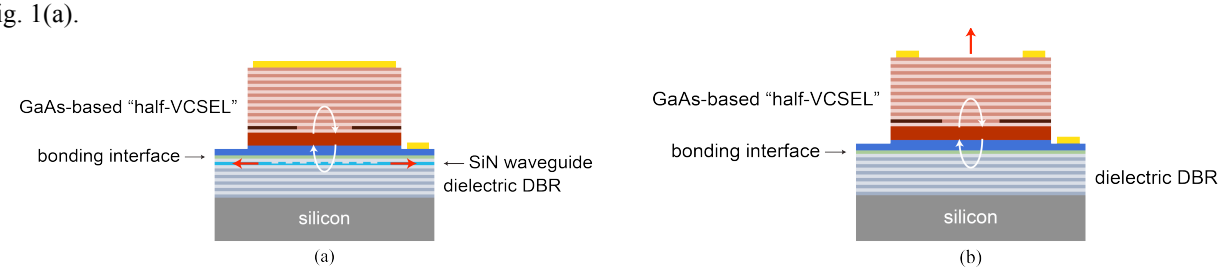

Fig. 1. (a) Hybrid III-V/dielectric 850 nm VCSEL with an intra-cavity grating for coupling to a SiN waveguide. (b) Surface emitting hybrid laser.

The SiN waveguide layer contains a weak grating structure that is designed to a) set the polarization of the VCSEL and b) to efficiently couple the optical power circulating in the VCSEL cavity to the SiN waveguide circuit. The SiN grating sets the polarization to transverse electric (electric field lines along the grating slits) by coupling a

substantially larger part of the transverse magnetic field out of the cavity, thereby resulting in a lower cavity loss for the TE mode. In order not to introduce high losses in the laser cavity, the fraction of TE optical power that is coupled out is kept low (~0.1%), but can be very efficiently coupled to the SiN waveguide circuit.

In order to evaluate the feasibility of such a hybrid III-V/dielectric VCSEL source, we have fabricated surface emitting hybrid laser structures depicted in Fig. 1(b). A detailed description of the design and fabrication is presented in [1]. In short, these structures consist of a 20 pair Ta_2O_5/SiO_2 DBR (with a calculated reflectance of above 99.99% assuming lossless materials) onto which the GaAs half-VCSEL structure is bonded. The half-VCSEL consists of an *n*-$Al_{0.12}Ga_{0.88}As$ intra-cavity contact layer, an active region with five 4 nm $In_{0.10}Ga_{0.90}As$ quantum wells (QWs) with photoluminescence (PL) peak measured at 840 nm, a *p*-$Al_{0.98}Ga_{0.02}As$ layer for the formation of an oxide aperture for transverse current and optical confinement, and a 23-pair *p*-$Al_{0.90}Ga_{0.10}As/Al_{0.12}Ga_{0.88}As$ DBR. The bonding interface is defined by a 40 nm DVS-BCB bonding layer and a thin SiO_2 layer deposited on the dielectric DBR. By modifying the interface thickness, the cavity resonance wavelength is altered. A cross-section of the device structure is shown in Fig. 2(a), showing the dielectric DBR, the bonding interface and the III-V half VCSEL with oxide aperture. Coplanar ground-signal-ground electrodes were defined for high-speed characterization as shown in Fig. 2(b).

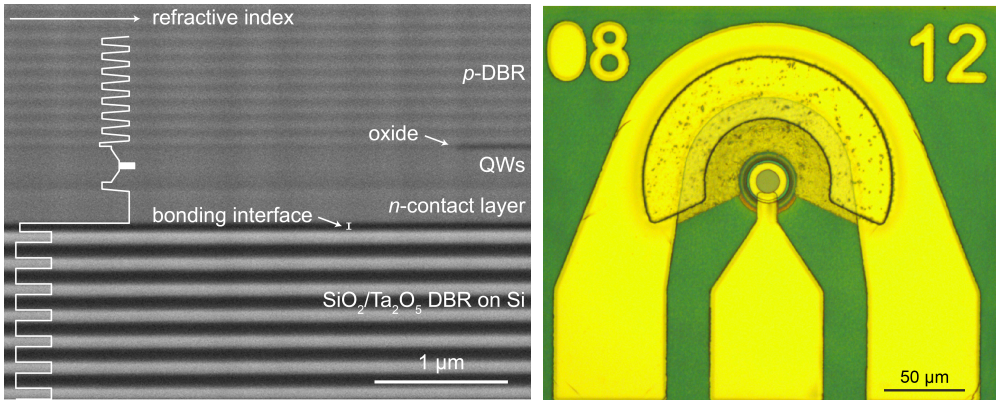

Fig. 2. (a) Cross-section through the hybrid III-V/dielectric 850 nm VCSEL structure. (b) Top-view of the finalized VCSELs.

3. Hybrid III-V/dielectric VCSEL device characterization

Four samples with an interface thickness of 35, 65, 125, and 180 nm (named A-D) and cavity resonance wavelengths of 843, 853, 861, and 867 nm were prepared, corresponding to a gain-to-resonance detuning of approximately +9, −1, −9, and −15 nm, respectively. The diameter of the oxide aperture is 10 µm. The output power and voltage versus current measured at ambient temperatures ranging from 15 to 100°C, in steps of 5°C, are shown in Fig. 3 [2].

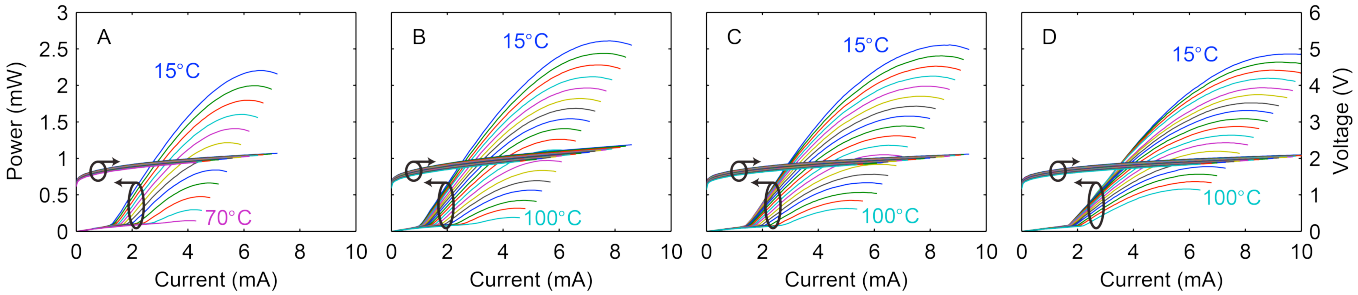

Fig. 3. Static characteristics of VCSELs A-D as a function of ambient temperature.

This analysis shows that by optimizing the interface layer thickness and hence the gain-to-resonance detuning, the structure can be optimized for either minimum threshold current at a specific ambient temperature or a small variation of threshold current over the temperature range. All VCSELs have similar slope efficiency (~0.5 W/A at

25°C). At high temperatures, the slope efficiency is reduced as a result of increased internal optical loss and reduced internal quantum efficiency. The thermal roll-over current is largely determined by the thermal impedance and the dependence of threshold current on temperature since the internal temperature increases with current due to heat dissipation. Therefore, while VCSEL B and C produce the highest output power at 25°C (2.3 mW), VCSEL D shows improved high temperature and high current performance since the gain peak aligns with the resonance wavelength at higher internal temperature. The maximum output power at 100°C is 0.6 mW.

The modulation response for VCSELs A–D at 25°C is shown in Fig. 4 [2]. Small signal bandwidths up to 10 GHz are observed. A device similar to VCSEL C but with a smaller oxide aperture diameter of 5 µm was chosen for back-to-back data transmission experiments. The small signal bandwidth for this device was 12.1 and 8.9 GHz at 25 and 85°C, respectively. The corresponding large signal modulation experiments at 25°C and 85°C are shown in Fig. 5 [2]. Error-free transmission at 10 and 25 Gbit/s operation is obtained at 25°C, while 10 Gbit/s error-free operation is obtained at 85°C.

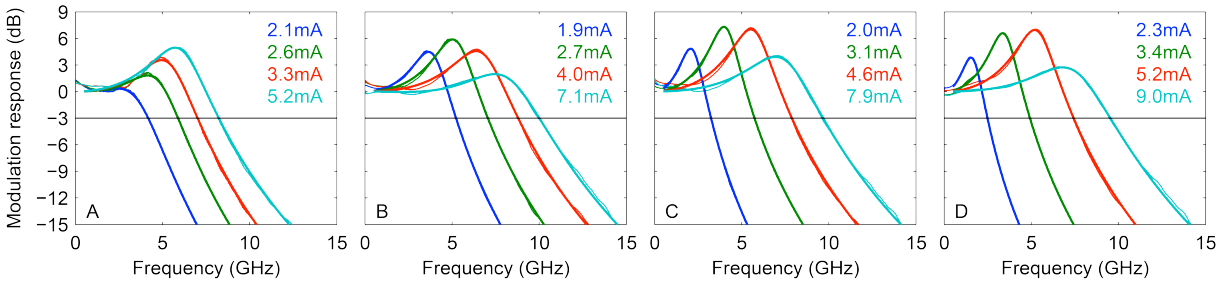

Fig. 4. Small-signal modulation response at 25°C for VCSELs A–D at indicated bias currents. The maximum 3 dB modulation bandwidth is reached at the highest bias currents indicated.

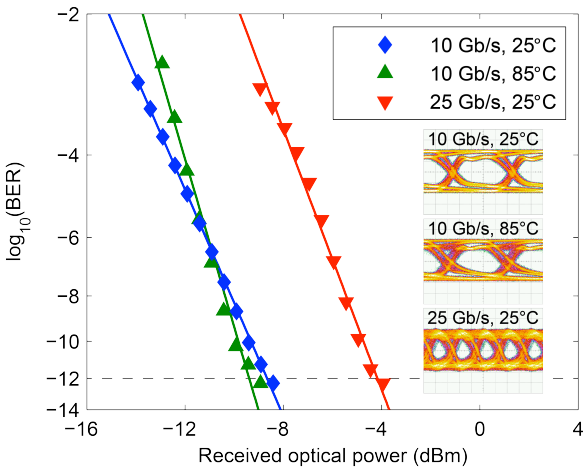

Fig. 5. Measured bit error ratio versus received optical power for a 5-µm oxide-aperture diameter VCSEL at data rates up to 25 Gb/s at 25°C and 10 Gb/s at 85°C. Insets: Corresponding optical eye diagrams (scales: 100 mV/div and 20 ps/div).

Acknowledgments

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