THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Cold-Electron Bolometer Fabricated with Direct Write Technology for Microwave Receiver Systems

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Department of Microtechnology and Nanoscience- MC2
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Cover: (Top) microscope image of a Log-Periodic Antenna and a CEB (inset)
(Bottom) microscope image of a Finline in a waveguide and a CEB (inset)

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Abstract

This thesis concerns the development of microwave detector technology for cosmology instruments and THz imaging, including fabrication of SIN tunnel junctions for thermometry and bolometric detectors, and also phase switch circuits as a part of integrated microwave receiver systems.

Cold-Electron Bolometers (CEB) based on Superconductor-Insulator-Normal metal (SIN) tunnel junctions have been developed for employment in sub-millimeter astronomical receivers. While used as direct detectors, their operation principle is based on hot-electron effect in nanoabsorbers and the dependence of SIN junction characteristics on temperature. In this thesis, the technology development for fabricating bolometric detectors based on these principles is presented, as well as CEB devices fabricated with the new technology and operating at 97 - 350 GHz.

The successful operation of CEB devices is reported here, including different advanced implementations of bolometers for effective detection of microwave electromagnetic signals. New fabrication technologies developed for manufacturing CEB, on-chip thermometers, THz detectors and Phase Switch devices are presented.

The necessity of this development work was determined by the demand of a robust and straightforward process for fabricating CEB devices with SIN tunnel junctions of large area, at high yield and good reproducibility. Advanced procedures developed for fabricating CEB devices include e.g. Direct-Write Trilayer Technology and Ti-based technology that enable fabricating devices of any geometry, with no limitations related to the layout. This is suitable for integrating the devices in planar antennas, such as log-periodic and double-dipole antennas or finline-shaped slotlines.

Properly operating CEB devices are demonstrated, characterized by measuring their DC characteristics and RF response at 280-315 mK. RF testing was performed using hot-cold method and using a black-body source heated by external current, with the estimated NEP down to about ~$3 \cdot 10^{-17}$ W/Hz$^{1/2}$ reported. Fabricating and testing these devices allows demonstrating the full functionality of the CEB detector fabricated with new technology and integrated in various planar circuits.

All devices presented here were fabricated by the author at Chalmers MC2.

Keywords: Cold-Electron Bolometer, thermometry, RF switch, microwave devices

List of Publications

Appended Papers

This Thesis is based on the work contained in the following papers.

I. **Direct-write trilayer technology for Al-Al_20_3-Cu SIN tunnel junction fabrication**
E. Otto, M. Tarasov, L. Kuzmin
*J. Vac. Sci. Technol. B **25** (4) Jul/Aug 2007 p.1156-1160*

II. **An array of 100 Al–Al_2O_3–Cu SIN tunnel junctions in direct-write trilayer technology**
E. Otto, M. Tarasov, G. Pettersson, D. Gustavsson and L. Kuzmin
Supercond. Sci. Technol. 20 (2007) 1155–1158

III. **Ti–TiO_2–Al normal metal–insulator–superconductor tunnel junctions fabricated in direct-write technology**
E. Otto, M. Tarasov and L. Kuzmin
*Supercond. Sci. Technol. **20** (2007) 865–869*

IV. **Optical response of Titanium-based Cold-Electron Bolometer**
E. Otto, M. Tarasov, P. Grimes et al
*Supercond. Sci. Technol. (SUST). – **26** (2013) 085020 July 2013*

V. **Cold-Electron Bolometer Integrated with a Unilateral Finline**
E. Otto, M. Tarasov, P. Grimes, L. Kuzmin, and G. Yassin
21st International Symposium on Space Terahertz Technology, Oxford, 2010

VI. **Experimental Investigation of a Superconducting Switch at Millimetre Wavelengths**
B. Tan, G. Yassin, E. Otto, and L. Kuzmin
IEEE Transactions on Terahertz Science and Technology, Vol. XX, no. XX, September 2015

VII. **Electrostatic effects in coupled quantum dot-point contact single electron transistor devices**
S. Pelling, E. Otto, S. Spasov et al
*Journal of Applied Physics, Vol. **112**, Issue 1, 2012*

Other Contributions

VIII. **A Class AB Monolithic CMOS RF Mixer for 2.4 GHz Applications,**
E. Otto, Y. Gusev, H. Olsson,
*Norchip Conference, November 2000, Åbo (Turku), Finland***.**

IX. **An Integrated Superconducting Phase Switch for Cosmology**
G. Yassin, L. Kuzmin, P. Grimes, M. Tarasov, E. Otto, and P. Mauskopf
Instruments Physica C 2007

X. **Investigation of planar switches for large format CMB polarization instruments.**
P. Grimes, G. Yassin, L. Kuzmin, P. Mauskopf, E. Otto, M. Jones, C. North.
Proc. SPIE, 6275: 25, 2006.

XI. **Superconducting Subterahertz Fast Nanoswitch**
L. Kuzmin, M. Tarasov, E. Otto, A. Kalabukhov, G. Yassin, P. Grimes, and P. Mauskopf
JETP Letters, 2007, Vol. 86, No. 4, pp. 275-7.

XII. **Finline-integrated cold electron bolometer**
E. Otto, M. Tarasov, P. Grimes, N. Kaurova, H. Kuusisto, L. Kuzmin , and G. Yassin
Proc. SPIE, June 2010.

XIII. **Cold-Electron Bolometer Array Integrated with a 350 GHz Cross-Slot Antenna**
M. Tarasov, L. Kuzmin, N. Kaurova, E. Otto, G. Yassin and P. de Bernardis
21st International Symposium on Space Terahertz Technology, March, 2010

XIV. **Fabrication and Characteristics of Mesh Band-Pass Filters**
M. Tarasov, V. Gromov, G. Bogomolov, E. Otto, L. Kuzmin
Journal: Instruments and Experimental Techniques, 2009, Vol. 52, No. 1, pp. 74–78, 2009.

XV. **Experimental Investigation of a 220 GHz Superconducting Switch**
B. Tan, G. Yassin, E. Otto, and L. Kuzmin
8th UK, Europe, China conference on Millimetre Waves and Terahertz Technologies at Cardiff. UCMMT-2015

XVI. **A Superconducting Millimetre Switch with Multiple Nano-Bridges**
B.-K. Tan, G. Yassin, L. Kuzmin, E. Otto, H. Merabet, and C. North
25th International Symposium on Space Terahertz Technology, Apr. 2014.

Abbreviations

AFM	Atomic Force Microscopy
BWO	Backward Wave Oscillator
CB	Coulomb Blockage
CBO	Coulomb Blockage Oscillation
CEB	Cold-Electron Bolometer
CMB	Cosmic Microwave Background
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapour Deposition
DOS	Density of States
EBL	Electron Beam Lithography
E-gun	Electron gun
HEB	Hot-Electron Bolometer
GaAs	Gallium Arsenide
IF	Intermediate Frequency
IMPATT	IMPact ionization Avalanche Transit-Time diode
IPA	Isopropanol
JFET	Junction gate Field-Effect Transistor
LOR	Lift-Off Resist
MOS	Metal-Oxide-Semiconductor
NEP	Noise Equivalent Power
NbN	Niobium Nitride
OMT	Orthomode Transducer
PC	Point Contact
PMMA	Polymethyl-Methacrylate
QD	Quantum Dot
RF	Radio Frequency
RMS	Root Mean Square
SD	Small Dot
SET	Single Electron Transistor
SiO	Silicon Monoxide
SiO_2	Silicon Dioxide
SIN	Superconductor Insulator Normal metal
SIS	Superconductor Insulator Superconductor
SOG	Spin-on Glass
SPM	Scanning Probe Microscopy
STM	Scanning Tunneling Microscopy
TES	Transition Edge Sensor
UHV	Ultra High Vacuum
2DEG	2-Dimentional Electron Gas

Contents

Thesis Outline and Scope

The development of Cold-Electron Bolometers based on SIN tunnel junctions and integrated in various planar circuits is presented, as well as the successful operation of CEB devices, with focus on the fabrication technology and different advanced implementations of CEB devices for efficient detection of electromagnetic signals at millimeter wavelengths. Also, other types of microwave detectors are presented, and also Phase Switch integrated circuits for millimeter-wave cosmology instruments.

In Chapter 1, an introduction to CMB cosmology is presented, including issues related to CMB polarization measurements. Existing instruments and different types of Millimeter-wave direct detectors are reviewed and discussed. The CEB detector is introduced, and different fabrication methods are discussed.

In Chapter 2, the CEB concept is examined, and factors determining CEB performance are discussed theoretically, including the performance of SIN tunnel junctions and noise issues in the CEB. Advantages and drawbacks of CEB in different configurations and with different readout schemes are discussed.

In Chapter 3, general fabrication principles and the fabrication procedures developed for manufacturing various detectors, on-chip thermometers and Phase Switch devices are described in detail, including Direct-Write Trilayer technology, Titanium-based technology, Advanced Shadow Evaporation technique, technology for fabrication of THz detectors and procedure for the fabrication of nanoswitches.

In Chapter 4, on-chip thermometers made of arrays of 100 SIN junctions as well as bolometric devices fabricated using Direct-Write Trilayer process are presented, and experimental results are discussed.

In Chapter 5, CEB integrated in a 97-GHz finline and the RF testing results are presented, including design considerations and RF characterization in a waveguide using a black-body radiation source. The devices were fabricated using the Trilayer technology.

In Chapter 6, CEB detectors fabricated with Ti-based process, integrated in planar log-periodic and double-dipole antennas, including experiments on RF testing, are presented and discussed.

In Chapter 7, CEB devices fabricated using Advanced Shadow Evaporation Technology, integrated in cross-slot antennas, are presented. The devices are arranged in parallel / series arrays; the concept of such CEB arrays is introduced and examined. The CEB performance was measured using hot-cold method and using a black-body source, and the experimental results are analyzed.

In Chapter 8, plasmonic detectors operating in THz frequency range are presented, including fabrication technology and experimental results; to be employed in radio astronomy or in other areas, such as security screening, environment monitoring or medical diagnostics. Among other types of sensors, these devices display very high sensitivity and reliable operation and are therefore widely used for these applications. The operation of such a device has been investigated; experimental data are presented; an electrostatic model of the system including an equivalent circuit introduced and examined, with a set of equivalent capacitances determined.

In the Chapter 9, planar NbN phase switch circuits integrated in a back-to-back finline for modulating the polarization of microwave signals are presented, including switching characteristics. The circuits considered here were designed as possible implementation of a planar on/off microwave switch, in order to replace mechanical switches for modulating microwave signals in waveguides. The switching devices comprise single or multiple niobium nitride (NbN) bridges, positioned across the slotline section of back-to-back unilateral finlines.

In Chapter 10, the material of the thesis is summarized and discussed, and conclusions regarding the achieved results are drawn. Also, possible ways of further development and potential improvements are discussed.

Chapter 1
Introduction

1.1. Introduction to CMB cosmology

Radio astronomy is one of the new research areas successfully explored in the last few decades. Very high sensitivities have been achieved using up-to-date detectors and advanced technologies. For example, Superconductor-Insulator-Superconductor (SIS) detectors were used in heterodyne receivers, which resulted in a breakthrough in that field and enabled advanced astronomical measurements using very sensitive detectors. These were implemented in the latest telescopes operating at frequencies 100 GHz to 1 THz, such as e.g. JCMT (James Clerk Maxwell Telescope) [1] and later also Atacama Large Millimeter / submillimeter Array (ALMA) [1, 2].

The performance of space instruments is determined by the sensitivity of detectors used, because radiation coming from the space is very weak. This thesis presents the technology development and bolometric devices fabricated using developed technologies. This includes fabrication technology for bolometric detectors and phase switch devices as a part of receiver systems.

The most important achievement in radio astronomy using modern instruments was the discovery of the Cosmic Microwave Background (CMB) and its anisotropy and polarization. CMB can be considered as the relic of the radiation emitted by the Big Bang, which is confirmation of the hypothesis of the Big Bang. After the Big Bang, an Inflation period started, which means a very rapid expansion of the space during approximately 10^{-35} s after the Big Bang. Then, the universe continued to expand and its temperature thereby decreased. 13.7 billion years ago, the recombination of the ionized matter began, and the first atoms were built. About 300 000 years after the

Big Bang, the Universe cooled down to ~3000 K and became transparent to electromagnetic radiation. The radiation interacted with particles, and information about this interaction can be obtained by detecting CMB radiation, which allows understanding of the history of the Universe. The CMB temperature measured today is about 2.73 K, with a maximum of the intensity around a frequency of 160.2 GHz.

The Big Bang and Inflation explain many phenomena and cosmological problems, e.g. the Hubble expansion, the distribution of matter across the space, and the temperature and density variations during the time of the evolution of the Universe. Also, the conclusions of Inflation theory and power spectrum models predicted by Inflation were confirmed by the CMB measurements of using numerous instruments (COBE [3], WMAP [4]).

The expansion of the early Universe is described by the Hubble law:

$$v = H_0 \cdot d$$

where v is the recession velocity and d is the distance of remote galaxies, and H_0 is Hubble constant which determines the rate of the expansion, $H_0 = 70.5 \pm 1.3$ $km \cdot s^{-1} \cdot Mpc^{-1}$, which corresponds to the age of the Universe of 13.72 ± 0.12 Gyr.

Due to gravitational attraction, the rate of the expansion of the Universe is determined by the density of matter in the Universe. CMB measurements have shown that radiation temperature is very uniform across the sky, and only small variations in temperature were observed, which reflect fluctuations in density in the early universe [5]. A number of experiments [6-13] were conducted in order to measure the distribution of CMB temperature, and the distribution mapped by satellite experiments (Fig. 1.1), such as WMAP satellite [12], and Planck [13].

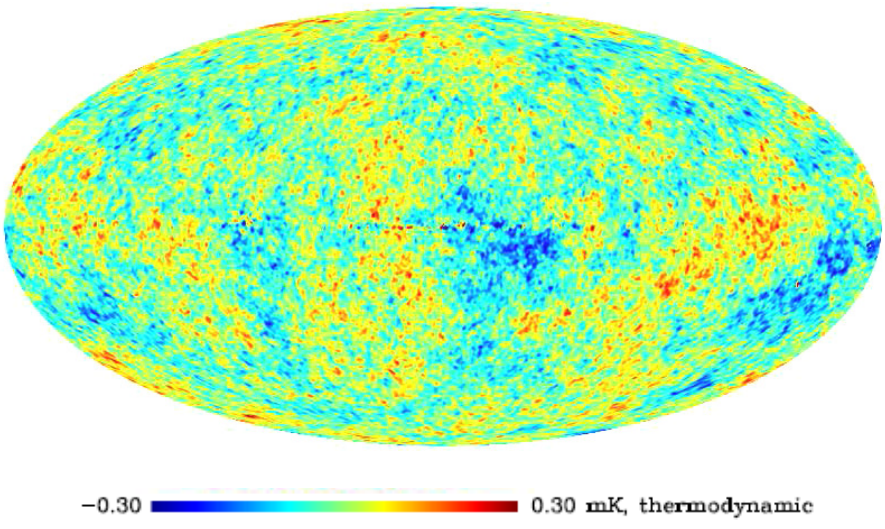


Figure 1.1: All-sky map of the CMB temperature [5, 12], projected onto a 2D image.

CMB angular power spectra measured by several instruments is shown in Fig. 1.2.

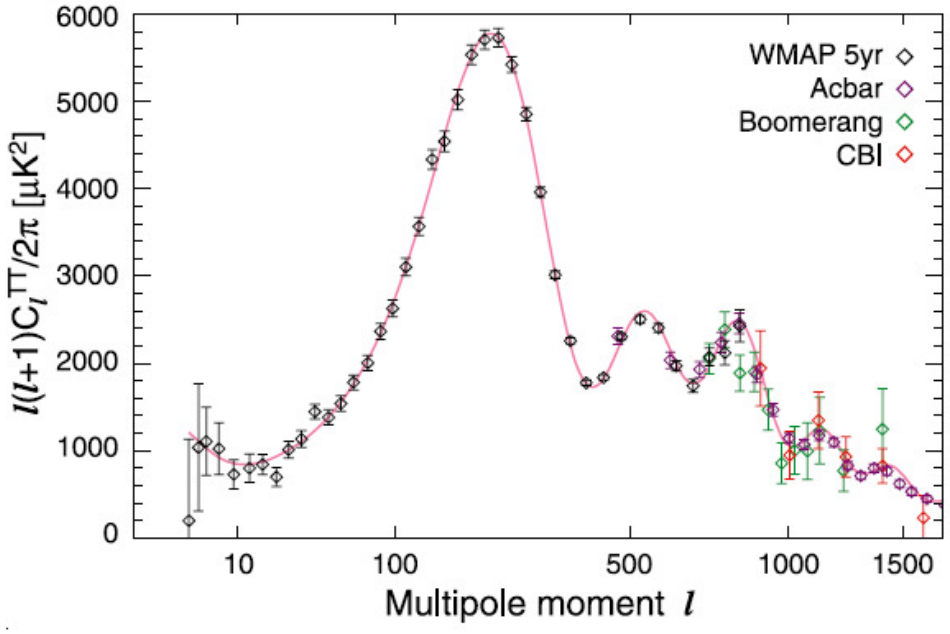


Figure 1.2. Angular power spectra of the CMB temperature [5, 6, 12]

1.2. CMB polarization

The cosmic microwave background (CMB) fluctuations are partly polarized, due to the Thomson scattering of photons by electrons near the last scattering surface [14, 5].

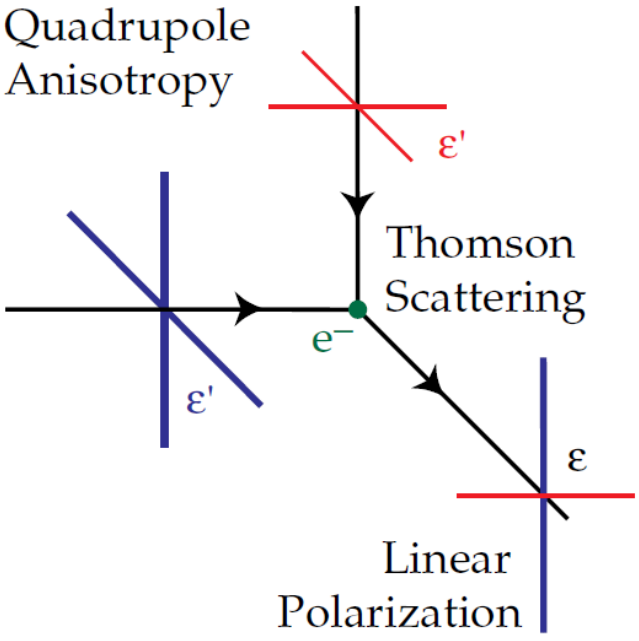


Figure 1.3. Thomson scattering of photons by electrons [5, 14].

After scattering, the incoming photons with different energies are partially polarized, as shown in Fig. 1.3. Perturbations after the Big Bang initiated density fluctuations, amplified later during Inflation. CMB radiation polarization due to scattering in anisotropic electromagnetic fields originates from temperature fluctuations produced by density fluctuations after the Big Bang and Inflation.

The Inflation hypothesis can be proven by measurements of the CMB polarization because CMB polarization contains Inflation indications. The CMB polarization measurement is the goal of most current CMB experiments, (e.g. BICEP [9], Planck [13], EBEX [15]).

The polarisation of the CMB can be decomposed into a curl component (B-mode) and a curl-free one (E-mode) [16]. The E-mode was detected [11, 17], whereas the B-mode signal is one order of magnitude weaker and is therefore still to be detected [16, 18]. Several ground based and balloon-borne instruments were designed to detect the B-mode signal. E.g., Clover included two telescopes operating at 97 / 150 and 225 GHz. BICEP (Background Imaging of Cosmic Extragalactic Polarization) is another ground based instrument dedicated to CMB polarization measurements. The BICEP instrument with an array of 98 detectors operates at 100 GHz and 150 GHz maps an area on the sky around the South Celestial Pole [9].

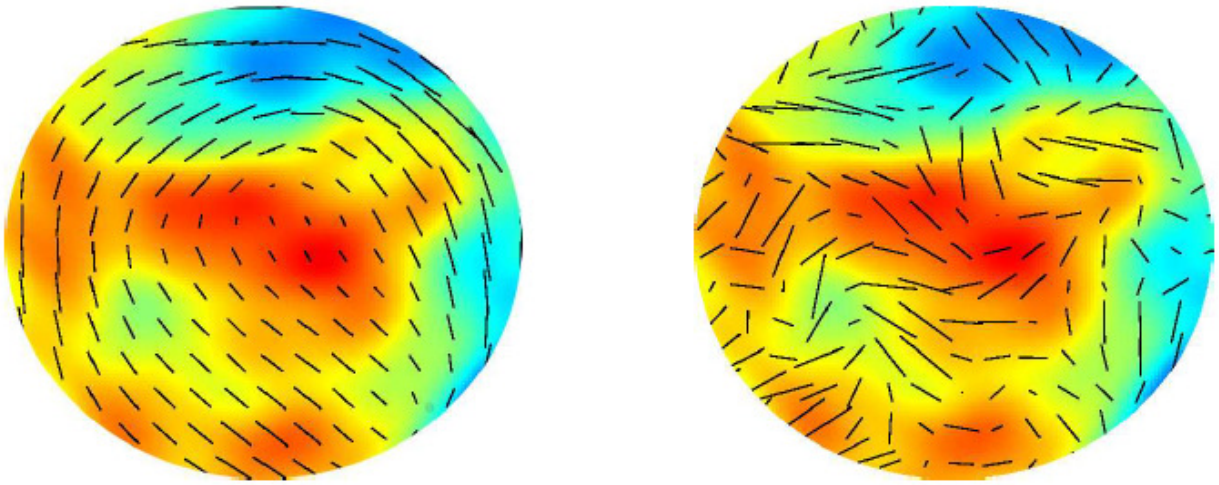


Figure 1.4: Simulation: (Left) E-mode fields; (Right) B-mode fields. Amplitude of polarization shown by color, directions indicated with lines [5].

The polarization amplitude and direction are correlated: the E-mode polarization is directed perpendicular or parallel to the amplitude gradient; the B-mode is directed at 45 degree to the gradient [5], see Fig. 1.4.

The theoretically predicted angular power spectra are shown in Fig. 1.5, including a forecasted B-mode secondary signal caused by the gravitational lensing of partially polarized CMB radiation travelling through large-scale structures. The predicted

foreground signals power spectra based on polarization observations and unpolarized emission models [17, 19, 20, 21] are plotted for the C$_\ell$over observation regions. The polarized foreground signals are plotted for 225 and 97 GHz and represent thermal emission from dust grains and synchrotron emission respectively [22].

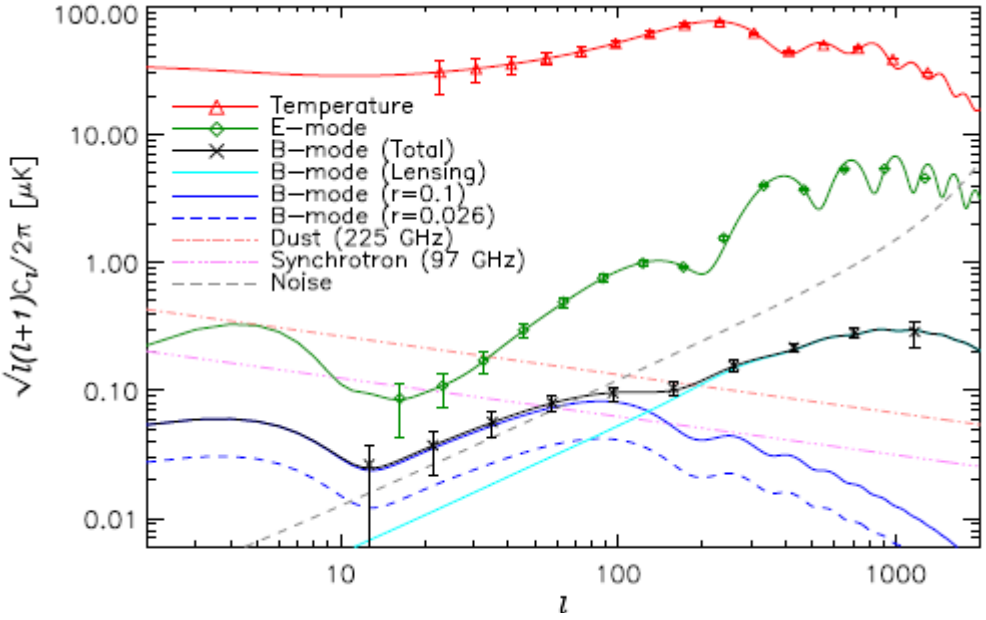


Figure 1.5: Theoretical angular power spectra for the temperature, E-mode and B-mode signals, and expected C$_\ell$over sensitivity [5, 21].

1.3. Instruments for polarization measurements

A number of cosmological instruments aiming to measure the CMB have been built. For example, the space-borne telescope WMAP (Wilkinson Microwave Anisotropy Probe) mapped the CMB in detail across the whole sky [4, 17]. DASI is a 13-element interferometer designed to measure temperature and polarization anisotropy of the CMB radiation over a large range of scales with high sensitivity [23, 24].

The B-mode signal is expected to be at least one order of magnitude weaker than the E component. Therefore, B-mode instruments must use extremely sensitive detectors for measurements. Hence, superconducting bolometric devices (or bolometers) are used by recently designed instruments.

C$_\ell$over was designed as a ground-based experiment for measuring the B-mode polarization of the CMB. Ground-based telescopes have certain advantages over space-borne and balloon instruments, due to easy access to the equipment. At the

same time, background noise is presented in the signal within the atmosphere; so to achieve reasonable sensitivity, a large number of sensitive detectors must be used.

Transition edge sensor (TES) detectors were designed to have sensitivity approaching the photon noise. Observations were planned in frequency bands around 97, 150 and 225 GHz, which corresponds to transmission windows at Llano de Chajnantor Observatory, while the CMB spectrum peaks at ~ 150 GHz.

Two receiver systems with the detectors were planned to be mounted at the focal planes of antennas with low cross-polarization. The schematic including the receiver and optical setup is shown in Fig. 1.6. Two TES detectors in each pixel are placed orthogonally to each other, which enables the detection of the electromagnetic waves with two polarizations.

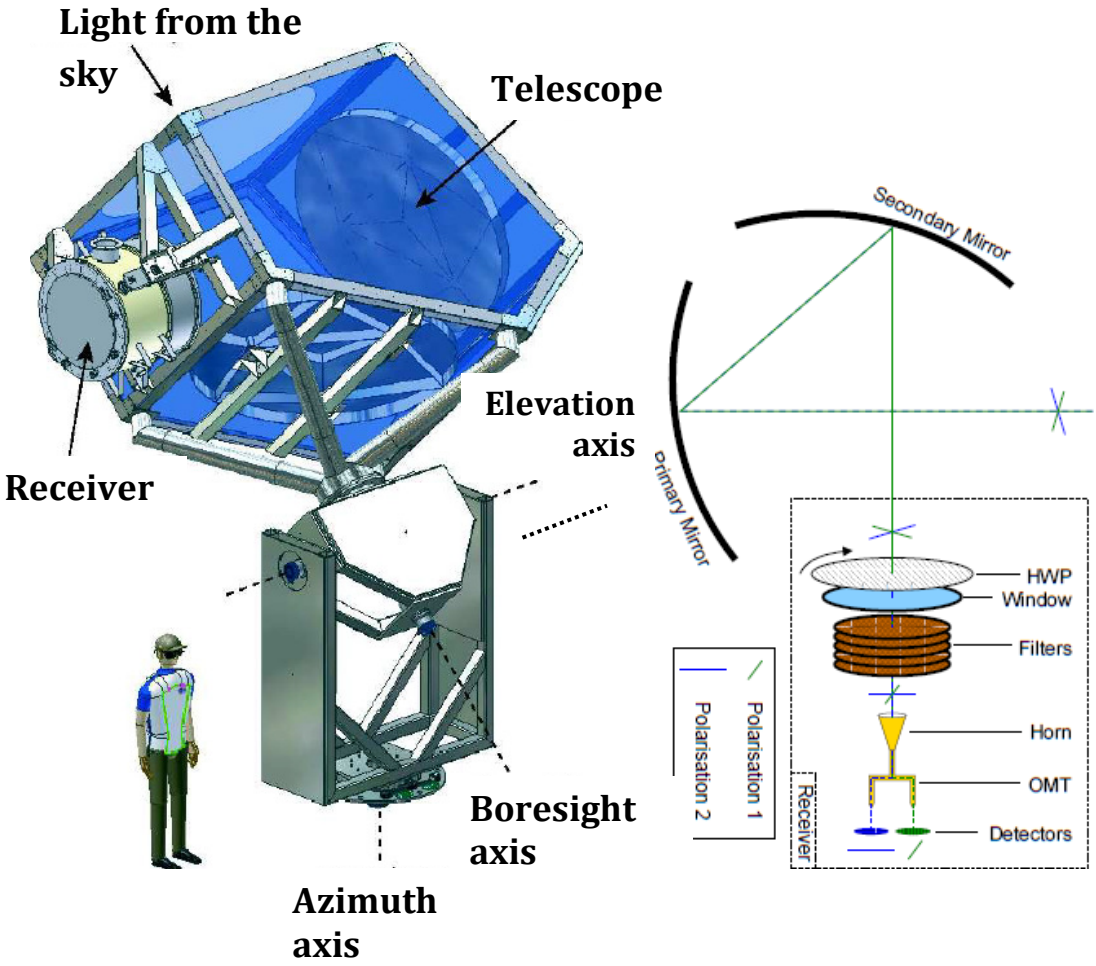


Figure 1.6. (Left) The design of a $C_\ell$over instrument, [5, 21]. (Right) Optical path of each pixel through the 97 GHz instrument [5]. Half-wave plate (HWP) rotates the polarizations of the incoming wave. After filtering, the signal is collected by the horn and decomposed by the OMT into two polarizations, detected then by TES detectors [5].

Each pixel includes a horn, an orthomode transducer (OMT) to decompose the incident electromagnetic wave into two orthogonal linear polarization components, and two TES detectors for the two orthogonal polarizations.

The instruments employ a compact range antenna (CRA) telescope [25], consisting of parabolic and hyperbolic concave mirrors. This approach ensures low level of cross-polarization, below -38 dB [5]. Focal plane layout and a horn are shown in Fig. 1.7.

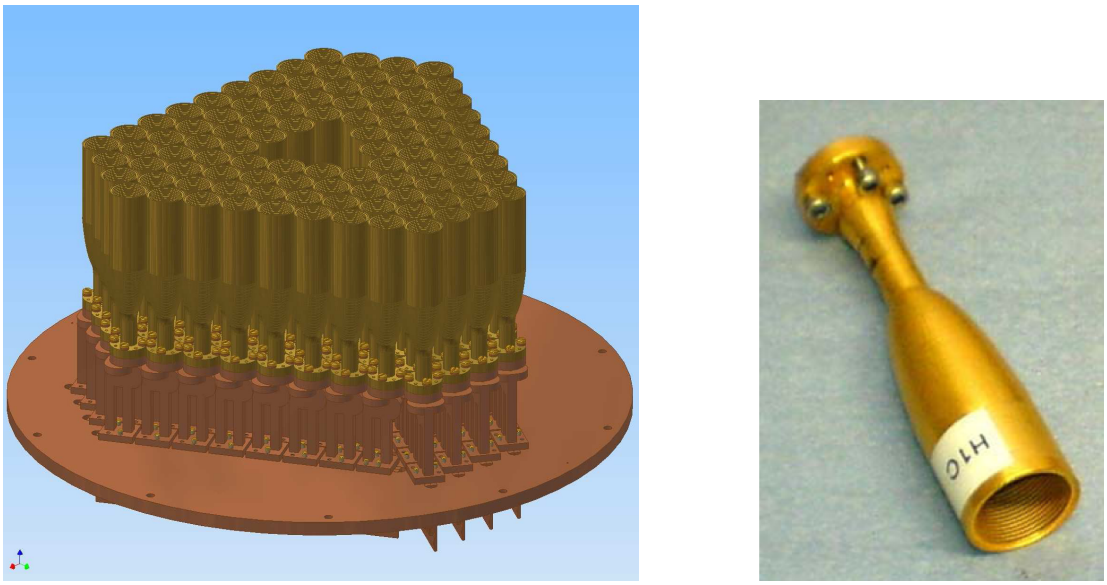


Figure 1.7. Layout of the detector block arrays within the focal plane array (left) and a 97 GHz prototype horn for Clover instruments (right), [5, 21]

Horns used for high-precision CMB-related measurements were designed to prevent the propagation of higher-order modes and for minimizing the cross-polarization. An attractive option is to use corrugated horns that have azimuthal corrugations on the inner surface creating isotropic boundary conditions at the surface for E- and H-fields [1]. This prevents the propagation of higher-order modes and allows primarily propagation of the modes contributing to polarized signals, which results in the narrow radiation pattern with minimum sidelobes and lowest cross-polarization [1, 5].

1.4. Millimeter-wave detectors

Two categories of Millimetre-wave detectors can be distinguished: direct detectors and coherent detectors. Direct detectors measure the power of the incoming radiation [26], which enables detection of very weak signals. In coherent detectors implemented in heterodyne receivers, the incoming RF signal is first downconverted to so-called Intermediate Frequency (IF), and then it is amplified and read out by a spectrometer. This preserves the phase information of the incoming signal and allows using low-frequency amplifiers and other RF components which is still challenging at

frequencies of hundreds of GHz. Thus, the sensitivity of the receiver is reduced compared to direct detection, since it is limited by the IF bandwidth.

Also, due to the uncertainty principle, obtaining phase information implies an uncertainty in amplitude in coherent detection, corresponding to detecting of one single photon.

In detectors of both types, superconducting tunnel junctions are often used, that are tunnel junctions between two superconducting electrodes with an oxide layer in between [26]. Depending on external conditions, such a 3-layer structure can be used either as a Josephson junction or SIS (superconductor-insulator-superconductor) tunnel junction. Unlike Josephson junctions with supercurrent, in SIS junctions the Josephson current is normally suppressed by magnetic field. This type of device is commonly employed as mixer for heterodyne detecting at frequencies of 1 THz and below [26, 27], while direct detectors of this type are mostly used as photon counters at frequencies above 10 THz.

At frequencies between ~1 and 10 THz, superconducting Hot-Electron Bolometers (HEB) are used as heterodyne receivers [26]. HEB mixers are crucial components in receiver systems for THz radio astronomy, which has revealed new potential for observations [28, 29, 30].

The intermediate frequency in such mixers can be as high as ~100 MHz due to the temperature relaxation time that was discovered to be as short as a few nanoseconds in thin Nb films [31]. Later, much shorter relaxation time values (~10 ps) were observed in thin NbN films [32], which enabled implementing superconducting bolometers as THz mixers with a gain-bandwidth in a GHz range [28, 33]. Even higher intermediate frequencies have been attained using other materials, such as e.g. MgB_2 that allow for IF values exceeding 10 GHz [34, 35].

In what follows next, direct detectors of different kinds will be considered, as opposed to the mixers for heterodyne receiver systems, mentioned above, among other types of detectors.

For sensitive detection of electromagnetic radiation at THz frequencies, plasmonic devices are extensively employed in radio astronomy, e.g. for investigation of molecular chemistry of the universe. They are also utilized in various other applications, such as security screening, environment monitoring and medical diagnostics [36]. These devices are based on excitations of the resonant plasma oscillations due to absorption of THz photons, followed by either rectification of the plasmons to DC voltage or charge excitation in nanoscale devices, which could be detected with a high spectral resolution.

Bolometers are implemented in millimetre and far-infrared instruments such as bolometric interferometers [24] and pseudo-correlation polarimeters [18]. Many discoveries were made by such instruments; e.g., a new class of dusty sub-millimetre luminous galaxies were discovered and effects of formed planets on protoplanetary discs observed by SCUBA [37].

Recently developed superconducting direct detectors made of superconducting thin films are e.g. Kinetic Inductance Detectors (KID) [38-40] and Transition Edge Sensors (TES) [22, 26].

The Kinetic Inductance Detectors (KID) are superconducting photon detectors that modulate the impedance of a superconductor by changing its kinetic inductance by incident electromagnetic signal, which modifies the density of Cooper pairs and quasi particles. Apart from geometrical inductance, superconductors display kinetic inductance due to the energy stored in the supercurrent, which is equivalent to an inductance. Incident photons change the impedance of a superconductor by modifying its kinetic inductance [41], because the kinetic inductance increases upon photon absorption due to increased density of quasi particles.

A change in the kinetic inductance can be measured using a thin film resonant circuit, from which the incoming power can be estimated. Receiver systems based on KID detectors include microwave resonant circuits. Each resonator with an antenna or absorber is capacitively coupled to a coplanar waveguide (CPW, Fig. 1.8). Several resonators with different resonance frequencies can be coupled to the same line; so, the frequency domain multiplexing at GHz frequencies is implemented, which enables simultaneous reading out several detectors.

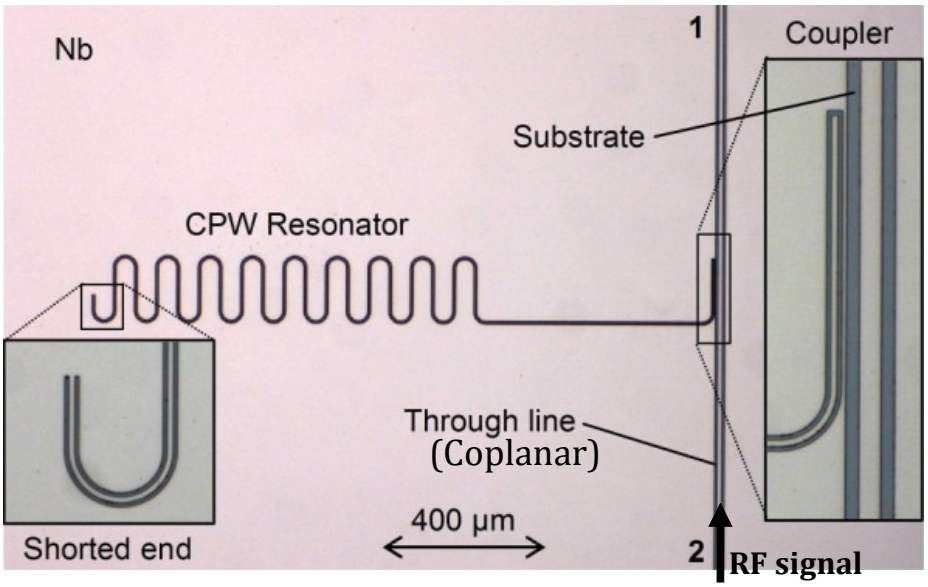


Figure 1.8. KID microwave circuit: CPW resonator coupled to through line [39, 40, 41].

Let us consider a superconducting film that absorbs an incident signal. At temperatures far below the transition, most of the electrons in a superconductor are condensed into Cooper pairs with density n_c, far above the density of the quasiparticles n_{qp} [41]. An incident electromagnetic wave with a frequency of $f > 2\Delta/h$ breaks Cooper pairs, resulting in increasing number of quasi-particles (with Δ being the superconducting gap, h Planck's constant):

$$n_{qp}^{excess} = \frac{\eta P \tau_{qp}}{\Delta}$$

where P is the incident power, τ_{qp} the quasi-particle lifetime and η the efficiency of energy transfer [41]. The sensitivity of such a detector can be expressed by the NEP [39, 41]:

$$NEP = \frac{2\Delta}{\eta}\sqrt{n_{qp} V / \tau_{qp}}$$

where V is the volume of the detector.

An equivalent circuit of the KID resonator is shown in Fig. 1.9. By changing the complex impedance of the resonance circuit, the resonance frequency can be changed. The measured transmission of such a resonator (Fig. 1.9, right) displays a minimum at resonance frequency that moves towards lower frequencies upon absorption of the incoming power [41].

KIDs arrays have not been implemented in real instruments so far but extensive research is currently carried out [39, 40].

The Transition-Edge Sensor (TES) comprises a superconducting film deposited on a thin membrane [42, 43]. Detection of incoming signals is realized by holding the superconductor at the transition between the superconducting and normal states [5]. The incoming power heats the device, causing a strong increase in the device resistance as it makes the transition from the superconducting to the normal states [5]. This sharp increase in the resistance leads to a flux change, which is measured by a SQUID, see a generic TES circuit schematic shown in Fig. 1.10.

In the TES circuit topology shown in Fig. 1.10, biasing is implemented using a voltage source V_{bias} and a load resistor R_{bias} [5]. The SQUID readout system is employed by coupling an inductance L to a SQUID flux meter that effectively measures the TES current by measuring the input flux to the SQUID.

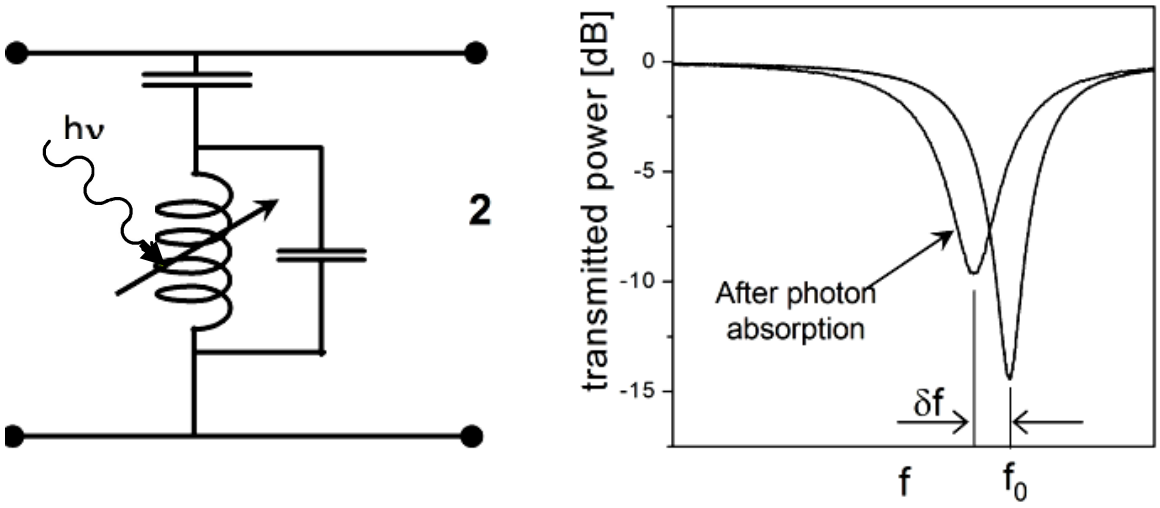


Figure 1.9. (Left) KID equivalent circuit [39, 40, 41]. (Right) Transmission of a KID resonator, $\delta f \cdot h$ = incident photon energy [39, 40, 41].

Using the thermal conductivity G, the Noise Equivalent Power (NEP) of TES detectors derived from phonon fluctuations can be estimated [43]:

$$NEP = \sqrt{4k_B T^2 G}$$

where k_B is the Boltzmann constant and T is the temperature of the detector. The reported values for NEP of TES detectors vary between ~10^{-18} and ~10^{-16} W/ $Hz^{1/2}$ in different systems.

TES bolometers are used in CMB-related projects such as the ground-based telescope BICEP, operating at 100 and 150 GHz, and EBEX (E- and B- Experiment) that is a balloon-borne instrument designed to measure the intensity and polarization of the CMB radiation [15]. EBEX consists of a telescope operating at frequencies of 150, 250, 350, and 450 GHz, with NEP reported around 1-2·10^{-17} W/ $Hz^{1/2}$ [15].

Another example of projects employing TES detectors was Cℓover relying on TES-microstrip integrated circuits with high sensitivity and noise performance. The TES system design proposed for Cℓover [21] operates as follows (see Fig. 1.11). The RF power is delivered to the bolometer through a microstrip terminated by a resistor (absorber). The power received by the TES is then dissipated in the terminating resistor which heats the TES absorber.

The microstrip-coupled TES architecture allows for efficient coupling to the waveguides and provides flexibility by separating the bolometer from the microstrip-

waveguide interface [22]. Thus, similar TES detectors can be used with different RF system topologies [44].

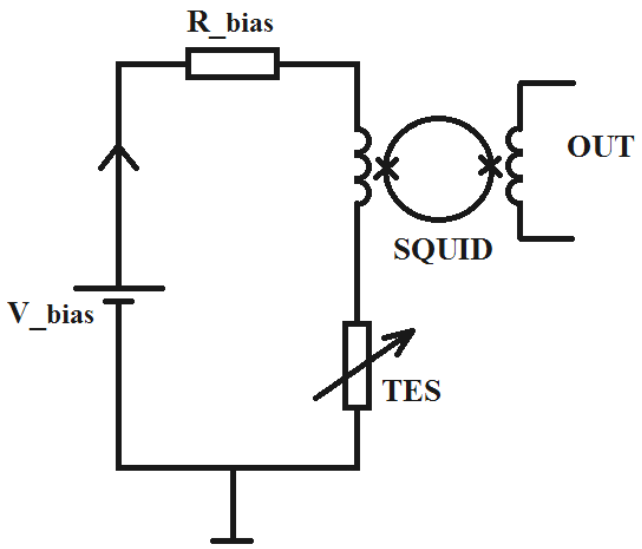


Figure 1.10. TES equivalent circuit schematic with SQUID readout [5]

An example prototype 97-GHz C$_\ell$over detector chip is shown in Fig. 1.11. The chips were fabricated using deep reactive ion etching (DRIE) for patterning the chip outline and the silicon nitride membrane. The processing was performed by the Detector Physics Group at the Cavendish Laboratory in Cambridge [45].

The finline transition is implemented in 97-GHz TES detectors to couple the power from the waveguide using a finline taper (Fig. 1.12) made of superconducting Nb film with an insulating SiO_2 layer [5, 22].

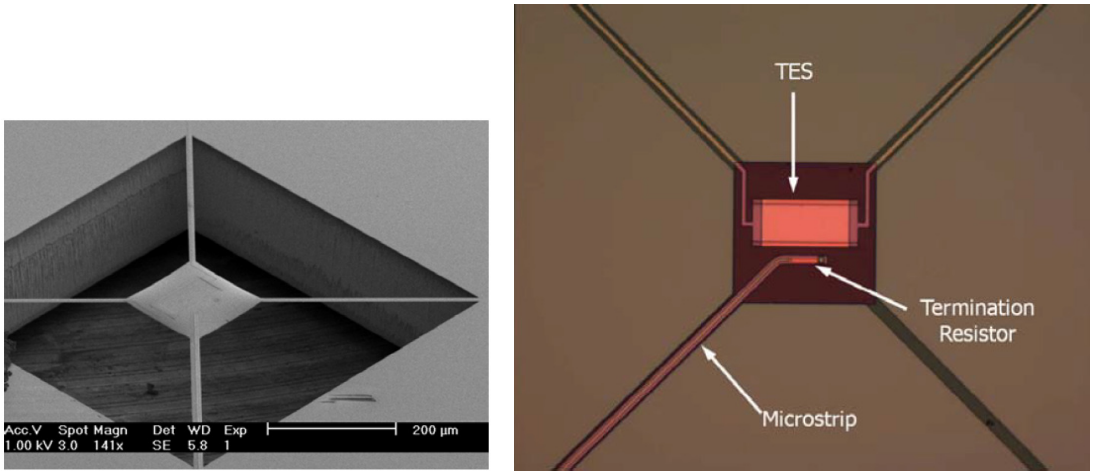


Figure 1.11. C$_\ell$over prototype bolometer on a silicon nitride membrane: TES and microstrip leading to termination resistor [22]; a scanning electron microscope image (Left) and an optical image (Right). Devices were fabricated at the Detector Physics Group (Cambridge).

For Clover, the required NEP level was 5 to $9 \cdot 10^{-17}$ W/ $Hz^{1/2}$ for 3 different channels at frequencies of 97 to 225 GHz [5]. The reported measured values for TES detectors are $1.7 \cdot - 3 \cdot 10^{-17}$ W/ $Hz^{1/2}$ [22, 44]. TES detectors employed in other projects, such as e.g. BICEP and EBEX, have the NEP values of same order of magnitude, $\sim 10^{-17}$ $W/Hz^{1/2}$ [5, 15].

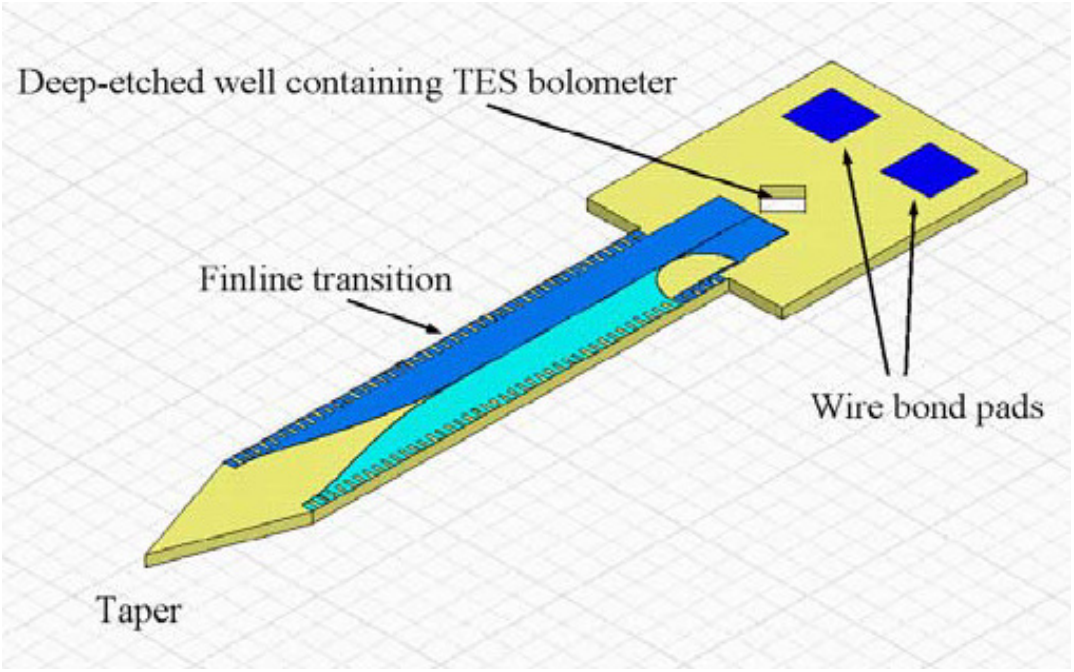


Figure 1.12. Layout of prototype 97-GHz $C_t$over detector chip [22], designed by the Detector group at Oxford University

1.5. Cold-Electron Bolometer

The main drawback of TES is its very limited saturation power. Due to the stochastic nature of the signals coming from space, TES bolometers saturate when the incident signal is strong enough to turn the device into normal. DC bias heating is applied to enable normal operation of TES, which leads to excess noise of the TES-based receivers. Besides, low-Ohmic TES detectors are read out using SQUID amplifiers, which are susceptible to the magnetic field [5]

In order to overcome the difficulties related to using TES detectors, a novel concept of the Cold-Electron Bolometer (CEB) has been introduced by L. Kuzmin in 1998 [46-52]. Cold Electron Bolometer with SIN tunnel junctions is a millimeter-wave detector which employs a strip of a normal metal that changes in temperature as it absorbs the incoming radiation [53-55].

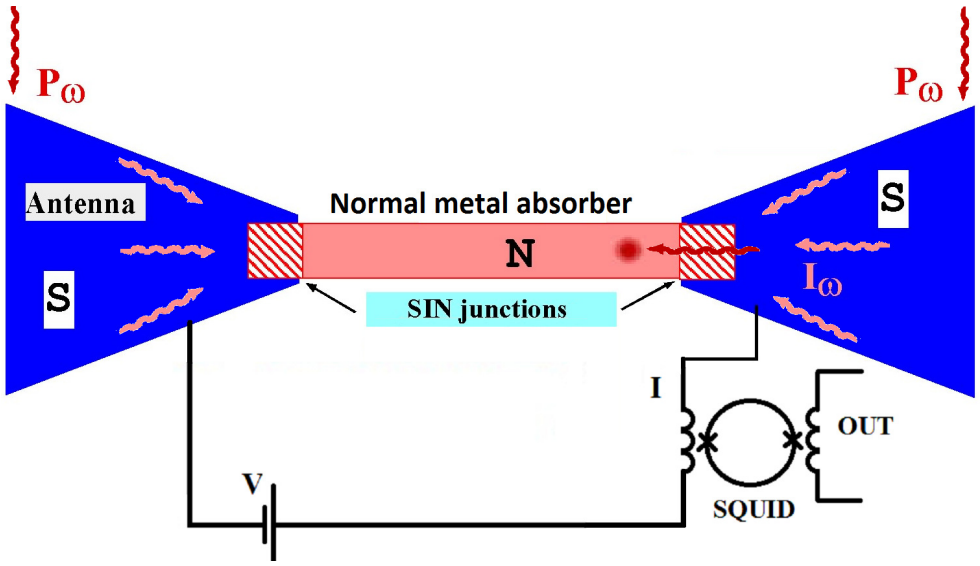


Figure 1.13. Cold-Electron Bolometer (CEB) with SIN tunnel junctions [56]. Incident power is supplied to the sensor through capacitances of tunnel junctions and dissipated in the absorber. The photon energy is absorbed by the electrons in the normal metal; thus, electrons in the absorber are heated; this increase in temperature can be measured by the SIN junctions.

The CEB devices presented in this thesis consist of a normal metal absorber coupled to superconducting electrodes via SIN tunnel junctions at each end of the absorber (Fig. 1.13). RF power from the antenna is capacitively coupled through the SIN tunnel junctions into the absorber. Incoming photons are absorbed by the normal metal causing hot electrons to be excited to a higher energy level (4 meV for 1 THz signal). The electrons are then relaxed due to electron-electron interactions, and their energy is distributed between hot electrons at quantization level k_BT, with the electron temperature over that of the phonons, see Fig. 1.14. The resulting change in the absorber electron temperature yields a substantial increase in the tunnelling current through the SIN junctions, due to exponential dependence of this current on the normal absorber temperature [57, 58]. The tunnelling current is amplified and measured, which allows measuring the temperature of the absorber and thus the incoming RF power [54-59]. Thereby, SIN junctions are employed in this topology as CEB readout, as the change in the absorber electron temperature is measured with SIN junctions [58-61].

The key features of this type of detectors are: large dynamic range of the CEB that prevents the system from saturation when the incoming RF power is relatively high; hence the ability to operate in a wide range of background load; easy integration in arrays on planar substrates; and the possibility of polarization measurements [56, 62]. Another advantage is a very simple and cheap readout systems used for CEB detectors.

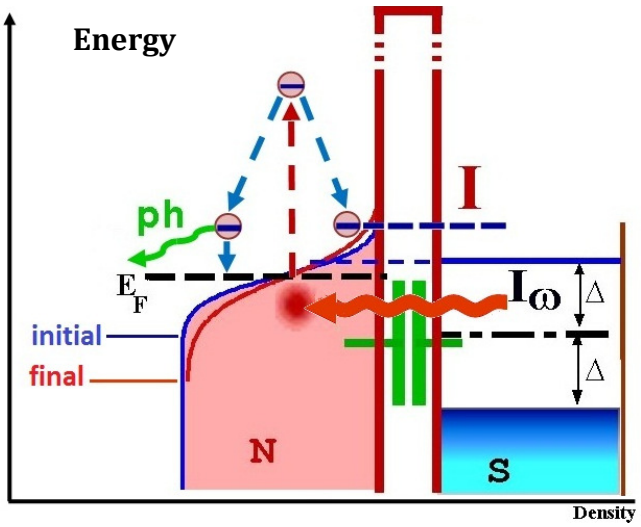


Figure 1.14. Energy diagram for SIN tunnel junctions in CEB [56]. As RF power is coupled to the absorber, the absorbed power excites electrons in the absorber; the electrons are then relaxed due to electron-electron interactions and their energy is distributed between hot electrons at quantization level k_BT for normal metal, thus increasing the electron temperature.

Since the electrons with the highest energy tunnel most rapidly through the oxide barrier of SIN junctions, the temperature of the absorber gets reduced. This phenomenon is referred to as electron cooling. The electron cooling by SIN tunnel junctions was reported in 1994 by Nahum et al., [63]. Later, effective cooling of normal-metal absorbers from 300 to 100 mK was successfully realized by several groups [64-66]. Electron cooling provides strong negative electrothermal feedback for the signal [52]. Unlike TES [58], the heating is replaced by electron cooling of the absorber using SIN tunnel junctions, down to electron temperatures below the phonon temperature [56], [66]. This electro-thermal feedback makes the saturation power of a CEB well above that of TES and other types of millimetre-wave detectors. In addition, the noise of a device is reduced when decreasing its temperature.

The development of sensors based on SIN tunnel junctions started in the 1970s by Bakker et al [67]. Methods of measuring the temperature with SIN junctions were then developed and experimentally verified by Pekkola [59] and Agulo [68], where SIN tunnel junctions and arrays were used for temperature sensing, which is also a part of CEB operation. Later, this approach was further developed by the author of this thesis, and the experimental results were published by Otto et al [Papers I-III] in 2007. In Paper II, the total temperature sensitivity of up to 100 SIN junctions was measured, and the approach was shown to be a feasible method of measuring the normal absorber temperature and, potentially, could be implemented for measuring the incoming RF power, upon further technology development and the design modifications.

The CEB can be combined with both JFET [69] and with SQUID readout [70-72]. For ground-based and balloon-borne instruments, the JFET readout can be employed, with NEP levels down to ~ $5 \cdot 10^{-18}$ W/Hz$^{1/2}$ [70]. For space-borne telescopes, sensitivity better than NEP ≈ 10^{-18} W/Hz$^{1/2}$ could be achieved with SQUID readouts [71]. Our goal is to achieve NEP approaching the level of the photon noise of the CMB radiation at given background power.

For the production of CEB devices, different fabrication methods can be used. For a long time now, Cold-Electron Bolometers with SIN tunnel junctions were manufactured using shadow evaporation technique based on one-cycle deposition of both superconducting electrode and normal metal absorber [54, 68, 73]. Another approach is a Direct-Write Trilayer technology proposed by L. Kuzmin for manufacturing Al-based SIN tunnel junctions and developed by Otto [Paper I]. Tunnel junctions presented there operate at ~300 mK, that is the temperature at which the bolometer operation is most efficient in terms of sensitivity. This technology allows manufacturing SIN tunnel junctions both in laboratory environment for the research on CEB applications and in the future in industry for mass production of millimetre-wave detectors. Devices fabricated using this Direct-Write technology are presented in this thesis. Also, advanced techniques for fabricating Cold-Electron Bolometers are described, based on depositing the normal absorber and oxidizing it prior to the superconducting electrodes. Different fabrication methods will be described in detail in Chapter 3.

The main focus of this thesis is antenna coupled CEB detectors deposited on planar substrates and coupled to the free space either by lenses or horns, directly or through waveguides. The RF power can coupled to the CEB using a unilateral finline, either through a waveguide or directly using quasi-optical coupling, by focusing the RF signal onto the chip surface. This approach is also applied for CEB devices integrated in other types of planar antennas, designed for optical coupling.

Chapter 2
Cold-Electron Bolometer

In this chapter, the CEB detector is examined, and factors that are crucial for the CEB performance are discussed theoretically, including general theory and performance of SIN (Superconductor-Insulator-Normal metal) tunnel junctions and CEB noise issues. Also, the CEB detector performance is analyzed, including advantages and drawbacks of CEB fabricated implemented in different configurations.

2.1. SIN tunnel junction theory

In a normal metal CEB bolometer, a normal metal strip, thermally isolated from the environment, is heated by incoming radiation. This change in temperature is then measured with SIN junctions [58-59]. CEB devices based on SIN tunnel junctions are studied in this thesis; therefore, properties of tunnel junctions are examined, with focus on SIN junctions that are used with CEB devices and their characteristics.
A tunnel junction is essentially a structure made of two metal layers separated by a 10-20 Å thick insulating layer. For a particle with a kinetic energy below the potential energy height of the insulating barrier, there is a finite probability to be found on the other side of the barrier. This is described by the Schrödinger equation [58, 75], while the tunneling probability depends exponentially on the thickness of the barrier thickness for a given energy across the barrier. Thus, tunnelling in a junction becomes significant if the insulating barrier is thin [58, 74]. The total tunnelling current through the junction is given by integrating single tunnelling currents of particles within the energy band of interest. Tunneling current through an SIN junction depends on the applied voltage [76], and the current-voltage characteristic of the junction is expressed as [58, 76-77]:

$$I_{SIN} = \frac{1}{eR_N}\int_{-\infty}^{\infty}\frac{E}{\sqrt{(E^2-\Delta^2)}}[f(E-eV)-f(E)]dE \qquad (2.1)$$

where R_N is the asymptotic or normal resistance of the SIN junction, Δ is the superconducting gap, $f(E)$ the Fermi-Dirac distribution function, and E the energy of the quasi-particles [77].

The distribution functions of the normal metal strip and the superconductor in an equilibrium are given by [77]

$$f_{N,S}(E) = \frac{1}{e^{\frac{E}{K_B T_{N,S}}}+1} \qquad (2.2)$$

Theoretical IV curve at the temperature of 0 K is shown in Fig. 2.1 for voltage values close the superconductive gap Δ. At voltages below the gap there is no significant current flow. When the applied voltage V approaches Δ, the energy levels in the normal metal are moved up by this value, and electrons in the normal metal can tunnel to empty states above the gap in the superconductor (Fig. 2.2). Therefore, the tunneling current increases rapidly at voltage values above Δ.

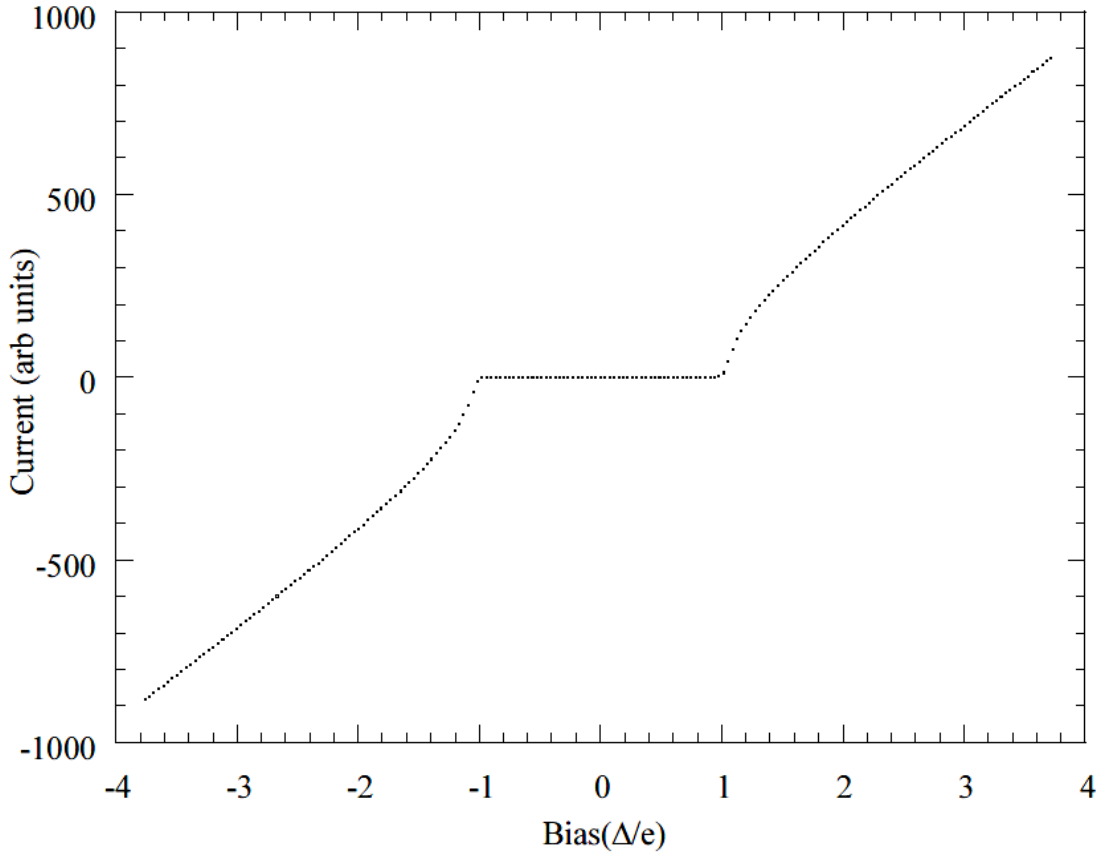


Figure 2.1. Current-voltage characteristic of an SIN tunnel junction [58].

For voltages above Δ, the density of states approaches that in the normal state, and, according to Eq. 2.1 the IV curve can be approximated by a linear asymptote, defined by the normal resistance R_N:

$$I_{SIN}(eV >> \Delta) \approx \frac{V}{R_N} \tag{2.3}$$

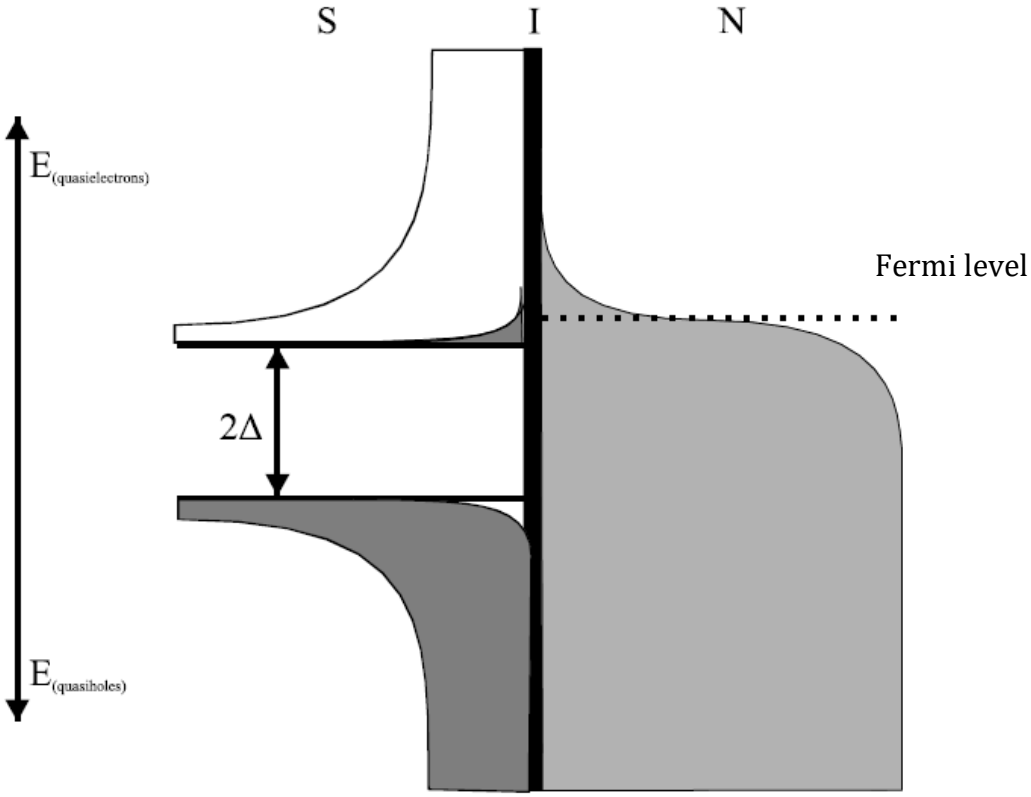


Figure 2.2. Energy diagram of an SIN junction showing the density of states distribution [58].

At bias voltages far above Δ, the current-voltage characteristics do not depend substantially on the temperature as it approaches the linear asymptote. For voltages below Δ, the IV curves vary strongly with the temperature, according to the Eq. 2.1. The tunneling current versus normal metal temperature is shown in Fig. 2.3. The current depends mainly on the temperature of the normal metal, because the temperature dependence is different for the number of electrons in the normal metal that are able to tunnel and the quasiparticle population in the superconductor [78].

Let us consider a CEB device with a normal metal absorber, irradiated by an RF signal δP. The temperature of the metal absorber is then determined by the heat balance between the electron and the phonon subsystems. The heat balance equation for a CEB can therefore be written as [71]:

$$P_C(V, T_e, T_{ph}) + \Sigma\Lambda(T_e^5 - T_{ph}^5) + C_\Lambda \frac{dT}{dt} = P_0 + \delta P(t) \tag{2.4}$$

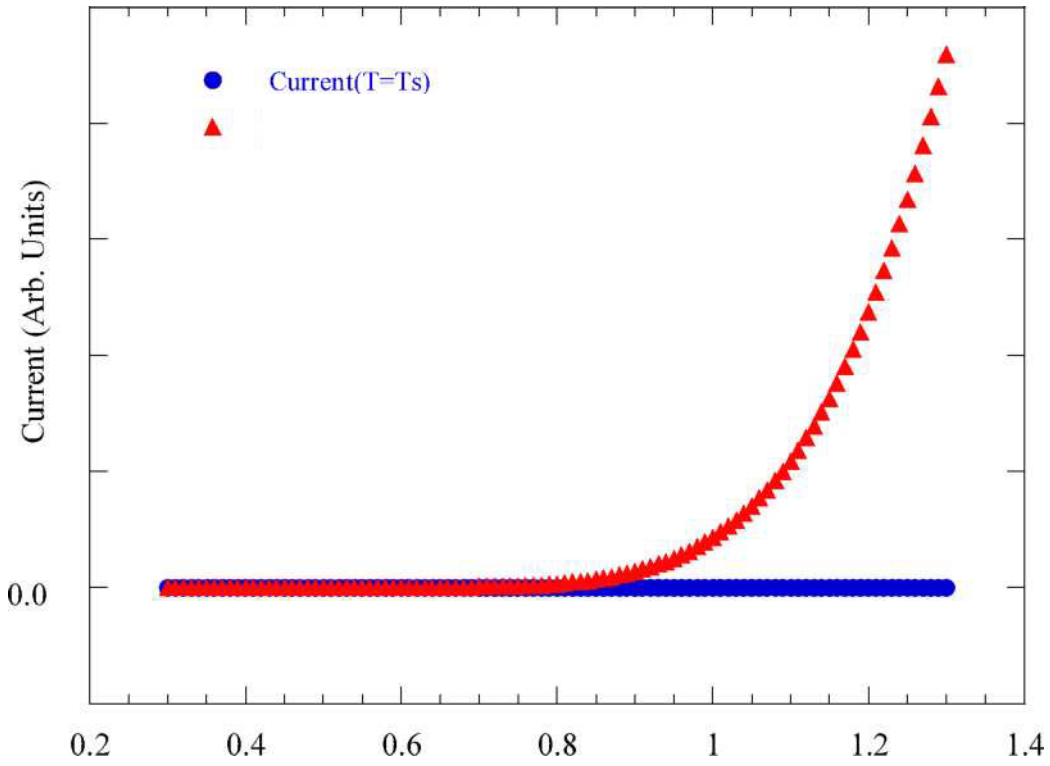


Figure 2.3 Current versus temperature in an SIN junction at fixed voltage around Δ [48]

where Σ is a material constant, Λ the volume of the absorber, T_e and T_{ph} are electron and phonon temperatures of the absorber, P_C is the cooling power of the SIN tunnel junction, and C_Λ is the specific heat capacity of the normal metal. The right-hand part of the equation represents the incident RF background power P_0 and the time-dependent $\delta P(t)$ is the incoming RF power to be detected.

Power flowing into and out of the CEB may be divided into two parts: a time independent term,

$$\Sigma\Lambda(T_{e0}^5 - T_{ph}^5) + P_C(V,T_{e0},T_{ph}) = P_0, \tag{2.5}$$

where T_{e0} is the electron temperature in the presence of the power load P_0, and a time dependent term,

$$(\partial P_C/\partial T + 5\Sigma\Lambda T_e^4 + i\omega C_\Lambda)\,\delta T = \delta P, \tag{2.6}$$

which is obtained by differentiating the Eq. 2.4 and considering a small change in temperature δT and in power δP, respectively, assuming that the incident signal is an electromagnetic wave at an angular frequency of ω.

The term $G_{SIN} = \partial P_C/\partial T$ is the effective cooling thermal conductance of the SIN junction that gives rise to the negative electrothermal feedback (ETF). It reduces the temperature response δT because the cooling power P_C compensates for the change

of signal power in the bolometer. The next term is the electron-phonon thermal conductance of the absorber:

$$G_{e\text{-}ph} = 5\Sigma\Lambda T_e^{4} \tag{2.7}$$

that represents the heat flow between electron and phonon sub-systems that can be expressed as

$$P_{e\text{-}ph} = \Sigma\Lambda(T_e^{5} - T_{ph}^{5}), \tag{2.8}$$

where Λ is the absorber volume and Σ is a constant for a given material.
From Eq. (2.6), an effective complex thermal conductance that determines the temperature response of the CEB to the incident RF power, could be obtained [71]:

$$G_{eff} = G_{SIN} + G_{e\text{-}ph} + i\omega C_{\Lambda} \tag{2.9}$$

The thermal conductance of the CEB is therefore increased by the effect of electron cooling, effectively producing negative Electro-Thermal Feedback.

The value of the thermal conductance is crucial for the noise performance of a CEB device because at equilibrium the phonon noise is expressed by $4k_BGT^2$, where G is the thermal conductance [79]. Lower heat conductance results in higher sensitivity since phonon noise increases linearly with thermal conductance. Due to dependence of electron-phonon thermal conductance on temperature, the term representing thermal conductance due to electron-phonon interaction G_{e_ph} is a critical parameter for estimating the optical performance of CEB, using the DC voltage to temperature response at a fixed current.

2.2. Noise performance of the CEB device

The sensitivity of a CEB device is expressed by the noise equivalent power (NEP). The NEP is defined as the low frequency spectral density of RF-power fluctuations (input noise), which would generate the same output voltage noise in an ideal noiseless device [72, 77, 79]. Alternatively, the NEP can be defined as the signal power that gives a signal-to-noise ratio of one in a one hertz output bandwidth [80]. The NEP is equal to the current or voltage noise spectral density divided, respectively, by the current or the voltage responsivity. The voltage responsivity dV/dP is defined as a measure of change in voltage to the incoming RF power at a fixed bias current, and current responsivity dI/dP denotes the current response to the RF power at a fixed voltage.

Depending on the techniques that are used for the device characterization, one can distinguish between electrical and optical NEP. Electrical NEP results from the direct thermal energy change of the detector, while optical NEP characterizes the ability of

the system to detect the incoming RF signal and includes the coupling efficiency of the whole RF system.

Since our goal of developing sensitive detectors is to measure extremely weak signals coming from deep space, we need to optimise the noise performance of the system. The total measured noise in the system includes the noise of the device and the noise of the readout electronics. In this thesis, the noise performance of the bolometer system is investigated, including amplifier noise and the bolometer noise, consisting of the SIN junction noise and noise due to electron-phonon interaction.

2.2.1. CEB noise in the voltage-biased mode

In this section, a circuit biased at fixed voltage is considered, and factors determining the current responsivity $S_I = dI/dP$ at fixed voltage are analyzed. Three independent contributions to the noise equivalent power can be distinguished:

$$NEP_{total}^2 = NEP_{e-ph}^2 + NEP_{SIN}^2 + \frac{\delta I^2}{S_I^2}. \tag{2.10}$$

Here NEP_{SIN} represents the noise of the tunnel junctions, $\delta I^2/S_I^2$ the noise of the amplifier due to its limited sensitivity δI, and $NEP_{e\text{-}ph}$ the noise due to electron-phonon interaction:

$$NEP^2_{e\text{-}ph} = 10 k_B \Sigma \Lambda (T_e^5 + T_{ph}^5) \tag{2.11}$$

The noise of the tunnel junction consists of shot noise $2eI$, the fluctuations of the heat flow and the correlation between these two processes [77]:

$$NEP_{SIN}^2 = \frac{\delta I_\omega^2}{S_I^2} - 2\frac{< \delta P_\omega \delta I_\omega >}{S_I} + \delta P_\omega^2 \tag{2.12}$$

The correlation represented by the second term in the above equation, reduces the shot noise by 30-70%, [66].

Analysis of the influence of the background power load on noise [56] shows that the optimal bolometer configuration is the CEB with voltage-biased SIN tunnel junctions and current readout by a SQUID. This is because the SQUID operates at low temperature and is a much more sensitive device than any room-temperature amplifier. SQUID detectors measure current effectively by measuring the magnetic flux, hence the voltage-biased operation of CEB is required when using SQUID-readout. For an absorber of volume of 0.01 μm^3, SQUID current noise of 5 $fA/Hz^{1/2}$ and 1 kΩ junction resistance, a total NEP = 1.2×10^{-19} $W/Hz^{1/2}$ can be achieved for a microwave background power P_0 = 0.01 pW [56]. This value is mainly determined by shot noise of the SIN tunnel junctions due to incoming power load. Electron-phonon and amplifier noise are, in that case, lower than noise of the SIN. A responsivity value

$S = dI/dP$ of 150 nA/pW can be achieved, which is determined mainly by electron temperature of the absorber and by quantum efficiency of the CEB [56].

For 300 mK operation in presence of the final background power load (P_0 = 0.1 pW) and current noise of the SQUID-amplifier of 10 fA/Hz$^{1/2}$, the analysis performed in [56] predicts NEP level of 10^{-18} W/Hz$^{1/2}$.

Quantum efficiency is defined as the number of excited electrons produced by one incident photon [66]. An incoming photon is absorbed and an electron is excited to an energy level of 4 meV for a 1 THz signal. The electron then relaxes due to electron-electron interactions and the energy is distributed between hot electrons at a quantisation level k_BT for a normal metal and between quasiparticle at quantization level Δ for a superconductor. This results in a lower quantum efficiency of ~20 for a superconductor compared to hundreds for a normal metal. Hence, using SIN junction bolometers with normal metal is advantageous in terms of quantum efficiency, compared to the superconducting absorber, and a higher responsivity is thus expected when using normal metal as the absorber material.

Low NEP and high responsivity to the incoming power are crucial parameters of a millimetre-wave detector, in particular in combination with fast response of the device.

The analysis above shows that the concept of a cold-electron bolometer can provide reasonable noise performance in the presence of a realistic background power load. Since incoming power is removed from the absorber by cooling, the dynamic range of the system is substantially increased. The CEB concept could therefore be very promising for future space telescopes operating in the millimeter and sub-millimeter regions [66].

2.2.2. CEB noise in the current-biased mode

Considering a circuit biased at fixed current, its voltage responsivity $S_V = dV/dP$ at fixed current can be investigated. In this section, operation of CEB in the current-biased mode is analyzed, which is the method realized for testing of the devices presented in this thesis. This is because room-temperature JFET and MOSFET amplifiers were used for readout electronics so current-bias mode was the only option for implementing the readout scheme.

As has already been mentioned in the previous section, a bolometer is characterized by its responsivity, noise equivalent power and the time constant. The voltage

responsivity of a current-biased CEB, S_V, represents the voltage response to the incoming power $\delta V_\omega / \delta P_\omega$, given by the following expression [66, 79]:

$$S_V = \frac{dV}{dP} = \frac{dV/dT}{G_{e-ph} + 2G_{SIN} + i\omega C_\Lambda} \tag{2.13}$$

where G_{SIN} is the thermal conductivity of SIN tunnel junction. The noise expressed by the noise equivalent power (*NEP*) can therefore be represented by three contributions. For a series array of N CEB devices, the NEP is defined as follows [66]:

$$NEP^2_{TOT} = N \times NEP^2_{e\text{-}ph} + N \times NEP^2_{SIN} + NEP^2_{JFET}, \tag{2.14}$$

Here, $NEP_{e\text{-}ph}$ represents the noise associated with electron-phonon interaction [66], NEP_{SIN} the noise of the SIN tunnel junctions, and NEP_{JFET} represents the amplifier noise. The SIN noise has three components: the shot noise and NEP associated with it $2eI/S_I$, the fluctuations of the heat flow through the SIN tunnel junctions and the correlation between these two processes [79, 81]:

$$NEP^2_{SIN} = \frac{\delta I^2}{(\frac{dI}{dV} S_V)^2} + 2 \cdot \frac{\langle \delta P \delta I \rangle}{\frac{dI}{dV} S_V} + \delta P^2 \tag{2.15}$$

This correlation is a form of the electrothermal feedback discussed earlier by Mather [82]. Due to this correlation the shot noise is increased by 30-50% in contrast to the CEB in voltage-biased mode where anti-correlation reduces the total noise [72]. The last term in the previous expression is due to the voltage δV and current δI noise of the JFET amplifier that are expressed in nV/Hz$^{1/2}$ and pA/Hz$^{1/2}$.

The availability of JFET readout electronics allows straightforward testing of our devices, whilst the employment of SQUID electronics mentioned in the previous section requires very involved laboratory equipment and advanced cryogenic electronics that might be a subject of a separate research. In the future, it will be possible to realize a voltage-bias scheme with SQUID readout that is the best implementation of CEB detection for ultimate noise performance. In this thesis, however, current biasing is used in order to demonstrate the feasibility of CEB devices as a concept.

The analysis of a single current-biased CEB with JFET readout has shown [83-85] limitations of noise performance due to decreased voltage responsivity and degradation JFET voltage noise under high optical power load due to overheating of the absorber. It was therefore proposed to use a series of bolometers combined with additional capacitances for the HF coupling, in order to improve the noise

performance and reduce NEP down to the photon noise level and below. This is because, in this case, the input power is divided between several absorbers in the array, thus limiting the electron temperature of the absorbers, which results in enhanced responsivity of the CEB array, as the voltage across all absorbers is summed and measured as total voltage collected from all the devices. At the same time, the noise is only proportional to the square root of the number of the devices, as the noise components coming from different devices are not correlated. This approach is partly realized in the current work and is presented in the Chapter 7 that discusses CEB arrays for balloon-borne telescopes.

To estimate the required number of devices in an array, for background power load of P_0 = 5 pW per polarization, the photon noise at 300 GHz could be estimated as

$$NEP_{phot} = \sqrt{2P_0 E_{quant}} = \sqrt{2P_0 \times hf} = 4.3 \cdot 10^{-17} \text{ W/Hz}^{1/2}.$$

For a given absorber material, the optimal number of the devices in an array is determined by the background power P_0 and the absorber volume Λ. By increasing the number of the devices N we can split the power load P_0 between the N bolometers until the point when the power load per device becomes equal to the phonon noise: $P_0/N = P_{ph}$, where the phonon power $P_{ph} = T^5_{ph} \cdot \Sigma \cdot \Lambda$ is determined by the volume of the absorber only. Increasing the number of the CEB devices in the array further does not yield any improvement as the power load per device becomes less than the phonon power, which saturates the sensitivity. In most practical cases, the amplifier noise dominates the junction noise, so the amplifier noise contribution is effectively reduced by increasing the number of CEBs up to the point when the amplifier noise per device becomes less than that of junction noise, thus resulting in the total noise below the photon noise level.

Bolometer arrays are discussed later in Chapter 7 of this thesis, where parallel/series arrays of several Cold-Electron Bolometers are introduced, and the experimental results are analyzed. In chapter 5, single CEB devices integrated in 97 GHz finlines are considered, with JFET readout in the current-biased mode. Although this approach does not yield maximum responsivity compared to CEB arrays, it allows investigating the performance of a CEB as a detector and the CEB-finline integrated circuit as a design to be employed in microwave systems comprising waveguides in conjunction with horns and other microwave components. In Chapter 6, single CEBs integrated in other planar antennas are presented, to be implemented in optical systems, with lenses and optical coupling for the RF signal.

Chapter 3
Fabrication

In this work, high performance devices are fabricated, to be utilized in cosmology instruments suitable for measuring very weak signals of power levels around the photon noise level, in the presence of realistic background power load. The fabrication process was therefore optimized to fulfill certain requirements regarding layout geometry that depend on a number of aspects, such as RF matching issues and thermal balance considerations. For that reason, e-beam lithography was employed for most critical parts of the design, where high-precision patterning was required. For less critical components photo lithography was used whenever possible as that process is more straightforward and less technologically demanding. Both processes are described and compared in this chapter.

3.1. General fabrication principles

Lithography is the process of transferring mask patterns to a resist film deposited on the surface of a substrate. Resist is a layer of a material sensitive to either UV radiation or electron beam (e-beam) and is normally spun on a wafer and baked at a certain temperature prior to the exposure. When positive resists are used, exposed areas are dissolved by the development process and removed, while negative resists work in the opposite way, i.e. unexposed portions of the resist are removed [86], which is useful for inverting patterns. Negative resists are often used for patterning by etching when the material deposited on the whole wafer is to be removed from the surface except for the exposed areas.

The patterns formed in this way define regions on the surface that are assigned for subsequent processing, e.g. metal deposition, wet or plasma etching, and other technological procedures, such as oxidation of the deposited materials. The design

features are first represented in the resist pattern; later, these features are replicated in the real materials, to be utilized as components of on-chip structures. This can be performed by either depositing metals into open resist windows or selective etching, i.e. removing uncovered parts of the materials previously deposited on the substrate. In this chapter, different patterning methods are discussed, including e-beam and photo lithography processes, various deposition techniques and etching processes, such as wet etching and reactive ion etching.

For the fabrication of high performance devices a clean processing room is required because the air contains many dust particles that can adhere to the surface and thus are likely to produce defects in the fabricated structures. E.g., particles remaining in a film of aluminium during its deposition or oxidation may cause inhomogeneity in the oxide film created by the oxidation of a deposited aluminium film. A particle in the oxide layer can result in increased tunnelling current at the location around the particle and possibly even leak currents through the oxide layer. Dust particles settled on the surface of a photomask interfere with mask patterns, and hence distorted patterns may be represented in the device layout. Typically, dust particles on photomasks may produce pinholes in insulating layers or short circuit different conducting parts; particles at the edges of a pattern may cause current disruptions [86].

The total number of dust particles per unit volume in a clean room, the temperature and humidity are critical parameters that are crucial for the performance of the fabricated devices. For example, in a class 100 clean room there are 100 particles of certain size per cubic foot of air. There are many more dust particles of smaller size, so for the fabrication of structures with extremely fine features a cleanroom with more stringent control of the environment is required, such as a class 10 clean room or even better [86].

3.1.1. Electron-beam lithography and photo lithography

The steps that are used for pattern transfer from a mask to a wafer are shown in Fig. 3.1. When using Si as a substrate material, an insulating layer is often formed on the surface of the Si wafer prior to the fabrication of detectors and related structures. Typically, a 400 nm thick SiO_2 layer is thermally grown on Si wafer by placing it in an oven filled with oxygen at a certain temperature. To be covered with a resist layer, the wafer is placed onto a vacuum spindle, and liquid resist is deposited onto the wafer, and then the wafer is spun at a certain speed for around 1 minute. As a result, a uniform thin film of a resist is produced on the surface of the wafer, while the thickness of the film depends mainly on the rotational speed for a specific resist at a given solvent concentration. Final thickness for a certain rotational speed is normally provided by the manufacturer for each type of resist and each value of solvent

concentration. E.g. spinning 10% copolymer resist dissolved in Ethyl Lactate at 3000 rpm yields c:a 350 nm thick copolymer resist film.

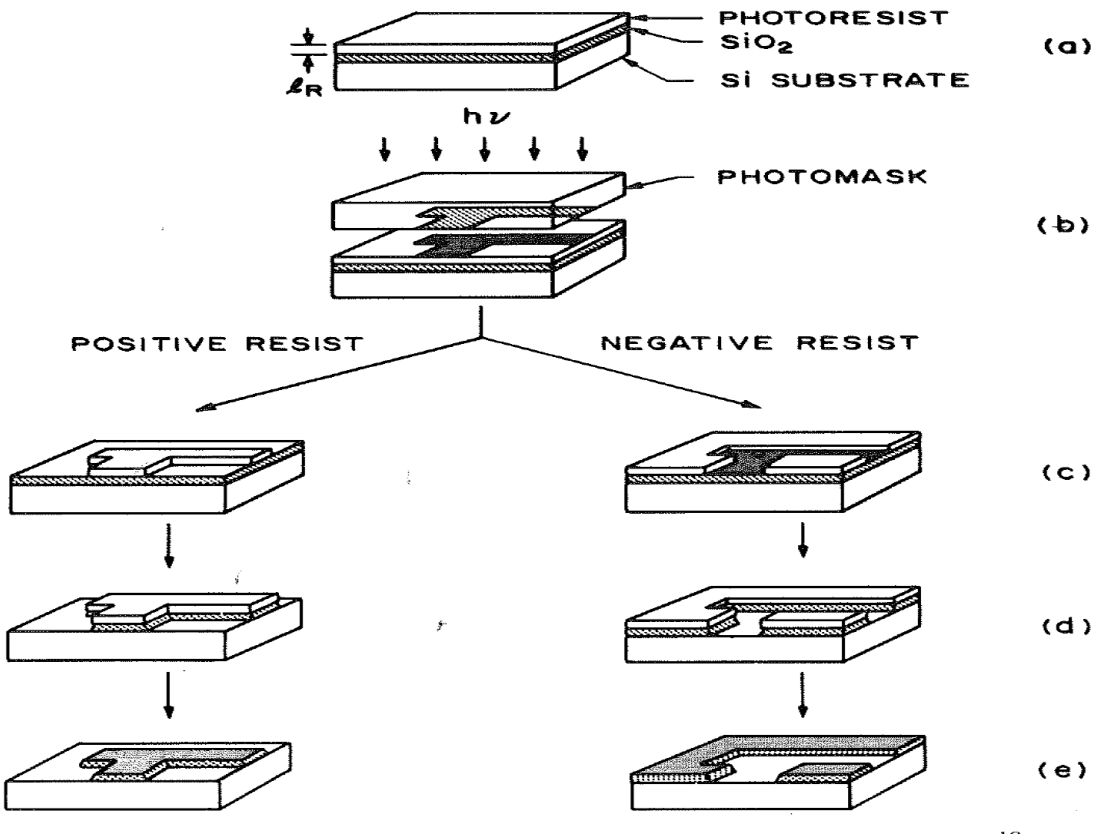


Figure 3.1. Details of an optical lithographic transfer process [86].

For fabricating samples in this thesis, a spin speed of 3000 to 6000 rpm was used to give a 100 – 900 nm thick resist film while using lower rotational speed might result in non-uniform films, which is undesirable for both photo and e-beam lithography. After spinning the resist, it is normally baked either on hotplate or in oven at temperatures of 90 – 195 ºC. Once baked, the resist is ready for the UV or e-beam exposure. The wafer with the resist is then exposed to UV radiation or an electron beam. After exposure, a post-exposure baking at 110 – 130 ºC may be required for certain resist types to accomplish the process. When using positive resist, the resist in the exposed areas is to be dissolved in the developer, which is usually done by dipping the wafer into the developer; after that the wafer can be rinsed and blow dried with nitrogen. A positive resist pattern is thus formed on the substrate (Fig. 3.2a and 3.2b). The material is then deposited over the whole surface of the wafer, including the resist and the substrate (Fig. 3.2c). Any contact of the deposited material with the resist walls around windows should be avoided; hence, the material layer that is deposited must be thinner than the resist film. As a rule, the thickness of the deposited material should not exceed a half of the total resist thickness. The parts of the material film that are deposited on the top of resist layers are then removed by dissolving the resist in a liquid solvent that selectively removes organic resists while keeps the

deposited materials untouched. As a result, the material film on the top of the resist layer is lifted off and thus removed (Fig. 3.2d). This patterning method called ***lift-off*** technique is extensively used for fabricating e.g. microwave and millimeter-wave detectors, as it provides high resolution and other characteristics required for high-performance device fabrication.

When using negative resists combined with etching, the unexposed areas are removed; this results in a reversed image in the resist pattern regarding the pattern in the required layout. The wafer is then subjected to plasma etching or wet etching that removes the materials within the open resist windows but does not affect those covered by the resist mask. E.g., H_3PO_4 based etchants are often used for Al wet etching, while CF_4 plasma can be used for NbN patterning. Finally, the resist is removed using a solvent, e.g. acetone or Shipley remover, and a material pattern replicating the original layout is left on the surface.

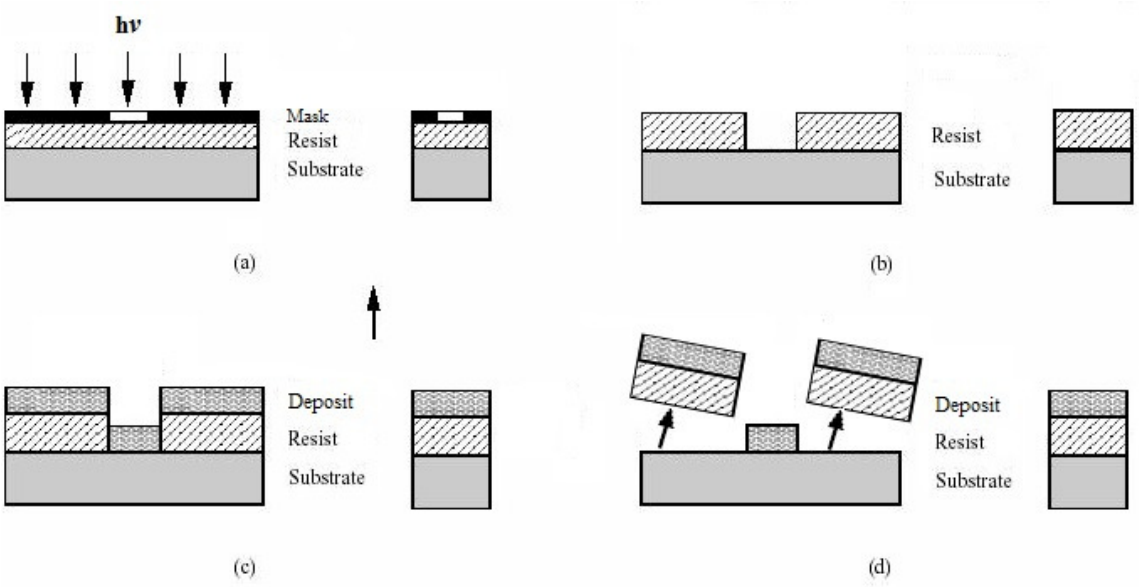


Figure 3.2. Lift-off process: a) Illuminating of positive photoresist through a photomask; b) development; c) deposition of the material; d) lift-off [86]

Many structures presented in this thesis were patterned with positive e-beam lithography and lift-off. Photo lithography was used for some samples, and negative e-beam lithography combined with etching was used for several devices. Exposure, development and deposition with lift off are performed in the same way when using either e-beam or photo lithography.

When using e-beam lithography, exposed areas are defined by an electron beam focused on the surface of the wafer and controlled by e-beam machine. The JEOL JBX-5DII machine employed at Chalmers for fabrication of the devices presented here employs accelerating voltage of 50 kV and two magnetic lenses for focusing: a

lens for rough exposures and another one for exposing fine patterns. The JBX-5DII machine consists of the main console (Fig. 3.3) and the computer system. The main console includes the optical system and the mechanical system.

The electron optics system operates as follows. The electron gun generates a beam of electrons; the JEOL JBX-5DII system employs an electron gun using LaB_6 single crystal cathode. The lens system consists of two intermediate lenses (second and third lenses) and one objective lens (fourth or fifth lens) focusing the electron beam onto a spot on the wafer surface. Beam-blanking plates are used to turn the electron beam on and off. A mechanical stage moves the substrate from one position to another during the exposure; this is necessary because the scan field size is 800×800 μm for the 4^{th} lens and about 80×80 um for the 5^{th} one, which is often much less than the area to be exposed. All the coils, lenses and the mechanical stage are controlled by a computer.

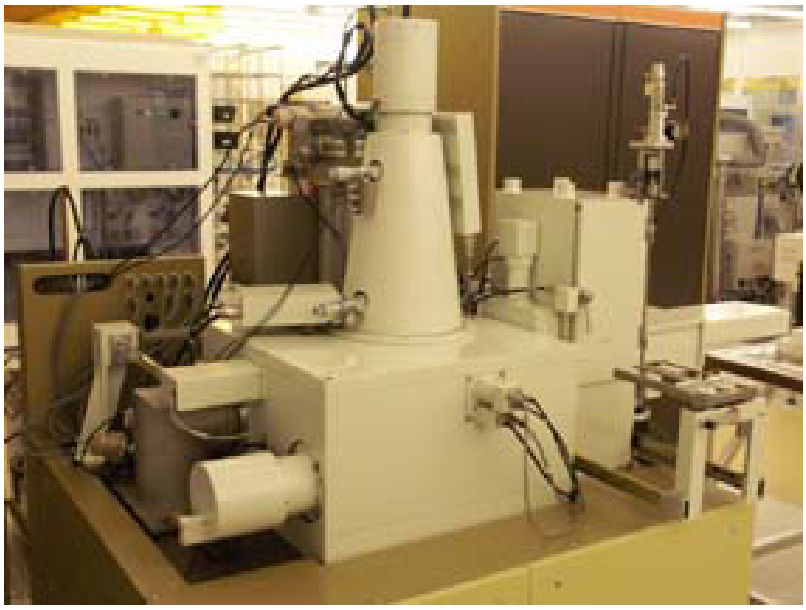


Figure 3.3. JEOL JBX-5DII e-beam machine, photo of the Main Console [66].

Either the fourth lens or the fifth lens is used as the objective lens, depending on the application: the fourth lens is used for larger patterns (down to submicron scale), and the fifth lens is used for smaller patterns (down to nanometer scale). The beam size can be changed by changing the currents of the second and third lenses.

The advantages of using the e-beam lithography are nanometer-scale writing, automated operation with full control, and direct writing on a wafer, without photo mask. A disadvantage of e-beam machines is the relatively low speed of processing: exposing contact pads on a 2-inch CEB wafer takes 4 to 5 hours compared to ~17 s when using optical lithography. The speed of operation of the e-beam machine depends on the largest beam diameter that is acceptable for the given minimum feature size of the structure. Hence, an exposure of large areas with submicron

resolution might require as much as 15 hours. Such a speed could be acceptable for fabricating photo masks or for patterning small on-chip areas with delicate design features. In the designs presented in this thesis, CEB absorbers, tunnel junctions, gates for THz sensors, and nano-bridges for phase switch devices were most often exposed using e-beam machines, when narrow lines are required by the design considerations.

3.1.2. Development

Developing the resist is the last lithography step which contributes to patterning the resist film across the surface of the wafer. In essence, this is a chemical wet etching process. E-beam resists are normally developed just before evaporation, while for most photo resists the development follows directly after exposure, including UV5, which happens to also be used as a resist for some e-beam exposures. Some resists must also be baked immediately following the exposure to ensure proper development.

3.1.3. Photoresist and e-beam resist

The photoresists are compound materials sensitive to the UV radiation. Most photoresists, including the ones used in this thesis, can be classified as positive, due to the type of their response to the exposing UV radiation. After the exposure, uncovered regions become soluble and therefore removed during the development. As a result, the patterns formed in the positive resist are the same as in the original layout. For negative resists, the unexposed areas are removed during the development, and the patterns formed in the negative resist are the reverse of the original layouts.

In [86], three components of positive photoresists are distinguished: a photosensitive compound, a base resin, and an organic solvent [86]. The solvent is mainly used to keep the resist liquid in the beginning to facilitate spinning the resist, and later part of it evaporates during the baking after spinning. The unexposed photosensitive compound is insoluble in the developer, while the UV illumination of the exposed areas changes the chemical structure of the compound in these areas, so the compound becomes soluble and can easily be removed during the development.

In negative photoresists that are polymers combined with a photosensitive compound, the latter receives the electromagnetic energy during exposure [86], which initiates a polymer linking reaction, shown in Fig. 3.4, thus causing cross linking of the polymer molecules. Finally, the polymer becomes insoluble and hence remains on the surface of the wafer, while the unexposed areas are removed during the development. In this process, the resists partly absorbs the developer solvent, which increases its final mass

and size, thereby limiting the resolution by negative exposure, being the major drawback of negative photoresists [86].

Positive e-beam resists are in essence polymers, in which a chemical change is induced by the electron beam. During the e-beam exposure, the interaction between electrons and polymer chains causes chemical bonds to be broken by the electrons with high kinetic energy and form shorter molecular fragments, Fig. 3.4a. In the exposed area, the molecular weight of the polymer is reduced, and the irradiated resist is dissolved in a developer. One of the most common positive e-beam resists that allows for manometer resolution is Poly Methyl Methacrylate, or PMMA, used in this thesis for most exposures.

In negative e-beam resists, the electron beam provokes polymer linking as shown in Fig. 3.4b. The polymer cross-linking creates three-dimensional structures [86] that are not affected by the developer solution, while the rest of the resist is dissolved during the development.

3.1.4. The Proximity Effect

The resolution of photo lithography is determined by the UV wavelength as the image transferring is limited by diffraction of UV radiation. For the e-beam exposures, possible distortions of the image can occur due to the electron scattering, which determines the quality of the resulting resist pattern. After penetrating the resist film, electrons collide with atomic lattice of the substrate or the deposited material, which results in possible backscattering, thus deteriorating the resolution and modifying the resulting image. The accelerating voltage in the e-beam system used in this thesis is 50 kV, so the de Broglie wavelengths of the electrons are in the nanometre range.

Due to backscattering, electrons can expose the resist far away from the electron beam centre (Fig. 3.5). The beam at each point affects the exposure in neighbouring areas, so the total effect can be expressed by the total dose that is given by the sum charge of the electrons in the main beam and re-scattered electrons from the neighbouring areas. Due to this effect, known as the ***proximity effect***, large areas are overexposed and are therefore enlarged in the resist patterns, while very narrow lines are underexposed and are therefore not developed properly. Besides, this effect limits the minimum spacing between different exposed parts of the pattern as neighbouring parts can merge when overexposed due to the backscattering. For the ***proximity correction***, different segments of the pattern are exposed by different doses; the final exposure dose is thus made of the sum charge of the incident electrons in affected segments of the pattern and the electrons re-scattered from the surface in other segments [86].

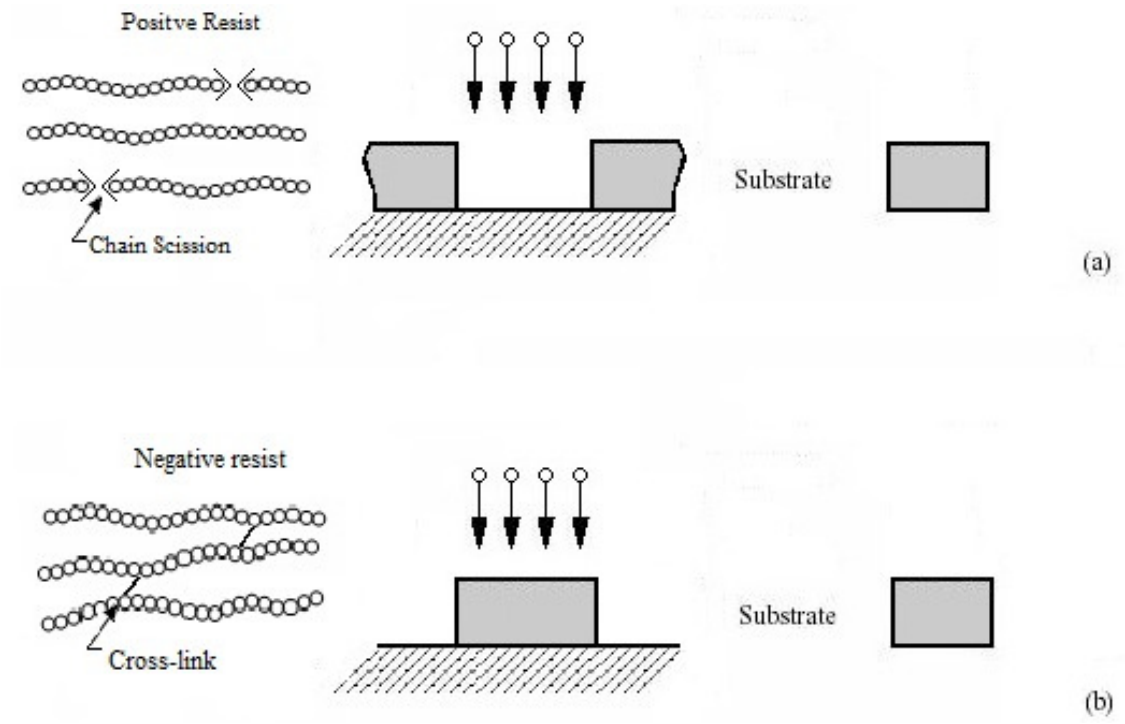


Figure 3.4. Cross-liking in positive (a) and negative (b) e-beam resists [86].

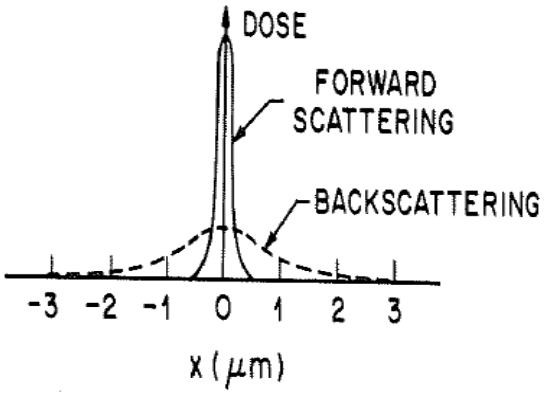


Figure 3.5. Dose distribution in the vicinity of the substrate surface [86].

3.1.5. Thermal evaporation and lift-off

Most materials in devices presented here were deposited using thermal evaporation, including the aluminium layer for tunnel junctions in trilayer structures. A source filled with the material to be deposited is placed at the bottom of a vacuum chamber, and the wafer is mounted on the interior side of the top of the chamber. The source is then heated by an electric current, thus melting the material and causing it to evaporate. When the evaporated material reaches the wafer, it condenses on its surface and crystallizes.

a) 

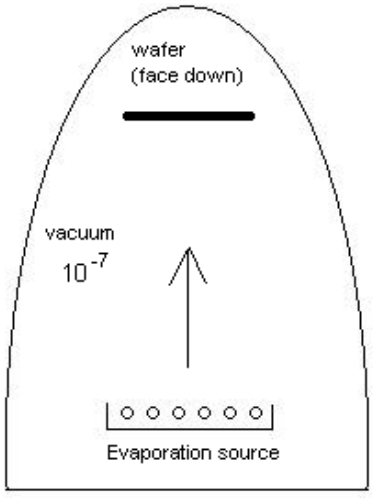
b) 

Figure 3.6. a) BOC Edwards HPTS Evaporation system; b) schematic view of the evaporator.

For the fabrication of tunnel junctions, appropriate evaporation rate should be maintained to enable proper crystallization. For aluminium, a rate of 2 – 8 Å/s is often used, being optimum rate for reasonable Al film property and hence Al oxide quality. A photo of the thermal evaporation system utilized for SIN devices fabrication is shown in Fig. 3.6a and a schematic view in Fig. 3.6b.

After the evaporation, the resist with redundant material on the top is removed by dissolving it in acetone or other solvent, e.g. Shipley 1165, remover. To alleviate the lift-off, a so-called lift-off layer is normally deposited prior to the top resist layer. The lift-off layer is developed just after the development of the top resist layer, either by the same developer or by different one. In the case of photo lithography, the lift-off layer is normally not sensitive to UV exposure, so it is plainly etched by the developer in the open windows. In the e-beam lithography processes, lift-off resist must be exposed at higher dose to obtain an appropriate undercut, i.e. slightly larger area of the developed lift-off layer compared to the resist layer. This results in a gap between the deposited material and the walls of the developed resist, which makes the lift-off process easy and straightforward.

3.1.6. Thermal evaporation of SiO / SiO_2 dielectric layer

To produce on-chip capacitors, insulating oxide layers are deposited, such as SiO and SiO_2. Both materials are widely used as insulating layers for planar on-chip capacitors. A source used in the Edwards BOC system for thermal evaporation of SiO is shown in Fig. 3.7a as a schematic view, and the photo is shown in Fig. 3.7b.

The source is made of 1 mm thick Mo plate and consists of three parts, namely a container for SiO, a lock with small holes and another top lock with a large hole in the middle. The main container is 11 mm wide, 21 mm long and has 11.5 mm long extensions from both sides for bolted contacts. The intermediate lock has 5 holes from

each side, 1.7 mm diameter each. The top lock has a 5 mm diameter hole in the middle. The latter is required for prevention from the re-sputtered material during the thermal SiO evaporation. When the top lock is used, the material remains on the surface of the intermediate lock in the form of large grains, and only the gaseous form of SiO leaves the boat and expands towards the wafer where it is deposited. 45 to 100 nm of SiO were successfully deposited with this source at a rate of 0.3 - 0.5 nm/s and a pressure of 10^{-6} mbar.

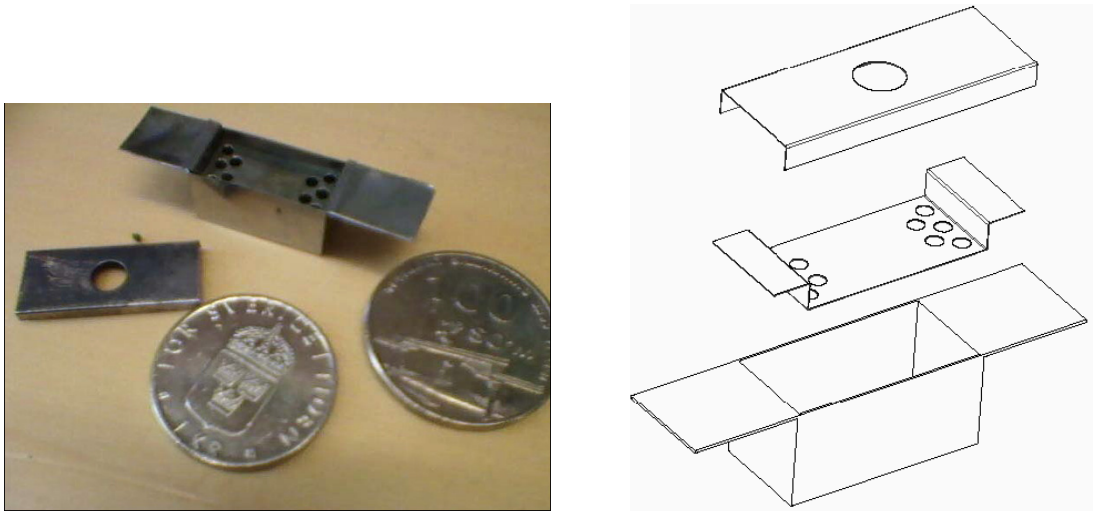


Figure 3.7. Mo boat for SiO evaporation, fabricated at Chalmers, a photo and schematic view

Another method of producing an insulating layer is to deposit SiO_2 in an electron gun (e-gun) evaporation system (Fig.3.8). In that case, the material is heated by electron beam and as a result deposited in the same way as when evaporated due to joule heating. In this thesis, e-gun evaporation systems were often used for the deposition of materials with rather high melting temperature, 2500 ºC and above, e.g. Ti and SiO_2. Thermal evaporation by joule heating is not efficient for such materials and is therefore not the best option for the deposition of those. Another e-gun evaporation system used for deposition of some metals is shown in Fig. 3.9.

Figure 3.8. AVAC HVC600 e-gun evaporation system.

Because of poor adhesion of both SiO and SiO_2 to the surface of SiO_2 substrates and metals, an adhesive layer may be used to overcome this issue. In most SiO and SiO_2 structures in this thesis, a 10 nm layer of Al_2O_3 was deposited prior to SiO or SiO_2 on the metal surface.

Figure 3.9. Balzers BAK600 e-gun evaporation system.

3.2. Fabrication of CEB devices and on-chip SIN thermometers

The CEB is a microwave detector made of a normal metal absorber with two or more Superconductor-Insulator-Normal metal (SIN) junctions for temperature measurements and detection of millimetre-wave radiation. Properties of SIN tunnel junctions, such as the dependence of current-voltage characteristics of the SIN junction on the temperature, are utilized in both applications [58-61]. Hence, the design and performance of CEB devices depend substantially on properties of SIN tunnel junctions employed and are therefore determined to a large extent by the details of the SIN junctions fabrication procedure.

For example, the dynamic resistance at the bias point affects noise matching with the readout amplifier. At the same time, experience shows that tunnel junctions with relatively high specific normal resistance exhibit a reasonably good ratio of the normal to subgap dynamic resistance as the sharpness of IV curve depends on the oxidation time and thus normal resistance. Experience shows that a longer oxidation time and a thicker oxide barrier provide a robust oxide barrier, consequently reducing leak currents, which yields higher ratio between the normal and subgap resistance and hence a sharper IV-curve. The superconducting gap should be large enough at operating temperature to enable strong voltage to the temperature response as gap suppression reduces the voltage response.

Assuming that JFET room-temperature amplifiers are to be used for the readout, an optimum dimensioning of the system topology implies typically normal resistance values of 1 to 10 kΩ, while employment of CMOS readout electronics allows using tunnel junctions with normal resistance of tens to hundreds of kΩ. In this thesis, tunnel junctions of areas of 1.5 to 4 μm^2 were implemented in CEBs fabricated using Trilayer Direct-Write technology with 12 Å thick Al_2O_3 layer as insulator, while junctions of area of 3 to 20 μm^2 were used for the fabrication of CEBs with TiO_x as an insulating barrier. This choice yields maximum voltage response at a reasonable normal to dynamic resistance ratio. For that reason, e-beam lithography must be employed for CEB fabrication by means of trilayer process with Al_2O_3, while it is still possible to utilize photo lithography to fabricate CEB devices with TiO_x as insulating barrier.

CEB devices with SIN tunnel junctions were traditionally manufactured using the so-called shadow evaporation technique based on one-cycle deposition of both superconducting electrode and normal metal absorber. First, the superconducting electrode was deposited at a certain angle and oxidized; then the table with the substrate was rotated so the absorber was deposited at another angle, resulting in a small overlap area constituting the tunnel junctions. This technique has certain advantages, such as its simplicity and an option of producing narrow absorbers and small tunnel junctions, and has therefore been used for years for SIN tunnel junction fabrication, especially in laboratory and academic environment as it does not require advanced equipment. However, it is not the most appropriate technique for fabrication of CEB operating at frequencies below ~300 GHz and it has many drawbacks and limitations.

The main limitation is related to the size of tunnel junctions which cannot be made as large as required due to the principle of shadow evaporation. It makes the shadow evaporation technique very practical for applications in single-electronics where small area of tunnel junctions is advantageous. But for CEB fabrication, this approach can only be used within certain frequency ranges, down to ~300 GHz, due to the small area of tunnel junctions fabricated using this method and hence relatively low capacitance value for RF signals. Besides, geometry considerations impose certain limitations on chip layouts and orientation of on-chip structures. In addition, this technique does not allow for use of magnetron sputtering which is commonly used in industry for manufacturing of high-quality tunnel junctions.

The CEB devices presented in this thesis were all fabricated using cleanroom facilities at the Department of Microtechnology and Nanoscience at Chalmers University in Sweden.

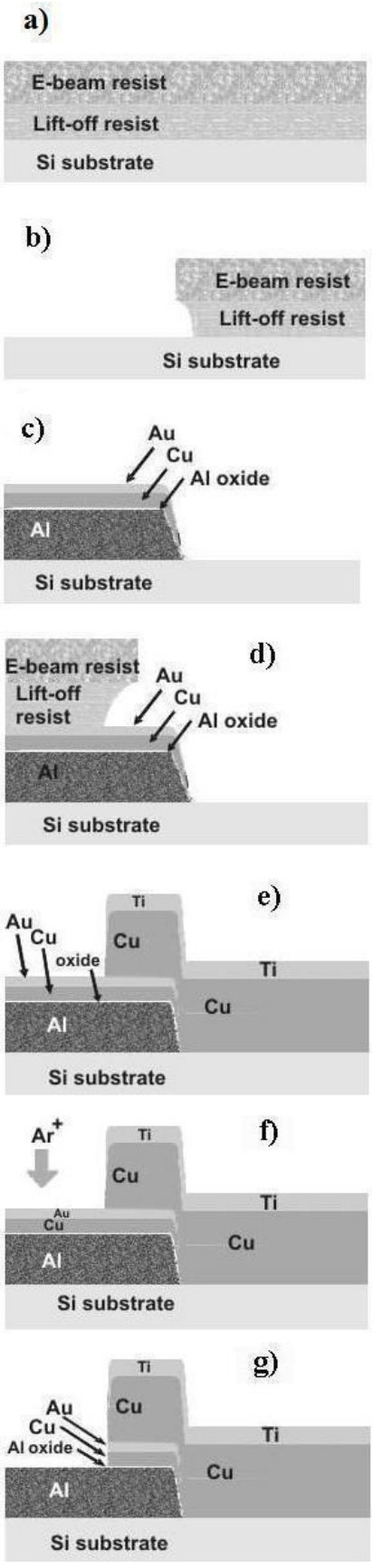
3.2.1. Trilayer Direct-Write technology for fabrication of CEB and SIN thermometers

Fabrication of high quality CEB devices required the development of new technologies, such as a direct-write Trilayer technology [Paper I] for manufacturing Al-based SIN tunnel junctions operating at 100-300 mK, which is the temperature range in which the bolometer operation is most efficient in terms of responsivity (dV/dP) and sensitivity (low noise). Direct writing means that the pattern in the drawing is directly transferred to a pattern in the resist layer and hence in the deposited material, unlike e.g. techniques employing shadow evaporation, causing the pattern to get distorted during the process, due to different evaporation angles.

The trilayer technology allows manufacturing SIN tunnel junctions of high quality, suitable for fabrication of millimetre-wave detectors and cryogenic thermometers. In this technology, the deposition procedure and direct writing of both superconductive layer and absorber do not impose any requirements on deposition of both layers in one vacuum cycle of evaporation. This simplicity of the technology provides additional freedom in realizing any possible layouts and any geometry.

The procedure of fabricating CEB and SIN thermometers using Trilayer technology, can be described as follows, Fig. 3.10. A silicon wafer, oxidized thermally to obtain 400 nm oxide thickness, is covered by a lift-off resist LOR3A and a positive photo resist S1813 and baked. Contact pads are then patterned by a standard process of photo lithography including exposure in a UV mask aligner and development by the MF-319 developer. Next, the wafer is cleaned using a standard reactive ion etching process in oxygen plasma for 30 seconds. A thin gold layer can then be deposited after the e-beam lithography for better alignment with the following layers (this layer is optional).

SIN tunnel junctions are created as an overlap between a normal absorber and an Aluminum superconducting electrode [Paper II]. For patterning the Al electrode, a lift-off resist and e-beam resist are spun over the wafer (Fig. 3.10a), exposed by the electron beam, and developed (Fig. 3.10b). Alternatively, a photo resist and photo lithography could be used for patterning at this step, if the resolution requirements are less rigorous. Then, an Aluminum layer is deposited at a base pressure of $\sim 10^{-7}$ mbar and oxidized during ~30 minutes in oxygen ambient at $\sim 5 \cdot 10^{-2}$ mbar. Then, a layer of copper is deposited as a normal metal electrode of the tunnel junction and covered by gold for passivation (Fig. 3.10c). Next, the normal metal copper/chromium absorber is patterned using e-beam lithography and deposited by means of thermal evaporation (Fig. 3.10d,e).



=> Si wafer with 400 nm thick SiO_2 layer covered with lift-off resist and e-beam resist or a photo resist; both spun and baked.

=> The resists exposed and developed. The bottom resist layer is slightly overexposed and /or overdeveloped.

=> The materials are deposited and lifted off: Al deposited as a first layer, then oxidized in oxygen; Cu deposited as second layer and then Au deposited for passivation. The tunnel junctions are created between Al and Cu with Al_2O_3 as tunnel barrier.

=> Next lithography: two resist layers are placed on the top of the Al-Cu-Au Trilayer structure.

=> The Cu/Cr absorber is deposited and lifted off. Absorbers are normally covered as by a hard material such as Ti with natural TiOx layer that is resistant to Ar ion beam etching.

=> Tunnel junctions shaped using self-alignment: Au and Cu are removed from areas, not covered by Ti and TiOx , using Ar ion beam etching (ion milling)

=> The profile of the final structure. Tunnel junctions are located between Al and Cu, to the right from the arrows

Figure 3.10. CEB and Thermometers fabrication procedure, Trilayer technology [Paper II]

Finally, argon ion beam etching performed in Oxford CAIBE system is used to remove copper and gold from the top of the trilayer structure, see Fig. 3.10 (f,g). An AFM image of an example CEB device fabricated in this way is shown in Fig. 3.11.

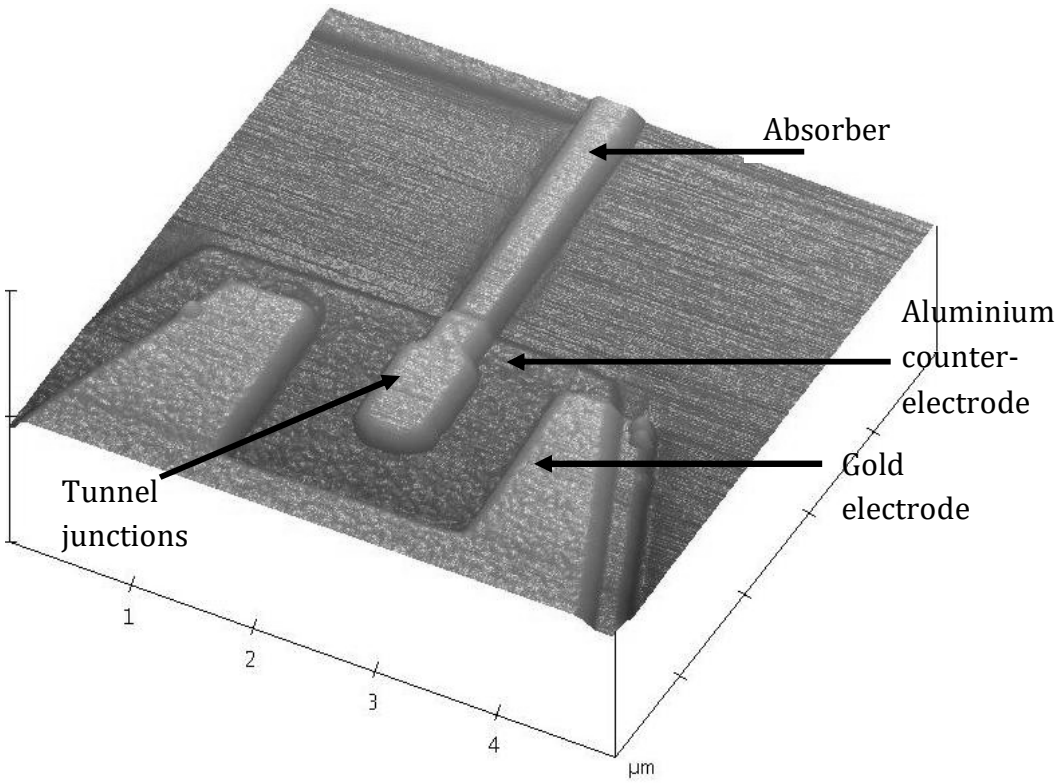


Figure 3.11. An AFM image of a CEB device fabricated with Trilayer technology [55].

The fabrication method described here is suitable for fabricating SIN thermometers and CEB devices with large area tunnel junctions and big absorbers. For CEB, the main drawback of this method is the deposition of the absorber on the top of the superconducting Al layer, resulting in a bigger absorber than in the case when the absorber is deposited first. This is because every consequent layer must be thicker than the previous one to enable a secure contact between successive layers. As a result, thin and narrow absorbers cannot be fabricated using this method. Besides, the absorbers fabricated using this method are not flat and contain bending parts on the top of the tunnel junctions. Another disadvantage of this method is the limited temperature at which the resist for absorber patterning is baked. When the resist is baked after creating the tunnel junctions, the temperature should not exceed 140 ºC, in order not to endanger the junctions. This deteriorates the resolution of the lithography and therefore limits the minimum size of the absorber fabricated using this method. In the next section, a novel approach is presented, that does not have these limitations.

3.2.2. Titanium-based fabrication technology

This is a simple and efficient direct-write technology for fabricating Ti-TiO_2-Al SIN tunnel junctions for bolometer devices and thermometry, using titanium oxide as a tunnel barrier [Paper III]. The key point of this technology is deposition of a normal Ti film as a bottom electrode and the superconducting Al film as the top layer after oxidation of Titanium.

As stated in the previous section, the CEB performance is largely determined by the properties of the SIN tunnel junctions. Another important aspect is the CEB layout and geometry considerations. One of the key parameters of a CEB is the volume of the absorber that determines the bolometer's sensitivity due to the principle of operation of a CEB. As indicated earlier, a big absorber limits the performance and the cooling ability of the CEB. The size of the absorber is therefore to be minimized; a thinner absorber increases the sensitivity and ensures efficient electron cooling.

The Titanium-based approach allows to realize thicknesses of the absorber down to 5 nm as the absorber is deposited prior to the other electrode and the tunnel junction is created after deposition of the absorber. Another advantage is the ability to realize a fully flat absorber without bending parts that are inevitable in most other processes and create leak currents degrading the performance of the microwave detector.

In addition, there are no limitations on the width of the absorber related to lithography resolution due to limited resist baking temperature, since the absorber is patterned before creating tunnel junctions.

The process includes two steps of lithography and deposition: first, the Ti film is patterned, deposited and oxidized, and then the Al counter-electrode is deposited and patterned. It uses ex-situ Ti oxidation for creation of TiO_X insulating barrier. The details of the fabrication process are shown in Fig. 3.12.

In the first step, a photo resist is spun and baked on a thermally oxidized silicon substrate for the following optical lithography. After exposure and development, a Ti film is deposited by magnetron sputtering. After lift-off and oxygen plasma etching, the surface of Ti is cleaned using ion milling in Ar ion beam and oxidized in oven in air ambient. Then an Al film is deposited and patterned by photo lithography and chemical wet etching. The final structure after resist stripping is shown schematically (Fig. 3.12 j) and in an optical image (Fig. 3.13).

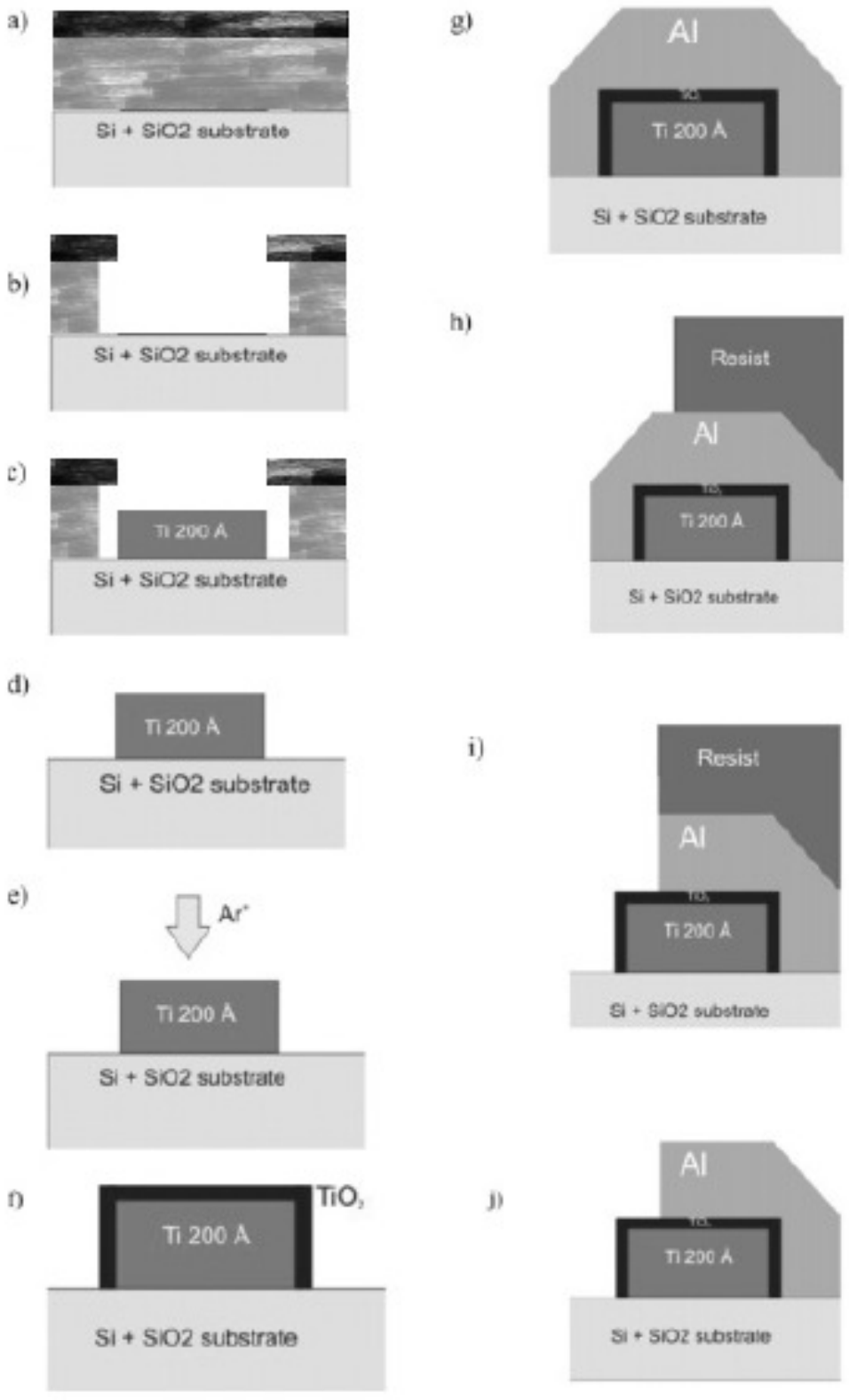


Figure 3.12. Fabrication procedure for Ti-based technology. A lift-off layer and photo resist are spun and baked (a). After exposure and development (b), a Ti film is deposited by magnetron sputtering (c). After lift-off (d), the surface of Ti is cleaned using ion milling in Ar ion beam (e) and then oxidized in oven (f). An Al film is deposited (g) and patterned by lithography (h) and chemical wet etching (i). Final structure after resist removal (j).

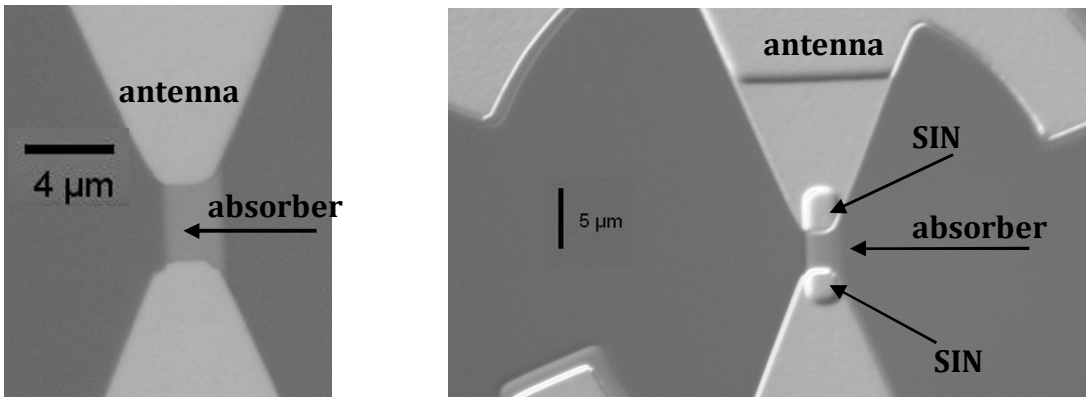


Figure 3.13. Optical image of a CEB fabricated in the Ti technology: a plain photo and a quasi-3D picture of the central part [Paper IV].

3.3. Fabrication of CEB-finline Integrated Circuits

In this section, the fabrication of CEB devices integrated in unilateral finlines is described, shown in Fig. 3.14. The finline taper was designed and optimized using software developed by Oxford Physics team [5, 26]. As has already been shown, a finline-CEB integrated structure is an attractive implementation of a CEB concept so the available technologies should be accommodated to fabricating SIN bolometers across the slot of a unilateral finline [Paper V], [87]

The finline considered here is a tapered unilateral finline 1270 μm wide and 3 mm long with a slot width of 5 μm, deposited on a 200 μm thick silicon substrate, which yields a characteristic impedance of ~42 Ω. The CEB device deposited across the slot consists of a 4 μm long absorber with two 2×2 μm^2 SIN tunnel junctions. [87]

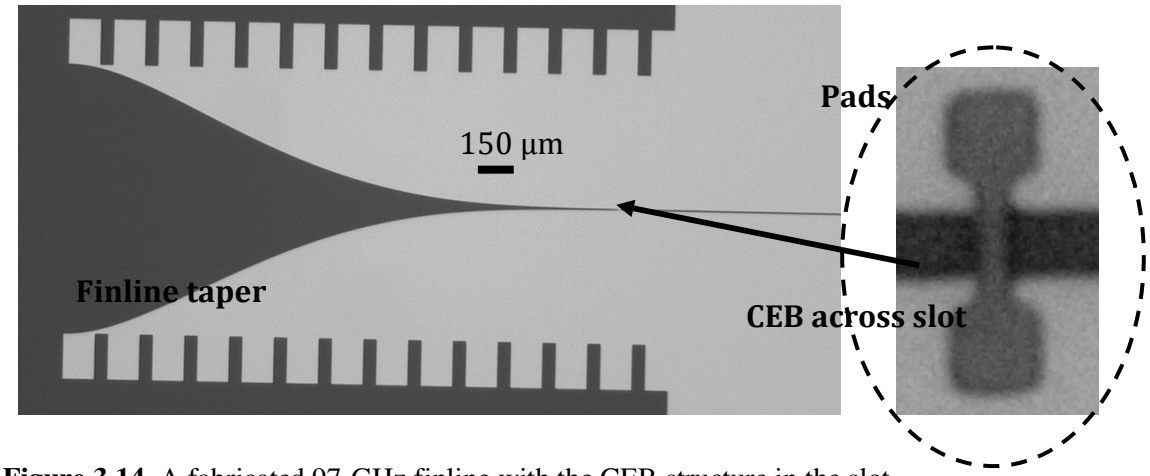


Figure 3.14. A fabricated 97-GHz finline with the CEB structure in the slot.

The CEB samples have been fabricated using e-beam lithography in direct-write mode according to the trilayer technology principle of fabricating tunnel junctions as described in section 3.2.1. Firstly, gold contact pads and wires are created using e-beam exposure and thermal evaporation. Then, Al finlines are produced, and the Cold-Electron Bolometers are fabricated in the middle of the finline slot using Trilayer process described above and presented in [Papers I, II]. As the last step, the Cu-Au layer on the top of the trilayer structure was removed by Ion-Beam Etching. The photo of the fabricated finline-CEB is shown in Fig. 3.14.

3.4. Fabrication of nanoswitches

The devices described here are nanoswitch bridges positioned across back-to back finline slots [55, Paper VI]. The switches are made of NbN as it has a high specific resistance in the normal state, – a crucial property for this application, due to the greater Open state resistance of the switch. The series resistance of a 0.5 μm wide nanobridge amounts several hundred Ohms which is essential for a reasonable On/Off power ratio. At the same time, NbN is a superconductor with the critical temperature of ~10-14 K, which implies a low impedance value in the Closed state. The finlines are fabricated of NbN and partly covered by a ~100 nm gold layer. The on-chip wires and contact pads are also made of NbN and gold.

The finlines presented here are 950 μm wide and ~2 mm long with a slot width of 5 μm, fabricated on silicon and quartz substrates (fused silica). Experience shows that crystalline quartz is not a good option as a substrate material due to mechanical tension arising during the deposition of the NbN film, resulting in cracks in the NbN film and on the substrate surface.

The method used for patterning the phase switch devices employs negative e-beam exposure of an image-reversal resist and subsequent plasma etching. In this process, the unexposed areas are removed, which results in the reverse of the pattern in the original layout. The NbN film is then subjected to CF_4 plasma etching that removes the material within the open resist windows. Hence, the final NbN structure reproduces the original layout, and the NbN bridges are observed on the surface after removing the remaining resist with Shipley 1165 remover.

The phase switch devices are fabricated by patterning back-to back unilateral finlines and nanostrips across the terminals of each finline in one lithography step on a NbN film deposited on a whole surface of a ~200 μm thick wafer. The fabrication process of the phase switch circuits includes two lithography steps, namely a photo lithography for patterning gold electrodes and e-beam lithography for patterning the structures made of NbN. The whole fabrication procedure is shown in Fig. 3.15.

The deposition of NbN (Fig. 3.15a) is performed using a niobium cathode in argon-nitrogen mixture plasma. The final thickness of the deposited NbN layer varies between 20 and 150 nm.

First, a thin Ti film is deposited on a quartz substrate by magnetron sputtering of Ti. This layer deposited prior to NbN for better adhesion also improves the superconductive properties of the nanostrip. This allows achieving higher critical temperature compared to that for NbN deposited directly on Quartz [55, 88]. Next, a NbN film is deposited by magnetron sputtering on a niobium cathode in an argon-nitrogen plasma mixture (Fig. 3.15a). This layer of NbN can be deposited either on a hot substrate heated by a lamp before and during the deposition [88] or on a substrate in a chamber without additional heating. The room-temperature deposition yields a critical temperature (11 - 12 K) that is somewhat lower than that of the films produced with heating (~14 K) but sufficient for the purposes in this thesis. Samples on Si substrate fabricated at room temperature have critical temperature of ~8 K, to be compared to ~10 K for the samples fabricated with heating.

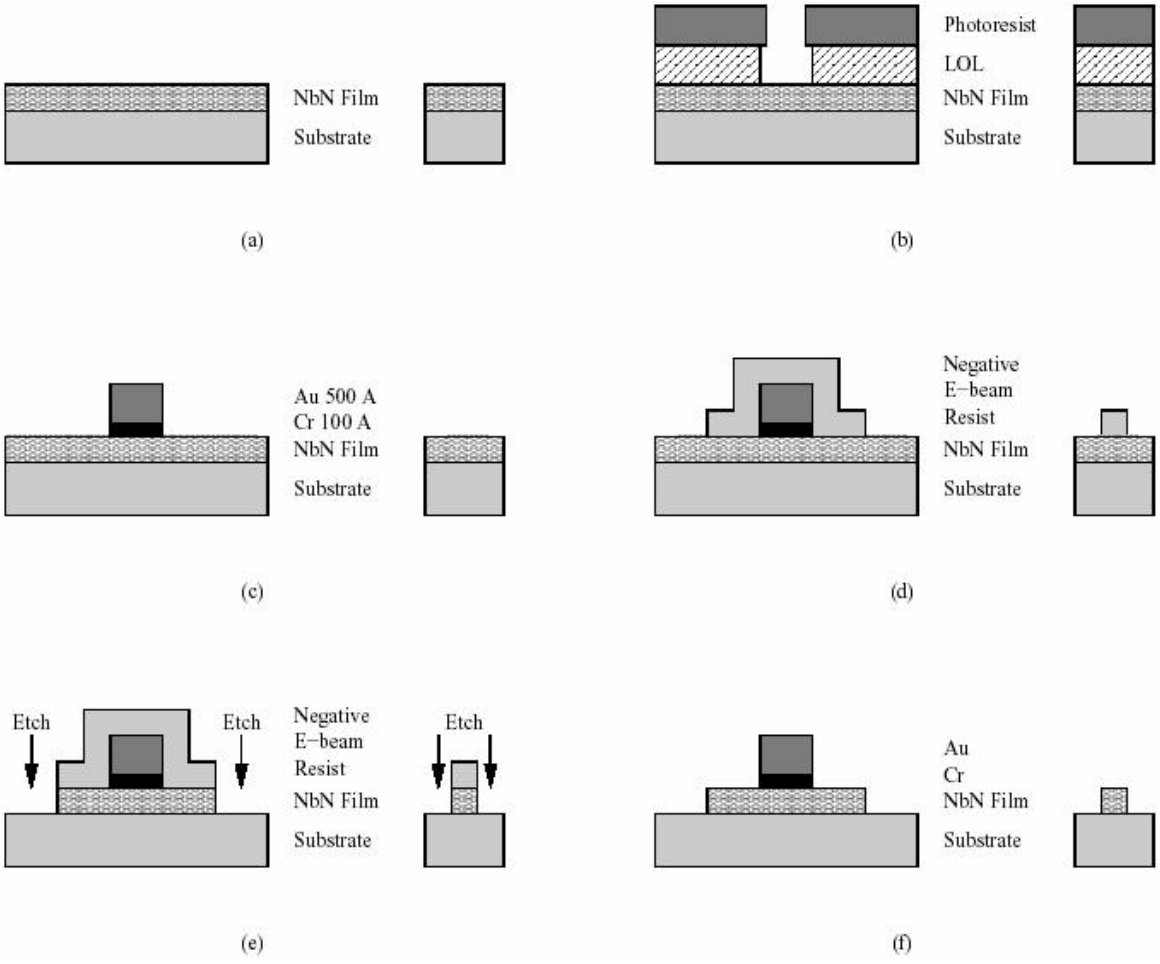


Figure 3.15: Fabrication of the nanostrip across a unilateral finline [18].
On each picture: (Left) Finline, (Right): nanobridge.

Two layers of resist are then spun on the wafer: a lift-off resist LOR3A and a photoresist Shipley S-1813. After baking both of the resist layers, the wafer is exposed to UV radiation at wavelength of 400 nm through a photo mask to pattern the gold pads and gold electrodes. After development of the photoresist, an undercut is formed in the lift-off layer (Fig. 3.15b). The wafer is then cleaned in a dry etching process by soft oxygen plasma and then a thin layer of chromium and ~100 nm of gold are evaporated through the open resist windows and lifted off (Fig. 3.15c).

The next process step is the e-beam lithography for the patterning of the NbN nanostructures. First, the negative e-beam resist SAL-601 is spun on the wafer and baked (Fig. 3.15d). Then, the NbN structures are patterned by an e-beam exposure.

After the development of the e-beam resist, the NbN structures are created by the reactive ion etching in CF_4 plasma (Fig. 3.15e), performed in Oxford RIE/CVD system. The rest of the resist is then removed in the Shipley 1165 remover (Fig. 3.15f) and finally the wafer can be diced using a diamond saw. An example device with a 5 µm long nanostrip integrated in a finline is shown in Fig. 3.16.

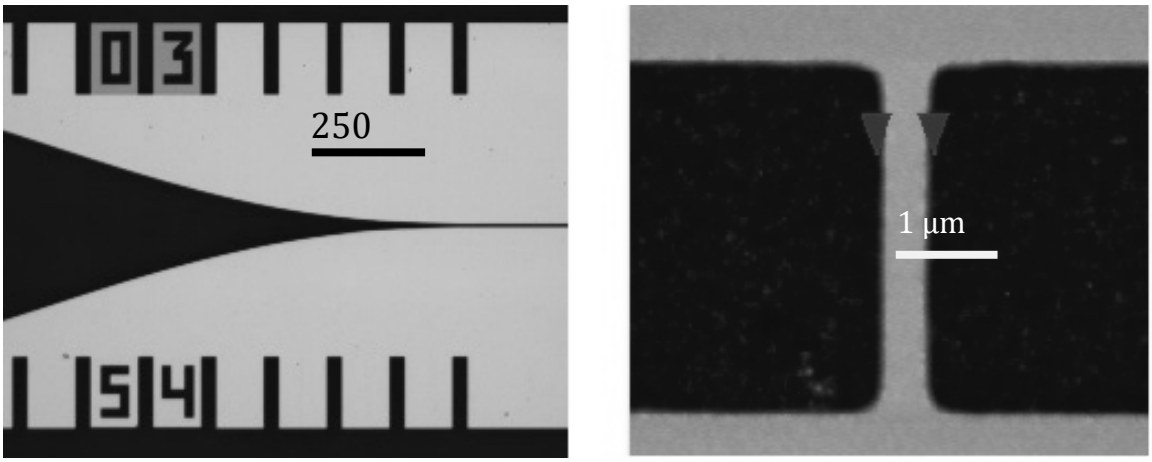


Figure 3.16: A photo of a finline and an AFM image of a NbN nanostrip switch device.

3.5. Fabrication of THz imaging devices

3.5.1. GaAs/AlGaAs heterostructure wafer

THz devices were fabricated on a 3 inch wafer with GaAs/AlGaAs hetero-structure, supplied by XPERT Semiconductors, Taiwan. The sequence of layers in the wafer is shown in Fig. 3.17. At a depth of 90 nm, a 2DEG layer is located in the semiconductor. The carrier concentration and mobility there at 4 K are 3×10^{11} cm^{-2} and 6×10^{5} $cm^{2}/(Vs)$ respectively.

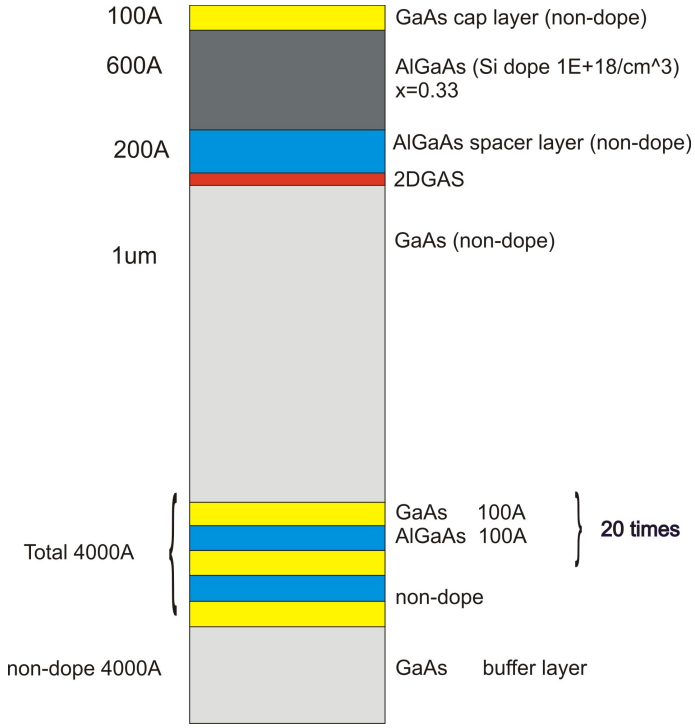


Figure 3.17. Design of wafer with GaAs/AlGaAs heterostructure.

3.5.2. Mesa pattern

First, the wafer is flushed with isopropanol and a photo resist is deposited on the wafer, spun and baked on a hotplate. A standard photo lithography procedure is then performed using a KS MJB3-UV 400 mask aligner, Fig. 3.18 a. The exposure time is 15 s at the lamp intensity of 275 W. The wafer is developed in a standard developer for the photo resist and wet etched in a H_3PO_4:H_2O_2:H_2O 4:2:94 solution, Fig. 3.19. Typical etching rate in this process is 78 nm/min. The depth of the etched material is measured using Surface profiler Stylus – Tencor AS500, Fig. 3.18 b. A standard depth of ~92.5 nm ± 7.5nm is normally achieved at this step. The resist mask is removed after that by dissolving it in acetone or another solvent during ~5 minutes.

Figure 3.18. Equipment for mesa pattern processing: Mask aligner - KS MJB3-UV 400 (a) and Surface profiler Stylus - Tencor AS500 (b).

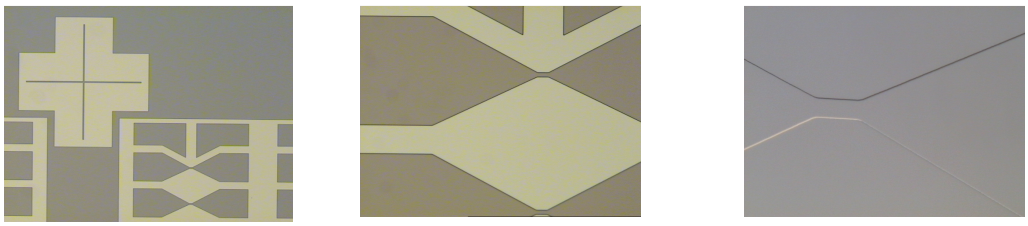


Figure 3.19. Mesa pattern defined by optical lithography; development and after etching.

3.5.3. Ohmic Ni/AuGe contacts

Figure 3.20. Ozone Cleaning System FHR UVOH 150.

Ni/AuGe contacts are patterned on the wafer by means of optical lithography, using standard exposure and development processes for two resist layers, a lift-off resist and a photo resist. Prior to metal deposition, the wafer is exposed to oxygen treatment in Ozone Cleaning System FHR UVOH 150 (Fig. 3.20) and etching in a solution of HCl acid. The Ohmic contacts are then deposited by E-gun evaporation of a 15 nm thick adhesive Ni layer and thermal evaporation of 150 nm of AuGe, followed by lift-off (Fig. 3.21). The deposition of both layers is performed in AVAC deposition system, equipped with cryo-pump, which allows keeping partial oxygen and water vapour pressure at a very low level, Fig. 3.8. Both layers are deposited in one vacuum cycle at a pressure of ~ 10^{-7} torr.

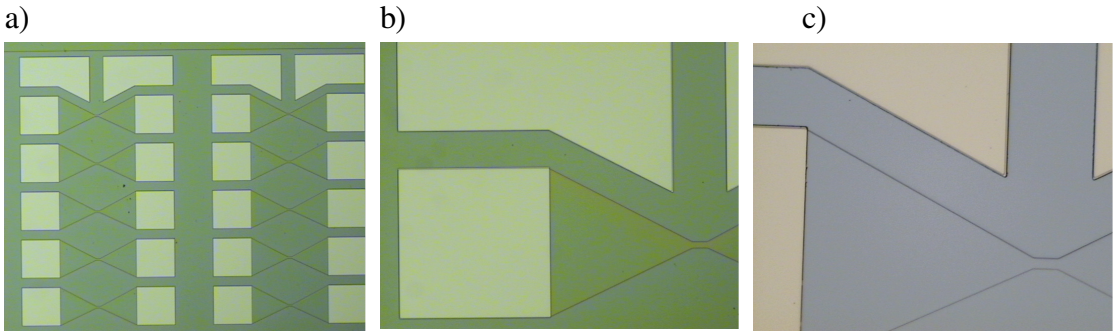


Figure 3.21. Processing of Ni/AuGe contacts. The pattern after development of the resist (a) and (b); the pattern after deposition of Ni/AuGe and lift-off (c).

After deposition of the Ni/AuGe contacts the wafer is annealed in JIPELEC JetFirst 100 at 450 C for 40 seconds.

3.5.4. Ti(Cr)/Au Metallization

The Ti(Cr)/Au metallization is patterned by optical lithography, using two resist layers. A set of marks for subsequent electron beam exposures is defined, along with the main pattern on the wafer. Edwards HPTS or Balzers System BAK600 is used for the deposition of metals. 15nm of Cr(Ti) and 120 nm of Au are deposited in this process, and then lift-off is performed using a standard developer, such as 1165. The Cr(Ti)/Au layer thickness was measured in 16 points across the wafer and averaged; a mean value of 135 nm was obtained.

3.5.5. Fine mesa pattern

Fine mesa fine pattern (Fig. 3.22) is defined using Electron-beam exposure with the mark detection, using a single layer 4% PMMA electron beam resist. The exposure is performed in JEOL JBX-5DII electron beam lithography system.

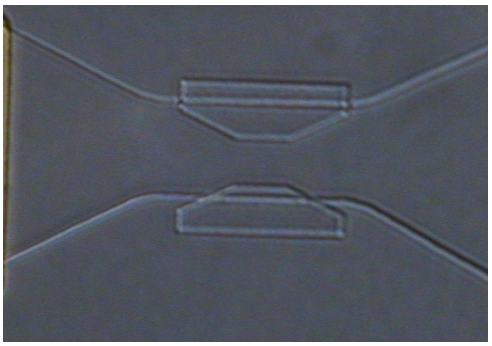


Figure 3.22. Mesa pattern defined by EBL lithography step

A standard development process is used after the exposure: Toluene: IPA 1:3 for 35 s, followed by rinsing with IPA. Then, wet etching is performed in a solution of H_3PO_4:H_2O_2:H_2O 4:2:94, see Fig. 3.22, with a typical etching rate of 1000 nm/min.

The measured etching depth was typically 92 nm after 50 sec etching. The resist mask is then removed in e.g. 1165 or acetone after processing.

3.5.6. Planarization of wafer with Spin on Glass

The process includes spinning of Spin on Glass T-12B of Honeywell Inc, exposure in JEOL JBX-5DII Electron Beam Lithography system, and development in an MF319 solution. An exceedingly high dose of 5000 $\mu C/cm^2$ is applied during this exposure in EBL, with a beam current of 10 nA and acceleration voltage of 50 kV. The resulting spin-on glass pattern is ~100 nm thick after the development, shown in Fig. 3.23.

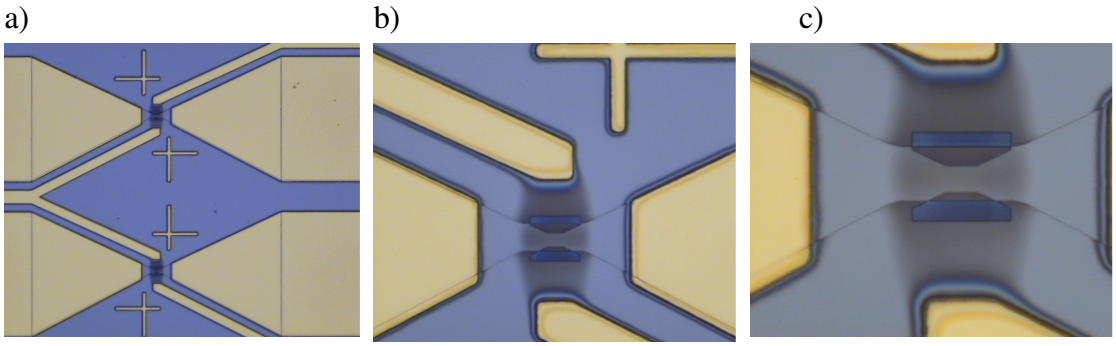


Figure 3.23. Planarization: the pattern after exposure and development of SOG with different magnification. The SOG performs planarization of the mesa profile and acts as an insulator to prevent current leak from the metal gates to 2DEG.

3.5.7. Metal gates

For patterning metal gates, standard electron beam lithography in JEOL JBX-5DII was used. A two-layer resist system, including 10% Copolymer as a lift-off resist and 50% ZEP520 as the main resist layer, was employed for this process. The exposed wafer was then developed in a solution of O-xylene, for 1 minute, and in IPA:H_2O 93:7, for 2 min 30sec. The 10 nm Cr and 100 nm Au layers were then evaporated in Edwards HPTS (Fig. 3.6) or Balzers BAK600 System (Fig. 3.9), followed by a standard lift-off process in acetone, see Fig. 3.24.

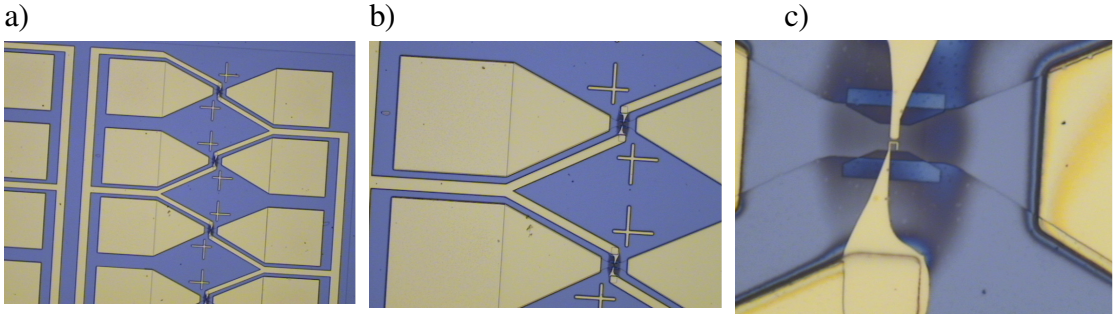


Figure 3.24. Metallic gates, after the deposition and lift-off.

Chapter 4
Thermometry and SIN tunnel junction devices

Thermometry is a cornerstone in low temperature physics as it is extremely important not only to reach the low temperature but also to be able to measure it [54, 59]. Besides basic requirements to a thermometer, such as accuracy, sensitivity and the range of temperature measured [54, 68], even matching with electronics set-up should be considered when fabricating thermometers. Although different cryogenic thermometers have already been developed [59] with high accuracy and sensitivity, matching with the external amplifier still remains an issue. The best temperature sensitivity has been achieved so far by Schmidt *et. al.* [89], where they embedded an SIN thermometer in a resonance circuit connected to a high frequency cryogenic amplifier [89]. However, this system is too complicated to be used for standard measurements at low temperatures in cryogenic systems.

The novel concept of a thermometer proposed by Kuzmin [90] offers rather high resolution in temperature and could be matched with standard room temperature readout amplifiers [90].

Thermometers can be classified into primary thermometers that return absolute temperature without calibration and secondary thermometers which need a calibration [59]. A primary thermometer is characterized by well established equation of state that relates the temperature to the measured characteristics [59]. As an example of such a thermometer, the SIN (Superconductor-Isolator-Normal metal) junction thermometer could be mentioned, to be classified as a primary on-chip thermometer.

4.1 The principle of operation

The principle of operation of the SIN junction thermometer is based on the dependence of current-voltage characteristics of SIN junctions on the temperature.

For thermometers, the voltage value V measured at a constant current corresponds to a certain value of the temperature T that can be obtained, provided the dependence V on T is known.

The theoretical dependence of voltage across an SIN junction on the temperature for various bias currents is shown in Fig. 4.1 to the left [90]. Flattering at low currents can be explained by leak currents of tunnel junctions, characterized by the ratio R_j/R that happens to be around 1000 in this example, where R_j is the subgap resistance, and R is the normal state resistance.

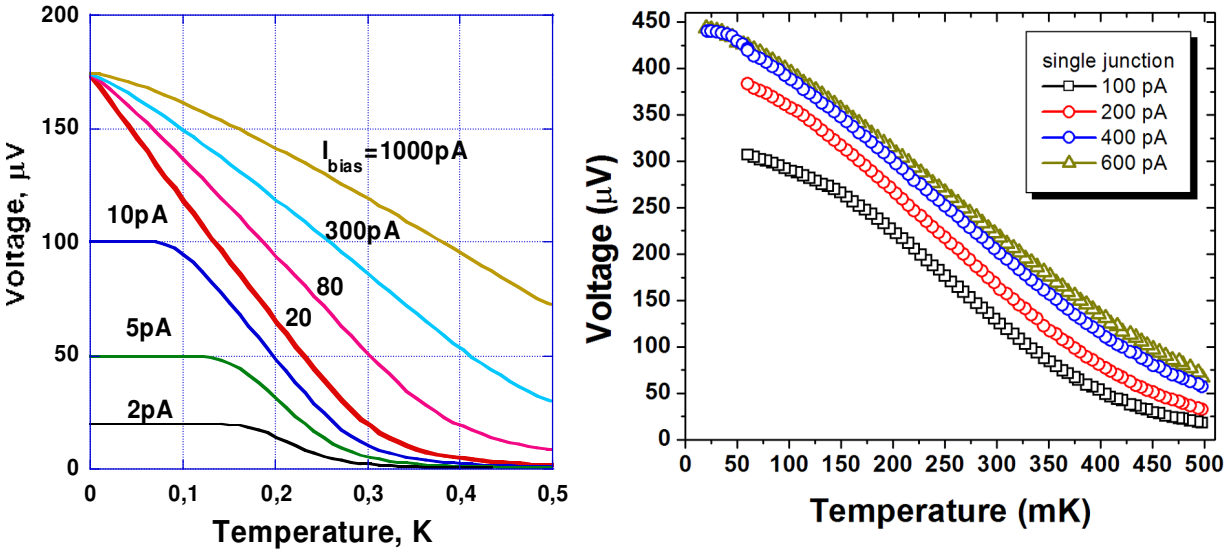


Figure 4.1. Voltage versus temperature dependence of an SIN tunnel junction [19, 21]

In Fig. 4.1 (Right), calibration of an SIN thermometer made of a single tunnel junction in Oxford Instruments Dilution Refrigerator performed by measuring *V(T)* dependence at different bias current is shown [68]. At bias current values starting from 200 pA and above, the dependence *V(T)* shows linear behavior at temperatures down to 25 mK [68]. Some disturbance was observed at a temperature around 50 mK due to swapping thermometers from a Ge one to a Ruthenium Oxide one. The necessity to change from Ge thermometer operating at temperatures down to 45 mK to the Ruthenium Oxide thermometer that operates at higher temperatures is one of main disadvantages of the thermometry method used in the Dilution Refrigerator for measuring the bath temperature in the cryostat.

The SIN thermometer proposed by Professor Leonid Kuzmin certainly does not have this disadvantage and is operating in a broad temperature range down to very low temperatures, with almost linear V on T characteristics. Measurements performed at temperatures down to 25 mK (which it is limitation of the cryogenic system used), were presented by L. Kuzmin and I. Agulo [68]. There is no evident limitation in the possible operation range of the thermometer itself, and in the future the temperature range could be potentially extended to even lower temperatures.

4.2 SIN thermometer characteristics

The SIN thermometers have a number of features which make them attractive in applications.

1. As has already been mentioned, this type of thermometers allows one to measure the temperature in the whole range of interest without switching from one thermometer to another, which is undesirable because calibration curves do not exactly coincide for different kinds of thermometers within different ranges, as e.g. when switching from a Germanium thermometer to a Ruthenium Oxide one in the Heliox AV-C cryostat or in the Dilution Refrigerator. The presented Al-based SIN thermometers are suitable for temperature measurements from 1K down to10 mK, while similar NbN-based ones can be employed at temperatures of 14 K down to 20 mk.

2. The precision of the temperature measurement is far better than that for thermometers currently used in cryostats. It has been demonstrated that the proposed thermometers allow measuring the temperature with an error of ±5 μK as standard deviation, while standard thermometers such as e.g. ITC-503 used currently by Oxford instruments in Heliox cryostat allows for resolution of about ± 1 mK.

3. Self-heating and power dissipation can be minimized due to operating in the sub-gap voltage range, where the total current through the tunnel junction and thereby power dissipation are negligible.

4. Simple readout electronics can be used for measurements in a very straightforward way unlike other kinds of on-chip thermometers, such as e.g. Coulomb-Blockade thermometers [59] that employ rather complicated readout schemes. For the thermometers presented here, an operational amplifier is implemented, along with a bias resistor, to sample and amplify the voltage across the junction. Then, standard readout electronics can be employed for further processing and displaying the measured signal in terms of temperature.

5. The simplicity of operation deserves to be emphasized. Usage of thermometer consists essentially in measuring the voltage across the junction and applying voltage-on-temperature calibration curves V(T).

6. Calibration procedure is rather simple. For the calibration curve, the voltage across the tunnel junction is measured, and the temperature is derived from the calibration curve of another thermometer that had already been calibrated and is used as a reference one.

7. In essence, the SIN thermometer can be classified as a primary one. Due to this fundamental property, preliminary calibration could be avoided, provided another two measurements with bias resistors of lower resistance value be performed in order to obtain the normal resistance R and the superconductive gap Δ. Namely, voltage values at a temperature above T_c and at lowest available temperature should be measured. After that, the voltage versus temperature curve will be produced. No preliminary calibration is needed in that case, which is an indication of the primary nature of the SIN thermometer.

8. The SIN thermometer can be protected from external noise and interferences by on-chip resistors deposited along with the SIN junctions during the process of fabrication and bias resistors (typically in the GΩ range) placed on a cold stage of the cryostat. Additional filters can be utilized for enhanced protection. However, using several SIN junctions in series as a sensing element of thermometer makes it almost insensitive for external noises and interferences. Internal noise of SIN junctions is proportional to the square root of the quantity of junctions, while the useful signal increases linearly with the number of junction. Using more than 30 junctions in series makes external noises and interferences as well as the contribution of the input noise of the amplifier negligible in comparison with the useful signal. All measurements can be done using proper 4-point measurement scheme, where these resistors are excluded from the values measured and do not deteriorate the accuracy of measurements.

9. SIN junctions are sensitive to the magnetic field as the magnetic field through the superconductive electrode should not exceed the critical value (to maintain the superconducting state). Using Nb shields, this problem can be alleviated. Provided proper shielding, the system is less sensitive to the magnetic field below threshold value. External magnetic field can be additionally attenuated by a ferromagnetic screen, in which case the influence of the magnetic field on the system will be negligible even if it exceeds the threshold value.

10. The sensing element is deposited on chip along with other structures; also, it can be made very small and thereby SIN junctions can probe temperature locally (on chip) and even detect temperature gradients across the chip.

4.3 SIN Thermometer Model

The SIN array concept is based on sampling the total correlated response of N individual junctions to a temperature change δT_{ph} [90]. Typical IV curves of a single SIN tunnel junction for different temperatures are shown in Fig. 4.2 [90].

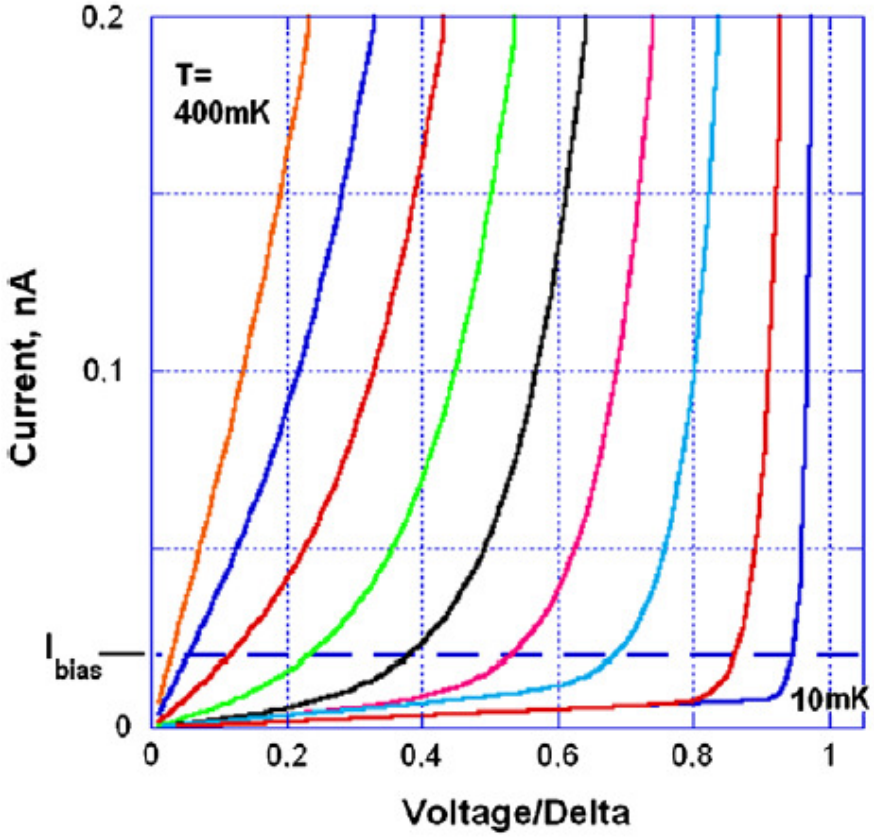


Figure 4.2. IV-curves of an Al-based SIN tunnel junction versus temperature:
T = 10, 50, 100, 150, 200, 250, 300, 350, 400 mK.
The dashed line represents the bias current I_{bias} = 20 pA.

The approach of the series array, similar to the one used for current-biased CEB arrays [69], can be used for thermometry [90]. Indeed, the noise of different junctions is not correlated and the total noise voltage of N junctions in series is therefore proportional to the square root of that number, √N, while the total correlated voltage response sampled across N junctions increases by the factor of N, compared to the response of each single junction. Finally, the total effective noise of an array normalized to the number of junctions in the array will be inversely proportional to the square root of the junctions, √N.

The heat balance equation similar to the one for single bolometer [69] is used in [90] for the analysis of the thermometer based on SIN array:

$$\Sigma\lambda\left(T_e^5 - T_{ph}^5\right) + P_{SIN}(V, T_e, T_S) + C_\lambda \frac{dT}{dt} = \frac{P_0}{N} + \frac{V^2}{R_S} \tag{4.1}$$

where Σ is the material constant, Λ - the absorber volume, T_e and T_{ph} are electron and phonon temperatures of the normal metal; P_{SIN} is the cooling power of the SIN tunnel junction; C_λ is the specific heat capacity of the normal metal; P_0 is a background RF power, while R_S is leak resistance of the SIN junction.

The left-hand side of the Eq. (4.1) can be presented as a sum of a time independent term,

$$\Sigma\Lambda(T_{e0}^5 - T_{ph0}^5) + P_{SIN}(V, T_{e0}, T_{ph0}) = \frac{P_0}{N} + \frac{V^2}{R_S}$$

and a time dependent term,

$$\left(5\Sigma\Lambda T_e^4 + \left(\frac{\partial P_{SIN}}{\partial T} - \frac{\partial P_{SIN}}{\partial V}\frac{\partial I}{\partial T}\Big/\frac{\partial I}{\partial V}\right) + i\omega C_\Lambda\right)\delta T_e = \left(5\Sigma\Lambda T_{ph}^4\right)\delta T_{ph}. \tag{4.2}$$

Here,

$$G_{e-ph} = 5\Sigma\Lambda T_e^4, \tag{4.3}$$

is normal metal electron-phonon thermal conductance that depends on volume of the normal metal electrode.

Higher electron-phonon conductance can be provided by larger volume of the normal metal, and the condition $\delta T_e = \delta T_{ph}$ can be achieved, which means better accuracy of temperature measurements. Besides, larger volume of normal metal allows decreasing electron-phonon noise of the thermometer.

Thermal conductance of the SIN junction

$$G_{SIN} = \frac{\partial P_{SIN}}{\partial T} - \frac{\partial P_{SIN}}{\partial V}\left(\frac{\partial I}{\partial T}\Big/\frac{\partial I}{\partial V}\right) \tag{4.4}$$

provides some electron cooling and can be minimized in the subgap region by making the tunnel junctions more high-ohmic.

The total thermal conductance is equal to

$$G_{tot} = G_{e-ph} + G_{SIN} + i\omega C_{\Lambda} \tag{4.5}$$

In the current-biased mode, the responsivity S_V of the thermometer is expressed by

$$S_V = \frac{\delta V_\omega}{\delta T_\omega} \tag{4.6}$$

Typical voltage on temperature dependence at different currents is shown in Fig. 4.1.

The responsivity of the Cold-Electron bolometer based on SIN junctons S_{VP}

$$S_{VP} = \frac{\delta V_\omega}{\delta P_\omega} = \frac{\delta V_\omega}{\delta T_\omega}\frac{\delta T_\omega}{\delta P_\omega} \tag{4.7}$$

consists of the thermometer responsivity S_V and the temperature response to the power, which means that results for bolometers can be used for thermometers, considering $\delta P/\delta T$.

The time constant of the device response to the temperature change

$$\tau = C_\Lambda / \left(G_{e-ph} + G_{SIN}\right) \approx C_\Lambda / G_{e-ph} \tag{4.8}$$

can be estimated as $\tau \cong 10\mu s$ at 100 mK and 0.5 μs at 300 mK.

4.4 Experiments on Arrays of 100 Al-Al_20_3-Cu SIN tunnel junctions for thermometry application

In this section, SIN tunnel junction thermometers made of arrays containing 4 to 100 Al-Al_20_3-Cu SIN tunnel junctions fabricated with Direct-Write Trilayer Technology, are presented. This technology is based on *in-situ* evaporation of the superconducting electrode followed by its oxidation and the normal electrode deposition as a first step and creating a normal-metal absorber as a second one (see details in Chapter 3). This approach [25] is especially advantageous for thermometry applications as it allows implementing large area tunnel junctions and big normal-metal electrodes, which is not feasible using the standard shadow evaporation technique.

Few thermometers with SIN junctions fabricated at Chalmers were used for temperature measurement inside a cryostat [68]. For example, the samples presented in [68] were used for temperature stability measurements in Heliox cryogen-free cryostat manufactured by the company Oxford Instruments. High accuracy, fast response and wide temperature range of SIN thermometers make them attractive for future employment [59], e.g. for the temperature control inside cryostats.

4.4.1. Readout electronics and design considerations

For characterization of SIN devices at low temperatures, a Heliox AC-V cryostat was used, which is a "cryo-free" system developed and fabricated by Oxford Instruments (Fig. 4.3). This is a pulsed tube cooler, able to cool down to ~280 mK without consuming any cryogen liquid, due to liquid He recycling system. Its cooling power is above 100 μW at 350 mK and the hold time is about 4 - 5 hours. After ~ 1 hour recycling of ^{3}He, the system can be cooled down again.

The current-voltage characteristics of the SIN devices presented here were measured using current biasing scheme. In that case, current through a device under test is controlled using a current source, and voltage across the device is measured using room temperature amplifiers. Thus, the voltage across the device under test is considered as a function of applied current through the device. In the generic scheme in Fig. 4.4, current biasing of the SIN devices is implemented using a voltage source with a bias resistance R_{bias} in series with the device under test. The voltage across the device is then sampled, amplified and read out (Fig. 4.4).

Figure 4.3. HELIOX "Cryogen-free" pulsed tube cryostat

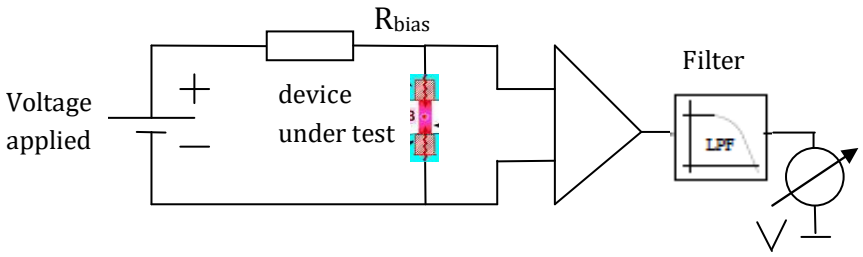


Figure 4.4. Current biasing circuit topology [55]

The SIN devices presented in this chapter were measured in the current-biased mode using a read out amplifier employing FET-based amplifier OPA 111 and operating at room temperature. It has noise voltage of 7 nV/Hz, and bias resistors with resistance values between 200 kOhm and 20 GOhm were used. This option allows adjusting the output impedance of the current source to a value far above the impedance of the device to be tested, in order to maintain the current bias mode. The circuit schematic diagram of the room-temperature readout amplifier block is shown Fig. 4.5.

In the circuit in Fig. 4.5, bias voltage V_b is applied to the amplifier box that includes bias resistors connected in series with the SIN device under test. The box incorporates amplifiers sampling the voltage across the device and current through it independently and has thus two outputs representing the current and the voltage.

The operation of the cryostat is managed by control units located on a measurements rack along with temperature readout electronics, room temperature amplifiers, external sweep generators and other readout electronics. The circuit to be tested is either biased with an external sweep generator or controlled digitally by LabView, with sets current to values determined by LabView and experimental setup parameters entered through GUI interface. The bias current is normally swept in a certain range, and both current and voltage values are sampled and logged by LabView.

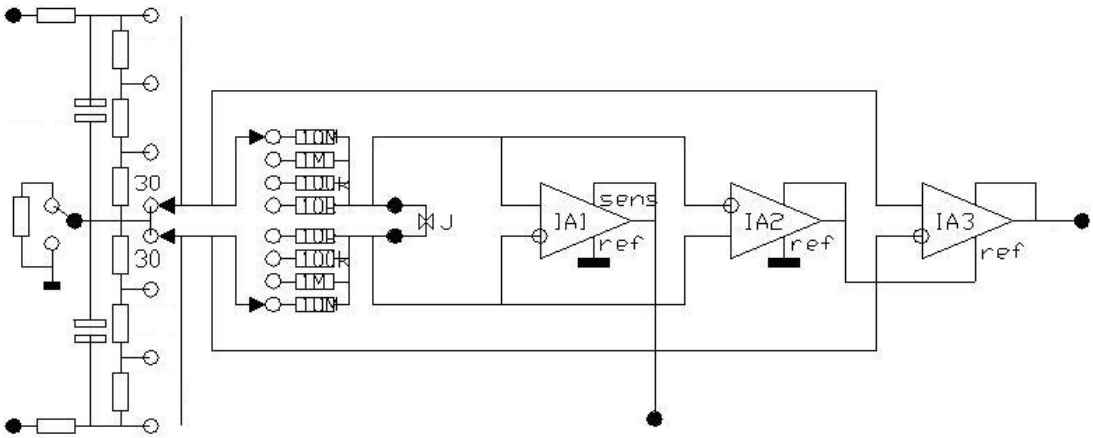


Figure 4.5. Circuit schematic of the amplifier for measurements in current-biased mode

SIN tunnel junctions (Fig. 4.6) and arrays of 4, 10, 30, and 100 junctions of 2×2 and 4×4 μm^2 have been fabricated using Trilayer technology and tested at temperatures between 300 mK and ~1 K [Paper II]. It had already been shown [68] that for an array of 10 tunnel junctions in series, much better temperature sensitivity can be achieved than for a single SIN junction. In that work, an array of 10 SIN junctions fabricated with shadow-evaporation technique was presented, and experimental results on its performance evaluation as a thermometer were reported. The resolution in temperature of ±30 μK was demonstrated, which is mainly determined by the noise of the room-temperature amplifier in the read-out system. For an array of 10 junctions, it was difficult to evaluate the noise of the junctions because of the noise of the amplifier that dominates in the total noise measured. Increasing the number of tunnel junctions in an array makes it possible to distinguish the noise of the junctions that can therefore be measured once the total noise exceeds the noise of the amplifiers.

It had also been shown [68, 90] that the total voltage drop across the array is directly proportional to the number of junctions, whereas the total voltage noise is proportional to the square root of the number of junctions. Therefore, increasing of number of junction in series allows achieving even higher sensitivity, which was confirmed experimentally in [Paper II] by measuring voltage response of samples containing arrays of different numbers of SIN junctions up to 100. Noise of an array of 100 junctions can easily be distinguished from the noise of the read-out amplifiers, which allows estimating the temperature sensitivity of the thermometer.

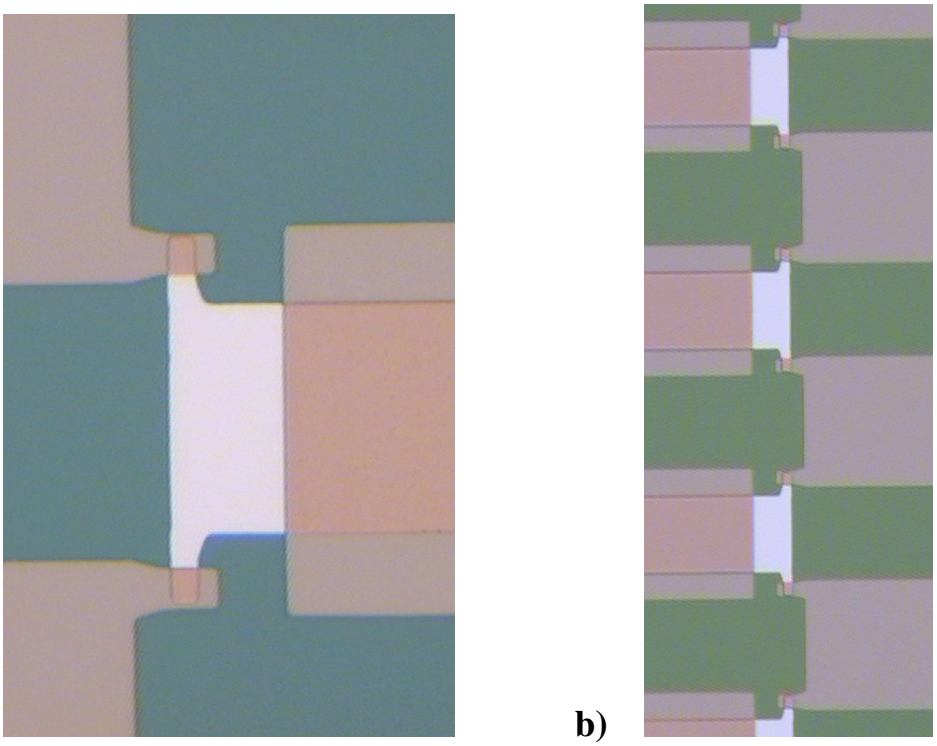


Figure 4.6. Optical images of SIN junctions: a) two 4×4 μm^2 junctions;
b) a fragment of an array of 30 junctions.

4.4.2. Experimental results

Measurements performed at 300 mK showed high quality of fabricated tunnel junctions, low leakage currents, and R_d/R_n ratio of 500 has been achieved at that temperature. An IV-curve and dV/dI of a single junction are shown in Fig. 4.7.

Optical images of some junctions in the arrays are shown in Fig. 4.6. The junctions were characterized as temperature sensors, and voltage versus temperature dependence for a single junction is shown in Fig. 4.8.; the IV-curve for a 100-array is shown in Fig. 4.9. Voltage versus temperature dependences for arrays (Fig 4.10) of 30 and 100 junctions have also been measured, and dV/dT of 52 μV/mK has been achieved for 100 junctions of 2×2 μm^2 in series (Fig. 4.10b), that is 0.52 μV/mK for each junction. The dV/dT value reported for 4×4 μm^2 tunnel junctions is 41 μV/mK (Fig. 4.10a), due to higher leak currents for larger junctions.

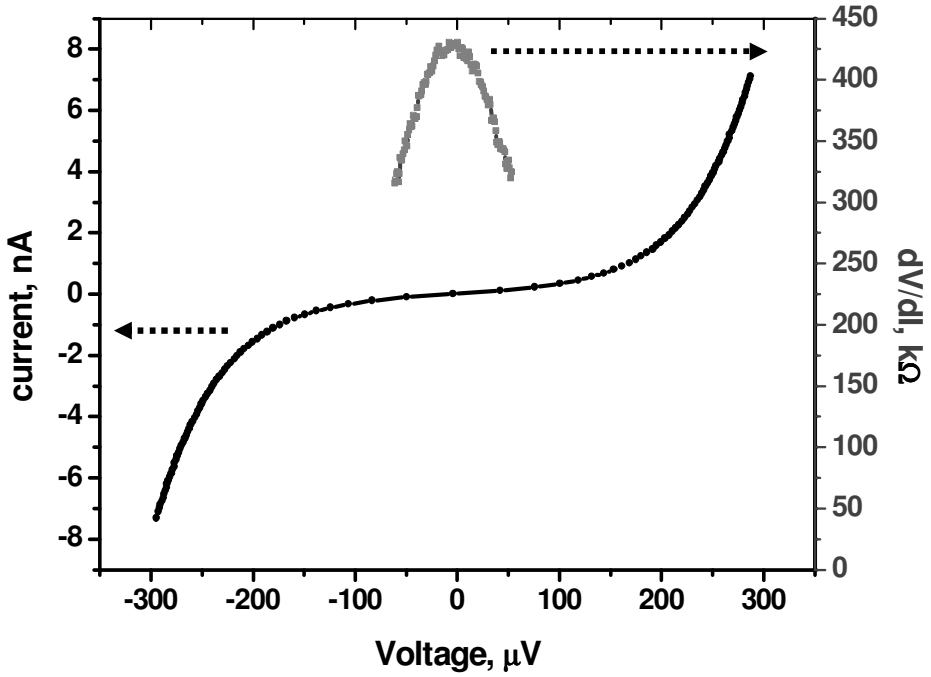


Figure 4.7. IV curves and dV/dI of a single tunnel junction at 300 mK, Trilayer Technology

Noise measurements yielded a value of 0.285 μV for the voltage noise of the 100-junctions array, which corresponds to the temperature standard deviation of ±5 μK, considering the value of 0.52 μV/mK for the thermometer responsivity of the array.

Thus, for an array of 100 junctions, a temperature resolution of ±5 μK has been achieved which is much better than previously reported result of ±30 μK for this type of thermometer [68] and for other types of cryogenic thermometer, e.g. Coulomb Blockage Thermometer [59], while the sensitivity of the original thermometer used in Oxford Instruments cryostats is ±2 mK [91].

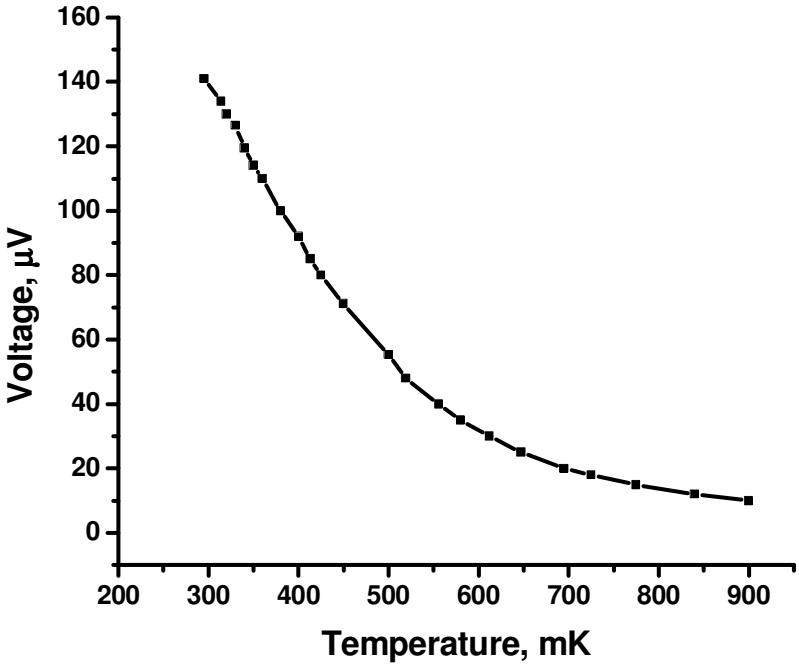


Figure 4.8. Voltage on temperature dependence of a single tunnel junction, Trilayer.

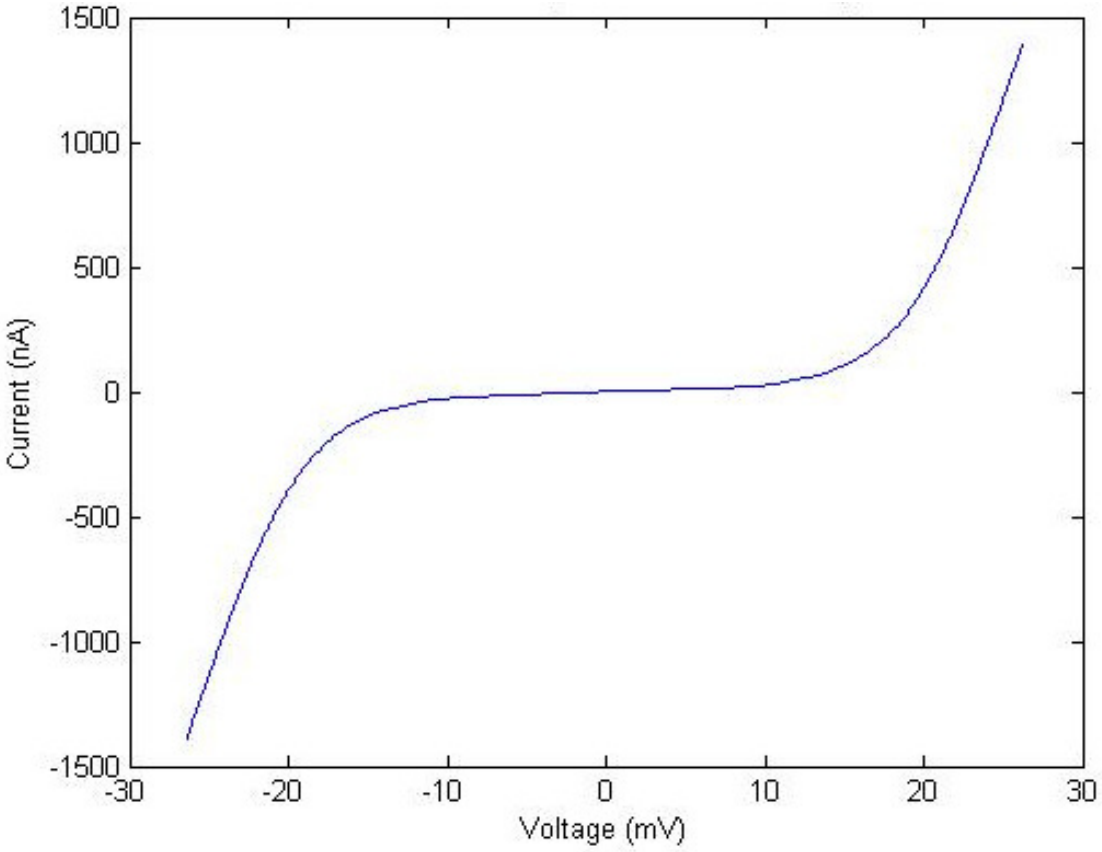


Figure 4.9. IV curve of an array of 100 SIN junctions at 305 μK.

The experimental value for the temperature resolution of an array versus the number of junctions is shown in Fig. 4.11. A comparison with other types of cryogenic thermometers is shown in Table 4.1. Increasing the number of junctions in the array will allow achieving even higher sensitivity [90], which enables for use of SIN tunnel junctions fabricated in Direct-Write technology for thermometry application.

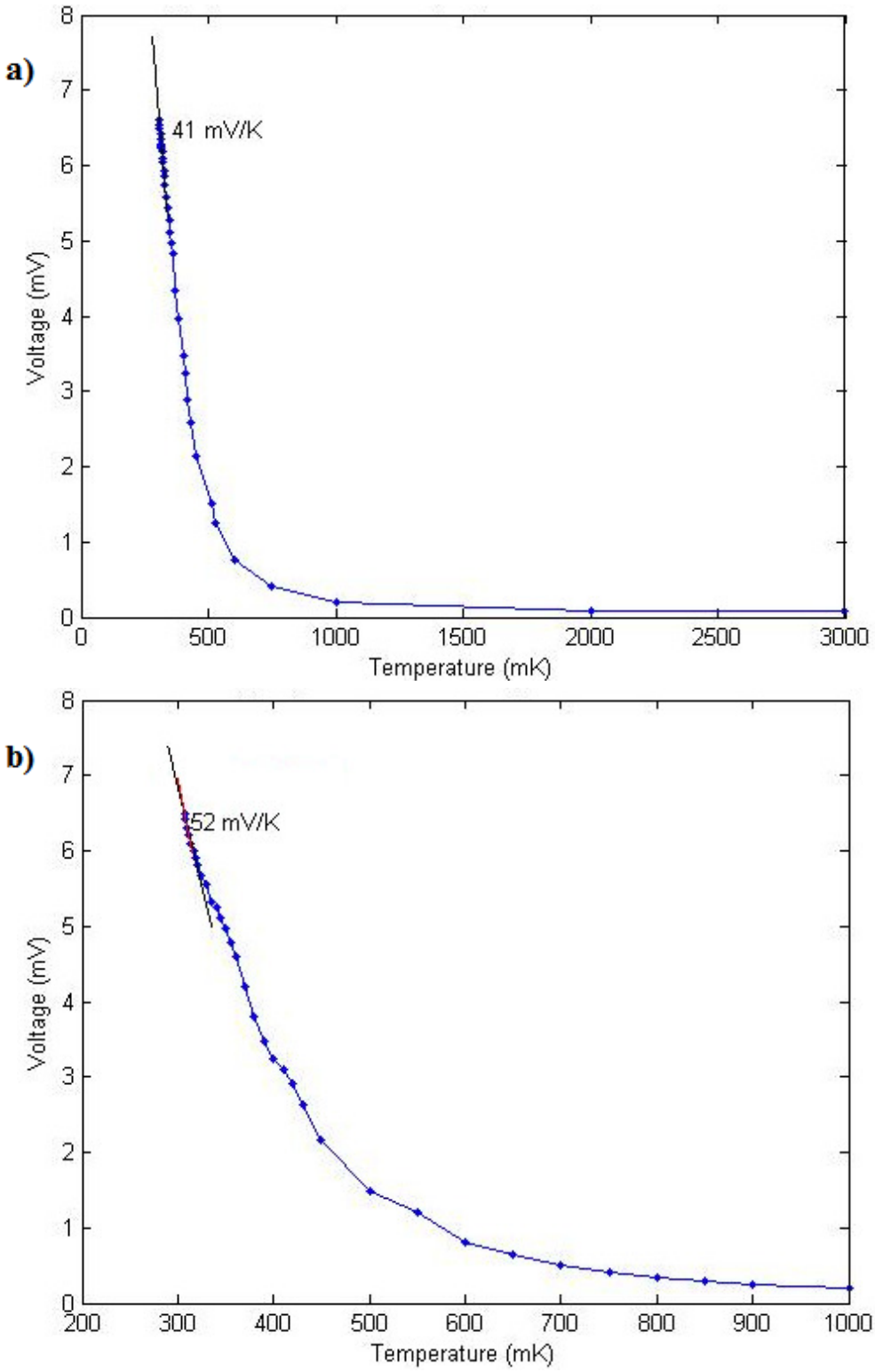
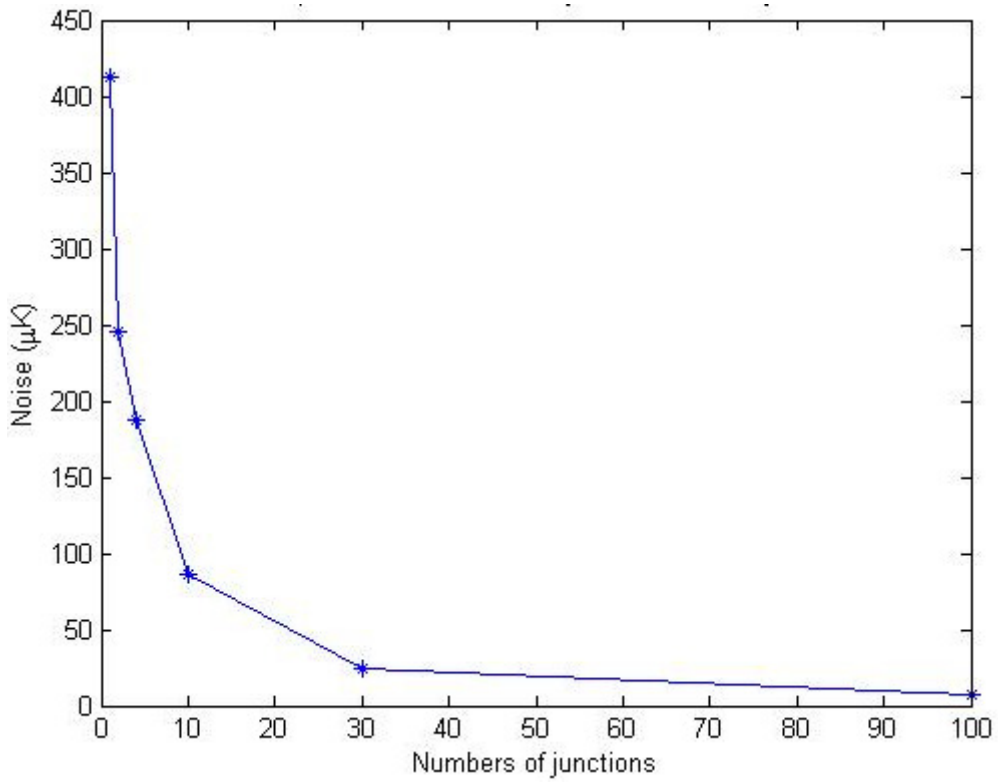


Figure 4.10. Voltage on temperature dependence for 100 junctions of area 4×4 and 2×2 μm^2

a)



b)

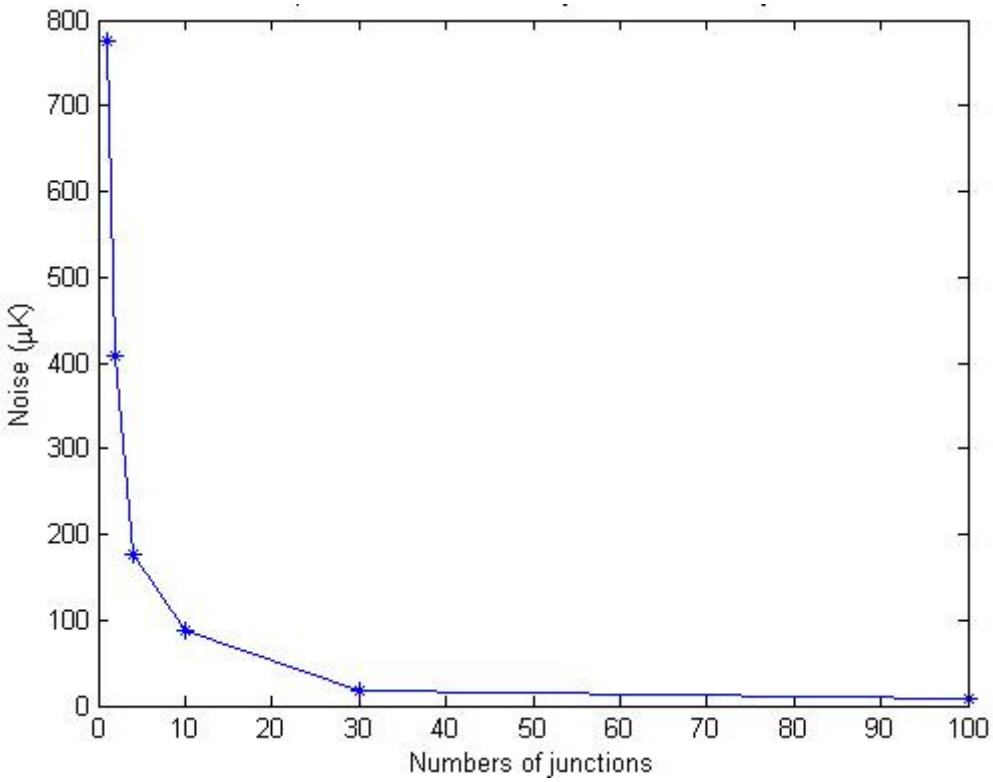


Figure 4.11. Temperature resolution versus number of junctions for arrays of up to 100 junctions of 2×2 μm^2 (a) and 4×4 μm^2 (b)

Temperature Sensor	Affiliation	Sensitivity
RuO	Oxford Instruments	2 mK
Coulomb Blockade Thermometer	Helsinki University of Technology, Chalmers	1 mK
Array of 10 SIN junctions	Chalmers	30 μK
Array of 100 SIN junctions	Chalmers	5 μK

Table 4.1. The sensitivity of different types of cryogenic thermometers

Though both the dynamic resistance and normal resistance are spread over the wafer, it is still possible to use arrays of SIN tunnel junctions for thermometry application. The total responsivity of such an array is determined by the voltage drop across the whole array and its total dynamic resistance. As mentioned above, a total voltage response of such an array at fixed biasing current is directly proportional to the number of junctions, whereas the noise of the junctions is proportional to the square root of that number [68, 90]. By increasing the number of junctions in the array, improvement of the temperature sensitivity of the array is possible, independent of the quality of each single junction in the array. This was confirmed experimentally for an array of 100 Al-based tunnel junctions [Paper II], where the dV/dI of 52 μV/mK was reported for 100 junctions in series, or 0.52 μV/mK for each single junction, which is very close to the theoretical value of 0.5 μV/mK for an SIN junction.

4.5 Conclusions

In this chapter, the concept of the on-chip SIN thermometer is introduced, and its model is considered, with focus on arrays of SIN tunnel junctions operating in current-biased mode. On-chip thermometers made of arrays of up to 100 SIN tunnel junctions fabricated using Direct-Write Trilayer process are presented, including measurement procedure and experimental results. A temperature resolution of ±5 μK is reported here, which is much better than previously reported results for similar types of on-chip thermometers.

Chapter 5
Finline-Integrated CEB fabricated with Direct-Write Trilayer technology

A possible implementation of CEB detector is to deposit the bolometer across a unilateral finline on a planar substrate [56, 87]. The CEB and the planar circuitry including the finline can be fabricated on the same substrate and in one fabrication cycle [Paper V, 87].

A finline taper is essentially a slotline with gradually changing slot width, used often for impedance matching at the interface between the chip and the waveguide. An example finline layout with possible readout electronics is shown in Fig. 5.1.

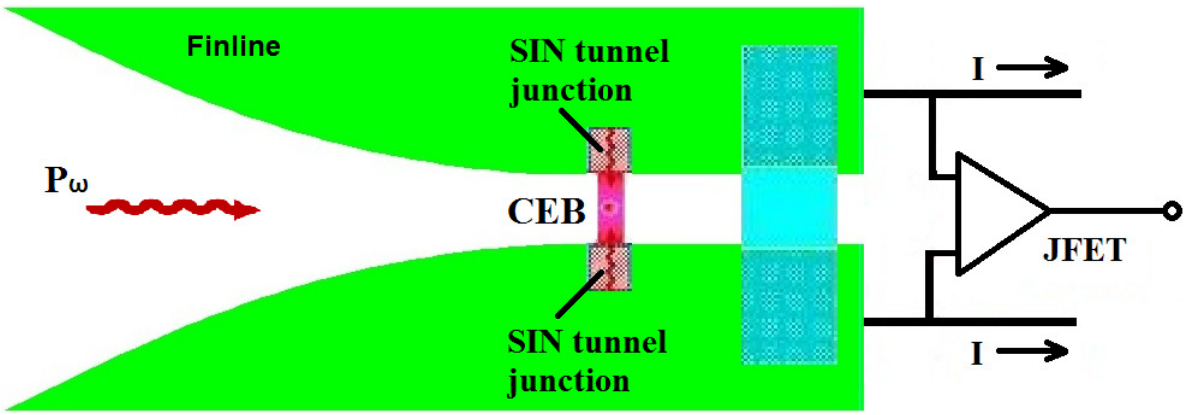


Figure 5.1. Cold-Electron Bolometer coupled to a finline with JFET readout [66, 87].

For use in conjunction with bolometric devices, two different types of finlines can be distinguished, namely unilateral and antipodal finlines. In a unilateral finline, both electrodes are located in the same plane. The electrodes of an antipodal finline are situated in different planes and overlap each other at some point, with an insulating layer in between. During the fabrication, several layers of different materials are to be deposited and patterned to form a planar 3-layer structure, including an insulating oxide layer, while in the unilateral finline both electrodes are made of the same material and are often deposited and patterned as one single layer.

5.1. Concept of CEB integrated in a 97-GHz finline

In this section, the design of a CEB with SIN tunnel junctions is presented, intended for coupling the incident signal through a 97–GHz waveguide into a finline (Fig. 5.1 and 5.4). The profile of the finline was designed using a taper optimization technique, implemented in software developed by our British collaborators at University of Oxford [5, 92].

The devices were fabricated using the Trilayer Direct-Write technology proposed by L. Kuzmin and developed by the author; described in detail in Chapter 3 of this thesis [Paper II]. This approach is particularly advantageous for low-frequency applications as it allows fabricating tunnel junctions with large area, which scarcely can be realized using traditional shadow evaporation technique. That method is more suitable for high-frequency applications (above 350 GHz) due to smaller size of tunnel junctions fabricated using traditional shadow evaporation.

Alternatively, the normal-metal absorber can be produced prior to the tunnel junctions and the superconducting electrodes, which is now feasible using Ti-based technology and Advanced Shadow Evaporation, developed later and presented in Chapters 5 and 6 of this thesis.

In the CEB-finline integrated circuit shown in Fig. 5.1, a CEB device made of two SIN tunnel junctions and a normal metal absorber is deposited across a unilateral finline. In that configuration, a room temperature JFET amplifier is used for current bias readout, i.e. current is applied using a current source and the voltage across the CEB device is measured using a room-temperature JFET amplifier.

5.2. Analysis and simulation of the CEB-finline integrated circuit

The electromagnetic performance of the CEB-finline integrated circuit has been analyzed using RF / microwave software packages Ansoft Designer and HFSS. An equivalent circuit for the CEB-finline was simulated including an ideal transmission line representing the finline in Ansoft Designer (Fig. 5.2). In this model, the incoming signal propagates through a transmission line and is coupled to the CEB represented by an RLC tank circuit. The other end of the transmission line is shorted at a distance from the CEB that was set initially to λ/4 and then parameterized in simulation, in order to achieve the best matching between the terminals, taking into account the characteristic impedance of the transmission line and the input impedance of the RLC circuit [Paper V].

Then, a finline-integrated CEB was simulated using HFSS, with slot widths between 2 and 10 microns, with silicon and quartz as the materials of the substrate. The CEB was represented by a lumped equivalent RLC circuit. Simulation performed in Ansoft Designer and HFSS showed that the best RF matching between the finline and the CEB circuit is achieved with tunnel junctions that are 1.5×1.5 to 2×2 microns large, which implies the capacitance values of 100-200 fF. The optimum values for the inductance and the resistance of a CEB on a Si substrate were obtained as 2.4 pH and 45 Ω respectively. For a quartz substrate, the appropriate values are 2.6 pH and 70 Ω. Simulations also showed that positioning a back short at a distance of 225 - 250 µm from the CEB, with a slot width of 3 to 5 µm, yields a reflection coefficient of about -20 dB for Si, while the result is almost insensitive to process variations. The reflection S_{11} for Si and for quartz are shown in Fig. 5.3, (Left) and (Right), respectively. Values down to -18 dB were obtained for a CEB on a quartz substrate when positioning a back short at a distance of 500 µm from the CEB (Fig. 5.3, right).

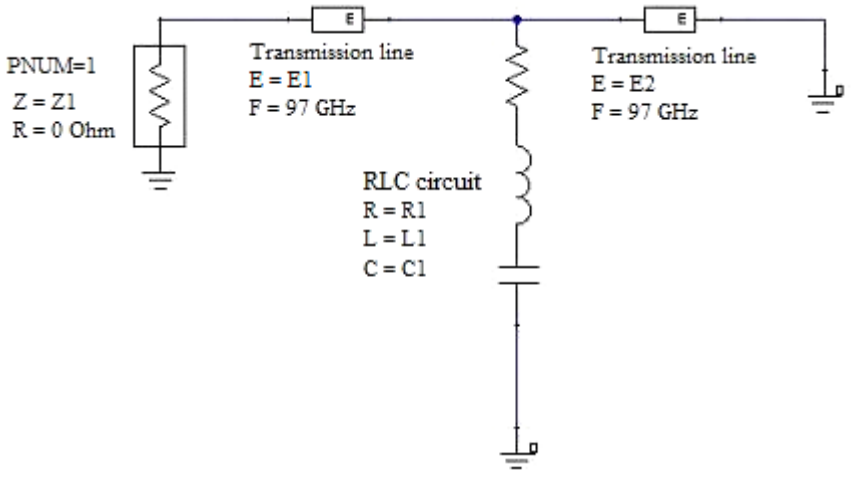


Figure 5.2. Equivalent circuit for finline-CEB for simulation in Ansoft Designer [74, 87]

Based on these results, a CEB-finline integrated circuit was fabricated on a silicon substrate, while quartz remains an option as the material for the substrate. For a 5 µm long absorber with 0.5 µm width and thickness of 50 nm, the inductance was estimated as 2.5 pH. Making a strip of Cr/Cu bilayer, the series resistance value of 45 Ω is obtained for a strip of that size. Hence, a 50 nm thick and 5 µm × 0.5 µm large absorber made of Cr/Cu bilayer, deposited in conjunction with two 4 μm^2 large tunnel junctions is a reasonable choice for RF matching.

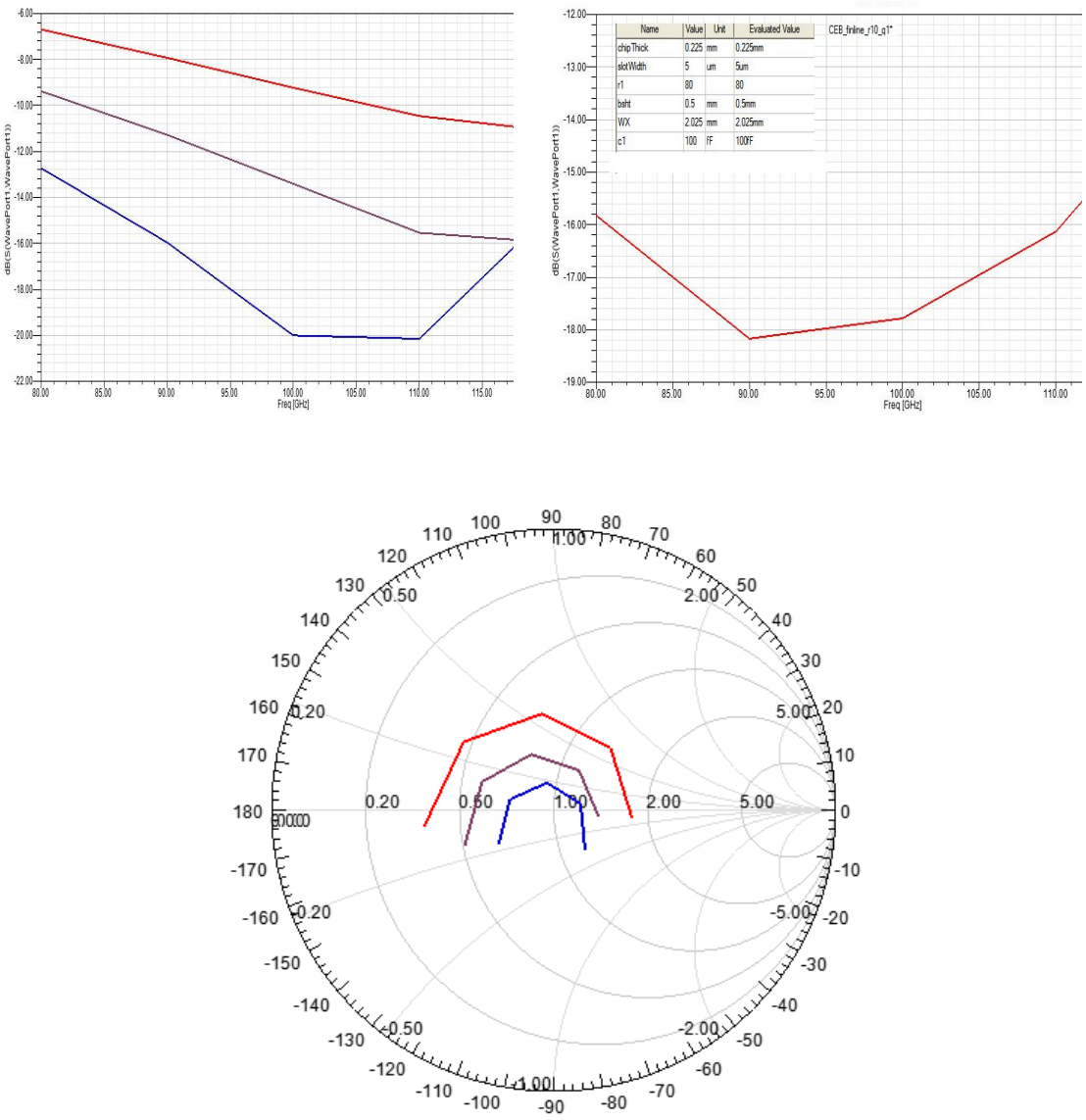


Figure 5.3. Reflection at the input of the CEB-finline on Si substrate (left) and quartz (right). Simulation performed using HFSS. The distance to the back short varied between 200 and 250 µm for Si and 350 to 500 µm for quartz. (Bottom) RF matching for Si substrate in Smith Chart [74, 87, Paper V].

5.3. Fabrication of finline-CEB integrated circuits using Direct-Write Trilayer technology

The CEB-finline samples presented here were fabricated by means of e-beam lithography in direct-write mode, with the SIN junctions formed using the Trilayer technology proposed by L. Kuzmin and developed by E. Otto, the author of this thesis; described in detail in Chapter 3 [87], [Papers I, II].

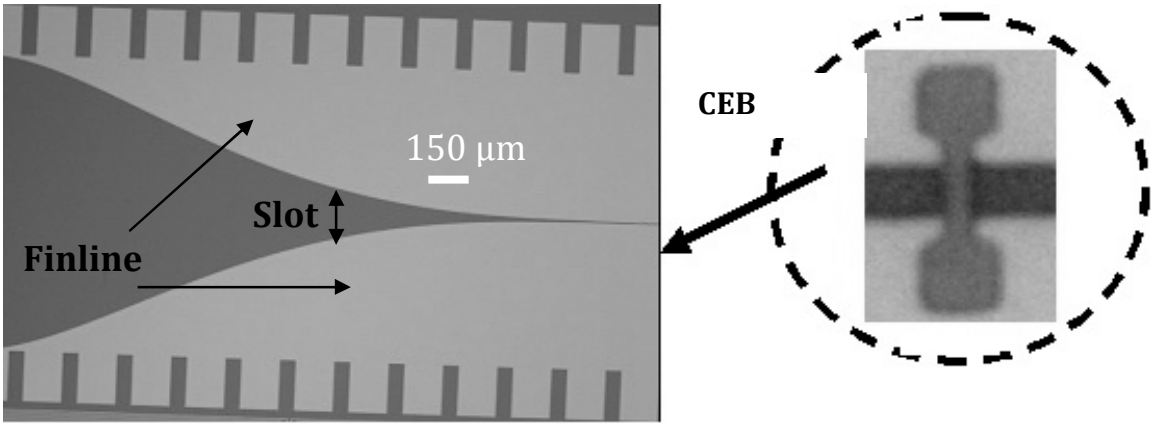


Figure 5.4 [74] Optical image of a finline with a CEB device across the slot (inset);

First, 100 nm thick gold contact pads were created using e-beam exposure and thermal evaporation. Then, ~45 nm thick finlines and the Cold-Electron Bolometer structures were fabricated using the trilayer process described in Chapter 3 [Paper II]. This is done by depositing Al as the bottom layer with subsequent oxidation in chamber for creating tunnel junctions, followed by depositing a layer of Cu and then gold on the top of it for passivation. Then, a normal absorber was patterned using e-beam lithography and deposited. As the last step, the Cu-Au layer was removed from the top of the trilayer structure, by means of ion-beam etching. A photo of a fabricated CEB integrated in a finline is shown in Fig. 5.4 [74].

5.4. The experiment setup and readout electronics

For evaluation of the performance of CEB devices at low temperatures, Heliox AC-V cryostat was used, fabricated by Oxford Instruments (Fig. 4.3).

The DC current-voltage characteristics of the CEB devices have been measured using current biasing scheme, which means that current through a device is controlled, while voltage across the device is measured. In these experiments, current biasing of CEB devices was implemented using a voltage source with a bias resistance R_{bias} in series with the CEB device according to the topology shown in Fig. 4.4. The voltage across the device is then measured and logged [74].

The specific schematic of the room-temperature readout amplifier used for testing CEB devices in this thesis is shown in Fig. 5.5. It operates in the fixed current bias mode, based on a differential bias circuit topology with room temperature amplifiers including AD743 BiFET input gain stage with input voltage noise of around 4nV/√Hz. The bias resistance is selected from values in a range between 100 kΩ and 10 GΩ, which allows adjusting the output impedance of the current source to a value far above the impedance of the device to be tested, in order to maintain the current bias mode. Current-voltage characteristics of CEB devices were measured in this way for bath temperatures between 286 mK and 356 mK [74].

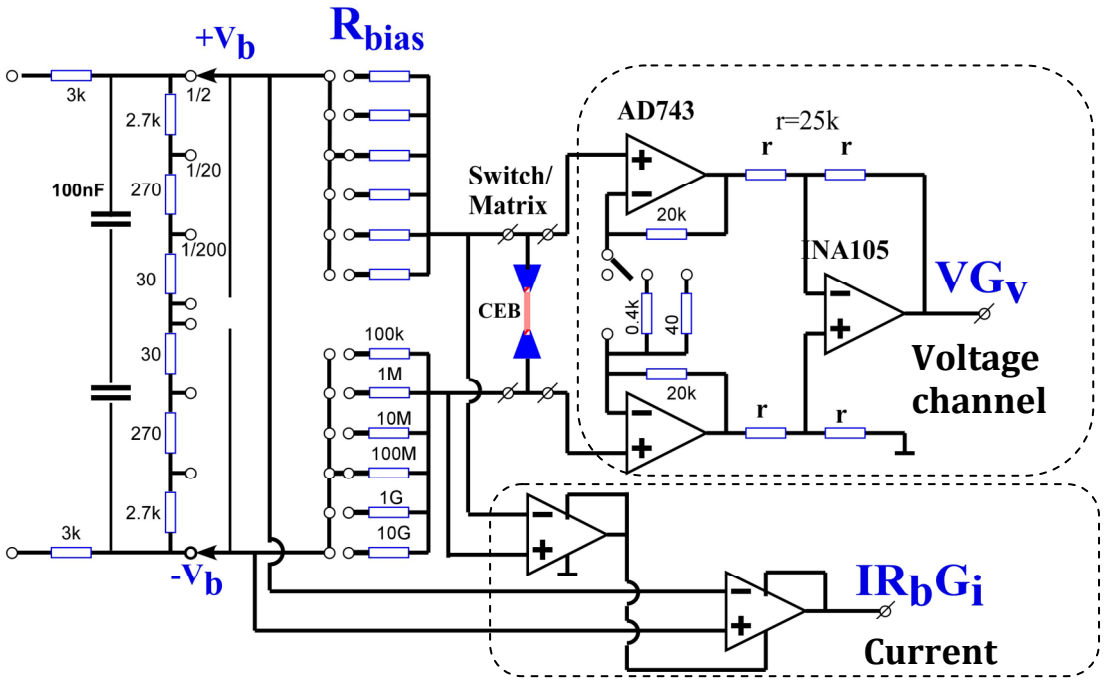


Figure 5.5. Circuit schematic of the room-temperature amplifier used for IV-curves measurements in current-biased mode [53, 74].

The circuit in Fig. 5.5 for measuring IV characteristics operates as follows. The bias voltage V_b is applied to the amplifier box, containing bias resistors that are connected to the CEB device. The amplifier box includes also two amplifier channels and has therefore two outputs: for the current through the device and the voltage across it.

In reality, both channels operate as voltage amplifiers. The voltage channel samples the voltage across the CEB device, amplifies it and reads out. On the contrary, the current channel samples and measures the voltage applied to the bias resistors connected in series with the CEB device. Both amplifier outputs are then connected to a computer, and the output data is logged using data acquisition software such as LabView. The voltage measured at the output of the current channel is proportional to the current through the bolometer I_{bolo} and the bias resistance value R_{bias} that is typically selected as 20 or 200 MΩ for SIN junctions in kΩ range. In order to obtain

the current through CEB, the voltage sampled at the current channel output and logged by LabView is then divided by R_{bias} and the channel gain. The voltage across the bolometer is obtained by sampling the voltage at the output of the voltage channel and dividing this value by the voltage gain of the channel, typically 1000 [74].

5.5. CEB testing using external RF power source

Preliminary testing of CEB devices fabricated with Direct Write Trilayer technology was carried out at Chalmers University of Technology using a HELIOX-AC-V ^{3}He sorption cryostat, which can reach a base temperature of 280 mK. In order to minimize the optical power load inside the cryostat, two low-pass filters with cut-off frequencies of 1 THz and 3 THz and two neutral density filters with 10 dB attenuation each were mounted over optical windows in the radiation shields inside the cryostat.

The voltage to temperature response, $S_V = dV/dT$ of the CEB was obtained by subtracting voltage values for different temperature values at the same current in each point on the I-V curves acquired at varying bath temperatures. Alternatively, change in voltage could be measured when sweeping the base temperature at fixed bias current. An IV curve of a finline-integrated CEB with SIN junctions and its voltage response to the temperature as a function of bias voltage are shown in Fig. 5.6 and Fig. 5.7, respectively.

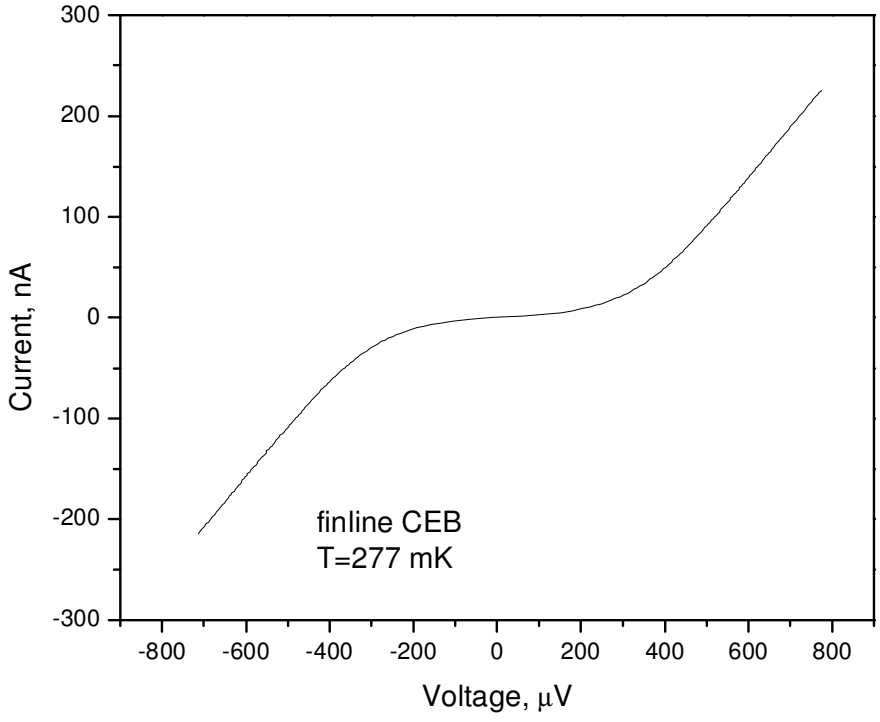


Figure 5.6. IV curve of a CEB integrated in a finline at a temperature of 277 mK [74, 87].

The RF response of the CEB was evaluated at 110 GHz with IMPATT diode, equipped with a horn, as an external RF source, by means of the experimental setup shown in Fig. 5.8. These measurements were performed by mounting the CEB-finline chip on a sample holder on the millikelvin stage in the cryostat and illuminating the chip from the outside (Fig. 5.9).

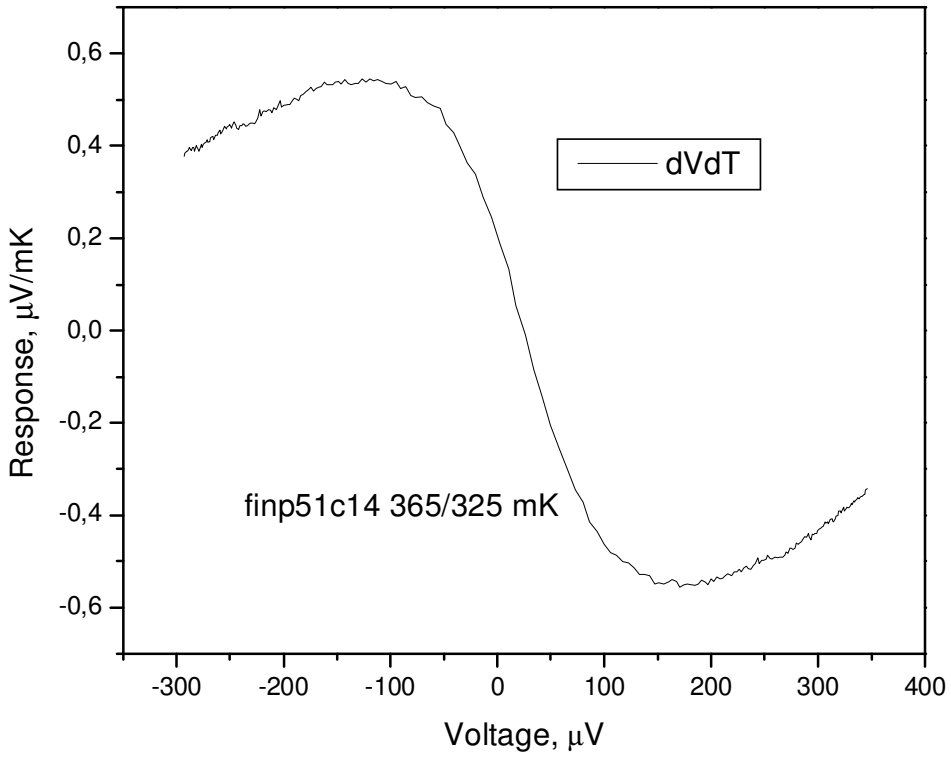


Figure 5.7. Voltage to temperature responsivity (dV/dT) of CEB versus bias voltage [74, 87].

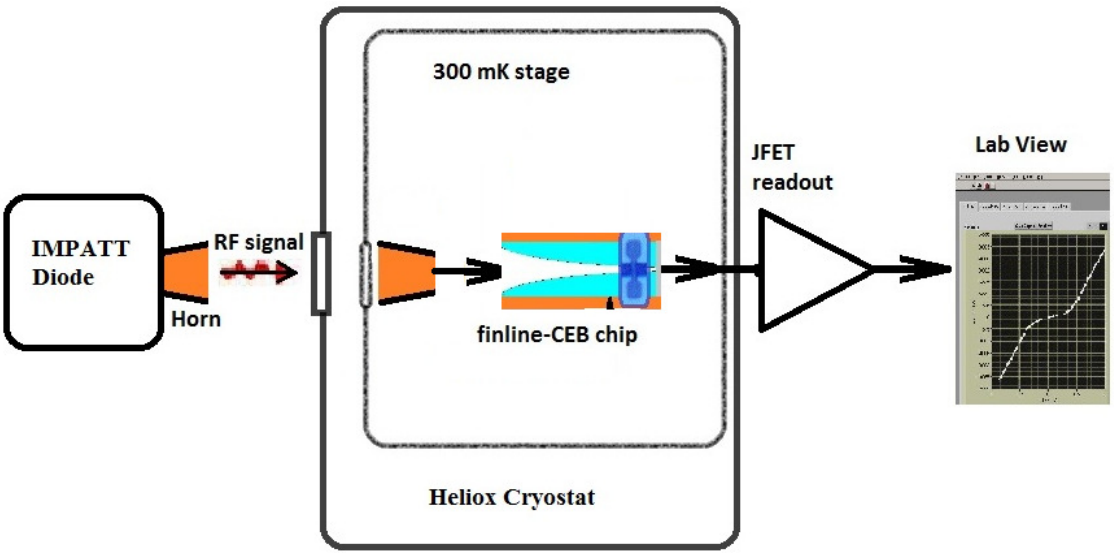


Figure 5.8. Experimental setup, block diagram. RF signal from IMPATT diode illuminates the finline-CEB chip through cryostat window; response is then measured by JFET readout.

Accordingly, some amount of RF power from a 110 GHz IMPATT diode with a horn was incident onto the finline that behaves similarly to a Vivaldi antenna in free space, loaded on one side by a dielectric substrate. The output RF power of the IMPATT diode was modulated at 127 Hz, and the response of the CEB was detected at three levels of the RF signal power. The measured total voltage noise is shown as a function of bias voltage in Fig. 5.10, and the RF response versus bias voltage is shown in Fig. 5.11 [87, Paper V].

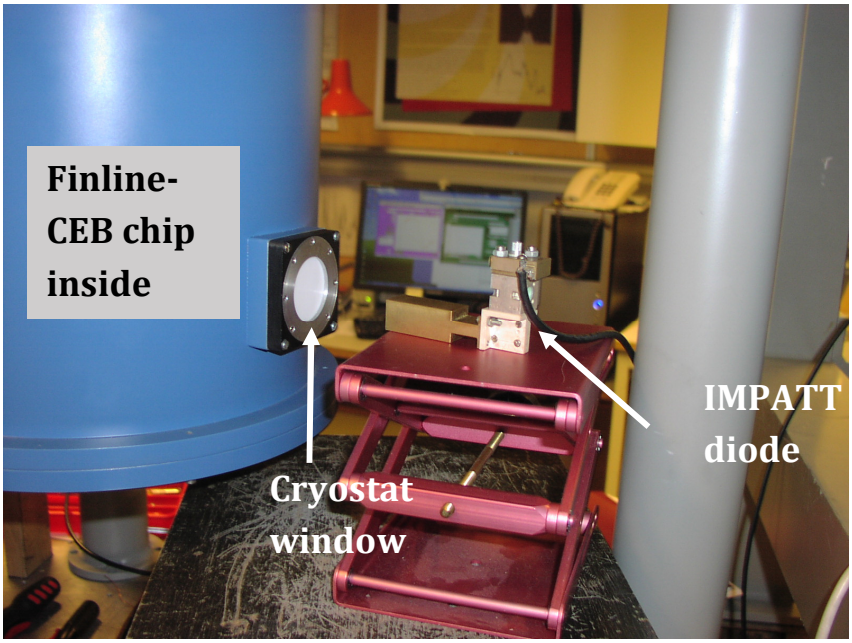


Figure 5.9. IMPATT diode source irradiating CEB through optical window [74, 87]

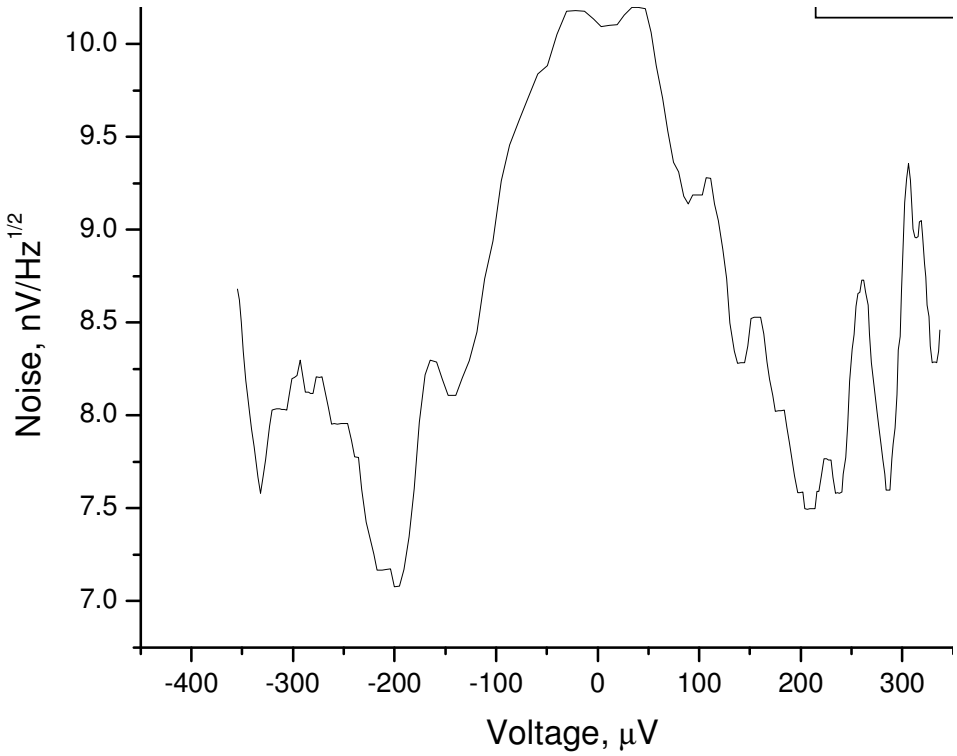


Figure 5.10. Noise of CEB at 127 Hz, measured with a room-temperature amplifier [74, 87].

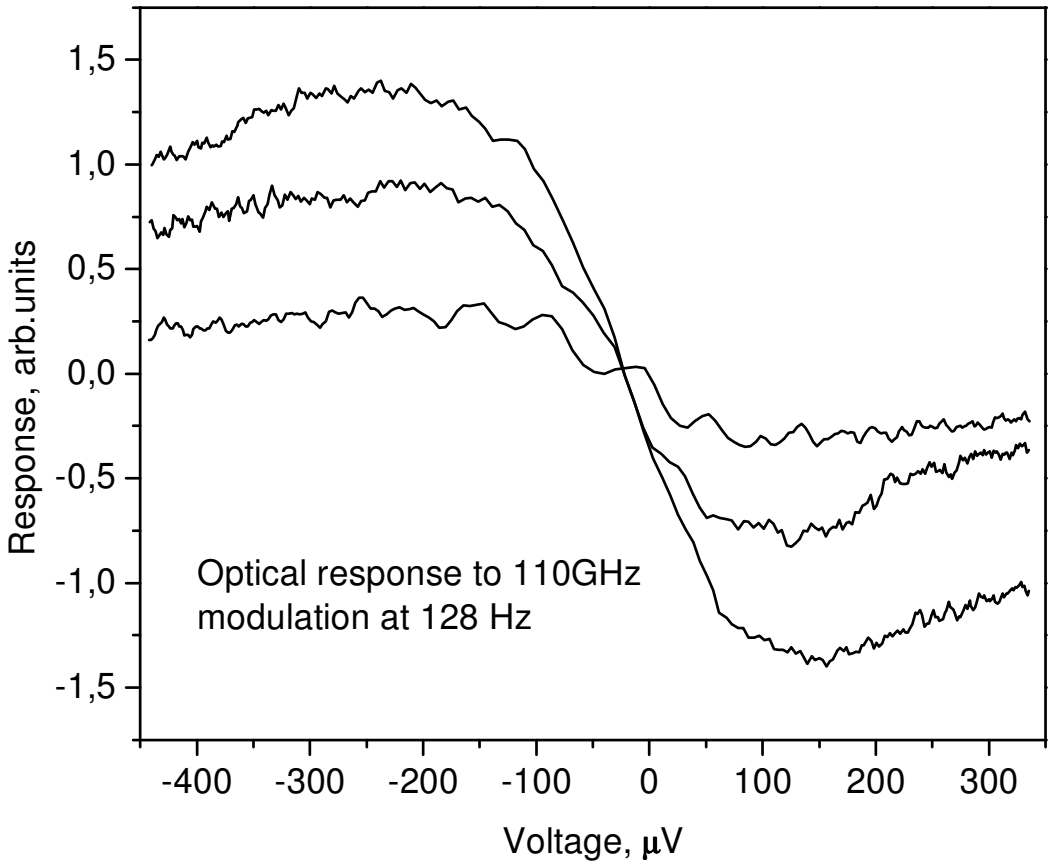


Figure 5.11. Voltage response of the CEB to incoming signal at 110 GHz at three levels of RF power, with additional attenuation of 0 dB, 3 dB and 6 dB, the three different curves [74]

The dark NEP of the CEB can be estimated using the above experimental data. The voltage response is expressed by:

$$S_V = \frac{dV}{dP} = \frac{dV}{dT} / G \tag{5.1}$$

Here, G is the total thermal conductivity that consists of the thermal conductivity due to the electron-phonon interaction given by $G_{e\text{-}ph}=5\sum \Lambda T^4$ and the thermal conductivity due to thermal flow by electrons:

$$G_i = \frac{dP}{dT} = \frac{d}{dT}\left(k_B T \frac{I}{e}\right) = \frac{k_B I}{e} \tag{5.2}$$

For a CEB with two SIN tunnel junctions of 1.5×1.5 μm^2 each and absorber thickness of 50 nm, volume of absorber is $\Lambda = 2\cdot10^{-19}$ m^3, and material parameter for copper is $\sum = 3\cdot10^9$ Wm^{-3}K^{-5}. Thus, at a bath temperature of 280 mK, the thermal conductivity due to electron-phonon interaction can be estimated as $G_{e\text{-}ph} = 1.84\cdot10^{-11}$ W/K. At bias current of 20 nA, the thermal conductivity due to the thermal flow by electrons

will be $G_i = 1.6 \cdot 10^{-12}$ W/K, which yields a total thermal conductivity of $2 \cdot 10^{-11}$ W/K. Using Eq. (5.1), for the experimental value of $dV/dT = 0.5$ μV/mK we obtain $dV/dP = 2.5 \cdot 10^{7}$ V/W. The NEP of our device can then be estimated using this value and the voltage noise v_n:

$$NEP = \frac{v_n}{dV / dP} \tag{5.3}$$

Relying on the maximum experimental value obtained for bolometer output noise about ~10 nV/Hz$^{1/2}$ (including the amplifier noise) and the estimated voltage response of $2.5 \cdot 10^{7}$ V/W, an estimate for NEP in current-biased mode can be obtained:

$$NEP_{ibias} \approx 4 \cdot 10^{-16} \text{ W/Hz}^{1/2}.$$

This assessment was performed in an experiment with the room-temperature readout system. It demonstrates that the finline CEB operates as a bolometric detector. With an absorber of reduced volume and in the voltage bias mode with SQUID readout, the dark NEP of CEB devices is expected to reach much lower levels.

5.6. Measurements of RF response with power source inside the cryostat

In this section, calibrated measurements of the RF response in experiments with the finline-integrated CEB mounted in a 97 GHz copper waveguide are presented. A black body RF power source was implemented inside the cryostat for this experiment.

For testing the CEB devices, an RF block made of oxygen-free copper was fabricated by our British collaborators at Oxford University, in Physics department workshop; the rectangular waveguide (Fig. 5.12) has a cross-section of 1.27 × 2.54 mm and is equipped with a 1.87 mm wide chip groove, to fit the finline-CEB chip.

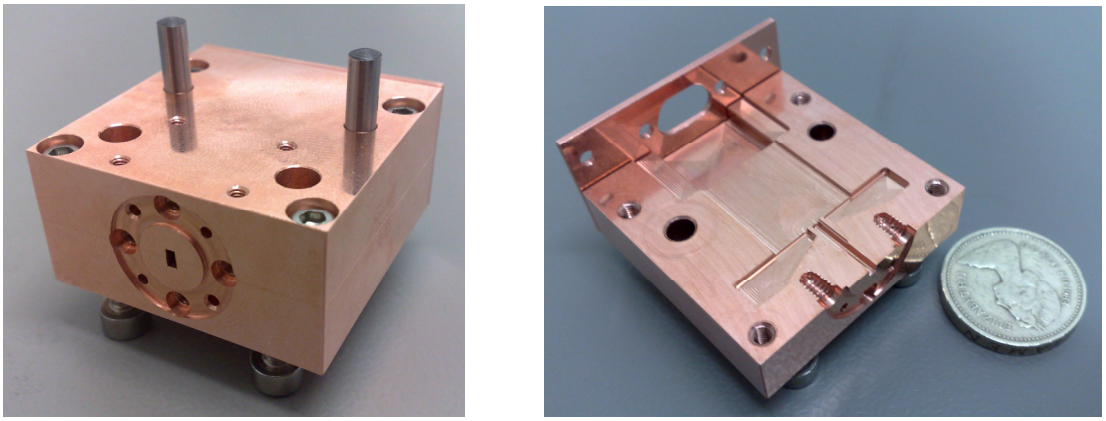


Figure 5,12. Photos of the 97 GHz waveguide block [87, Paper V].

The chip with a CEB-finline integrated circuit was mounted in the waveguide and coupled to the DC readout electronics using bondwires, see Fig. 5.13. The incoming RF signal was focused onto the waveguide input with a horn connected to the waveguide window.

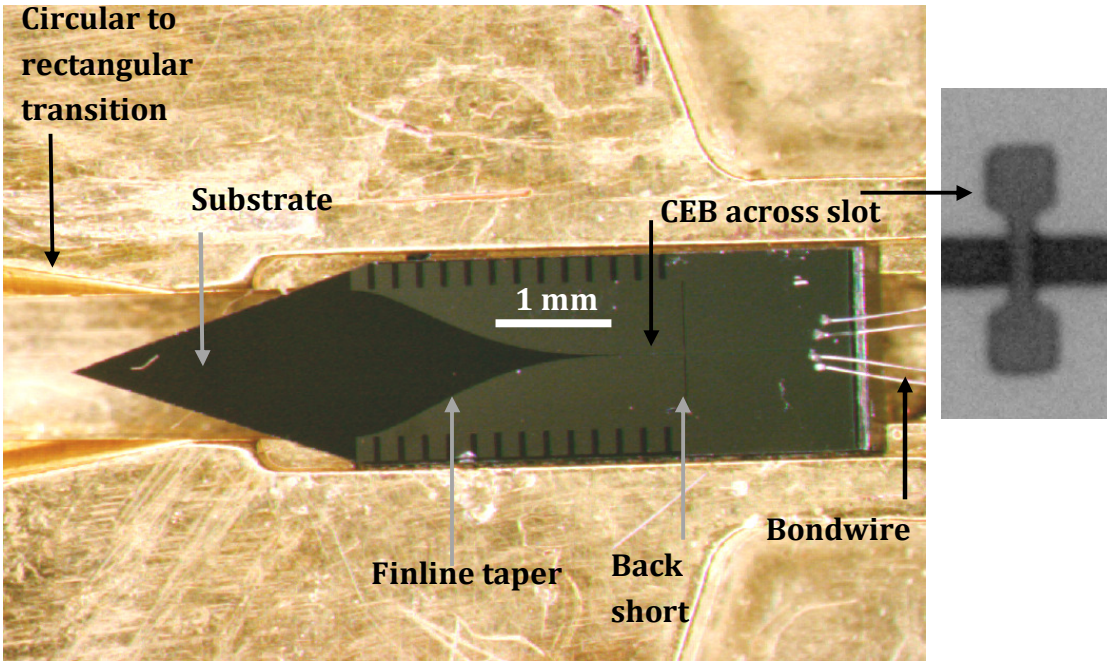


Figure 5.13. Photo of a 97 GHz finline-CEB IC mounted in the waveguide and bonded; (inset): enlarged CEB device across the slot [87].

For this experiment, a black body RF source was fabricated, including a concave surface for focusing the radiated signal onto the waveguide. The temperature of the RF source can be varied using a heater made of a copper coil heating the concave entity. The heating power is controlled by adjusting the applied voltage and hence the current through the copper coil.

The RF power source was equipped with a temperature sensor connected to the readout electronics for controlling its temperature in a range between 3 K and 25 K by measuring the actual temperature and adjusting the applied voltage in a feedback loop. The photo of the RF source with an aluminum shield for protection from excessive irradiation is shown in Fig. 5.14. The shield has a window equipped with a filter and facing the waveguide horn. The horn input was placed at a distance of 2 cm from the black-body RF source. The block diagram of the whole setup is shown in Fig. 5.15.

The CEB performance was tested in a ^{3}He sorption cryostat, at a bath temperature of 310 mK. The photo of the experimental setup in the cryostat is shown in Fig. 5.16.

DC IV curves were measured in the current bias mode, and the voltage to RF power response was obtained by subtracting IV curves in current-biased mode at different RF source temperatures. Voltage response of up to 40 μV was obtained for the temperatures of 7 K and 10 K, see Fig. 5.17.

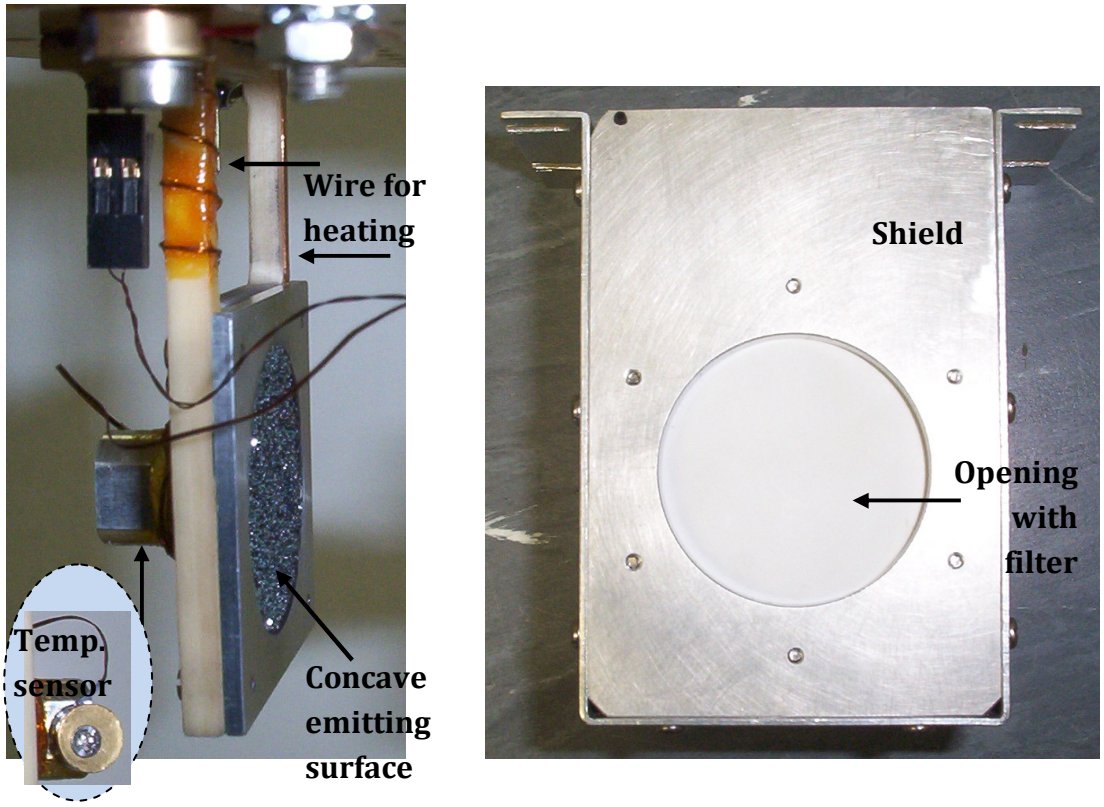


Figure 5.14. Black body RF power source (Left) with cover (Right). Temperature sensor is coupled to electronics. The connector on the top feeds heating current into the power source.

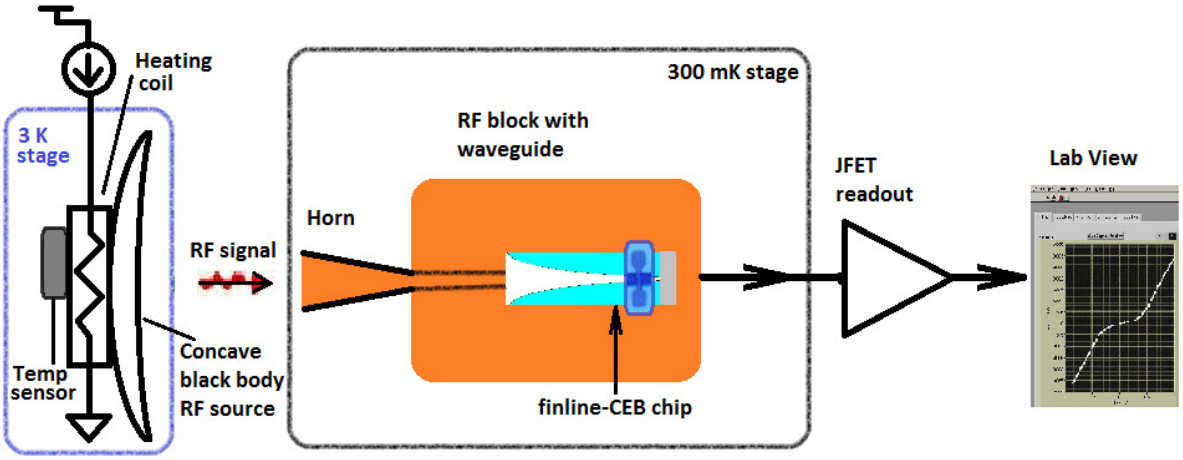


Figure 5.15. Schematic of the experiment. RF signal is emitted by a controllable RF source; focused onto the waveguide input and detected by the CEB device mounted in the waveguide.

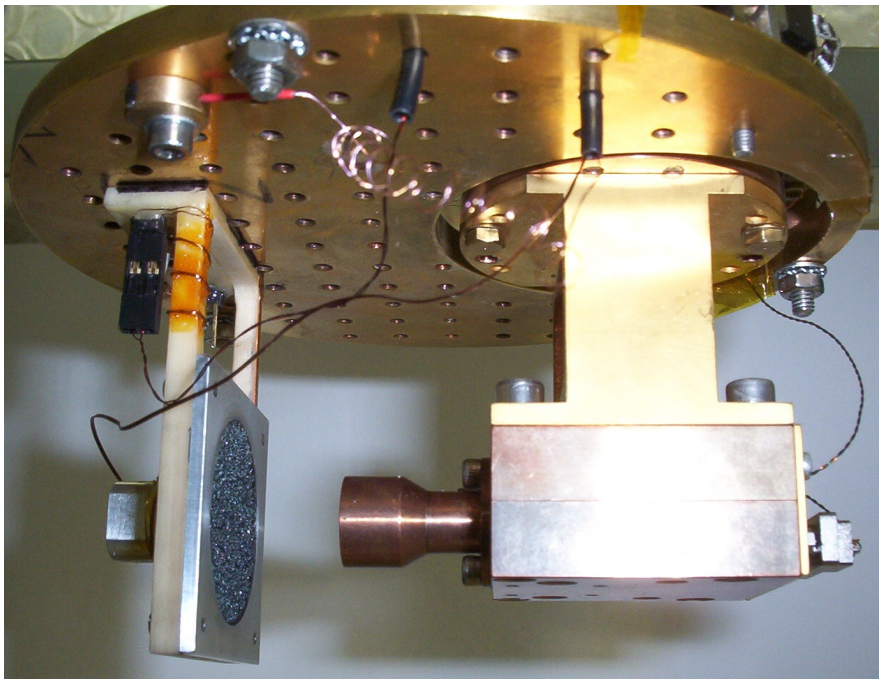


Figure 5.16. Photo of the setup: detector block with CEB device on the cold stage (300 mK), and the black-body RF source on the 3K stage inside the cryostat.

5.7. Analysis of the RF measurement results

The voltage to the RF power response obtained by subtracting IV curves at the temperatures of 7 K and 10 K versus bias voltage across the CEB device is shown in Fig. 5.17. Maximum voltage response of about 40 μV was achieved; using these data, the voltage to RF power responsivity and hence the NEP can be estimated, relying on the Planck formula for the given source temperatures (5 to 10 K).

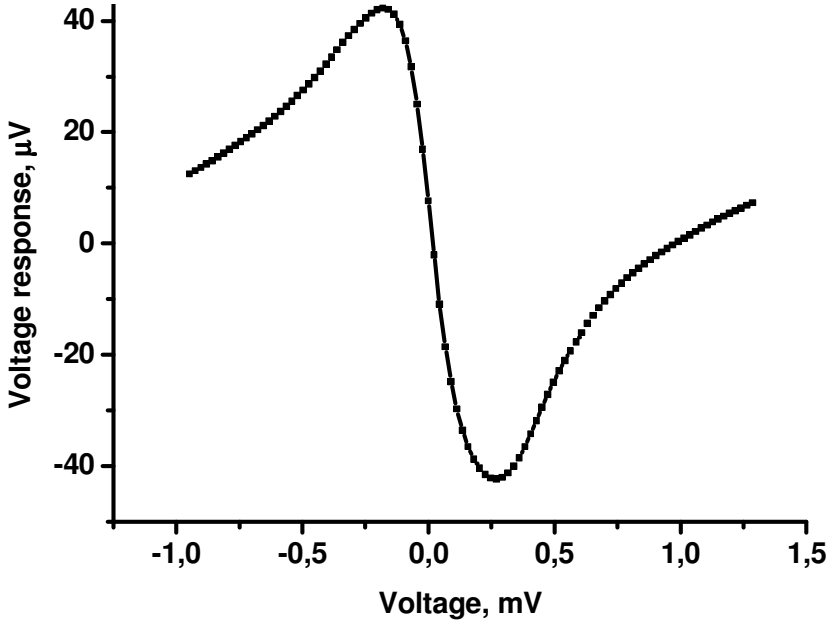


Figure 5.17. Voltage response to incoming power versus bias voltage, 7 K and 10 K

Simulations performed with HFSS software showed that the bandwidth of the finline chip in the waveguide is around 34 GHz (Courtesy Dr. Boon Kok Tan). This result was obtained using the HFSS setup shown in Fig. 5.18 and is consistent with the fact that the waveguide operates as a filter that does not accept lower frequencies, limited by the waveguide dimensions. On the other hand, high-frequency components are not matched with the finline impedance at the interface between the waveguide and the finline and are therefore rejected. In addition, high-frequency modes are filtered out by finline notches, see Fig. 5.18 (top).

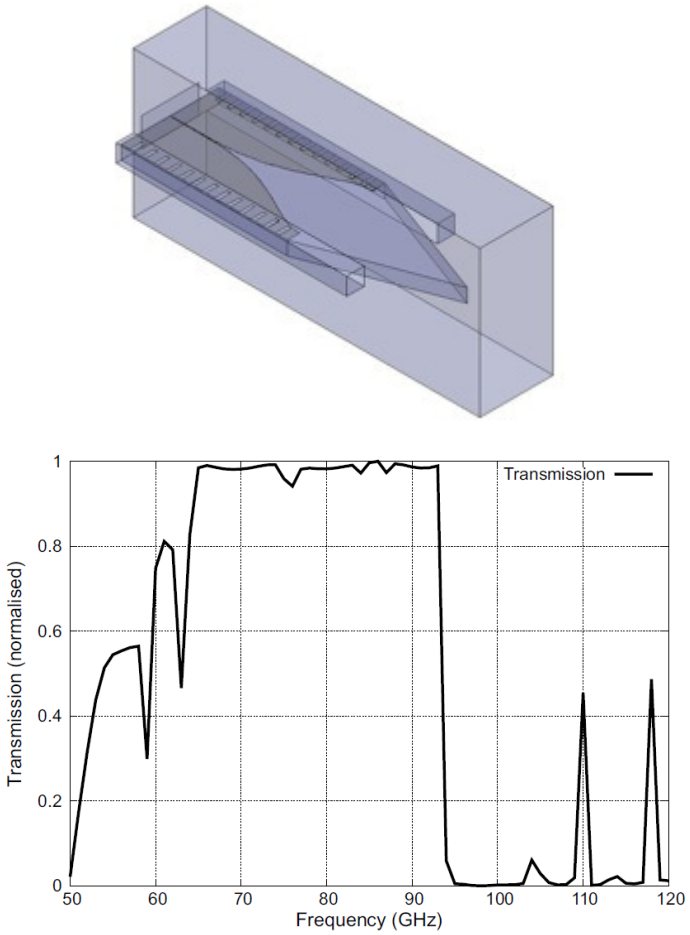


Figure 5.18. (Top) HFSS setup used for bandwidth estimation (Bottom): the normalized transmission (Courtesy Dr. Boon Tan)

For a frequency range around the frequency of f = 78 GHz with a bandwidth of δf = 34 GHz, the RF power emitted by a black body at a temperature of T = 10 K is given by:

$$\delta P = \frac{\kappa \cdot hf \cdot \delta f}{\exp(hf / k_B T) - 1} = 3.87 \times 10^{-12} \text{ W}, \tag{5.4}$$

assuming the emissivity of the black body source κ = 1, where h is Planck's constant and k_B is the Boltzmann constant.

The emitted power for 7 K is estimated as 2.5×10^{-12} W. Subtracting the calculated power values at source temperatures of 10 K and 7 K yields $\Delta P = 1.37\times10^{-12}$ W. Assuming a voltage change of 40 μV for this power difference, a voltage responsivity can be obtained:

$$S = dV/dP = \Delta V/\Delta P = 2.92\times10^{7}\ \text{V/W}\ , \tag{5.5}$$

The total voltage noise measured in this experiment was v_n = 11 nV/Hz$^{1/2}$; hence, the optical NEP is obtained by dividing this value by the voltage to the RF power response:

$$NEP = \frac{v_n}{dV/dP} = v_n/S = 3.76\times10^{-16}\ \text{W/Hz}^{1/2}.$$

The above result is only an estimate; while the connection from the RF source to the finline-CEB chip includes several interfaces, the coupling all the way from the source to the detector chip was regarded as ideal.

A straightforward and robust technology was chosen for the fabrication of these devices, which was a reasonable choice; in this experiment the full functionality of the finline-coupled CEB device was demonstrated. Also, the CEB-finline integrated circuit coupled to a waveguide and further to the free space with a horn was demonstrated as a feasible design.

At the same time, fabrication methods used here were not optimized in terms of the CEB performance. The trilayer fabrication technology employed for manufacturing these devices, does not allow for a thin and narrow absorber. Hence, the volume of the absorber was not selected for the best sensitivity. Consequently, the performance of the CEB could be improved by using advanced technologies and by modifying the chip layout. Also, further improvements are possible using advanced read-out schemes, including low-temperature readout amplifiers combined with measurements in voltage-biased mode.

Theoretically, for a CEB with reduced volume of the absorber and in the voltage bias mode with SQUID readout, the dark NEP can reach levels down to ~ 10^{-18} W/Hz$^{1/2}$ [56, 66]. Different NEP components and current responsivity anticipated for such as device when using SQUID readout are shown in Fig. 5.19. For most practical cases the NEP will be determined by a background power load P_{bg} that amounts to about 5 pW for CMB, and for a frequency of 100 GHz the photon NEP can be estimated as:

$$NEP_{phot} = \sqrt{2P_{bg}E_{quant}} = \sqrt{2P_{bg}hf} = 2.4\cdot10^{-17}\ \text{W/Hz}^{1/2}.$$

The goal is to be able to detect signals with intensity close to the above order of magnitude. Experimental results presented here confirm that we approach the required level in our development.

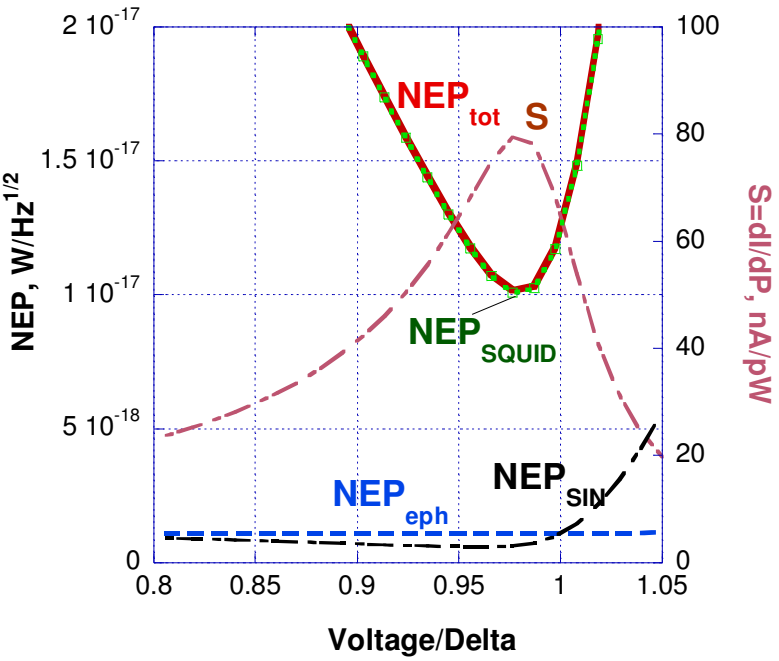


Figure 5.19. Simulated NEP components and responsivity S for improved parameters of the CEB, power load of 20 fW, and SQUID noise current of 0.8 pA/Hz$^{1/2}$ [56, 87, Paper V].

5.8. Conclusions

In this chapter, the analysis and experimental investigation of a Cold-Electron Bolometer, deposited across a unilateral finline on a planar substrate, were presented. This detector is a potential candidate for forthcoming space cosmology missions and is also of interest to ground-based experiments, due to its low NEP, the simplicity of integration in planar circuits, the high saturation power and the fast response.

The finline-integrated CEB devices were fabricated using Direct-Write Trilayer technology for processing of the bolometer structures. Successful operation of a CEB device was demonstrated, and its DC and RF characteristics were measured. Based on the DC experimental data, the dark noise equivalent power was estimated as NEP ~ $5 \cdot 10^{-16}$ W/Hz$^{1/2}$, for the devices in the current biased mode operating at 300 mK and read out by room-temperature amplifiers.

The detector's RF response was measured by focusing an electromagnetic signal onto the waveguide input with a horn. The estimated optical NEP of ~4×10^{-16} W/Hz$^{1/2}$ approaches the requirements of CMB polarisation measurements. This value can be improved by adjusting the optical coupling and modifying the readout electronics. Further improvement could be expected by the employment of smaller absorber and modifications in the design and fabrication technology, and also by using advanced readout schemes.

Chapter 6
CEB fabricated with Titanium based technology and integrated in planar antennas

Bolometric devices presented in this thesis are fabricated using electron-beam and photo lithography and can be integrated in planar antennas fabricated in the same fabrication run. Planar antennas and quasi-optical coupling schemes [93, 94] have been employed extensively for high-frequency applications during the last decades, after the first experiments [94, 95]. This approach has certain advantages over waveguide systems, including simpler and cheaper fabrication procedures, better accuracy and the option of integrating large arrays in planar antennas [93, 94].

In this chapter, SIN tunnel junctions and CEB devices integrated in planar antennas and fabricated using Ti-based technology are presented. Also, CEB performance is evaluated experimentally and analyzed. Experimental results include DC and RF testing of CEBs comprising a thin Ti film absorber and two SIN junctions integrated in planar antennas, such as log-periodic antennas and double dipole antennas. The experiments were performed using different types of RF power sources inside a He^3 sorption cryostat HELIOX-AC-V at bath temperatures of 280 to 305 mK, including the hot/cold method with flipping a Cu reflector opposite a blackbody surface inside a 3 K shield and using a thermal power source with variable temperature.

As has been shown in the previous sections, the CEB performance is determined by the properties of the SIN junctions and the CEB layout. The volume of the absorber determines the CEB's sensitivity due to the principle of operation of hot-electron bolometric detectors. Large volume limits the sensitivity and thus the overall performance of the CEB; so, it seems attractive to reduce thickness of the absorber, which ability is limited when using the Trilayer direct-write technology. In Trilayer process, the absorber is deposited on the top of the superconducting Al electrode, which results in a thicker absorber than in the case when the absorber is deposited prior to the superconducting counter-electrode. Consequently, the Trilayer process does not provide fabricating of very thin absorbers. Besides, after creating the tunnel junctions, the temperature of baking the resist for absorber patterning is limited; this reduces the resolution of the lithography and therefore limits the minimum feature size of the absorber.

6.1. The concept of the Titanium-based CEB

In order to overcome the above limitations and to optimize the CEB performance, new approaches have been investigated [Papers I-IV], including the employment of titanium-based CEB devices as an alternative to Al-based structures [Papers III, IV]. This is a novel direct-write technology for fabricating Ti-TiO_2-Al tunnel junctions for bolometer devices and thermometry [Paper III, 55]. The goal was to develop a simple and efficient technology for fabrication of SIN tunnel junctions between Ti and Al with TiO_x as an insulating barrier. The key feature of this method is the deposition of a normal Ti film as a bottom electrode and the superconducting Al film on the top of it after creating a TiO_x insulating barrier, possibly by *ex-situ* oxidation of Ti. This fabrication procedure is described in detail in Chapter 3 and shown in Fig. 3.12. The process consists of two steps: first, the Ti absorber is created and oxidized, and then the Al counter-electrode is deposited and patterned (Fig. 3.12).

This approach allows for an absorber thickness below 5 nm since the absorber is deposited prior to the superconducting counter-electrode, and the tunnel junction is created after the deposition of the absorber. This is possible by using TiO_x as an insulator for the tunnel barrier created by natural oxidation of Ti that is deposited as the first layer. Another advantage of this method is the ability to realize a fully flat absorber with no bending parts that are inevitable in Trilayer processes and create leakage currents that degrade the performance of the CEB detector. In addition, since the absorber is patterned before creating the tunnel junctions, there are no limitations on the width of the absorber related to lithography resolution due to limited resist baking temperature.

6.2. Fabrication and chip layout

The devices presented here were fabricated by the author of this thesis using photo-lithography and the technology for fabricating tunnel junctions proposed by Kuzmin [Paper IV]. The procedure includes *ex-situ* Ti oxidation for the creation of the TiO_2 insulating barrier; the fabrication process is described in detail in Chapter 3. Some example CEBs and other devices with SIN junctions fabricated using this method are shown in Fig. 6.1 [Paper IV]

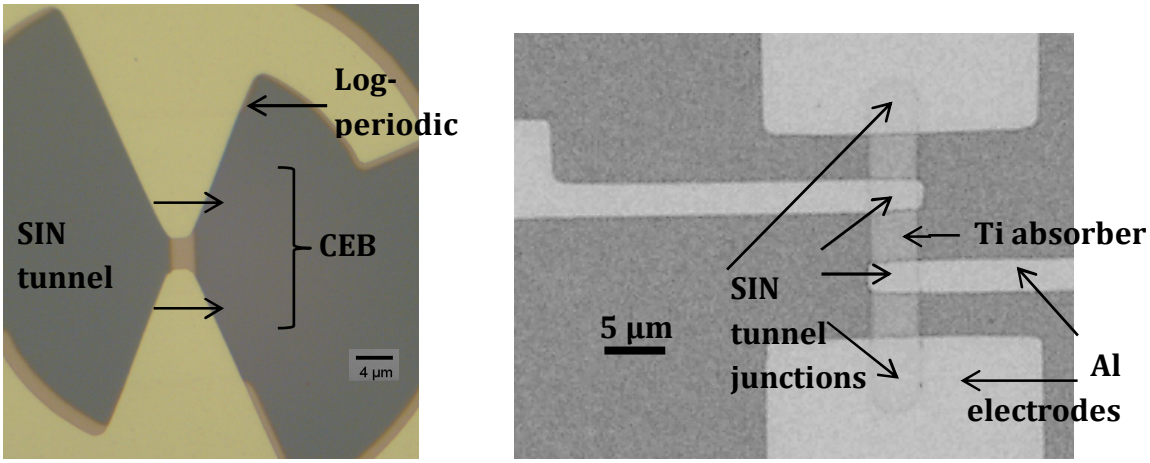


Figure 6.1. Optical images of: (Left) a CEB integrated in a log-periodic antenna; (Right) a 4-junction test structure; both devices fabricated using Ti-based technology [Paper IV, 74].

Due to the oxidation temperature of 130 to 150 ˚C one can expect better quality of the junctions than that of the junctions created at room temperature when the molecules of water and/or hydrogen atoms are involved in the process of creating the tunnel barrier. One of the key features of *in situ* evaporation is the deposition and the oxidation at a very low base pressure. As a result, the influence of water and hydrogen is mostly eliminated. On the other hand, in our *ex-situ* process, the temperature exceeds the water evaporation temperature, which ensures absence of hydrogen in the vicinity of the tunnel barrier. Other sources of contamination degrading the quality of the tunnel barrier, such as residues of organic materials, are eliminated by oxygen plasma etching followed by subsequent ion milling. This process also removes any compounds of Ti with other elements, built on the surface. Experience shows that this is a critical step in the fabrication procedure as the quality of a tunnel junction strongly depends on the process time of ion milling. If this time is not long enough, the quality of the tunnel barrier is very poor, measurements show. Increasing this time (at the same ion gun voltage) assures complete removal of any residues from the surface and enables reasonably good quality of the tunnel barrier.

The chip layout of the devices presented here includes CEB devices integrated in a double dipole antenna that is optimized for RF reception in the 100 GHz frequency band around 300 GHz and CEB devices integrated in a log-periodic antenna designed for reception at frequencies between 30-150 GHz (e.g. Fig. 6.1, left). Both the double dipole and the log-periodic antennas were fabricated on a Si wafer with a 400 nm thick SiO_2 layer.

Double dipole antenna design and characteristics are discussed in [58]; a generic layout is shown in Fig. 6.2 [58]. A double dipole antenna consists of two symmetrical elements [94] that in our case are made of thin metal films deposited on a Si substrate (Fig. 6.2). The incident signal is received as a differential signal between the two halves of the antenna [58], unlike monopole antennas which receive single-ended signals between a conductor and a ground. Double dipole antennas are resonant elements, with standing waves between the two halves of each element. The length of the elements in the antennas is determined by the wavelength to be received: in a half-wave dipole, each half of the two elements is about 1/4 wavelength long, so the whole antenna is a half-wavelength long [58].

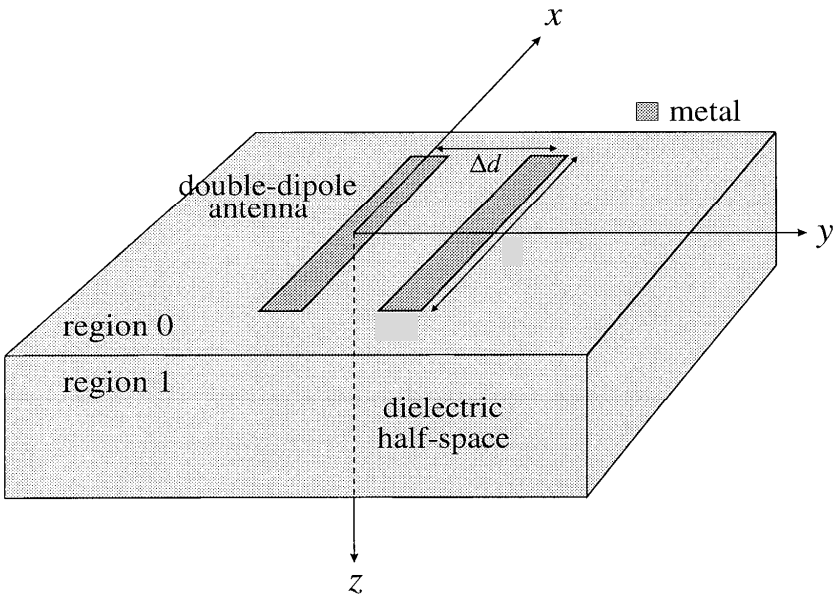


Figure 6.2. Layout of a double dipole antenna made of two thin metal film elements deposited on a dielectric substrate [58]

Log-periodic antennas are broadband antennas with regularly repeating characteristics as a logarithmic function of the received radio frequency. This is achieved by designing the layout of the elements of a log-periodic antenna in such a way that their lengths and the spacing between them increase logarithmically from the interior part to the exterior one (see e.g. the antenna in Fig. 6.3). As a result, the input impedance depends as a function of logarithm on the incident signal frequency. This approach is used for high-frequency applications when a wide frequency range and narrow beam are desirable. The log-periodic antennas used in our designs are dipole elements

driven by a balanced (differential) signal between the two halves of the antenna, see Fig. 6.3. A CEB devices fabricated using the Ti-based technology and integrated in such an antenna is shown in Fig. 6.4; a CEB device with a double-dipole antenna is shown in Fig. 6.5.

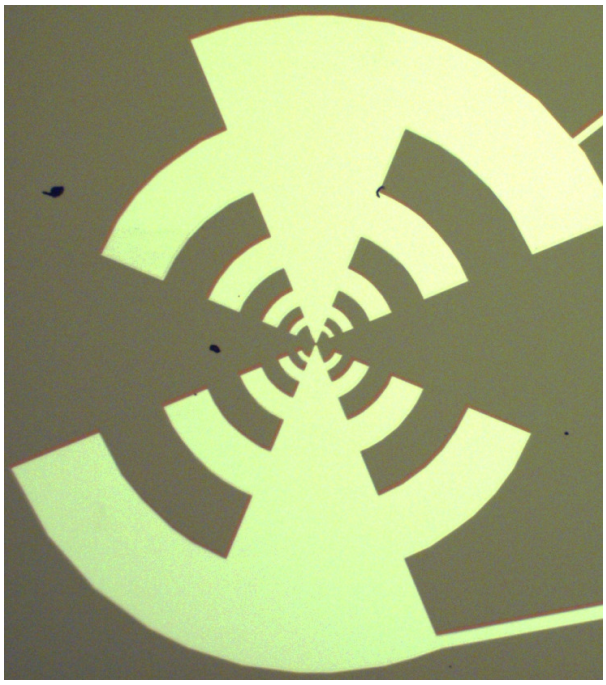


Figure 6.3. An optical image of a log-periodic antenna, fabricated for feeding a CEB device.

A photograph of a 4-probe test structure comprising a device with 4 tunnel junctions is shown in Fig. 6.1, right. The device consists of an absorber and 4 SIN junctions connected to 4 wires for measurements by 4 points. Our photo mask layout allowed fabricating 24 chips, 7×7 mm each, on a single 2-inch Si wafer.

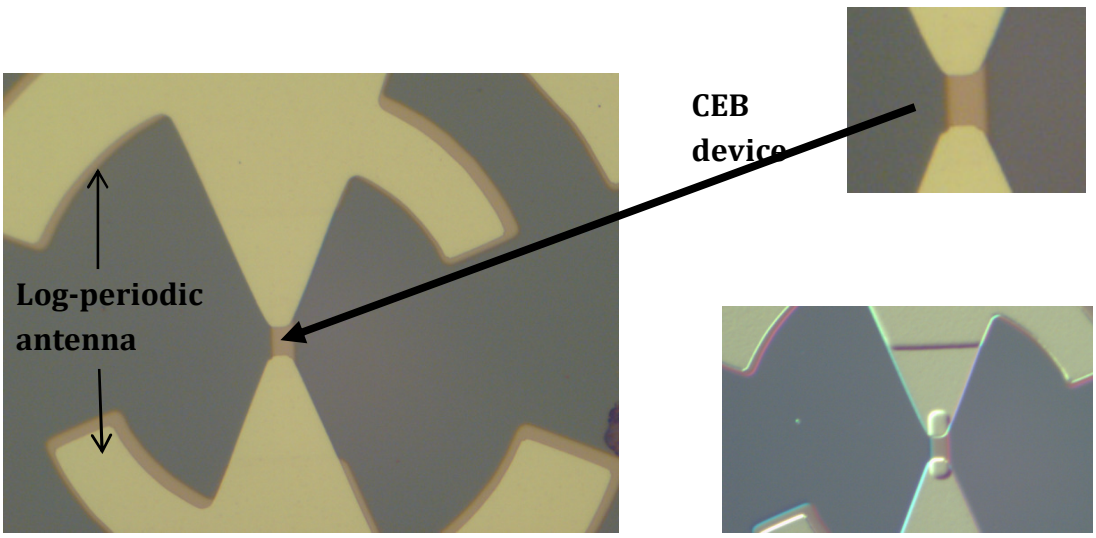


Figure 6.4. Optical image of a CEB detector with log-periodic antenna: a plain photo (Left) and a quasi-3D picture (Right); inset: CEB device enlarged.

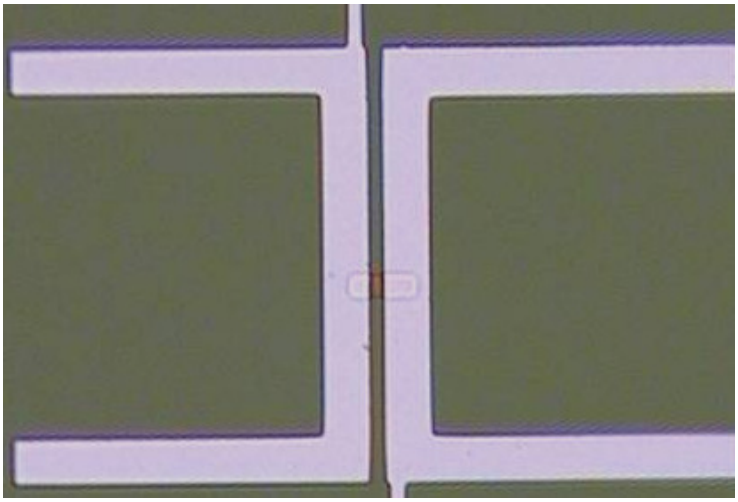


Figure 6.5. Photo of a CEB integrated in a double-dipole antenna designed for 280-350 GHz.

6.3. Experimental results and analysis

Several CEB devices fabricated with Ti-TiO_2-Al tunnel junctions and integrated in log-periodic or double dipole antennas were tested at temperatures of 280-310 mK using the HELIOX AC-V cryostat manufactured by Oxford Instruments. DC testing was performed in current bias mode using bias resistance values of 20 MΩ to 2 GΩ in the readout box described in Chapter 5 (see Fig. 5.5). Ti deposited with magnetron sputtering was not superconducting in the above temperature range, and the tunnel junctions showed typical behavior of SIN junctions. An example IV curve of a single SIN tunnel junction is shown in Fig. 6.6. The dynamic resistance at zero voltage R_d and the normal resistance R_n of the SIN junctions were measured, and the ratio R_d/R_n was estimated, as a measure of quality of the tunnel junctions. Measurements have shown very high quality of fabricated tunnel junctions along with low leakage currents, as ratios R_d/R_n of 1000 and above were achieved for some SIN junctions at 280-300 mK. These results are comparable to previously reported data for Al-based tunnel junctions fabricated with the standard shadow-evaporation technique [64, 73].

The DC temperature response of the device was obtained by measuring the voltage response to the change in bath temperature in the cryostat between 300 and 800 mK. A dV/dT value of 1 μV/mK was achieved for two junctions in series, which is 0.5 μV/mK for each junction. Increasing number of SIN junctions in an array yields higher sensitivity, as has already been demonstrated for Al-based junctions [Paper II], which enhances the potential of using SIN tunnel junctions for measuring the on-chip temperature and hence apparently the RF power.

It has already been shown [68, Paper II] that a total voltage response of a series array of SIN tunnel junctions at fixed biasing current is proportional to the number of junctions in the array, whereas the total noise of several junctions is proportional to

the square root of that number. Therefore, by increasing the number of junctions in an array, the temperature sensitivity of the array can be enhanced. This was confirmed experimentally for an array of 100 Al-based tunnel junctions by Otto *at al* [Paper II], with a dV/dT of 52 μV/mK achieved for 100 junctions in series, which yields a value of 0.52 mV/K for a single junction.

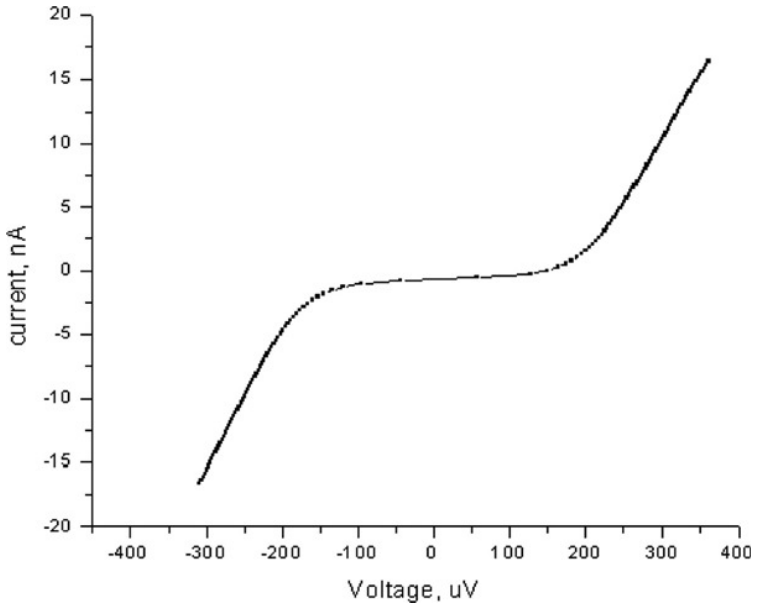


Figure 6.6. IV curve of a single SIN tunnel junction fabricated with Ti-based technology [55]

Noise voltage spectra were measured using a room temperature MOSFET readout amplifier with a lock-in detector, and a voltage noise level of about v_n ~10 nV/Hz$^{1/2}$ was obtained. Based on these results, a dark Noise Equivalent Power (NEP) can be estimated by dividing the output noise by a voltage to power response *dV/dP* estimated from *dV/dT* measurements:

$$NEP = \frac{v_n}{dV / dP}$$

Assuming a *dV/dT* value of 1 μV/mK for two junctions in series and voltage noise of 10 nV/Hz$^{1/2}$, *dV/dP* can be estimated as ~10^8 V/W, which yields NEP ~10^{-17} W/Hz$^{1/2}$. This is however merely rough estimation based on DC measurement results. More accurate data based on results of RF measurements are presented later in this chapter.

The next step in evaluating the performance of the CEB devices was to measure the optical response using the hot/cold load method. For this, a rotating table carrying a Cu reflector and a blackbody surface inside the 3 K shield of the cryostat was implemented. Magnets placed on the table, along with an external magnet outside the cryostat, allow positioning either the blackbody surface or the reflecting one in front of the CEB device under test (Fig. 6.7). The CEB detector chip was mounted across a waveguide fed by a horn to couple the beam emitted by the black body or reflected by

the shiny surface to the antenna of the CEB detector. When the shiny surface faces the horn, it reflects the radiation emitted by the 280 mK stage. Therefore, by switching between the reflector and the blackbody source, the incident radiation temperature perceived by the detector was changed from 3 K to 270 mK. The corresponding change in the voltage across the device at fixed tunnel current was measured (Fig. 6.8); the voltage response measured for the detector integrated with a double-dipole antenna amounts to $\Delta V_{out} = 120\ \mu V$ (Fig. 6.8)

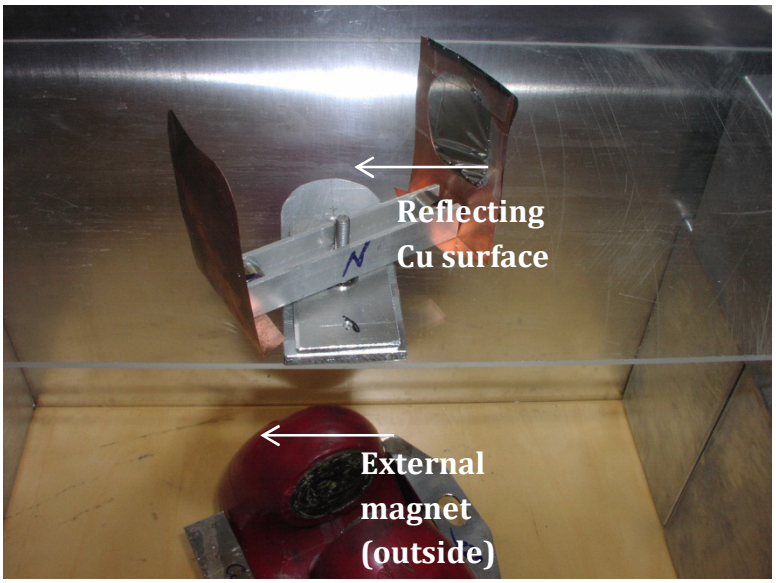


Figure 6.7. Photo of cold rotatable surfaces, later mounted inside the cryostat at 2.7 K. Below there is a magnet which was used to switch between the Cu shield and NDF in front of the window.

The optical properties of a double dipole antenna were studied earlier [96] and verified by our Bolo group at Chalmers using the Hilbert-spectroscopy technique [97]. Based on published data from experimental results, we estimate the bandwidth of our CEB-antenna integrated circuit to be around 100 GHz.

Considering the CEB-antenna integrated circuit as a single mode detector, one can easily calculate the radiation power δP incident on the detector [98]; the power received by 300 GHz antenna with a bandwidth δf =100 GHz, assuming a radiation source temperature of 3 K :

$$\delta P = \frac{\kappa \cdot hf \cdot \delta f}{\exp(hf / k_B T) - 1} = 3.8\times10^{-13}\ \text{W},$$

where h is Planck's constant, k_B is the Boltzmann constant, and $\kappa \approx 1$ is the emissivity of the black body source. Combining this with the maximum measured voltage response of $\Delta V = 120\ \mu V$ yields an estimate of the voltage to power response of

$$dV/dP = 3.18\cdot10^{8}\ \text{V/W}.$$

In this calculation, the RF power irradiated at 270 mK was neglected, as it is orders of magnitude lower than that at 3 K due to an exponential dependence of the power on the temperature in Planck formula. For the measured noise of $V_n = 10 \cdot 10^{-9}$ V/Hz$^{1/2}$, the optical noise equivalent power is therefore evaluated as:

$$NEP = V_n/(dV/dP) = 3.5 \cdot 10^{-17} \text{ W/Hz}^{1/2}.$$

In the next experiment [Paper IV], calibrated measurements of the RF response of CEB device with a log-periodic antenna to RF radiation was performed, when illuminated by externally controlled blackbody source, mounted inside the cryostat. The CEB was tested in a He^3 sorption cryostat with a base temperature of 280 mK, while the temperature of the blackbody source was controlled by external current.

In order to select a frequency band of interest, a bandpass filter was placed between the RF source and the sample. This is a mesh filter with a central frequency of 300 GHz, fabricated by the author of this thesis at Chalmers University using optical lithography and wet etching of a copper film on a 2-inch quartz substrate. The photo of the filter is shown in Fig. 6.9.

For measuring the transmission of the filters, a backwards-wave oscillator was used as an RF source, and a pyroelectric detector measured the propagating power.

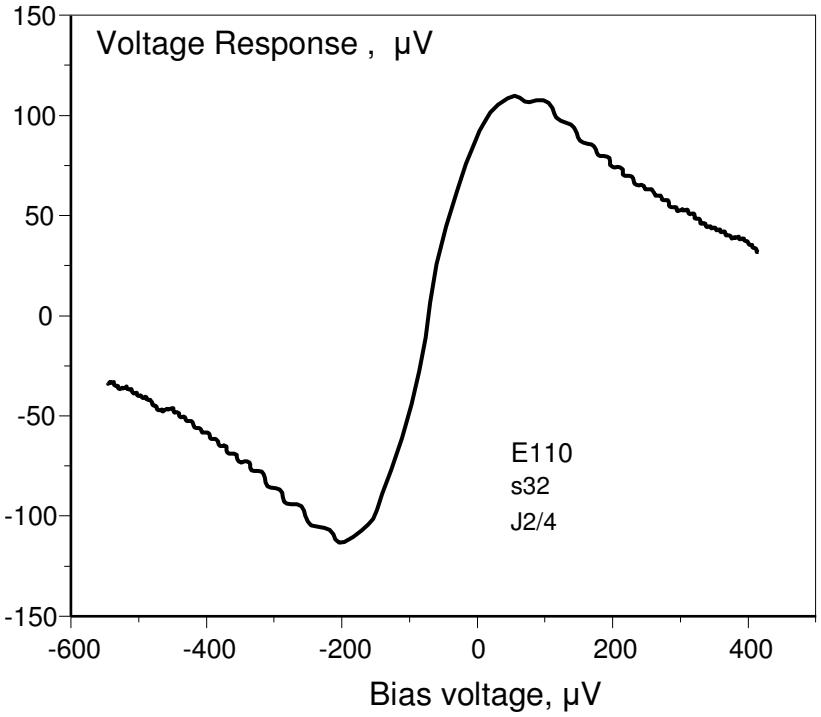


Figure 6.8. Optical response to hot/cold load, source temperature of 3 K and 270 mK

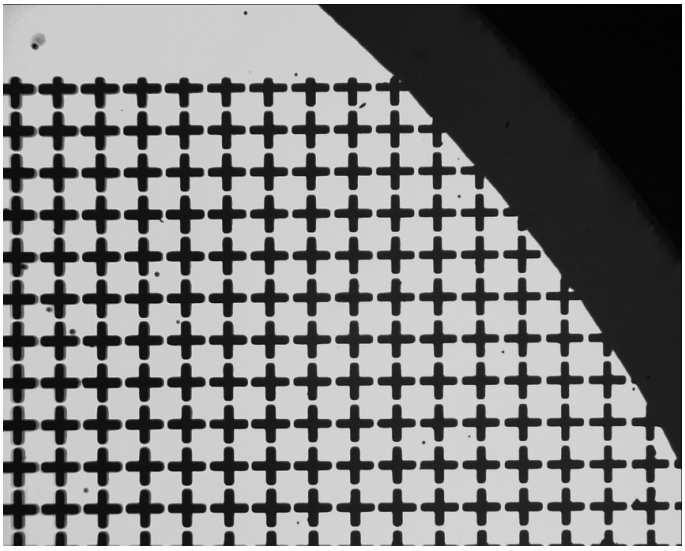


Figure 6.9. Photograph of the mesh filter made of copper on 2-inch quartz substrate.

The design the filter used in this experiment is similar to that of a filter presented in our work on mesh filters for other frequencies [99], which is a resonant bandpass filter consisting of flat periodic structures. In general, resonant metal-mesh filters made of copper films perforated with arrays of cross-shaped apertures were used in our experiments. Such filters are compact, easy to fabricate, can be cooled to millikelvin temperatures, and exhibit high center-band transmission, narrow bandpass, and significant stop-band rejection [100].

The layout of such a filter is shown in Fig. 6.10. The design is scalable, i.e. the central wavelength is scaled proportionally to the mesh period, while the spectral characteristic remains the same under such variations. The proper selection of dimensions L and W in Fig. 6.10 allows producing a filter with a reasonably high quality factor, which is one of the advantages of using cross openings.

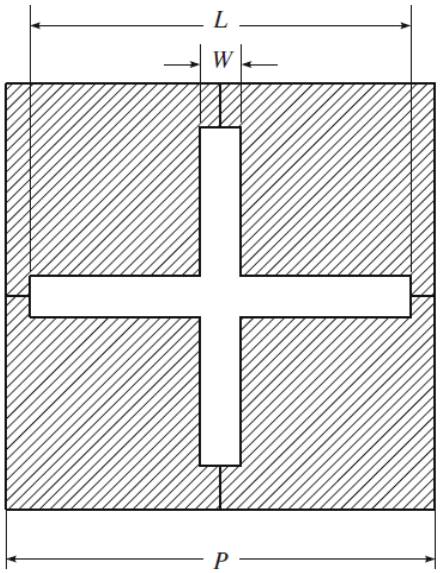


Figure 6.10. Layout of a unit cell of a band-pass mesh filter [99].

DC IV curves of the CEB devices with log-periodic antennas were measured in a current bias mode. The optical response was measured by illuminating the CEB with a black body source mounted inside the cryostat, at a 3 K stage. An attenuator with reflectivity of about 1% made of NiCr film on a KAPTON carrier was used as the black body source, glued onto a Cu plate equipped with a heater and a temperature sensor. The source temperature was regulated by controlling the current flowing though the black body source. The response to the incident signal was then obtained by subtracting voltage values for the same current points on the IV curves at different temperatures of the RF source (Fig. 6.11). The voltage response to the incoming radiation at different emitter temperatures versus bias current is shown in Fig. 6.12; the dependence of the response on the emitter temperature is shown in Fig. 6.13. The voltage response of up to 45 μV was achieved as the voltage difference at the same bias current for the temperature values of 3 K and 8 K for the black body source. Based on this value, the voltage to RF power response can be estimated using the Planck formula for the given emitter temperatures.

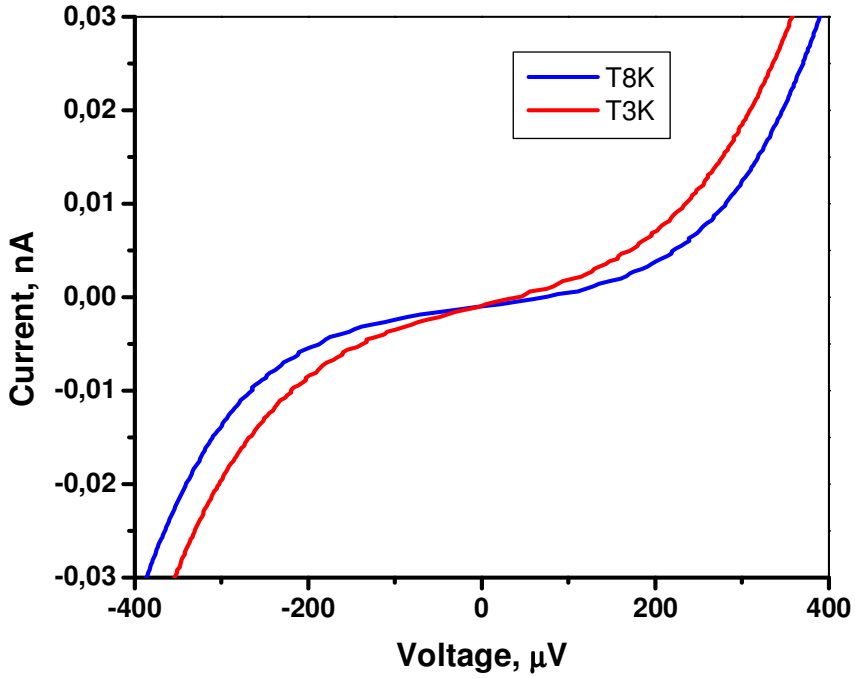


Figure 6.11. IV curves of CEB at 310 mK for 3 and 8 K black body source temperatures.

For a center frequency of f = 300 GHz and a bandwidth of 10 GHz, calculating the radiation power δP incident on the detector, with the CEB-antenna integrated circuit as a single mode detector [98], yields the power emitted by a black body at a temperature of T = 8 K given by

$$\delta P = \frac{\kappa \cdot hf \cdot \delta f}{\exp(hf / k_B T) - 1} = 4.3\times10^{-13}\ \text{W},$$

where h is Planck's constant, k_B the Boltzmann constant, δf the bandwidth, κ=1 is the emissivity of the black body source. The corresponding power for 3 K is ~3×10^{-14} W.

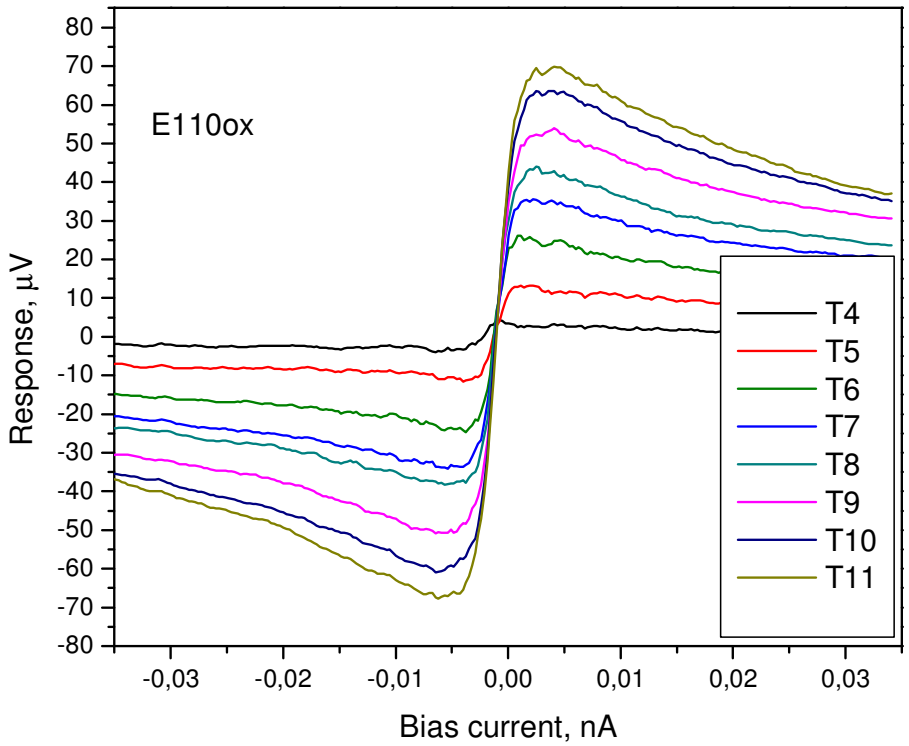


Figure 6.12. Optical response of a CEB versus bias current at different RF source temperatures, with a filter. The blackbody temperatures: T = 4, 5, 6, 7, 8, 9, 10 and 11 K.

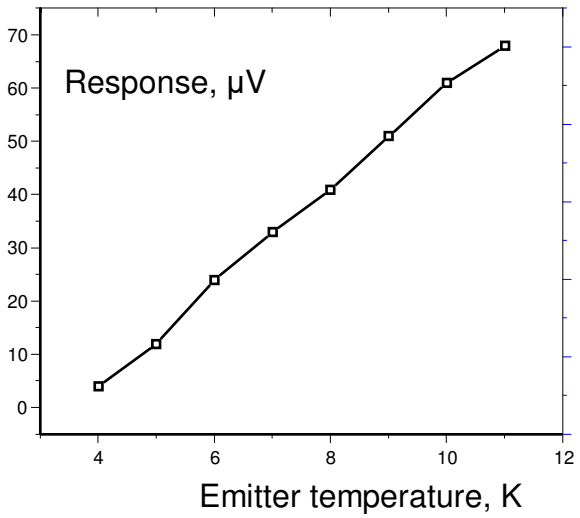


Figure 6.13. Voltage response versus emitter temperature

Subtracting the above values for RF power at source temperatures of 3 K and 8 K yields the difference in the incident power at these temperatures: $\Delta P = 4\times10^{-13}$ W. Considering a voltage change of 45 µV for this power difference and the total voltage noise of $V_n = 10$ nV/Hz$^{1/2}$, the optical NEP is obtained:

$$NEP = 8.88\cdot10^{-17}\ W/Hz^{1/2}$$

6.4. Discussion

The optical NEP values reported above are only estimates. The pathway from the RF source to the CEB detector includes several interfaces, and losses due to the mismatches at different interfaces from the source to the detector in the current configuration were only estimated. Also, the optical losses at temperatures below that of the load could reduce the power received from the load by the detector, which implies that the above optical NEP value is an overestimate of the inherent optical NEP of the device.

The voltage noise value of ~10 $nV/Hz^{1/2}$ was measured using the room-temperature amplifier box. As a result, the noise coming from the amplifier dominates the total noise measured. Therefore, much better noise performance can be expected when using cold amplifiers for noise measurements.

Regarding fabrication, a straightforward and robust Ti-based technology was chosen for the production of these devices. This was a reasonable choice for developing this experiment, because it allows demonstrating the full functionality of the CEB fabricated with this technology as a state-of-the-art bolometric detector. Also, it allowed demonstrating an integrated circuit comprising a CEB detector and a planar antenna as a feasible design. This is an important conclusion concerning possible implementation of CEB detectors in large format focal plane arrays.

However, the fabrication procedure and the chip layout were not optimized for best device performance. The volume of the absorber was not chosen for best responsivity; partly because photo lithography was used for fabricating these devices, which limits the minimum absorber width, and partly due to its thickness that was optimized for the RF impedance matching and therefore was not chosen for the best sensitivity, when fabricated using this technology. Therefore, improvements in the fabrication and design of the next generation of devices and readout electronics can potentially yield enhanced responsivity and improved overall performance.

Although photo lithography has been used to manufacture the samples presented here, the e-beam lithography with negative e-beam resist can be used for fabrication, in order to achieve better resolution and therefore smaller volume of absorber which is critical for the performance of the CEB [56, 66]. Devices with a reduced absorber volume operating in voltage bias mode with SQUID readout or another high performance cold amplifier should achieve much better NEP levels [56].

For most of practical cases the NEP will be determined by a background power load that is about P_{bg} = 5 pW (the CMB level) for ground based observations at a signal frequency of ~100 GHz, which yields a photon NEP of

$$NEP_{phot} = \sqrt{2P_{bg}E_{quant}} = \sqrt{2P_{bg}hf} \quad = 2.4 \cdot 10^{-17}\ \mathrm{W/Hz^{1/2}}.$$

Our measurements and analysis have thus demonstrated that such NEP values can be potentially achieved using Cold-Electron Bolometers with SIN tunnel junctions.

6.5. Conclusions

A novel technology for the fabrication of tunnel junctions between Ti and Al using titanium as a base electrode and titanium oxide as an insulating barrier has been developed. CEB devices have been fabricated using this technology, with the absorber deposited prior to the superconducting counter-electrodes. Fabricated CEB devices with Ti-TiO_2-Al SIN tunnel junctions are presented, as well as their performance evaluated at 300 mK. Specifically, the results of DC and RF measurements on a Cold-Electron Bolometer deposited across a double dipole antenna and a CEB integrated in a log-periodic antenna on a planar Si substrate have been presented. The fabricated SIN junctions are rather high-ohmic due to long oxidation time applied for creating the tunnel barriers. Shortening oxidation time combined with proper choice of temperature during oxidation allows creating more low-ohmic tunnel junctions. Thus, more development work is needed to realize SIN junctions that are more suitable for CEB fabrication. Hence, some optimization work is required in order to achieve optimal oxidation conditions during the creation of the tunnel barrier.

Optical measurements have yielded NEP ~3.5×10^{-17} $\mathrm{W/Hz^{1/2}}$ which is close to the CMB power level. Improving the design, using series arrays of SIN junctions and improving the readout should yield an NEP level below 1×10^{-17} $\mathrm{W/Hz^{1/2}}$.

Therefore, the detector can be a potential candidate for the next generation of space telescopes and is also of interest to ground-based astronomical experiments due to its high sensitivity, the simplicity of its integration to planar circuit technology, high saturation power and fast response.

Chapter 7
CEB Arrays for balloon-borne experiments

In this chapter, the Cold-Electron Bolometer array concept is presented, as well as CEB detectors fabricated for balloon-borne telescopes using the Advanced Shadow Evaporation technique and experiments conducted for testing of these CEB devices. This includes experimental results on testing of CEB detectors comprising a non-superconducting thin absorber made of a CrO_x/Cr/Al trilayer film and an array of Superconductor-Insulator-Normal (SIN) tunnel junctions integrated in a planar cross-slot antenna. Two series / parallel arrays of 10 Cold-Electron Bolometers with SIN tunnel junctions are integrated in orthogonal ports of each antenna.

The performance of the CEB devices was evaluated in a He^3 sorption cryostat HELIOX-AC-V at bath temperatures of 280 to 350 mK and in a dilution refrigerator TRITON at temperatures down to 50 mK.

High performance IV curves are demonstrated as an indication of high quality of tunnel junctions fabricated with this technology. Also, RF experiments are described, including measurements of the voltage response of the CEB arrays to the incoming RF power [65]. The optical response was measured in two different ways: first, using the hot/cold load method by flipping a Cu reflector opposite a blackbody surface inside a 3 K shield; and then using a black-body source placed in front of the detector chip mounted in a sample-holder inside a 3 K shield. Electron cooling that improves the sensitivity and increases the dynamic range of the device is also demonstrated in this chapter.

7.1 Balloon-borne telescope projects

CEB detectors presented here were designed for balloon-borne experiments dedicated to the CMB-related measurements. The BOOMERANG project was planned as a telescope employing bolometric detectors for mapping the CMB radiation. The BOOMERANG, which stands for Balloon Observations of Millimetric Extragalactic Radiation and Geophysics, was a sub-orbital (high altitude) balloon-borne telescope project that was dedicated to the measurements of cosmic microwave background radiation of a part of the sky [6, 101, 102]. The balloon and the instruments before the launch in Antarctica are shown in Fig. 7.1.

Figure 7.1. Boomerang: The balloon and the instruments before the launch.

The first flights of BOOMERANG around Antarctica started in 1998 in order to map the Cosmic Microwave Background (CMB). One of the first missions made a circle around the South Pole, while measuring variations in the temperature of the CMB across the sky, thereby mapping the CMB temperature anisotropies. The second flight in 2003 was dedicated to measuring both temperature and polarization anisotropies [101, 103], and a detailed map of the CMB's temperature fluctuations was produced. This provides information about the early universe, such as its geometry and the amount of matter and energy in it [101, 103].

For detecting millimeter-wave signals coming from the space, bolometric detectors operating at ~270 mK are used. The principle of operation of the instrument and the detectors is similar to other CMB-related projects. A mirror focuses the incident signal onto horns located in the focal plane, including 3 channels at 145 GHz, 245 GHz and 345 GHz. Only a fraction of the sky can be seen simultaneously, and the telescope needs to be rotated in order to scan the whole area [103].

7.2 The concept of parallel/series CEB arrays

For applications in radio astronomy, including balloon-borne and space experiments, such as e.g. BOOMERANG telescope project [101], the power of the background radiation determines the requirements for the detector performance. For a potential detector, it seems attractive to achieve an NEP level below the photon noise of an optical power load of 5 pW; as to polarization measurements, the cross-polar response should be at least 25 dB below the co-polar one. In this chapter, CEB detectors that can be used for CMB power and polarization measurements at frequencies around 345 GHz are presented.

When used with JFET voltage readout and current-biasing scheme, CEBs could be integrated on planar substrates using parallel / series arrays, proposed by L. Kuzmin for efficient noise matching between the detector output and the JFET amplifier readout [56, 66]. The incoming RF power is distributed between several absorbers, which improves the sensitivity of the array. This allows achieving low NEP levels and satisfying power load requirements. In such an array, made of several CEBs, additional decoupling capacitors are implemented for AC coupling of adjacent absorbers to the antenna in the RF path, while some absorbers are disconnected from the antenna in the DC lead, according to the topology shown schematically in Fig. 7.2.

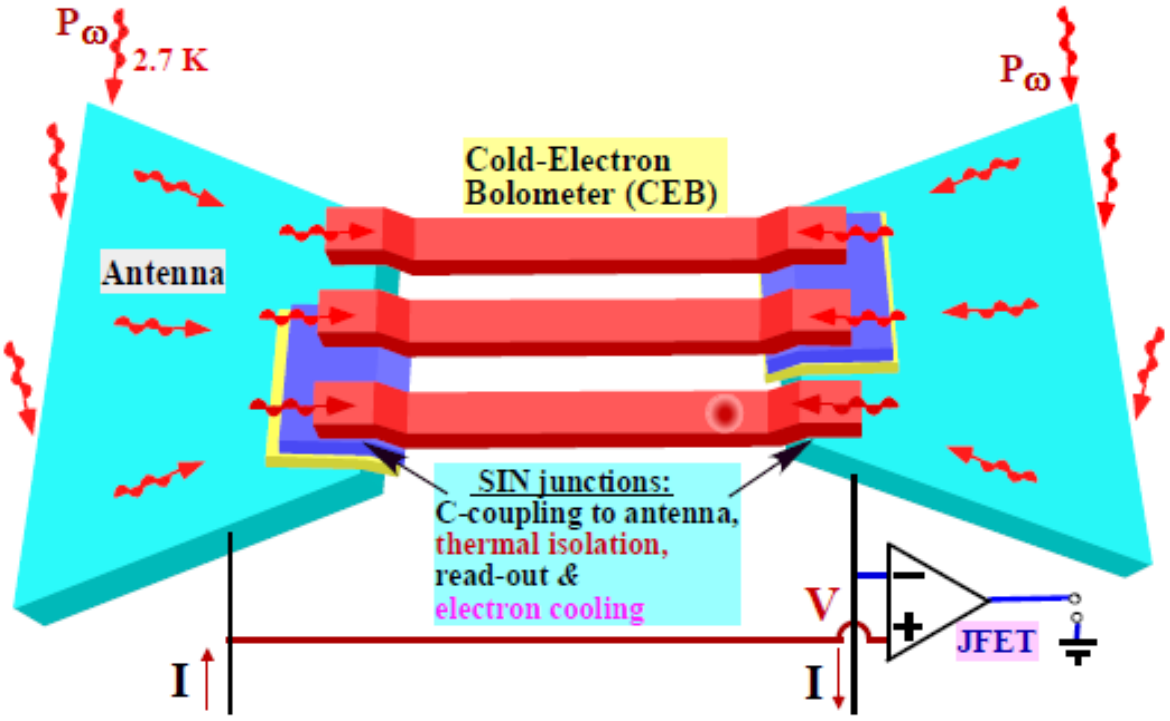


Figure 7.2. Schematic of three CEBs connected in a parallel / series array. Decoupling capacitors (blue) make AC connections between absorbers and the antenna; DC disconnected.

The parallel/series array shown in Fig. 7.2 can be represented by two equivalent circuits for DC and RF signal paths shown in Fig. 7.3 (top) and 7.3 (bottom), respectively. For a DC signal, tunnel junctions are connected in series with absorbers and are represented in the equivalent circuit in Fig. 7.3 by non-linear resistors. The decoupling capacitors are made with a thick oxide layer, which ensures that no tunneling can occur through the capacitors which are therefore considered as open circuits for DC signal. Therefore, for the DC signal, the array shown in Fig. 7.2 constitutes an array of normal absorber resistors in series with non-linear resistances of tunnel junctions, see Fig. 7.3, top.

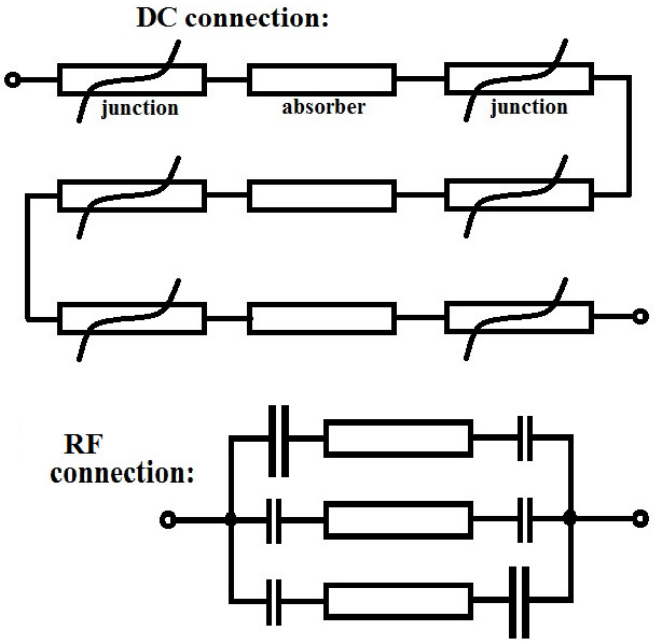


Figure 7.3. Equivalent circuit of a parallel/ series array for DC (top) and RF (bottom) paths.

For an RF signal in GHz range, both the decoupling capacitors and capacitance of tunnel junctions exhibit very low impedance, often negligible in comparison with that of absorbers. Therefore, for the RF signal, the array is represented by a parallel array of normal absorbers in series with capacitors, shown in Fig. 7.3, bottom. When tunnel junctions and decoupling capacitors are large enough to be considered as RF short at a given frequency, the capacitors in series with absorbers in Fig. 7.3 are regarded as zero impedance components in this equivalent circuit. An implementation of this approach is presented later in this chapter for CEB arrays integrated in a planar antenna operating at 350 GHz.

As to the production of CEB devices in an array, various fabrication methods can be used. CEB devices fabricated using a Direct-Write Trilayer technology [Papers I, II] for manufacturing Al-based SIN tunnel junctions and using Ti-based technology are presented in previous chapters. To optimize the CEB performance, new technologies were explored including the Advanced Shadow Evaporation technique proposed by Kuzmin [104]. CEB devices presented here and used for CEB arrays integrated in

planar antennas were fabricated using Advanced Shadow Evaporation that is a fabrication procedure based on depositing the normal absorber and oxidizing it prior to the superconducting electrodes.

The main innovation of the CEB array, in comparison with a single CEB [51], is the distribution of the power absorbed upon RF reception between several bolometers, which enhances the dynamic range. Effective distribution of power is achieved by a parallel RF connection of CEBs, which couple to the RF signal through capacitors (Fig. 7.2). For an individual CEB in an array of N devices, the absorbed power is reduced by the factor of N, which has certain advantages, such as:

(1) The background power is distributed among several absorbers, which enhances the sensitivity of the array; (2) the amplifier noise becomes less important, since the voltage response of the array is multiplied by N whereas its noise is only proportional to the square root of this number; (3) this reduces the RF power absorbed by each device and limits the overheating and saturation of the absorber, which substantially increases the dynamic range; (4) connecting several devices in series for DC connection (see Fig. 7.3) enables proper noise matching of the output impedance to the JFET amplifier.

At the same time, increasing the number of CEB devices in an array leads to an increase of the total absorber volume and consequently electron-phonon noise. For a parallel / series array presented here, an optimal number of 10 CEB devices was found, in which case the total noise of the detector approaches the photon noise of the incoming signal [65, 66, 74].

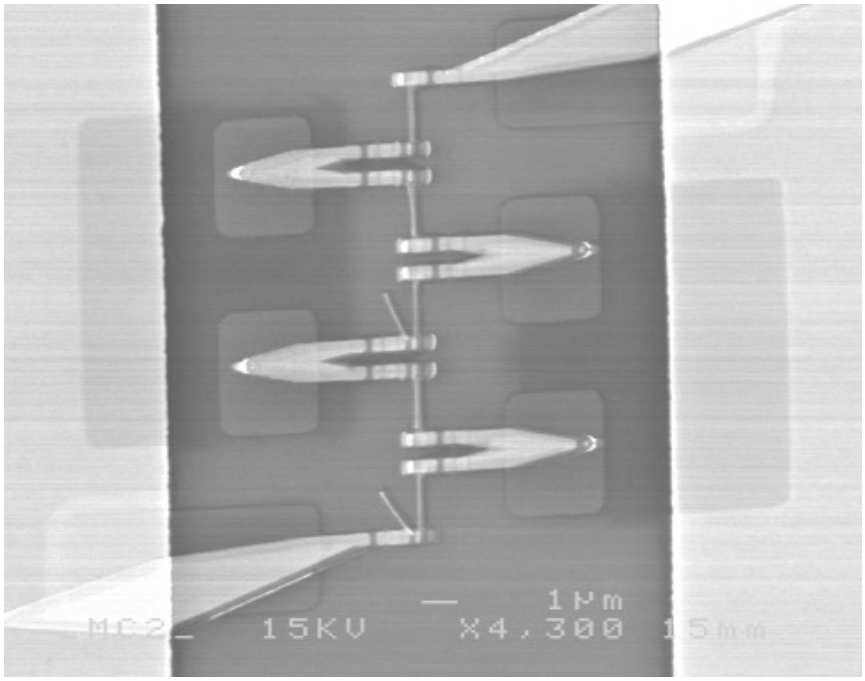


Figure 7.4. SEM image of an array comprising 5 absorbers and 10 SIN tunnel junctions [65]

In this work, two arrays with several CEBs integrated in orthogonal ports of a cross-slot antenna with a series connection for DC bias and a parallel connection for the RF signal were implemented for optimal performance, Fig. 7.4. The ratio of the resistance at zero bias voltage to the asymptotic resistance of over 3000 at 100 mK was achieved as a figure of merit for each array, which provides clear evidence of a good quality of tunnel barrier and proper measurement conditions with low levels of interference.

Also, 4-point test structures with two additional pairs of SIN tunnel junctions connected to each absorber strip were used for DC characterization of bolometers.

This approach is suitable for detector fabrication, which is confirmed in this chapter by demonstrating high performance IV curves and voltage response to the incoming RF power, including results of optical testing and also noise measurements for detectors fabricated using the Advanced Shadow Evaporation, with varying thickness of the tunnel barrier [65].

7.3 Chip design and fabrication

The samples presented have been fabricated using electron-beam lithography and Advances Shadow Evaporation technology for fabricating tunnel junctions proposed by L. Kuzmin [104]. As already stated, this procedure employs *in-situ* Al oxidation for the creation of the Al_2O_3 insulating barrier. The process involves two steps of deposition in one vacuum cycle: first, the normal Al absorber is deposited and oxidized, and then the Al counter-electrode is deposited.

The layout design of CEB arrays was optimized for CMB and foregrounds polarization measurements with balloon-borne telescope projects in a frequency band around 345 GHz. The bolometer arrays integrated in a cross-slot antenna were placed at the center of a 7×7 mm chip on a thermally oxidized Si substrate with a 400 nm thick SiO_2 layer. There are 32 chips on a single 2-inch Si wafer, and several wafers were produced using nearly the same fabrication procedure. The layout of the antenna is based on a cross-slot antenna design [105]. This is a slot antenna consisting of two pairs of slots (a pair for each polarization component), i.e. 4 slots in total. Based on published data and the previous experimental results, the bandwidth of that CEB-antenna integrated circuit is estimated to be around 100 GHz.

Each orthogonal array consists of 10 CEB devices connected in series for DC bias and DC readout. An optical image of the antenna is shown in Fig. 7.5. The dark narrow slots in Fig. 7.5 are covered with an AlO_x/Al capacitive layer, thus making capacitive coupling between the two CEB arrays. Each port of the antenna contains 5 CEBs detecting signals with the same polarization, thus making an array of 10 CEBs for vertical polarization and 10 CEBs for horizontal polarization components. The SIN tunnel junctions for the CEB devices were made of CrAl/AlO_x/Al trilayer, in which the first Al layer is made of non-superconducting Al and then oxidized to form

a thin oxide barrier. This structure was deposited according to the Advanced Shadow Evaporation scheme for CEB fabrication [104]. A detailed SEM view of a half of an array with 5 absorbers and 10 tunnel junctions is presented in Fig. 7.4. In this view, two CEB devices on the left and two devices on the right of the absorber are coupled capacitively, similarly to the capacitors shown in Fig. 7.2.

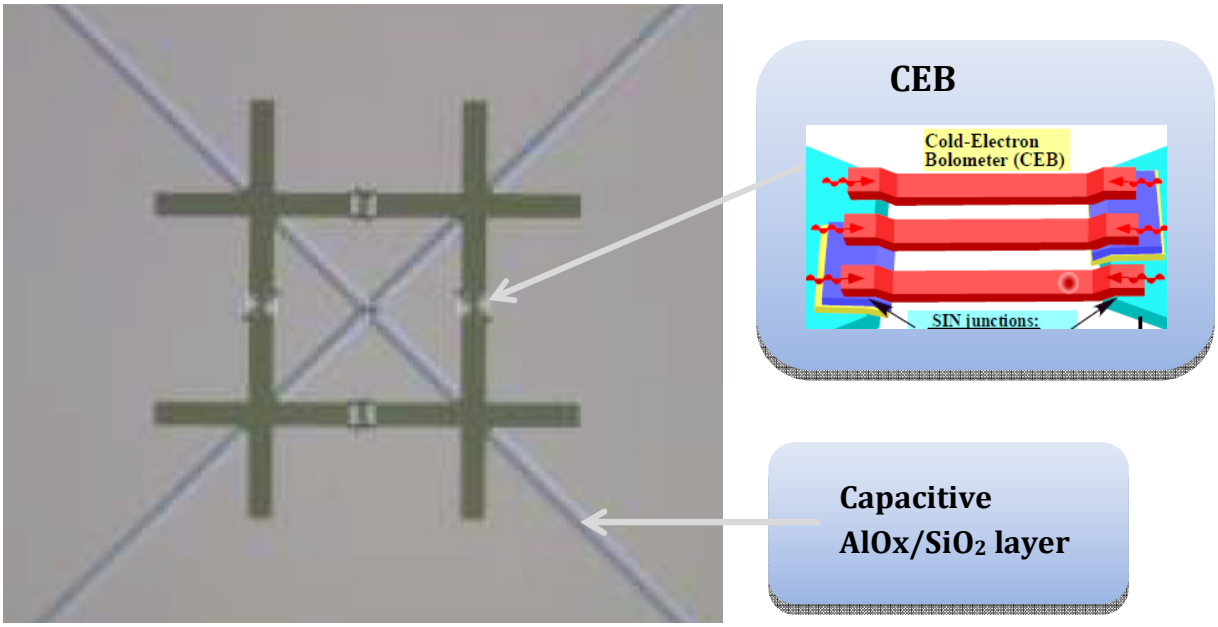


Figure 7.5. Optical image of a cross-slot antenna with CEB arrays (inset).

This chip comprising two CEB arrays integrated in the cross-slot antenna can be coupled to the free space using an extended hyperhemispherical Si lens or with a horn for simple measurements with a cold radiation source. The lens or the horn faces the optical window, and two filters are placed in the signal path, in order to prevent overheating by IR radiation. These filters, shown in front of the Si lens in Fig. 7.6., provide attenuation of ~10 dB above the cut-off frequencies of 3 THz and 1 THz. Additional protection was attained using neutral density filters (NDF) with attenuation of about 6 dB, which resulted in no visible overheating of the cold stage or reduction of the hold time observed.

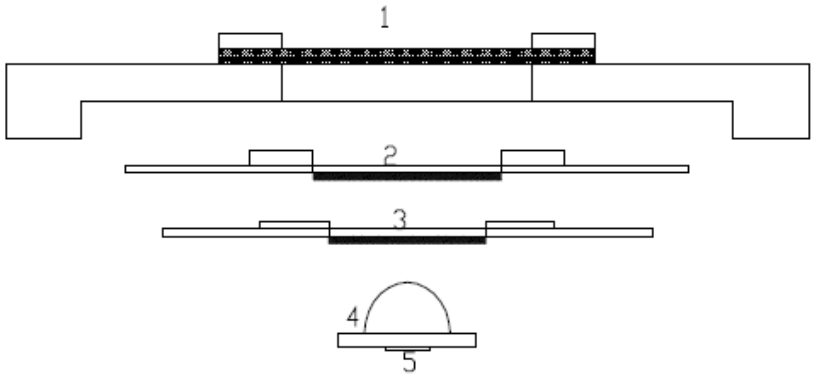


Figure 7.6. Schematics of the quasioptical beam path in the cryostat.
(1) - Teflon window, (2) - first filter, (3) - second filter, (4) – Si lens, (5) –detector chip.

7.4 Experimental characterization of CEB arrays

First, DC characteristics of the fabricated CEB devices were measured by applying a bias current and measuring the voltage across each array. High performance IV curves were obtained, which is an indication that this technology is suitable for detector fabrication. The topology of the readout system used in this experiment was described earlier in the Chapter 5 and the circuit schematic is shown in Fig. 5.5. The IV characteristics of an array of 10 cold-electron bolometers and the voltage response to temperature are shown in Fig. 7.7. The dynamic to normal resistance ratio of the fabricated devices of up to 1000 was measured. The voltage shown in this graph is the total voltage across the whole array so the superconducting gap observed represents the sum gap voltage of the SIN junctions in the array.

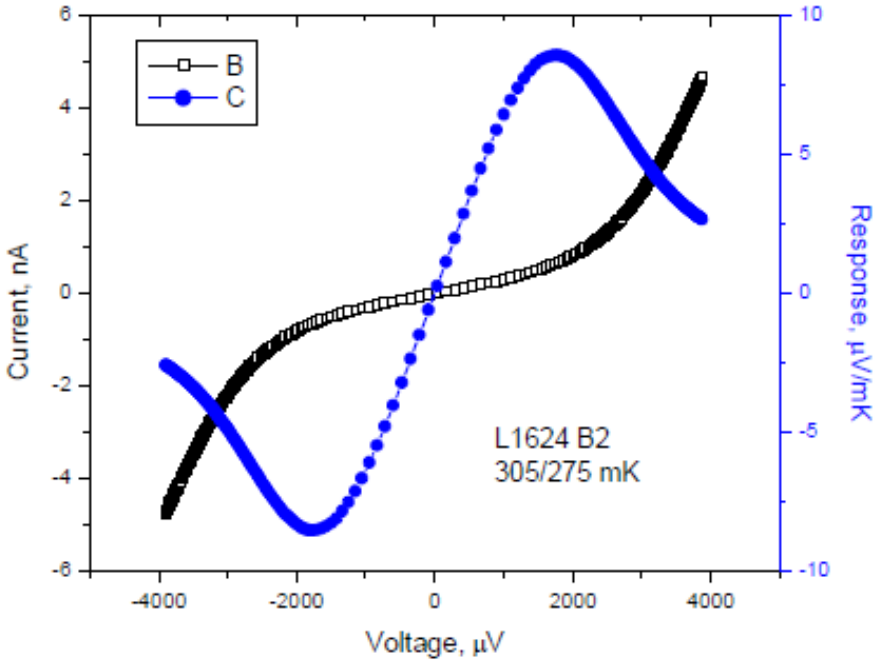


Figure 7.7. IV curve and voltage response to temperature difference 305-275 mK, r_d/R_n ~500.

The voltage across an array at a bias current of 0.1 nA and the dynamic resistance at zero DC voltage are plotted as a function of temperature in Fig. 7.8. The maximum voltage response to the temperature obtained in this experiment was 8.8 μV/mK [65].

In the next experiment with calibrated RF signal incident onto the CEB, a rotatable holder was installed inside the cryostat with a reflecting Cu foil screen and an NDF at 3 K, similarly to the hot-cold experiment described in the Chapter 6. An external magnet is used to rotate the holder with the cold CEB device in the cryostat. In this way the CEB detector can be positioned to face a blackbody source (NDF) at 3 K or a reflecting surface, effectively at ~300 mK. A photo of this setup demonstrated at room temperature is presented in Fig. 6.7; the measured voltage response versus bias voltage is shown in Fig. 7.9.

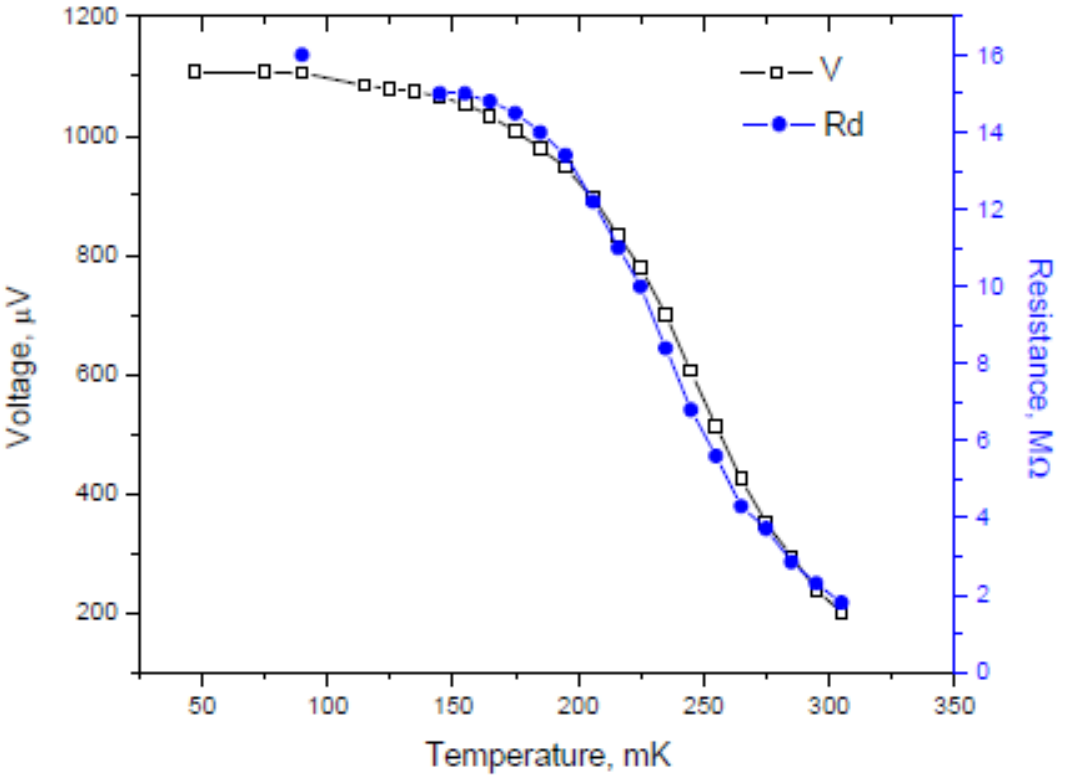


Figure 7.8. Voltage across an array of 10 CEBs versus temperature at bias current 0.1 nA. The maximum responsivity is 8.8 μV/mK. [65]

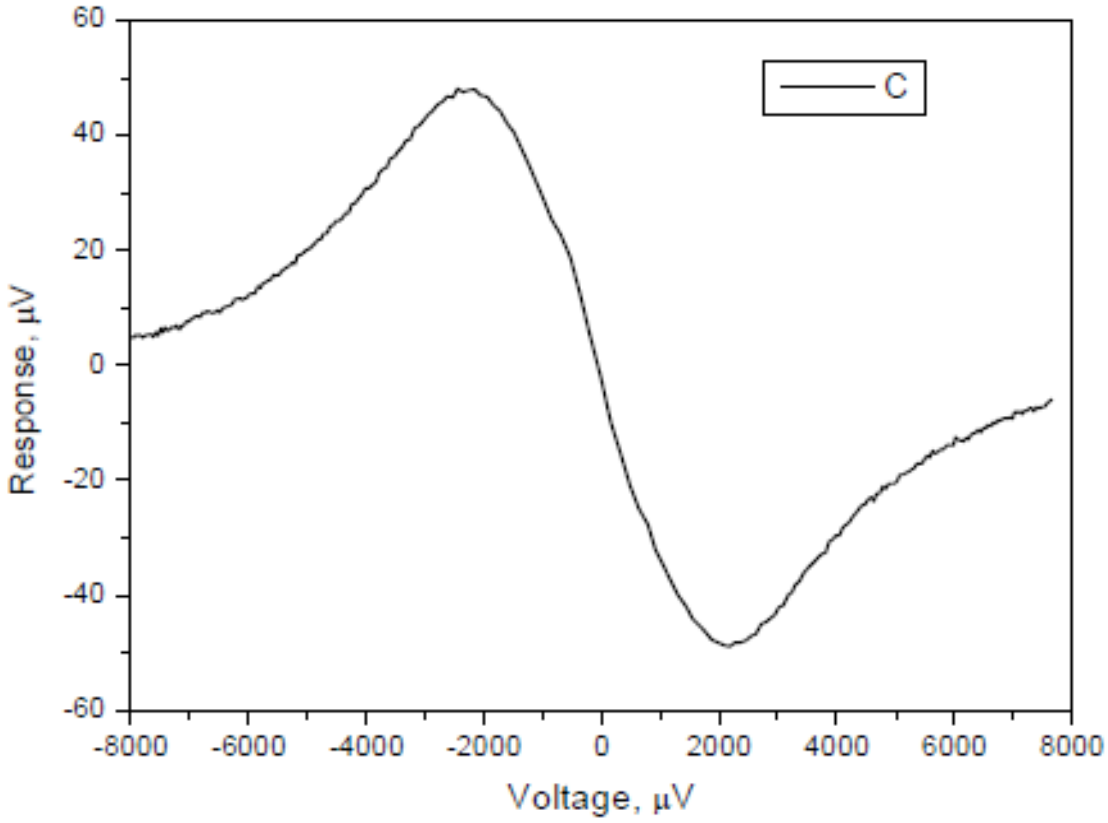


Figure 7.9. Voltage response to swapping the RF source illuminating the detector from reflecting Cu foil (T=300 mK) to an NDF emitter at 3 K. [65]

To estimate the NEP, the output noise of the array was measured using a MOSFET OPA111 instrumentation amplifier as the input stage integrated circuit. The optical NEP can be estimated, relying on the data presented in Fig. 7.9. Considering the CEB-antenna integrated circuit as a single mode detector, the incident radiation power δP with the Planck formula for such a detector can be calculated [98]. For a frequency range around the frequency of f = 350 GHz within a bandwidth of a cross-slot antenna of δf = 100 GHz, the power emitted by a black body at a temperature of T = 3 K is given by [98]:

$$\delta P = \frac{\kappa \cdot hf \cdot \delta f}{e^{hf/k_B T} - 1} = 1.1\times10^{-13}\ \text{W},$$

where h is Planck's constant, k_B is the Boltzmann constant, κ=1 is the emissivity of the black body source, assuming that the effective RF bandwidth is 100 GHz. The RF power for a source at 300 mK is well below 10^{-15} W and can therefore be neglected. Thus, the difference in RF power values for source temperatures of 3 K and 300 mK yields $\Delta P = 1.1\times10^{-13}$ W. Considering a voltage change of 50 µV for this RF power difference, the voltage to temperature responsivity can be calculated:

$$S = dV/dP \approx \Delta V/\Delta P = 5\times10^{8}\ \text{V/W},$$

The optical NEP is obtained by dividing the total voltage noise of v_n = 11 nV/Hz$^{1/2}$ by the voltage to power response:

$$NEP = \frac{v_n}{dV/dP} = 2.2\cdot10^{-17}\ \text{W/Hz}^{1/2}.$$

Advantages of connecting bolometers in an array and electron cooling can be demonstrated by optical measurements of the dynamic range of the array using e.g. a Backward Wave Oscillator (BWO) as an RF power source. The oscillator operates in a frequency range of 250-380 GHz for anode voltages in the range of 1100 to 3800 V. A calibrated polarization grid attenuator was used for accurate control of the incident power. Inside the cryostat, a 20 dB NDF cold attenuator was mounted at the optical window, and the cold rotatable stage with the reflective Cu surface and an NDF was used [65]. A photo of the setup is presented in Fig. 7.11.

In this experiment, a dynamic range over 40 dB was demonstrated. The dependence of the measured output voltage on the incident RF signal in terms of attenuation is presented in Fig. 7.12. Considering the lower boundary of the signal level equal to an amplifier noise of 11 nV/Hz$^{1/2}$ and the saturation level as presented in Fig. 7.12 of 200 µV, a full dynamic range of the bolometer array of about 43 dB can be obtained. This is also consistent with the range between 0.2 µV and 200 µV for the voltage response for the B1 array in Fig. 7.12. The dynamic range obtained for CEB arrays is rather high, compared with that of the TES detectors, typically several dB.

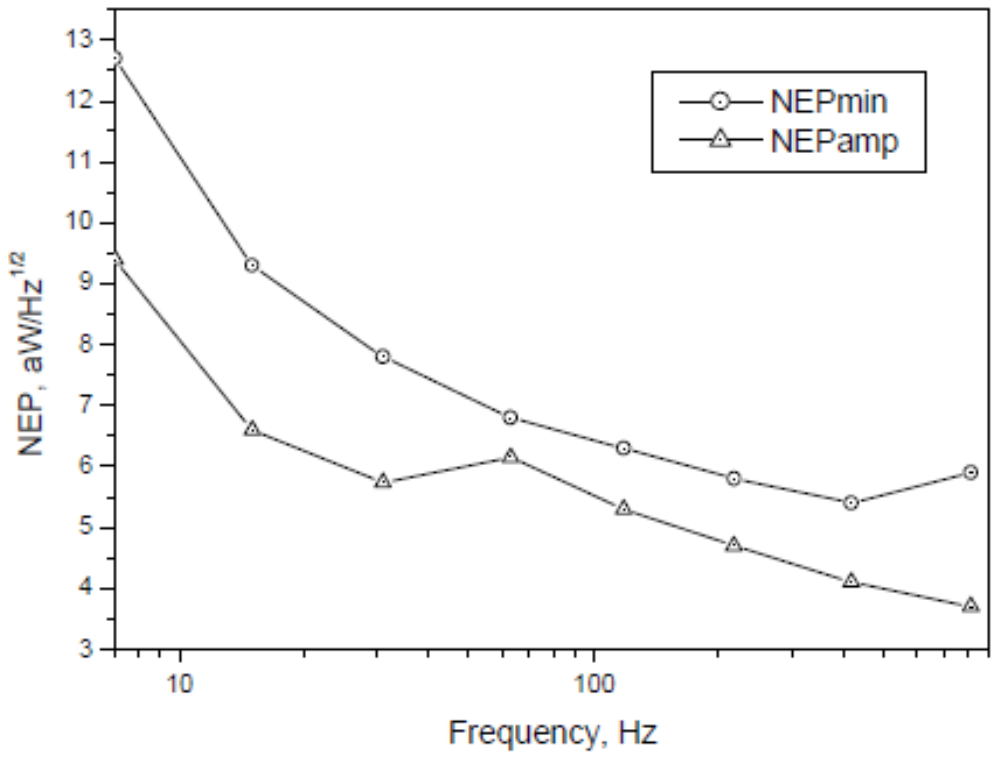


Figure 7.10. The minimum Noise Equivalent Power (NEP) and contribution of amplifier [65]

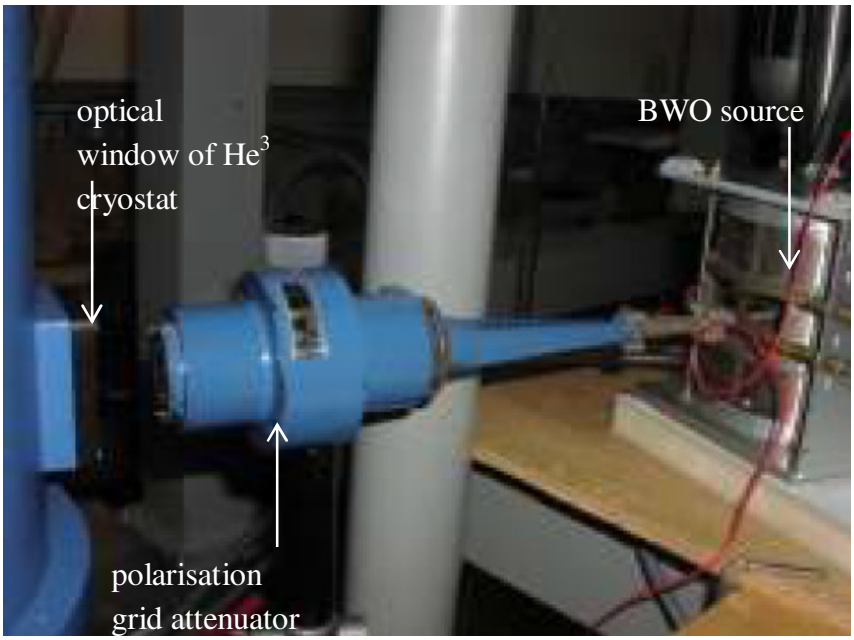


Figure 7.11. Measurements of the CEB array dynamic range: The BWO oscillator (to the right), the polarization grid attenuator (in the center), and the optical window of the ^{3}He cryostat (to the left) [65]

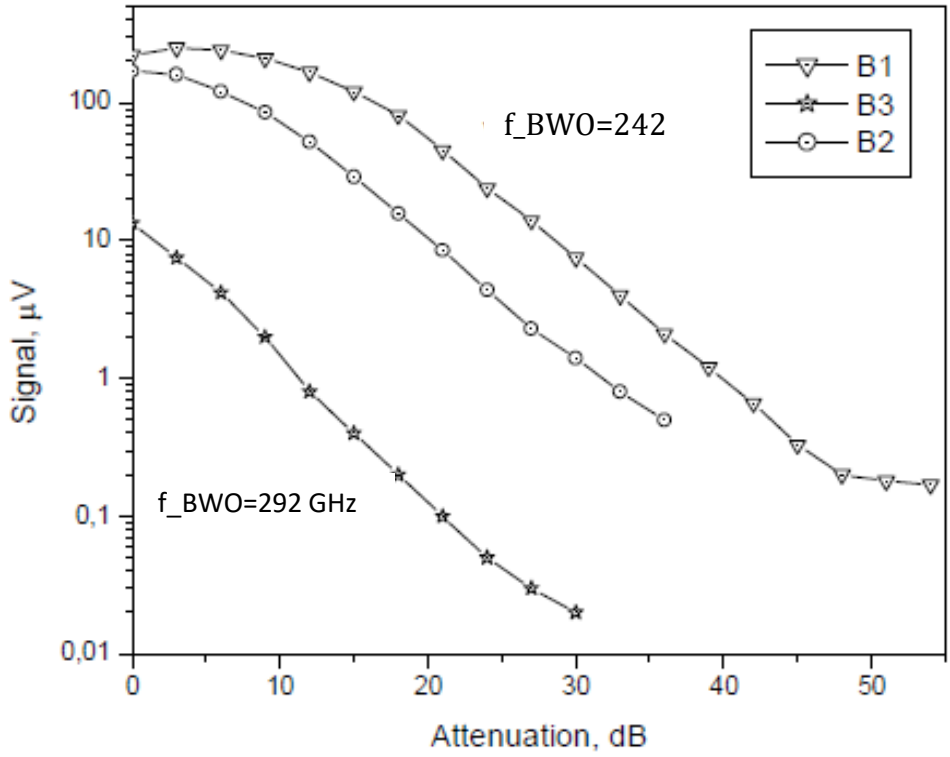


Figure 7.12. The output voltage versus the attenuation of the incoming ~300 GHz signal. B1, B2 – arrays for vertical and horizontal polarization components, B3 – "4-probe" structure.

7.5 Experiments on DC response and electron cooling using a 4-junction test structure

In this section, experiments on a set of bolometric devices fabricated in a similar way using the same technology are presented; the chip layout (Fig. 7.13) includes bolometric devices implemented in 4-probe test structures consisting of 4 SIN junctions and an absorber, similar to the one described in the Chapter 6. The device is essentially a bolometer with two additional electrodes connected to the absorber though SIN tunnel junctions, which enables for proper 4-point measurements.

I-V curves were measured and logged at several bath temperatures between 286 mK and 356 mK, and a voltage to the temperature response, $S_{V/T} = dV/dT$ was obtained for these devices by subtracting the I-V curves at different bath temperatures. For a 4-junction structure shown in Fig. 7.13, the voltage across two junctions at 0.12 nA and 0.25 nA bias current was measured as a function of temperature. Voltage across two junctions in series versus temperature at a fixed bias current for a 4-junction bolometer structure is shown in Fig. 7.14.

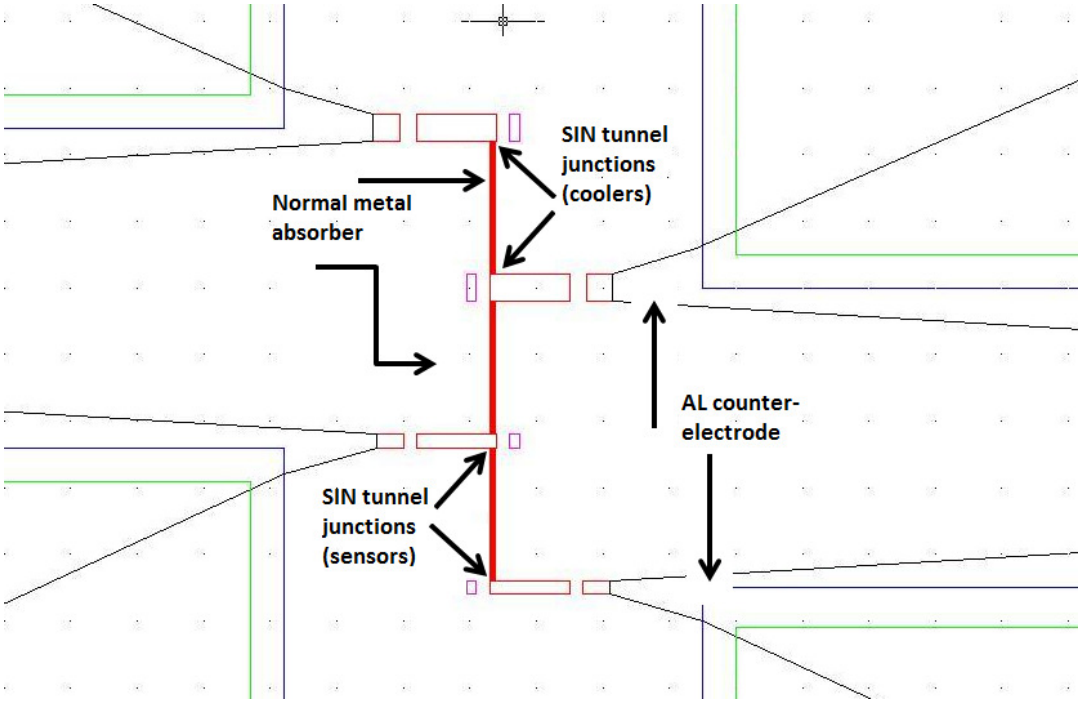


Figure 7.13. Layout of a 4-probe bolometer made of a normal absorber and 4 SIN junctions

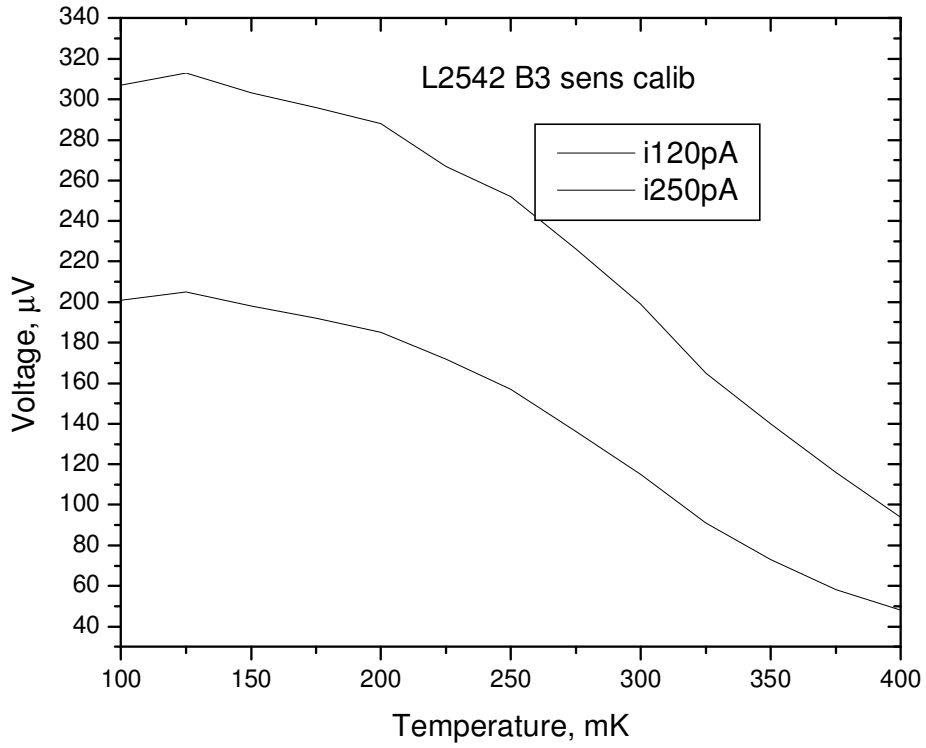


Figure 7.14. Voltage across two sensor junctions at bias currents of 0.12 nA and 0.25 nA versus bath temperature

Next, a voltage response as an indication of the reaction of the bolometric device on Joule heating was measured for a 4-junction structure. The response to DC heating was measured by applying a bias current flowing through two tunnel junctions in series in a 4-probe test structure (Fig. 7.13) and measuring the DC voltage across the other two junctions. The results of this experiment are shown in Fig. 7.15.

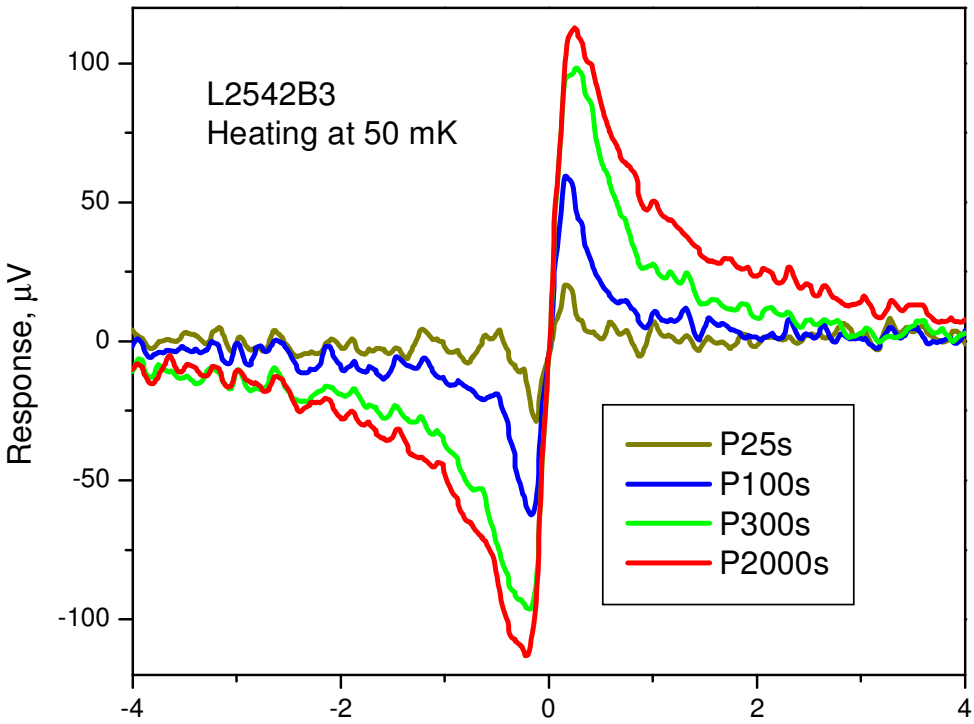


Figure 7.15. Voltage response of an absorber in a test structure to DC power dissipated in the absorber by applying bias current. Different curves represent response to 4 different values of DC power dissipated in absorber: 25 fW, 100 fW (blue), 300 fW (green) and 2000 fW (red).

In the next experiment, the same 4-junction test structure was employed for measuring the electron temperature, which allowed observing the electron cooling, using SIN junctions of different areas. Two of the SIN junctions in the device (called coolers) operate in electron cooling mode, while the other two junctions of smaller area (called sensors) were used as thermometers, by measuring the voltage across these junctions and thus the absorber temperature. The schematic diagram of the setup of this experiment including cooling and sensing junctions is shown in Fig. 7.16.

The area of the cooling junctions was 0.48 μm^2, while the sensor SIN junctions used as thermometers had an area of 0.24 μm^2 each. A photo of such a structure is shown in Fig. 7.17.

IV curves of the cooling SIN junctions measured at different temperatures are shown in Fig. 7.18; the sensor voltage versus the phonon temperature at fixed bias current in Fig. 7.14; while voltage across the SIN thermometer versus the SIN cooler voltage are shown in Fig. 7.19 and Fig. 7.20, respectively.

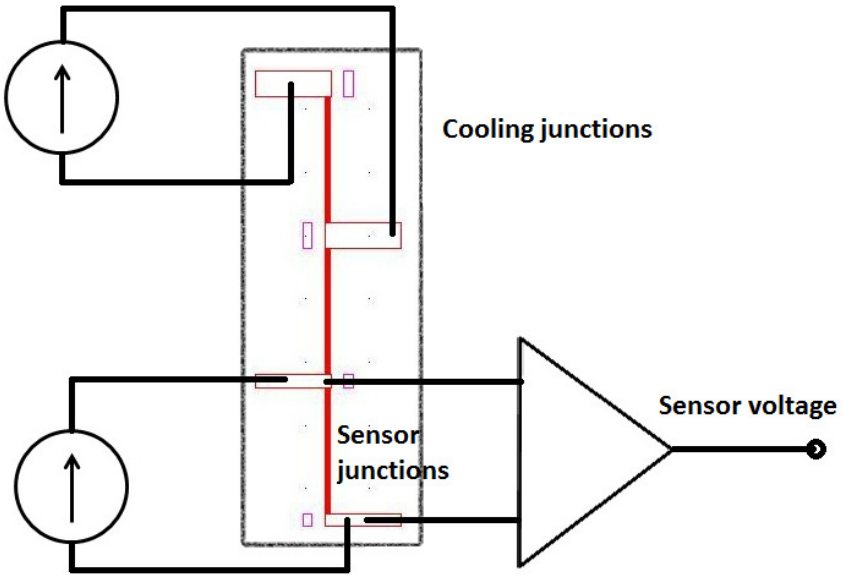


Figure 7.16. Schematic diagram of the cooling experiment. The top 2 junctions cool the absorber when bias current is applied; voltage across 2 sensor junctions (bottom) is measured.

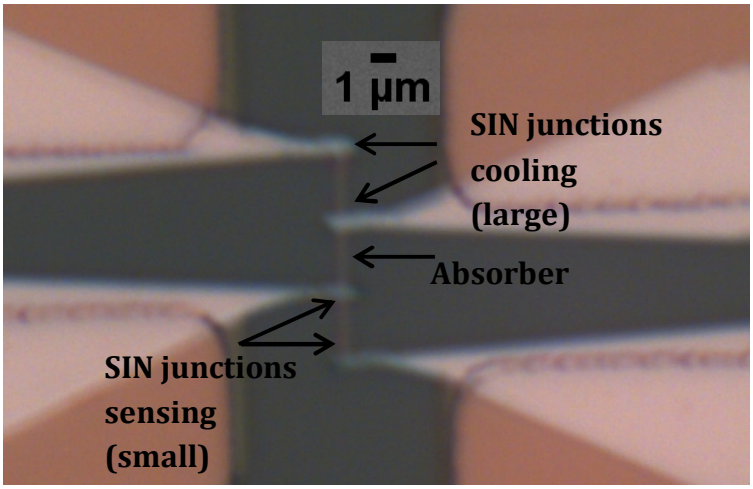


Figure 7.17. An optical image of a 4-probe bolometer structure.

The electron cooling by ~100 mK observed in Fig. 7.19 can be considered as an underestimate because of electron heating in the SIN thermometer at low bias voltages, which can also be seen in Fig. 7.19. In addition, the coolers and the sensors are located at different ends of a 7 µm long absorber, which results in a temperature gradient between these two points so the absorber temperature near the cooling junctions will be below that near the sensor that also heats a part of the absorber. Therefore, it seems desirable to estimate the electron cooling relying on the IV curves of the cooling junctions.

As can be seen in Fig 7.18, the effect of electron cooling modifies the shape of the IV curve, due to decrease in the electron temperature near the gap. The device is also affected by the electromagnetic radiation and interferences that may cause the heating

of the electron system and, as a result, regions with an electron temperature different to the phonon temperature can be represented in the IV curve.

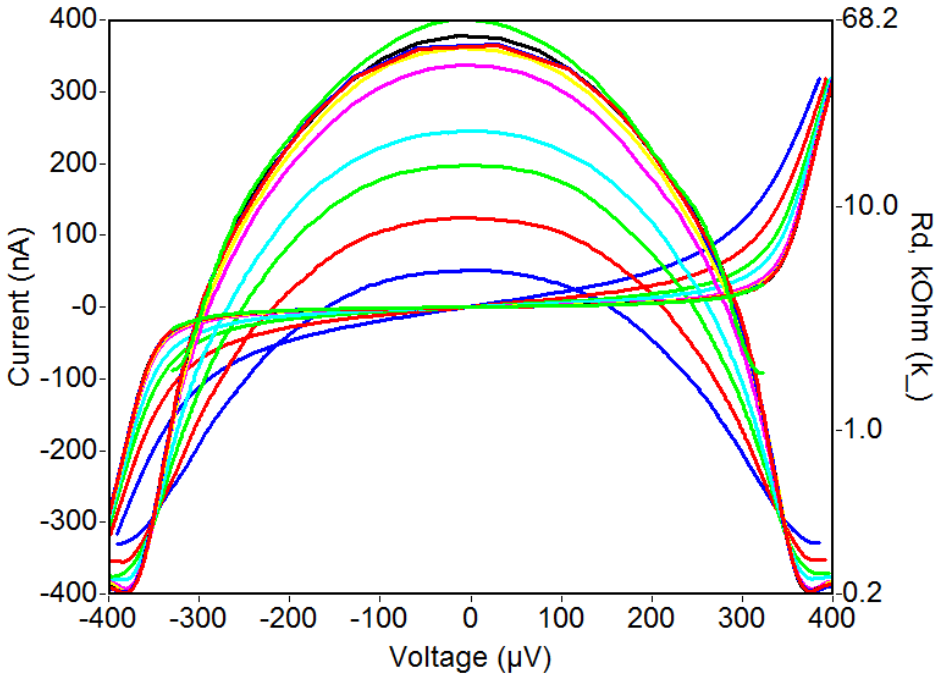


Figure 7.18. Family of IV curves of cooling SIN junctions at temperatures of 120 to 550 mK and the dynamic resistance versus bias voltage; Colors represent different temperatures.

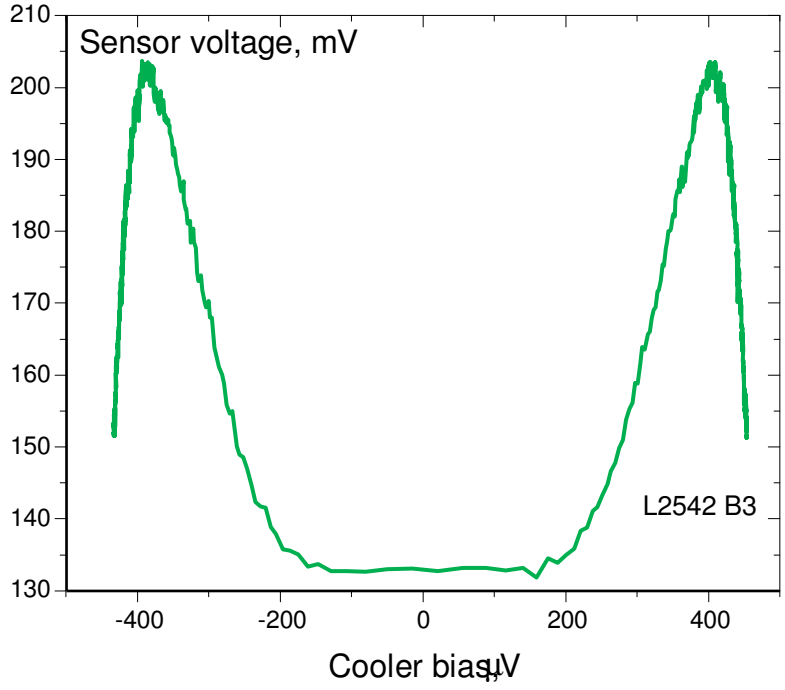


Figure 7.19. Sensor voltage versus the bias voltage across cooling junctions. At low bias voltages the temperature is close to the bath temperature of 280 mK, while at maximum cooling it can be estimated as ~100 mK according to the curve in Fig. 7.14.

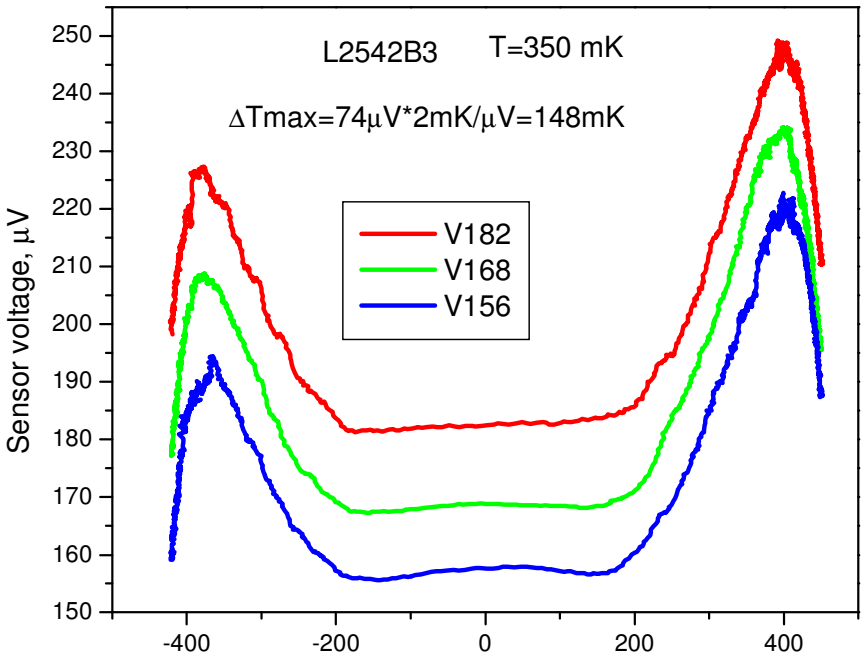


Figure 7.20. Example of electron cooling at 320 mK.

These processes could be described by the thermal balance equation:

$$\Sigma\lambda\left(T_e^5 - T_{ph}^5\right) + P_{SIN}(V, T_e, T_S) + C_\lambda \frac{dT}{dt} = \frac{P_0}{N} + \frac{V^2}{R_S}$$

where $\Sigma\lambda(T_e^5 - T_{ph}^5)$ is the heat flow from the electron system of the normal metal to the phonon system, Σ is the material parameter of the absorber, λ is the volume of the absorber, T_e and T_{ph} are the electron and phonon temperatures of the normal metal; $P_{SIN}(V, T_e, T_{ph})$ cooling power by SIN junctions; C_λ is the heat capacity of the normal metal; P_0 is the background power load, and V^2/R_S is the heat load due to the leak resistance R_S. The accuracy of such a modeling is rather low, as several parameters are included that are not possible to determine independently and exactly, such as the material parameter, effectiveness of electron cooling, heat capacity of the normal metal, background power load, effectiveness of the heat sink in the superconductor etc. In addition, the definition itself of the electron temperature becomes incorrect, because the energy distribution of the electron becomes different to the Fermi distribution. The number of electrons with energy above the Fermi level in the case of electron cooling turns out to be substantially less than that for the equilibrium state, while when heated by the incoming photons with energy higher than the superconducting gap, this number is considerably more than in the equilibrium. Hence, an equivalent electron temperature could be considered that can be defined as the temperature of the SIN junction in the equilibrium at which the same differential

resistance is observed at the same bias voltage or current. Estimated equivalent electron temperature for many different bias points can be plotted versus the bias voltage, which can be done for IV curves at different temperatures. Three curves representing the equivalent electron temperatures versus bias voltage are shown in Fig. 7.21 for the phonon temperature values of 540, 380, and 260 mK.

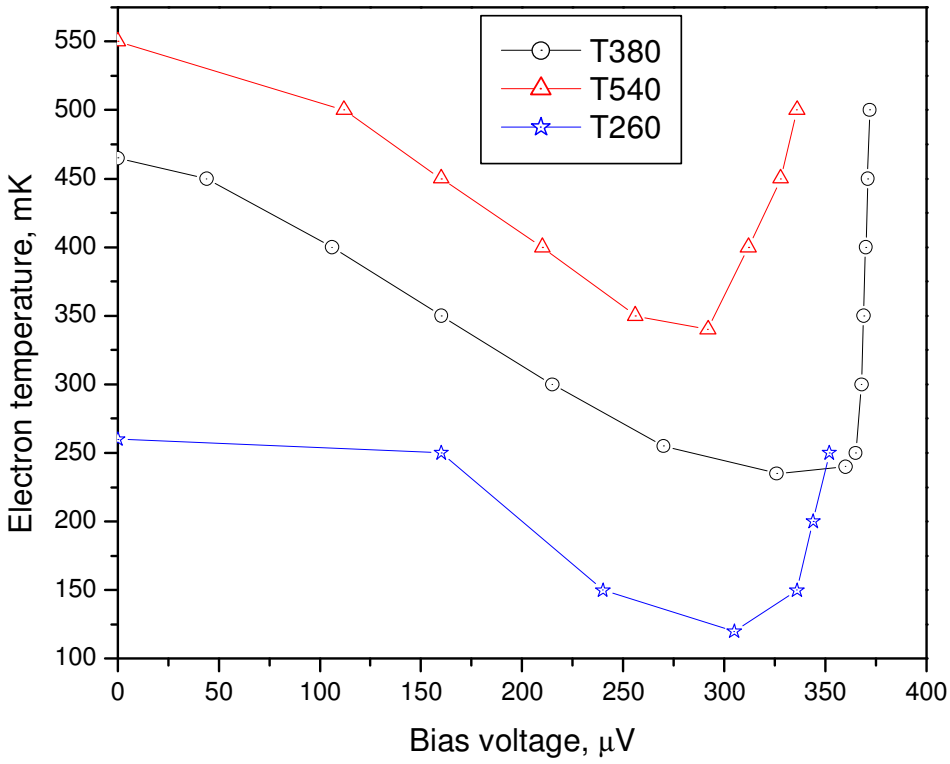


Figure 7.21. Equivalent electron temperatures versus bias voltage at phonon temperatures of 540, 380 and 260 mK.

In Fig. 7.21, when shifting the bias point from zero voltage towards the gap, some cooling is observed which corresponds to the cooling power of 0.4 pW at the base temperature of 380 mK; at 540 mK the maximum cooling power amounts 0.9 pW, while at 260 mK it is reduced to 20 fW. In general, the cooling power can be expressed by the formula [106]:

$$P_c = \frac{\sqrt{2\pi\Delta kT}}{2eR}\left(\frac{\Delta}{e} - V\right)\exp\left[-\frac{\Delta - eV}{kT}\right]$$

Due to the exponential decrease of the cooling power with the decreasing base temperature, obtaining electron temperatures below 100 mK using Al-based SIN junctions with a gap of around 200 μV is a challenge. Even small overheating by interference currents or background radiation will obstruct cooling down to 100 mK.

In order to increase the cooling power, a superconductor with a gap of 60 – 80 μV must be used instead of Al.

The increased electron temperature at zero bias can be explained by a process of tunneling of hot quasi particles from the superconductor to the normal metal because the density of quasiparticles above the gap exceeds the density of electrons in the normal metal. As a result, hot quasiparticles leave the superconductor and tunnel to the normal metal, which results in the electron temperature of the normal absorber becoming higher than the phonon temperature.

7.6 Conclusions

In this chapter, the measurement results of a Cold-Electron Bolometer array deposited across a cross-slot antenna on a planar substrate have been presented. The devices have been fabricated using the Advanced Shadow Evaporation technique, with the absorber deposited prior to the superconducting counter-electrodes. The detector is a potential candidate for the next space cosmology missions and is also of interest to ground-based experiments as a result of its sensitivity, the simplicity of its integration to planar circuit technology, high saturation power and fast response.

Cold electron bolometer arrays integrated in a cross-slot antenna were tested in a ^{3}He sorption pump refrigerator within a temperature range around 0.3 K. The optical response was measured by positioning the detector chip to face a blackbody source at 3 K or a reflecting surface, effectively at ~300 mK. The estimated noise equivalent power in the current biased mode as read out by room temperature electronics amounts the NEP of $2.2 \cdot 10^{-17}$ W/Hz$^{1/2}$. A dynamic range over 40 dB and voltage to temperature response of dV/dT = 8.8 μV/mK were measured at about 280 mK for an array of Cold-Electron Bolometers integrated in a cross-slot antenna. Electron cooling by 45 to ~100 mK was demonstrated, which improves the NEP of such a detector and increases its dynamic range. The measured characteristics approach the requirements for balloon-borne experiments, and CEB devices could be considered for future balloon and ground-based radio telescope experiments.

Chapter 8
Semiconductor plasmonic detectors for THz imaging

Among other types of sensors, semiconductor plasmonic detectors display very high sensitivity and reliable operation and are therefore widely used for various applications. In particular, very good noise performance has been reported for such devices, with noise equivalent power levels NEP ~10^{-17} W/Hz$^{1/2}$. Detectors relying on plasma waves excitations are able to perform resonance operation with a spectral resolution below ~50% and potentially approaching 1% for certain types of detectors [36], [Paper VII].

8.1. Introduction to plasmonic detectors

Quantum dots (QD), point contacts (PC), and single electron transistors (SET) are the components used to build the THz detector systems presented here. QDs have a well defined excitation spectrum of plasmons upon absorption of the THz photons with a typical energy of several meV; the SET and the PC have high charge sensitivity, better than 10^4 e/Hz$^{1/2}$ at low temperatures, which allows using combination of these devices for construction of sensitive THz detector [107, 108]. In this chapter, a coupled system of QD, PC, and metallic SETs utilized for terahertz detection is investigated. The SET and the PC are able to sense the state of charge of the QD that is modulated upon absorption of the terahertz photons. This property can be used for detection of electromagnetic radiation in the terahertz frequency range. Single photon counting with the SET-QD detector was reported earlier [109]; the PC-QD detector is less sensitive than that with SET, but its fabrication is less technologically demanding, and it has the advantage of a higher operation temperature [36]. The

photo sensitive operation of these devices is strongly dependent on the operation point. In the samples presented here, SET-QD and PC-QD devices are both implemented in one system, in order to investigate electrostatic effects of the devices and compare their performance, see Fig. 8.1.

The samples consist of a mesa patterned channel in GaAs/AlGaAs heterostructure with two metal gates, namely a PC gate and a QD gate, and an SET on the top of the QD, see Fig. 8.1. The hetero-structure has been grown by molecular beam epitaxy. The layer sequence is 0.4 μm super-lattice GaAs/$Ga_{0.3}Al_{0.7}As$ buffer, 20 nm GaAs well, 20 nm $Ga_{0.7}Al_{0.3}As$ barrier layer, 60 nm $Ga_{0.7}Al_{0.3}As$ doping layer with a Si concentration of 1×10^{18} cm^{-3}, and 10 nm undoped GaAs layer. The two-dimensional electron gas (2DEG) has been created 90 nm below surface in a GaAs well. It has carrier concentration of $n = 3.7\times10^{11}$ cm^{-2} and mobility of $\mu = 1.2\times10^{5}$ cm^2/Vs at the temperature of 4.2 K. The QD is formed in 2DEG by negatively biased QD gate. An Aluminium SET is fabricated above the QD using two-angle shadow deposition technique, which includes oxidation between depositions of two Al layers at different angles [110].

8.2. The operation principle of the sensors

The principle of the operation was originally introduced in experiments on photon counting of radiation in terahertz region using quantum dots (QD) in high magnetic field [111] and further developed and described in detail in later works [36]. Absorption of photons with terahertz energy could excite plasma oscillations in a resonant way, followed by charge excitation of the QD that could be sensed by an SET. A spectral resolution of such a device is ~30 %; in magneto-plasmon devices, it can be reduced to ~2 % when a QD is placed in the magnetic field, so that magneto-plasmon oscillations are excited.

8.2.1. QD Devices based on point contact and SET

In this chapter, the operation of a system is investigated, where quantum dot (QD) and point contact (PC) defined in a high-mobility two-dimensional electron gas of a GaAs/AlGaAs heterostructure are capacitively coupled to each other and to a single electron transistor (SET). Accordingly, two modes of the device operation are considered here, in which the state of charge of the QD can be sensed either with the PC or the SET.

The QD is defined in a mesa channel by applying negative bias voltage to the QD gate, see Fig. 8.1. The mesa channel is created in the focal point of a planar log-periodic antenna about 1.5 mm in diameter made of gold deposited on the top of the heterostructure. The antenna is designed to operate in the frequency range between

0.2 THz and 2 THz. An aluminum SET is fabricated straight above the QD. Once the QD is charge excited by sequence of processes, namely: absorption of the photon – excitation of the plasma waves – decay of plasma waves with excitation of the electron from the QD, the potential of the QD is changed.

Because of capacitive coupling between the QD and the SET, this results in a shift of the Coulomb Blockage Oscillations (CBOs) of the SET by $\Delta V_g = \frac{V_{CBO} \times C_{QD}^{SET}}{C_{\Sigma}^{QD} + C_{QD}^{SET}}$.

This implies changes in the SET current at fixed voltage value, which can be detected. Here, V_{CBO} denotes the period of CBO oscillations in terms of gate voltage, i.e. the difference between two voltage values corresponding to two peaks of SET current.

In order to function with the PC, both the QD and PC gates are negatively biased so a narrow conductance channel is created in 2DEG. A voltage of 0.25 mV is applied across the PC in series with a 200 kΩ resistor. The current of the PC is sensitive to the state of charge of the QD due to the field effect, and the photo response is seen as a variation of the PC current.

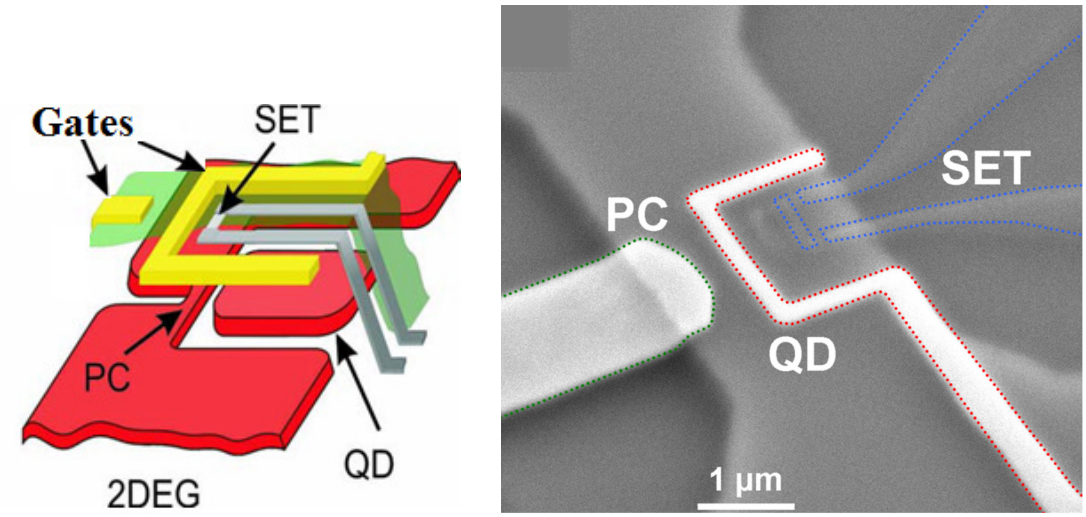


Figure 8.1. (Left) Schematic view of components; QD is formed in 2DEG and probed by a SET or a PC. (Right) SEM image of THz quantum dot sensor consisting of a QD coupled to SET and PC. Dotted lines denote the QD gate (green), the SET (blue), and the PC gate (red).

8.2.2. Electrostatic model with equivalent capacitances

An electrostatic model of the system is investigated in this chapter, and the sensitivity of the point contact and the SET to the charge excitations of the quantum dot are derived from this model. In the electrostatic model, different elements of the system are capacitively coupled to each other, which is reflected in the equivalent circuit shown in Fig. 8.2. In this configuration, equivalent capacitors represent connections between SET, PC, and QD, as well as from these components to the external electrodes and to the ground, see Fig. 8.2.

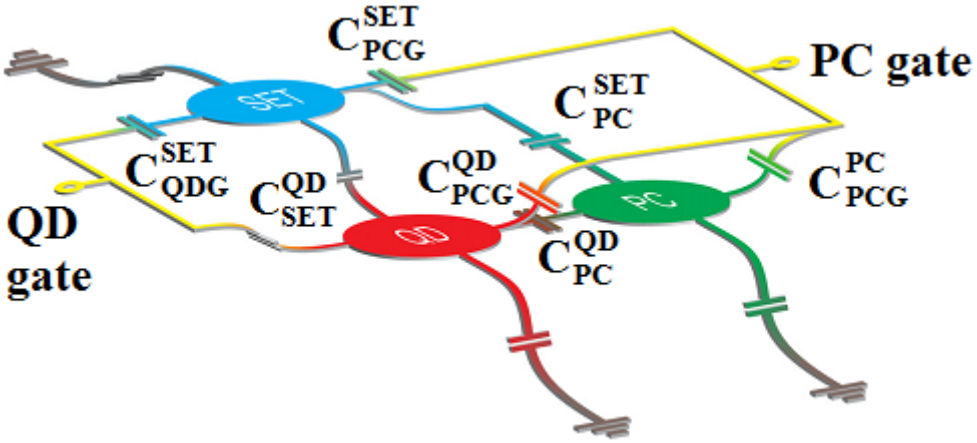


Figure 8.2. Equivalent circuit of the device, based on Electrostatic Model.

8.2.3. IV characteristics of the devices

In devices operating in the PC probe mode, negative bias voltage is applied to the gates, and the conductance $G = I_{SD}/V_{SD}$ of mesa channel is measured; see Fig. 8.3 (a). In the intensity plot, individual curves $G\ (V_{QD})$ are shown, measured at constant voltage applied to the PC gate, V_{PC}, while sweeping the voltage, applied to the QD gate, V_{QD}. Pinch-off in the channel occurs when high negative bias voltage is applied to both gates. Some asymmetry in the pinch-off boundary is observed, due to difference in the PC and QD gate's geometry. The slopes of the pinch-off boundary are identical in regions A and C, while becoming larger in region B, as an indication of higher sensitivity of the PC conductance to the QD gate voltage in that region, Fig. 8.3 (a).

The change of the slope can be expressed in terms of the change of the ratio, $C_{PCG}^{PC} / C_{QDG}^{PC}$, from 2.1 in regions A and C to 0.78 in region B, where C_{QDG}^{PC} and C_{PCG}^{PC} are capacitances of the PC to QD gate and to PC gate, respectively. In region B, the conductance channel is formed exactly between the PC and QD gates. In this region the system can be employed as terahertz detector [36]. The QD is gradually isolated from reservoirs when the QD gate is negatively biased, which increases the effective capacitance C_{QDC}^{PC}, due to additional parallel capacitance between the QD gate and the PC through the isolated QD. The dashed line in Fig. 8.3 (a) denotes the boundary where the QD is isolated from the reservoirs.

In region A, the conductance channel is shifted towards a location below the QD gate, so the QD is formed simultaneously with the conductivity pinch-off. In region C, the conductance channel is moved to a position underneath the PC gate. V_{QD} is beyond the dashed white line, so the QD is isolated from the reservoirs. There is additional capacitance of the QD gate to the conductance channel, because of the isolated QD, but it is small because the QD and conductance channel are spatially separated from

each other. Therefore, the slopes of the pinch-off boundary in regions A and C are expected to be almost identical. Periodic oscillations of the PC conductance are observed close to the pinch-off boundary in region B, see Fig. 8.3 (b). These were present in more than a half of the devices fabricated on the same GaAs/AlGaAs wafer. The reproducibility of the oscillations was very high for a particular sample. The other samples display a smooth pinch-off curve. In the sample presented here, the oscillation amplitude is largest at V_{PC} ~ -1.3V and V_{QD} ~ -1.47 V.

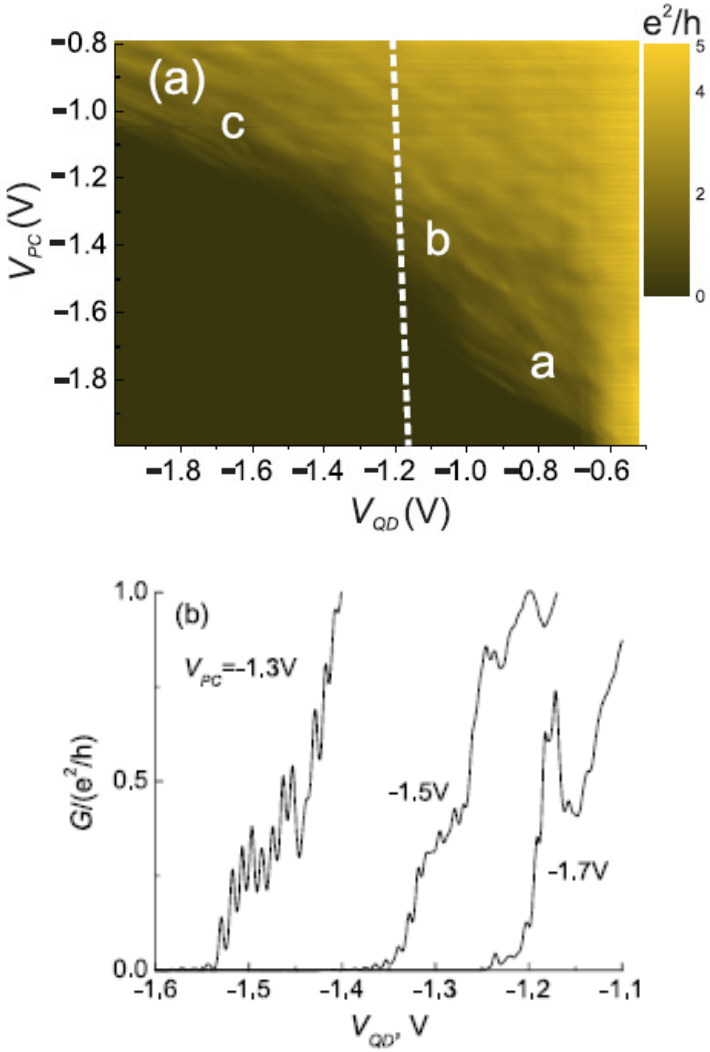


Figure 8.3. (a) Intensity plot of conductance in coordinates of V_{PC} and V_{QD} close to pinch-off region. In regions labeled A and C, the pinch-off boundary is a straight line with identical slope; in region B the slope is larger. The white dashed line indicates the boundary between isolated (left) and strongly coupled to reservoirs (right) QD. (b) Periodic oscillations of conductance observed when crossing the pinch-off boundary, at PC gate voltage values of 1.3 V, 1.5 V, and 1.7 V. The oscillations are strongest in region B and weaker in regions A and C.

In regions A and C, the oscillations become weaker and finally disappear. As can be observed in Fig. 8.3 (b), the periodicity is not related to the conductance quantization of PC, as the position and number of oscillations are not correlated with the conductance quantum plateaus at multiples or rational numbers of e^2/h [Paper VII].

There are more than ten periods of oscillations when G is below e^2/h. It was verified that oscillations are not sensitive to the magnetic field of up to 1 T, which excludes possible quantum interference of the scattered electron waves. Similar effects, including periodic and aperiodic oscillations of conductance of narrow channels observed in 2DEG in GaAs/AlGaAs and Si quasi-1D systems were reported before [112]. The oscillations of conductance can be explained by the Coulomb blockade of electrons tunneling between quantum dots. In Fig. 8.4, a stability diagram of the second derivative of source-drain current $-d^2I_{SD}/dV^2_{SD}$ versus both V_{SD} and V_{PC} at fixed $V_{QD} \sim -1.5$V is shown. The slope of this map is not monotonous, so the features of the pinch-off region are clearly seen. The diamond-shape structure marked by dashed white lines in Fig. 8.4 can be explained by transconductance of the point contact in a regime of bound states. The diamonds reflect the PC conductance quantization, specifically peaks in differential conductance at transitions between different conductance plateaus. A small dot (SD) of electrons is formed inside the PC conductance channel in regime of Coulomb blockade. From the horizontal diagonal of the diamonds, the charging energy of the dot can be estimated as $E_C \sim 3$ meV. This corresponds to a diameter of $d = e^2/[4\varepsilon_0(\varepsilon_r+1)E_C] \sim 100$ nm, if the SD is modeled as a circular disk inside the conductance channel, where $\varepsilon_r = 13$ is the relative permittivity of GaAs, ε_0 is the permittivity of free space. Such a dot can be accommodated in a channel between the QD and the PC gates, with a width of the same order, ~200 nm [Paper VII].

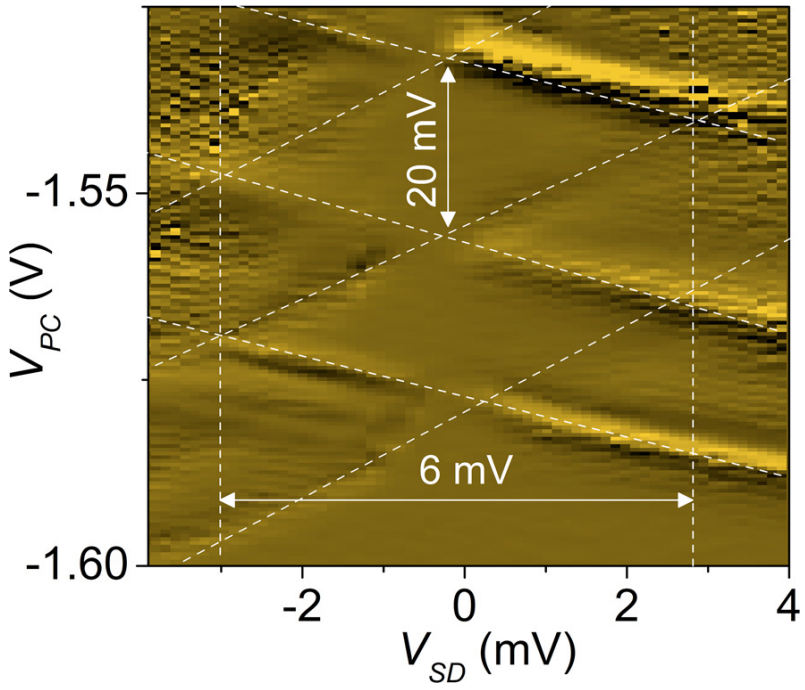


Figure 8.4. Intensity plot of $-d^2I_{SD}/dV^2_{SD}$ close to pinch-off region. The white dashed lines are guide to the eye depicting the diamond-shape of stability diagram [Paper VII].

The actual size of the dot is, however, much smaller, obtained from the analysis of conductance oscillations: in a wide range of V_{QD} the period of oscillations DV_{QD} ~14 mV, which corresponds to a capacitance between the QD gate and the dot C_{SD}^{QDC} ~1.1×10^{-17} F. The solution of the Laplace equation for a system "QD gate—SD" with this capacitance value to be obtained yields the diameter of the small dot of ~35 nm, which implies that such a dot would contain 3 to 30 electrons [Paper VII]. The potential profile created by the QD and PC gates was modeled; it has a saddle shape, without any local minima. In all samples, the oscillations were nearly periodic; impurities in the channel are not expected. The SD origin could be explained by increase in modulation of the bound state energies due to monolayer roughness of quantum well interfaces [Paper VII], which can amount up to ~0.5 meV in the heterostructure presented here. A lateral scale of this roughness can amount 10 nm, depending on parameters of growth and substrate orientation. The SD in the PC channel could be created randomly because of this roughness, apparently giving rise to periodic conductance oscillations.

8.3. Chip layout and Fabrication

In this work, technological procedures for fabrication of arrays of devices for THz imaging have been developed at Chalmers University in Sweden. A set of photo masks was designed in collaboration with NPL and University of London (RHUL). The photo masks were fabricated by the author at Chalmers University. The mask layout (Fig. 8.5) includes patterns for Ohmic contacts, mesa area pattern, and antenna metallization layer.

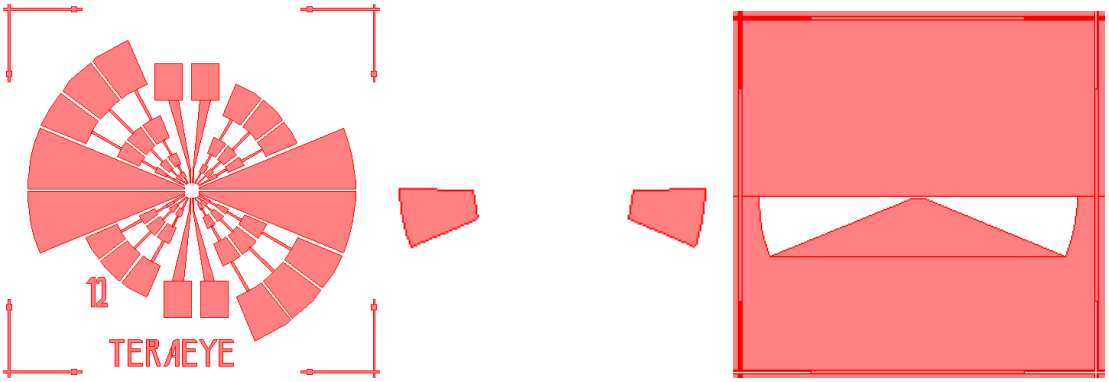


Figure 8.5. Mask layout for fabrication of a single device, including patterns for Au metallization layer, AuGe Ohmic contacts, and mesa layer.

The photo masks were then used for optical lithography with a ~400 nm UV mask aligner. The patterns in the photo masks were supplemented with three patterns for the e-beam lithography, namely the fine mesa area, planarization, and the gold gates. The dimensions of chip marks were optimized for accurate mark detection; the chip marks

were placed within ~ 60 µm distance from the chip centre, which is within one scanning field of the electron beam (~80 – 90 µm). This enables detecting the chip marks in one scanning cycle and yields enhanced precision of coordinates obtained by mark detection and hence improves the alignment between different layers of lithography. A photo of an example single device is shown in Fig. 8.6.

The fabrication technology is described in detail in Chapter 3.

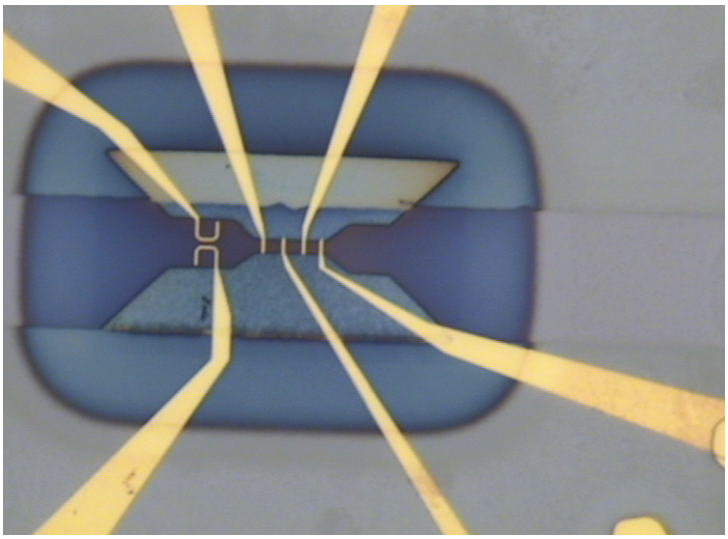


Figure 8.6. A single THz sensor integrated in a log-periodic antenna

8.4. Experimental results

8.4.1. Oscillations in QD devices

Results of experiments with the SET allow obtaining additional information about QD-SET and QD-PC devices. In particular, the region where the QD is formed can be identified with the SET. Constant voltage of 1mV was applied between the source and the drain of the SET, and the current was sensed. When V_{PC} is fixed the SET current oscillates with V_{QD}, Fig. 8.7 (a). The period of oscillations has a sharp transition from 81 to 5.5 mV at V_{QD} ~ –1.2 V due to extra capacitance created between the QD gate and the SET through the newly formed QD, see Eq. (8.1). The map of CB oscillations was measured by sweeping V_{QD} from –1.0 to –1.4 V at fixed V_{PC}, see Fig. 8.7 (b). In this map, two regions with different oscillation periods of SET can be observed. The boundary between those indicates creating of the QD, which enables possible use of the QD-SET device as terahertz detector in the vicinity of the boundary [109]. This boundary was transferred to Fig. 8.3 (a) as a white dashed line displaying the region where the QD is formed. The white dashed line in Fig. 8.7 (b) indicated the boundary of the pinch-off region of the PC, obtained from Fig. 8.3 (a). The pinch-off region of the PC channel is located below the dashed line in Fig. 8.7 (b). An effect of charging of the small dot can be expected in the vicinity of the dashed line of Fig. 8.7 (b),

which is determined by the capacitance C_{SD}^{SET} between the SET and the SD. Such an effect would be seen as a shift of the SET's CB peak position by ~0.7 mV, which is beyond the accuracy of this experiment, due to the large period of charging of the SD compared to the period of CB of the SET, 14 mV vs 5.5 mV. Small shift of the CB peaks of the SET over several periods is hampered by fluctuations of the CB position.

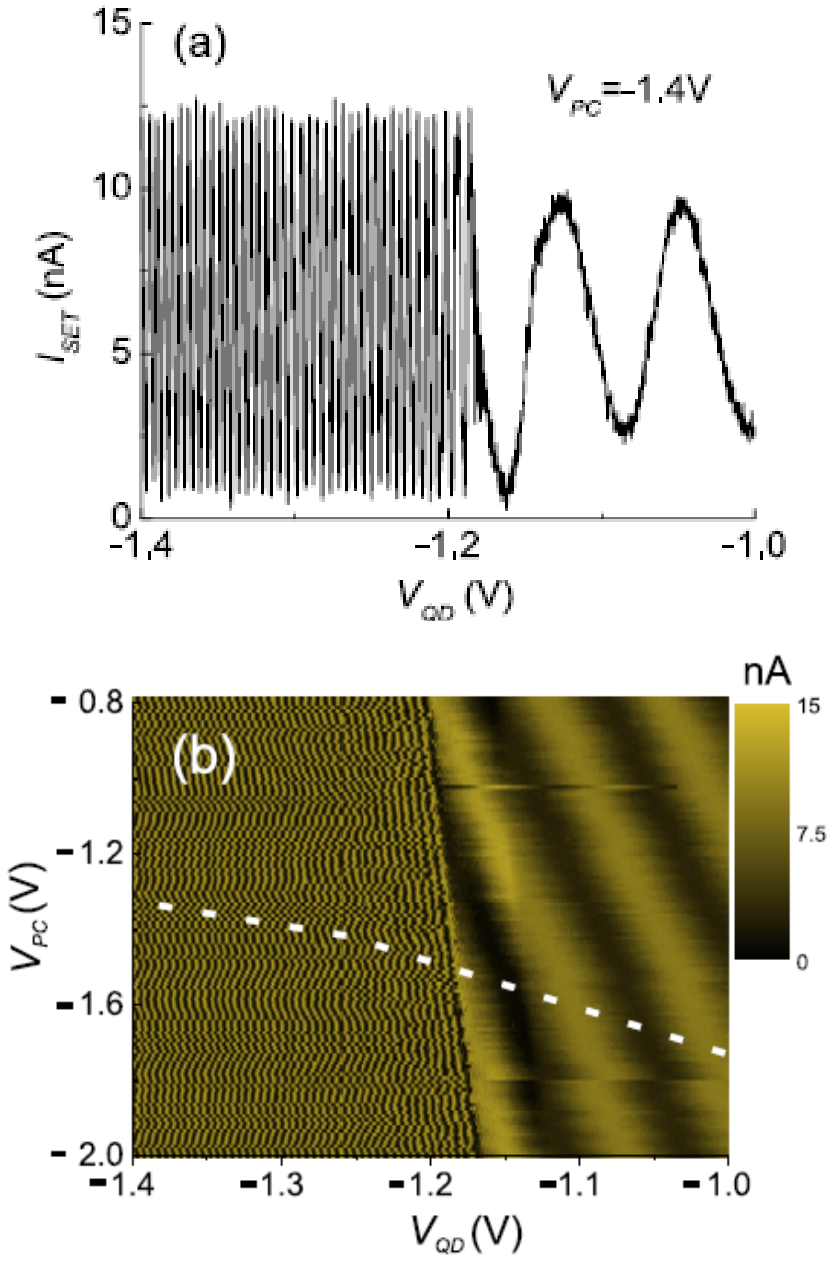


Figure 8.7. (a) CB oscillations of the SET current; period of oscillations changes from 81 to 5.5 mV when QD is decoupled from the reservoirs. (b) Intensity plot of the CB oscillations in coordinates of V_{QD} and V_{PC}. The dashed white line indicates pinch-off boundary of the PC [Paper VII].

8.4.2. Analysis of the device using Electrostatic Model

The equivalent capacitances of the electrostatic model are presented in Table 8.1 for further analysis. The total capacitance of a certain element to the environment is denoted by Σ. The capacitance values are based on the period of CB oscillations of SET.

For C_{SET}^{QD} estimation, some potential is applied to 2DEG, at zero potential at the QD gate. C_{Σ}^{SET} was calculated from the charging energy of SET.

	SET	QD	PC	Σ	QDG	PCG
SET	-	75 aF	21 aF	0.4 fF	2 aF	0.24 aF
QD	75 aF	-	56 aF	0.25 fF	0.27 fF	24 aF
PC	21 aF	56 aF	-	50 aF	50 aF	50 aF

Table 8.1. Capacitances of the electrostatic circuit model of the device. Symbol Σ denotes the total capacitance of a corresponding element to the environment.

C_{PC}^{SET} ~21 aF is found using CB oscillations of the SET when some potential is applied to the 2DEG with the PC at the boundary of the pinch-off. By solving the Laplace equation for the PC that is 0.1×0.1 μm^2 large, C_{PC}^{SET} ~30 aF is obtained, which is close to the experimental value. The remaining capacitances were found from numerical solution of Laplace equation.

The consistency of the capacitance values can be verified by calculating the effective capacitance between the SET and the QD gate for two cases: when the QD is strongly coupled to and when it is isolated from the reservoirs. In Fig. 8.7 (a), the difference in effective capacitance can be observed as a change of period of the SET CB oscillations. In the case of strong coupling, when $C_{\Sigma}^{QD} => \infty$, the effective capacitance is equal to C_{QDG}^{SET}. When the QD becomes isolated from the reservoirs, the capacitance turns into

$$C_{eff} \approx C_{QDG}^{SET} + \frac{C_{QDG}^{QD} C_{\Sigma}^{SET} C_{SET}^{QD}}{C_{\Sigma}^{QD} + C_{QDG}^{QD} C_{\Sigma}^{SET}}. \qquad (8.1)$$

From the experiment, a value of $C_{eff} = 2.9\times10^{-17}$ F is obtained, which is close to the estimated value of 3.1×10^{-17} F.

8.4.3. Charge sensitivity of the devices

The sensitivities of the SET and PC to charge fluctuations at the QD are determined by the transconductance dG/dV_g and the capacitive coupling between the PC and the SET to the QD, where V_g is the voltage applied to the PC gate or the SET gate. Both factors can be taken into account by introducing the sensitivity of the source-drain current to charge variation at the QD, dI/dQ. Once the current noise in the system, dI, is known, the detectable level of QD charge excitation would be $\delta Q = \delta I / \frac{dI}{dQ}$. A moderate sensitivity of the PC to charge excitation in region B of Fig. 8.3 was determined, dI/dQ ~4×10^6 A/C; Current noise of dI ~3 pA in a bandwidth of ~1 kHz was observed in the set up, which enables the detection of excitation of few electrons by the PC, δQ ~4e, enhanced in regions with CB oscillations, typically by ~15% at maxima.

At the same time, the charge sensitivity becomes dependent on the operation point, which deteriorates the stability of the detector's operation. The sensitivity of the SET readout is slightly higher, dI/dQ ~10^7 A/C and is constant along the boundary where the QD is formed. There is ~25% variation of sensitivity depending on the operation point of the SET.

The SET is apparently able to detect excitation of dQ ~e in a bandwidth of 1 kHz since the excitations of individual electrons are detected by the QD-SET device, producing spikes close to the pinch-off region, shown in Fig. 8.7 (a).

8.5. Extension to scalable Arrays

The investigated THz sensors can easily be arranged in arrays, for enhanced sensitivity due to the total voltage response constituted of several contributions of single devices. In this work, arrays of THz devices were deposited on a 3-inch wafer that accommodates 400 arrays, see Fig. 8.8. Each array includes 14 sensors, each of those coupled to a bow-tie antenna and controlled by a pair of gates. The chip layout is scalable to a large array that can be extended to larger number of sensors of different shapes. An optical image of an array of sensors is shown in Fig. 8.9.

Each sensor in the array includes semiconductor mesa area aligned with a gold gate and metallization. The size of a single array is about 2×2 mm^2. The metallization includes bow tie antennas for 14 sensors in the focal points.

The mesa pattern and metallization in an array are shown in Fig. 8.10. The mesa area is a 100 nm deep pattern formed in a GaAs/AlGaAs heterostructure with high mobility two dimensional electron gas (2DEG). The Ohmic contacts are annealed, and metallization is deposited over electrodes and point contact (PC) gate to define planar

bow tie antennae. The quantum dots are formed in the 2DEG channels by negatively biased gates, in total 14 quantum dots in an array. Diagonal leads for the gates are shown in Fig. 8.10 (b). Each 2DEG channel has one source electrode and a common drain electrode to read out the PC.

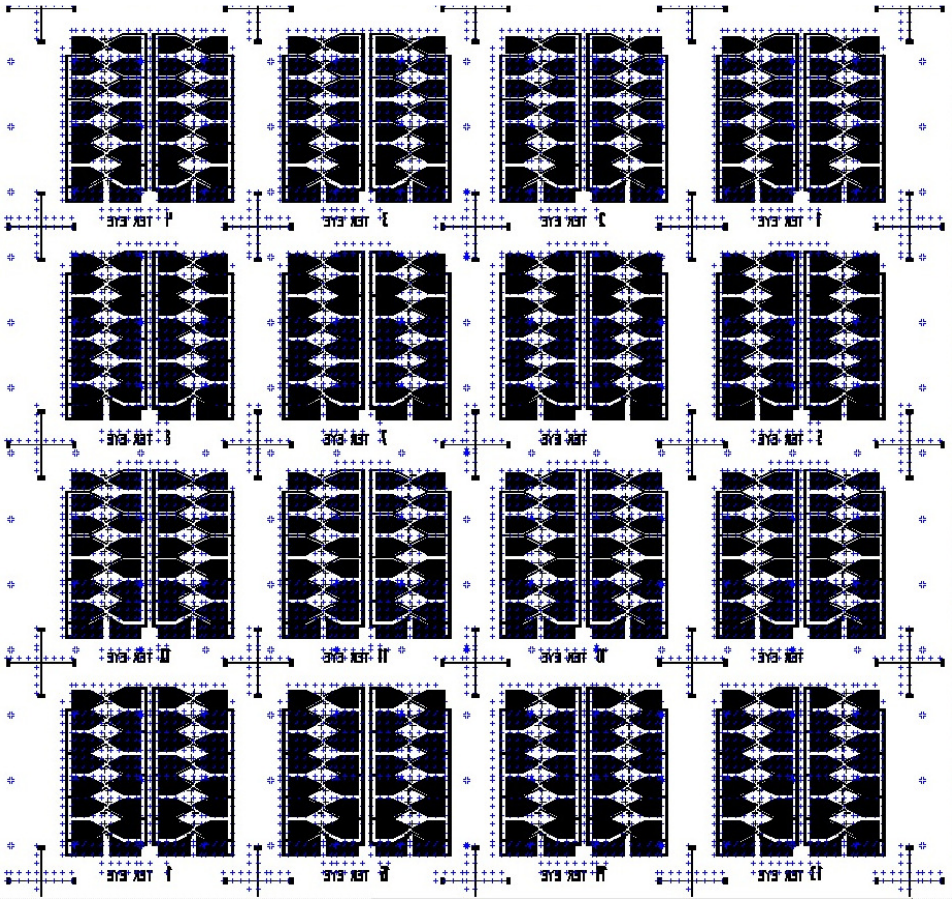


Figure 8.8. Layout of a part of a wafer with 16 arrays (10 × 10 mm^2).

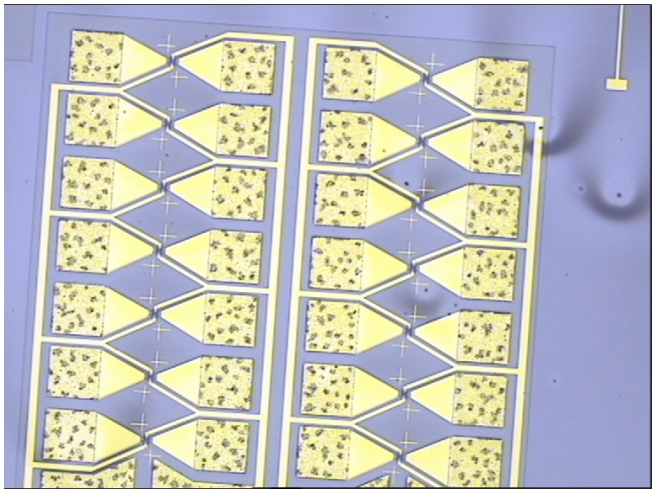


Figure 8.9. Optical image of an array of sensors. The dimensions of the array is ~2×2 mm.

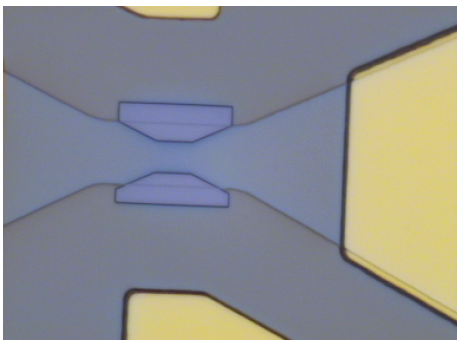
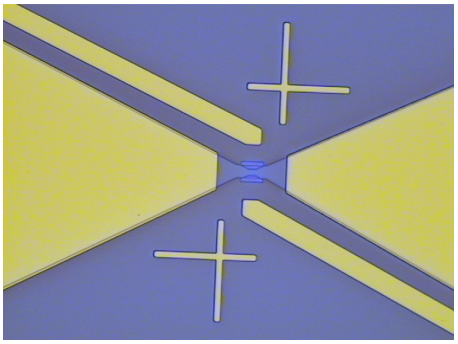
a)  b) 

Figure 8.10. Photo of mesa pattern with metallization, different zoom

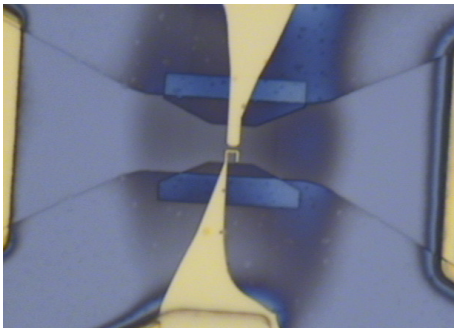
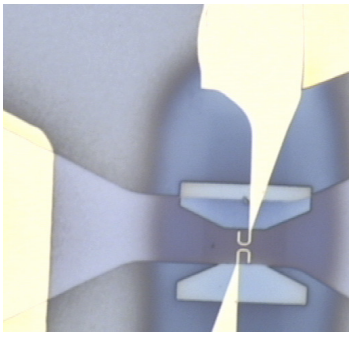
a)  b) 

Figure 8.11. Photo of the gate pattern, defined by Electron Beam Lithography

The gate pattern and details of one individual sensor are shown in Fig. 8.11. The gates are controlled by two electrodes, common for all sensors. The gate metallization is made of a 100 nm thick Au film.

8.6. Conclusions

The operation of the QD-SET-PC device has been investigated; the electrostatic model of the system is described, with a set of equivalent capacitances determined. The device is able to detect charge excitations of the QD with accuracy close to one electron for the SET-QD system and several electrons for the PC-QD system. Periodic oscillations of the PC conductance are observed close to the pinch-off region, which is explained by the Coulomb blockade of electron tunnelling in a quasi-1D channel.

Chapter 9
Superconducting Nanostrip Phase Switch for cosmology instruments

In this chapter, planar phase switch circuits integrated in unilateral back-to-back finlines are presented. The circuits considered here were designed to replace mechanical switches for modulating microwave signals in waveguides; the samples have been developed, fabricated and tested in collaboration between Chalmers and Oxford Universities. All investigated planar phase shift circuits have been fabricated by the author of this thesis in the cleanroom at Chalmers MC2 and tested at Chalmers and Oxford.

The microwave switching characteristics are examined, measured at a switching rate of up to 100 kHz. The switching speed of the proposed circuit is demonstrated to be well above the speed required for phase modulation in astronomical instruments and is mainly limited by the time constant of the measurement system (~10 μs). Real switching time of a superconducting nanobridge is expected to be much shorter, in a picoseconds range, when not limited by thermal effects.

9.1. Measurements of CMB polarization

The electric field in a polarized electromagnetic signal can be represented by its orthogonal components, E_x and E_y. The Stokes parameters are then expressed by the average values of the amplitude of the electric field over many cycles of the electromagnetic wave, i.e. [5]:

$$I = \langle E_x^2 + E_y^2 \rangle$$

$$Q = \langle E_x^2 - E_y^2 \rangle$$

$$U = \langle 2E_xE_y \cos(\varphi) \rangle$$

$$V = \langle 2E_xE_y \sin(\varphi) \rangle$$

where ‹…› means time averaging over periods and φ is the phase difference between the fields in the x and y directions.

The polarization of an electromagnetic wave can therefore be determined by measuring the Stokes parameters I, Q, U, V where I is the total intensity, V measures the degree of circular polarization and Q and U measure the degree of linear polarization in two orthogonal directions [18]. In the pseudo-correlation polarimeter, shown in Fig. 9.1, the signal incident onto a horn is split into two linear polarizations using an orthomode transducer (OMT). The signals are then converted into circular polarization using a quadrature hybrid. One of the signals is then phase modulated relative to the other; finally the two signals are converted back to linear polarization and measured by the detectors. The output signals D_1 and D_2 in Fig. 9.1, measured by the detectors are [18]:

$$D_1 = I - Q \cdot \cos\varphi - U \cdot \sin\varphi \tag{9.1}$$

$$D_2 = I + Q \cdot \cos\varphi + U \cdot \sin\varphi \tag{9.2}$$

Since the CMB radiation is linearly polarized, measuring U and Q is of primary interest.

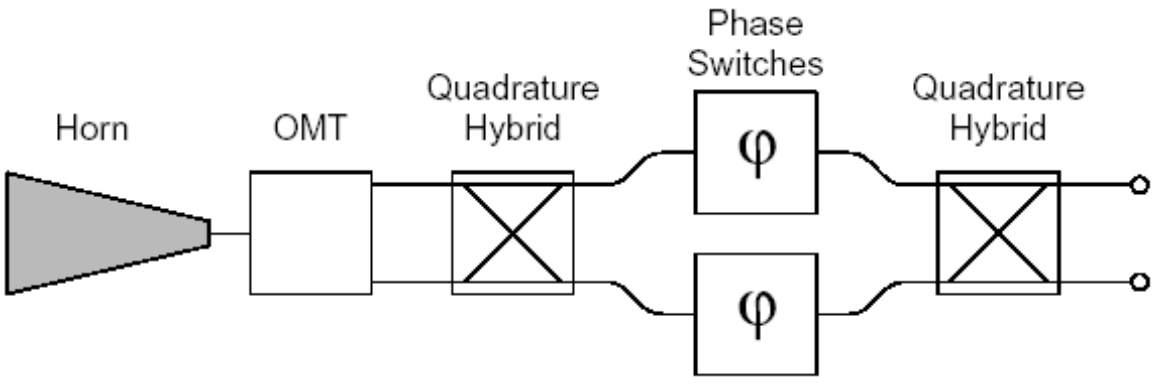


Figure 9.1: The layout of a pseudo-correlation polarimeter [18].

According to the equations (9.1) and (9.2), the outputs respond to I, U and Q Stokes parameters, which allows determining the linear polarization parameters by obtaining

the difference of the detector outputs. Indeed, by switching the phase difference between 0 and 180 degrees, the U term remains zero and Q is measured. By changing the phase difference between 0 and 90 degrees the output is switched between Q and U [18].

Methods employing rotating mechanical parts for phase modulation in cosmology instruments, suffer from significant RF losses [113], are difficult to fabricate and do not provide the required accuracy. Therefore, implementing phase modulation using planar high-frequency circuits [16] would be advantageous as planar circuits are easy to fabricate and they do not include rotating components. It would allow fabricating the whole polarimeter in planar circuit technology with only the horn and OMT implemented in waveguide, and the rest of the setup integrated in the detector block. Large arrays employing phase modulation at high frequencies could be fabricated reliably and cheaply [18].

An On/Off switch can be implemented by producing a superconducting nanostrip across the electrodes of the transmission line. By applying a bias current signal through the superconducting nanostrip, it can be switched from the superconducting state to the normal one, thus switching from shunt to open at some point along the transmission line.

The device presented here is possible implementation of a planar superconducting on/off switch operating at millimeter wavelengths. The switching devices comprise single or multiple niobium nitride (NbN) bridges, positioned across the slotline section of back-to-back unilateral finlines. The NbN bridges are switched from the superconducting state to the normal state by passing current through the bridges with magnitude that exceeds its critical current value [Paper VI].

9.2. RF analysis of the phase switch circuit

A finline with single or multiple nanobridges across it can be modeled with a transmission line that is shunted by a variable load resistance representing the impedance of a NbN bridge.

An electromagnetic wave propagating along a transmission line with a switch is transmitted in the open state and reflected in the shunted state of the switch. A low loss transmission and high reflection can be achieved by proper choice of the impedance Z_L across the terminals of the transmission line of characteristic impedance Z_0. If the impedance of the load changes between $Z_{off} << Z_0$, and $Z_{on} >> Z_0$, the device switches from the closed to the open state respectively.

For a simple model including a transmission line shunted by a single load resistance to represent the impedance of a NbN bridge, the transmission coefficient τ and reflection coefficient Γ are given by [paper VI]:

$$\tau = \frac{2Z_L}{Z_0 + 2Z_L} \quad ; \quad \Gamma = \frac{-Z_0}{Z_0 + 2Z_L} \tag{9.3}$$

where Z_0 is the characteristic impedance of the transmission line and Z_L is the load impedance of the bridge. The switching ability of the circuit is therefore determined primarily by the ratio between $Z_L = Z_{on}$ and $Z_L = Z_{off}$.

The On/Off switching device can be produced by fabricating a directly or capacitively coupled superconducting nanostrip across the electrodes of the transmission line (see Fig. 9.2 (a) and 9.2 (b)). For a capacitively coupled device, it impedance in the superconducting state is given by:

$$Z_{off} = i\omega(L_g + L_k) + 2/i\omega C = (2 - \omega^2 LC)/i\omega C \tag{9.4}$$

By applying a bias current signal through the superconducting nanostrip, it can be switched to the normal state with an impedance

$$Z_{on} = R_N + i\omega L_g + 2/i\omega C = R_N + (2 - \omega^2 L_g C)/i\omega C, \tag{9.5}$$

where R_N is the normal resistance and L_g, L_k and L are respectively the geometrical, kinetic and total inductances of the strip [18]. At resonance ($\omega^2 LC = 2$), the impedance in the superconducting state becomes small, resulting in high reflection, which means that the switch is closed. As to the normal state, the impedance in that state is mainly determined by the normal resistance of the nanostrip, provided $\omega L << R_N$. The material and geometry of the nanostrip are therefore chosen to maximize the value of its normal resistance R_N and to ensure that this value $R_N >> Z_0$, making thereby the switch open in the normal state, where Z_0 is the characteristic impedance of the slotline.

For example, Niobium Nitride is a material that meets this requirement. NbN is a superconductor with a relatively high critical temperature (up to 14 K) that in the normal state becomes a conductor with relatively high specific resistance. In our measurements, a 22 nm thick NbN film displayed about 70 Ω per square sheet resistance, which is consistent with the table value of 200 μΩ·cm for the specific resistance of NbN. At the same time, its characteristic temperature varying between 7 to 14 K for our films allows testing our devices at liquid He temperature, around 4 K.

The devices presented in this thesis are DC coupled to the finlines as in that case NbN nanobridges are easy to fabricate in one layer with the finlines; a nanobridge and a finline can be both patterned in one e-beam exposure. While this approach does not yield best performance as it does not provide strongest mismatch between the nanobridge and the finline in Open state due to kinetic inductance of the nanobridge, it still allows verifying the concept of switching the RF signal between Open and Closed states using planar Phase Switch devices.

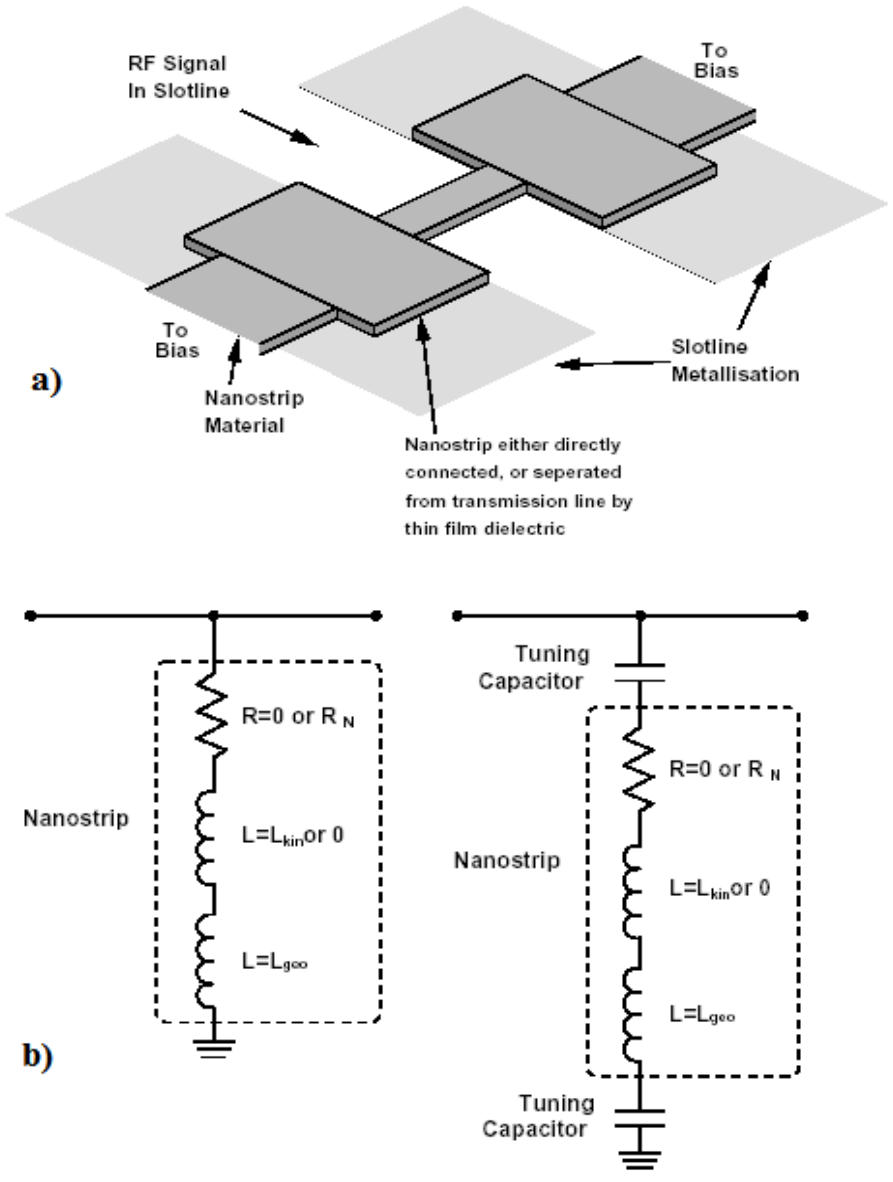


Figure 9.2: (a) Geometry of a nanostrip switch in slotline.
(b) Equivalent circuits for the directly and capacitively coupled nanostrip switches.

For example, a 20 nm thick and 1 μm wide niobium nitride film nanostrip of a length $l = 5\ \mu$m has the normal resistance of ≈ 500 Ω, the geometrical inductance of ≈ 3 pH, and its kinetic inductance at frequencies well below the superconducting gap is about 12.6 pH [18].

The DC coupled nanobridge with such dimensions will therefore display a considerable total inductance, yielding relatively high impedance in the Closed state, possibly comparable to the characteristic impedance of the finline (~70 Ω). This could deteriorate the performance of the DC coupled devices compared to the devices with capacitive coupling. Nevertheless, fabricating and testing devices with DC coupling allows verifying the concept of switching the RF signal in the waveguide by shorting the transmission line with a NbN nanostrip, implementing simple and straightforward technology for fabricating DC coupled Phase Switch devices.

The geometric inductance of the superconductive strip determined by the geometry of the strip, is given by [Paper VI]

$$L_{geo} \approx 0.2l(\frac{1}{2} + \ln(\frac{2l}{w+t}) + 0.11(\frac{w+t}{l}))\mu H. \tag{9.6}$$

and the kinetic inductance of the nanostrip in the superconducting state by

$$L_{kin} = \mu_0 \frac{l\lambda}{w} \coth \frac{t}{\lambda} \approx \mu_0 \lambda^2 \frac{l}{wt} \tag{9.7}$$

where λ is the London penetration depth of the material.

For a directly coupled switch circuit, eq. 9.4 and 9.5 are reduced to:

$$Z_{on} = R_N + i\omega L_g; \text{ and } Z_{off} = i\omega(L_k + L_g) \tag{9.8}$$

The ratio between Z_{on} and Z_{off} determines the transmission and the reflection and hence the ratio of the transmitted power in Open and Closed states. Therefore, the geometry must be chosen to optimize the operation of the switch, i.e. to ensure high normal state resistance and low impedance in superconducting state that is determined by the kinetic inductance.

Power dissipation is an essential aspect for operation of a switch. The power dissipated by a switch in the normal state equals to $P = V^2/R_N$. This input electrical power should be balanced by the heat dissipation via the electron-phonon interaction.

The thermal conductivity due to the electron-phonon interaction is expressed as:

$$G = 5\sum wltT^4, \tag{9.9}$$

where $\sum$ is the coefficient of the electron-phonon interaction ($\approx 10^9$ W/m^{3}K^5) for niobium nitride), *wlt* is the volume of the nanostrip and *T* is the electron temperature. Maintaining the nanostrip in the normal state will therefore require a power dissipation of

$$P_N = V^2/R_N \approx GT \tag{9.10}$$

For typical niobium nitride nanostrip with dimensions of l = 5μm, w = 1μm and t = 20 nm, this results in a power dissipation of $\approx 2\mu W$ at 4 K to keep the nanostrip in the normal state. For a niobium nitride film of cross-section of 1 μm × 20 nm, the critical current required for switching to the normal state is expected to be around 100 μA. On switching, this current is dissipated in the now resistive nanostrip, giving a transient power dissipation of around 10 μW for a 1 kΩ nanostrip on switching from the superconducting to the normal state.

9.3. Chip layout and fabrication

The chip layout is shown in Fig. 9.3. Phase switch devices were fabricated on Silicon and Quartz wafers. Silicon and Crystalline Quartz were used for fabrication of a few samples, and were later replaced by Fused Quartz ("Fused Silica"), that was finally chosen as the material for the substrate, mainly due to a lower dielectric constant of quartz compared to Silicon.

The wafer layout includes 24 chips of 7×7 mm area on each wafer, and the chip layout incorporates three to five finline-integrated phase switch devices with different nanobridge widths, varying between 0.2 μm and 2 μm.

The devices were fabricated at Chalmers by patterning back-to back unilateral finlines and nanostrips across the terminals of each finline in one lithography step on a NbN film deposited on a ~200 μm thick substrate. The fabrication process of the phase switch circuits includes two lithography steps, namely a photo lithography for patterning gold electrodes and e-beam lithography for patterning the structures made of NbN. The whole fabrication procedure is described in detail in Chapter 2 and is shown in Fig. 9.4.

On quartz substrates, a NbN film was deposited on a thin Ti layer using magnetron sputtering of a niobium cathode in an argon-nitrogen plasma mixture. In some samples [88], the NbN film was deposited on a hot substrate that was heated by a lamp before and during the deposition process. But for most samples presented in this

thesis, room-temperature processes were used for device fabrication. The resulting critical temperature is somewhat lower than that of films produced with heating but sufficient for the purposes in this thesis.

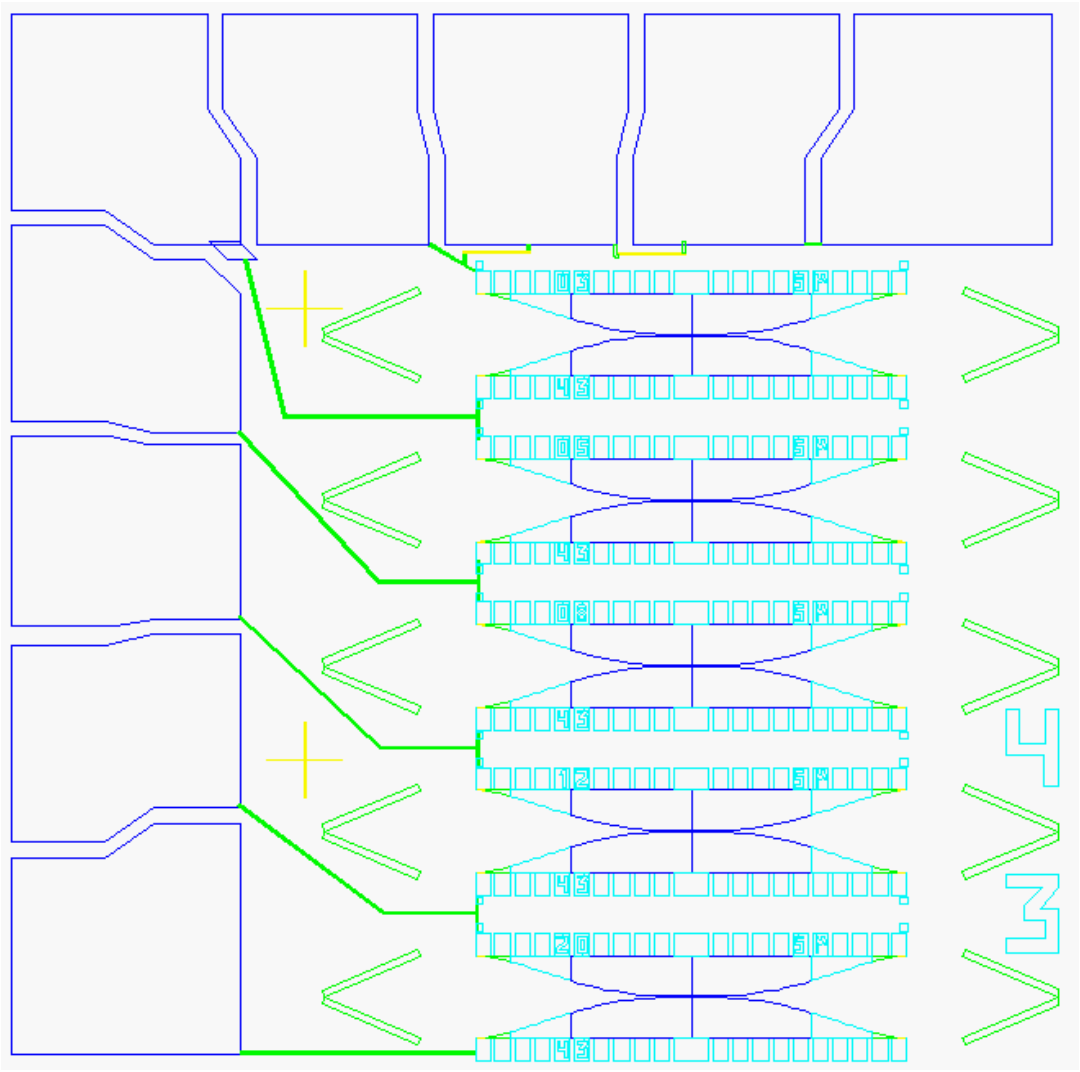


Figure 9.3. Chip layout with 5 Phase Switch devices integrated in back-to back finlines

Standard photo lithography was then performed for pattering gold electrodes, including spinning two layers of on the wafer (a lift-off resist and a photoresist), baking both of the resist layers, UV exposure at a wavelength of 400 nm, and the development of the photoresist, with an undercut formed in the lift-off resist. The wafer was then cleaned in a RIE process by oxygen plasma, and a layer of chromium and ~100 nm of gold were evaporated and lifted off. The finlines are thus made of NbN covered partly with gold.

The pads and the finlines formed at this stage are shown in Fig. 9.4. For the patterning of the NbN nanostructures, the e-beam lithography was employed, including baking and spinning of the negative e-beam resist SAL-601, an e-beam exposure and development of the e-beam resist, the reactive ion etching of NbN in CF_4 plasma.

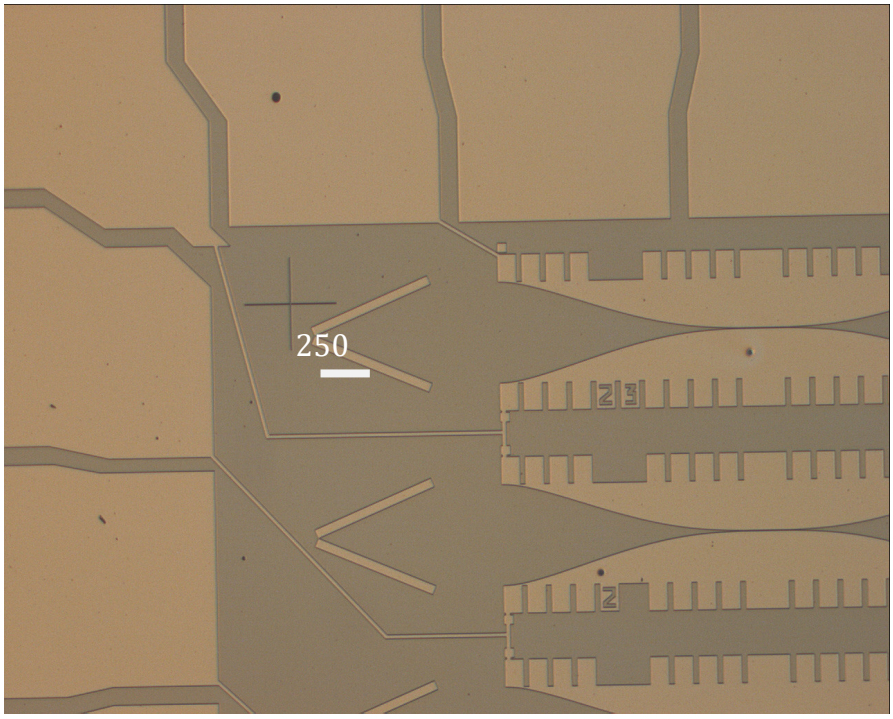


Figure 9.4. Gold pads and finlines formed by photo lithography and thermal evaporation

An example finline is shown in Fig. 9.5 in conjunction with a 5 μm long nanostrip. The unilateral finline was chosen as a transmission line for these experiments due to the simplicity in fabricating such a structure and because it offers straightforward coupling of RF power to the device from waveguide, and from the device to the detector.

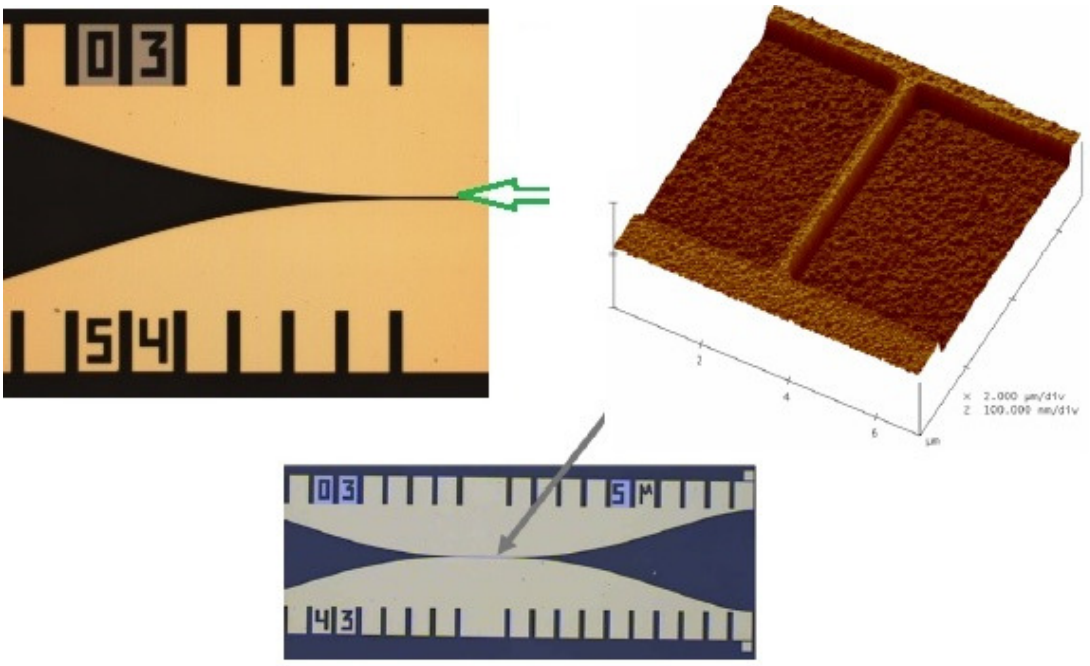


Figure 9.5: Optical images of NbN finlines; inset: An AFM image of the nanostrip.

For RF testing, the device is mounted in a waveguide. The serrations in Fig. 9.5 act as $\lambda/4$ open-ended stubs to prevent the propagation into the waveguide groove that supports the chip.

9.4. DC testing of phase switch circuits

Several samples with the finline gap of 5 μm were DC tested at 4.2 K. The thickness of NbN film was 22 to 50 nm and width ranged from 0.2 to 2 μm. The measured critical temperature of the NbN film ranges between 9 and 14 K, while critical currents for nanostrips of different widths deposited on different substrates using the above sputtering process with minor variations varied from ~40 μA to ~1 mA.

Time domain DC switching was observed by applying a square-wave current to the phase switch device, at switching frequencies from 100 Hz to 100 kHz. In Fig. 9.6 one can observe the current changing rapidly from non-zero value to a higher value, while voltage changes from zero to a finite value at the same time. This is an indication that the device toggled between the normal and the superconductive states. Some time delay was observed at the leading edges of the modulation voltage, though negligible compared to switching period, as shown in Fig. 9.6. The observed delay was in fact caused by the RC-time constant of the measurement setup rather than by the switching properties of the NbN nanostrip, which was confirmed experimentally by measuring the RC-delay of the experimental setup. This result is also consistent with previously published data that reported delays in switching in a picoseconds range for superconductive nanostrips [114]. The switching speed of the nanostrip is well above that required for large format interferometers, which is of the order of ~100 Hz.

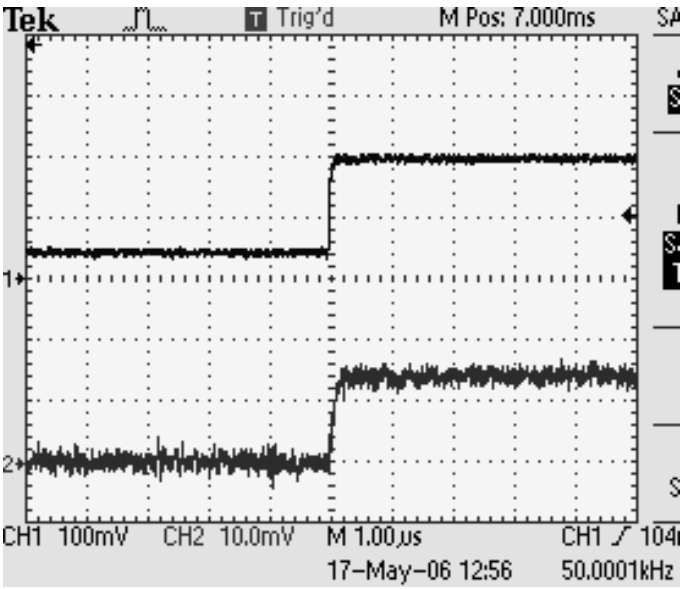


Figure 9.6. DC test of the nanostrip: the top trace represents the bias current, while the bottom one shows the output voltage across the strip.

9.5. RF testing of the phase switch

Switch circuit finline chips were mounted in a groove in a waveguide block (Fig. 9.7) containing a waveguide with a cross section of 0.55 × 1.1 mm. An OB-65 backward-wave oscillator was used as a radiation source for measurements at frequencies around 230 GHz. The RF signal was coupled to the RF block using a waveguide; a detector based on a Josephson junction was located at the output of the RF block with the switch circuit finline chip. Measurements of the current–voltage characteristic of the Josephson junction allow determining the signal level at the output of the switch.

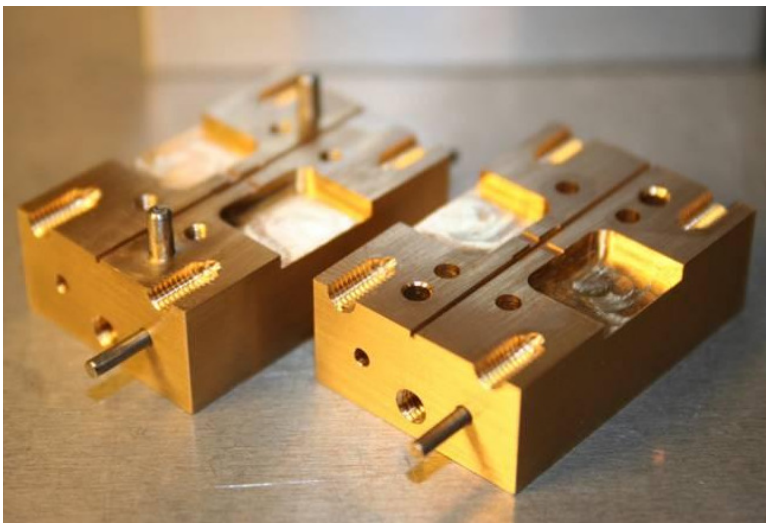


Figure 9.7. Waveguide block for RF measurements using Josephson detector.

In another experiment, the signal at 198 - 252 GHz was created by generating an 11-14 GHz signal using Anritsu MG3692B signal generator and then multiplying the frequency by 18 with a Radiometer Physics 2008004b frequency multiplier.

Both the phase switch finline chip and a detector chip were mounted in the same RF block with a waveguide as shown in Fig. 9.8 - 9.10. The RF signal was incident through a horn onto the input of the waveguide with the finline chip and the detector. In that case, a detector based on an SIS junction shown in Fig. 9.9 - 9.10 was used for measurements of the signal transmitted by the finline. The measurement of the current–voltage characteristics of the SIS junction allows determining the signal level at the output of the phase switch.

In both experiments, the phase switch circuit and the detector chip were operating at the same temperature (around 4 K). The phase switch finline chip mounted in a block is shown in Fig. 9.10, with finlines connected to biasing DC leads using bondwires.

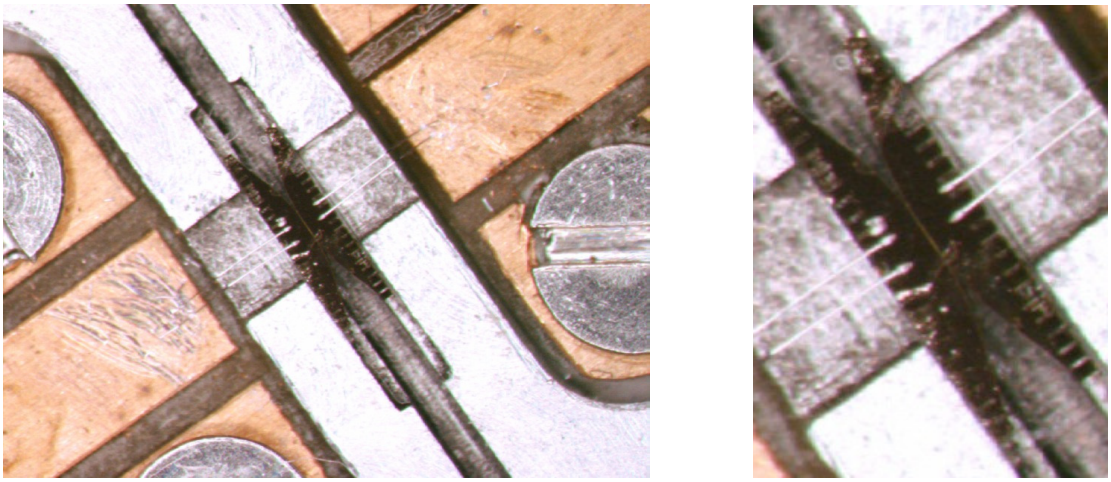


Figure 9.8. Phase Switch device mounted in a waveguide, different zoom

The SIS device (Fig. 9.10) placed across a unilateral finline deposited on a quartz substrate consists of a Nb/Al_2O_3/Nb trilayer structure fabricated using Nb technology. The RF block with the 0.55 × 1.1mm waveguides for the phase switch device and a the SIS detector has an option of suppressing Josephson current by magnetic field produced by a Nb coil around the finline chip with the SIS device (Fig. 9.9, left). The block with the phase switch device and the SIS detector was cooled using a Heliox Pulsed Tube Cooler.

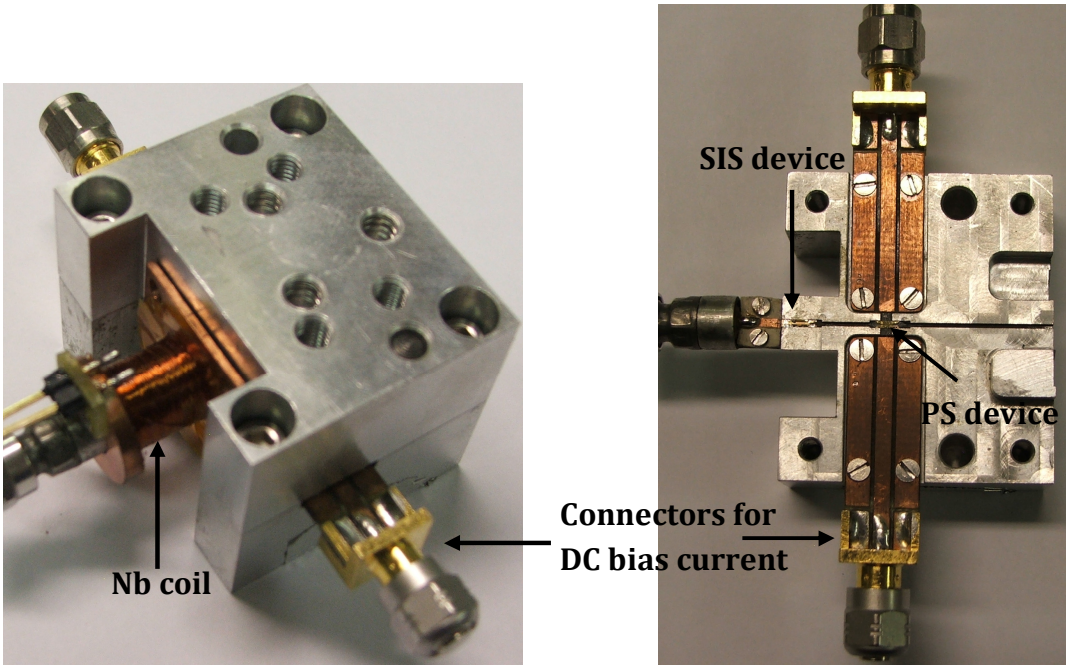


Figure 9.9. (Left) RF block with a coil for suppressing Josephson current with magnetic field; (right) the top view of the RF block, with Phase Switch and SIS device mounted.

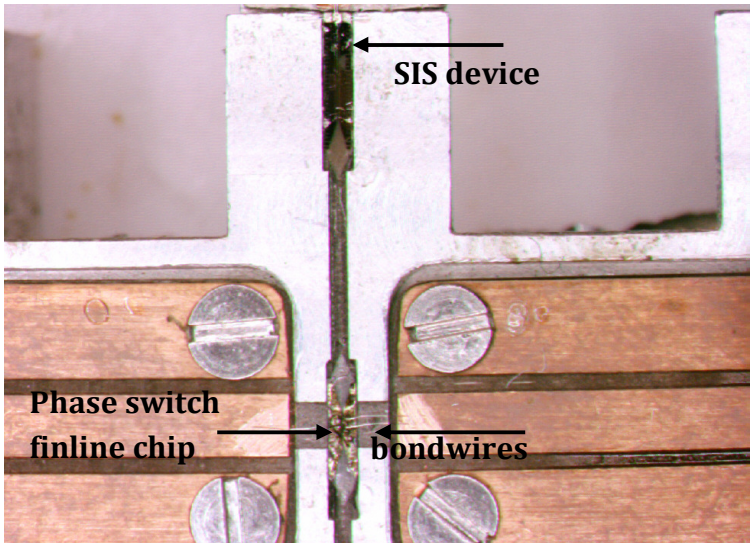


Figure 9.10. (Left) Switch and SIS devices mounted in the waveguide.

In the experiment with Josephson junction as a detector, Fig. 9.11 shows its current–voltage characteristics in the absence of RF signal; also, with RF signal and the switch circuit in Closed and Open states. As can be observed in Fig. 9.11, small transmission of the signal occurs in the closed position, while in the open position the transmission increases by ~14 dB. The resulting modulation depth is somewhat lower than that expected for the properly matched switch (100%); modifying the nanobridge impedance or implementing AC coupling with integrated on chip capacitors could improve the switching performance. The IV-curve of the phase switch device is shown in Fig. 9.12.

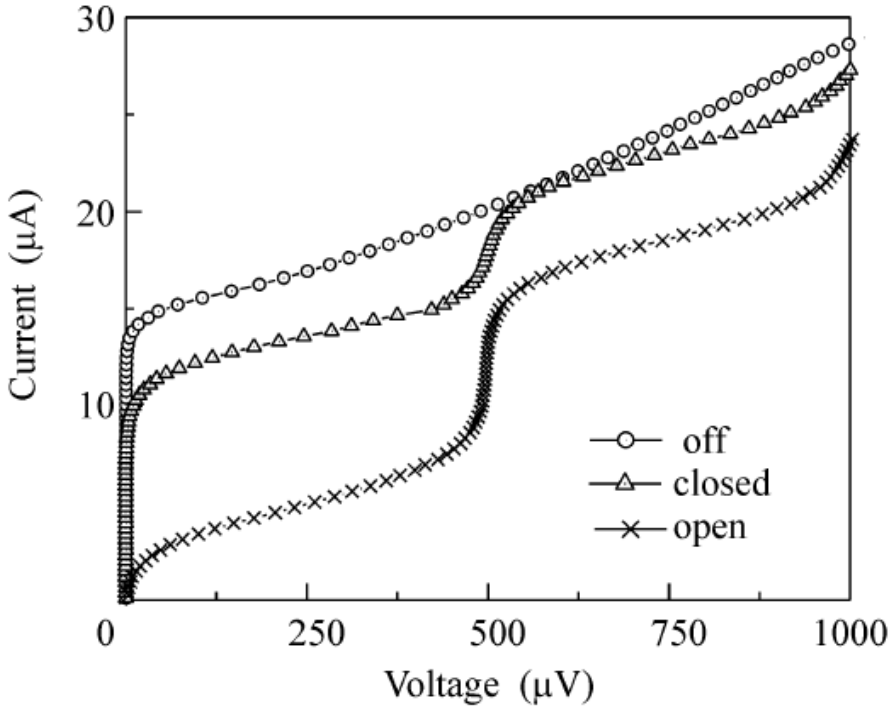


Figure 9.11. A current–voltage characteristics of the Josephson detector. The lines marked as open, closed, and off are for an open switch, closed switch, and turned-off radiation source.

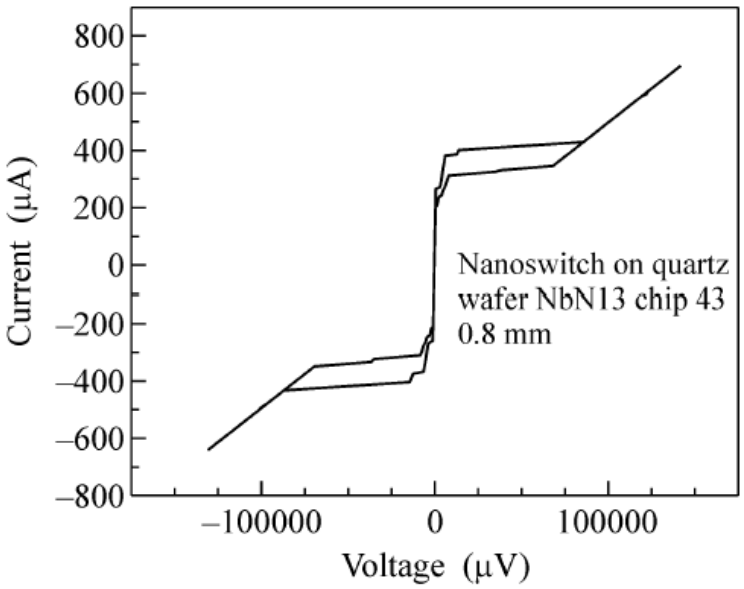


Figure 9.12. IV-curve of the 800 nm bridge with a resistance of 200 Ω.

In the experiments with SIS detector, the IV curve of the SIS device (Fig. 9.13) was pumped by incoming RF signal which results in photon steps on IV curve, due to photon-assisted tunnelling. The steps on IV curves of SIS detector for phase switch device in open and closed state at RF signal at 243 GHz are shown in Fig. 9.13, right.

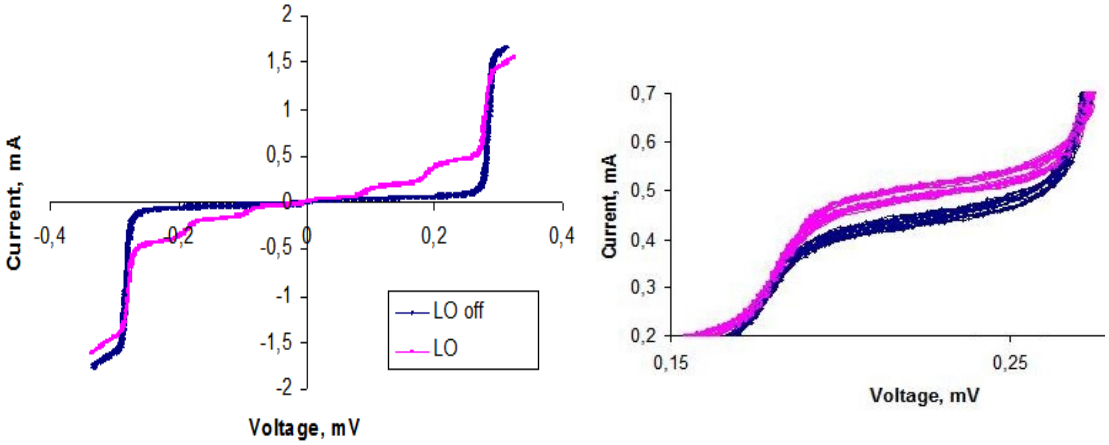


Figure 9.13. (Left) IV curves of SIS detector with and without RF signal. (Right) Steps on IV-curve in open and closed state of the switch.

The above experiments confirm that switching the nanostrip between the superconducting and normal states changes the finline transmission. At some frequencies, even the inverted switching was observed, i.e. the transmission was lower in the normal state than in the superconducting state. Most tested devices display proper switching of correct polarity at ~200 - 205 GHz and inverse switching at frequencies around 235 – 245 GHz. This is an indication that the kinetic inductance limits the switching ability, which effect becomes less significant at lower frequencies around 200 GHz and degrades switching at higher frequencies around 225 GHz and then leads to the inverted switching at even higher frequencies, 235 - 245 GHz.

9.6. Phase Switch with Multiple Bridges

For a switch operating at frequencies above 200 GHz, the total impedance including the component induced by the kinetic inductance of the bridge could be significant and even comparable with the characteristic impedance of the slotline, thereby degrading the performance of the switch. This can be alleviated using multiple bridge design that allows altering the total impedance of the switch perceived by the incident RF signal [Paper VI].

In this section, planar switch circuits with multiple nanobridges are considered. The circuit topology presented here comprises three narrow superconducting strips fabricated across a back-to-back unilateral finline [88], as shown in Fig. 9.14. These three bridges were produced of a 50 nm thick niobium nitride (NbN) film. Each NbN bridge is ~0.5 µm wide and 5 µm long, and the bridges are separated by a 50 µm long slotline. The whole circuit including the finlines is deposited on a quartz substrate and patterned using electron-beam lithography [115]. This switching circuit was designed to operate in the frequency range of 180 – 260 GHz.

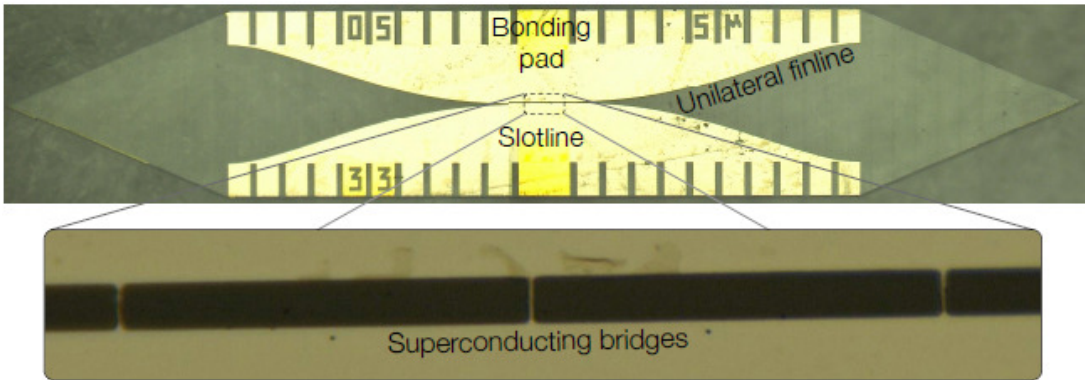


Figure 9.14. A planar superconducting switch circuit chip comprising three NbN bridges deposited across the slotline section of a back-to-back unilateral finline [Paper VI].

9.6.1. The analysis of the circuit

The transmission and the reflection of a switch and hence the switching ability of the circuit are determined primarily by the ratio between $Z_L = Z_{on}$ and $Z_L = Z_{off}$. An ideal switch would have high normal state resistance and zero superconducting kinetic inductance. At relatively low frequencies, this condition could be approached by employing highly resistive superconductors such as niobium titanium nitride (NbTiN) and NbN films. The RF impedance is, however, frequency dependent, and at higher frequencies exceeding ~200 GHz, the surface impedance induced by the kinetic inductance of the bridge could be rather high, approaching the characteristic impedance of the transmission line and possibly even the normal resistance value.

This reduces significantly the switching ability of the circuit at frequencies in a range around 200 GHz and above.

In order to alleviate this issue, a multiple bridge circuit topology can be used that allows optimizing the total impedance of the switch seen by the incoming RF signal in both normal and superconducting states. In Fig. 9.15, the RF power transmission is shown as an example dependence of the power transmission on the surface resistance of a superconducting strip across a slotline. Since this dependence is strongly nonlinear, the switching characteristics of the switch circuit can be significantly improved by modifying the surface impedance value.

Therefore, the initial design strategy based on a single bridge with high normal resistance could be changed to three NbN bridges in parallel made of a thicker film, which reduces R_N, but at the same time yields much smaller kinetic inductance L_k value (see Eq. 9.6 – 9.8).

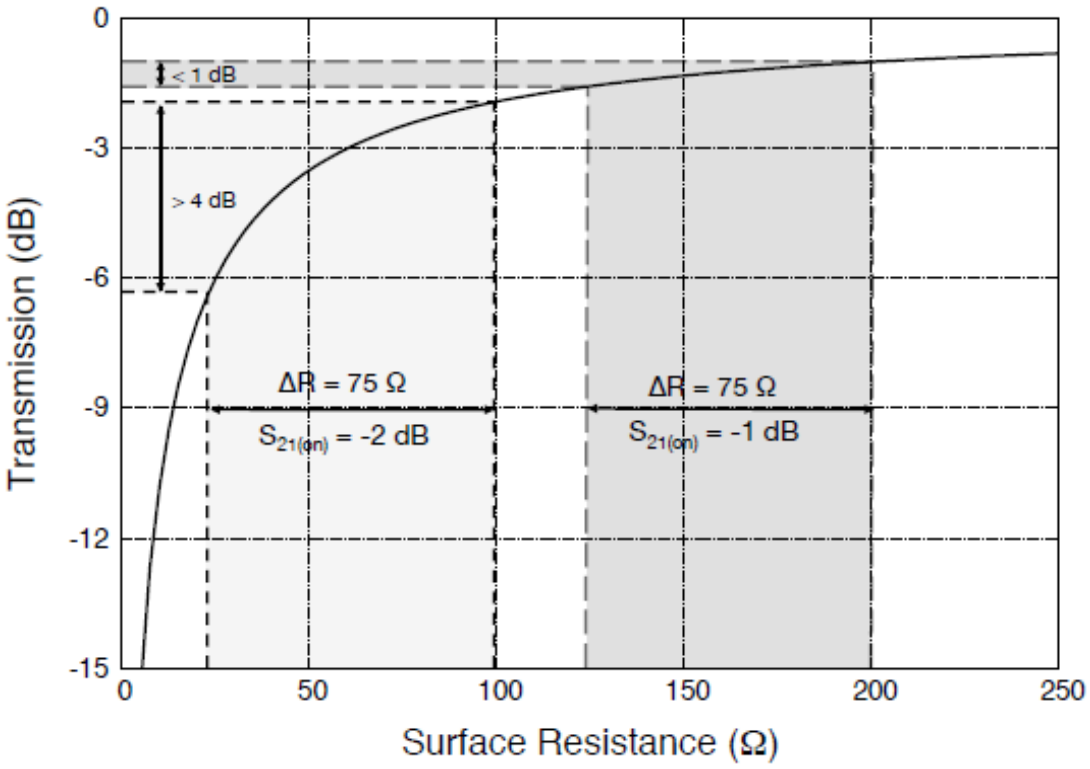


Figure 9.15. The relation between the surface resistance of a superconducting strip deposited across a slotline and its power transmission [Paper VI], according to Eq. 9.3.

A triple cascaded loads model shown in Fig. 9.16 was used for calculation of the characteristics of the triple-bridge design, with three loads representing the impedances of the NbN bridges.

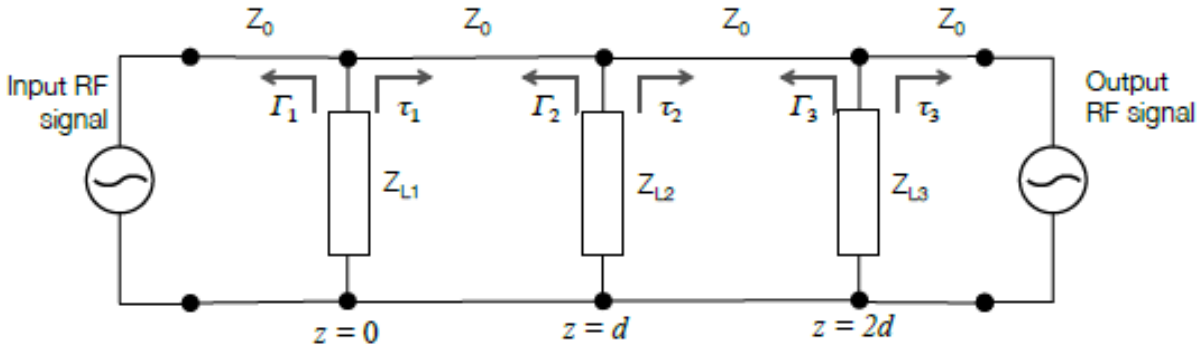


Figure 9.16. Transmission line model including a transmission line shunted with three loads.

To find the total transmission coefficient from the input to the output port, all three loads and distances between them and to the ports must be addressed. The reflection at the input (z = 0) and the transmission can be obtained by calculating the effective input impedance of Z_{L2} and Z_{L3} transformed by a transmission line of length d and 2d respectively, where d is the distance between two bridges. The input impedance at a distance l from the load can be expressed as

$$Z_L'(l) = Z_0 \frac{1+\Gamma(l)}{1-\Gamma(l)}, \qquad \text{where}$$

$$\Gamma(l) = \frac{-Z_0}{Z_0 + 2Z_L} e^{-i2\beta l}$$

The total impedance seen by the incoming signal at z = 0 will include three components as an outcome of three parallel loads. The output transmission and reflection coefficients for the complete circuit are obtained by substituting $Z_L = Z_{z=0}$ in Eq. 9.3, and for z = d and z = 2d.

For a 5 µm wide slotline with three nanobridges at a distance of 50 µm between them on a 100 µm thick quartz, the On/Off power ratio DP = τ^2_{on}/τ^2_{off} can be estimated as ~20 dB at 180 GHz and approximately 12 dB at 260 GHz, see Fig. 9.17. This gradual decrease can be explained by the increase in the kinetic inductance of the bridges at higher frequencies [Paper VI].

This transmission line model does not take into account the fringing effect of electromagnetic structures, such as the slotline. In reality, the field strength of a slotline is not fully confined between the two parallel electrodes, while a small part of it is fringed outside the slotline.

This can be analyzed by means of 3-D electromagnetic simulation, considering the switch circuit as a 3-D structure, which allows predicting its performance accurately. E.g., Ansys High Frequency Structure Simulator (HFSS) includes the fringing effect

and the superconductivity. The On/Off power ratio computed by HFSS is about 10 dB lower than the value obtained by the transmission line model (Fig. 9.17), as a result of HFSS taking into account the increase in the transmitted power in the superconducting state due to the fringing.

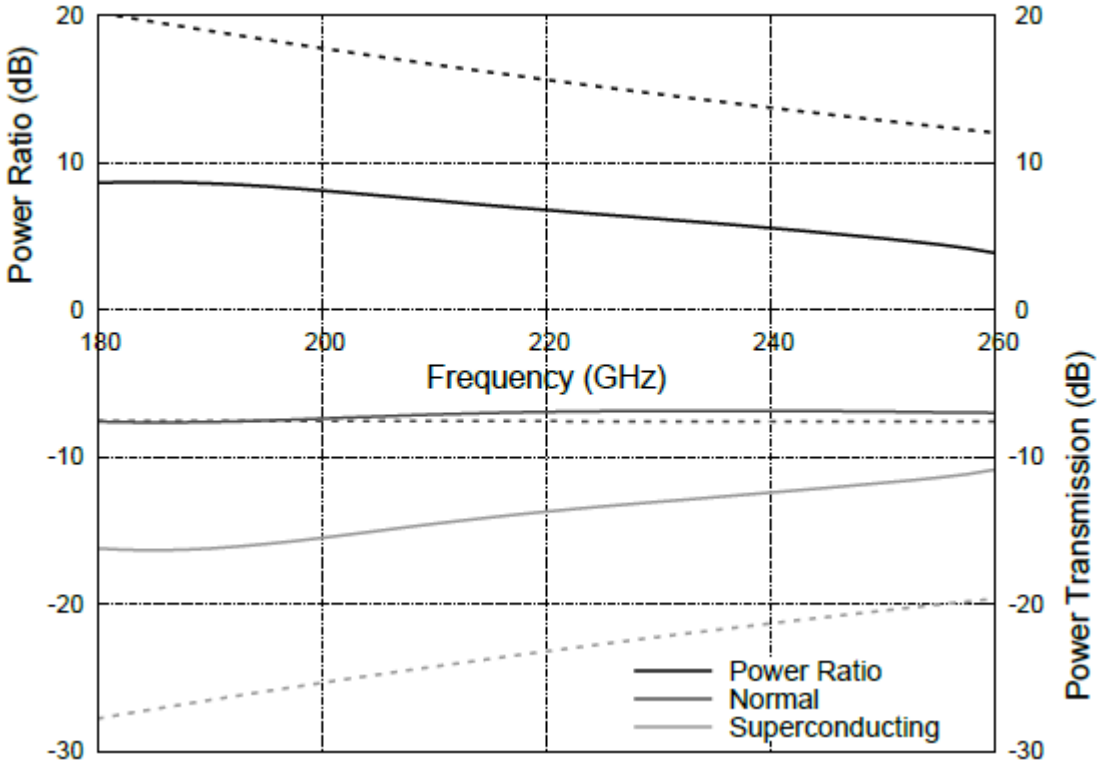


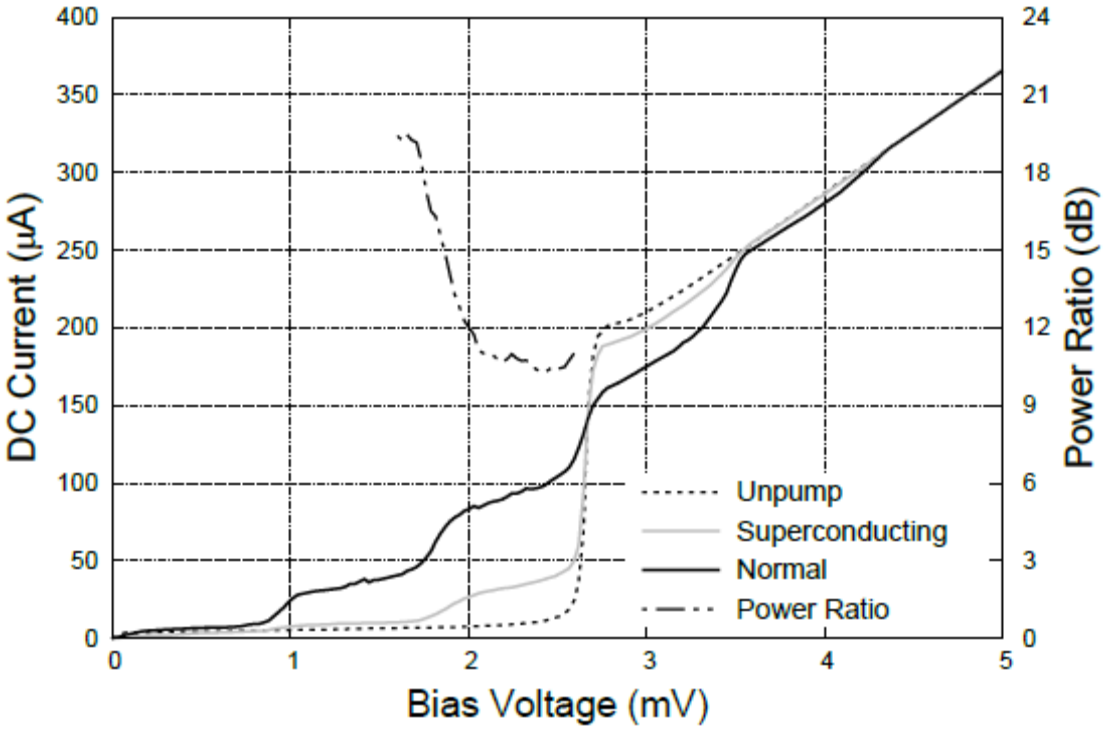
Figure 9.17. On/Off power ratio (black) and power transmissions (grey) of a slotline with three NbN bridges separated by 50 μm slotlines. The solid lines represent the predictions from HFSS model; the dashed lines show the calculated performances from the transmission line model [Paper VI]

9.6.2. Experimental results

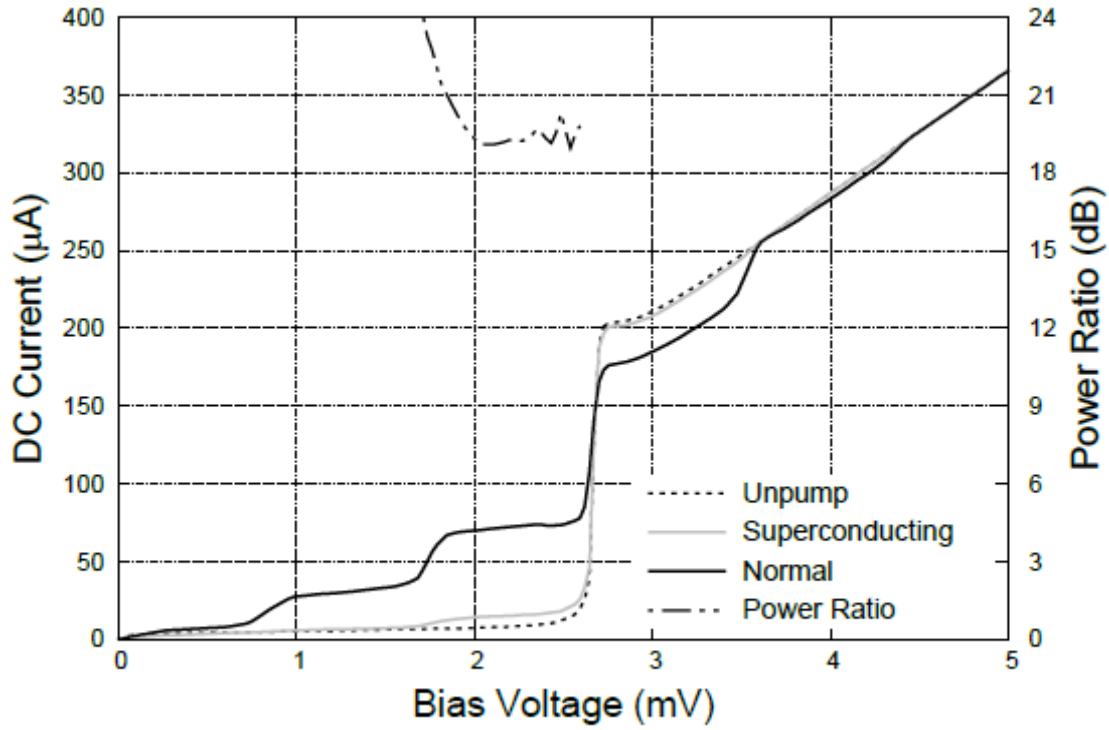
The switch circuit chip was positioned in a rectangular waveguide shown in Fig. 9.10, with a horn connected to its input. The RF signal incident onto one end of the chip was either transmitted towards the other end of the chip or reflected back to the input, depending on the state of the switch. A superconductor-insulator-superconductor (SIS) device operating in the same frequency range was placed after the switch chip (Fig. 9.10) to detect the transmitted RF power [116, Paper VI].

Both the switch and the SIS detector chip were located in an aluminium split block, which was mounted on the cold plate of a cryostat to cool both chips down to 4.2 K.

The switching characteristics of the switch are obtained by comparing the tunnelling current through the SIS device in the On and Off states at the same bias voltage values [117, Paper VI]



(a) $f_{RF} = 216$ GHz



(b) $f_{RF} = 230$ GHz

Figure 9.18. Normalized IV curves of the SIS devices illuminated with the RF source. The dashed lines labeled ”unpumped” represent IV curves in absence of RF signal. Power ratio between the switching states is shown above the IV curves as dot-dot-dash line [Paper VI]

In Fig. 9.18, current-voltage characteristics of the SIS device are shown, measured at 216 GHz and 230 GHz, respectively. The ratio between the power transmission in the On and Off states amounts about 11 dB at 216 GHz and ~20 dB at 230 GHz. This switching ratio is measured as the change in the tunnelling current, with reference to the current measured without any RF signal applied.

These experimental results demonstrated that the multiple bridge circuit topology is an efficient switch design to be used in RF circuits operating at frequencies around 200 GHz. The switching characteristics could be improved further by improving the matching of the chips to the waveguide; also, the joule heating of the chip could be minimized. One of drawbacks of the current design is the somewhat reduced total normal resistance of the switch, which decreases the power transmission in the normal state (see Fig. 9.15). This weakness can potentially be overcome by using advanced circuit topologies, such as e.g. resonant bridge architecture [118].

9.7. Conclusions

The planar NbN phase switch circuits with a 5 μm long nanostrip across the gap of a unilateral finline have been designed, fabricated, and tested in collaboration with Oxford University.

The successful operation of a planar On/Off switch was demonstrated, including RF experiments with devices comprising one to three NbN bridges deposited across a slotline section of a back-to-back finline. The NbN bridges were made to alternate between the superconducting and the normal state by passing a bias current of a magnitude either below or above the critical current value of the bridges. With Josephson and SIS devices used as direct detectors in different experiments, RF switching was observed with On/Off ratios of about 14 - 20 dB.

Time-domain switching observed at frequencies up to 100 kHz confirmed that the response time is sufficiently short for phase modulation in astronomical instrument. The switching speed was mainly limited by the time constant of the measurement system (5-10 μs). Real switching time of the nanobridge could be much shorter, if it is not limited by thermal effects.

The investigated planar phase shift circuits are easy to fabricate and they can be integrated in planar receivers. This allows replacing awkward mechanical switches with moving parts and rotary motors in cryostats by planar phase switch.

The low losses, the simplicity of the design and the fast response allows implementing of the proposed design in planar structures in a wide range of modulation frequencies, allowing cosmology instruments to be fabricated with many thousands of detectors.

Chapter 10
Summary

In this thesis, work on the development of millimeter-wave devices and circuits is reported, including CEB detectors based on Superconductor-Insulator-Normal metal (SIN) tunnel junctions, phase switch circuits and THz sensors. The operation principle of CEB detectors presented here relies on absorption of incident photons in a normal metal film and use of SIN tunnel junctions to measure a change in the electronic temperature of a normal metal absorber. The readout principle is based on a strong dependence of the tunneling current on the temperature and thus the SIN junction characteristics that depend on the temperature of the absorber. The devices presented in this thesis were fabricated by the author of this thesis using the fabrication procedures that he developed during his PhD research at Chalmers University in Sweden. The devices are designed for millimetre-wave receivers for sensitive measurements in new generations of telescopes.

The concept of the Cold-Electron Bolometer (CEB) as a sensitive millimeter-wave detector was examined, with focus on SIN tunnel junctions employed as readout of changes in the electronic temperature of normal metal. This concept was verified in several different implementations, including CEB devices integrated in 97-GHz unilateral finlines and CEBs integrated in other types of planar antennas for quasi-optical coupling, such as log-periodic antennas, 350 GHz double dipole antennas and cross-slot antennas.

Also, the electron cooling which is involved in the CEB operation and provides electro-thermal feedback, was considered in this thesis. The electro-thermal feedback is based on the cooling of the absorber that occurs when hot electrons escape the system through the tunnel junctions. This makes the saturation power of a CEB well above that of other types of millimeter-wave receivers.

Different fabrication techniques were developed for manufacturing CEBs and other detectors and microwave devices, such as Phase Switches, as well as SIN on-chip thermometers.

The concept of the on-chip SIN thermometer was examined. On-chip thermometers based on arrays of up to 100 SIN tunnel junctions fabricated using Direct-Write Trilayer technology are presented. A temperature resolution of ±5 μK is reported.

Cold-electron Bolometer integrated in a 97-GHz finline was fabricated using Direct-Write Trilayer technology, while depositing the CEB detector across a unilateral finline onto a planar substrate. Such a fabrication procedure involves the creation of both CEBs and finlines. In this configuration, CEB with SIN tunnel junctions is used for the signal detection, whilst a unilateral finline is used as a simple solution for planar microwave components that can be integrated on the same chip. The Trilayer fabrication technology used for fabrication of the CEB device was developed by the author of this thesis. The detector testing was performed in a cryostat at 280 - 315 mK using both an external RF power source and an internal black body source placed inside the cryostat.

A properly operating CEB device was demonstrated, with its performance evaluated, including the DC and RF characteristics. First, IV curves at different temperatures were measured, thus demonstrating the high quality of SIN tunnel junctions and the proper response to the bath temperature. Based on DC characteristics, the dark noise equivalent power for devices in the current biased mode operating at 300 mK, read out by room-temperature JFET electronics was estimated as NEP ~ $4 \cdot 10^{-16}$ W/Hz$^{1/2}$.

Then, the detector's optical response was measured by focusing an RF signal onto the waveguide input with the horn. The voltage response to the RF power was obtained; the estimated optical NEP reported in this thesis is about ~$3.8 \cdot 10^{-16}$ W/Hz$^{1/2}$ which approaches the requirements for CMB polarisation measurements. This demonstrates that the CEB-finline integrated circuit, assembled in a receiver system with a waveguide and a horn, is a feasible design for millimeter-wave detection.

The noise performance reported here was evaluated using the room-temperature amplifier box. As a result, the noise coming from the amplifier dominates the total noise measured. Thus, improved noise performance of CEB is expected, when using low-temperature readout electronics. Regarding the fabrication method used, a straightforward and robust technology was chosen for the production of these devices. This was a reasonable choice for developing this experiment, in that it allowed demonstrating the full functionality of the CEB detector integrated in a finline. However, the fabrication methods were not optimized in terms of device performance as the trilayer fabrication technology, used for manufacturing these devices, does not allow for a thin and narrow absorber. Thus, the volume of the absorber was not

chosen for the best responsivity. Further development of the design using advanced technologies and readout schemes, including low-temperature readout amplifiers combined with measurements in the voltage-biased mode, could potentially yield future improvements in the device performance.

Also, CEB devices integrated in other types of planar antennas, used for quasi-optical coupling, are reported, as well as the technology development for fabricating SIN tunnel junctions and CEB devices. CEB detectors fabricated using advanced technologies, are presented, integrated in log-periodic, double-dipole and cross-slot antennas. The CEB performance was evaluated and the experimental results analyzed.

The design of the CEB detectors was investigated, and experimental results presented, including the testing of CEBs comprising a thin Ti film absorber and two SIN junctions integrated in a log-periodic antenna or a 350 GHz double dipole antenna. Both designs are presented, with the devices fabricated using a novel approach for fabricating Ti-TiO_X-Al tunnel junctions, developed by the author of this thesis. This is a simple and efficient technology for fabrication of SIN tunnel junctions between Ti and Al with TiO_X as an insulating barrier. This is done by depositing a normal Ti film as a bottom electrode and the superconducting Al film on the top of it after creating a TiO_X insulating barrier by *ex-situ* oxidation of Ti.

The CEB performance was evaluated at 300 mK using the hot-cold method and using a black-body source that is heated and controlled by an external current. The reported data include results of DC and RF experiments on a CEB deposited across a double dipole antenna and another one fed by a log-periodic antenna on a planar Si substrate. The fabricated junctions are rather high-ohmic due to a very long oxidation time used for creating tunnel barriers. Shortening the oxidation time and combining it with a proper choice of temperature should allow creating more low-ohmic tunnel junctions.

Measurements using the above methods have yielded NEP ~3.5×10^{-17} W/$Hz^{1/2}$ to ~9×10^{-17} W/$Hz^{1/2}$, which is close to the CMB power level. Design improvements, use of series arrays of SIN junctions and improvements of the readout are expected to yield an NEP level below 1×10^{-17} W/$Hz^{1/2}$.

Therefore, the detector can be a potential candidate for the next generation of space cosmology missions and is also of interest to ground-based astronomical experiments as a result of the simplicity of its integration to planar circuit technology, high saturation power and fast response.

Next, experimental results are presented on the testing of CEB detectors comprising a non-superconducting thin absorber made of CrO_x/Cr/Al film and an array of SIN tunnel junctions integrated in a planar cross-slot antenna. Each antenna contains two series / parallel arrays of 10 Cold-Electron Bolometers with SIN tunnel junctions

integrated in orthogonal ports of the antenna. Bolometric devices made of a normal metal absorber and 4 SIN tunnel junctions in a 4-probe test structure were also investigated. The CEB devices, integrated in cross-slot antennas, were fabricated using Advanced Shadow Evaporation technology and designed for balloon-borne telescope projects that are dedicated to the CMB measurements.

The CEB detectors were tested in a ^{3}He sorption cryostat HELIOX-AC-V at bath temperatures of 280 to 350 mK and in a dilution refrigerator TRITON down to 50 mK. High performance IV curves demonstrate that this technology is suitable for detector fabrication, and also RF experiments on the measurements of the voltage response to the incoming signal power are presented. The optical response was measured using the hot/cold load method by flipping a reflector opposite a blackbody surface inside a 3 K shield in a cryostat. In addition, electron cooling was investigated that increases the dynamic range of the device.

The reported estimated noise equivalent power in the current biased mode as read out by room temperature electronics is NEP ~$2.5 \cdot 10^{-17}$ W/Hz$^{1/2}$. Voltage to temperature response of around dV/dT = 8.8 μV/mK is reported for 10 devices in series, and the dynamic range over 40 dB was demonstrated, measured at the temperature of 280 mK for arrays of cold-electron bolometers integrated in a cross-slot antenna. Moderate electron cooling by up to 100 mK is reported, which improves the NEP of the detector and increases the dynamic range.

The above results reported in this thesis have demonstrated that the CEB device is an operating millimeter-wave detector with high sensitivity and a large dynamic range that prevents saturation of the system, which can easily be fabricated on planar substrates and integrated into planar antennas.

Semiconductor plasmonic detectors for radio imaging employing quantum dot and single point contacts and operating in THz frequency range are presented, including fabrication technology and experimental results. The operation of the THz detector has been investigated, and the electrostatic model of the system introduced and examined, with a set of equivalent capacitances determined.

THz devices can be employed in radio astronomy and in other areas, such as security screening, environment monitoring or medical diagnostics.

Also, planar phase switch circuits are presented, including NbN devices based on single and multiple nanostrips and integrated in unilateral back-to-back finlines, operating at 200 - 245 GHz. The phase switch circuits were designed in order to replace mechanical switches for signals in waveguides. The presented fully planar design allows switching the microwave signal between two branches of a circuit with low losses and high speed.

The investigated planar phase shift circuits were fabricated by the author of this thesis and tested at Chalmers and Oxford. The phase modulation scheme can be integrated in planar circuits and systems and used in high-precision astrophysical experiments such as the investigation of the polarization of the CMB. The scheme could allow to measure Stokes parameters without moving the optics and to improve the sensitivity.

Switching characteristics of the devices are reported, and the switching rate is demonstrated to be well above that required for phase modulation in astronomical instruments. The speed is mainly limited by the time constant of the measurement system (~10 μs), while the real switching time of a nanobridge is much shorter.

This confirms that the concept of signal switching using a superconducting nanostrip is a promising technology. The efficiency of the switching could be potentially enhanced by modifying the geometry of the circuits and using capacitively coupled devices. Layouts with advanced geometries are currently under development.

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Fabrication recipes

A.1. Thick gold (Pads, antennas, finlines, marks, and wires)

- rinse an oxidized silicon wafer with acetone and isopropanol on a spinner
- spin the lift-off resist LOL-2000 or LOR3A at 3000 rpm
- bake for 10 min on a hot plate at 180-200 °C
- spin photo resist S-1813 at 4000 rpm
- bake for 90s on a hot plate at 110 °C
- expose for 50s at 1.5 mW/cm^2 (exposure time adjusted with intensity)
- develop in MF319 for 2.5 min
- rinse with water, blow dry
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- evaporate 10 nm Cr and 140 nm Au
- lift-off in Shipley 1165 Remover at 60 °C

A.2. Thin gold

- rinse the wafer with acetone and isopropanol on a spinner
- spin the lift-off resist copolymer 10% at 3000-4000 rpm
- bake for 5-10 min at 155-160 °C on a hotplate
- spin the top resist layer PMMA 2-4% at 3000-4000 rpm
- bake for 5-10 min at 155 °C on a hotplate
- expose the pattern in e-beam machine with dose of 320 μC/cm^2
- develop the top resist in Toluene:IPA during 1-2 min
- rinse in isopropanol, blow dry
- develop the bottom resist using EtylCellosolveAcetat (ECA) : Etanol 1:5, for 3-5min (or in another solvent)
- rinse with isopropanol, blow dry
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- evaporate 10 nm Cr, 30 nm Au and 10nm Pd.
- Lift-off in acetone at 40-42 °C

A.3. Trilayer structure

- rinse the wafer or diced set of chips with acetone and isopropanol.
- spin the copolymer 10% at 4000 rpm
- bake for 5-10 min at 155-160 °C on a hotplate
- spin the top resist layer PMMA 2-4% at 3000-4000 rpm
- bake for 5-10 min at 155 °C on a hotplate
- expose the pattern in e-beam machine using a dose of 320 $\mu C/cm^2$
- develop the top resist in Toluene:IPA
- rinse in isopropanol, blow dry
- develop the bottom resist using ECA:Etanol 1:5 (or in another solvent , e.g. IPA:H_2O 93:7 if another top resist used for selective development)
- rinse with isopropanol, blow dry
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- evaporate 20-40 nm of Al
- oxidize Al in Oxygen at 5×10^{-2} mbar for 2-30 min.
- evaporate 7-10 nm of Cu
- evaporate 8-10 nm of Au for passivation
- lift-off in acetone at 40-42 °C

A.4. Absorber/Normal metal electrode

- rinse the wafer with acetone and isopropanol on a spinner
- spin the lift-off resist copolymer 10% at 3000-4000 rpm
- bake for 5-10 min at 105-140 °C on a hotplate or 1 hour in vacuum oven
- spin the top resist layer PMMA 2-4% at 3000-4000 rpm
- bake for 5-10 min at 105-140 °C on a hotplate or 1 hour in vacuum oven
- expose the pattern in e-beam machine with dose of 320 $\mu C/cm^2$
- develop the top resist in Toluene:IPA during 1-2 min
- rinse in isopropanol, blow dry
- develop the bottom resist using EtylCellosolveAcetat:Etanol 1:5 for 3-5min (or possibly in another solvent , e.g. IPA:H_2O 93:7, see A.3)
- rinse with isopropanol, blow dry
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- evaporate 20-40 nm Cu and 20-40 nm Cr (or 5-40 nm Ti on top of Cu)
- lift-off in acetone at 40-42 °C
- ion mill for 5-6 min using CAIBE #417 at 300 V, 7 mA.

B.1.1. Ti absorber for Ti-based technology (negative patterning)

- deposit 20-30 nm of Ti in magnetron Nordiko2000 #400 at 100W
- spin photo resist S-1813 at 4000 rpm
- bake for 90s on a hot plate at 110 °C
- expose for 50s at 1.5 mW/cm^2
- develop in MF319 for 50s
- soak in Toluen
- post-bake on hotplate at 110 °C for 1 min.
- etch Ti in 1% HF: water solution for 30s
- rinse with water
- ion mill for 6 min using CAIBE #417 at 500V, 10 mA.
- oxidize in oven at 130-150 °C during 1-10 hours

B.1.2. Ti absorber for Ti-based technology (positive patterning)

- rinse a wafer with acetone and isopropanol on a spinner
- spin the lift-off resist LOL-2000 or LOR3A at 3000 rpm
- bake for 10 min on a hot plate at 180-200 °C
- spin photo resist S-1813 at 4000 rpm
- bake for 90s on a hot plate at 110 °C
- expose for 50s at 1.5 mW/cm^2 (exposure time adjusted with intensity)
- develop in MF319 for 2.5 min
- rinse with water, blow dry
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- deposit ~ 20-30 nm Ti in Nordiko2000 #417 in Ar plasma at 100 W
- lift-off in Shipley 1165 Remover at 60 °C
- rinse with water
- ion mill for 6 min using CAIBE #417 at 500V, 10 mA.
- oxidize in oven at 130-150 °C during 1-10 hours

B.2. Al electrode for Ti-based technology

- deposit 50-120 nm of Al on the wafer with oxidized Ti absorber
- spin photo resist S-1813 at 4000 rpm
- bake for 90s on a hot plate at 110 °C
- expose for 50s at 1.5 mW/cm^2
- develop in MF319 for 50s
- clean for 30s in oxygen plasma, process ash_30s in Batchtop #319
- etch Al for 2-5 min in ALETS etchant (containing ~85% H_3PO_4 etc)
- rinse with water, blow dry
- remove the photoresist in Shipley 1165 remover

C. NbN nanobridge for Phase Switch

- (optionally) deposit ~ 1 nm Ti in Nordiko2000 #417 in Ar plasma at 100 W
- deposit 22-50 nm NbN in Nordiko2000 #417 in 4:1 Ar:N_2 plasma at 1.4 A
- pattern and deposit gold pads, wires and finlines (recipe A.1.)
- spin e-beam resist SAL-601 at 3000-4000 rpm
- expose rough pattern on 4^{th} lens and/or fine pattern on 5^{th} lens by e-beam
- bake at 105-108 °C for max 90s on hotplate
- develop in MF322 for 4 – 12 min , depending on baking conditions
- etch NbN in CF_4 plasma for 1min 45s using Oxford RIE #404
- remove the e-beam resist in Shipley 1165 remover

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