Encapsulation of graphene in Parylene

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Graphene encapsulated between flakes of hexagonal boron nitride (hBN) demonstrates the highest known mobility of charge carriers. However, the technology is not scalable to allow for arrays of devices. We are testing a potentially scalable technology for encapsulating graphene where we replace hBN with Parylene while still being able to make low-ohmic edge contacts. The resulting encapsulated devices show low parasitic doping and a robust Quantum Hall effect in relatively low magnetic fields <5 T. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4975491]

The most common substrate for graphene has historically been an oxidized silicon.[1] The advantage of this substrate lies in the possibility of seeing the graphene flakes after exfoliation.[2] However, SiO_2 is highly hydrophilic, which promotes parasitic doping in the graphene.[3,4] This problem can be partially solved by annealing graphene on SiO_2 at high temperatures[5] or by separating graphene from SiO_2 by a hydrophobic layer of e.g., hexamethyldisilazane (HMDS).[6,7] However, sometimes, annealing even reduces the charge-carrier mobility.[5] It is also possible to reduce the doping of graphene devices with UV light illumination, but after some time, the doping returns to the initial state in ambient conditions.[8] All this points to a need for another substrate for graphene.

Nowadays, the best graphene devices are based on encapsulation of graphene in hexagonal boron nitride (hBN).[9] Such devices show a very high mobility and low doping.[10,11] A great advantage of the hBN-graphene-hBN heterostructure lies in the possibility of fabricating low-resistive one-dimensional (1D) edge contacts to them, avoiding the exposure of the graphene surface to resists.[11] However, it requires a sophisticated technique[12] and high quality hBN which seem to be only available in one laboratory.[13]

Encapsulation of graphene is used to protect it from the local environment and sometimes even from the chemicals used during the lithography process. Different combinations of encapsulating materials can be used, i.e., those still having SiO_2 under graphene, in combination with e.g., PMMA[14,15] or Parylene[16] on top. Epitaxial graphene on SiC can also be encapsulated from the top with PMMA, and the charge-neutrality point can be shifted to zero with UV light[17] or by using discharges.[18]

In this paper we introduce graphene encapsulation in Parylene as a potentially scalable replacement for hBN. Parylene is an oxygen-free polymer with a dielectric constant of the same order as that of SiO_2.[19] This polymer can easily be deposited using commercially available systems and is widely used in industry.[20] Importantly, we show that after encapsulating graphene inside Parylene it is possible to fabricate 1D edge contacts, in a similar manner to hBN-graphene-hBN structures. These contacts show a low resistance, which

is beneficial for many types of graphene devices. Also, the graphene devices encapsulated in Parylene show low doping and high mobility. The Quantum Hall Effect (QHE) is observed in relatively low magnetic fields (~4–5 T).

Although the CVD graphene is more suitable for scalable device technology, we use exfoliated graphene to start with a well-characterized material and exclude unknown parameters.[16] We use a commercial coating system (specialty coating systems (SCS)) to deposit Parylene (150 nm) on SiO_2(90 nm)/Si chips. The overall thickness of the transparent layer is adjusted to yield a high optical contrast for the graphene laid on it, which allows the potentially useful monolayer flakes to be easily identified. In contrast to bare SiO_2/Si-substrates, we cannot use oxygen plasma for the last minute cleaning of the surface, since it would partially etch Parylene and possibly result in some residual oxygen at the surface. After flake detection, the samples are immediately covered with another Parylene layer to seal the graphene before subsequent fabrication steps. The contrast of the flakes degrades somewhat due to the second Parylene layer, but still allows for an optical alignment during the lithography step (see Figure 1). The device lithography patterning process consists of two steps: first to define the Hall-bar shape of the device and then to deposit contacts. We use a 370 nm thick layer of e-beam resist ZEP 520A to protect the structure during the relatively long plasma etching needed to etch through both layers of Parylene (150 + 90 nm). The etching of the Parylene/graphene/Parylene structure is
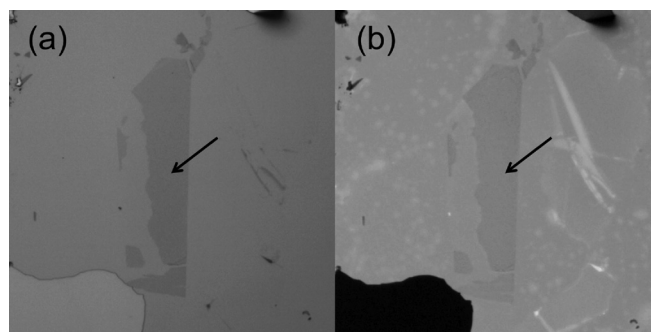

FIG. 1. Optical image of a graphene flake (marked with arrows) exfoliated on Parylene N (150 nm)/SiO_2 (84 nm)/Si before (a) and after (b) the deposition of the top Parylene layer (90 nm). The contrast of graphene is sufficiently high to allow for the optical alignment during device fabrication.

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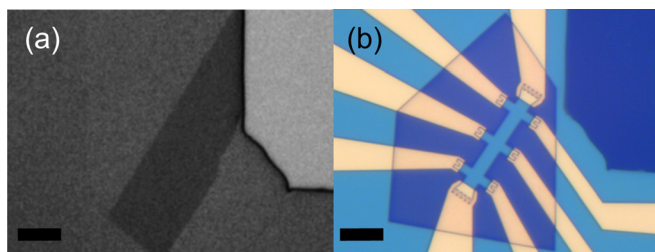
FIG. 2. Optical image of an 8-terminal Hall-bar device (b) fabricated from Parylene-encapsulated graphene (a). The electrode "legs" are cut in combs in order to increase the contact length and thereby reduce the overall contact resistance. The scale bars are $10\,\mu m$.

FIG. 4. Tapping mode AFM scans of SiO_2 (84 nm)/Si (a) and Parylene N (150 nm)/SiO_2 (84 nm)/Si (b). The roughness values are 0.27 nm (a) and 2.0 nm (b). The size of both images is $10 \times 10\ \mu m^2$.

performed in 40 W oxygen plasma at 250 mTorr resulting in an approximate etching rate of 120 nm/min. The contacts to the defined graphene device are fabricated using a bilayer e-beam resist (60 nm of PMMA on top of 360 nm of MMA copolymer), followed by the deposition of three metal layers Cr (1 nm)/Pd (15 nm)/Au (200 nm), which is very similar to what has been used for the original hBN-encapsulated devices.[11] A somewhat thicker layer of gold is used in order to ensure the 240 nm high step coverage. A finished Parylene/graphene/Parylene Hall-bar structure is presented in Figure 2. For some of our devices, the legs have comb structures at the ends in order to increase the length of the edge contacts and therefore reduce their overall resistance.

We have used two types of Parylene, Parylene N, and Parylene C. The difference between the monomer units of these compounds is the presence of a Cl atom in Parylene C (see Figure 3). Both these polymers have similar deposition processes and can be deposited using the same system. The deposition process starts with evaporating Parylene dimer at 160–175 °C, followed by cracking the dimer to monomers at 650–690 °C, and finishes by polymerization on the surfaces of everything in the main chamber, including the samples. The final thickness of the Parylene layer and the deposition rate are controlled by the initial mass of the dimer and the process pressure respectively.[21] We have characterized the surface morphology of both Parylenes deposited on SiO_2/Si chips with the aid of an Atomic Force Microscope (AFM). As presented in Figure 4, a bare 84 nm thick SiO_2 has a RMS roughness value of 0.27 nm. When a similar chip is covered with 150 nm of Parylene N, the roughness is 2.0 nm, an order of magnitude larger. The films of Parylene C have approximately twice the roughness of Parylene N. We have observed that the roughness depends on the chamber pressure during Parylene deposition. For Parylene N deposited at 16 mbar, the roughness is 4.0 nm, whereas for 12 mbar, it is 2.0 nm. This pressure can be set even lower, but the deposition rate then decreases as well, making the fabrication process excessively long. Most of our samples have been covered with
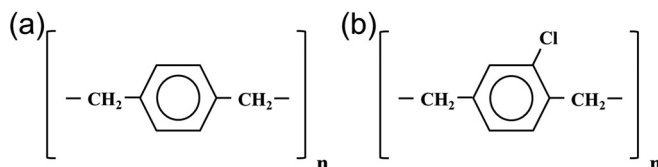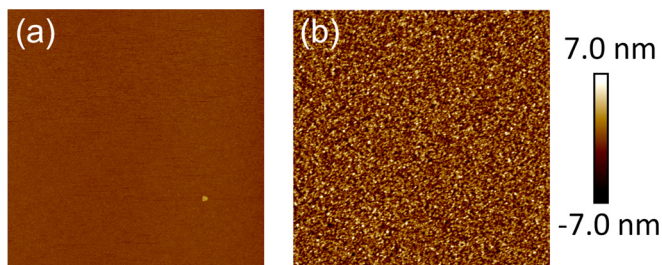
Parylene N at 12 mbar, which appears to be a trade-off between increased roughness and deposition time. We use a highly doped Si base as a backgate electrode to change the charge-carrier type and concentration in graphene.

In Figure 5, we show the channel resistance R_{xx} vs. the backgate voltage V_g for the fabricated devices. The voltage corresponding to the charge-neutrality point for all our devices made with Parylene N does not exceed 10 V, indicating a low background doping of the devices $<3.0 \times 10^{11}\,cm^{-2}$. This low doping can be explained by the chemical inertness and hydrophobicity of Parylene N. In our case, graphene is exfoliated directly onto the hydrophobic substrate and after that is immediately encapsulated with the top Parylene layer. This minimizes the graphene exposure time to ambient conditions. All the lithography steps are performed after encapsulation, so the graphene is not in contact with anything, but the Parylene during the fabrication process.

On the other hand, we see a significant ($>2.3 \times 10^{12}\,cm^{-2}$) background doping for Parylene C devices. Unlike Parylene N which has only C and H atoms in its formula, the presence of Cl in Parylene C makes the molecules polar and thereby creates extra doping in graphene. Indeed, Parylene C has recently been found to be a useful piezoelectric material.[22] This also supports the earlier hypothesis, that a good substrate for graphene should not have oxygen or any other strongly electronegative atoms in its chemical formula.[23]

For some devices, we have performed annealing in an inert atmosphere at 250 °C in order to produce a possible improvement in the transport properties. As has previously

FIG. 3. Chemical formulas of Parylenes N (a) and C (b) used for graphene encapsulation.
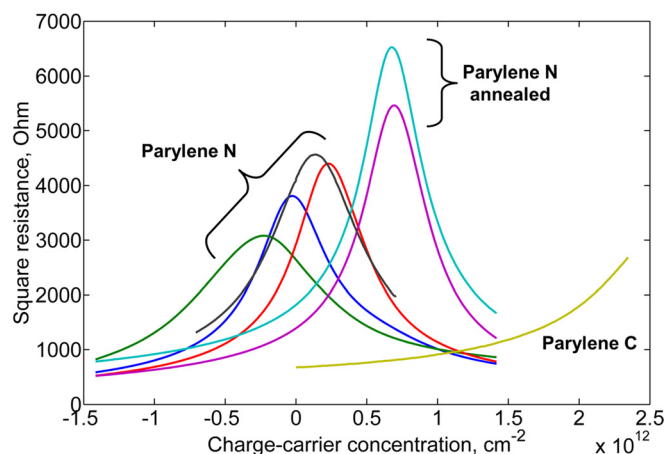

FIG. 5. Field-effect curves for Parylene-encapsulated graphene devices at 300 K. The resistance is normalized to the number of squares for each device.

been reported, the charge-carrier mobility can increase after annealing.[24] In our experiments we observe that if the annealing is done on a finished device, it drastically increases the contact resistance from $1-10\,\Omega$ to more than $100\,k\Omega$, rendering the device impractical. However, if the annealing is performed before the lithography process, the final device has the usual contact resistance ranging from 1 to $10\,\Omega$, while the mobility increases. Clearly, it is impossible to measure and compare the properties of the same device before and after annealing.

We estimate the charge-carrier mobility μ in our devices in two ways, by fitting the $R_{xx}(V_g)$-curves with the model dependence[25] and/or from the Hall-resistance R_{xy} measurements in a magnetic field. The best value measured for our encapsulated devices is $\mu = 16\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at $T = 2\,K$ which is still much lower than the μ reported for hBN-based ones.[11] We explain this by a significant surface roughness difference between atomically flat hBN flakes and Parylene on SiO_2. Nonetheless, we have observed QHE for all the fabricated devices in a magnetic field as low as 4–5 T. In Figure 6, we present a typical 3D-plot of the resistance vs. V_g and the magnetic field B, which reveals the well-defined Landau levels and zero-resistance QHE plateaus.

The edge contact resistance between graphene and a metal film can be extracted from the three probe measurements in the QHE regime where the longitudinal resistance turns to be zero.[26] We get values as low as $14\,\Omega\,\mu m$ which is slightly less than that reported for hBN-encapsulated graphene[11] and is much lower than the resistance of typical surface contacts.[27]

We have also performed the critical current measurements for one of the devices, depicted in Figure 7. In this experiment the device is first brought to the QHE regime ($B = 8\,T$, $T = 2\,K$ in this case) and the backgate voltage is then used to zero the device resistance within a Hall plateau. After that, the current is swept upwards from the initial low value. The current value at which the resistance starts to grow significantly is taken as the critical current. It depends on the distance from the nearest edge of the Hall plateau,
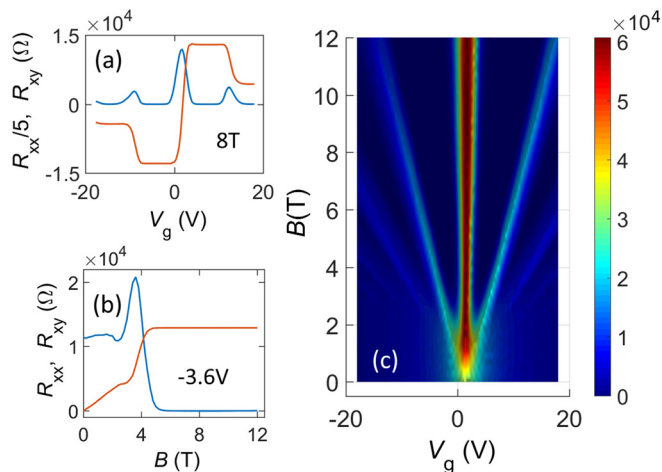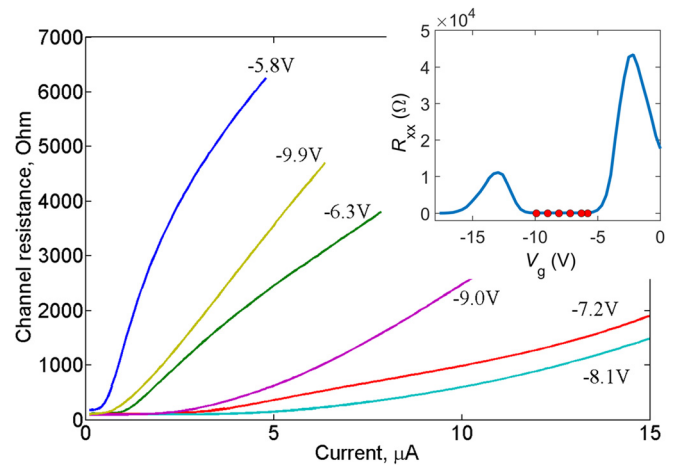

FIG. 7. Critical current measurements for one of the Parylene-encapsulated graphene devices at 2 K and 8 T. The graphene channel width is 3 μm.

and has its maximum value around 1 $\mu A/\mu m$, which is of the same order as previously reported[28] (see Figure 7).

In summary, we have demonstrated a technology for graphene encapsulation using Parylene, a compound well-established in industry, as a dielectric. We have shown that it is possible to make 1D edge contacts with these structures. The contacts have a low resistance comparable with the values reported for state-of-the-art hBN-encapsulated graphene. Our devices show a high charge-carrier mobility and low doping, resulting in QHE at relatively low magnetic fields. Our encapsulation technique is much easier than when using hBN flakes. This technology can be scaled up for large areas of CVD graphene and allows for the stability of device characteristics.

FIG. 6. (a) The longitudinal (R_{xx}, blue) and Hall (R_{xy}, red) resistances as a function of V_g at $B = 8\,T$. (b) $R_{xx}(B)$, and $R_{xy}(B)$ at $V_g = -3.6\,V$. Note the well-defined plateaus of the QHE. (c) 3D-plot of $R_{xx}(V_g, B)$. The temperature is 2 K. $V_g = 20\,V$ corresponds to the charge density of $1.4 \times 10^{12}\,cm^{-2}$.

[1]K. S. Novoselov, S. V. Morozov, T. M. G. Mohinddin, L. A. Ponomarenko, D. C. Elias, R. Yang, I. I. Barbolina, P. Blake, T. J. Booth, D. Jiang, J. Giesbers, E. W. Hill, and A. K. Geim, Phys. Status Solidi B 244(11), 4106 (2007).
[2]P. Blake, E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim, Appl. Phys. Lett. 91(6), 063124 (2007).
[3]R. A. Nistor, M. A. Kuroda, A. A. Maarouf, and G. J. Martyna, Phys. Rev. B - Condens. Matter Mater. Phys. 86(4), 041409(R) (2012).
[4]S. K. Hong, S. M. Song, O. Sul, and B. J. Cho, J. Electrochem. Soc. 159(4), K107 (2012).
[5]Z. Cheng, Q. Zhou, C. Wang, Q. Li, C. Wang, and Y. Fang, Nano Lett. 11(2), 767 (2011).
[6]S. F. Chowdhury, S. Sonde, S. Rahimi, L. Tao, S. Banerjee, and D. Akinwande, Appl. Phys. Lett. 105(3), 033117 (2014).
[7]M. Lafkioti, B. Krauss, T. Lohmann, U. Zschieschang, H. Klauk, K. v. Klitzing, and J. H. Smet, Nano Lett. 10(4), 1149 (2010).
[8]A. Yurgens, N. Lindvall, J. Sun, Y. Nam, and Y. W. Park, JETP Lett. 98(11), 704 (2014).
[9]A. K. Geim and I. V. Grigorieva, Nature 499(7459), 419 (2013).
[10]L. Banszerus, M. Schmitz, S. Engels, J. Dauber, M. Oellers, F. Haupt, K. Watanabe, T. Taniguchi, B. Beschoten, and C. Stampfer, Sci. Adv. 1(6), e1500222 (2015).
[11]L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean, Science 342(6158), 614 (2013).

[12]P. J. Zomer, M. H. D. Guimarães, J. C. Brant, N. Tombros, and B. J. van Wees, Appl. Phys. Lett. **105**(1), 013101 (2014).

[13]Y. Kubota, K. Watanabe, O. Tsuda, and T. Taniguchi, Chem. Mater. **20**(5), 1661 (2008).

[14]A. Sundararajan, M. J. Boland, D. Patrick Hunley, and D. R. Strachan, Appl. Phys. Lett. **103**(25), 253505 (2013).

[15]T. Yager, A. Lartsev, R. Yakimova, S. Lara-Avila, and S. Kubatkin, Carbon **87**, 409 (2015).

[16]S. S. Sabri, P. L. Lévesque, C. M. Aguirre, J. Guillemette, R. Martel, and T. Szkopek, Appl. Phys. Lett. **95**(24), 242104 (2009).

[17]S. Lara-Avila, K. Moth-Poulsen, R. Yakimova, T. Bjørnholm, V. Fal'Ko, A. Tzalenchuk, and S. Kubatkin, Adv. Mater. **23**(7), 878 (2011).

[18]A. Lartsev, T. Yager, T. Bergsten, A. Tzalenchuk, T. J. B. M. Janssen, R. Yakimova, S. Lara-Avila, and S. Kubatkin, Appl. Phys. Lett. **105**(6), 063106 (2014).

[19]V. Kale and T. Riley, IEEE Trans. Parts, Hybrids, Packag. **13**(3), 273 (1977).

[20]See http://scscoatings.com/ for information about various Parylene coatings and their applications in industry; accessed 05 December 2016.

[21]B. E. Rapp, A. Voigt, M. Dirschka, and K. Länge, Thin Solid Films **520**(15), 4884 (2012).

[22]J. Y. H. Kim, A. Cheng, and Y. C. Tai, paper presented at the 2011 IEEE 24th International Conference on Micro Electro Mechanical Systems, 2011.

[23]Y.-P. Hsieh, C.-L. Kuo, and M. Hofmann, Nanoscale **8**(3), 1327 (2016).

[24]K. Alexandrou, F. Farmakis, A. Arapis, N. Georgoulas, Y. Hao, J. Hone, and I. Kymissis, J. Vac. Sci. Technol. B **34**(4), 041805 (2016).

[25]S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **94**(6), 062107 (2009).

[26]T. Yager, A. Lartsev, K. Cedergren, R. Yakimova, V. Panchal, O. Kazakova, A. Tzalenchuk, K. H. Kim, Y. W. Park, S. Lara-Avila, and S. Kubatkin, AIP Adv. **5**(8), 087134 (2015).

[27]M. Politou, I. Asselberghs, I. Radu, T. Conard, O. Richard, C. S. Lee, K. Martens, S. Sayan, C. Huyghebaert, Z. Tokei, S. De Gendt, and M. Heyns, Appl. Phys. Lett. **107**(15), 153104 (2015).

[28]V. Singh and M. M. Deshmukh, Phys. Rev. B **80**(8), 081404(R) (2009).