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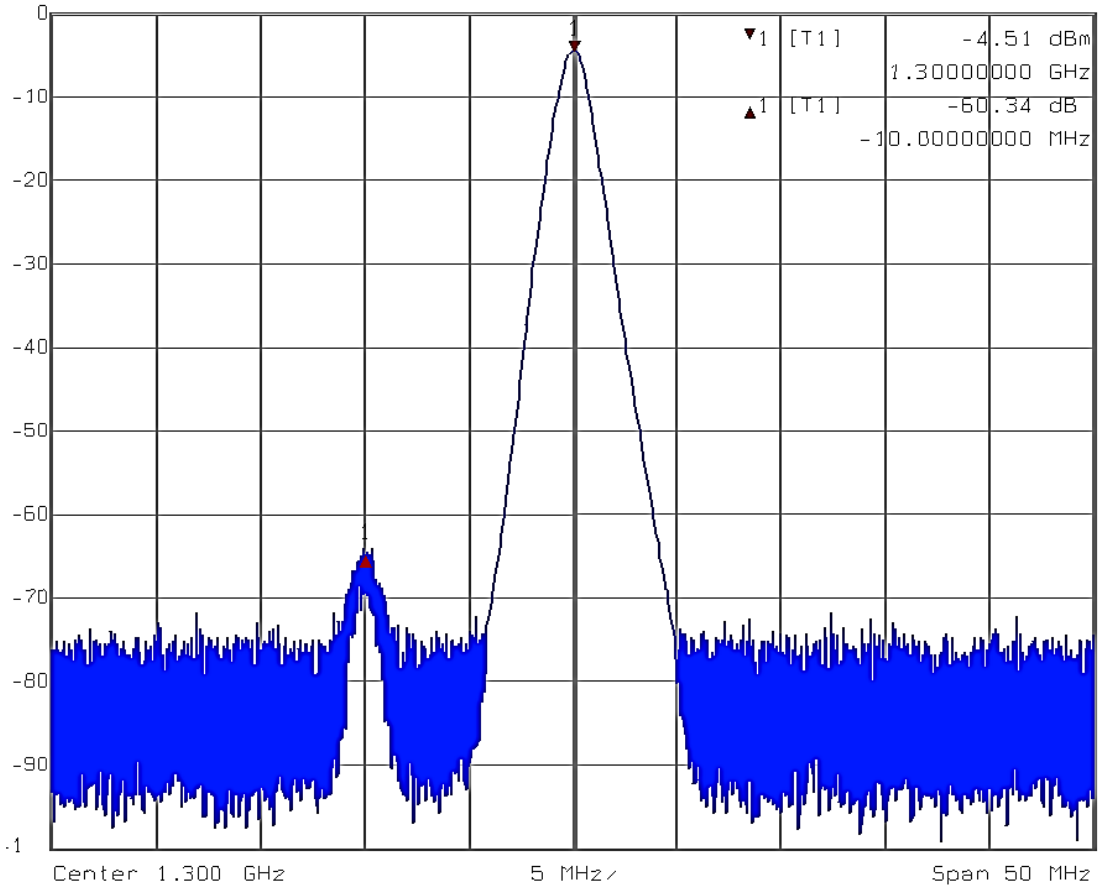

Performance evaluation of a software defined multi-channel transceiver for radar systems

Degree project in Electrical Engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY

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Thesis for the Degree of Bachelor of Science in Engineering

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Abstract

Radar systems are becoming more and more digital. This allows for lighter and more affordable systems on the market. This degree project is about performance evaluation of a digital transceiver for radar systems. The evaluated transceiver consist of multiple analog-to-digital converters(ADC), digital-to-analog converters(DAC) and sampling clocks for the converters. The report deals with the difficulties and problematics of measuring the sampling and reconstruction progress of radar signals. The methodologies to measure non-trivial quantities in radio frequency systems are presented along with results and possible improvements for future systems. The results show that the ADCs of the evaluated system have a SNR at a 240 MHz bandwith of -64 dBFS and a channel isolation between the ADCs of 61 dB. The DACs of the evaluated system have a SNR at a 1 Hz bandwith of -163 dBFS and a channel isolation between the DACs of 60 dB. These results conclude that data converters are a matured technology suitable for use as a key component in a modern radar systems. Some problems with the system are pointed out and discussed, and ideas for improvements are proposed.

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We want to thank our supervisor at SAAB Surveillance, David Lindh at the Research and Development (R&D) department for support in the degree project and giving an insight of what it is like to work in an industry that is highly dependent on electrical engineering. We are also immensely grateful to Rune Olsson and Johan Bodin, both at R&D, for technical support and expertise in the fields of signal processing and measurement.

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List of acronyms

AC	Alternating current
ADC	Analog-to-digital converter
BP	Bandpass
DAC	Digital-to-analog converter
dB	Decibel
dBc	Decibel-to-carrier
dBFS	Decibel-to-full scale
DC	Direct current
DFT	Discrete Fourier transform
FFT	Fast Fourier transform
IC	Integrated circuit
IMD	Intermodulation distortion
IMD3	Third Order Intermodulation distortion
PCB	Printed circuit board
PSD	Power spectral density
R&D	Research and Development
RBW	Resolution bandwidth
RF	Radio frequency
SFDR	Spurious free dynamic range
SNR	Signal-to-noise-ratio
TRB	Transceiver backend

1 Introduction

Many years have passed since the invention of the first radar system. The technology started out as a tool for military and defense purposes, but has since grown and made its way into the commercial and private market. This will open up for more possibilities to use radar in fields that have constraints on weight and size. An example is the use of radar in autonomous cars to detect surrounding traffic.

The purpose of this degree project is to evaluate the performance of a digital transceiver system for radar. To perform the necessary measurements for the project, a digital transceiver backend system has been provided by SAAB. This will allow for implementation of the theory in a real environment. Quantities that are confidential for SAAB will be rounded to a mathematically suitable magnitude. This will not affect using the methods and conclusions that are derived in this degree project. The two questions that are answered in this report are as following:

What are the performance parameters of the transceiver?

Based on the measurements, which hardware improvements can be identified to improve the performance for future revisions of the system?

The end result of the report will contain the transceiver systems measured parameters and the methods used to acquire them. A feasibility study is performed to choose the parameters of interest for the system and gain the required knowledge.

The report starts with an introduction to the subject in Section 2. Theory that is of importance to understand the degree project, such as performance parameters and signal processing is presented in Sections 3, 4 and 5. Measurements and calculations on the system are given in Section 6 and are summarized and concluded in Section 7.

2 Radar Systems

Radar is a method of detecting distant objects by transmitting electromagnetic signals which are reflected and received as echoes. The word “radar” is an acronym for ***ra**dio **d**etection **a**nd **r**anging*. Another similar technology is sonar, which uses sound waves instead of microwaves. The wave propagation of sonar is relatively slow in comparison to radar, 1500 m/s in water for sound waves and approximately the speed of light for radio waves in vacuum.

2.1 History

James Clerk Maxwell had brought together all the necessary theory for electromagnetics, but it was not until 1886-1888 that Henrich Hertz made it possible to start exploring the opportunities of the technology. With physical experiments, he proved the existence of radio wave propagation. The first use of radio waves for detecting larger metallic objects is typically attributed to the German inventor Christian Hülsmeyer in 1904. Hülsmeyer demonstrated the possibility of detecting a ship in conditions that left the human eye inefficient. Eventually, radar technology was accepted for military purposes and used to detect hostile vehicles in air, at sea and on land. Today radar has made its way into a commercial market with systems that are used on boats and vehicles for private use. Read more about radar technology and history in [3][5].

2.2 Radar System Design

Radar systems exist in a broad variety of configurations and designs. The most common model consists of one antenna that is used both as a transmitter and a receiver. The system switches between the two modes depending on if it is supposed to send a signal or to receive an echo. A basic radar system operates as follows: A digital signal is converted to the analog domain using a digital-to-analog data converter. The signal is then transmitted from the antenna and reflected from the surrounding objects. The echoes are received at the antenna and converted to the digital domain using an analog-to-digital data converter. The data is analyzed and the process is repeated.

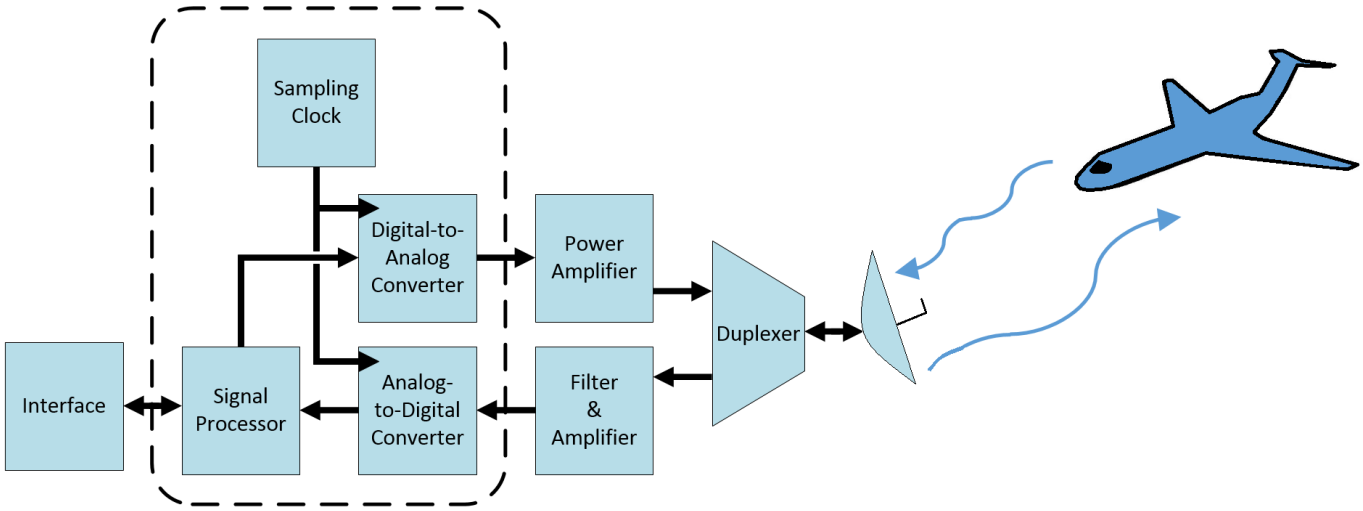

Figure 2.1: A block diagram of a radar system. The transceiver has been circled.

The main focus of developing and enhancing the performance of radar systems today is to push the digitalizing of the signal closer to the antenna and minimizing the need of analog components. This allows for smaller and lighter systems which open up for more ways to use radar applications.

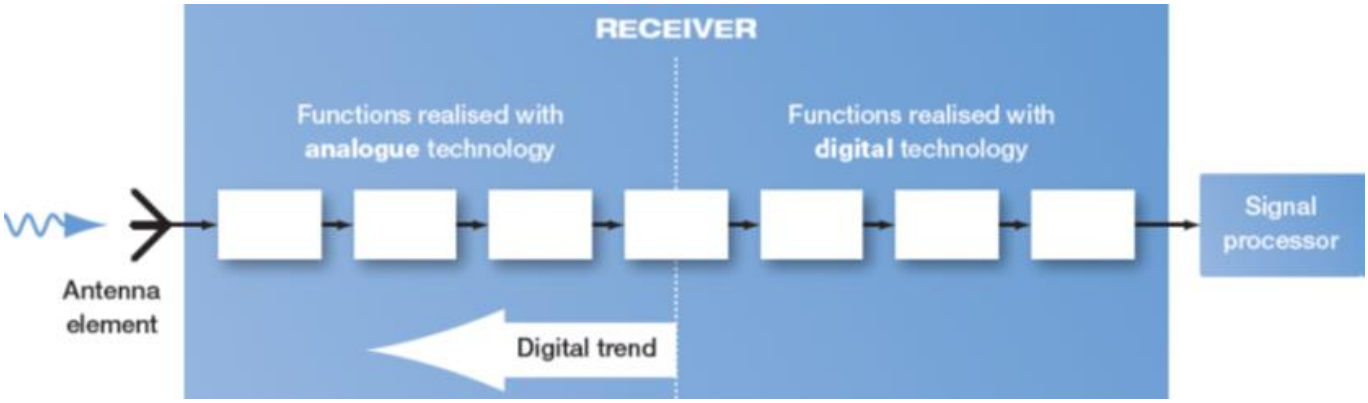

Figure 2.2: Example of how the digital trend is moved closer to the front end.

2.3 Multi-Channel Transceiver

The system evaluated in this report is a multi-channeled RF-sampling system. The system has multiple outputs and inputs. The transceiver has one sampling clock for each of the transmitters and the receivers. The transceiver backend (TRB) uses integrated circuits, each of which has two data converters. The approximated technical specifications are given in Table 2.1 and 2.2.

Table 2.1: Multi-channel transmitter

Sampling clock frequency	6 GHz
Carrier frequency	1300 MHz
Number of DAC units	8

Table 2.2: Multi-channel receiver

Sampling clock frequency	2 GHz
Sampling frequency	1 GHz
Center frequency of third Nyquist zone	1300 MHz
Center frequency of first Nyquist zone	300 MHz
Receiver bandwidth	240 MHz
Number of ADC units	8

2.4 Data Converters & Sampling Clock

Conventional radar systems typically consist of microwave electronics used to both transmit and receive pulses. These systems are usually heavy and large. As data converters have become cheaper and more reliable, backend systems can be replaced with digital ones. The purpose of the data converter unit is to convert quantities from the analog domain to the digital domain, and vice versa. Each converter is paired in two on the same integrated circuit (IC).

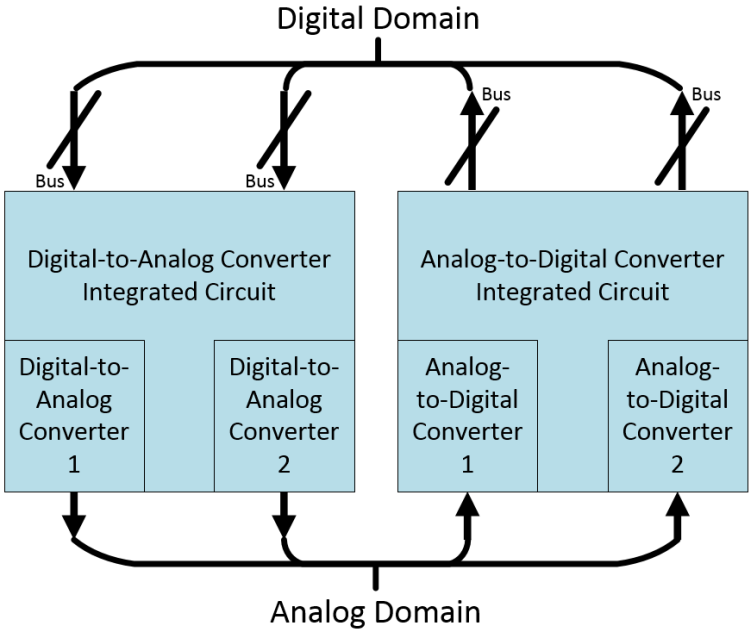

Figure 2.3: A block diagram of how each ADC and DAC comes in pairs of two on one IC.

2.4.1 Digital to Analog Converter (DAC)

A DAC converts a discrete number to a voltage level. Each discrete level corresponds to a voltage level. As a square wave consists of an infinite number of frequency components, a low pass filter at the output of a DAC will smooth the signal. An example is shown in Table 2.3.

Table 2.3: Example of a 3 bit DAC with a 7 volt reference level.

Binary	000	001	010	011	100	101	110	111
Voltage	0	1	2	3	4	5	6	7

2.4.2 Analog to Digital Converter

ADC converts an analog voltage to a discrete number. An ideal ADC has voltage intervals that are equally large for each discrete increment. An example is shown in Table 2.4.

Table 2.4: Example of a 3 bit ADC with an 8 volt reference level.

Voltage	0-1	1-2	2-3	3-4	4-5	5-6	6-7	7-8
Binary	000	001	010	011	100	101	110	111

2.4.3 Sampling Clock

To sample an analog signal or to reconstruct the original signal from samples, a sampling clock is used to time the interval between each sample. To avoid interference with other alternating currents and signals the sampling clock uses a high amplitude to have a clear reference to when a sample is supposed to be made. A sampling clock that varies in frequency and amplitude will affect the data conversion, which results in a less precise sampled signal.

3 Nonidealities

When working with complex electronic systems, it is important to consider possible problems, which may occur and affect system performance. These are here called *nonidealities*. In the following, some expected nonidealities are discussed and analyzed. More about nonidealities can be found in [7].

3.1 Noise

Noise is random variation in an electric signal. Its power depends on the quality of the signal and noise source. A noise free ideal analog system would have no resistive elements and would be fully shielded from external electromagnetical interferences. The most common noise is the internally generated noise. It is generated in the resistive elements of the circuit. Both resistors, cables and signal lines on PCBs contains resistive elements, which add noise to the system. A high operating temperature leads to more noise in a system. This effect is commonly decreased by adding cooling elements, such as fans and heat sinks. The differential error of a quantified signal generates a quantization noise. Non-linearities in the ADC are a source of quantization noise, as well as digital signal processing since the algorithms are quantized.

3.2 Spurious Components

Unwanted components in the spectrum of a sampled signal are often described as *spurious components* or *spurs*. Spurs can originate from other internal frequencies in the system such as switching from a power converter or a sampling clock. Spurs can also be harmonic products from frequencies outside of the system bandwidth or intermodulation distortion products (see Section 3.4) from adjacent frequency components.

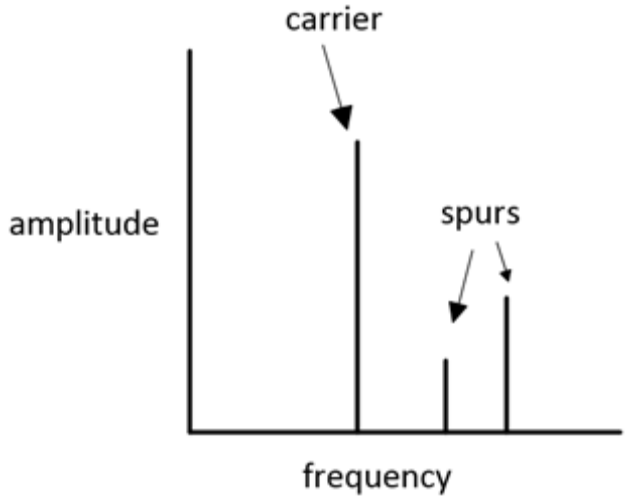

Figure 3.1: Example of spectrum with spurious components. [7]

3.3 Isolation

A common problem with integrated circuits is the occurrence of interference between the onboard components. These occurrences are often related to capacitive and inductive interferences between signal transmission lines or the onboard power electronics.

The transceiver-backend (TRB) consists of a number of ADCs and DACs which are mounted close to each other on the PCB. This may result in interference between adjacent data converters. This is because they share the same ground shielding and power source. The channel isolation between ADC and DAC will not be studied in this report, since the ADC and DAC will never operate simultaneously. The sampling clocks are continuously active and can interfere with the system. The interference caused by the sampling clocks may result in spurs in the received or transmitted signal.

3.4 Intermodulation Distortion (IMD)

Intermodulation Distortion is an amplitude modulation of a signal consisting of two or more different frequencies. The intermodulation between each component creates additional components at different frequencies depending on the frequencies of the two original components. Intermodulation is caused by non-linearities in the system.

Table 3.1: The first three orders of intermodulation products are presented in the table. The products are dependent on the two frequency components of 100 MHz and 101 MHz in this example. The table also shows that the third order modulation product is the most troublesome one, because it is close to the two fundamental signals.

First order	f_a	f_b	100 MHz	101 MHz
Second order	$f_a + f_b$	$f_a - f_b$	201 MHz	1 MHz
Third order	$2f_a - f_b$ $2f_a + f_b$	$2f_b - f_a$ $2f_b + f_a$	99 MHz 301 MHz	102 MHz 302 MHz

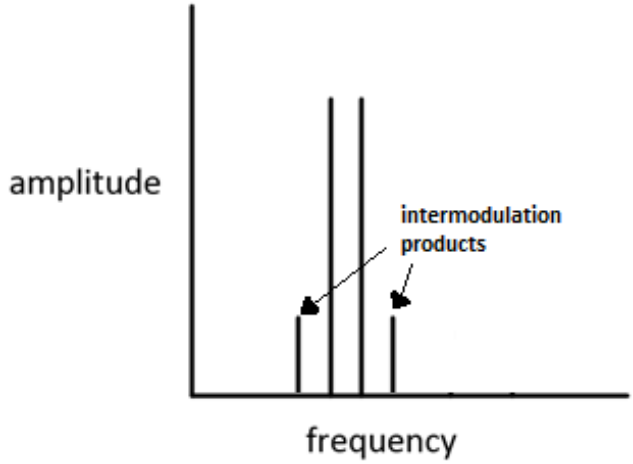

Figure 3.2: Example of the appearance of third-order intermodulation products around two adjacent frequency components. [7]

4 Performance Parameters

Based on the theory presented in Section 3 the following performance parameters to measure have been selected:

Signal-to-Noise Ratio
Spurious-Free Dynamic Range
Third-order Intermodulation Distortion

These parameters quantify noise, spurious components and intermodulation distortion and are important benchmarks for radar systems. The parameters are presented in Section 4 and can be further read about in [7].

4.1 Power Ratios

Power ratios often vary over several orders of magnitude and are therefore often expressed in logarithmic units, most often decibels. Equation (1) and (2) can be used to convert linear power ratio to a logarithmic scale.

$$(1)\ Decibel\ =\ 10 \cdot log_{10}(P_2[W]/P_1[W])\ \text{[dB]}$$

$$(2)\ Decibel\text{-}milliwatts\ = 10 \cdot log_{10}\left(\frac{P_{mW}}{1mW}\right)\ \text{[dBm]}$$

Full-scale refers to the maximum input or output signal power level of a system. The systems maximum input/output is refered to 0 decibel to full-scale (dBFS). If a systems maximum signal input is 13 dBm, a signal input at 12 dBm would be refered to as -1 dBFS, as it is one decibel lower than the maximum input.

An input (or output) signal that exceeds the systems maximum power level will lose data and become distorted. Data loss and distortion is avoided by selecting a carrier power level below 0 dBFS.

4.2 Signal-to-Noise Ratio (SNR)

SNR is the ratio between the signals power density and the power density of the noise within a chosen bandwidth. Greater SNR implies that a signal is easier to distinguish from the noise. When measuring the SNR of the ADC, it is important to distinguish the noise generated in the signal source. Similarly, when measuring the SNR of the DAC, it is important to distinguish the noise from the measurement equipment and the converter. This makes sure that the measured SNR characterizes the data converters and not the measurement equipment.

4.3 Spurious Free Dynamic Range (SFDR)

SFDR is the systems dynamic range to the greatest spurious component. It is either expressed in relation to the full-scale (dBFS) or to the power of the carrier (dBc). A high SFDR is desired in radar applications to distinguish the carrier reflections on targeted objects from spurious components. When the received signal is analyzed and the system contains interference such as spurs, they might be interpreted as real echoes.

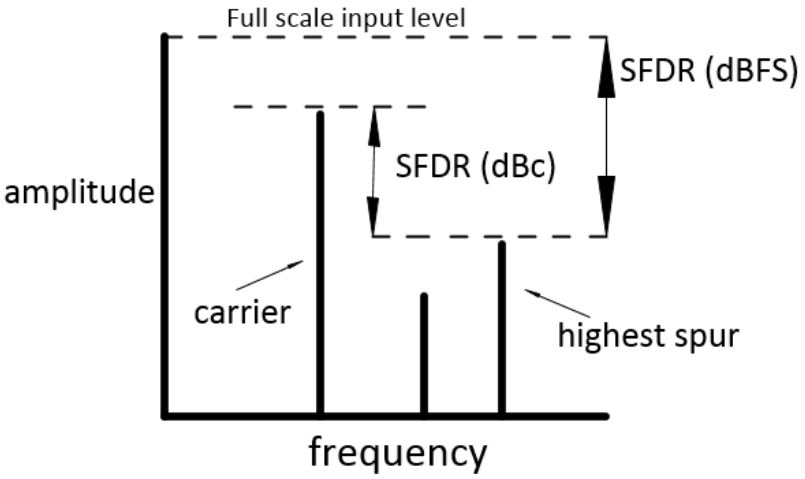

Figure 4.1: Example of spectrum that explains SFDR. [7]

4.4 Third-order Intermodulation Distortion (IMD3)

Third-order intermodulation distortion is the measurement of the third order intermodulation products produced in a non-linear system when two signals close to each other in frequency are received on the same input. The offset in frequency between modulation product and carrier is related to the offset frequency between the two received frequency components. The two third order products closest to the carriers will be located at $2 \cdot f_1 - f_2$ and $2 \cdot f_2 - f_1$.

5 Signal Processing

This section introduces signal processing concepts that are important for understanding the receiver end of a modern radar system. The focus will be on how intermediate frequencies are converted to baseband and how the collected information can be analysed using discrete fourier transform (DFT).

5.1 Undersampling

The sampling theorem is the condition for the minimum sampling rate that is needed to capture the data of a continuous time signal with a limited bandwidth.

$$(3)\ fs \geq 2 \cdot highest\ occurring\ frequency\ in\ a\ signal \text{ [1]}$$

The theorem is expressed this way to include signals that exceeds half the minimun required sample rate, also called the Nyquist rate. The frequency spectrum can be divided into an infinite number of zones with a bandwidth of the Nyquist rate. These zones are called Nyquist bands and are illustrated in figure 5.1.

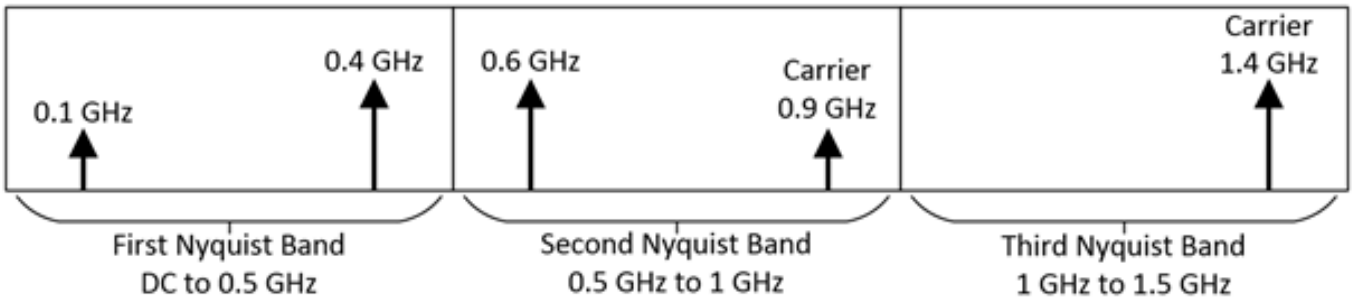

Figure 5.1: A diagram illustrating aliasing in the first, second Nyquist zone. There are two signals present but they get sampled as different frequencies depending on the bandwidth. [7]

Aliasing occurs when a sampled signal contains frequencies greater then the Nyquist rate. This has the effect of folding the frequency components down to the lower Nyquist bands as illustrated in figure 5.1, allowing for sampling of a signal at a sampling rate that is below the Nyquist rate.

Radar applications often uses frequencies higher than the Nyquist rate of ADCs. By utilizing aliasing, frequency components of a radar system is folded down to the first Nyquist band. This allows for sampling of signals that does not fulfill the Nyquist criterion. This technique is called undersampling. Undersampling is when the phenomenon of aliasing is used to convert the signal down to the first Nyquist band. This phenomenon does not continue infinitely in the non-ideal world, as analog inputs do not have infinite bandwidth. The signal would eventually attenuate below the noise floor. An example of undersampling can be seen in figure 5.2. [1]

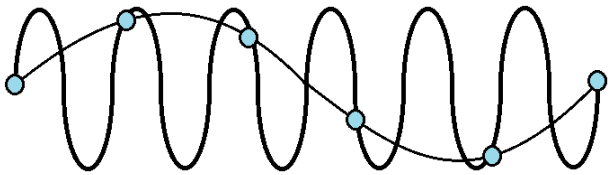

Figure 5.2: Example of undersampling. The thick sine wave is the original analog signal and the blue dots are the samples. The reconstructed signal is the thin sine wave that is of lower frequency than the actual signal.[7]

5.2 Baseband Conversion

Baseband conversion is used to reduce the total sampling rate needed by shifting the wanted frequency band towards DC. A lower sampling rate leads to less needed data and processor power for signal analysis. The negative frequencies will be shifted to the left and their band will be of higher frequency.

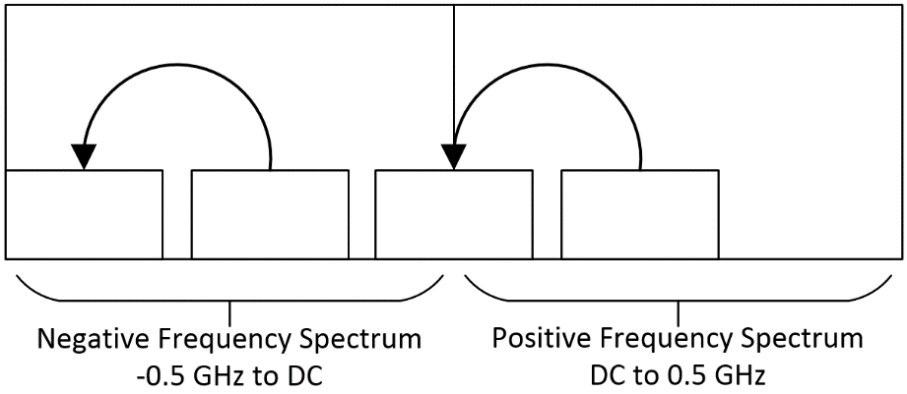

Figure 5.3: An illustration of how digital mixing is realized.

The sample rate is now greater then what is needed to store the signal. To reduce the sample rate and the bandwidth, data decimation is used. This is done by reducing the number of bits used to store each sample, the data rate, or a combination of both. Performing decimation of data results in the data gets aliased. This problem is solved by filtering out unwanted bandwidth by adding digital filters.

5.3 Discrete Fourier Transform (DFT)

By converting the signal from time domain to the frequency domain, each frequency component can be analyzed. The FFT algorithm is used to compute the discrete Fourier sum. A signal expressed as a phase vector can either move in a positive or negative direction in the quadrants. The signal needs to be sampled in both the real and imaginary domain for acquiring the phase direction of the signal. The imaginary component is acquired by shifting the main signal 90 degrees out of phase and sampling it simultaneously to the main signal. The real and imaginary parts are called I respectively Q.

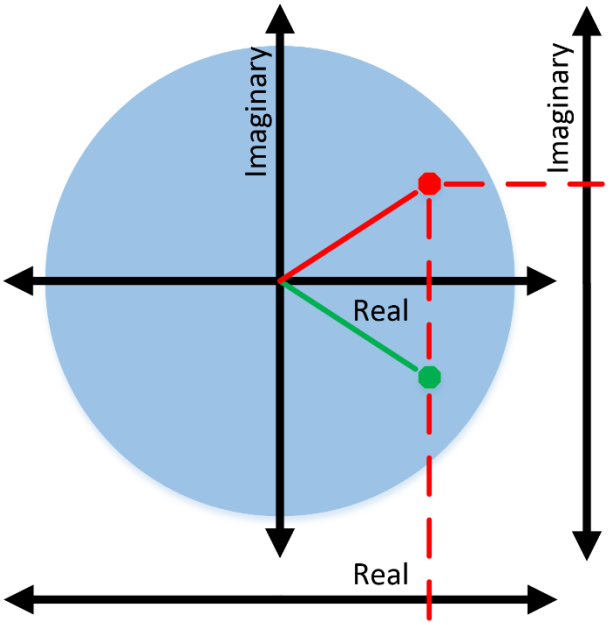

Figure 5.4: A phasor diagram of how signals are sampled. The vector in the first quadrant is sampled both in the real and imaginary domain. The phase of the signal can be detected by comparing two data samples. The vector in the fourth quadrant is sampled in the real domain. The phase of the signal cannot be detected by comparing data samples. This is due to the lack of sampled data of the movement in the imaginary domain. [4]

6 Measurement Methods and Data Collection

The performance parameters and methodologies that were presented in Section 4 will be measured and the results will be presented in this section. The data converters will be evaluated first, then the sampling clocks impact on the ADC will be investigated.

6.1 Measurement of Analog to Digital Converter

A signal generator is used as the transmitter, connected to the input of an analog-to-digital converter on the TRB, shown in Figure 6.1. The signal is sampled using a MATLAB-script that puts the sampled data in a vector. The Discrete Fourier transform is then computed using FFT and the spectrum is plotted. The MATLAB script used to acquire the ADC data can be read in Appendix A. The created script was influenced by [2]. If nothing else is mentioned, all ADC measurements are made with an input power of -1 dBFS which is explained in Appendix C, to test the system with an input as high as possible without saturating it.

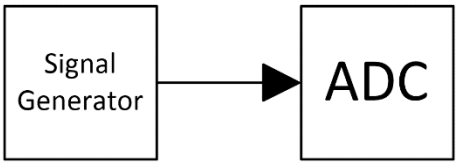

Figure 6.1: Block diagram of measurement setup.

The spectrum of figure 6.2 shows a 1300 MHz sine wave transmitted from the signal generator through an RF-cable which is then received by one of the ADCs on the TRB. The spectrum shows the carrier signal at 1300 MHz, along with multiple spurs on both sides. These spurs are unwanted, since they greatly decrease the quality of the signal.

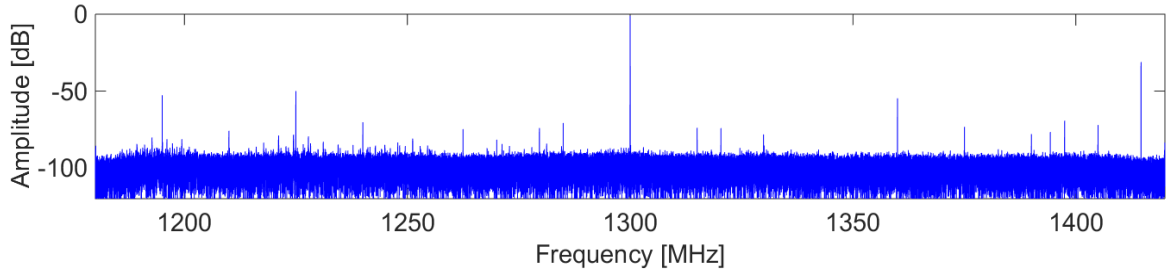

Figure 6.2: Unfiltered 1300 MHz signal received on the TRB.

To determine if the spurs are internally or externally generated, a BP-filter tunable between 1000 – 2000 MHz (Appendix B) is connected between the signal generator and ADC input. The BP-filter will suppress spurious components from the signal generator, and the components from the ADC will remain unaltered. The setup is shown in figure 6.3.

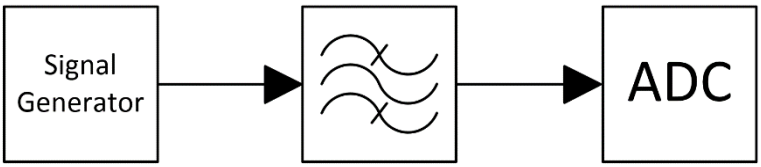

Figure 6.3: Block diagram of filtered measurement setup.

Figure 6.4 shows the spectra of the filtered 1300 MHz signal. As expected the majority of the spurs are now suppressed. These spurs will be ignored in the evaluation as they originate from the signal generator and not from the TRB.

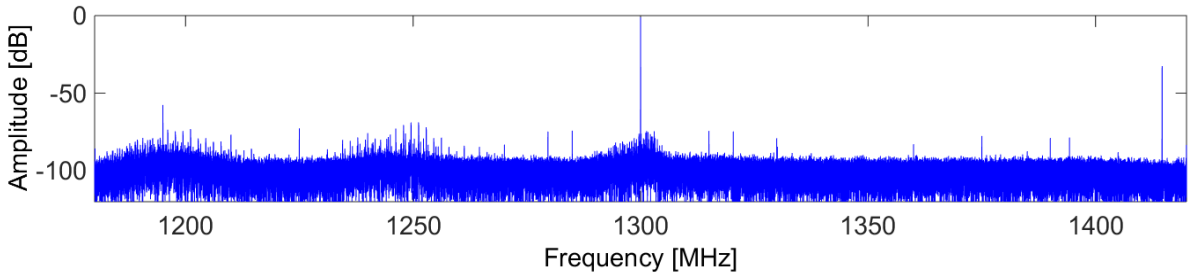

Figure 6.4: Filtered 1300 MHz signal received on the TRB.

Even though most larger spurs were suppressed by applying the BP-filter, there are still some components that have not changed in amplitude. There are spurs on each side of the carrier component which are believed to originate from the conversion from analog to digital of the carrier signal due to the ADC not being linear. Two large spurs are visible on the far left and right side of the spectrum. These spurs are believed to be interference from the TRB, as they do not change in amplitude with a filter applied, nor do they change frequency when the carrier frequency is changed. The spurs are also visible when the ADC input is terminated (shown in figure 6.7). Two other plots at 1250 and 1350 MHz can be found in Appendix C.

6.1.1 ADC SNR

SNR of the ADC is acquired by sending a signal from the signal generator. The noise floor from the signal generator is assumed greater than the noise floor of the ADC. A steep bandpass filter is used to remove the noise around the carrier created by the signal generator as shown in figure 6.5. By tuning the filters pass band to 1200 MHz and transmitting a signal at the same frequency, the most noise suppression from the signal generator is acquired in the opposite side of the systems frequency band.

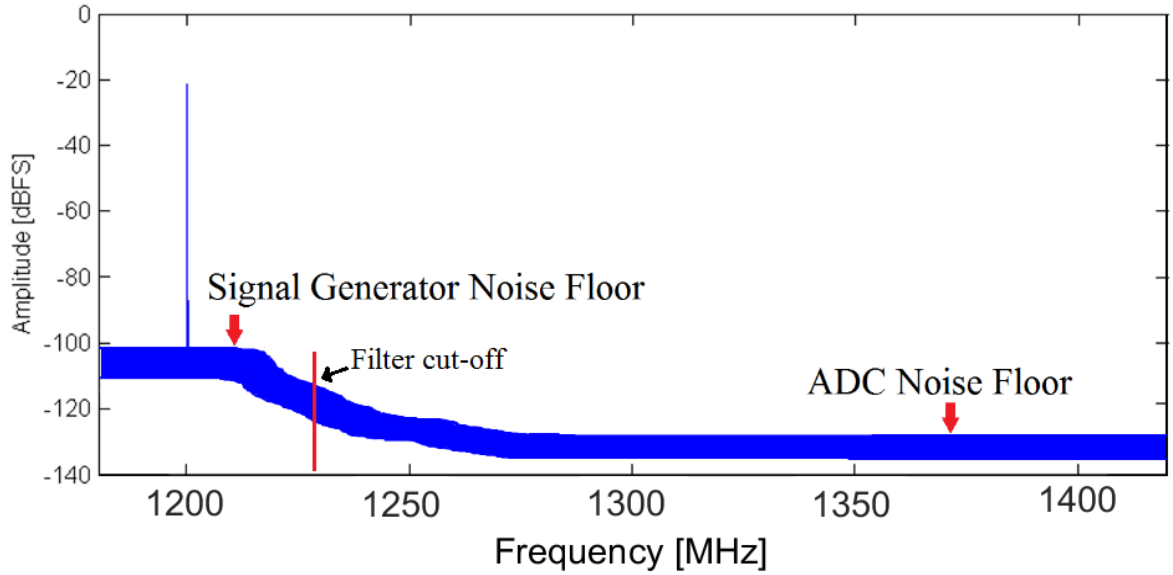

Figure 6.5: Illustration of the expected data acquired from the ADC. The filter is tuned to 1200 MHz, a carrier is generated at 1200 MHz and the ADCs noise floor can be seen in the right area of the systems frequency band.

As seen in figure 6.6, the noise floor is not attenuated by the narrow bandpass filter. The noise can be fully suppressed by using a 50Ω termination plug at the input of the ADC, which is shown in figure 6.7.

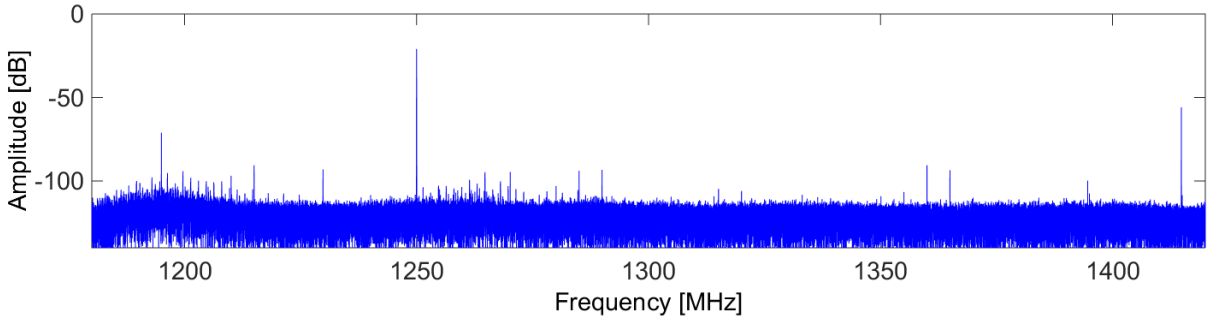

Figure 6.6: The filter is tuned to pass a 1250 MHz signal. Since the noise floor is not attenuated, the noise floor shown must originate from the ADC.

To calculate the SNR, all of the noise components in the bandwidth must be added to calculate the total noise power of the signal. The scenario used in the SNR calculation is presented in figure 6.7. The noise floor is estimated to be at -105 dBFS. The SNR is then calculated using Equation (4).

$$(4)\ ADC\ SNR = FFT\ Noise\ floor - 10 \cdot log_{10}(Samples)\ \text{dBFS}$$

$$ADC\ SNR = 105 - 10 \cdot log_{10}(131072)\ \text{dBFS}$$

$$ADC\ SNR = 105 - 51\ \text{dBFS}$$

$$ADC\ SNR = 54\ \text{dBFS}$$

The average noise floor level is multiplied with the number of samples to calculate the sum of all the noise in the spectra. An extra 1 dB is added since the signal is 1 dB below the input full scale, and the SNR is expressed in relation to the full scale.

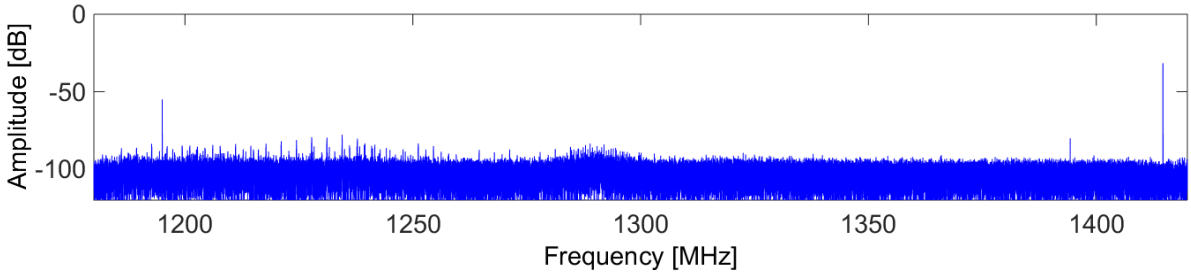

Figure 6.7: Input terminated with a 50Ω terminator.

6.1.2 ADC SFDR

When measuring the SFDR of the ADC the filtered sample in figure 6.4 is used. The SFDR is limited to 35.6 dBFS by the spur at 1415 MHz. If the two static interfering components at 1195 MHz and 1415 MHz were removed, the SFDR would be limited to 74.3 dBFS by the spurs close to the carrier signal.

6.1.3 ADC Aliasing

A spur at 1195 MHz is constantly visible at the input of the ADC. The spur is also visible when the input is terminated by a 50Ω resistance as seen in figure 6.8. The spur does not depend on the frequency components that are present on the input. This is further investigated by applying a signal with a frequency near the 1195 MHz spurious component. The input signal becomes aliased around the spur at 1195 MHz.

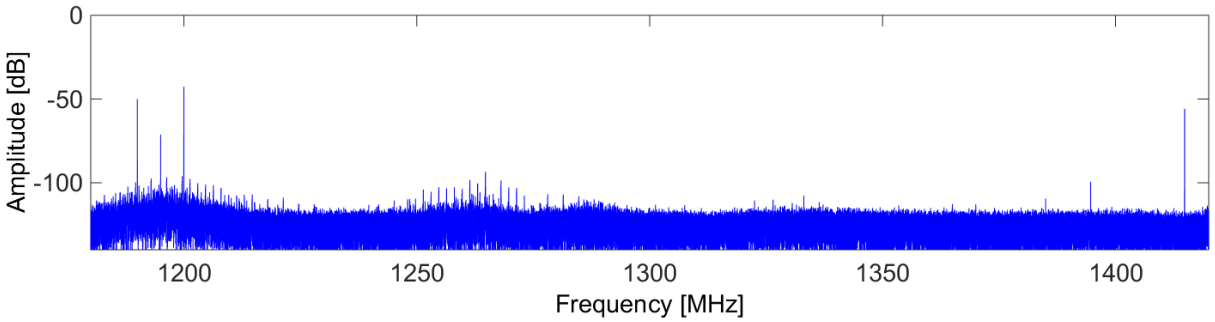

Figure 6.8: Carrier at 1190 MHz.

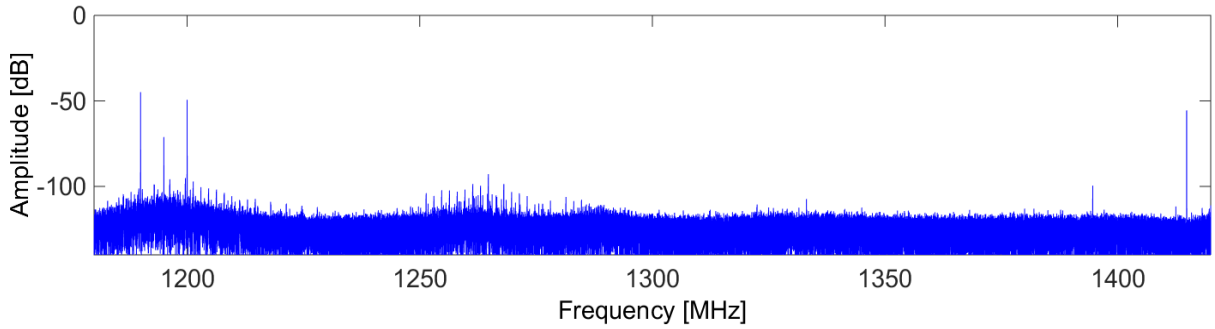

Figure 6.9: Carrier at 1200 MHz.

If a carrier is applied just outside of the systems bandwidth, the same carrier will be aliased into the sampled frequency band. The same thing applies for when a carrier is sent to the further right of the spurious component. An aliased component appears at the further right of the frequency band. A carrier that is applied at 1410 MHz will be aliased and a spur at 1220 will appear in the sampled frequency band as seen in figure 6.10.

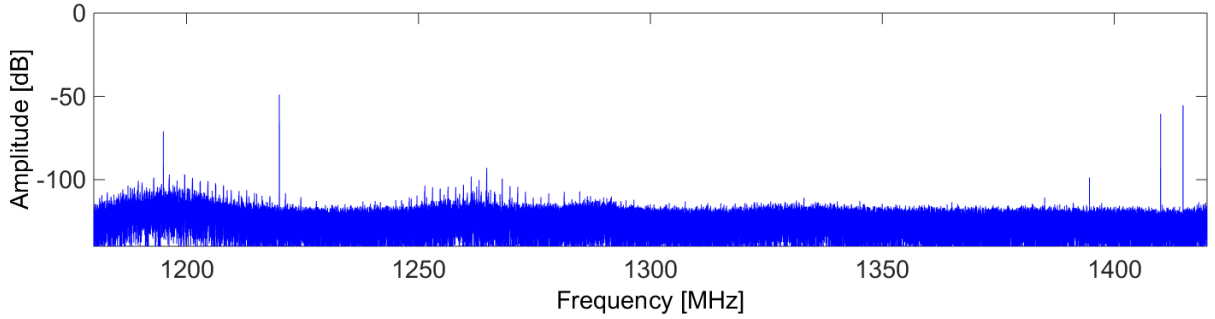

Figure 6.10: Carrier at 1220 MHz.

This is the result of baseband conversion in conjunction with data decimation. The baseband conversion creates new frequency components. If these components are not filtered out, they will be included in the final data when the data decimation is performed. This may create fake echoes that can be interpreted as an object that is seen by the radar application.

6.1.4 ADC Channel Isolation

The channel isolation was tested on two different inputs, X3 and X4, which are connected to the same ADC. A 1295 MHz, -1 dBFS signal was transmitted to the X4 input. X3 was terminated with a 50Ω load, and then measured to see if the signal on input X0 is visible. Figure 6.11 shows the spectra of a terminated ADC input with a signal leakage at 1295 MHz from the adjacent channel. The signal was attenuated with 61 dB.

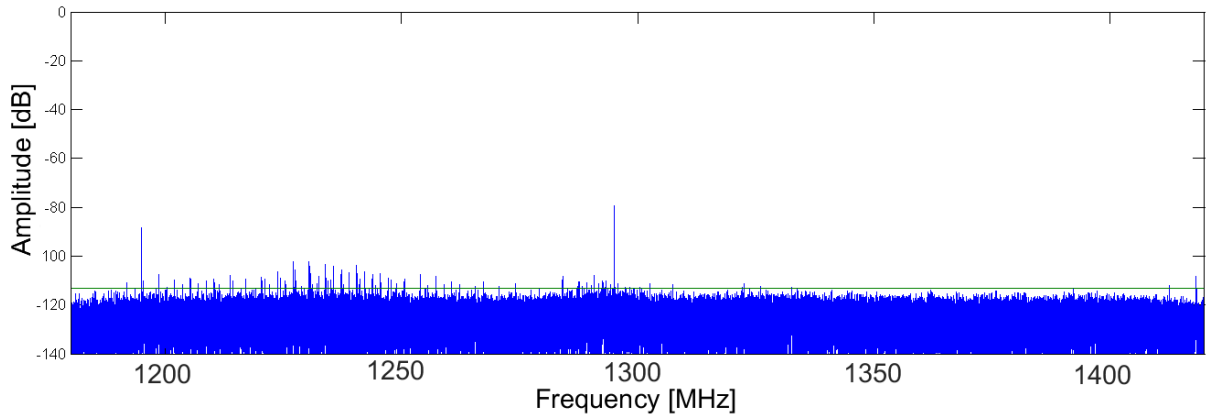

Figure 6.11: Spectra of terminated input X5, with a 1295 MHz signal transmitted to input X4.

6.1.5 ADC Third-order intermodulation distortion

Figure 6.12 shows the measurement setup for the following IMD3 measurements. Figure 6.13 shows the spectra of two signals at 1300 and 1301 MHz, -7 dBFS received on the same channel on the ADC. The result of having two signals so close to each other in frequency are third order intermodulation products close to the two carrier signals. The product on the right of the carriers is located at $1301 \cdot 2 - 1300 = 1302$ MHz, and the left one at $1300 \cdot 2 - 1301 = 1299$ MHz. The highest resulting intermodulation product is at 76 dBFS.

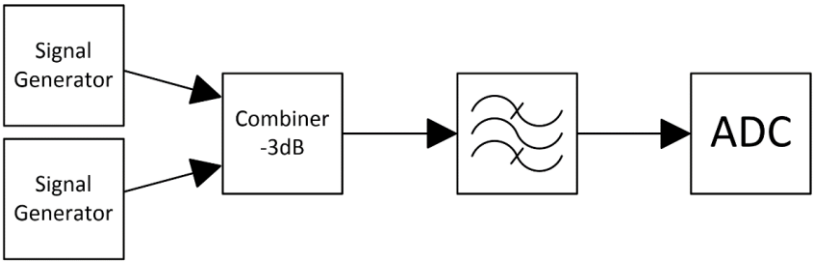

Figure 6.12: Block diagram of two-tone measurement setup.

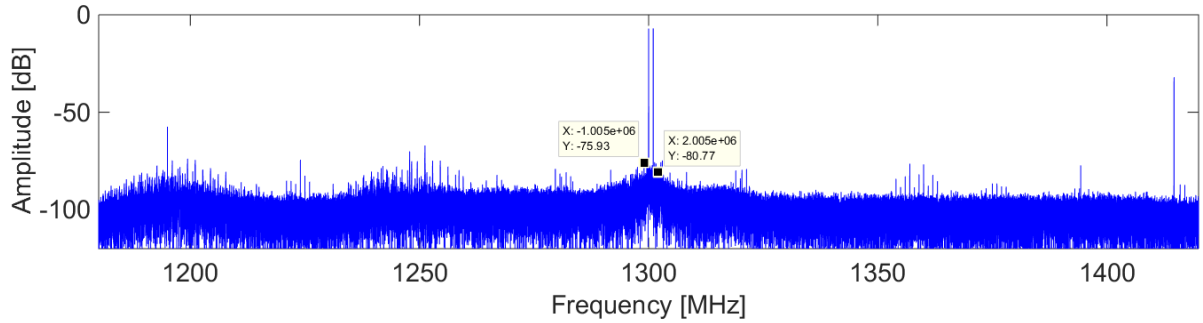

Figure 6.13: Two signals at 1300 and 1301 MHz are combined and transmitted to the same input on the ADC.

6.2 Measurement of Digital to Analog Converter

To evaluate the performance of the digital-to-analog converters a digital signal is generated using a MATLAB-script. The signal is then converted into the analog domain and transmitted through a RF-cable to a spectrum analyzer, shown in figure 6.14.

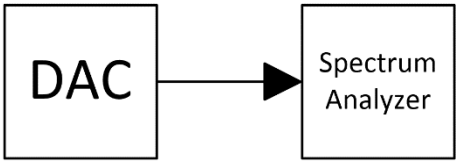

Figure 6.14: The signal of the DAC is directly sent to the spectrum analyzer.

6.2.1 DAC SNR

SNR from the DAC is measured using a spectrum analyzer. The dynamic range of the spectrum analyzer is assumed too limited to measure the SNR of the DAC. This is because of the DACs great performance in SNR. A steep bandpass filter (Appendix B) in conjunction with RF-amplifiers for the signal is used to pass and amplify the DACs noise floor and suppress the carrier, shown in figure 6.15. This increases the dynamics of the spectrum analyzer and the SNR can be calculated from the spectrum analyzer measurement.

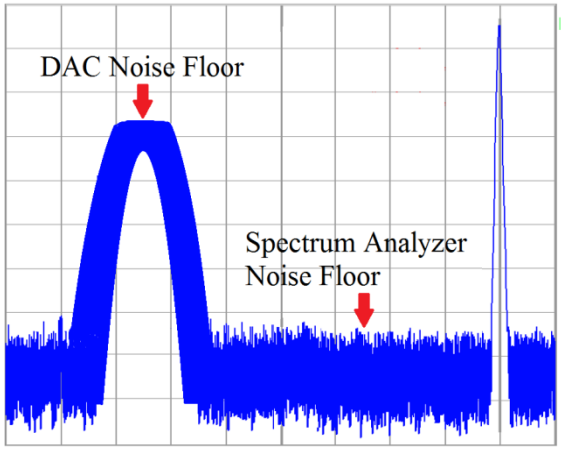

Figure 6.15: Illustration of the expected data acquired from the spectrum analyzer. The filter is tuned to 1200 MHz, a 1400 MHz carrier is generated and the DACs noise can be seen in the left area of the frequency band.

Figure 6.16 shows the spectra of the amplified noise floor from the DAC. The DAC noise floor is shown to the left in the spectra, where the red marker measures an amplitude level of -64.87 dBm. Equation (5) is used to calculate the SNR over a 1 Hz bandwidth.

$$(5)\quad DAC\ SNR = -Noise\ floor - RBW - gain - carrier\ [\text{dBFS}]$$
$$= -64{,}87 - 10 \cdot log_{10}(1MHz) - 43 + 4\ [\text{dBFS}]$$
$$= -163\ [\text{dBFS}]$$

The amplified noise floor is divided by the bandwidth to calculate the SNR over 1 Hz. The 43 dB gain is then subtracted to get the actual noise floor level. 4 dB is added to have the noise floor expressed relative to carrier, which is -4 dBm. Since the DAC does not have a defined bandwidth, the SNR is presented in power ratio per Hz.

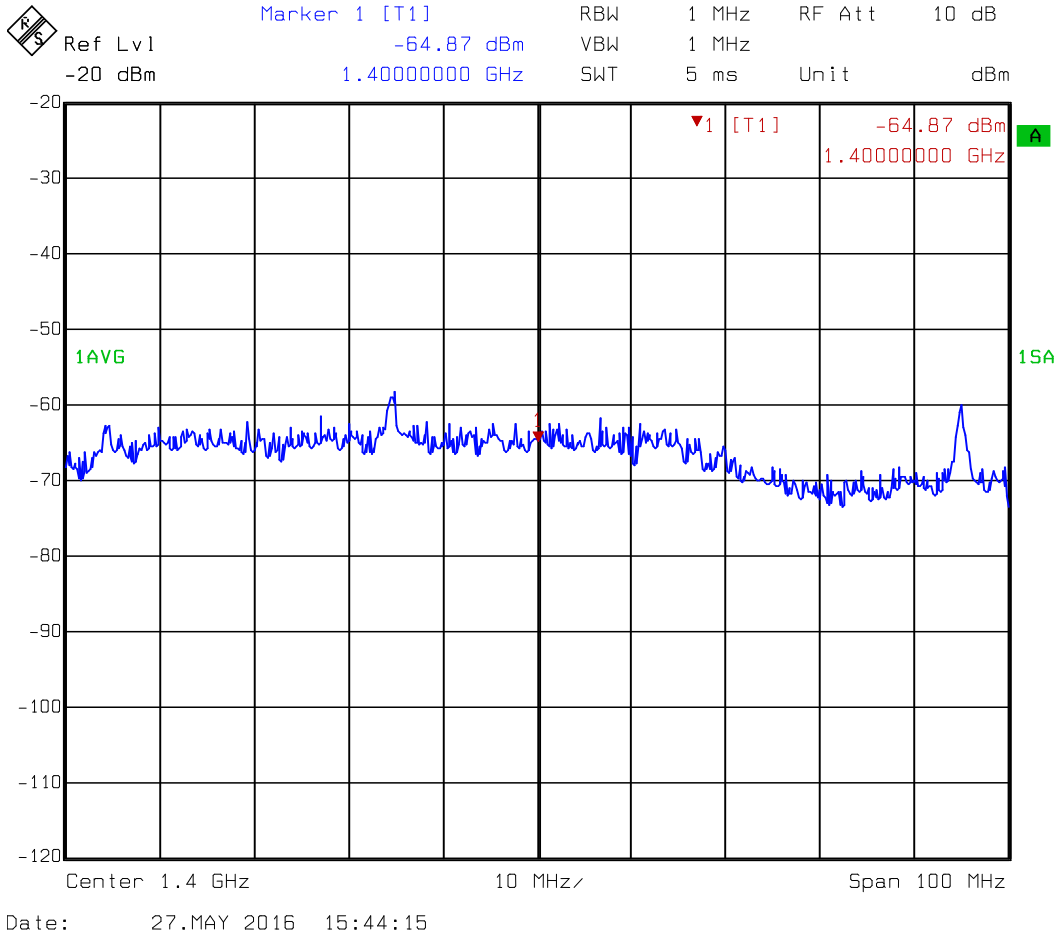

Figure 6.16: The DAC noise floor has been raised with an amplifier in conjunction of a steep bandpass filter. The noise floor is amplified with 43 dB.

6.2.2 DAC SFDR

The first test was made by generating a 1300 MHz signal from one of the DACs and then analyzing it on a spectrum analyzer. The result is a clear spectrum with the 1300 MHz carrier in the middle of the picture, along with two small spurs on both sides. The spurs are always located at ±125 MHz from the carrier, unaffected by the carrier frequency. The SFDR is limited to 68-77 dBFS by the ±125 MHz spurs, depending on which of 8 DACs are tested. Figure D.3 and D.4 in Appendix D shows two other tested outputs. The spurs are confirmed to originate from the harmonics of the sampling clock at 6 GHz, and the problem is known by the manufacturer of the DAC. An even number is acquired by dividing the sampling clock frequency with the offset frequency: 6 GHz/125 MHz = 48. This implies that the spurs are created by modulation between the clock and the carrier.

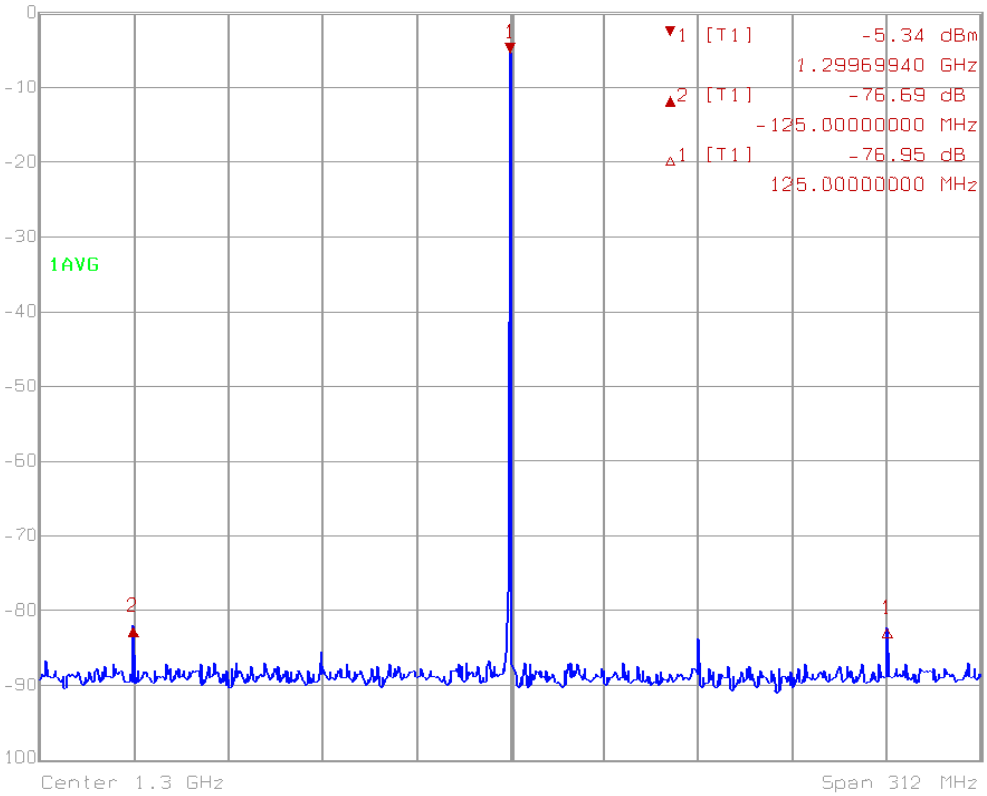

Figure 6.17: 1300 MHz signal on output X0, with visible 125 MHz spurs

6.2.3 DAC Channel Isolation

The system is built with 8 DACs distributed on 8 different channels on 4 different integrated circuits. These channels are then connect to 8 different outputs, X0-X7. The test is done by transmitting a signal from one of the outputs and see if the signal is visible on any of the other outputs.

The first test is to see if there is any signal leakage between the DACs on the same IC. The X0 output is connected to a spectrum analyzer and a 1300 MHz signal is transmitted. Simultaneously a 1290 MHz signal is transmitted from the X1 output. This can be seen in figure 6.18. On the right of the 1300 MHz carrier we can see small spur at 1290 MHz. This shows that there is signal leakage coming from the other channel transmitting a signal. The interfering signal is attenuated with 60.3 dB.

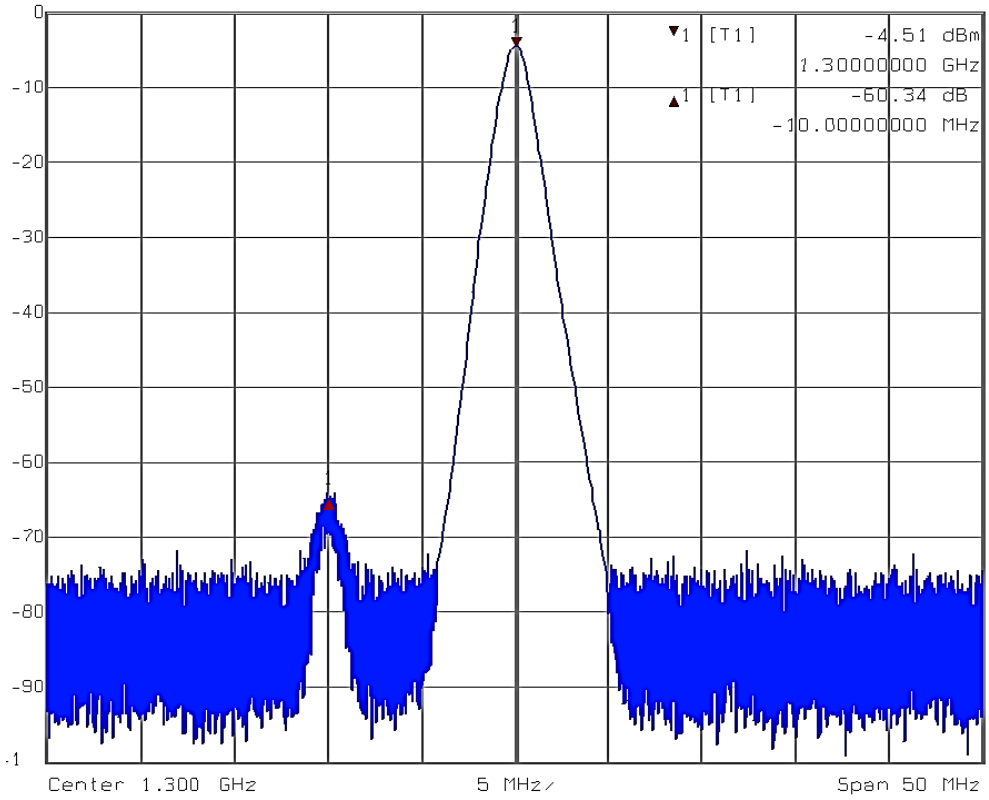

Figure 6.18: Signal leakage between two channels on the same IC.

The second test is to see if there is any signal leakage between the DACs on different integrated circuits. The test setup is the same; except the outputs are X0 and X2, which is on a different IC. There are no signal leakage between different ICs as seen in figure D.2 in appendix D.

6.3 Measurements of Sampling Clock

In this section the sampling clocks were measured to investigate their impact on the data conversion.

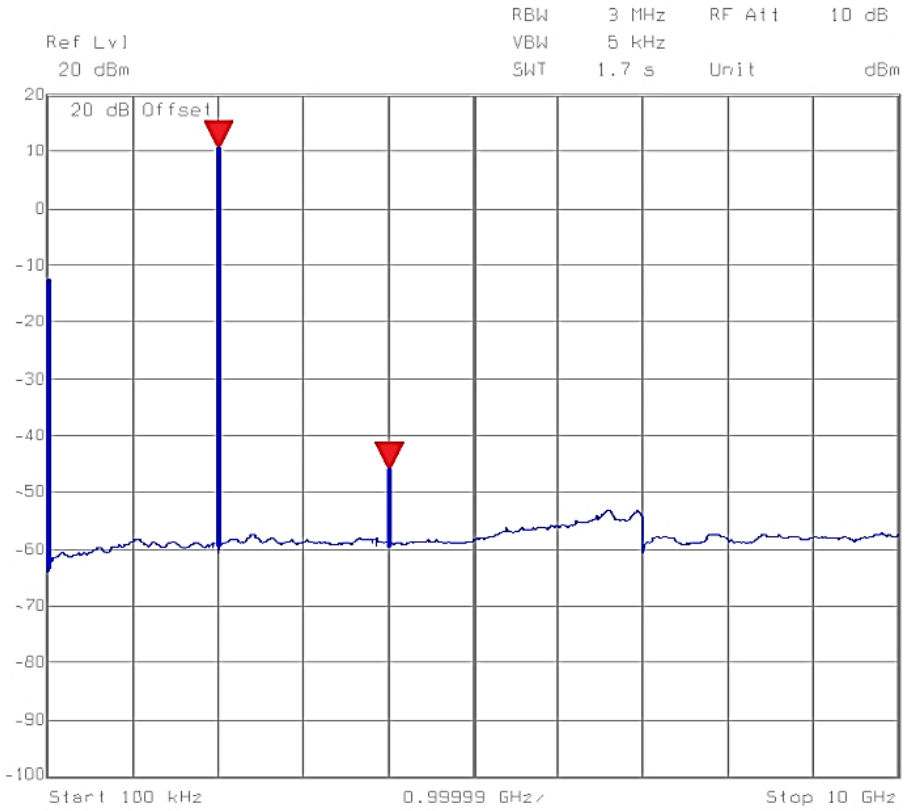

Figure 6.19: 10 GHz bandwidth overview of ADC Clock.

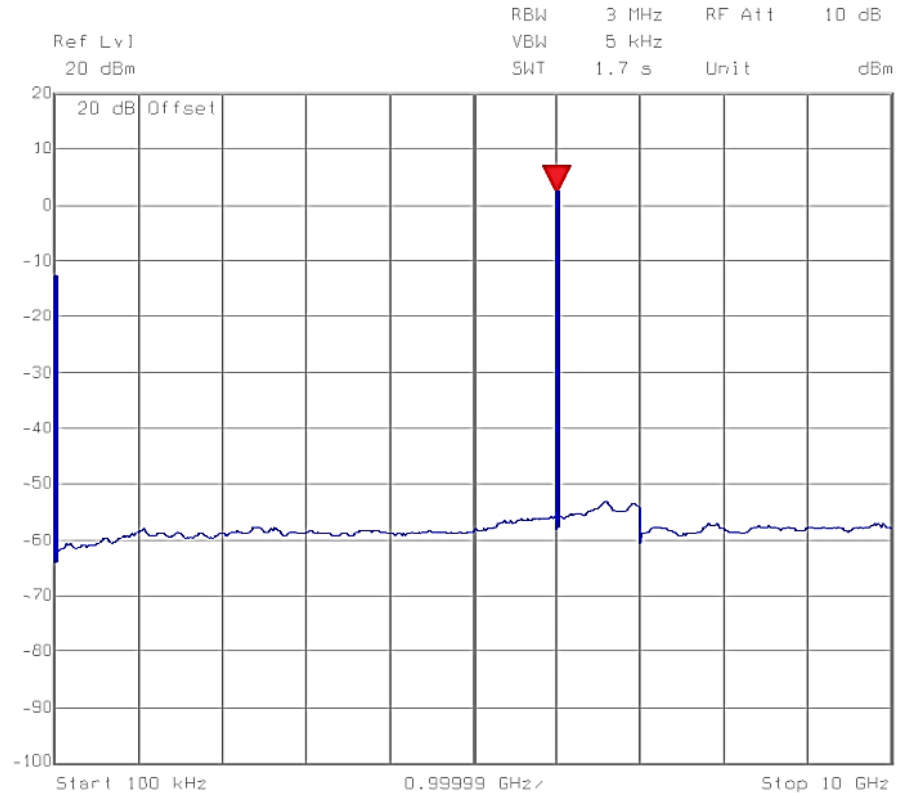

Figure 6.20: 10 GHz bandwidth overview of the DAC Clock.

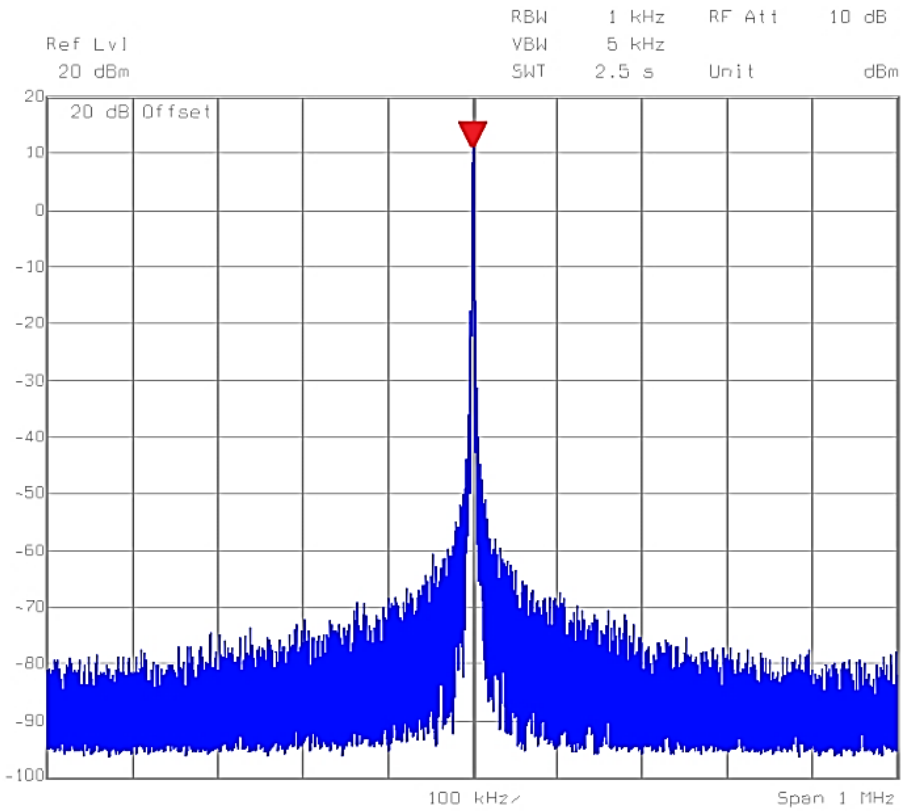

Figure 6.21: An enlarged image around the 2 GHz sampling clock..

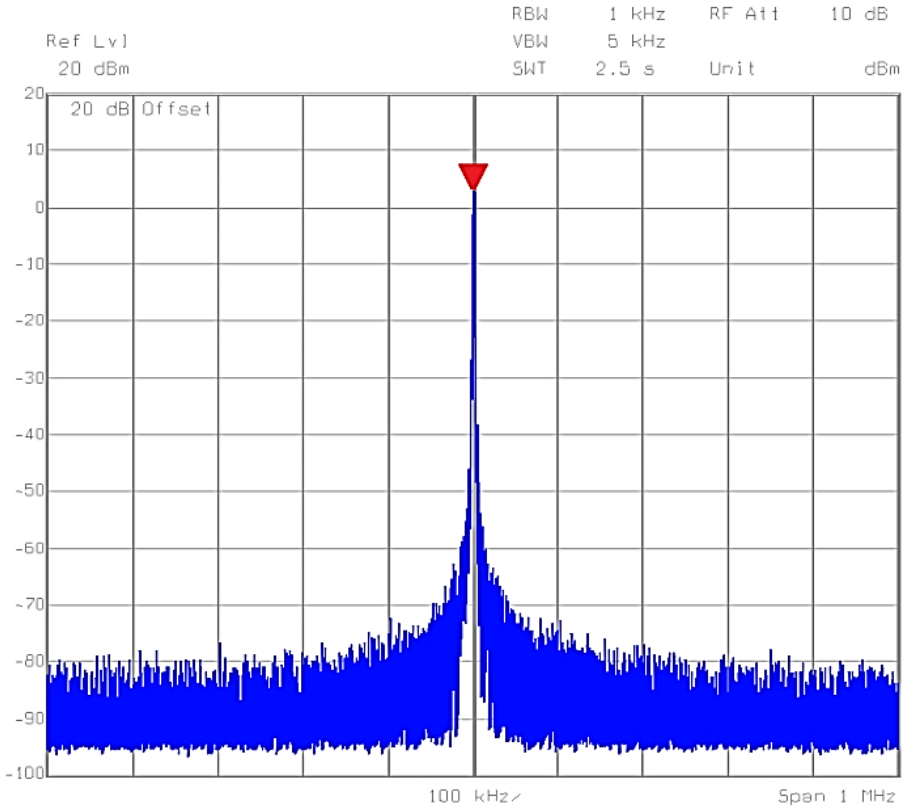

Figure 6.22: An enlarged image around the 6 GHz sampling clock.

Figure 6.19 and 6.20 show a wide frequency band spectra of the two sampling clocks. This measurement was made to see if there were any unwanted frequency components that could interfere with the data converters. As the figures show, both sampling clocks are free from any spurious components, except harmonics which are significantly lower than the sampling clock. Figure 6.21 and 6.22 shows a narrow frequency band spectra of the sampling clocks. The spectras show that the sampling clocks are well defined at its specified frequency, meaning that the signals are accurately sampled.

A power meter was used to measure the power of the sample clock signals. The power level of the sample clocks was greater than the specified maximum input of the power meter. A power attenuator was used to reduce the power of the signal, reducing 29.8 dB at 2 GHz and 29.6 dB at 6 GHz. The measured power level has been recalculated to non-attenuated power level. This is seen in table 6.1.

Table 6.1: The power delivered to the system by the sampling clocks.

Clock	Total Power
ADC sample clock	13.52 [W]
DAC sample clock	21.76 [W]

The clock signals are split with an internal network as there are multiple converters on the PCB. This makes the power delivered to each IC lower than the total power delivered to the system. The amplitude of the sampling clock was changed to see if there were any changes in the signal acquired by the ADC. The changes to the sampling clock can be seen in table 6.2. The measured data from the ADC are shown in Appendix E, figure E.1 and E.2. The measurements show no changes in the noise floor or the signal received by the ADC.

Table 6.2: The power delivered to the system by the sampling clocks after varying the power level.

Clock	Total Power +3dB	Total Power -6dB
ADC sample clock	27.04 [W]	5.44 [W]

6.4 Error Sources of Measurement Methods

6.4.1 Unshielded equipment

All of the tests were done without any shielding on the TRB, which makes the system vulnerable for interference from external sources. Unshielded electronics may act as antennas and pick up radio frequencies.

6.4.2 Non-linearity in the filter

In figure 6.4 there are two notable clutters of spurious components and an increase in the noise floor around 1195 MHz and around the carrier. These are believed to come the BP-filter, as the spurs and noise floor changes at 1195 MHz are not seen in the unfiltered signal in figure 6.2.

6.4.3 Unmatched Impedances

The spur clutter at 1250 MHz is believed to come from the ADC. Spurs are visible in the 1230 to 1250 MHz frequency band when the input of the ADC is free from any cables or filters. These spurs are enlarged when the cables are connected, which is caused by reflections between signal source, cables and load.

7 Summary and Conclusion

Table 7.1: ADC Performance parameter results

ADC Performance Parameter	Magnitude
SNR at a 240 MHz bandwidth	-64 dBFS
SFDR	-74 dBFS
Channel Isolation	61 dB
IMD3	-74 dBFS

Table 7.2: DAC Performance parameters results

DAC Performance Parameters	Magnitude
SNR at a 1 Hz bandwidth	-163 dBFS
SFDR	-67 dBFS
Channel Isolation	60 dB

The goal of this degree project was to evaluate the transceiver backend for a radar system given by SAAB and propose possible improvements of the transceiver backend. A feasibility study was performed and parameters of interest were chosen for evaluation of the system. Finding relevant information in the feasibility study was problematic as information about radar technologies available to the public domain is limited. This is because of the company confidentiality and military interests in the technique.

The SFDR result of the ADC in table 7.1 is limited by the spurious components at 1195 and 1415 MHz as seen in figure 6.4. As the spurs are coming internally from the TRB, finding the source of these and eliminate them will greatly increase the SFDR performance of the ADC. These static spurious components can be reduced in the digital signal processing.

The spurious components occurring by aliasing can be seen as faulty measured objects that does not exist. An autonomous vehicle that would operate with a similar system and acquire faulty data could make a decision that would have negative consequences. Accidents can be avoided by using fully functional radar systems on vehicles. If the system observes an incoming obstacle, it can give orders to the vehicle to act and try to avoid the obstacle. Choosing sampling clocks, sampling rates and mixing frequencies so that unwanted frequency bands are thrown and not aliased is vital for having an optimized system. By not using more bandwidth than needed for a certain application, we can reduce the amount of unwanted signals obtained by the system.

Optimizing radar systems is important for sensing and clarifying which objects are observed by the system. Digital radar systems are smaller and lighter than analog systems, a vehicle that carries the system will consume less fuel in comparison to a heavier system. The components of the system can be changed accordingly if the performance criteria of the system is met or not met. The cost of the system can be decreased by using cheaper components that still fulfill the performance criteria specified for the system. Better components should be used if the criteria is not met.

The quantitative data of the degree project concludes that data converters are a mature technology and suitable as key components in modern radar systems.

References

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[6] Roger J Sullivan., Radar Foundations for Imaging and Advanced Concepts, 2004

[7] Walt K., The Data Conversion Handbook, 2004

Appendix A: ADC Data Collection Script

```
% Data Sampling
dc{3}.trc.setBit(5);
samples_max = 2^n; % Samples acquired where n is the number of bits.
Fs = 240E6; % Samplerate per channel.
bw = 240E6; % I and Q combined bandwidth.
% Number of samples to use. Multiply with 0 to 1.
samples = floor(samples_max * 1);
[i q] = dc{3}.getFifoData(samples, 0); % Get data.
% Rightshift data 2 bits because of none used control bits.
i = i ./ 4; q = q ./ 4;

% Time Spectrum Plot
subplot(2,1,1);
n = 0:samples-1;
plot(n, i);
xlabel('Samples'); ylabel('Amplitude');

% Settings
dF = Fs/samples; % hertz/bin
f = -Fs/2:dF:Fs/2-dF; % hertz

% Window
w = hanning(samples); % Hanning window.
i = i .* w; q = q .* w; % Apply window.
% Calculate the amplitude loss of window.
window_offset = samples/sum(w);
% Compensation for amplitude loss of window.
iq = (i - 1j*q) * window_offset;

% FFT for i & q
fft_iq = fftshift(fft(iq/(samples*2^number_of_bits_for_adc)));
fft_iq_dB = 20*log10( abs(fft_iq) );

% Mean value calculation.
g = -0; % Changeable mean max [dB].
str = num2str(10*log10(mean(abs(fft_iq(fft_iq_dB<g)).^2)));
S0 = {'Noise = ',str,' dBFS'};
S1 = {'For all less than ',num2str(g),' dBFS'};
str0 = strjoin(S0);
str1 = strjoin(S1);

% Frequency Spectrum Plot
subplot(2,1,2);
plot(f, 20*log10(abs(fft_iq)+30-7.3), [f(1),f(end)], g*ones(1,2));
axis([-inf, inf, -140, 0])
xlabel('Frequency [hertz]');
ylabel('Amplitude [dBFS]');
text(-1.16E8,-12,str0);
text(-1.16E8,-18,str1);
```

Appendix B: Bandpass Filter

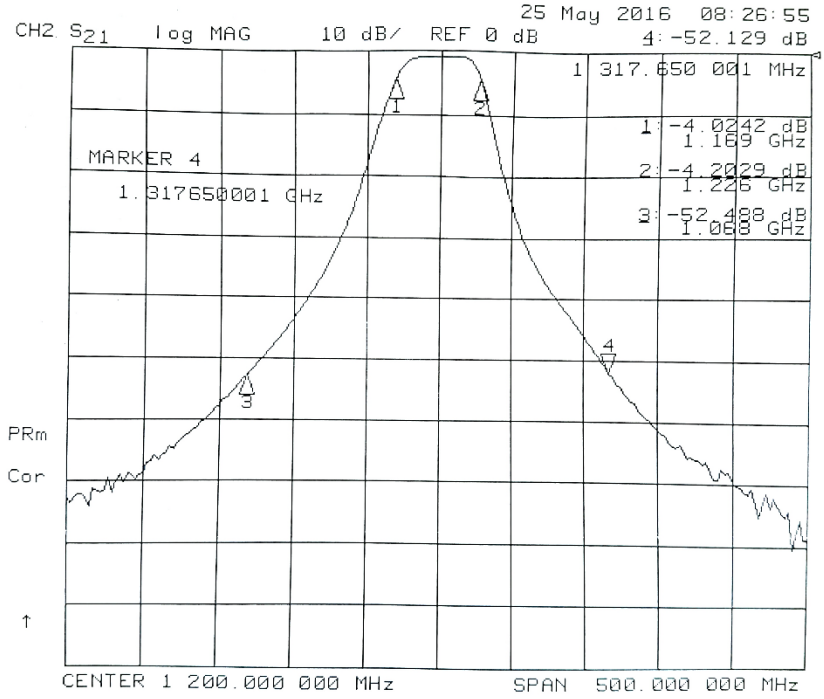

Figure B.1: The frequency characteristics of the used tunable BP-filter. It has a passband of 50 MHz, and attenuates by 53 dB when 160 MHz away from the passband. The passband attenuates 1 dB.

Appendix C: ADC Data

The fullscale of the ADC input is specified to 1.46 V_{pp}. On a 50Ω input impedance this equals to 7.3 dBm maximum input power. All signals transmitted to the receiver have been -1 dBFS (6.3 dBm), to test the ADC with an input power as high as possible, without saturating it. The two-tone measurement is made with two tones at -7 dBFS, so the combined signal does not exceed the maximum input when the amplitude peaks of the two tones are in phase.

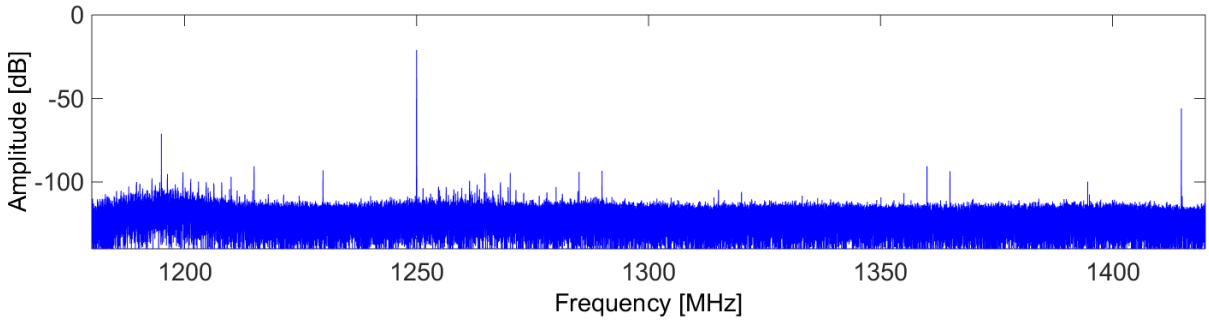

Figure C.1: Filtered 1250 MHz signal received on the TRB.

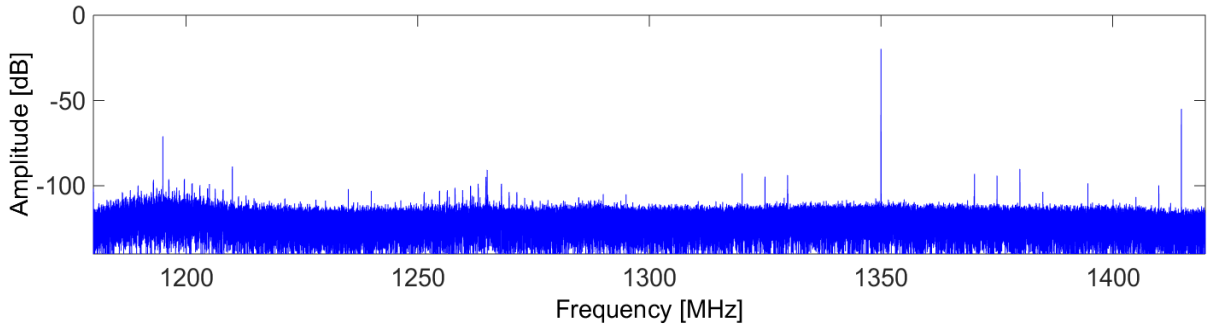

Figure C.2: Filtered 1350 MHz signal received on the TRB.

Appendix D: DAC Data

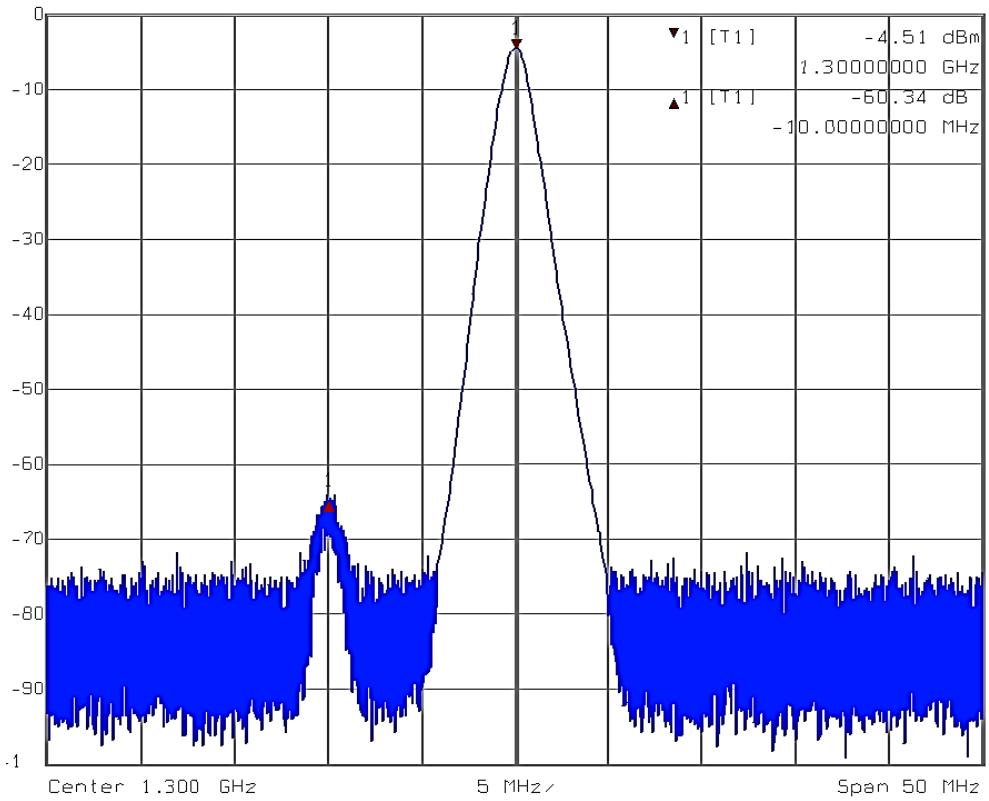

Figure D.1: Signal leakage between two channels on the same IC.

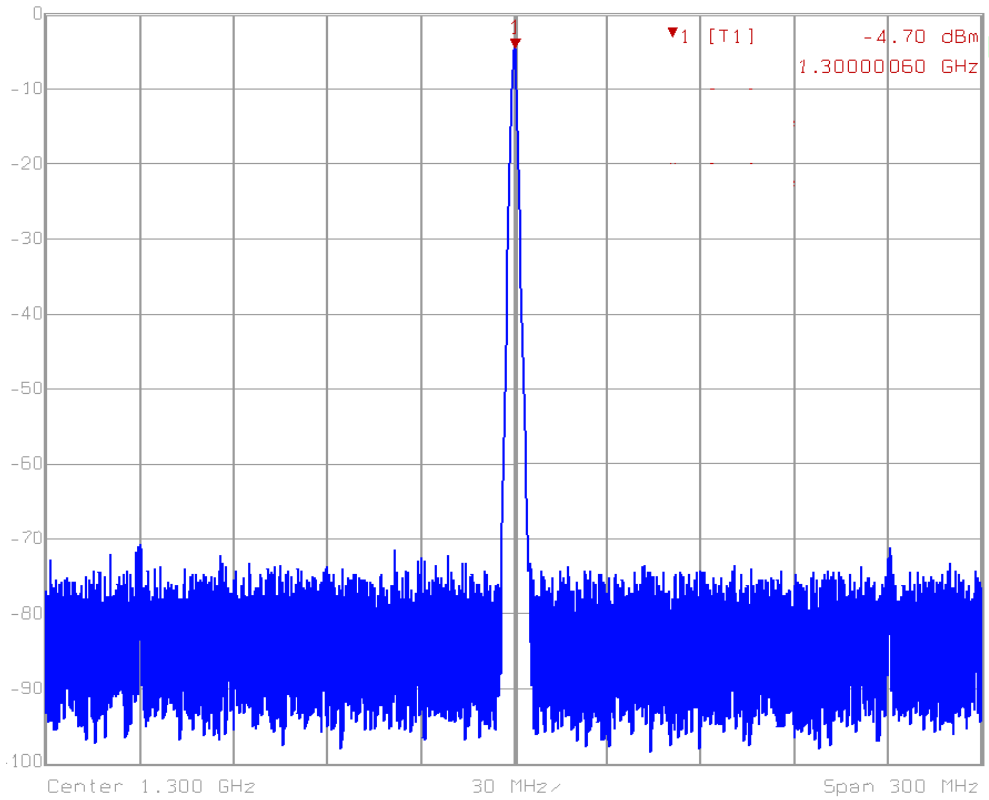

Figure D.2.: There is no signal leakage between two channels on different ICs.

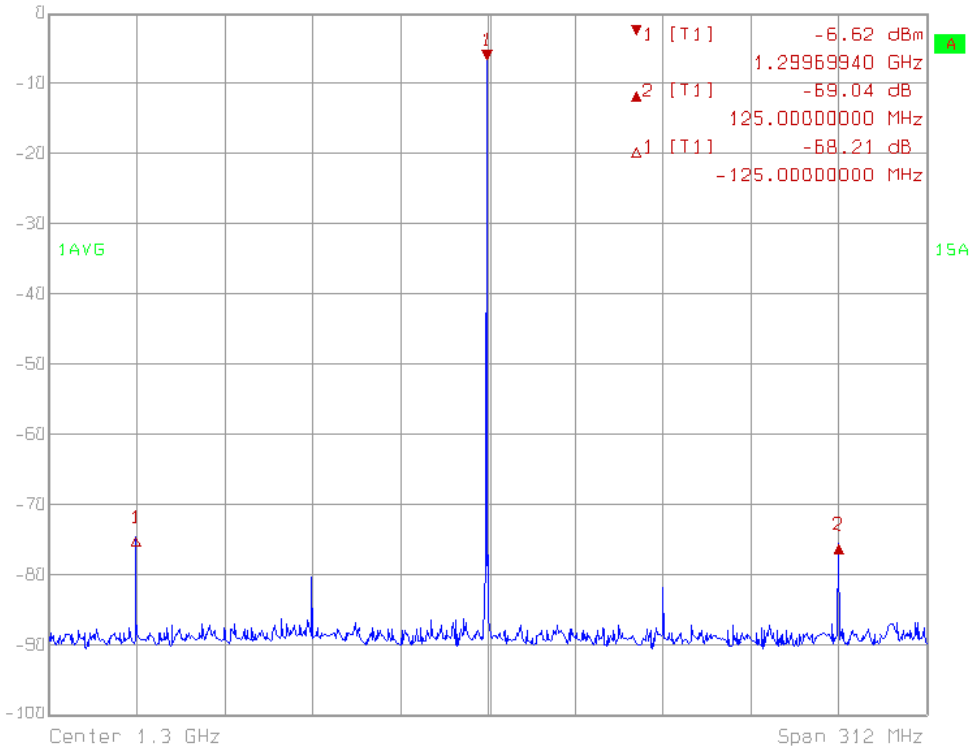

Figure D.3: 1300 MHz signal on output X7, with visible 125 MHz spurs.

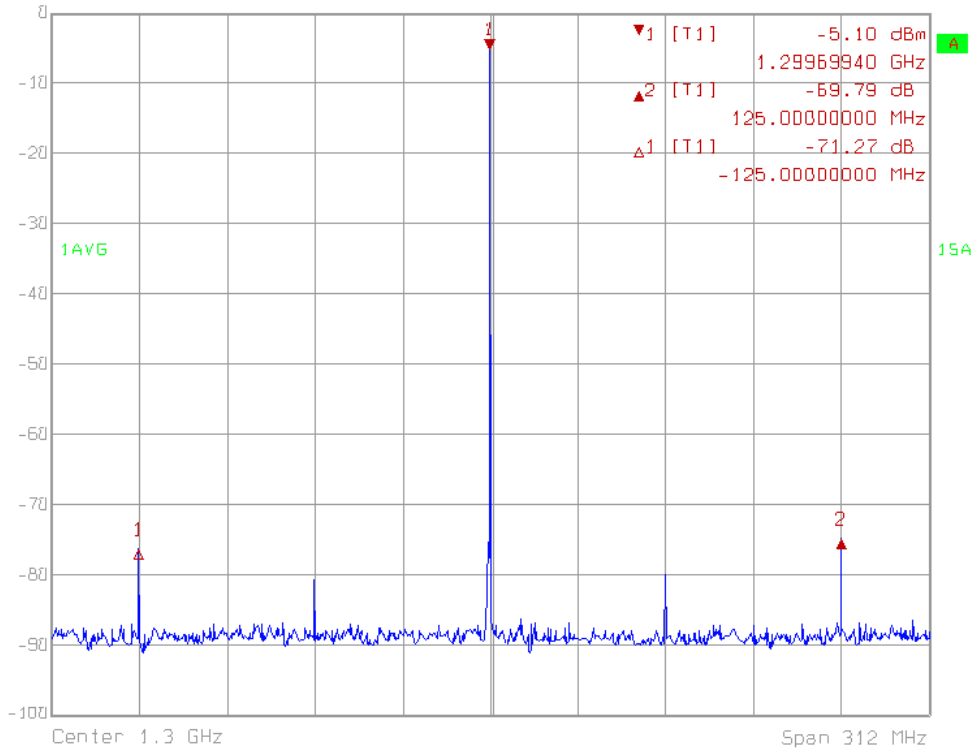

Figure D.4: 1300 MHz signal on output X11, with visible 125 MHz spurs.

Appendix E: Sampling Clock Data

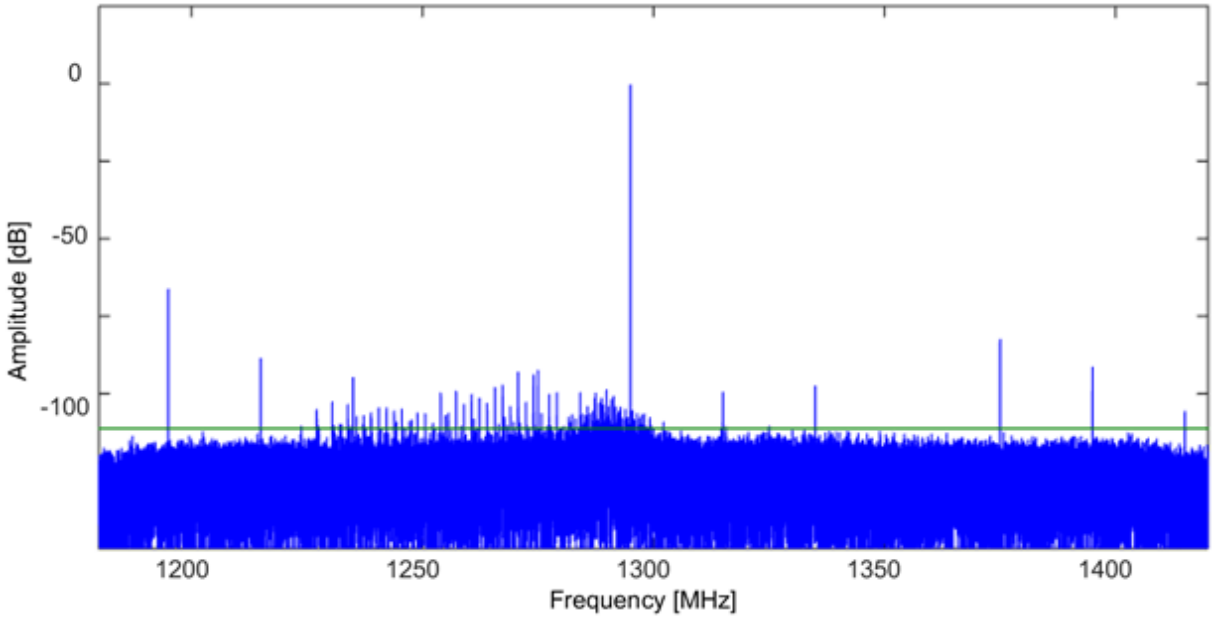

Figure E.1: The ADC data with a 1295 MHz carrier. The sampling clock is decreased with 6 dB.

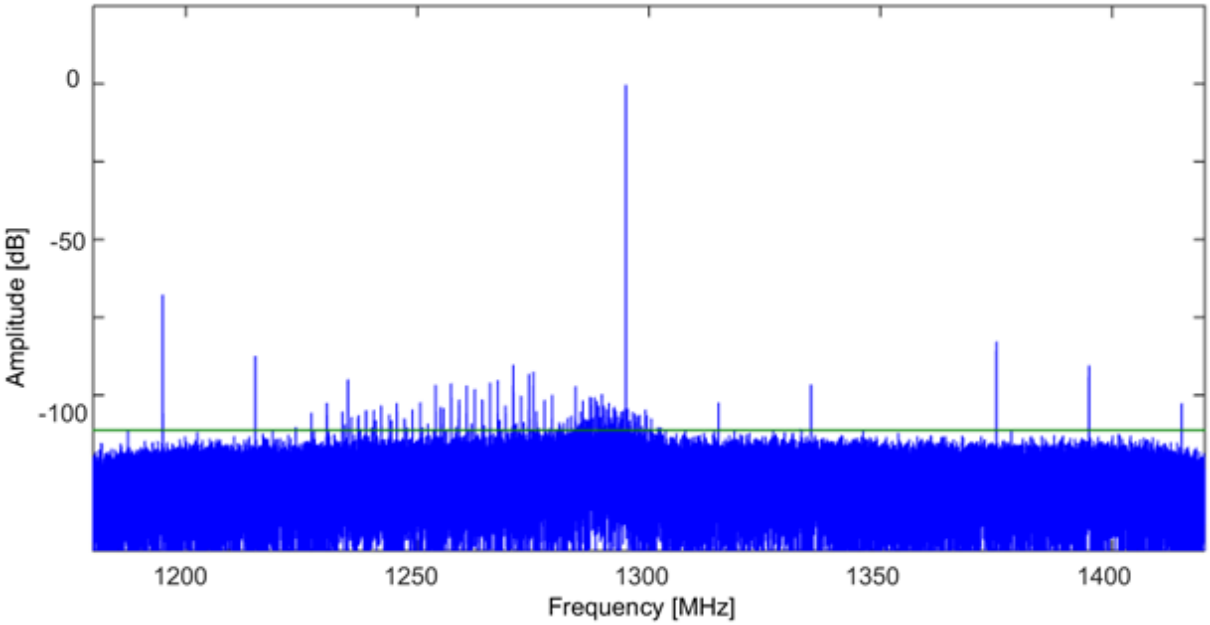

Figure E.2: The ADC data with a 1295 MHz carrier. The sampling clock is increased with 3 dB.