Effect of oxide traps on channel transport characteristics in graphene field effect transistors

Marlene Bonmann, Andrei Vorobiev, Jan Stake, and Olof Engström

---

Articles you may be interested in

Universal conformal ultrathin dielectrics on epitaxial graphene enabled by a graphene oxide seed layer
J. Vac. Sci. Technol. B **110**, 013106013106 (2017); 10.1063/1.4973200

Effect of oxide traps on channel transport characteristics in graphene field effect transistors

Marlene Bonmann,[a] Andrei Vorobiev, Jan Stake, and Olof Engström
Terahertz and Milimetre Wave Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Gothenburg, Sweden

A semiempirical model describing the influence of interface states on characteristics of gate capacitance and drain resistance versus gate voltage of top gated graphene field effect transistors is presented. By fitting our model to measurements of capacitance–voltage characteristics and relating the applied gate voltage to the Fermi level position, the interface state density is found. Knowing the interface state density allows us to fit our model to measured drain resistance–gate voltage characteristics. The extracted values of mobility and residual charge carrier concentration are compared with corresponding results from a commonly accepted model which neglects the effect of interface states. The authors show that mobility and residual charge carrier concentration differ significantly, if interface states are neglected. Furthermore, our approach allows us to investigate in detail how uncertainties in material parameters like the Fermi velocity and contact resistance influence the extracted values of interface state density, mobility, and residual charge carrier concentration. © 2017 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). [http://dx.doi.org/10.1116/1.4973904]

I. INTRODUCTION

The inherent high charge carrier velocity in graphene establishes its potential use in high frequency electronics. The intrinsic mobility limit in graphene at room temperature is predicted to be 2×10^5 cm^2/V s and conformed in suspended graphene.[1,2] During fabrication of top gated graphene field effect transistors (G-FET) the mobility is degraded. The application of a top gate dielectric affects the mobility significantly, due to extrinsic scattering mechanisms. When graphene needs to be transferred (in the form of exfoliated flakes or as a sheet grown by chemical vapor deposition on copper) onto a substrate prior to the fabrication of the top gate, the mobility might be reduced even more. The highest reported room-temperature mobility values in top-gated G-FET, utilizing different dielectric materials, including Al_2O_3, Y_2O_3, HfO_2, BN, SiC, SiO_2 and polymers, are still below 2.4×10^4 cm^2/V s.[3–7]

In literature, the carrier mobility of graphene has been extracted by different methods, some of which require additional structures in the form of Hall bars and van der Pauw structures.[5,7–9] The disadvantage of these methods is, that the conditions under which the mobility is obtained are not the same as for a transistor structure. Alternatively, a commonly accepted experimental method for finding mobility values by direct measurements on G-FETs is to fit a simplified expression for the drain resistance to drain resistance–gate voltage characteristics[10–14]

$$R = R_c + (L/W)(q\mu)^{-1}((n_0'^2 + (C(V_g - V_{Dirac})/q)^2)^{-1/2}. \tag{1}$$

The residual charge carrier concentration, n_0', the contact resistance, R_c, and mobility, μ, are fitting variables. L and W,

are the gate length and width, q is the elementary charge, C is the gate capacitance per unit area, V_g is the applied gate voltage, and V_{Dirac} is the applied gate voltage needed to position the Fermi-level of the graphene at the Dirac-point. The gate capacitance can be approximated as $C \approx C_{ox}$, when $C_{ox} \ll C_q$, where C_{ox} is the oxide capacitance and C_q is the quantum capacitance.

However, a hysteresis effect is often observed in capacitance and drain resistance characteristics for a dual sweep of the gate voltage. This indicates that charge carriers are captured in oxide traps within tunneling distance from the graphene/oxide interface. Hence, in contrast to the common view, the last term in Eq. (1) not only corresponds to concentration of carriers, n_G, in the graphene channel, but incorporates also carriers captured into oxide traps, n_{int}, such that

$$C_{ox}(V_g - V_{Dirac})/q = n_G + n_{int}. \tag{2}$$

Only n_G contributes to the conductivity of the graphene sheet. Ignoring the contribution of n_{int} will lead to an overestimation of n_G. Therefore, the mobility, μ, will be significantly underestimated, since the conductivity, σ, is given by $\sigma = q\mu n_G$. This expression is valid when the effect of charge accumulation near the edges can be neglected. In this work, we can neglect the edge effect since we consider transistors with 30 μm wide gates.[15] The amount of charge carriers, which is captured into oxide traps, depend on the nature of the traps and the applied gate voltage. The dynamics of injection and ejection of charge carriers, n_{int}, leads to an interface capacitance, C_{int}. In the capacitance model of G-FETs the contribution of the interface capacitance, C_{int}, is often neglected in the expression for the total capacitance, C_t.[10,16]

In the present study, we propose a semiempirical model for the dependency of oxide charges and charge carriers in

graphene on the applied gate voltage, including interface states. The model allows us to investigate their effect on resistance and capacitance characteristics and the extracted mobility values. Our approach has the advantage that we can examine limits set by uncertainties of material parameters such as Fermi velocity, capture and emission rates of charge carriers, and mobilities for electrons and holes.

II. EXPERIMENT

Measurements were performed on double-finger-gate G-FETs fabricated with gate lengths, $L = (0.3, 0.6, 1)$ μm and gate width, $W = 2 \times 30$ μm. Throughout this work we consider $L = 0.6$ μm. The ungated access length is 100 nm. Graphene was grown on a copper foil in a cold-wall low-pressure CVD system (Black Magic, AIXTRON Nanoinstruments, Ltd.) and transferred by a PMMA and frame assisted transfer method onto LiNbO$_3$ substrate. The LiNbO$_3$ substrate is a z-cut single crystal with spontaneous polarization pointing into the surface and the in-plane and out-of-plane dielectric constants of 85 and 25, respectively. After transfer of graphene, the GFET was formed in four steps by e-beam lithography. First, the source and drain were fabricated as stacks of 1 nm Ti/15 nm Pd/100 nm Au using e-beam evaporation followed by lift-off. Next, a seed layer for the gate oxide was applied by two steps of thermal oxidation of 1 nm thick Al films deposited by e-beam. Thereafter, the graphene mesa was formed, etching Al and graphene outside the mesa by HCl and O$_2$ plasma. Then, the gate was prepared by applying Al$_2$O$_3$ as gate dielectric and the gate metal 10 nm Ti/300 nm Au stack. Al$_2$O$_3$ was deposited by atomic layer deposition in thermal mode at 300 °C on top of the seed layer. The total thickness of the gate oxide was 17.5 nm with an estimated dielectric constant of 7.5. No annealing was performed. In the last step, the source and drain pads for contacting were prepared by evaporation of 10 nm Ti/305 nm Au and lift off. Transfer characteristics and capacitance–voltage (C-V) characteristics were measured using a Keithley 4200 semiconductor characterization system and an Agilent B1500A semiconductor device analyzer at 1 MHz,

respectively. The drain resistance was calculated as the ratio between drain voltage and drain current at the drain voltage equal to −0.1 V.

III. MODELING

A. Charge carriers and charges in intrinsic graphene

We built up our model starting from the Fermi distribution and the density of states (DOS) of graphene. The probability of a charge carrier to occupy an energy state at energy E is given by the Fermi distribution

$$f(E, E_F) = \left(1 + \exp\left(\frac{E - E_F}{k_B T}\right)\right)^{-1}, \quad (3)$$

where, k_B is the Boltzmann constant and $T = 300$ K and, E_F is the Fermi level. Figure 1(a) shows the occupation probability for electrons given by Eq. (3) and for holes given by (1-f). We define the Dirac point to be at $E = 0$ eV and the Fermi level, E_F, as the energy where the occupation probability is 0.5. It is important to realize that for temperatures $T > 0$ K the occupation probability for electrons at energies $E > 0$ eV and holes at $E < 0$ eV is not zero. This is the origin of thermally generated charge carriers, n_{th}. The density of states describes the number of states per m^2 and eV. For pristine graphene, it is derived as[17]

$$g(E) = \frac{2q^2}{\pi \hbar^2 v_F^2} |E|, \quad (4)$$

where, q is the elementary charge, $\hbar$ is the reduced Planck's constant and, v_F is the Fermi velocity. It has a linear dependence on the energy and the slope is determined by the Fermi velocity, v_F. There are various values of Fermi velocity reported in literature ranging from 0.8×10^6 m/s to 3×10^6 m/s depending on the substrate.[10,18–21]

The smallest values of v_F are associated with substrates with high permittivity. Figure 1(b) shows the DOS for various values of the Fermi velocity. Since the DOS depends on the Fermi velocity as $\alpha \, v_F^{-2}$, the slope of DOS becomes
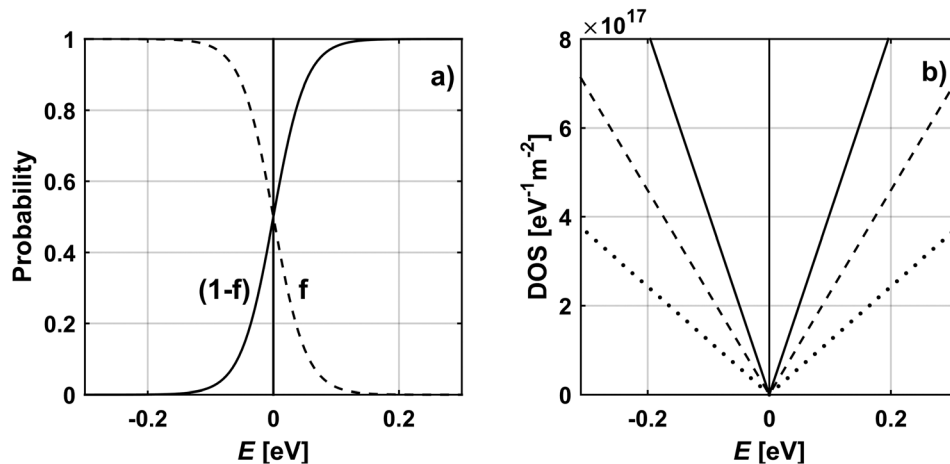

FIG. 1. (a) Fermi distribution of electrons, *f*, and holes, (1-f). (b) Density of states vs energy for Fermi velocities of $v_F = 0.6$ (solid line), 0.8 (dashed line) and 1.0×10^6 m/s (dotted line).

steeper with decreasing Fermi velocity. This strongly affects the concentration of electrons, n_e, and holes, n_h, since these quantities are obtained as

$$n_e(E_F) = \int_0^\infty g(E)f(E, E_F)dE ,$$ (5)

and

$$n_h(E_F) = \int_{-\infty}^0 g(E)(1 - f(E, E_F))dE,$$ (6)

respectively. In intrinsic graphene the charge, Q_G, is calculated by the difference of electron and hole concentrations

$$Q_G(E_F) = qn_h(E_F) - qn_e(E_F) = -q\,\mathrm{sign}(E_F)\frac{4\pi q^2 (E_F)^2}{(hv_F)^2}.$$ (7)

The total charge carrier concentration is calculated by the sum of electron and hole concentrations

$$n_G(E_F) = n_e(E_F) + n_h(E_F) .$$ (8)

Figure 2 demonstrates the dependency on the Fermi level position for carrier densities of electrons, $[g(E)f(E, E_F)]$ and holes $[g(E)(1 - f(E, E_F))]$, the charge in graphene, Q_G, and the charge carrier concentration, n_G. The area under the curves in Fig. 2(a) is equal to the concentration of the respective charge carrier type. Moving the Fermi level toward higher energies increases the electron density and, simultaneously, the hole density decreases significantly [Figs. 2(b) and 2(c)]. This results in a negative net charge in graphene, Q_G [Fig. 2(d)] and the charge carrier concentration, n_G, is dominated by the electron concentration [Fig. 2(e)]. At $E_F = 0$ eV the concentration of holes and electrons is equal, leading to a charge carrier concentration, n_G, while the net
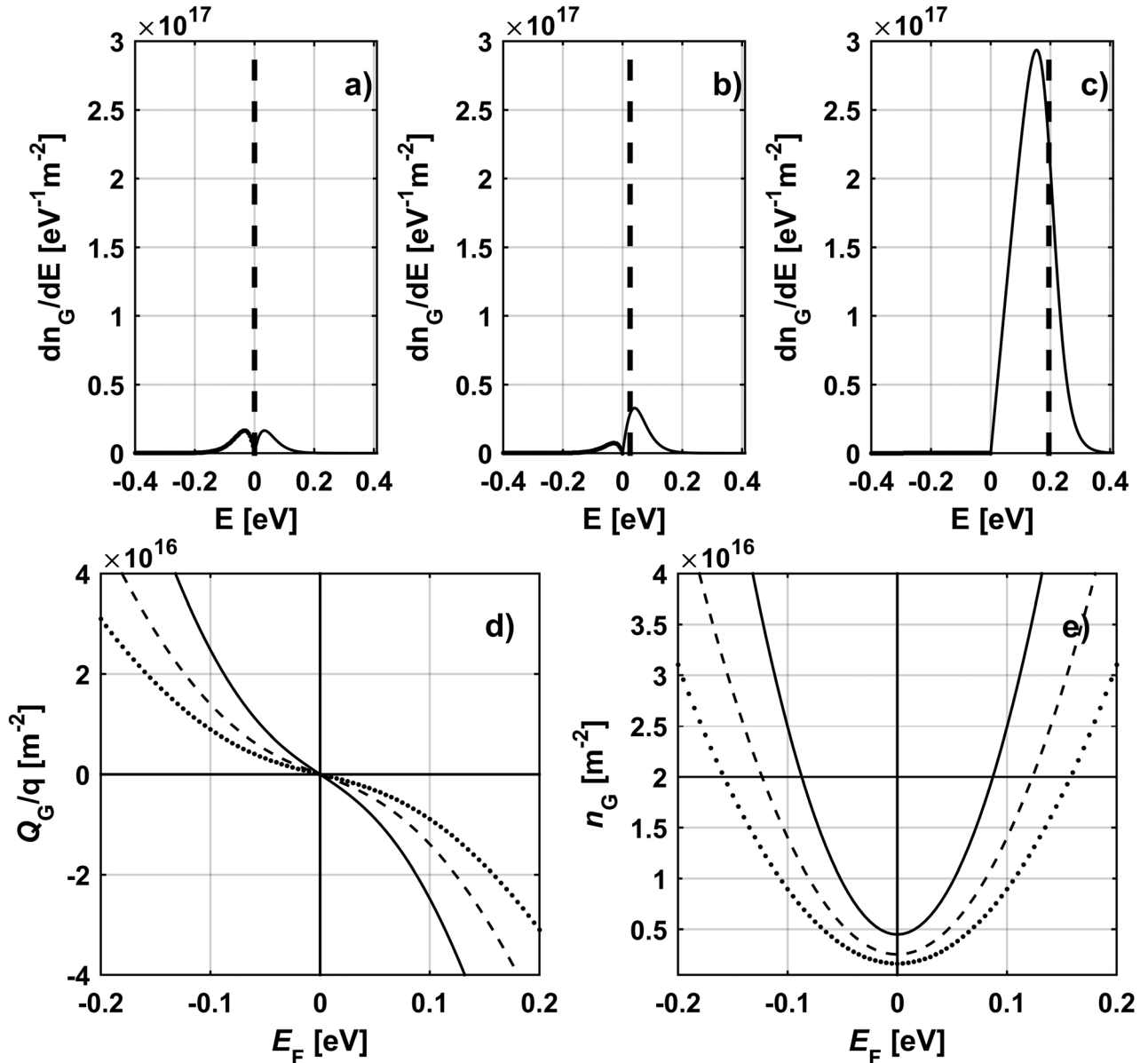

FIG. 2. (a)–(c) Carrier densities for holes (thick line) and electrons (slim line) for different position of the Fermi level (black dashed line). (d) Net charge, Q_G, and (e) total charge carrier concentration, n_G, vs Fermi level position for Fermi velocities of $v_F = 0.6$ (solid line), 0.8 (dashed line) and 1.0×10^6 m/s (dotted line).

charge, Q_G, is zero. Moving the Fermi level from positive to negative energies will result in change of the sign of the net charge from negative to positive, since the dominating charge carrier type changes. The charge carrier concentration, n_G, depends strongly on the Fermi velocity since it enters Eq. (4) as v_F^{-2}. It is worth noting that an increase of δv_F by about 20% decreases the concentration of charge carriers by 50%.

B. Interface charge and capacitances

The total capacitance is given by the oxide capacitance, C_{ox}, in series with quantum capacitance, C_q, and interface capacitance, C_{int}, connected in parallel. The equivalent circuit for the total capacitance is shown in the inset of Fig. 3(c) and calculated as

$$C_t = \frac{C_{ox}(C_{int} + C_q)}{C_{ox} + C_{int} + C_q}, \tag{9}$$

where

$$C_{ox} = k\varepsilon_0 \frac{A}{t_{ox}}, \tag{10}$$

and[17]

$$C_q = A \frac{8\pi k_B T q^2}{(hv_F)^2} \ln\left[2 + 2\text{Cosh}\left(\frac{E_F}{k_B T}\right)\right]. \tag{11}$$

The quantum capacitance, C_q, is defined as the derivative of the total net charge in graphene with respect to the applied electrostatic potential. Its dependence on Fermi level position is shown together with the oxide capacitance, C_{ox}, in Fig. 3(a). While C_{ox} is constant, C_q increases symmetrically around $E_F = 0\,\text{eV}$. Furthermore, it can be seen in Figs. 3(a) and 3(c) that small variations of the Fermi velocity will strongly affect the value of C_q and thus also the total capacitance, C_t, since the Fermi velocity enters Eq. (11) as v_F^{-2}. C_q and C_t are parallel shifted to smaller capacitance values with an increase of the Fermi velocity. The interface capacitance is calculated as

$$C_{int} = A \int_{-\infty}^{\infty} \chi_{int} dE. \tag{12}$$

χ_{int} is the capacitance density per energy and area unit as derived in[22]

$$\chi_{int} = \frac{q^2}{k_B T} \frac{N_{id} + N_{ia}}{2} \frac{2e_n^2}{4e_n^2 + \omega^2} f(1-f), \tag{13}$$

where, $\omega = 1\,\text{MHz}$, is the measurement frequency and, e_n, the tunneling emission and capture rates of charge carriers that we set to 50 MHz. N_{id}, and, N_{ia}, denote donorlike and acceptorlike interface state densities, respectively, situated close to the graphene/oxide interface, thus contributing to the interface capacitance.

C_{int} versus Fermi level position and C_t versus the applied gate voltage is shown in Figs. 3(b) and 3(d) for different interface state densities $N_{int} = N_{id} = N_{ia}$. It can be seen in Fig. 3(b) that constant interface state distribution results in constant interface capacitance and the higher the interface state density the bigger the interface capacitance. The graphs of C_t versus gate voltage become wider for higher interface state densities, e.g., higher interface capacitance [Fig. 3(d)]. The widening of the curves is caused by the increase in the net negative interface charge by shifting the Fermi level to higher energy, i.e., increasing V_g. This will gradually move the capacitance graph toward higher values on the V_g axis. A corresponding gradual negative voltage shift takes place when the Fermi-level moves in the negative energy direction. Figure 4(a) shows how the net interface charge, Q_{int}, depends on the Fermi level position and the interface state density, N_{int}. Acceptorlike states are negatively charged below the Fermi level and neutral above. Donorslike states are neutral below the Fermi level and positive above. If the density of the donorlike states is higher than the density of acceptorlike states, there will be a net charge at the interface for $E_F = 0\,\text{eV}$. The interface charge, Q_{int}, the bulk oxide charge, Q_{ox}, and the charge, Q_G, in the graphene layer influence the relation between applied gate voltage and the Fermi-level position according to[23]

$$V_g(E_F) = \Phi_{ms} - \frac{Q_{ox} + Q_G(E_F) + Q_{int}(E_F)}{C_{ox}} + \frac{E_F}{q}, \tag{14}$$

where, Q_{ox} is constant or varies slowly and gives rise to hysteresis when ramping V_g. Generally, there is a work function difference, Φ_{ms}, between the gate metal and the graphene. This would give rise to a parallel shift of the minimum of the C-V curves along the voltage axis. However, the value of Φ_{ms} is hard to predict, especially since the work function of graphene has been suggested to be tuned by the electric field.[24] Furthermore, for the present samples, the Dirac point is close to $V_g \sim 0\,\text{V}$ [Figs. 5(a) and 5(b)]. Therefore, in our model, we assume that the work function difference between the gate metal and graphene can be neglected in Eq. (14). The relation between the applied gate voltage and Fermi level position according to Eq. (14) for different interface state densities, N_{int}, is shown in Fig. 4(b). The gate effect is strongly reduced for higher N_{int}. That means, a higher gate voltage needs to be applied to the gate to obtain the same relative shift of the Fermi level to the Dirac point. The black dashed line in Fig. 4(b) indicates the relation between applied gate voltage and Fermi level if no interface states were apparent. For $N_{int} < 0.02 \times 10^{18}\,\text{m}^{-2}\text{eV}^{-1}$ and $E_F < \pm 0.2\,\text{eV}$ the influence of the interface charge in Eq. (14) can be nearly neglected.

C. Drain resistance versus gate voltage

We used E_F as the independent parameter in all our calculations, which means that the influence of interface charges, charge carrier concentrations, capacitances, and gate voltage are calculated as a function of the Fermi level position. All charge is automatically taken into account by using Eq. (14). A change in the position of E_F will change interface charge, Q_{it}, and entail a change in Q_G, and finally
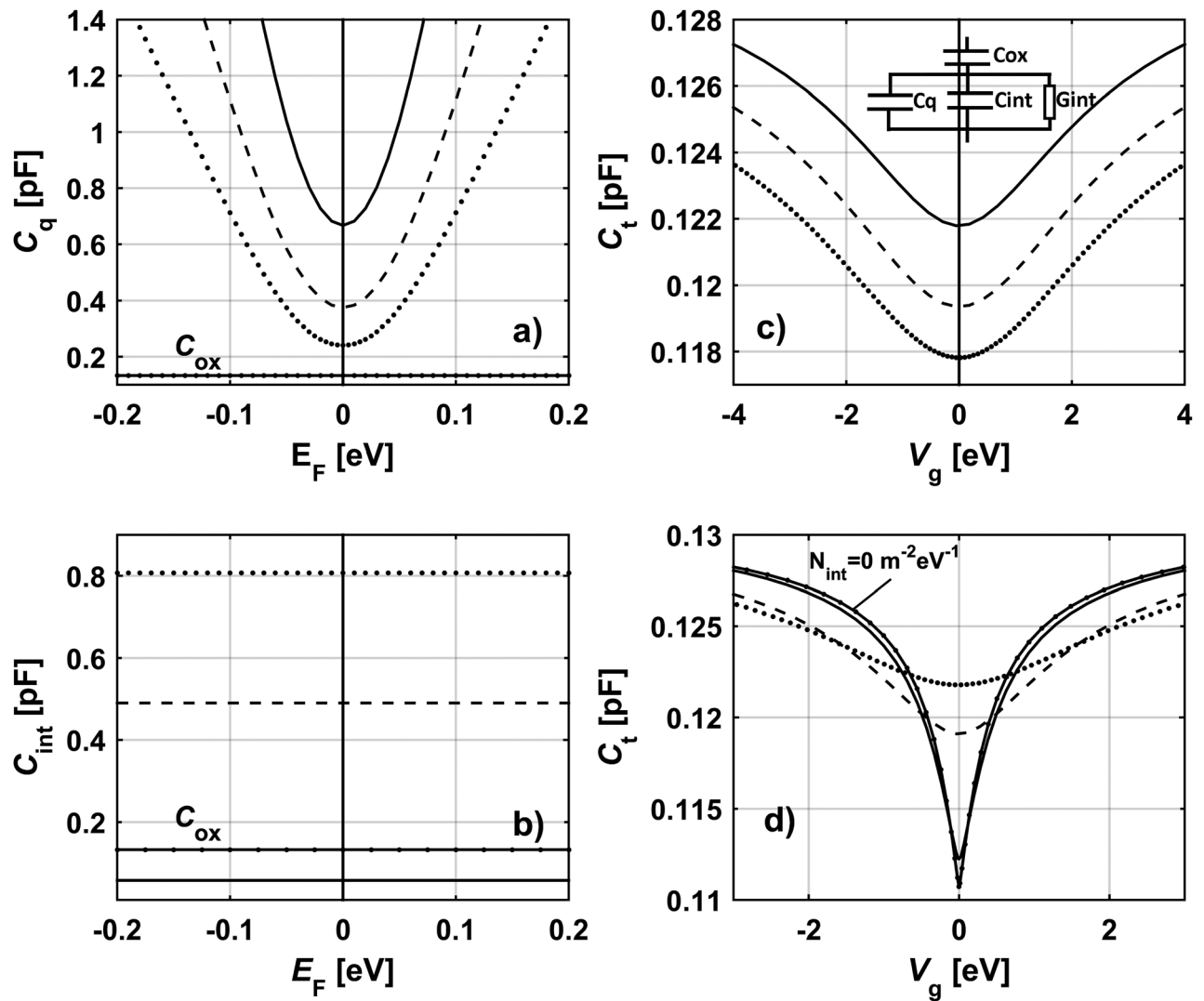
FIG. 3. (a) Quantum capacitance, C_q, and (b) interface capacitance, C_{int}, as function of Fermi level position, E_F. (c) and (d) Total capacitance, C_t, as function of gate voltage, V_g. In (a) and (c) v_F is varied as $v_F = 0.6$ (solid line), 0.8 (dashed line) and 1.0×10^6 m/s (dotted line), while in (c) $N_{int} = 0.28 \times 10^{18}$ m^{-2}eV^{-1}. The inset shows the equivalent circuit of the total capacitance, C_t. In (b) and (d) N_{int} is varied as $N_{int} = 0.02$ (solid line), 0.17 (dashed line) and 0.28×10^{18} m^{-2}eV^{-1} (dotted line), while in (d) $v_F = 0.6 \times 10^6$ m/s.
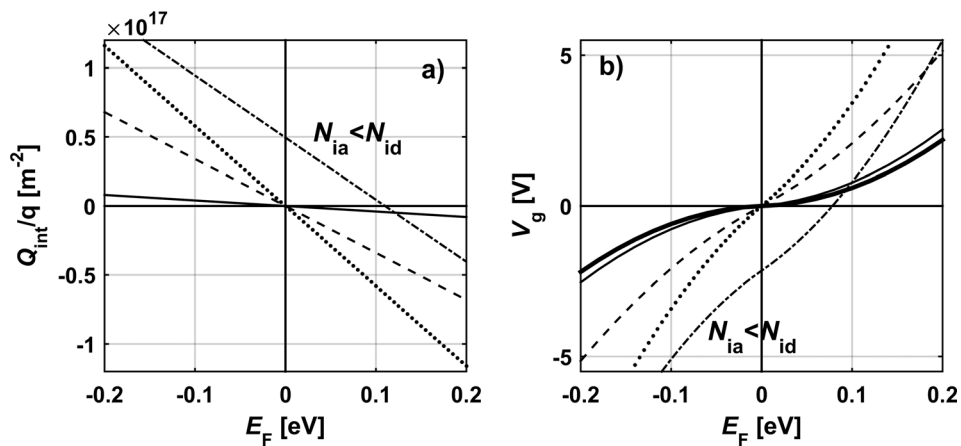

FIG. 4. (a) Interface charge, Q_{int}, and (b) applied gate voltage, V_g, vs Fermi level, E_F, for $N_{int} = 0.02$ (solid line), 0.17 (dashed line) and 0.28×10^{18} m^{-2}eV^{-1} (dotted line). The dash-dotted graphs show the dependencies when the density of donorlike interface states is higher than density of acceptorlike interface states.
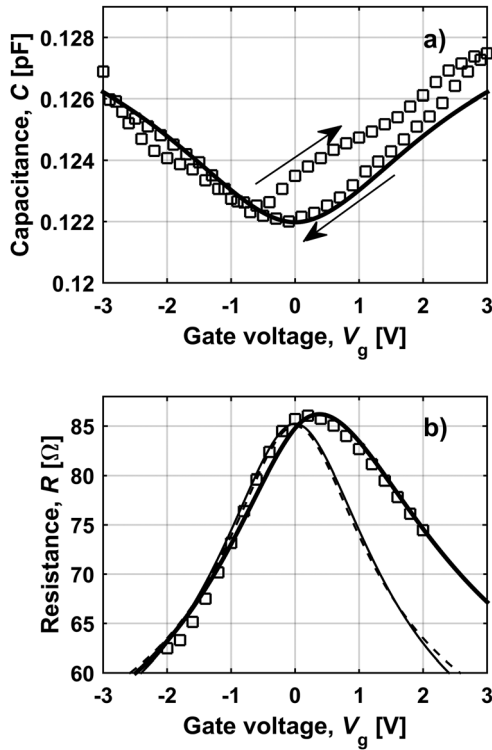
FIG. 5. Fit (solid bold line) of model in this work to measured (squares) (a) capacitance–gate voltage and (b) drain resistance–gate voltage characteristics. In (b) the fitting results of our model [Eq. (15), with equal hole and electron mobilities (solid slim line)] are compared to the commonly used model [Eq. (1), dashed line].

V_g. Using this technique, we suggest a modified model for the drain resistance

$$R(V_g) = R_C + \frac{L}{W} \frac{1}{q(\mu_h(n_h + n_0/2) + \mu_e(n_e + n_0/2))}. \tag{15}$$

The denominator is the conductivity $\sigma = q(\mu_h(n_h + n_0/2) + \mu_e(n_e + n_0/2))$. The electron and hole concentrations, n_e and n_h, dependent on Fermi level are calculated according to Eqs. (5) and (6). We use a residual charge carrier concentration, n_0, occurring close to the Dirac point which consists equally of holes and electrons. In Eq. (1) the residual charge carrier concentration is commonly defined as $n'_0 = n_{th} + \delta n$, where n_{th} is the thermally generated charge carrier concentration. δn is the charge carrier concentration due to potential fluctuations (puddles) created by impurities in the oxide and the substrate close to the graphene interface.[16,25–27] We take n_{th} into account by the sum of $n_e + n_h$ at the Dirac point in Eq. (8). Therefore, in our definition of the residual charge carrier concentration is $n_0 = \delta n$, only.

As will be demonstrated below, the measured channel resistance characteristic shows an asymmetry for the hole and electron branch. This appearance is expected since holes and electrons have different scattering cross sections in the vicinity of charged impurities.[28,29] An additional effect may originate from a change in contact resistance due to the formation of p-n junctions along the graphene channel.[30–32]

Furthermore, in a recent work the channel width is argued to vary, when charge puddles alter the effective channel area.[33] In the present analysis, we follow theoretical predictions[29] and assume different mobilities for electrons, μ_e, and holes, μ_h. Transistors studied in this work exhibit underlap (access length between source/drain and gate), which contribute to the contact resistance, R_c. Hence, one can expect modulation of contact resistance with gate voltage due to the fringing field effect.[34] According to our estimation, this modulation can be neglected in our transistors because of much shorter access length (0.1 μm). It is worthwhile to observe that we do not use the square root in the denominator of R in our model [Eq. (15)]. The square root part in Eq. (1) seems to lack physical background and barely fulfils the need to provide a correct value for the mobility.

IV. RESULTS AND DISCUSSION

A. Results

The output, the transfer, and the C-V characteristics of our devices show hysteresis as can be seen for the C-V characteristic in Fig. 5(a). This is a common feature observed for graphene field effect transistors.[35,36] The hysteresis can be associated with capture and emission of charge carriers into and out of traps situated relatively deep in the oxide compared to interface traps. While interface traps influence the capacitance level [Fig. 3(d)], the charging of bulk oxide traps affects the value of the gate voltage for a given position of the Fermi-level [Eq. (14), Fig. 4(b)]. When the bulk oxide traps are filled by negative charge in the period of the measurement cycle the Dirac point, V_{Dirac}, is shifted to higher voltage, when sweeping the gate voltage back from $V_g = 3$ to -3 V. The shift and, consequently, the hysteresis is the same in both, the transfer and the C-V characteristics. $V_{Dirac} \approx 0$ V is an indication that the deep laying bulk oxide traps have donor character and become neutral when filled with electrons. Figures 5(a) and 5(b) demonstrates the fit of our model to capacitance and resistance measurements. The interface state density, $N_{int} = N_{id} = N_{ia}$, is found by fitting the expression for the total capacitance [Eq. (9)] to the measured capacitance–gate voltage characteristic using Eqs. (10)–(14). The extracted interface state density is high, which is reasonable since the capacitance variation of about 3% is much smaller than expected from an intrinsic structure. The capacitance minimum point depends on the density of interface states as shown in Fig. 3(d), but also on the rate of tunneling emission between the states and the channel, e_n. Uncertain parameters are the Fermi velocity in Eq. (11) and, e_n, in Eq. (13). The rate, e_n, is set to 50 MHz. In this way, all interface states are assumed to contribute to the interface capacitance.

The mobilities, μ_e and μ_h, the contact resistance, R_C, and residual charge carrier concentration, n_0, are obtained by fitting Eq. (15) to the measured resistance characteristic. The fitting parameters are summarized in Table I. We found that the best fit for R_C was in the range 43–47 Ω and use the average $R_C = 45$ Ω when extracting the mobility values. For $R_C = 43$ Ω, the mobility values for fitting needed to be decreased by ~10%. For $R_C = 47$ Ω, n_0 needed to be

TABLE I. Fitting parameters of Eqs. (9) and (15) to the measured capacitance and resistance characteristic in Figs. 5(a) and 5(b), respectively.

v_F (m/s)	$N_{int} \times 10^{18}$ (m^{-2})	$n_0 \times 10^{16}$ (m^{-2})	μ_h (cm^2/V s)	μ_e (cm^2/V s)
0.6	0.29	0.6	2050	950
0.8	0.28	0.4	3100	1600
1.1	0.25	0.28	4900	2600

decreased by ($\sim$10%) while mobilities needs to be increased by $\sim$20%, in order to obtain well fitting. Comparing the fitting parameters in Table I for different values of the Fermi velocity, a critical point becomes apparent. Small differences in $\Delta v_F = 0.2 \times 10^6$ m/s lead to extracted mobility values that differ approximately $\Delta \mu = 0.1$ m^2/V s for both electron and hole mobilities. The Fermi velocity for graphene on LiNbO$_3$ substrate is not exactly known, but can be expected to be smaller than in SiO$_2$ ($\sim$1.1–1.3 $\times 10^6$ m/s), due to the high dielectric constant in LiNbO$_3$.[18]

Furthermore, we compare the extracted mobility values obtained from the commonly used model according to Eq. (1) and our approach Eq. (15). The result is shown in Fig. 5(b) and the fitting parameters are summarized in Tabel II. For this case, we consider equal mobility for electrons and holes in our model since the commonly used model does not distinguish between mobilities for different charge carrier types. We found an equally good fit of the hole branch for both approaches, but the extracted mobility values differ considerably (Table II). While the former method extracts a very low mobility value of 670 cm^2/V s we extract a mobility of 2400 cm^2/V s. Also, the extracted values for n'_0 and n_0 disagree by a factor $n'_0/n_0 \approx 10$. That could be expected, since we do not need to include the thermally generated charge carriers in the expression for n_0. The thermally generated charge carriers are already included in $n_h + n_e$ and should only contribute with maximal 0.5×10^{16} m^{-2} [see Fig. 2(b)]. Another reason for the high value for n'_0 needed in the commonly used approach is that it leads to a widening of the resistance curve, which cannot be obtained in another way if the interface charge and the relation of Eq. (14) is not taken into account.

B. Discussion

Assumptions have been made for some of the parameters, which influence the values of interface density, mobility, contact resistance, and residual charge carrier concentration. First, reported Fermi velocities of graphene differ depending on the substrates the graphene was transferred onto. Even for the most common substrate SiO$_2$ exist different results for the Fermi velocity.[10,18–21] Since the density of states is proportional to the Fermi velocity as $\propto v_F^{-2}$, a small change in Fermi velocity has a strong effect

on the charge carrier concentration in the graphene channel [Fig. 2(b)]. The product of charge carrier concentration and mobility determines the conductivity in the graphene sheet as, $\sigma = q\mu n_G$, and hence an uncertainty in n_G affects the extracted mobility value. A second assumption for the applicability of the model is that the mobility needs to be independent on charge carrier concentration. This means that the dominating scattering mechanism is governed by Coulomb interaction with charged electron states in the oxide.[37] Furthermore we assume that the mobility depends on charge carrier type. Especially at the Dirac point, where the concentration of holes and electrons is equal [Fig. 2(a)] the mobility for both types of charge carriers should be taken into account. The difference between the mobilities of electrons and holes can explain the observed asymmetry of the measured resistance curves. Other possible sources for the asymmetry are discussed above in Sec. III of the drain resistance.

We fitted our model using a constant energy distribution of interface states. This approximation is reasonable, since we move the Fermi level in our samples only about $\Delta E_F \sim \pm 0.07$ eV for a variation of ± 3 V of the gate voltage, due to the high concentration of interface states [Fig. 3(c)]. In addition the tunneling emission and capture rates of charge carriers, e_n, is high so that all interface states are assumed to contribute to the interface capacitance.

It would be beneficial if the extracted values obtained by the two different models described in this work could be compared to a third independent method. A possibility is the method of transfer length measurement (TML) to extract contact resistance and Hall and van der Pauw measurements to obtain mobility and carrier concentration in a graphene sheet.[5,7–9] It was shown that the contact resistance extracted by TML and the fitting procedure of resistance characteristics does not give the same result for the extracted contact resistance, since the processing steps for the test structures differ from the processing steps of the transistors.[38] Especially, the fabrication of the top gate of the transistor is likely to introduce defects and impurities. Additional impurities influence the mobility in the device negatively.[39] Hence, a direct comparison between contact resistance and mobility extracted by TML and Hall measurements and from a top gated transistor would not be fully correct.

TABLE II. Fitting parameters of Eqs. (1) and (15) to the measured resistance characteristics in Figs. 5(b). In Eq. (15) equal hole and electron mobility was used.

	$N_{int} \times 10^{18}$ (m^{-2})	$n'_0/n_0 \times 10^{16}$ (m^{-2})	μ (cm^2/V s)
Eq. (1)	—	2.4	650
Eq. (15)	0.29	0.2	2400

V. CONCLUSIONS

We developed a model which describes the influence of interface states on characteristics of gate capacitance and drain resistance versus gate voltage of G-FETs. We showed that incorrect estimation of the charge carrier concentration, n_G, in G-FETs entails a misinterpretation of the extracted parameters, such as the mobility and residual charge carrier concentration. The correct estimation of, n_G, depends strongly on the correct data for the Fermi velocity in the substrate and the interface state density, N_{int}. We included the effect of interface states in our model, compared the results with the commonly accepted model[10] and found that the extracted values for mobility and residual charge carrier concentration differ largely between the models.

ACKNOWLEDGMENTS

[1] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, Nat. Nanotechnol. **3**, 206 (2008).

[2] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, Solid State Commun. **146**, 351 (2008).

[3] Y. Liang, X. Lang, Z. Zhang, W. Li, X. Huo, and L. Peng, Nanoscale **7**, 10954 (2015).

[4] B. Fallahazad, S. Kim, L. Colombo, and E. Tutuc, Appl. Phys. Lett. **97**, 123105 (2010).

[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).

[6] L. Wang *et al.*, Science **342**, 614 (2013).

[7] T. Ciuk, P. Caban, and W. Strupinski, Carbon **101**, 431 (2016).

[8] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, Phys. Rev. Lett. **101**, 96802 (2008).

[9] L. J. van der Pauw, Philips Res. Rep. **13**, 1 (1958).

[10] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, and Z. Yao, Appl. Phys. Lett. **94**, 62107 (2009).

[11] M. A. Uddin, N. Glavin, A. Singh, R. Naguy, M. Jespersen, A. Voevodin, and G. Koley, Appl. Phys. Lett. **107**, 203110 (2015).

[12] A. Di Bartolomeo, F. Giubileo, F. Romeo, P. Sabatino, G. Carapella, L. Iemmo, T. Schroeder, and G. Lupina, Nanotechnology **26**, 475202 (2015).

[13] S. Sarkar, K. R. Amin, R. Modak, A. Singh, S. Mukerjee, and A. Bid, Sci. Rep. **5**, 16772 (2015).

[14] S. Bidmeshkipour, A. Vorobiev, M. A. Andersson, A. Kompany, and J. Stake, Appl. Phys. Lett. **107**, 173106 (2015).

[15] P. G. Silvestrov and K. B. Efetov, Phys. Rev. B **77**, 155436 (2008).

[16] J. Tian, A. Katsounaros, D. Smith, and Y. Hao, IEEE Trans. Electron Devices **62**, 3433 (2015).

[17] G. I. Zebrev, *Physics and Applications of Graphene-Theory* (InTech, Rijeka, Croatia, 2011).

[18] C. Hwang, D. A. Siegel, S.-K. Mo, W. Regan, A. Ismach, Y. Zhang, A. Zettl, and A. Lanzara, Sci. Rep. **2**, 590 (2012).

[19] R. S. Deacon, K.-C. Chuang, R. J. Nicholas, K. S. Novoselov, and A. K. Geim, Phys. Rev. B **76**, 81406 (2007).

[20] W. Zhu, V. Perebeinos, M. Freitag, and P. Avouris, Phys. Rev. B **80**, 235402 (2009).

[21] G. Li, A. Luican, and E. Y. Andrei, Phys. Rev. Lett. **102**, 176804 (2009).

[22] J. Piscator, B. Raeissi, and O. Engstroüm, J. Appl. Phys. **106**, 54510 (2009).

[23] O. Engstrom, *The MOS System* (Cambridge University, United Kingdom, 2014).

[24] Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, Nano Lett. **9**, 3430 (2009).

[25] H. Xu, Z. Zhang, and L.-M. Peng, Appl. Phys. Lett. **98**, 133122 (2011).

[26] S. Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma, Proc. Natl. Acad. Sci. U. S. A. **104**, 18392 (2007).

[27] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby, Nat. Phys. **4**, 144 (2008).

[28] J.-H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, Nat. Phys. **4**, 377 (2008).

[29] D. S. Novikov, Appl. Phys. Lett. **91**, 102102 (2007).

[30] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, *2009 IEEE International Electron Devices Meeting (IEDM)* (International Electron Devices Meeting (IEDM), Montgomery Village, MD, 2009), pp. 1–4.

[31] J. W. Liu *et al.*, IEEE Electron Device Lett. **32**, 128 (2011).

[32] B. Huard, N. Stander, J. A. Sulpizio, and D. Goldhaber-Gordon, Phys. Rev. B **78**, 121402 (2008).

[33] Y. G. Lee, S. K. Lim, C. G. Kang, Y. J. Kim, D. H. Choi, H.-J. Chung, R. Choi, and B. H. Lee, Microelectron. Eng. **163**, 55 (2016).

[34] H. Wang, A. Hsu, D. S. Lee, K. K. Kim, J. Kong, and T. Palacios, IEEE Electron Device Lett. **33**, 324 (2012).

[35] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, ACS Nano **4**, 7221 (2010).

[36] A. A. Sagade, D. Neumaier, D. Schall, M. Otto, A. Pesquera, A. Centeno, A. Z. Elorza, and H. Kurz, Nanoscale **7**, 3558 (2015).

[37] S. Adam, E. H. Hwang, and S. Das Sarma, Physica E **40**, 1022 (2008).

[38] J. Anteroinen, W. Kim, K. Stadius, J. Riikonen, H. Lipsanen, and J. Ryynänen, World Acad. Sci. Eng. Technol. **6**, 1604 (2012).

[39] M. C. Lemme, T. J. Echtermeyer, M. Baus, B. N. Szafranek, J. Bolten, M. Schmidt, T. Wahlbrink, and H. Kurz, Solid State Electron. **52**, 514 (2008).