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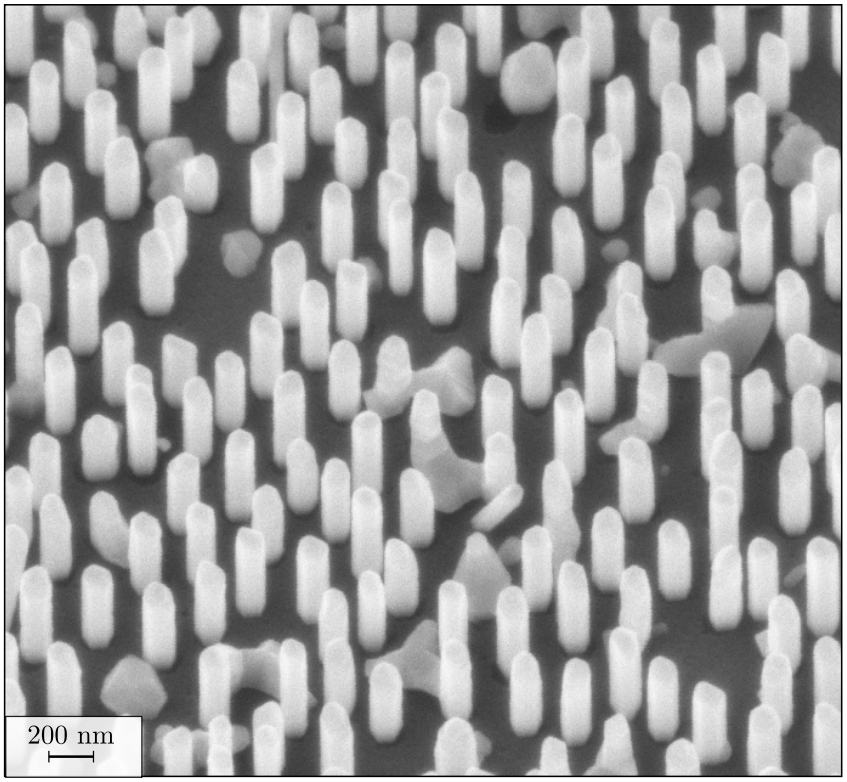

Synthesis of Catalyst-Free InAs Nanowires on Silicon

Thesis for the Erasmus Mundus Master of Science in Nanoscience and Nanotechnology

KU LEUVEN

GHADA BADAWY

Promoter: Prof. Huan Zhao
Co-promoter: Prof. Marc Heyns

Department of Microtechnology and Nanoscience
Terahertz and Millimetre Wave Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
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External referee: Prof. Thilo Bauch

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience
Chalmers University of Technology
SE-412 96 Göteborg
Sweden

Cover: 30 degree tilt of a scanning electron microscope (SEM) micrograph of vertically oriented InAs nanowires on lithographically patterned silicon-dioxide-masked silicon substrates using one of the techniques discussed in this thesis.

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Abstract

Semiconductor nanowires are nanometre-sized structures offering a wealth of unique and novel properties affiliated with their nanoscopic dimensions and are thus being extensively studied and appraised for their potential to reshape future electronic, photonic and sensing device applications. Of great significance, are nanowire (NW) synthesis techniques providing control over position, dimensions and quality of these nanostructures, enabling the fabrication of nanowire-based devices with reproducible and predictable performance. Specific to this work, both bottom-up and top-down approaches are developed to acquire position-controlled arrays of indium arsenide (InAs) NWs on silicon (Si) substrates. In the bottom-up approach, selective-area growth of InAs NWs is demonstrated using molecular beam epitaxy (MBE) on pre-patterned SiO_2-masked silicon substrates with (111) orientation. The patterning of the oxide mask is achieved via a cost-effective bottom-up technique, termed colloidal lithography, which relies on self-assembled colloidal particles on the surface to produce large scale templates with nanohole patterns. Effects of growth parameters and oxide mask quality on the NW growth are investigated. Furthermore, a theoretical growth model is developed to explain the size scaling behavior of NWs as a function of growth time, inter-wire spacing and growth temperature. This model calls attention to the presence of three growth regimes governing the NW growth kinetics depending on inter-wire distance. The top-down approach for the synthesis of in-plane NWs presented in this work relies on the patterning of high-quality epitaxial InAs thin films. The wires are obtained via wet chemical etching of InAs through a resist serving as an etch mask. The ordered NW arrays acquired are eventually transferred to a silicon substrate using an elastomeric stamp without loss of crystal orientation or arrangement.

Keywords: nanowires, molecular beam epitaxy , indium arsenide, bottom-up, selective-area epitaxy, catalyst-free, colloidal lithography, growth modelling, top-down

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I would like to first and foremost start by dedicating this thesis to my sister and parents for their endless love, support and encouragement. In life's wanderings, great sisters are the stairways that make the climb easier. I've been blessed with a sister who believed in me when I did not believe in myself, making me stronger. Unlike friends, who just listen to your problems, you make my problems your own, thank you for being an amazing sister.
As for my parents, these few words do not give justice to the sacrifices you made and the dreams you had to let go, just to give me a shot at achieving mine. Thank you for always leading by example, and for giving me the strength to believe in myself and encouraging me to always shoot for the stars. I am eternally grateful for your trust and faith in me. I hope I can manage to always make you proud.
I place on record, my sincere thank you to my supervisor Huan Zhao for the continuous encouragement as well as providing me the platform to innovate and experiment independently. I've learned so much during my work with you and for that I am very grateful.
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Ghada Badawy, Gothenburg, August 2016

Contents

1
Introduction

1.1 Background

The past 50 years have been witnessing an exponential progress in the power of electronics, as predicted by Moore's Law. In fact, Moore's prediction that the number of transistors in an integrated circuit would double roughly every two years, still holds and remains to be the guideline instructing the semiconductor industry [1]. Unlike Netwon's Law or Gauss's Law, Moore's Law is not a physical law that describes nature. Moore's Law was coined from obersvations based on the exponenetial increase of device densities during the inception days of integrated electronics [1]. The true insight provided by Moore's observations was the fundamental understanding of the economics governing the microelectronics industry [2]. As the number of transistors increased, each transistor became smaller, faster and cheaper, thus resulting in an unprecedented enhancement in performance [3]. The driver of the microelectronics revolution was not solely the shrinking of the transistor, but rather the declining transistor cost. Certainly, transistor footprint scaling makes the diminishing transistor cost possible, but this is only sustained so long as the increased complexity does not devalorize manufacturing yields [4]. Metal-oxide semicondcutor field effect transistors (MOSFETs), the workhorse of the semiconductor industry, constitute the building blocks of microprocessors, memory chips and telecommunications microcircuits [5]. To put things into perspective, a modern microprocessor can accomodate more than 2 billion MOSFETs, and a 32-gigabyte memory card weighing only 0.5 g holds an astounding 256 billion transistors, which is comparable to the number of stars in the Milky Way [5]. A unique feature of Si MOSFETS is enhanced logic properties with reduced transistor dimensions. More specifically, the decrease of MOSFET size over the years resulted in an exponential increase in their switching speed and density, whereas transistor energy decreased proportional to the decrease in size. Grievously, Si device scaling is gradually approaching its limits, threatening to stagger the micro- and nanoelectronics revolution.

Further scaling by traditional geometric miniaturization of the conventional planar silicon devices (see Fig. 1.1a) is facing physical limitations and technical challenges. These encompass, amongst others, immense leakage currents through the gate oxide, exponentially increasing source-drain leakage currents, carrier-mobility degradation in the channel due to increased electric fields in the continuously decreasing channel lengths, as well as increased variations in the fabricated devices [6]. Short channel effects illustrated in Fig. 1.1b, become more prominent as the channel length is further scaled down. They arise due to the electrical charges being shared between the transistor gate, on the one hand and the source and drain on the other. The source and drain junctions set up depletion regions that infiltrate the channel region from both sides of the gate, thus effectively shortening the channel length [5](see Fig. 1.1a). The penetration of these depletion regions into the channel weakens the gate control on the channel. Increasing the drain voltage further amplifies this effect, which results in the potential in the channel region and the eventual carrier concentration to be controlled not only by the gate electrode, but also by voltage applied to the drain and the source to drain distance. Loss of gate control on the channel leads to an increase in the leakage current of the transistor, thus impeding further MOSFET scaling [5].

The beneficial implications provided by the device miniaturization, such as enhanced performance per microprocessor due to the enormous number of transistors on a chip are incurring serious power density issues, thus resulting in 'power-constrained scaling' [7]. More specifically, the increase in power density is provoking severe packaging and cooling costs, which are gradually eroding the beneficial cost reduction of chips brought about by the transistor scaling. Reduction in

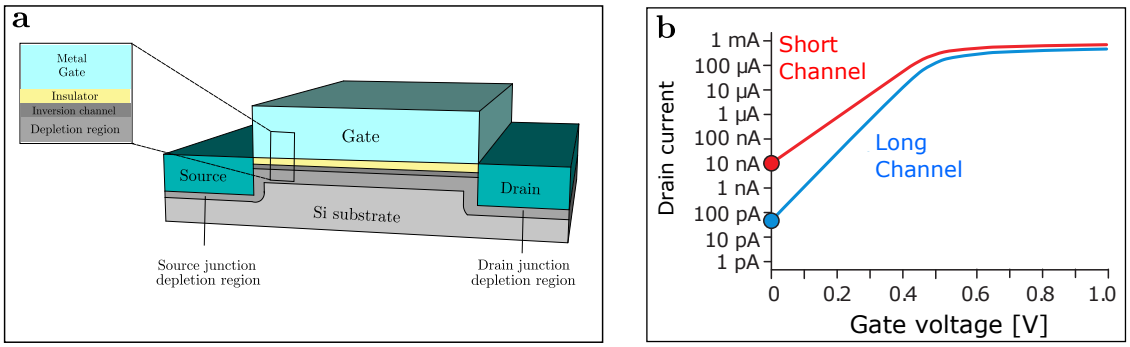

Figure 1.1: a. A schematic of a classical bulk MOSFET. The space between the source and drain is the channel length. A metal electrode together with an insulator compose the gate stack, which controls the electron flow in the channel. When a bias is applied to the gate, charge carriers from the source and drain are attracted to the gate, thus forming an inversion layer, referred to as the channel. Opposite charge carriers in the substrate are repelled by the gate voltage and end up being pushed into the source and drain regions, leaving behind carrier free regions , known as depletion regions. Adapted from [5]. b. Short channel effect. As the channel length is decreased, the sub-threshold slope is less steep, resulting in a slower variation of the current as the gate voltage is changed below the threshold voltage. As indicated with the coloured circles, the off-current is thus higher for short channels. Adopted from [5].

the operating voltage of transistors is necessary to alleviate problems associated with power density and to allow the continued progress of transistor densities on a chip. A reduction in the operating voltage however, compromises the switching speed. One viable solution is to use a material other than silicon, in which carriers are transported at much higher velocities, thus allowing a decrease in voltage without loss of speed and device performance.

In fact, to address the aforementioned challenges and limitations, various research breakthroughs and innovations have been proposed and are being developed to allow the sustainability of Moore's Law. Examples of these breakthrough technologies are summarized in Fig. 1.2 and include mechanically strained Si channels to improve charge carrier mobility, high-k (high dielectric constant) dielectric gate stacks and metal gate electrodes to allow for higher drive current without increasing the overall gate leakage. Though these technologies made significant advances in device scaling possible, the feasibility of further sustaining Moore's Law requires new transistor architectures as well as investigating new device materials. New device architectures necessitate a transition from the planar device structure to three-dimensional, multi-gate devices (see Fig. 1.2). One of the main advantages of these non-planar devices includes improved electrostatic gate control on the channel, thus diminishing short channel effects and allowing further scaling. Furthermore, much attention has been granted to non-silicon electronic materials for logic applications and their integration on the cost-effective Si platform. Amidst, the most investigated materials are $III-V$ compound semiconductors, such as gallium-arsenide (GaAs), indium-arsenide (InAs) and indium-phosphide (InP), combining materials from columns III and V of the periodic table. These materials have a superior list of attributes when compared to Si, as summarized in Table 1.1. As a matter of fact, $III-V$ semiconductors have intrinsically higher electron mobility as compared to silicon. InGaAs and InAs have 10 times higher electron mobility than Si at a comparable sheet density [4]. Generally, $III-Vs$ have lower carrier density than Si, because they have fewer density of states. Nevertheless, they possess a lower effective mass ($m^* \approx 0.023m_0$ for InAs), which results in higher carrier mobilites and injection velocities, thus it over compensates for their lower carrier density [8, 9]. Moreover, most $III-V$ materials have a direct bandgap, unlike Si and are therefore optimized for optoelectronic applications, such as lasers and light-emitting diodes [8, 9].

It is worth noting, that though $III-Vs$ seem to outperform Si in many aspects and applications, Si is anticipated to remain the preferred platform for most technology applications and future devices. The reasons for the former are manifold; the price of Si as compared to other materials is very attractive, it is available as large area wafers with high purity and crystal quality [11]. Fur-

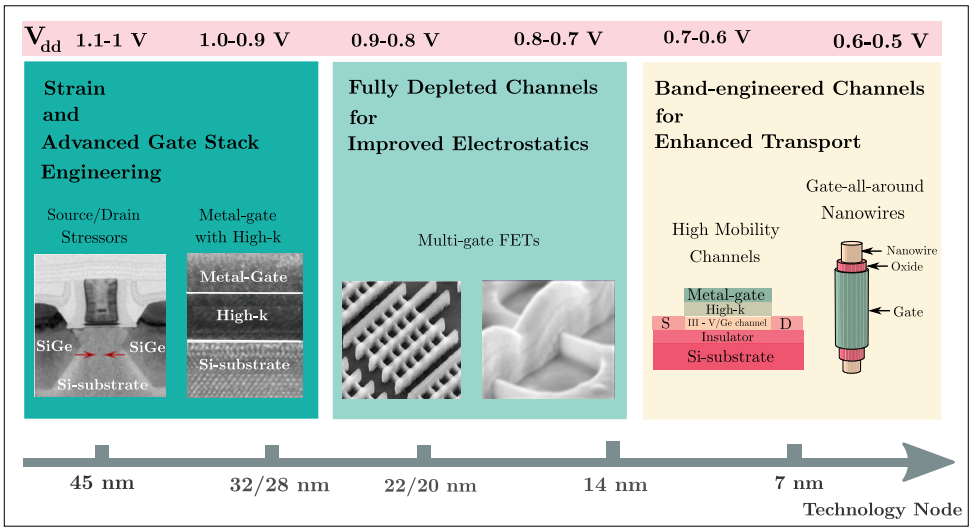

Figure 1.2: Current device technologies combining innovative tecnoligies, new device materials and architectures to enable continuous scaling. The top bar indicates possible voltage scaling for the different device technoliges, whereas the bottom bar indicates the transistor feature size, commonly referred to as the technology node, conceivable for the respective transistor technologies. Adapted from [10]

thermore, it exhibits mechanical stability and has a stable oxide (SiO_2). The enormous investments provided to the Si-technology, have stimulated extensive research for this material, rendering it extremely well-studied and characterized [11]. Accordingly, the prospect lies in integrating these superior materials on the mature Si platform, to combine the advantages of both material systems. In particular, $III-V$ nanowires (NWs) are of particular interest for achieving $III-V$ material integration on Si as they combine the benefits of non-planar devices as well as new channel materials. In what follows, the reader is guided through the challenges encountered during III-V integration on Si, as well as the opportunities provided by NWs for overcoming these challenges.

1.2 $III-V$ Materials Integration on Silicon

The monolithic integration of $III-Vs$ on Si is a sought after goal, however it remains a major challenge. The high defect density (10^6-10^6 cm^-2) encountered during the planar growth of these materials onto Si is a primary concern [12]. Defects originate due to a mismatch of lattice parameters as well as thermal expansion coefficients between the two material systems, as illustrated in Fig. 1.3b. A lattice mismatch signifies that the growing layer needs to adapt its own lattice constant to the lattice parameter of the underlying substrate by changing its native bondlengths

Table 1.1: Selected material properties comparing Si with $III-V$ materials. Values are for room temperature measurements

Properties	**Si**	**$III-V$-materials**
Bandgap (eV)	indirect ≈ 1.12	mostly direct, wide range, InAs: ≈ 0.36, AlN ≈ 6.02
Electron Mobility (cm^2/Vs)	1900	InAs: 20000, InSb: 78000
Hole Mobility (cm^2/Vs)	500	GaAs: 400
Wafer Cost with (111)-orientation (EUR/cm^2)	≈ 0.2 (4 inch)	≈ 8 (2 inch)

(pseudomorphic growth) [11]. This change causes the layer to be strained. In particular, as the layer grows thicker the energy accumulated in the strained layer increases to the extent that it becomes energetically more favourable for the growing crystal to form defects, by introducing mismatch dislocations to relieve the lattice strain [12]. The maximum thickness of a defect-free layer, also referred to as *critical layer thickness*, is dependent on the magnitude of the mismatch [13]. Similar to the lattice mismatch, a difference in thermal expansion coefficients stimulates defect formation. The growth of III − V semiconductors is typically performed at high temperatures, and during the cooling process to room temperature the thermal mismatch invokes further lattice strain yielding crystal defects. A third technology barrier encountered during III − V growth on Si are so-called anti-phase boundaries (APBs). APBs are a type of structural defects and occur when polar semiconductors are grown on top of non-polar semiconductors. Non-polar semiconductors consist of a single atom, unlike polar materials, which consist of two or more different elemental atoms. Basically, the Si crystal structure is composed of two face-centered-cubic (fcc) sublattices, in which Si atoms occupy both sublattices. In contrast, in the zinc blende crystal structure in which InAs crystallizes, In and As atoms reside in a sublattice each. Accordingly, as these atoms are deposited onto the non-polar Si surface there is an ambiguity as to which sublattice each atom should occupy. This ambiguity could result in two domains growing together, in which In atoms dwell in different sublattices, thereby creating a defective boundary containing In-In and As-As bonds (see Fig. 1.3a) [11, 14]. These defects degrade device performance, as they enhance carrier scattering. APBs specifically are charged defects and thus act as scattering centres for electrons [15].

The integration of III − V semiconductor nanowires (NWs) directly onto the mature Si platform has emerged as a viable route towards achieving monolithic integration, while circumventing the discussed defects. In fact, nanowire growth mitigates lattice and thermal mismatch restrictions due to a small contact area with the growth crystal. In contrast to planar structures which can only relax strain in one dimension, NWs are able to efficiently relax the accumulated strain in two dimensions due to their small lateral dimensions [16]. Furthermore, it is justifiably expected that the formation of anti-phase-domain boundaries will be inhibited in NWs, seeing as NW growth is considered to take place in a layer by layer fashion with a single nucleation event per layer [17], hence suppressing the formation of anti-phase domains. Accordingly, III − V NWs allow for high quality heterojunctions on Si with a low defect density, which is less feasible using conventional thin film epitaxy.

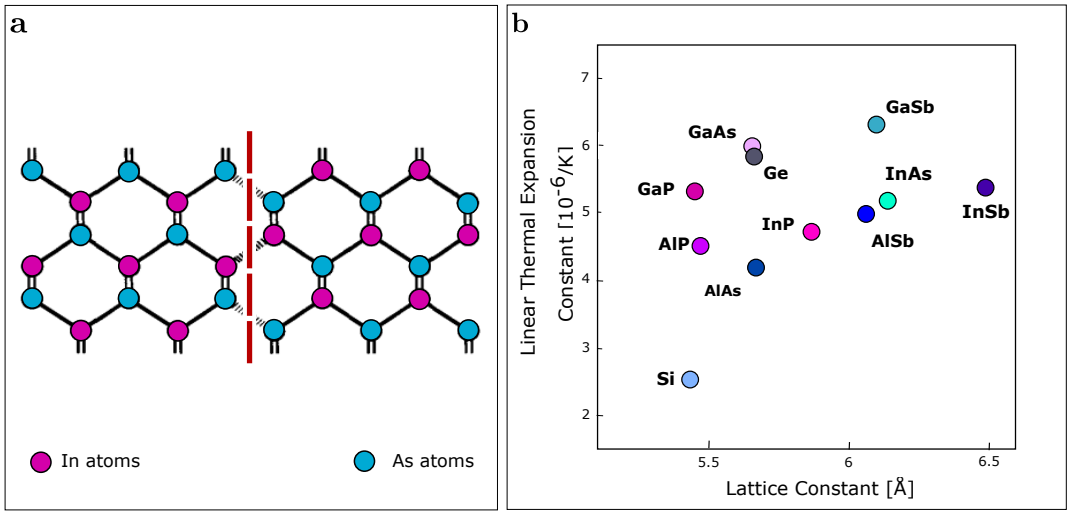

Figure 1.3: a. Anti-phase boundary formation. The different anti-phase domains are indicated by the dashed redline. APB is formed due to growth on an unmatched substrate, however the lattice mismatch is omitted for clarity. Adapted from [11]. b. Thermal expansion coefficients and lattice parameters for Si, Ge and selected III − V compound semiconductors. Based on [12].

1.3 III – V Semiconductor Nanowires

Nanowires are rod-shaped crystalline nanostrucutres possessing lateral dimensions as small as tens of nanometres (nm), whereas their axial dimensions are considerably elongated, typically in the micrometre (μm) range. III – V NWs are composed of stoichiometric quantities of materials from group – III and group – V elements in the periodic table. Owing to their small diameters, they can relax strain laterally, thus allowing for the axial stacking of profoundly lattice-mismatched materials [18] as well as sustain the seamless integration on Si [11]. In addition to these benefits, their small lateral dimensions enable the confinement of electrons in two dimensions, resulting in 1D ballistic transport [19] along their axis. Their capacity to confine carriers in two dimensions is the reason why NWs are sometimes referred to as 1D structures.

A wealth of interesting and novel phenomena are affiliated with nanometre-sized structures, such as NWs, including size-dependent absorption and emission [20], quantized or ballistic conductance [21] as well as Coulomb blockade [22]. Generally, quantum confinement of electrons in potential wells within nanoscaled structures is anticipated to cater powerful as well as versatile routes to control electrical, optical , magnetic and thermoelectric properties of semiconducting functional materials [23]. NWs in particular, are being extensively investigated due to their unique physical and geometrical attributes, e.g., different structural and optoelectronic properites from the corresponding bulk materials , thus making them viable candidates for future nanoscale devices. They represent good systems for studying the dependence of physcial properites, such as electrical, thermal or mechanical, on dimensionality and size reduction [23] as well as provide a platform for studying low-dimensional physics [24]. Furthermore, III – V have been considered for their use, among other things, in high performance electronics [25, 26], solar cells [27], light-emitting diodes (LEDs) [28], sensors [29, 30] and most recently for the study of Majorana fermions [31]. In contrast to planar structures, semiconductor NWs exhibit stronger coupling with light, which makes them efficient photon emitters and absorbers, consequently providing rich prospects for their application as light emitting diodes (LEDs) and solar cells [32]. NWs deemed to be very efficient in sensing applications. Their extremely high surface-to-volume ratios makes their electrical properties highly sensitive to species adsorbed on their surface, making them excellent candidates for chemical and medical sensing applications. In regards to electronics applications, NWs offer an idea geometry for field-effect transistors (FETs) with wrap-around gates for enhanced electrostatics, allowing for high speed, ultra-dense electronic chips [33].

Furthermore, nanowire heterostructures have emerged as a possibility to examine quantum mechanical phenomena and to combine a wide range of materials to possibly achieve a wide variety of applications, such as quantum information and computing devices. In particular, NWs allow for structural and compositional complexity. NW heterostructures accommodate abrupt interfaces and can lodge two structural configurations; axial and radial heterostructures. Axial heterostrucutres, in which the material composition is varied along the wire axis, allow for the local tuning of the bandgap along the NW length, thus paving the way to new alternatives for device optimizations, such as tunnel barrier structures [34]. Radial heterostructures appear in the form of core-shell structures, where the shell layer is used to cap the NW with a higher bandgap material to passivate or modulate doping, for instance. [34–36]. Tunnel field effect transistors (TFETs), which have recently emerged as true contenders to outperform the current MOSFET technology at low voltages and high performance, have been realized using III – V NW heterostructures [26, 37, 38].

In this regard, the focus of the work at hand is on InAs nanowires, due to several unique attributes associated with this material system. InAs in particular proved to be an attractive contender for NW-based devices due its high room temperature electron mobility ($\mu_e \approx 20000$ cm^2/Vs) predicated by its very small electron effective mass ($m^* \approx 0.023 m_0$) [9]. Furthermore, it exhibits high injection velocities as well as surface Fermi Level pinning in the conduction band [39], which results in the formation of an electron surface accumulation layer [40], providing low resistance Ohmic contacts [41]. Furhtermore, InAs can be combined with GaAs or aluminum antimonide (AlSb) to enable direct band gap tuning across a wide range of values, from 0.36 electron Volts (eV) to 1.42 eV, opening up a broad specturm of possibilites for photonic device appliations. In combination with Si, InAs displays profoundly high current densities by the virtue of steep source-channel p-n heterojunctions among both materials in comparison to other III – V/Si material combinations [42]. As a matter of fact, extraordinary prototype NW devices, such as photodetec-

tors [43], Esaki tunnel diodes [42], single-electron transistors [44] and high perfromance FETs [45] have been realized using InAs NWs.

Although NWs have been extensively studied over the past decade, further development towards practical ways to achieve large quantities of NWs from a diverse palette of materials at reasonably low cost and reduced complexity requires ingenuity and hence remains an active subject of debate and investigation. In particular, to be of real interest to the electronics industry, it is essential to solve issues related to their crystal quality and reproducibility as well as provide possibilities to achieve control over their position, direction and geometry [34].

1.4 Nanowire Synthesis

Nanowire growth was first reported in 1964 when Wagner and Ellis announced their novel vapour-liquid-solid (VLS) mechanism for growing elongated, rod-shaped crystals, commonly known back then as 'nanowhiskers' [48]. In fact, Wagner and Ellis were able to successfully synthesize Si whiskers with diameters in the range of 100 nm using liquid gold droplets as catalysts. The key feature of their mechanism relies on the promotion of anisotropic crystal growth employing a metal nanoparticle as a catalyst [46]. In the VLS-mechanism (see Fig. 1.4), as the name suggests, three phases are included in nanowire growth. Through heating of the metal nanoparticles on the growth substrate, an alloy is formed with the substrate material and the vapor components in the gas phase [49]. Formation of this eutectic mixture turns the metal nanoparticle into a liquid, as predicted by phase diagrams of material systems [50]. As a consequence, the liquid droplet acts as a preferred sink for incoming precursors from the gas phase [51]. Continuous supply of vapor phase materials to the droplet causes it to saturate, until it reaches supersaturation, thus driving the precipitation of component materials at the liquid-solid interface to minimize the energy of the alloy system [50]. Precipitated atoms from the supersaturated droplet form bonds at the liquid-solid interface, thus initiating crystal nucleation at the droplet-substrate interface. The solid nucleated crystal grows layer-by-layer causing the metal droplet to be lifted and yielding an elongated crystal (nanowire) with lateral dimensions as big as the droplet diameter.

This growth mechanism, is a typical example of so-called 'bottom-up' processes, in which structures are self-assembled or organized from their constituent components in an additive fashion [52]. For NW growth employing the VLS mode, the nanoscale diameter is already defined during the growth process and can be regulated with nearly atomic-scale precision. This efficient control over the structure dimensions, size and chemical composition goes far beyond what is achievable in 'top-down' lithography techniques. In contrast to bottom-up techniques, top-down fabrication relies on carving or etching structures from a large piece of material in a subtractive manner.

To date, the majority of $III-V$ NWs are synthesized using bottom-up fabrication techniques,

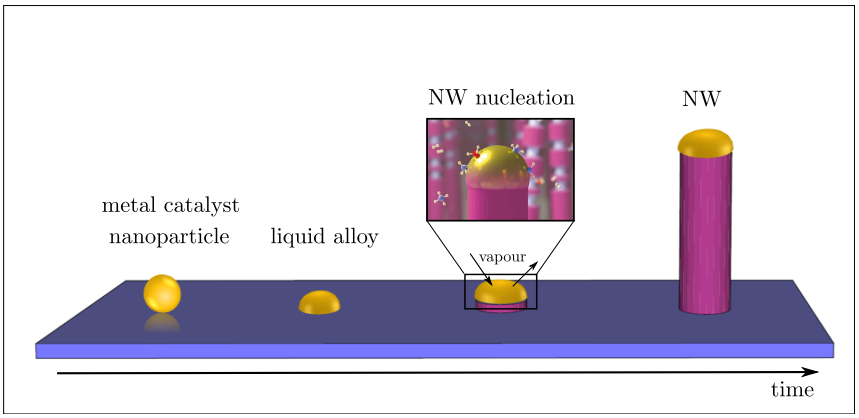

Figure 1.4: Schematic illustration of the vapor-liquid-solid growth mechanism of nanowires, indicating the different stages of growth, including alloying and nucleation and eventual nanowire growth, from [46]. The inset illustrates the liquid droplet acting as a preferred deposition site for vapour molecules, adapted from [47].

more specifically utilizing the well-established VLS mechanism using a range of growth techniques, amongst others, metal-organic vapor phase epitaxy (MOVPE) [53, 54], chemical beam epitaxy (CBE) [55, 56] or molecular beam epitaxy (MBE) [57, 58]. Adopting the VLS growth mode, entails the dependence on a catalyst. In fact, conventional nucleation mechanisms which rely on foreign catalysts, such as gold (Au) or nickel (Ni), could lead to inadvertent catalyst incorporation within the growing wire. Grievously, for specific material combinations, the incorporation of the foreign catalysts within the wires could possibly obscure carrier profiles, thus degrading device quality and performance [59]. Gold specifically in combination with Si is known to introduce deep level traps in the semiconductor bandgap, thus regressing the proficiency of functional $III-V$-based devices on silicon [60]. In order to mitigate the metal contamination, much effort has been directed towards self-induced VLS growth mechansims, which rely on self-catalytic droplets composed of the group-III element. Although this self-catalysed technique deems promising, and has been realized on many growth substrates with high growth rates [61], it is not free of shortcomings. In fact, serious limitations correlated with this growth technique remain a concern, including unpremeditated NW kinking and tapering as well as non-uniform composition profiles along the synthesized NWs due to droplet consumption during growth [62–65].

These challenges have stimulated further research to investigate the feasibility of synthesizing catalyst-free $III-V$ NWs. Lately, non-catalytic $III-V$ NW growth has been reported to primarily depend on facet-driven selective-area epitaxy (SAE) on dielectric masks-templated substrates [66, 67]. Apart from mitigating the deficiencies of the catalysed growth techniques, SAE with patterned masks achieves position-controlled and aligned NWs, thus facilitating subsequent device fabrication steps. Even though this catalyst-free growth approach provides many advantages and opens a new channel towards NW device fabrication and analysis, it has been granted less attention compared to the VLS NW growth mechanisms. In fact, few studies have focused on SAE in MBE systems specifically.

1.5 Thesis Outline

The objective of this thesis is to achieve a NW synthesis technique that provides control over NW position, growth dimensions and quality while minimizing fabrication cost and complexity with the intention to facilitate subsequent device fabrication steps. On that account, this work focuses on acquiring fundamental knowledge over the catalyst-free growth of InAs NWs on Si by molecular beam epitaxy. This encompasses the understanding of the growth kinetics driving NW growth via a theoretical growth model as well as outlining the dependence of NW dimensions and geometry on substrate preparation and growth window (growth temperature, In-flux, and dielectric mask quality) for achieving NWs with optimized properties and geometries. To further explore methods associated with achieving device fabrication-compatible NWs, a top-down approach for fabricating horizontally aligned InAs NWs on Si utilizing an epitaxy lift-off technique is presented and discussed.

This thesis is organized in six chapters. An introduction to the MBE system and its two main real-time monitoring techniques, particularly reflection-high energy diffraction an quadrupole mass spectrometry, are provided in chapter 2. Chapter 3 discusses the techniques used for sample patterning and substrate preparation prior to NW growth, while outlining their strengths and limitations. A growth parameter study of the bottom-up synthesis of InAs NWs in an MBE system via catalyst-free selective-area epitaxy is also presented. In Chapter 4, a theoretical growth model describing the growth kinetics of position-controlled selective-area epitaxy in MBE systems is derived and discussed. Chapter 5 presents a top-down approach for fabricating horizontally aligned epitaxial InAs NWs utilizing epitaxy lift-off. A conclusion together with a brief outlook on the field are presented in Chapter 6.

2

Molecular Beam Epitaxy

This chapter discusses the experimental growth technique, Molecular Beam Epitaxy (MBE), used for the epitaxial growth of different materials and material structures. First, an overview of the MBE working principle will be presented, followed by an introduction of the solid-source MBE system used in the work at hand. Moreover, an outline of the *in-situ* growth monitoring techniques is provided, where their main capabilities and limitations are discussed.

2.1 The Molecular Beam Epitaxy System

Molecular beam epitaxy is a process used to grow epitaxial structures of different materials, ranging from oxides to semiconductors to metals. The focus is mainly on compound semiconductors, in large part, due to their high technological value to the electronics industry. In this process, non-interacting beams of atoms or molecules of constituent materials are evaporated or sublimed to strike a heated crystal substrate in an ultra-high vacuum (UHV) environment, in the range of 10^{-9} Torr, thus producing high purity material structures. The beams do not interact in the gas phase since their mean free paths are considerably longer than the typical 20 - 30 cm source-to-substrate distance supported by the UHV environment [68], thus producing a 'molecular flow' of beams. The long mean free paths, inherent to the UHV conditions, additionally result in directional beams, implying that no carrier gas is required, unlike other growth techniques, such as metal-organic vapor phase epitaxy (MOVPE) [69]. These molecular beams contain the molecules or atoms necessary to constitute the composition of the growing structure. Incorporation of the incoming atoms into the growing structures takes place via exchange processes with the substrate atoms, attachment to atomic steps or nucleation of growth islands and subsequent attachment of adatoms to these islands. Surface diffusion is essential to the latter two processes, where the growth temperature has to be sufficiently high to ensure that the adatoms can thermally overcome the surface diffusion energy barrier for them to efficiently reach lattice sites and be incorporated. Accordingly, the arriving atoms form a single crystalline layer in registry with the underlying substrate, i.e. an epitaxial film [70]. The word *epitaxy* has its origin from the Greek words *epi* denoting 'on top of' and *taxis* denoting 'ordered arrangement' [71]. Epitaxial films of semiconductors have been playing a fundamental role in device processing because they allow the fabrication of specialized devices and device structures. The invention of the transistor together with the economic importance of the semiconductor hype have stirred research in the science of materials and propelled the development of a variety of methods to grow semiconductor crystals.

Molecular beam epitaxy was initially developed by J.R. Arthur and A.Y.Cho for the growth of GaAs and GaAs/AlGaAs structures [72]. The technique has successively been expanded to encompass an ever increasing variety of materials while maintaining crucial benefits over other methods developed for epitaxial film growth such as chemical vapor deposition (CVD) [73], liquid phase epitaxy (LPE) [74], and other associated techniques [75–80]. In contrast to the aforementioned growth techniques, MBE growth is achieved far from thermodynamic equilibrium conditions and is essentially governed by the surface kinetics arising when the incoming beams react with the peripheral atomic layers of the growth crystal. Other growth techniques proceed under nearly thermodynamic equilibrium conditions and are thus governed by diffusion processes taking place during the crystallizing phase encircling the substrate [81]. Key benefits of MBE growth as compared to other growth techniques include the accurate control of material growth to achieve structures with atomic monolayer precision, extremely low background impurity levels in the grown struc-

Table 2.1: Comparison of epitaxial growth techniques

Growth Parameters	**MOVPE**	**MBE**
Growth pressure (Torr)	~ 15	$\sim 10^{-9}$
Growth rate (μm/h)	~ 10	~ 1
Growth temperature (°C)	~ 750	~ 550
Thickness control (Å)	~ 25	~ 5
Interface width (Å)	< 10	< 5
Characteristics	carrier gas required (typically H) to transport reactants across the substrate	directional beams, no carrier gas required

tures, yielding high purity materials predicated by the UHV conditions, as well as the ability to scrutinize the growth process in real-time. The atomic scale control conceivable in MBE systems is mainly achieved by fast response mechanical shutters in front of the beam sources. These shutters interpose the beam fluxes almost immediately, i.e., initiation and termination of the deposition and doping is much faster than the growth of an atomic monolayer of material, thus enabling atomic scale precision. In addition to the accurate control over the beam fluxes, the growth rate of usually 1 μm/h (1 monolayer/s) is low enough to ensure surface migration of the incoming species on the growth substrate. Thus, the surface of the grown films is nearly atomically smooth [81]. In fact, these distinctive attributes provide the possibility to grow high purity structure and more importantly grant the ability to very abruptly alter the composition of the incoming stream of atoms, thus yielding structures with sharp interfaces on an atomic scale. Table 2.1, which is adjusted from [69] and [82] , summarizes the main differences between two of the main epitaxial technologies used for the growth of semiconductor structures, molecular beam epitaxy and metal-organic vapour phase epitaxy (also referred to as metal-organic chemical vapour deposition), for a gallium arsenide epitaxial process.

The system shown in Fig. 2.1a is a topview schemcatic of the solid source Riber Compact C21 – TE MBE system used for all growth experiments reported in the work at hand. The different components of the system are indicated on top of each system module respectively. Each system module is equipped with suitable pumping systems, to allow for independent pumping of each system compartment. In fact, the *pumping system* used to maintain the ultra-high vacuum

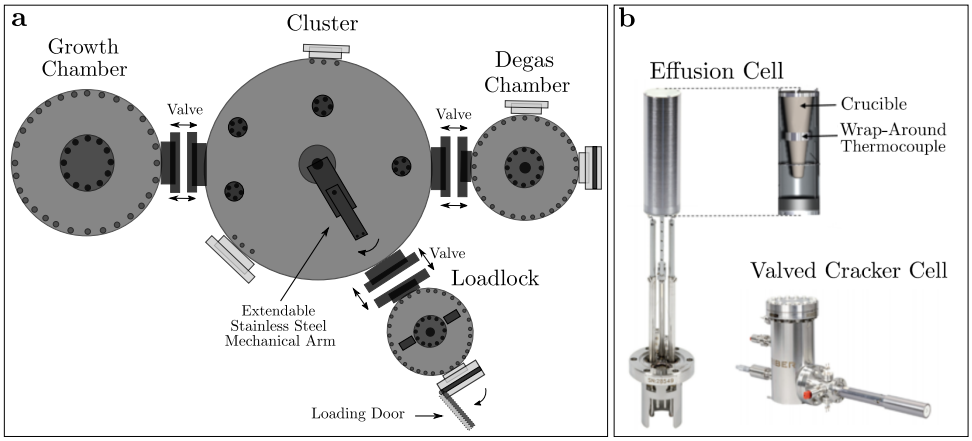

Figure 2.1: a. Topview schematic of the solid source Riber C21 – TE MBE used in all growth experiments performed in the work at hand. b. Effusion cell [83] with a cross-section of the top of the effuison cell [70], bottom right a valved cracker cell [84].

environment constitutes various pumping technologies including cryopumps, ion pumps, and turbomolecular pumps [68]. For instance, the growth chamber of the system under consideration is supplied with helium-operated cryopumps assissted by liquid nitrogen filled cryopanels to decrease residual gas species, thus ensuring an ultra-high vacuum environment with base pressures in the order of $10^{9} - 10^{-10}$ Torr as scruitinized by an ionization gauge. A *loading chamber* or a vacuum interlock is used to load one or more substrates to the system, prior to opening the valve to the rest of the system. Accordingly, only the small loading chamber is exposed to the atmospheric pressure environment, which significantly decreases the pumping time, diminishes the possibility of contamination and reduces the introduction of air load in the remaining chambers. Vacuum interlocked systems necessitate means for transferring substrates from the loading chamber to the other vacuum chambers. Sample transport between the different system modules is achieved via a stainless-steel mechanical arm, as illustrated in Fig. 2.1a. This arm is contained within the *cluster* and it ensures the selection of the desired sample from a stack of samples in the loading chamber, accurately moves it to the other chambers and docks it to a substrate holder present in the other system enclosures. The *degas chamber* serves as a preparation chamber prior to growth. It is equipped with provision for heating the samples before their introduction to the growth chamber; the heating is typically done at temperatures in the range between T = 300 – 400 °C in order to outgas the substrate and the holder preceding the growth chamber loading to maintain the cleanliness of the growth environment. The *growth chamber*, is where the most essential step of the process takes place . A schematic of a typical MBE growth chamber is depicted in Fig. 2.2, illustrating a substrate docked onto the substrate holder facing down and is heated from the backside to the desired growth temperature to ensure the diffusion of adsorbed molecular species on the sample surface and stimulate epitaxial growth. As indicated in the schematic, the substrate holder is rotated to promote growth uniformity across the growth substrate. Furthermore, the main source of pumping taking place during growth is the liquid nitrogen-flushed cryopanel surrounding the substrate holder and sample. These cryoshrouds capture materials which condense at liquid nitrogen temperatures and ensure their retention away from the growth front [68]. Additionally, they provide cooling to the system by dissipating heat originating from the hot substrate and hot material sources, thus bypassing any chance of crosstalk between the heated sources.

The effusion cells, pointed towards the heated sample provide the materials used during the growth process and are switched on and off by mechanical shutters interposing the molecular beams produced by the evaporation of materials, and thus prevent the beams from reaching the substrate. The materials in the Knudsen effusion cells are contained in crucibles and are thermally heated via tantalum (Ta) ribbons. The temperature of the cells is regulated by tungsten/rhenium (W/Re)

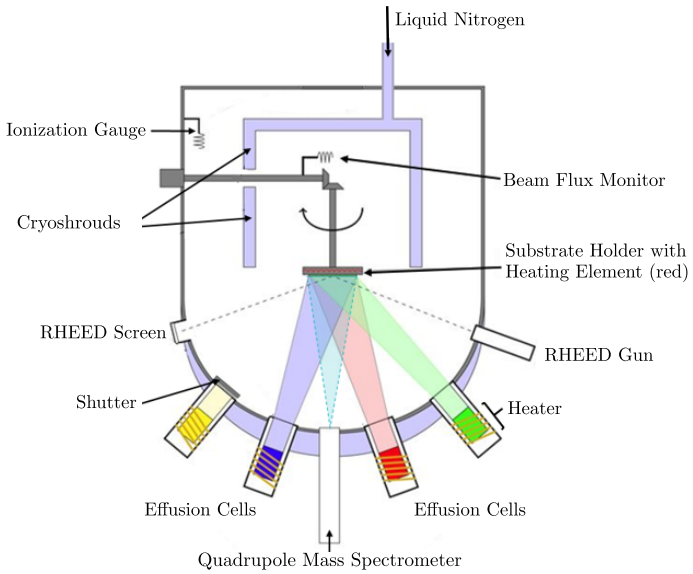

Figure 2.2: a. Schematic of a typical MBE growth chamber. Adjusted from the schematic in [85].

thermocouples located at the bottom or the side-wall of the cell [70]. These metals are chosen due to their compatibility with high temperatures and the corrossive environment of the MBE [86]. The MBE system under consideration has various types of source ovens depending on the temperature requirements to evaporate the different materials, including effusion cells, valved cracker cells and radio frequency (RF) plasma cells. Valved cracker cells shown in Fig. 2.1b are used for high vapour pressure group − V elements such as arsenic (As) and antimony (Sb). The use of cracker cells for group − V materials has been reported to demonstrate enhanced quality and reduced defects of epitaxial structures if the group-V material vapours usually composed of tetramers, e.g. As_4, are cracked into dimers (As_2) before their incorporation in the growing structures [70]. In contrast to effusion cells, where the flux is mainly controlled by the cell temperature, valved crakcer cells rely not only temperature but also on a precision valve to control the material flux. Group − III elements on the other hand, as indium (In) or gallium (Ga) are evaporated using effusion cells illustrated in Fig. 2.1b. The flux of atoms produced by the cells is measured by a beam flux monitor, which is simply an ionizing gauge yielding the beam equivalent pressure (BEP) for a corresponding cell temperature [68]. The flux of atoms is dependent on the source temperature T and the temperature-depedent vapour pressure $P(T)$ and is governed by the following equation [68, 87]:

$$J(T) = 1.118 \times 10^{22} \frac{A \times P(T)}{l^2 \sqrt{MT}} \tag{2.1}$$

where J is the flux, representing the number of atoms arriving into a given surface area per unit time, expressed in (atoms/cm$^2 \cdot$ s), A is the effusion cell orifice area, l is the source-to-substrate distance and M is the mass of the gas species of the evaporated material. Note, that the temperature dependence in the denominator is small compared with that of the vapour pressure (P(T)), thus the flux increases fundamentally exponentially with cell temperature [86]. Furthermore, the flux equation indicates that the beam flux is independent on the quantity of material in the cell. Eq. (2.1) implies that for a given temperature and vapour pressure, the beam flux scales with cell orifice area. Small effusion apertures limit the mass transfer of material, thus require higher cell temperatures, which gradually degrades the material quality. Nonetheless, the flux profile is significantly different for cells with large apertures and differs as the evaporated material depletes [86]. Accordingly, to achieve consistent beam uniformity, MBE machines are equipped with conical shaped crucibles, as shown in the cross-section of Fig. 2.1b.

Table 2.2, adapted from [71], displays the significant effect of pressure on the atomic flow of molecular species. Primarily, pressure affects the density of atomic species within a given volume, which in turn impacts their mean free path (λ). More specifically, an increased density of atomic species leads to an increased likelihood of collision and scattering, thus decreasing their mean free path. Additionally, pressure directly influences the flux (J), thus affecting the time, τ, required to acquire one monolayer of material, which fundamentally corresponds to the coverage of a flat surface with one atomic layer. The three pressure ranges presented in Table 2.2 correspond to atmospheric pressure, typical vapor pressure of source cells and usual background pressure of MBE growth chambers, respectively. The data displayed in Table 2.2 highlights the importance of UHV for achieving high epitaxial growth control and emphasizes the superiority of MBE growth with respect to other growth techniques for achieving high purity epitaxial structures.

The UHV environment of the MBE and the inherit limited spatial extension of the molecular beams has the superior advantage over other epitaxial growth techniques of allowing the inclusion of real-time growth monitoring techniques. Reflection high-energy electron diffraction (RHEED)

Table 2.2: Effect of pressure on atomic flow

Pressure [Torr]	**Density** [cm^{-3}]	$\boldsymbol{\lambda}$ [m]	**J** [atoms/cm^{2}s]	$\boldsymbol{\tau}$ [s]
760	2.5×10^{19}	10^{-7}	2.6×10^{22}	3.8×10^{-8}
10^{-6}	3.3×10^{10}	7.8×10^{1}	3.4×10^{13}	2.9×10^{1}
10^{-10}	3.3×10^{6}	7.8×10^{3}	3.4×10^{9}	2.9×10^{5}

and quadrupole mass spectrometers (QMS) are two of the main growth monitoring techniques used in typical MBE systems, which provide an insight on the nature of the structures during growth as well as allocate the calibration of growth rates.

2.2 Reflection High-Energy Electron Diffraction

RHEED is an extremely powerful *in-situ* method for the analysis of crystalline materials. This technique is commonly known from thin film MBE growth where it is typically utilized to determine growth rates as well as investigate the overall growth and morphological quality. The high senstivity of RHEED is attributed to the fact that it only samples very few atomic layers beneath the surface under study [88]. The underlying principle of RHEED, as depicted in Fig. 2.3a, relies on the scattering of electrons upon their impingement on a crystalline surface, where high-energy electrons are diffracted as postulated by kinematic and dynamic diffraction theories [88]. Basically, a RHEED gun, located in the growth chamber (see Fig. 2.2a) is operated at an acceleration voltage of about 10kV, generates an electron beam that strikes the growth substrate under a very flat angle ($\theta \approx 1 - 3°$). The electron beam is focused on the surface via a convoluted interplay of electric and magnetic fields. Subsequently, the electron beam impinges on a fluorescent RHEED screen, where intensity-modulated bright streaks are observed, as illustrated in the inset of Fig. 2.3a and Fig. 2.3b. Bright streaks are observed when incident electrons are scattered due to the periodic arrangement of atoms in the crystal lattice, thus producing a diffraction pattern on the RHEED screen. The condition for observing the streaks requires the difference between the incident and diffracted electron wave vectors to be equal to the reciprocal lattice vector ($\vec{k}_i - \vec{k}_o = \vec{G}$) [88]. The shape of the streaks indicates the surface roughness. More specifically, rough surfaces exhibit spotty features, whereas smooth surfaces yield diffraction patterns composed of elongated streaks [89].

2.3 Quadrupole Mass Spectrometer

Quadrupole mass spectrometery is commonly used to monitor residual gases, such as hydrogen or water vapor, contained within the UHV environment of the growth chamber of the MBE system. QMS is additionally used for leak detection or to quantitatively determine the desorbing species from the growth substrate in the surface reflected beam, as illustrated in the schematic in Fig. 2.4a. As the name indicates, QMS analysers are composed of *four* rods, which generate an electric field. Each opposing rod pair is connected to an RF voltage source with a DC voltage offset. The basic principle of a QMS relies on the stability of the trajectories of ions in oscillating electric fields. More specifically, only ions with a specific mass-to-charge ratio (m/z) travelling in the quadrupole electric field with a given voltage ratio, will be able to reach the QMS detector. Accordingly, other ions, with different m/z ratios will exhibit unstable trajectories, thus resulting in their collision with the rods and their restraint from accessing the detector. Correspondingly, by varying the applied voltage, the detector is able to scan the different molecules present in the UHV environment [92]. A typical mass spectrum is depicted in Fig. 2.4b, and implies that the residual gases in this vacuum environment are hydrogen, water and nitrogen molecules. It is worth noting that the presence of nitrogen in the vacuum of the growth chamber indicates a nitrogen leak, probably originating from the liquid nitrogen filling the cryoshrouds. Furthermore, hydrogen and water molecules are usually present in the UHV with negligibly low partial pressures, usually in the range of 10^{-12} Torr, as measured by the mass spectrometer of the MBE system used in this thesis.

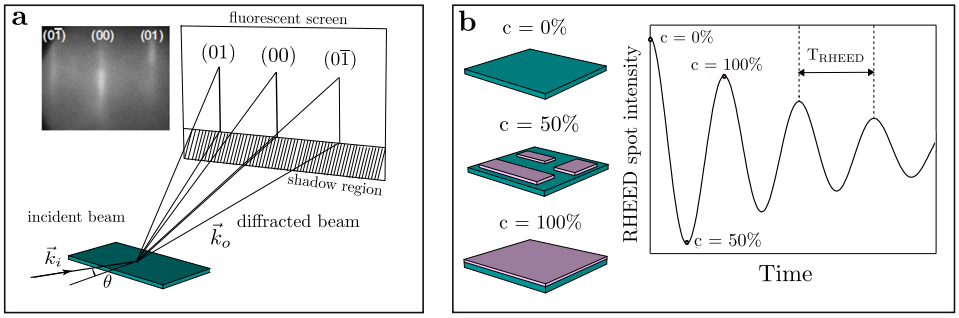

Figure 2.3: a. Schematic diagram of the key principle of an in-situ RHEED measurement, showing the incident electron beam at a flat angle θ to the substrate surface. The diffraction of the incoming beam produces intensity-modulated streaks, which is visualized on a fluorescent screen. Adapted from [89].The inset illustrates the diffraction pattern of a Si(111) surface as obtained from a RHEED measurement, showing typical zero and first order streaks (from [90]). b. Schematic illustration of thin film layer formation during epitaxial MBE growth over different time intervals, showing various fractional layer coverage, c, given in percent. The typical RHEED oscillation plotted over time is observed giving varying intensity according to different layer coverage. As indicated in the oscillatory graph, one RHEED period (T_{RHEED}) corresponds to the growth of one monolayer, which corresponds to coverage of a flat surface by one atomic layer [91]. Adapted from [90, 91].

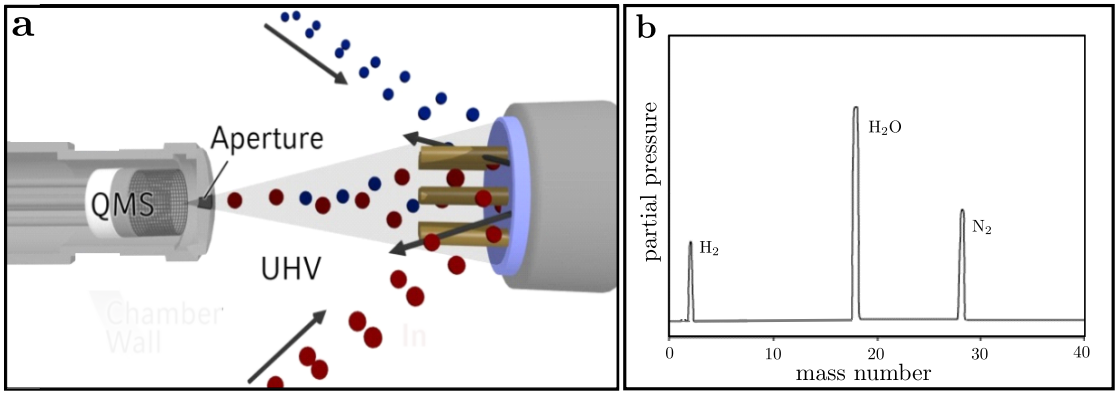

Figure 2.4: a. Schematic of a quantitative in-situ line-of-sight quadrupole mass spectrometer during nanowire growth, demonstrating incoming and reflected beams due to desorbing atoms from the growth substrate, adapted from [90]. b. Typical mass spectrum indicating the partial pressures of the residual gases present in the UHV environment, modified based on [93].

3

Bottom-up Synthesis of Positioned Catalyst-Free InAs NWs on Si

In this chapter, positioned, catalyst-free growth of InAs nanowires on lithographically patterned silicon-dioxide- (SiO_2)-masked silicon substrates is presented. The first part of this chapter, discusses the substrate patterning process via colloidal lithography (CL) and hole-mask colloidal lithography (HCL), as well as introduces the basic concepts of these techniques. Furthermore, the influence of the patterned mask quality and substrate processing steps on nanowire growth is investigated. The second part of this chapter focuses on the MBE growth of catalyst-free InAs nanowires on pre-patterned Si(111) substrates. The defined pattern provides nucleation sites for the incoming molecules to nucleate and grow, yielding nanowires. The size-scaling behavior and morphology of the synthesized nanowires as a function of growth temperature, In growth rate and V/III ratio are discussed.

3.1 Substrate Patterning for Positioned InAs NWs on Si

3.1.1 Colloidal Lithography

To date, the fabrication of structures where both the structure dimensions and ordering can be controlled at the nanoscale are of significance to the fabrication of nanoscopic systems with the intent of pursuing the novel properties affiliated with their nanometre dimensions [94]. Conventionally, such structures are obtained by direct writing techniques, such as electron-beam (e-beam) lithography. However, such fabrication methods require complex, expensive and in most cases, sophisticated machinery to be able to generate the energetic particles used to write the desired patterns. In this regard, these tools are slow and have low throughput, thus are only suitable for patterning very small areas [95]. Furthermore, e-beam lithography for instance, which is considered as one of the high resolution direct writing techniques, lacks the flexibility to scale down the feature sizes below 50 nm due to fundamental physical limits. These limitations arise due to, amongst others, electron scattering, e-beam spot size and secondary-electron range [96].

An alternative strategy exploits colloidal particles (nanometre-sized) as masks for etching or deposition to create two-dimensional (2D) fabrication patterns. This process is commonly referred to as colloidal lithography (CL) and benefits form being a large area (few cm^2), robust, parallel and cost-effective lithography method providing the possibility to scale down the critical dimensions below 100 nm [95]. In particular, this bottom-up lithography technique relies on the lateral *self-assembly* of colloidal spheres on surfaces without the aid of pre-defined templates to pattern large-scale planar arrays of nanosized structures. This self-assembled colloidal monoalyer is subsequently used as etch and/or deposition masks. [97]. The particles are eventually lift-off yielding different nanostructures and nanoarchitectures. Specific to this work, the charged nanoparticles were used as an evaporation mask to define nanohole patterns in SiO_2 layers on (111)-oriented Si substrates. Accordingly, the nanoholes were essentially defined by the size of the colloidal particles. The details of the fabrication process, tools and materials presented in this chapter are reported in Appendix A.

The basic fabrication steps for creating nanoapertures on SiO_2-masked Si substrates are illustrated in Fig. 3.1. The substrates used for the patterning and subsequent growth of InAs nanowires are commercially available single-side polished 2-inch Si(111) wafers. These wafers were diced into

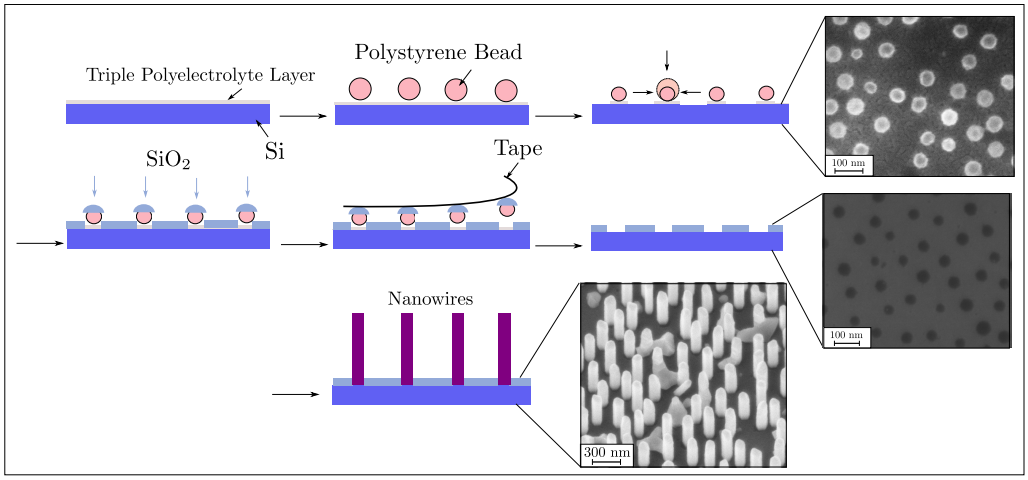

Figure 3.1: A schematic denoting the different fabrication steps for the nanohole template pattern using colloidal lithography, where the horizontal arrows denote the chronological order of the described process: the process starts with the surface charging of the Si(111) substrate with the triple polyelectrolyte suspensions, next, the PS beads are drop-cast on the Si surface, where they self-assemble due to electrostatic interactions, the particle size is reduced via exposure to oxygen plasma, which in-evidently partly removes the exposed charged polymer layers, the particle pattern is used as an SiO evaporation mask, the beads are tape stripped, leaving behind a nanoaperture patterned SiO film, selective-area epitaxy of NWs proceeds through the pattern openings. The SEM insets illustrate the results of the key fabrication steps and the SAE NW growth.

4 quarters to comply with the sample holder size of the MBE system. Subsequently, the wafer quarters were exposed to oxygen plasma for one minute, to enhance surface hydrophilicity [97]. In fact, oxygen plasma treatment of Si surfaces introduces polar functional groups, mostly silanol groups (SiOH), which renders the surface less hydrophobic [98]. This step is performed directly before the initiation of the colloidal lithography process, seeing as Si surfaces, like other material surfaces undergo hydrophobic recovery within minutes, depending on subsequent processing steps, induced by the reorientation of the silanol groups or their condensation [98]. In order to deposit the negatively charged colloidal particles on the Si substrate, the surface charge needs to be inverted, seeing as the silanol groups yield a negatively charged surface, which would repel the colloidal particles. The charge inversion is achieved by depositing water-suspended polyelectolytes on the substrate surface in a layer-by-layer fashion [17]. The positively charged (polycation) polydiallyldimethylammonium (PDDA) suspension is drop-cast on the surface to form the first charged layer. The charged molecule components within the PDDA solution are attracted by the negatively charged sialnol groups, hence form a charged layer. Particularly, as more and more suspended particles deposit on the substrate surface, thus inducing a surface charge inversion, non-adsorbed particles will no longer be attracted by the surface, in contrast they will be repelled. This repulsion will ensure that only very thin layers are formed. Once the layer is adsorbed, the substrate is rinsed with deionized water to remove any excess or loosely bound particles from the surface. The rinsing step is essential to guarantee the formation of a monolayer of surface charge rather than multi-layers, as it only allows strongly attached particles to remain on the surface [17]. The rinsing is followed by a nitrogen gas flow to dry the substrate. Next, a negatively charged (polyanion) suspension of poly(sodium $4-$styrenesulfonate) (PSS) is pipetted on the now positively charged Si substrate surface. The negatively charged particles contained in the PSS solution will assemble onto the surface equivalent to the previous step. Following this deposition, the sample will be analogously rinsed and dried. The final step before the colloidal particle deposition necessitates a further charge inversion step to acquire a positively charged surface, to ensure the self-assembly of the colloidal nanoparticles. Accordingly, PDDA is once again pipetted on the negatively charged surface in analogy to the preceding steps to yield a positively charged surface layer. The charged multi-layers ensure a uniform surface charge, in contrast to relying on only one PDDA monolayer to induce the adsorption of the colloidal nanoparticles. The charged multi-layers are a few nanometres thick

as reported in literature [97]. Following the surface charge inversion by the polycation/polyanion suspensions, the deposition of a colloidal suspension containing polystyrene (PS) beads is achieved via pipetting. The beads form a short-range order on the sample surface induced by the electrostatic interactions, as previously mentioned. The substrate is rinsed with deionized water to expel loosely attached beads from the surface. Ultimately, an intense nitrogen gas flow is applied to expunge the colloidal solution to avoid the reorganization of the colloids via hydrodynamic or capillary interactions during the evaporation of the liquid [97, 99]. All experiments reported in this work employed PS beads with an average diameter of 100 nm as reported by the supplier.

Before proceeding to subsequent fabrication steps, the PS-beads-functionalized substrates are exposed to oxygen plasma for a duration of 30 seconds. This oxygen plasma treatment step leads to the etching of the exposed regions of the charged multi-layers as well as the reduction of the PS beads' size, resulting in an effective increase in the inter-particle distance, as depicted in Fig. 3.1. In fact, increasing the plasma treatment duration yields smaller sized beads, due to longer etching. This step, thus paves the way towards achieving patterns with differently sized nanoapertures, providing flexibility in mask fabrication with minimized complexity, and goes beyond the minimum features sizes achieved with top-down lithography techniques. This etching process is achieved via energetic oxygen molecules contained within the plasma. These molecules induce the decomposition of polymer containing material by inserting radicals into the polymer chain backbone followed by chain scission, resulting in the removal of material (etching) [100]. The size of the beads at this stage defines the nanoaperture size within the SiO_2 mask. In this regard, the PS beads are used as an evaporation mask. More specifically, a 24nm-thick SiO_2 film is evaporated from vitreous quartz pieces from a tantalum crucible via a 4 kW (kilo Watt) electron gun. The evaporation is performed under vacuum (Pressure $< 10^{-5}$ mbar) conditions to ensure film purity. The poor step and side-wall coverage associated with the low energy particles contributing to the evaporation process as well as the directional film deposition affiliated with evaporation methods [101], allow for the creation of the off-cut profile illustrated in Fig. 3.2. It is noteworthy, that this off-cut profile is also possible via the regulation of the evaporated film thickness. More specifically, if the evaporated film thickness is comparable to the bead dimensions, the evaporated film will fully submerge the beads, thus eliminating the off-cut profile as indicated in Fig. 3.2. This off-cut profile is essential to the following lift-off step of the beads. In fact, following the thin film evaporation, the PS beads are lift-off via sticky-tape stripping, mainly enabled by the off-cut profile, resulting in a thin film with nano-holes arranged in a pattern determined by the self-assembled colloidal particles. The SiO_2-masked Si substrates are exposed one last time to oxygen plasma for one minute to remove any residual charged polymer layers that were inaccessible during the bead shrinking step. Finally, SiO_2 patterned Si samples are dipped into a diluted buffered hydrofluoric acid (BHF) solution to remove any contaminants as well as the native oxide [102]. The native oxide removal reduces the mask thickness, resulting in a 17 nm-thick patterned oxide layer. The BHF ($HF:NH_4F:H_2O$) etches the native SiO_2 on the Si surface and the hydrogen (H) atoms contained in this acidic etchant terminate the dangling bonds on the Si surface (passivation), thereby preventing the re-oxidation of the Si surface for a couple of hours even when exposed to air under ambient conditions [102, 103]. Accordingly, immediately after (within 20 minutes) this etching step, the prepared samples are loaded into the UHV environment of the MBE system for nanowire growth. The effect of the native oxide on the nanowire growth yield will be further elucidated in section 3.2. As presented in the (scanning electron microscope) SEM image of Fig. 3.1, the nanowires nucleate and grow preferentially within defined openings, where they have access to the crystalline silicon surface, thus exhibit *selective-area* growth on the substrate. The mechanisms of selective-area growth will be discussed in further detail in section 3.2.

3.1.1.1 Effects of Mask Quality

As aforementioned, the transfer of the short-range arrangement of PS beads onto the Si substrate is achieved via thin film evaporation of SiO_2. Grievously, the quality of evaporated silicon-dioxide is inferior in comparison to other silicon-dioxide films achieved via different thin film deposition technniques, such as sputtering or plasma-enhanced chemical vapor deposition (PECVD) [101]. Nevertheless, these thin film deposition techniques are not fit for the particle lift-off process, as they exhibit good step-coverage and side-wall coverage, thus entraping the beads within the deposited

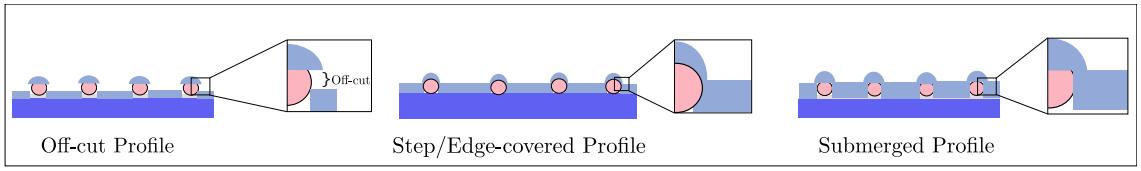

Figure 3.2: Schematic illustration of the different mask profiles due to difference in deposition technique or deposited film thickness. The 'off-cut profile' is produced by evaporation of SiO_2 while maintaining an evaporated film thickness less than the average bead diameter. The 'step/edge profile' is produced by non-directional beam deposition techniques such as sputtering or PECVD and impedes the particle lift-off with tape. The 'submerged' profile is produced via evaporation, however the deposited film thickness is in the order of the bead size, causing the particles to be fully submerged, not allowing their subsequent lift-off.

films [101], as schematically illustrated in Fig. 3.2. The inferiority of the evaporated oxide is manifested in its porosity [104]. In fact effects of the porosity of the oxide layer become more prominent after the BHF etching step. In particular, these pores induce unequal etching rates across the silicon-dioxide films, resulting in an increased surface roughness as well as much higher etch rates with respect to thermally grown oxides [105]. An increased surface roughness, as well as the presence of pinholes within the evaporated film serve as additional nucleation sites for nanowires and parasitic clusters. It is noteworthy, that nucleation of polycrystalline clusters and nanowires outside the defined nanoholes is enhanced for lower growth temperatures, as indicated in the SEM micrograph of Fig. 3.3a. In fact, in the MBE growth process, lower growth temperatures,

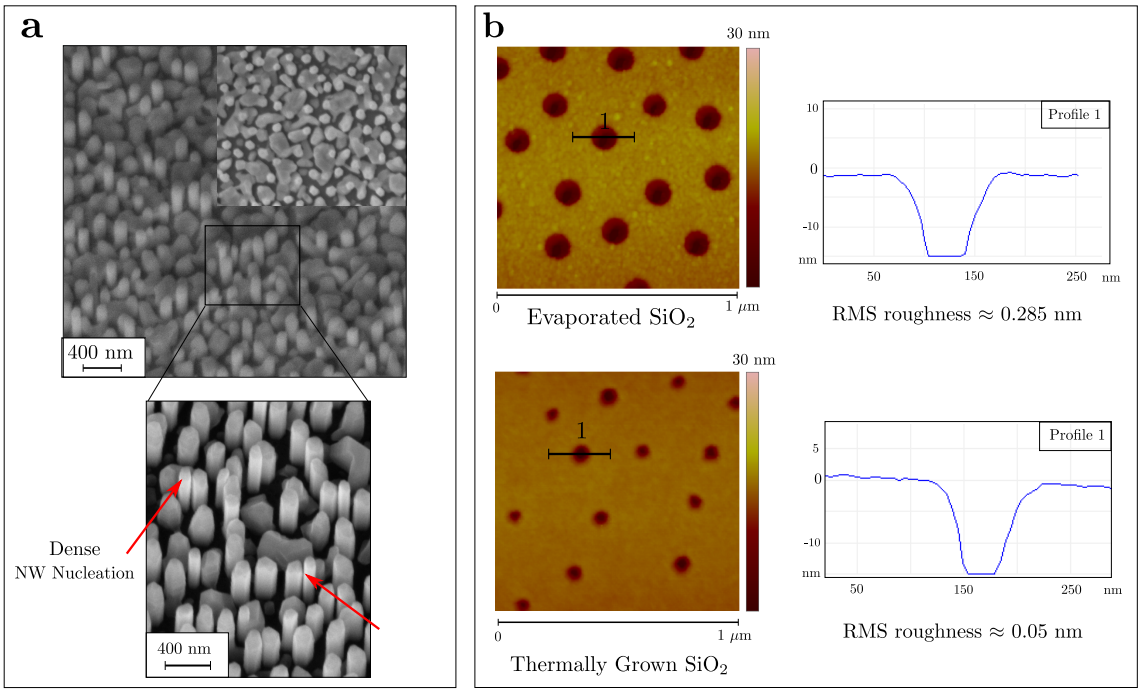

Figure 3.3: a. 30 degree tilted SEM image showing selective-area growth of NWs a on patterned *evaporated* oxide-masked Si substrate. The image indicates a high density of clusters. The inset shows a top view, where also a high density of clusters is observed. NWs have a hexagonal cross-section and are therefore clearly recognized with respect to the clusters. A zoomed-in SEM image indicates closely positioned NWs (red arrow), where NW nucleation is not limited to the pattern-openings. b. Atomic force microscopy (AFM) surface scans with a profile scan across a selected nanohole, of the obtained nanoaperture patterns in evaporated and thermal oxide. The RMS value given for each oxide mask indicates a higher surface roughness for the evaporated oxide.

yield higher sticking coefficients of adatoms on the SiO_2 surface as well as result in rather short diffusion lengths of incoming adatoms, thus facilitating their capture by nucleation centres present on the oxide mask surface [106]. In contrast, higher growth temperatures result in reduced sticking coefficients and longer adatom diffusion lengths, thus impeding their capture by rough edges and pinholes on the oxide mask, and suppressing cluster formation on the oxide surface [106].

One alternative to circumventing issues associated with the oxide mask quality is to use Si substrates with high-quality thermally grown silicon-dioxide. Thermal oxide is known to have much smoother surfaces, in addition to being free of pores and pinholes and thus is expected to show reduced clusters and suppress nanowire nucleation outside the nanoholes [107, 108]. The superior quality of the thermal oxide is additionally manifested in much lower and more uniform etch rates [105]. The surface scans of both evaporated and thermally grown patterned oxide surfaces are depicted in Fig. 3.3b, indicating the higher surface roughness of the evaporated oxide specified by the root-mean squared (RMS) roughness value. In this context, a modified colloidal lithography technique, hole-mask colloidal lithography, has been developed and adjusted to accommodate for the use of thermal oxide in the patterning process.

3.1.2 Hole-Mask Colloidal Lithography

Hole-mask colloidal lithography (HCL) is an adjusted version of colloidal lithography, where the main difference lies in the presence of a sacrificial layer in combination with a thin film mask with nanoapertures (accordingly the name 'hole-mask') used as an evaporation and/or etch mask for patterning [97]. This film mask is obtained based on colloidal particles, that were used as a mask for the deposition of this 'hole-mask'. Eventually, the sacrificial layer is removed, which in turn removes the hole-mask, after the patterning process is completed [97]. In contrast, to the described

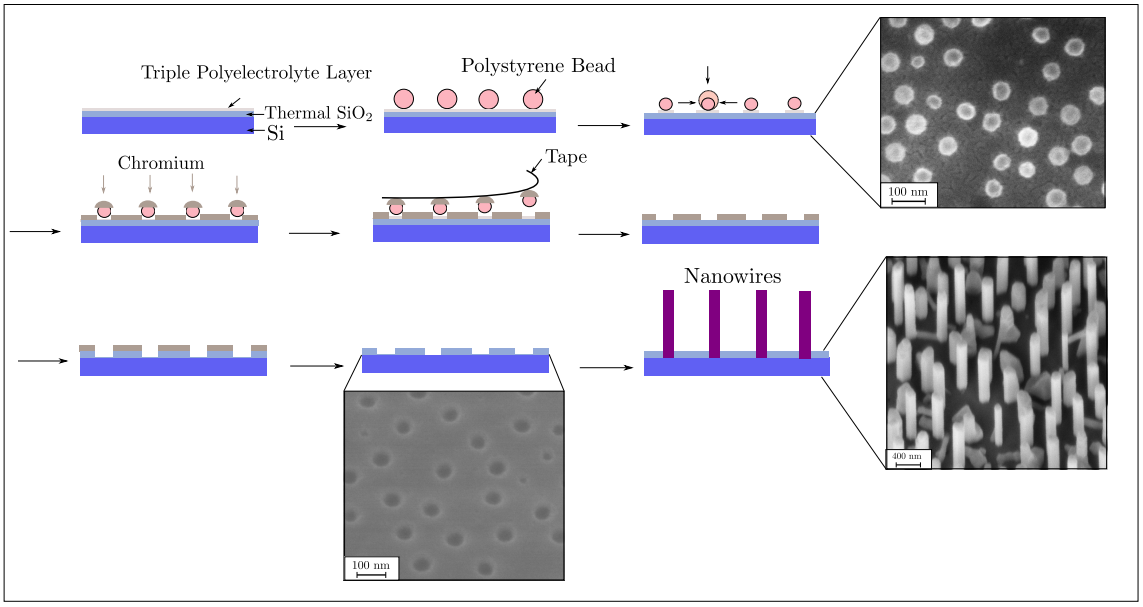

Figure 3.4: A schematic denoting the different fabrication steps for the nanohole template pattern using hole-mask colloidal lithography, where the horizontal arrows denote the chronological order of the described process: the process starts with the surface charging of the SiO_2/Si(111) substrate with the triple polyelectrolyte suspensions, next, the PS beads are drop-cast on the Si surface, where they self-assemble due to electrostatic interactions, the particle size is reduced via exposure to oxygen plasma, which in-evidently partly removes the exposed charged polymer layers, the particle pattern is used as a chromium (Cr) evaporation mask, the beads are tape stripped, leaving behind a nanoaperture patterned Cr film, SiO_2 is dry etched through the Cr mask openings, the Cr is wet-etched, leaving behind a patterned thermally grown SiO_2 layer with a nanohole template. Selective-area growth of NWs proceeds through the mask openings. The SEM insets illustrate the results of the key fabrication steps and the SAE NW growth.

HCL process, the technique developed here to pattern the thermal silicon-dioxide does not rely on a sacrificial layer. In fact, the fabrication steps depicted in Fig. 3.4 indicate, that a hole-mask is indeed used to define openings in the silicon-dioxide, but after processing the hole-mask is simply removed rather than lift-off by the sacrificial layer.

In analogy to the colloidal lithography process the polycation/polyanion layers are deposited in the same manner on the sample surface after the surface activation step by oxygen plasma treatment as previously described, in order to enable the self-assembly of the PS beads on the surface. In contrast to the CL process, the sample to be patterned here is a Si substrate with a 24 nm thermally grown silicon-dioxide layer, accordingly the charged polymer layers and the PS beads are deposited on the thermal SiO_2 surface. Following the particle deposition, a 30-second-oxygen plasma treatment step is performed to shrink the particles and eliminate the exposed charged polymer layers. Next, a 20 nm thick chromium (Cr) film is evaporated. In analogy to the CL process, the PS beads are removed via tape stripping, leaving behind a Cr film with nanoapertures on top of the SiO_2 surface. Similar to the CL process, following the tape stripping, oxygen plasma is used to ash away the residual polymer layers that were inaccessible in the previous oxygen plasma treatment step.

In order to transfer the nanohole pattern to the SiO_2 layer, the patterned Cr layer is used as an etch mask. The SiO_2 is etched using a dry etching step. In fact, a mixture of tetrafluoromethane (CF_4) and oxygen are fed to the inductively coupled plasma/ reactive ion etching (ICP/RIE) chamber to etch the SiO_2 through the mask openings. It is noteworthy, that the etch rate has been calibrated to ensure that this dry-etching step does not reach the underlying Si substrate, i.e. a roughly 22 nm-thick layer of the exposed SiO_2 is etched, leaving a few nanometres of SiO_2 in the bottom of the etched openings. This consideration is essential, seeing as Si has been reported to be efficiently etched by the CF_4/O_2 mixture [109, 110]. Accordingly, over etching of the SiO_2 layer could eventually lead to the unpremeditated etching of the underlying Si substrate, thus compromising the quality of the Si surface [110], which in turn might affect the integrity of the grown NWs on Si. As a matter of fact, it has been reported that reactive-ion etching beyond the SiO_2/Si interface yields non-vertical NW growth on the Si(111) surface [66]. The etching of SiO_2 through the hole-mask transfers the hole-pattern to the silicon-dioxide layer. Next, the Cr mask is removed. The Cr is removed using a chemical wet-etch step using a ceric ammonium nitrate-based solution. This solution has been reported to be compatible with SiO_2 [111], thus maintaining SiO_2 film thickness and surface roughness properties, which has been indeed confirmed by AFM surface and profile scans (see Fig. 3.3b). It has been observed that following the SiO_2 dry etching step, soaking the patterned samples in the Cr etchant fails to remove the Cr layer. The removal of the Cr layer is easily identified by observing the color of the sample surface. The color of the Cr layer is dark brown, whereas the surface of the SiO_2/Si surface is grey-colored. For the successful removal of the thin Cr layer by the Cr etchant solution, an oxygen plasma exposure step preceding the wet-etch of Cr, has deemed to be very effective in removing the Cr thin film. This could be explained by the presence of a fluorocarbon layer on the chromium surface formed during the SiO_2 etching in CF_4/O_2 [112], which inhibits the active species from reaching the Cr layer and efficiently etching it. In this regard, oxygen plasma treatment seems to successfully remove this fluorocarbon layer. This could be ascribed to oxidation reactions of fluorcarbon species with oxygen, resulting in free fluorine atoms [112]. These fluorine containing species are then diluted with oxygen [112]. It is worth mentioning that although this oxygen plasma procedure is able to successfully eliminate the unintentionally deposited fluorocarbon layer, it might cause oxidation of the Cr surface. In fact, this Cr oxide layer seems to reduce the Cr etch rate. Furthermore, observation of the etching procedure shows that it usually takes about 1-1.5 minutes for the color of the Cr to start fading (indicating the onset of the etching process), but once this oxide barrier is overcome, it takes about 20-30 seconds to completely remove the Cr layer. This is in agreement with the time it takes for the Cr etchant to successfully remove the Cr oxide layer, which exhibits a much slower etch rate, whereas the removal of the pure Cr takes less time for etching which is in agreement with the etch rate obtained for pure Cr thin films.

The removal of the Cr layer yields a Si substrate with a patterned thermal oxide. In analogy to the CL technique, the patterned samples need to be etched in BHF to remove the few nanometre oxide layers in the bottom of the openings to ensure the Si surface is exposed through the mask openings. In analogy to the CL technique, this oxide etch step reduces the mask thickness to

roughly 17 nm. The etch step in BHF additionally removes any contaminants and guarantees the cleanliness of the substrates before MBE loading. It is worth mentioning, that this two-step removal of the thermal oxide within the holes by combining RIE (anisotropic etching) and BHF wet etching (isotropic etching) yields good control over the lateral dimensions of the holes while keeping the Si surface unharmed. As indicated in Fig. 3.3b, the nanoperture size seems to be in correspondence with the bead size (see inset of of Fig. 3.4), indicating almost negligible lateral etching (highly anisotropic etching).

NW growth is successfully demonstrated on the patterned thermal-oxide/Si substrates. The growth on thermal-oxide patterned samples still exhibits parasitic clusters. Nevertheless the clusters are reduced and the NW nucleation outside the defined openings is completely suppressed, predicated by the much higher mask quality (free of pinholes). It is worth mentioning, that the existence of the parasitic clusters could be ascribed to the low growth temperature. As already mentioned, low growth temperatures tend to increase the sticking coefficient of incoming adatoms on the mask surface as well as reduce their surface diffusion length, thus facilitating the formation of parasitic clusters, which is in agreement with selective-area growth on e-beam patterned thermal silicon-dioxide substrates for MBE NWs [66, 106]. The reduction in parasitic clusters is also signified by the longer NWs for the high-quality oxide samples, implying reduced competition for the incoming atoms between the clusters and NWs, allowing the wires to grow higher, as will be further elucidated in section 3.2.

3.2 Catalyst-Free Growth of InAs NWs on Si

3.2.1 Experimental Details and Selective-Area Epitaxy

All growth experiments were performed in a Riber Compact C21 MBE system. As previously mentioned in sections 3.1.1 and 3.1.2, following the BHF etching, the samples were loaded in the MBE system. The growth-ready samples are loaded to the degas chamber and annealed there for an hour at 400°C prior to loading to the growth chamber. Next, the wafer is transferred to the growth chamber, where it is further annealed at a higher temperature (T = 750°C) for 10 minutes to ensure proper degassing and contamination removal. This degassing step as well as the subsequent substrate cooling to the desired growth temperature was performed under a flow of an As-flux, as indicated in the diagram of Fig. 3.5a. The opening of the As-shutter prior to growth initiation serves the purpose of ensuring the stabilization of the As-flux. It is noteworthy, that As possess a very low sticking coefficient to the surface at temperatures above 500°C unless combined with group-III atoms [113]. Furthermore, the formation of an As prelayer (for lower temperatures) on the substrate is not critical to the growth process, seeing as this As pre-layer is known to be very unreactive, accordingly excess As atoms do not stick to the almost inert As prelayer, thus avoiding the presence of an As-rich layer on the surface. As a matter of fact, in UHV environments As molecules tend to desorb at temperatures greater than 250°C [114]. Furthermore, variations of the duration of this arsenic pre-exposure step was reported to have no effect on InAs NW growth in MBE systems [66]. As the cool down is completed and the growth temperature is reached, the In shutter is opened (see Fig. 3.5), thus signifying the growth initiation. During the growth process, the substrate is rotated at a rate of 3 rotations per minute to promote growth uniformity across the substrate. When the desired growth time is reached, the In shutter is closed indicating the termination of growth. The substrate is cooled down to 200°C to allow its transfer once again to the loadlock, where it can be taken out for post-growth characterization. The final temperature ramp down is also performed under a flow of As-flux.

For the growth runs examined in this work, substrate temperatures were varied between 440°C and 490°C. Furthermore, the growth time was fixed at 90 minutes, unless otherwise specified. With the regards to the In-flux, it was varied to yield In growth rates between 0.25 Å/s and 0.05 Å/s, as calibrated for equivalent thin film InAs growth via RHEED oscillation measurements. The effect of the V/III ratio on NW morphology was investigated as well by varying the As beam equivalent pressure (BEP) for a given In-flux. Accordingly, the As-flux was changed to encompass a BEP between 4.5×10^{-6} Torr and 7.5×10^{-6} Torr.

Non-catalytic $\mathrm{III}-\mathrm{V}$ NW growth has been reported to primarily rely on facet-driven selective-

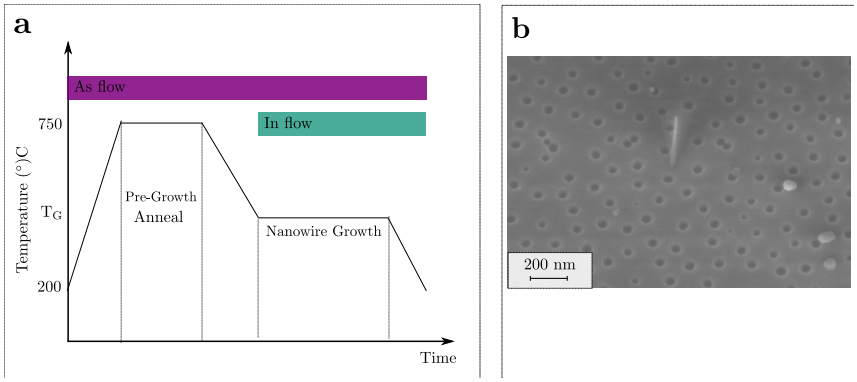

Figure 3.5: a. Schematic illustration of molecular beam flow of As and In together with the temperature sequence depicted over time. Adapted from [119]. b. 30 degree titled SEM image indicating no NW growth, due to coverage of the crystalline openings with native oxide, thus suppressing nucleation

area epitaxy (SAE) on dielectric mask-templated substrates [66, 67]. The purpose of SAE is to limit the incorporation of the group-III atoms to pre-defined areas on a patterned growth substrate by the choice of appropriate growth conditions [106]. As a matter of fact, the dielectric mask, in which the pattern is defined is amorphous. In contrast, the openings in the mask are crystalline in accordance with the underlying growth substrate. Accordingly, crystalline growth is suppressed on the dielectric mask, whereas in the openings grown structures are crystalline seeing as the incoming atoms have access to the crystal surface. Thus crystalline growth is preferentially achieved within the pre-defined pattern openings. As a matter of fact, Fig. 3.5b shows, that if incoming atoms have no access to the underlying crystalline substrate, NWs are not able to nucleate. The native oxide within the holes of the sample shown in Fig. 3.5b was not removed, thus resulting in extremely poor NW nucleation yield. This confirms the importance of the accurate execution of the patterning process, as well as confirms the selectivity between the masked and unmasked regions in providing efficient nucleation sites. SAE could be ascribed to two main effects, adatom diffusion on the oxide surface and a higher desorption rate of adatams on the oxide mask compared to the crystalline openings [106]. Diffusion of adatoms from the mask surface to the openings is partially driven by a concentration gradient between the masked and unmasked Si surface. This gradient originates from different lifetimes of adsorbed In-atoms before desorption from the mask surface or incorporation in the growing structures [106]. Accordingly, this gradient results in a net diffusion of In adatoms from the mask surface to the Si openings. Diffusion of adatoms is additionally dependent on the growth temperature. Nevertheless, this effect has been reported to be less significant for driving SAE in comparison to the desorption effect. In fact, the desorption is promoted by the higher sticking coefficient of In(As) atoms on the Si substrate with respect to the mask surface, due to increased binding sites on Si. In this regard, the unfavored growth on the oxide mask is thus highly dependent on the presence of rough edges or steps on the oxide surface where the diffusing adatoms become easily attached. Rough edges and steps provide good nucleation sites due to their possession of two attachment facets, as indicated in Fig. 3.6a [115], thus facilitating the capture of diffusing adatoms. As a result, polycrystalline InAs clusters (parasitic) are observed to grow at these nucleation kinks. The clusters are polycrystalline, seeing as the mask surface is amorphous.

The SEM micrographs in Fig. 3.6b indicate that indeed selective-area epitaxy was achieved on the lithographically patterned substrates. The topview of the InAs nanowires, showing a hexagonal structure, is a clear indication of the epitaxial conformity with the underlying Si substrate. As indicated in Fig. 3.6b-(a), the projection of the atomic face-centered-cubic {111}-plane, yields a hexagonal contour [116], which explains the hexagonal cross-section of the synthesized wires. In accordance with the crystallinity of the Si surface, the synthesized wires have six vertical $\{\bar{1}10\}$ side-facets where as the crystal orientation of the top surface is a (111)-oriented plane. Furthermore, the vertical growth of the NWs with respect to the horizontal further confirms the epitaxial relationship with the underlying Si (111) substrate. As a matter of fact, this perpendicular orientation corresponds to one of the four $< 111 >$ typical directions for the (111) crystal [117]. The

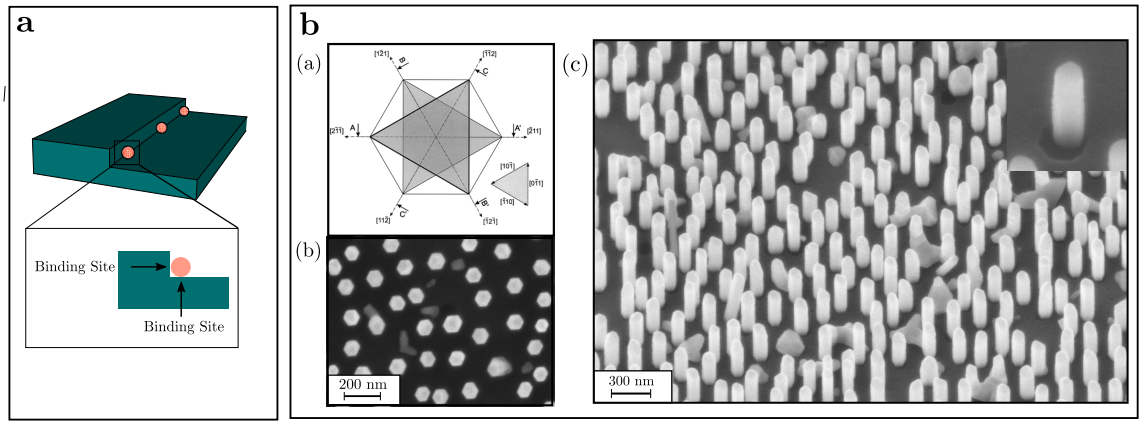

Figure 3.6: a. Schematic illustration of step nucleation, where adatoms are eassily attached due to existence of 2 or more attachment facets. b. (a) A schematic illustration of the projection of the fcc {111}-plane, resulting in a hexagonal contour. From [116]. (b) top view of selective-area growth nanowires on patterned substrates, indicating a hexagonal cross-section in accordance with growth on (111)-oriented substrates. (c) 30 degree tilt of SAE NWs, indicating growth selectivity between the mask and substrate. The inset is a zoomed in view of a NW showing typical edge/step nucleation of site-selective growth.

three other equivalent $< 111 >$ directions yield NWs that are tilted by an angle of 19.5° with respect to the horizontal. The three titled growth directions arise due to the polar/non-polar heterointerface between the $III - V$ and the Si surface [118]. The control over growth directionality has been reported by Tomioka et. al. [119] for selective-area InAs NWs in metal-organic vapor phase epitaxy (MOVPE), where the varying hydrogen, arsenic pre-wetting conditions affected the growth yield of vertical NWs. Nevertheless, the control over growth directionality for MBE growth has been reported to mainly depend on the optimization of the pattern processing step, i.e. by not inferring damage to the Si surface during SiO_2 etching [66]. This stands in agreement with the wires obtained in the presented work, as indicated in Fig. 3.6b. The difference between the two growth processes MBE vs. MOVPE, could be attributed to the different chemistries and kinetics governing both growth techniques. The precursors in MOVPE contain hydrogen and carbon, whereas the MBE process relies on elemental species. Furthermore, molecular arsenic is known to desorb at relatively low temperatures as already mentioned, accordingly pre-wetting conditions do not play a role in controlling directionality in MBE growth [114].

The inset of Fig. 3.6b-(c) showing NWs grown less than the conventional 90-minutes used in this work, indicates that the synthesized NWs are smaller than the opening diameter and nucleate preferentially at the edge of the of the pattern opening, which stands in agreement with site-selective growth [120]. As the growth proceeds longer, past this nucleation phase, NWs grow longer and thicker, completely filling the nanoholes, as indicated in the SEM images of Fig. 3.1 and 3.4.

3.2.2 Effects of Growth Parameters on NW Morphology

After confirming the epitaxial growth of InAs NWs via SAE, investigation of the size-scaling behavior of NWs in response to varying In-flux, V/III ratio and growth temperature is presented.

3.2.2.1 In-flux

The examination of the varying In growth rate on NW morphology necessitates the fixing of the other growth parameters. In this regard, the growth time was fixed for one hour, the V/III ratio was constant at 24 and the growth temperature at T = 440°C. Fig. 3.7 shows SEM images of NWs grown with different In growth rates, as well as presents a plot of NW height and diameter as a function of varying In-flux. Seeing as the As-flux for this growth series is relatively high, the growth is expected to be limited by the In growth rate. Observation of the NW dimension's

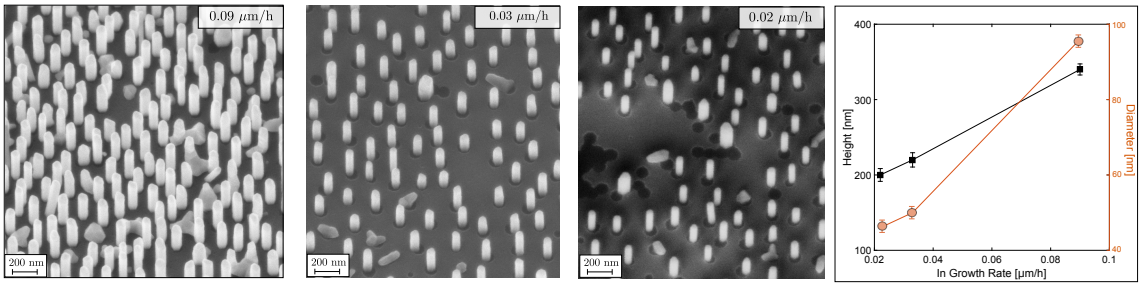

Figure 3.7: 30 degree tilted SEM images of NWs grown with different In growth rates as indicated in the top right corner of each image respectively. A plot of NW height and diameter as a function of growth rate, gives a quantitative scaling behavior.

dependence on In-flux (see plot of Fig. 3.7) confirms this hypothesis. In particular, the NW length and diameter are observed to scale with In growth rate, in agreement with SAE InAs NWs [121, 122]. Calculating the axial growth rate for synthesized wires, by dividing the NW height over the growth time, yields much higher growth rates than the supplied In-flux. More specifically, the NW axial growth rate for the highest In-flux supply is calculated to be 1.3 Å/s as opposed to the supplied In growth rate of 0.25 Å/s, yielding a ratio of 5.2. The same behavior is observed for NWs grown under the lowest In-flux, yielding an even higher ratio between the NW axial and supplied In growth rate ≈ 7.5. This clear difference between the NW axial growth rate and the supplied In flux, signifies that NW growth is not limited to direct incorporation from the NW top facet, but is also strongly dependent on the contribution from surface-diffusing In-atoms.

3.2.2.2 Growth Temperature

Analogous to the previous case, in order to investigate the effect of growth temperature on the NW growth process, other growth parameters were fixed. More specifically, the growth time was fixed at 90 minutes, the In growth rate and V/III ratio were kept at 0.25 Å/s and 24 respectively. The growth temperature was varied between T = 440°C and T = 490°C. Fig. 3.8 shows SEM micrographs of NWs grown at different temperatures as indicated on the top right corner. Observation of these images signifies that the choice of growth temperature clearly affects the NW dimensions as well as the amount and size of parasitic clusters in between the wires. With regards to the NW morphology, higher temperatures result in significantly shorter wires. In fact, the NW length drops from 640 ± 40 nm (at T = 440°C) to 184 ± 21 nm (at T = 4750°C). The NWs grown at T = 490°C no longer exhibit the typical elongation along the axial direction, thus yielding nanodiscs. In contrast, the increase in diameter with increasing growth temperature is less severe, in particular the diameter is observed to increase from 102 ± 7 nm (at T = 440°C) to 177 ± 30 nm (at T = 475°C). The characteristic NW height dependence on growth temperature has been previously reported and has been attributed to enhanced thermal decomposition of the NW from the top (111) plane as well as the re-evaporation of surface-diffusing In atoms before their arrival to the NW axial growth front [66, 121, 123]. The increase in NW lateral dimensions with growth temperature, stands in contrast with selective-area growth of InAs NWs in MOVPE [123]. In particular, SAE of InAs NWs in MOVPE show a decrease in NW diameters with increasing substrate temperature predicated by the enhanced desorption of As from the NW side-facets, resulting in fewer bonding sites for the In-atoms, which in turn suppresses the lateral growth [123]. These contradicting observations for the two growth techniques could be attributed to the different growth kinetics of both techniques. The UHV environment of the MBE yields much longer diffusion lengths of adatoms compared to MOVPE [124], which in turn could lead to an enhanced deposition from the NW side-walls. In fact, the reduced clusters observed for higher growth temperatures result in reduced competition for the diffusing adatoms, i.e. increases the capture area for diffusing adatoms per NW [121]. More specifically, the rate of side-wall deposition could be higher than the dissociation rate, yielding a net increase in NW lateral dimensions. Nevertheless, since the two mechanisms are contending, the effective radial growth rate with temperature is rather low. It is worth noting that for all investigated temperatures, the NW diameter exceeds the pattern openings, i.e. lateral

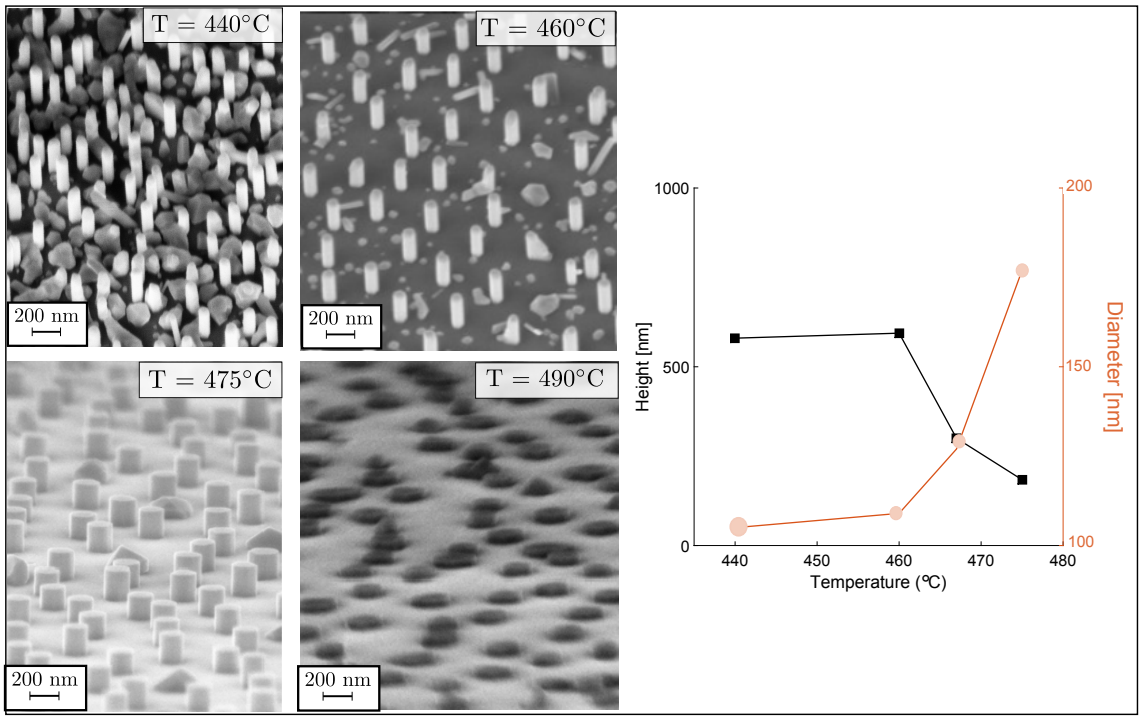

Figure 3.8: Tilted SEM images of NWs grown at different temperatures as indicated in the top right corner of each image respectively. A plot of NW height and diameter as a function of growth temperature, gives a quantitative scaling behavior.

overgrowth is observed. This observation could indicate that the pattern dimensions put no restriction on the NW diameters, they merely serve as nucleation sites. This stands in contrast to catalyst-assisted NW growth, where the NW lateral dimensions are observed to comply with the droplet diameter [125, 126].

In regards to the increase in parasitic clusters with decreased growth temperature, this is most likely attributed to the dependence of the diffusion length on substrate temperature as well as on different sticking probabilities of incoming atoms. It has been reported that lower growth temperatures yield higher sticking coefficients of impinging atoms on the dielectric mask surface [66, 106, 121]. Accordingly, lower growth temperatures promote the immobilitzation of adatoms on the dielectric mask surface, thus nucleation of polycrystalline clusters is observed. Furthermore, the capture of diffusing adatoms by these clusters is facilitated by the reduced diffusion length associated with lower substrate temperatures. As a matter of fact, the diffusivity, D is exponentially dependent on temperature, where the diffusion length λ is given by the well known equation $\lambda = \sqrt{D\tau}$, where τ is the average time of adatoms on the mask surface [127]. This clear temperature dependence of adatom diffusion length and sticking coefficients on temperature, increases incorporation selectivity between the Si openings and the mask surface, thereby suppressing the growth of parasitic clusters for higher growth temperatures, where adatoms are able to migrate longer on the surface and efficiently reach the NW nucleation sites.

3.2.2.3 V/III Ratio

Even though the lowest temperature investigated (T = 440°C) yielded the highest amount of parasitic clusters, it exhibited NWs with the highest aspect ratio (NW height/NW diameter). In this regard, the effect on varying the V/III ratio is investigated at this temperature for a growth duration of 90 minutes and a fixed In growth rate equal to 0.25 Å/s. Since the In-flux is fixed for this growth series, the V/III ratio was varied by changing the As-flux (from 4.5×10^{-6} Torr to 7.5×10^{-6} Torr). Observation of the size scaling behavior of the synthesized NWs (see Fig. 3.9), indicates that the NW height increases with an increased V/III ratio. In particular the NW height

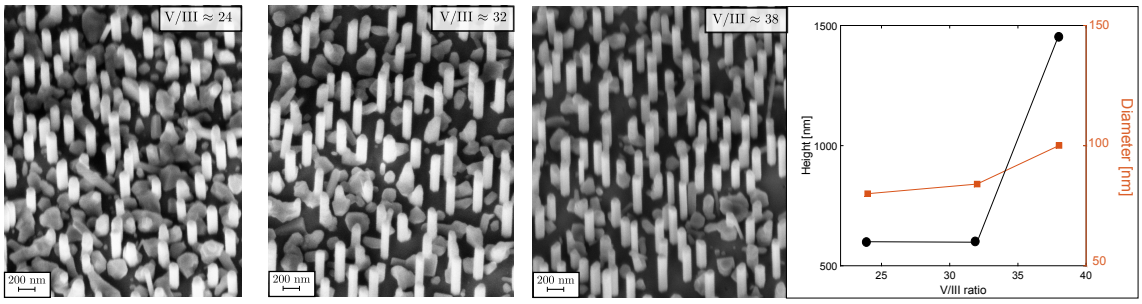

Figure 3.9: Tilted SEM images of NWs grown at varying V/III rati as indicated in the top right corner of each image respectively. A plot of NW height and diameter as a function of growth temperature, gives a quantitative scaling behavior.

goes from 640 ± 40 nm (V/III $\sim$ 24) to 978 ± 44 nm. In contrast, the NW lateral dimensions are observed to remain almost unchanged. This behavior has been reported for catalyst-free growth of InAs [121] and has been associated with enhanced In surface diffusion on the mask surface as well as on the NW side-falls, thus favoring incorporation at the NW apex. It is worth noting, that in analogy to the growth series with varying In-flux, this growth series is also As-rich. Accordingly, the growth proceeds under In-limited conditions. the enhanced diffusion of In adatoms is also manifested in the reduction of parasitic clusters for the highest examined V/III ratio. In fact, this growth series is performed at a rather low growth temperature, where the density of parasitic clusters is expected to be high, an increase in the As-flux (V/III ratio) seems to induce the preferential incorporation of surface-diffusing In atoms towards the NW axial growth front via improved diffusion, thus impeding parasitic growth.

4

Theoretical Growth Modelling for Selective-Area Growth NWs using Molecular Beam Epitaxy

4.1 Introduction

Fundamental physical limits of conventional top-down fabrication techniques are restraining the continued miniaturization of electronic devices. Therefore, new device architectures, materials and the investigation of new ways of device fabrication, such as nanoscale self-assembly methods, are being extensively studied to meet the growing computational demands of the electronic industry as well as effectively contribute to the extension of Moores Law beyond the current complementary metal oxide semiconductor (CMOS) fabrication technology [128]. Nanoscale self-assembly is a bottom-up fabrication approach, which presents a viable option for mitigating the constraints put forth by the commonly used top-down fabrication methods. Bottom-up approaches achieve control over the spatial arrangement of nanoscale building blocks in the different growth directions already during growth via self-assembly. An example of such self-assembled nanostructures, are semiconductor nanowires (NWs). Semiconductor NWs are being comprehensively scrutinized due to their unique physical properties, including their large surface-to-volume ratio, as well as their growth and structural properties. III-V NWs, predominantly provide promising prospects for innovative electronic and optoelectronic devices, due their outstanding electron mobility as compared to silicon and the flexibility to tune and engineer their bandgap [4, 129, 130]. In addition to these advantages, III-V NWs are compatibile with the existing cost-effective and high performance silicon (Si) platform. The integration of III-V semiconductor NWs with the well-established Si technology combines the benefits of the current device technologies with the exceptional electronic and optoelectronic properties of III-V semiconductors. The mature compatibility of III-V NWs with the existing Si platform is predicated by their small lateral dimensions, which are able to efficiently relax strain, in particular, by accumulating strain in only two dimensions, thus alleviating the challenges associated with the large lattice and thermal mismatches encountered during III-V hetero-epitaxy on Si [16]. Consequently, enabling the direct growth of III-V NWs on Si and yielding epitaxial NWs with possibly reduced defect-density III-V/Si hetero-junctions.

In spite of the abundant advantages provided by these nanostructures, an understanding on how growth and growth kinetics affect the geometry and quality of III-V NWs remains an inquiry worth investigating. Currently, most of the III-V NWs are synthesized via catalysts (foreign catalysts or self-catalysts) in the well-developed vapor-liquid-solid (VLS) growth mechanism employing diverse growth techniques, e.g. metal-organic vapor phase epitaxy (MOVPE) [53, 54] , chemical beam epitaxy (CBE) [55, 56], molecular beam epitaxy (MBE) [57, 58], etc. Conventional nucleation mechanisms, which rely on foreign catalysts, such as gold, could lead to unpremeditated catalyst incorporation within the crystalline NWs. Metal impurities are known to adversely impact the performance of functional III-V devices [131]. In particular, gold in combination with Si has been identified to introduce deep level traps in the semiconductor bandgap and thus deteriorate device performance [59].

On the other hand, selective-area epitaxy (SAE)of NWs on patterned substrates provides a strategy to grow catalyst-free NWs. Non-catalytic NW growth techniques have received less con-

sideration, eventhough they posses the great potential of avoiding catalyst contamination. By creating well-defined openings in a dielectric mask, facet-driven SAE could accomplish position-controlled nanowires [123, 132]. The main concept of SAE is to limit nucleation of nanostrucutres to predefined openings on a patterned substrate by applying the appropriate growth parameters. Two main processes are known to contribute to SAE. The first is ascribed to adatom diffusion on the patterned mask and their eventual arrival at the openings, where the adatoms can form an epitaxial relation with the underlying crystalline substrate. The second is assigned to the enhanced desorption of adatoms from the amorphous mask as compared to the mask openings [133].

Nanowire growth using SAE has been demonstrated [66, 123, 132, 134, 135], where the focus has been directed towards achieving optimized NW geometries and properties. In particular, experimental studies have been conducted to investigate NW geometry and quality dependencies on process conditions (temperature, growth time, V/III ratio) [121, 122], on pattern design (opening diameter and pitch) [66, 135] and dielectric mask quality [108]. These investigations yielded various observations, including increased NW diameter and height with longer growth time [66], reduced NW height with increased mask opening diameters [136] and shorter NWs with increased temperature [121]. Though these studies offer valuable insights, they lack a comprehensive description that explains the observed phenomena and thus fail to offer a general model that underlies a quantitative process optimization.

Most of the studies dealing with the growth mechanisms of NWs are concerned with catalyst-induced growth. Fewer studies have been devoted to selective-area epitaxy of NWs. Growth models developed for catalytically-induced NWs fail to describe the growth kinetics of catalyst-free NWs, due to differences in the growth mechanism of both synthesis techniques. One main difference between both techniques is the presence of a liquid catalyst droplet at the wire apex of catalytically-synthesized wires acting as an efficient collector to incoming atoms and limiting the NW lateral dimensions. The absence of this droplet in catalyst-free wires is expected to eliminate restrictions on NW lateral dimensions and to alter the kinetics of the growth mechanism, making it rather dependent on the diffusion of adatoms. Accordingly, to develop a model for the catalyst-free growth of nanowires, the different kinetic adatom processes such as adsorption and surface diffusion need to be accounted for. Adatom diffusion, particularly is a crucial parameter, seeing as it can have a significant impact on growth rate, material quality and surface morphology [137]. The purpose of the current study is to propose an explanation for the experimental observations and to develop a growth model for nanowires synthesized via selective-area epitaxy using MBE (SA-MBE) with the aim to propose a guideline for controlling the growth process parameters to achieve NWs with optimzied geometries and structure dependent properites. The derived model is based on a diffusion-induced growth mechanism. A similar model has been proposed for selective-area growth of nanowires using metal-organic chemical vapor deposition (MOCVD) [136, 138], but the work at hand presents a derivation for SAE nanowire growth using MBE. The discrepancies regarding the nanowire length-diameter correlations for both systems, MOCVD versus MBE, can be attributed to dissimilarities of the growth systems. Nanowire growth by elementary source MBE is considerably different than that by MOCVD or metal-organic vapor phase epitaxy (MOVPE). In MBE systems, adsorption of the species in the vapor phase contained within the molecular beams does not entail a thermally-activated decomposition of organometallic molecules. Thus, adatom depositon is not selective and accordingly is mainly driven by adatom diffusion on the surface and on the nanowire side-walls [126]. Eventually, the derived model is fit to experimental data to evaluate the dependence of nanowire lengths, radii and growth rates on the growth process parameters.

4.2 Nanowire Growth via SAE

The data from selective-area epitaxy of InAs NWs in an MBE system are taken as an expample. InAs nanowires are grown on Si(111) substrates. SAE is achieved via a thin dielectric mask, e.g. SiO_2 with hole structures on top of the Si(111) substrate. Seeing that the dielectric mask is amorphous, crystalline growth is suppressed on the mask, whereas within the openings the incoming atoms have access to the crystalline Si substrate, thus they form crystalline nanowires in registry with the underlying substrate [139] and preferentially grow within the mask openings.

This effect is also enhanced due to the higher volatility of In(As) on SiO_2 with respect to Si surfaces. This volatility could be explained by the lower sticking coefficient of In(As) adatoms on SiO_2 relative to Si, due to reduced favorable binding sites on the dielectric mask. This implies that the growth of InAs on the surface of the oxide mask is highly dependent on the availability of nucleation sites, where In atoms can become easily attached. In cases where the oxide is rather rough, providing nucleation centers, parasitic polycrystalline InAs clusters are observed [133]. The growth selectivity could be further optimized by adjusting the growth temperature. At low growth temperatures, the sticking probability of the incoming atoms is enhanced, due to shorter diffusion lengths of adatoms, thus the formation of parasitic clusters on top of the amorphous mask is observed [66]. However, for higher growth temperatures, a lower sticking probability of incoming atoms on the dielectric mask is observed, thus allowing the adatoms to diffuse longer on the SiO_2 mask allowing them to reach the nanowire nucleation sites more efficiently. Hence, growth selectivity is improved and the nanowires are observed to nucleate only within the predefined openings.

4.3 Growth Model

In the following, the focus is on In-atoms seeing as they (group – III) are the rate limiting, surface diffusing species, implying that they determine the growth rate, seeing as the group – V atoms, in the given example As molecules, are generally supplied in excess. The calculated nanowire lengths and radii from the derived model for different growth times are compared to experimental data.

4.3.1 Radial Growth

MBE grown wires using SAE are observed to have increased diameters with increased growth time, which stands in contrast to wires grown via a catalyst [66]. Typically, catalytically synthesized nanowires have negligible radial growth, seeing as the catalyst droplet at the apex of the wire defines the nanowire lateral dimensions [55]. As opposed to other derived models that assume the diameter to be defined by the mask opening size and thus be constant over growth time [124, 137, 138, 140], NWs grown via SAE in MBE systems has been reported to overgrow the mask-defined openings [66]. This observation necessitates the inclusion of the diameter evolution with growth time.

Regarding the inception of the growth phase, the work of Koblmüller, *et.al* reveals that dur-

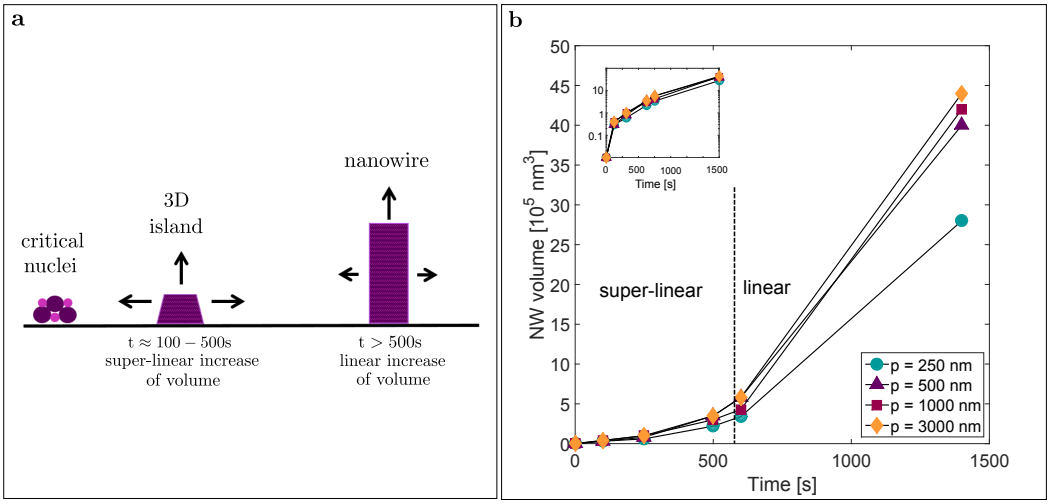

Figure 4.1: a. Schematic showing the evolution of nanowire nucleation and growth over relevant time interverals, reproduced from [90]. b. Data extracted from [66, 121], nanowire volume increase with respect to time during SA-MBE growth, showing super-linear growth followed by a linear volume increase. The inset illustrates the same curve but for a semi-logarithmic scale.

ing the nucleation and early growth phase of thin films, supear-linear growth takes place. This super-linear growth is in good agreement with the 3D-island nucleation and growth behaviour, demonstrating power-law growth relationship with early onset of growth time [141]. Similar behavior is observed for nanowires, super-linear growth is followed by steady state growth regime, during which a linear increase of nanowire volume is observed over time [142] as indicated in Fig. 4.1. The data for the nanowire volume in Fig. 4.1b is obtained by assuming a cylindrical shape of the nanowires, where the nanowire height and diameter at the different growth times for different pitches are extracted from [66]. In the following, the focus will be on deriving an expression for the time-dependent diameter evolution with respect to growth time.

The model for the nanowire radial growth is derived based on the observation that the NW volume changes linearly with time [121], $V_{\mathrm{NW}} \sim t$, as depicted in Fig. 4.1. By taking into account the cylindrical shape of NWs, the nanowire volume is thus proportional to the square of the nanowire diameter d multiplied by the nanowire height h:

$$\begin{aligned} V_{\mathrm{NW}} &\sim d^2 \cdot h \\ \frac{V_{\mathrm{NW}}}{d} &\sim d \cdot h \end{aligned} \tag{4.1}$$

The radial growth rate is observed to decrease with time [66], as obtained from experimental data (see Fig. 4.2c). The decrease of the lateral growth rate can be attributed to the fact that the *continuously growing* nanowire side-facets are consuming a *fixed* In-flux. In essence, the capture area of the impinging group-III atoms on the nanowire side-walls is increasing with time. Furthermore, the data in Fig. 4.2c indicates that the decrease in lateral growth rate is more prominent for shorter growth durations and less prominent for longer growth times. This can be elucidated by the fact that the relative incremental increase of the side-wall dimensions of the growing wire is more significant in the onset of growth. As the NW diameter matures, however, this incremental increase becomes relatively negligible with respect to the NW diameter. Accordingly, the radial growth rate can simply be expressed by dividing the incoming flux (adatom supply) over the nanowire side-facets:

$$\frac{\Delta d}{\Delta t} = \frac{J_{\mathrm{p}} A_{\mathrm{s}}}{d \cdot h} \tag{4.2}$$

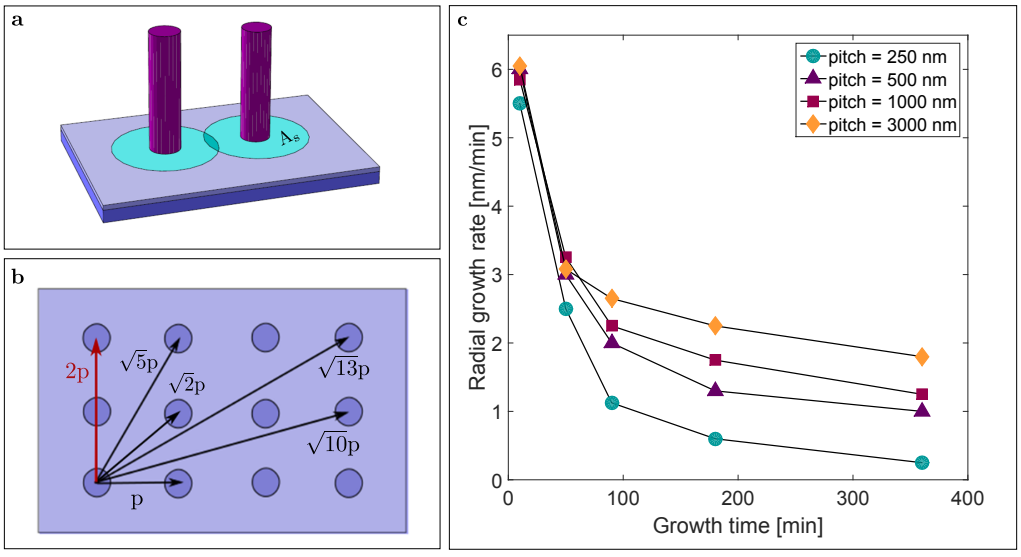

Figure 4.2: a. Schematic of positioned NWs with the effective assembly area of incoming adatoms on the substrate inidicated by a circle A_s. b. Distances to adjacent NWs arranged in a quadratic lattice with pitch p. c. Time evolution of the radial growth rate for different pitches, indicating initially rapid growth rates during early growth phase and gradual transition to moderate growth rates with increased growth time. Data extracted from [66].

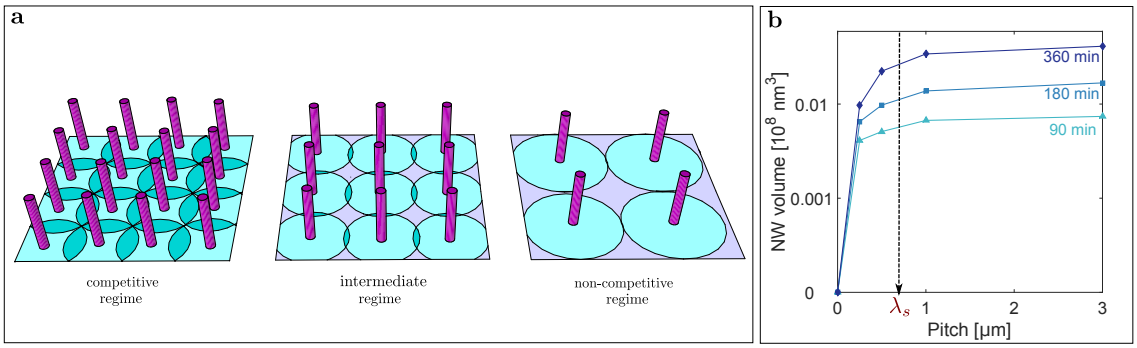

Figure 4.3: a. Schematic of the three distinct regimes by which NWs compete over incoming flux. The circles, indicating the assembly areas of incoming adatoms, are differently overlaid depending on the inter-wire spacing, giving rise to the three regimes: the competitive regime, the intermediate regime and the non-competitive. b. A semi-logarithmic scale of the NW volume plotted against pitch, indicating that the NW volume saturates for bigger pitches. The surface diffusion of adatoms on the surface is extracted, from on the onset of saturation as indicated by the dashed line.

where J_p is the growth rate in [μm/h] representing the equivalent In-flux calibrated for InAs thin film growth by reflection high energy electron diffraction (RHEED) and A_s takes into account the collection of adatoms on the substrate around one NW. This area will be referred to as the adatom *assembly area*. For an array of nanowires in a quadratic lattice, there are different regimes by which the nanowires compete for the In-adatoms on the surface as depicted in Fig. 4.3a. Basically, the collection area of adatoms around a nanowire can be described by a circle, reduced by the partial overlay of circles of neighbouring wires (see Fig. 4.3a). The size of this overlap is dependent on the pitch or the inter-wire spacing. The radius of these circles is dependent on λ_s, the diffusion length of adatoms on the silicon dioxide surface. In fact, the value of λ_s can be estimated from observing the NW volume dependence on pitch, as illustrated in Fig. 4.3b. As can be seen, the NW volume staturates at a pitch of $p \approx 0.75$ μm. The early increase of NW volume with pitch indicates that the impinging adatoms from the area around a NW are assembled to drive NW growth. Hence, the value of p at which the onset of saturation is observed, can be used as a provisional value for λ_s [135].

The assembly area of adatoms around a nanowire, A_s is thus defined over three distinct regimes as follows:

A *competitive regime* where the incoming atoms are distributed equally between the nanowires. More specifically, the pitch is small enough so that every incoming atom ends up in the assembly area of at least one NW. Due to the quadratic arrangement of the NWs on the substrate, this regime is valid for $p < \sqrt{2}\lambda_\mathrm{s}$,

An *intermediate regime* where the assembly area of the adatoms are partially overlapping. As illustrated in Fig. 4.3a, in this regime, the assembly areas are not fully covering the substrate, in defiance to the competitive regime. Thus,A_s in this regime is dependent on both p and λ_s.

A *non-contending regime*, in which the pitch is rather large compared to the adatom diffusion length on the substrate. In particular, p is bigger than double the diffusion length. Thus the wires can be treated almost independently. Thus, the amount of adatoms accessible to each NW is limited by λ_s.

Based on geometrical considerations (see Fig. 4.2b), the effective assembly area, A_s, for each regime is given by [125, 135]:

$$A_\mathrm{s} = \begin{cases} \pi(\lambda_\mathrm{s}^2 - \frac{d_0^2}{4}) & \text{for } p > 2\lambda_\mathrm{s} \\ \pi(\lambda_\mathrm{s}^2 - \frac{d_0^2}{4}) - 4\lambda_\mathrm{s}^2 \cos^{-1}(\frac{p}{2\lambda_\mathrm{s}^2}) + p\sqrt{4\lambda_\mathrm{s}^2 - p^2} & \text{for } \sqrt{2}\lambda_\mathrm{s} < p < 2\lambda_\mathrm{s} \\ p^2 - \frac{\pi d^2}{4} & \text{for } p < \sqrt{2}\lambda_\mathrm{s} \end{cases} \tag{4.3}$$

where d_0 is the hole diameter defined on the dielectric mask. Furthermore, it is assumed that the dielectric mask is isotropic, implying that the adatoms diffuse on it with no preferential direction.

Based on equation(4.1) the lateral growth rate can be equivalently expressed as:

$$\frac{\Delta d}{\Delta t} = \frac{J_{\mathrm{p}} A_{\mathrm{s}}}{\frac{V_{\mathrm{NW}}}{d}} \tag{4.4}$$

Recalling that the nanowire volume is proportional to time, $V_{\mathrm{NW}} \sim kt$, where k is a proportionality constant with the units [nm^3/s], the radial growth rate is thus expressed as:

$$\frac{\Delta d}{\Delta t} = \frac{J_{\mathrm{p}} A_{\mathrm{s}}}{kt} \cdot d \tag{4.5}$$

Considering that the nanowire diameter evolves with growth time, equation (4.5) is more accurately given by:

$$\frac{\Delta d}{\Delta t} = \frac{J_{\mathrm{p}} A_{\mathrm{s}}}{kt} \cdot d(t) \tag{4.6}$$

In order to get the diameter dependence on time, the first-order linear ordinary differential equation is solved analytically by integrating equation (4.6) from t_0 to t, where t_0 is close to zero . The integration yields:

$$d(t) = c \cdot d_0 \cdot (t/t_0)^{\frac{J_{\mathrm{p}} A_{\mathrm{s}}}{k}} \tag{4.7}$$

where c is an arbitrary fitting constant. Fitting the derived diameter model (4.7) to the data extracted from [66] concurs the proportionality constant, k, to be a pitch-dependent constant. More specifically, k increases non-linearly with pitch. The increase of the nominator ($\mathrm{J_p} \cdot \mathrm{A_s}$) is faster than the increase of k causing the whole fraction to increase with pitch. Surveying the exponent values indicates that the diameter-time correlation is less than linear for all the investigated pitches, i.e. the exponent is less than unity for all inter-wire distances. The exponent value for the smallest pitch ($p = 250$ nm) is a factor of 3 less compared with that of the largest pitch ($p = 3$ μm). This significant increase in lateral dimensions with pitch is expected, as for larger pitches, each nanowire is supplied with more atoms, than in the case where the pitch is rather small and neighbouring wires are required to share the incoming atom supply. In addition to the competition on the incoming supply, NWs placed in close proximity, as is the case for smaller pitches, suffer from shadowing effects. In dense arrays of NWs, neighbouring NWs obscure impinging adatoms from reaching the NW side-walls, which becomes even more prominent for growth systems in which the incident angle of the molecular flux is not perpendicular to the growth surface [143]. Shadowing effects, make it thus more difficult for incoming atoms to reach NW side-walls, thus further slowing down the lateral growth rate. This trend, of increased lateral dimensions with larger inter-wire spacing, is anticipated to saturate, seeing as the adatom diffusion length on the silicon dioxide surface is finite. In particular, when the pitch is much larger than the diffusion length of the adatoms on the SiO_2 surface, less adatoms can contribute to the NW growth. The observation of increased diameters with pitch is contrary to what is reported for catalytically synthesized InAs nanowires by MBE. NWs which rely on catalyst-induced growth exhibit diameters, which are mostly pitch invariant [125], seeing as the diameter is mainly constraint by the droplet size. For SAE, the mask opening size seems to not put limitations on the NW lateral dimensions, in fact, according to the data extracted from [66] the nanowires overgrow the openings defined on the amorphous mask.

4.3.2 Axial Growth

The model for axial growth is derived based on a diffusion-induced mechanism and accounts for three different sources of adatoms involved in driving the nanowire vertical growth. The different kinetic phenomena taking place during growth are illustrated in Fig. 4.4a. In addition to the direct incorporation of the atoms from the nanowire tip, there is a significant contribution from the adatoms diffusing on the nanowire side-walls towards the growth interface at the top of the nanowire. The adatoms diffuse to the wire apex from its side-facets driven by a lower chemical potential at the nanowire top surface [137]. Thus, diffusing atoms drive the vertical growth and high aspect ratio nanowires are obtained. The third source includes the diffusion of atoms on the dielectric mask towards the nanowire apex.

The model described in this work is a modified version of the growth model proposed in [136, 138]. The model derived by Ikejiri *et. al* and Xu *et.* al, is based on classifying three main precursor sources which contribute to nanowire axial growth for a selective-area epitaxy using MOCVD. Their model however, treats the diameter dependence on time to be constant. This assumption cannot be applied to SA-MBE where experimental studies indicate, the increase of the diameter with growth time.

It is worth noting that nanowires grown via SAE using MBE systems show almost no tapering across the nanowire. In fact, [66] reported no evident dependence of pitch and growth time on nanowire tapering. The nanowire's gradual decrease from bottom to top is negligible and is measured to be within 2% - 4% for SAE [66]. Thus, the model assumes the diffusion length on the nanowire side-facets to be longer than the nanowires. This assumption is valid in MBE growth, seeing as this is a high-vacuum technique where adatoms are expected to have significantly long diffusion lengths [124]. This implication is in agreement with experimental data of wires grown via SAE. In other systems, considerable material deposition on the nanowire side-walls occurs, which leads to tapered wires. In such growth mechanisms, the adatoms diffusion length is not long enough to allow them to reach the nanowire apex, thus extensive incorporation on the nanowire sides is discernible.

According to the mass conservation principle, nanowire growth is driven by the continuous incorporation of the incoming adatoms to the expanding nanowire volume from the different sources. Consequently, the volume increment of a nanowire during a time interval Δt, as depicted in Fig. 4.4b, can be described by:

$$\frac{\Delta V}{\Delta t} = \frac{\Delta[d^2(t) \cdot h(t)]}{\Delta t} = J_{\mathrm{p}} \cdot [k_{\mathrm{d}} d^2(t) + k_{\mathrm{w}} d(t) h(t) tan(\phi) + k_{\mathrm{s}} A_{\mathrm{s}}] \tag{4.8}$$

The left-hand side of (4.8) represents the time-dependent volume increment. The right-hand side on the other hand accounts for the different contributions to the volume increment from each source multiplied by the growth rate. The first term of the sum describes the direct incorporation from the nanowire top, the second accounts for the side-wall impingement and diffusion to the growth interface and the last term accounts for the surface diffusion on the patterned mask and then on the nanowire side-walls to reach the nanowire top. The factor $tan(\phi)$ accounts for the fact that the incoming molecular beams in the MBE system are at an angle of $\phi = 33°$ with respect to the horizontal. Furthermore, the coefficients k_{d}, k_{w} and k_{s} are time-independent constants, which are positive by definition and serve as weighting factors to each source contribution. They basically account for thermodynamic effects such as nucleation barrier, adsorption and desorption, seeing as thermodynamic effects are not implicitly included in the model. Hence, these coefficients are process dependent. It is worth mentioning, that A_{s} in (4.8) is defined as in the previous section in (4.3).

To express (4.8) in terms of axial growth rate, the right-hand side of equation (4.8) needs to be differentiated, thus yielding:

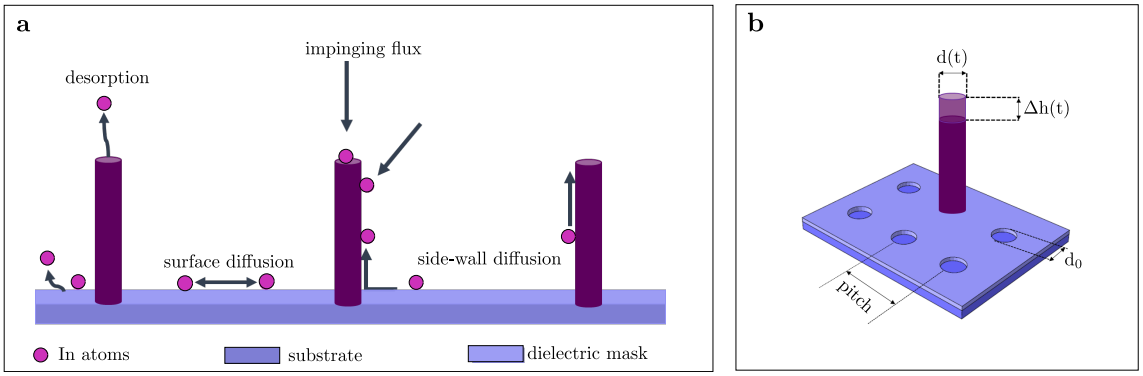

Figure 4.4: a. Schematic of MBE nanowire growth process depicting the relevant kinetic and thermodynamic phenomena b.schematic showing different process parameters and incremental volume increase of a growing nanowire

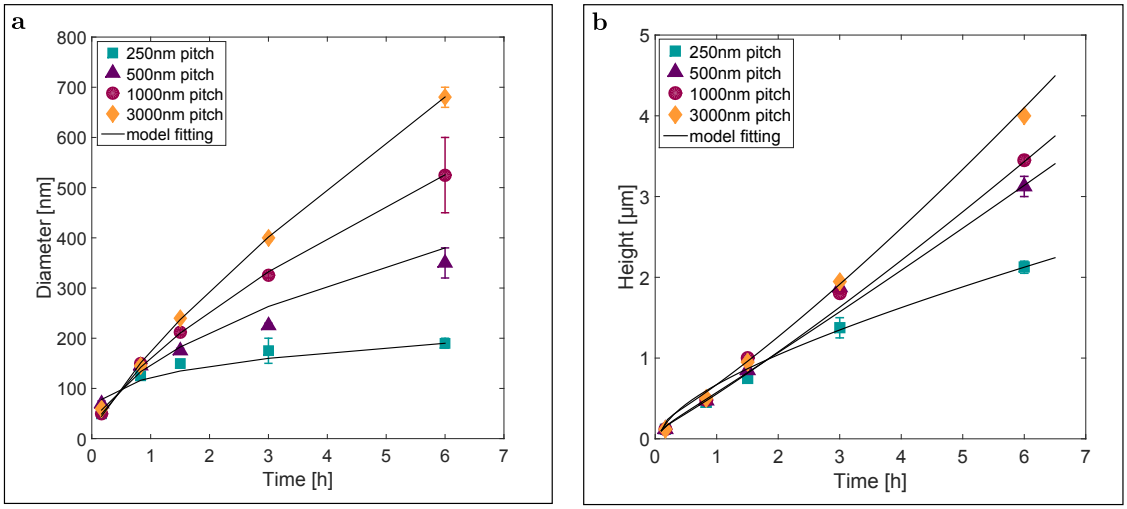

Figure 4.5: a. NW diameter and b. NW height with respect to growth time in hours for different pitches: 250nm − 3μm. The errorbars are extracted from experimental data in [66] The solid lines represent the model fit to experimental data.

$$\frac{\Delta[d^2(t)\cdot h(t)]}{\Delta t} = \frac{\Delta d(t)}{\Delta t}\cdot 2d\cdot h + d^2(t)\cdot\frac{\Delta h(t)}{\Delta t} \tag{4.9}$$

Accordingly, to get an expression for the axial growth rate, the first term in equation (4.9) is subtracted from equation (4.8) as follows:

$$d^2(t)\cdot\frac{\Delta h(t)}{\Delta t} = J_{\mathrm{p}}\cdot[k_{\mathrm{d}}d^2(t) + k_{\mathrm{w}}d(t)h(t)tan\phi + k_{\mathrm{s}}A_{\mathrm{s}}] - \frac{\Delta d(t)}{\Delta t}\cdot 2d\cdot h \tag{4.10}$$

The subtracted term from equation (4.10) essentially, ensures that adatoms contributing to the lateral growth rate are not counted twice, i.e. considered to be contributing to the axial growth rate as well. The term $\frac{\Delta d(t)}{\Delta t}$ in equation (4.10) is replaced by the term derived for the lateral growth rate (equation (4.6)) in the previous section. In order to get an expression for the axial growth rate, a division by $d^2(t)$ is performed, thus yielding the axial growth rate equation as follows:

$$\frac{\Delta h(t)}{\Delta t} = J_{\mathrm{p}}\cdot[k_{\mathrm{d}} + k_{\mathrm{w}}\frac{h(t)}{d(t)}tan\phi + k_{\mathrm{s}}\frac{A_{\mathrm{s}}}{d^2(t)}] - 2\frac{A_{\mathrm{s}}}{kt}\cdot h \tag{4.11}$$

This differential equation can be solved analytically by enforcing the condition that $h(0) = 0$. However, the equation will be solved numerically in the work at hand and will account for the different contributions from the different sources at each iteration.

4.3.3 Model Validation and Discussion

In order to validate the model's conceptual consistence with experimental data reported in literature for nanowires synthesized via SAE using MBE, the model is fitted to experimental data as shown in Fig. 4.5. The solid lines in Fig. 4.5a. and 4.5b. represent the curves generated by the theoretical model based on equations (4.11) and (4.7) respectively, whereas the errorbars represent the experimental data. Data of growth rates of SA-MBE InAs nanowires were reported by Hertenberger *et. al* [66], where they investigated the height and diameter dependence of these nanostructures over growth time. The investigation was executed for different pitches ranging from 250 − 5000 nm, for wires grown with an In growth rate of 0.24 Å/s, a growth temperature equal to T = 480°C and a fixed hole diameter of $d_0 = 80$ nm in the dielectric mask.

The validation of the derived model would be valuable as it would be able to provide insight on the growth kinetics of the NW growth process. Additionally, it would be able to offer a guideline for the choice of the process parameters leading to nanowires with desired geometries and dimensions.

Fig. 4.5a and b clearly illustrate that a two-fold increase in pitch does not yield double the height or diameter for the same growth time. This examination indicates that many effects come into play as the pitch changes. Though bigger pitches exhibit increased assembly areas and reduced competition between neighbouring wires, the NW dimensions do not increase proportional to the increase in pitch. This is attributed to the fact that increased pitches reduce the contribution from the surface diffusing atoms, due to limited adatom diffusion length on the dielectric mask. Furthermore, pitches smaller than the surface diffusion length on the one hand allow surface diffusing atoms to contribute to nanowire axial and lateral growth more efficiently. However, they promote shadowing and competition for adatom supply. Furthermore, Fig. 4.5a shows that for the given growth conditions, the diameters seem to grow beyond the mask opening of $d_0 = 80$ nm. This observation implies that the mask openings merely act as nucleation centres for the growing wires, but do not confine the lateral dimensions of the NWs.

The thermodynamic effects will be discussed in the following section by focusing on the three coefficients providing the relative contributions from the different adatom sources to the NW axial growth.

4.3.3.1 Coefficients: $k_\mathbf{d}$, $k_\mathbf{w}$, $k_\mathbf{s}$ dependence on pitch

In order to get an idea of the kinetic adatom processes taking place, it is important to observe the different trends of the incorporation coefficients k_d, k_w and k_s for the different pitches as shown in Fig. 4.6a. The direct incorporation from the nanowire top seems to be significant for all pitches and changes slightly with pitch. The contribution from the side-wall diffusion is included in both the second and the thrid term in eq. (4.11), k_w accounts for adatoms directly impinging on the nanowire side-walls and their subsequent diffusion to the top. While the third term accounts for adatoms diffusing on the nanowire side-wall after having spent time diffusing on the dielectric mask. For the smallest pitch considered, $p = 250$ nm, the direct impingement on the nanowire side-walls is zero, due to shadowing from neighbouring structures obstructing impinging atoms to efficiently reach the NW side-facets. Accordingly, for the smallest pitch, the main sources contributing to the axial growth are the direct impingement on the nanowire apex (k_d) and the side-wall diffusion following the surface diffusion (k_s). On the contrary, bigger pitches seem to rely on the side-wall impingement and diffusion to drive the vertical growth of NWs. This conclusion is based on investigating the dependence of the side-wall coefficient on pitch. In particular, k_w increases with pitch, which is in consonance with less effective shadowing for larger inter-wire spacing. In contrast, k_s shows the opposite behaviour, it starts out contributing significantly to the axial growth and decreases gradually with pitch. For bigger pitches $p = 1\ \mu\mathrm{m} - 3\ \mu\mathrm{m}$, k_s becomes less significant and saturates. This behaviour is in accordance with experimental observations of the diffusion length of adatoms on the growth substrate which is in the order of $\lambda_\mathrm{s} = 0.75 - 0.8\ \mu$m [66, 125]. This is similar to the value extracted from observing the NW volume dependence on pitch, as shown in Fig. 4.3b. Accordingly, for rather large pitches, with $p > 2\lambda_\mathrm{s}$, the amount of material supplied to each NW from the surface diffusion is limited by λ_s and becomes pitch independent. Thus, the sources contributing to the vertical growth of nanowires are mainly the direct incorporation of adatoms at the wire apex and the side-wall diffusion of adatoms through direct impingement on nanowire side-facets.

By changing the growth process parameters, the surface diffusion length can be tuned. More specifically, the growth temperature has a significant impact on the diffusion length of adatoms on the mask surface. The diffusion length is described by the following equation [127]:

$$\lambda_\mathrm{s} = \sqrt{\mathrm{D_s t_s}} \tag{4.12}$$

where $\mathrm{D_s}$ is the diffusivity coefficient and $\mathrm{t_s}$ is the average time of the adatoms on the mask surface. $\mathrm{D_s}$ is proportional to the squared velocity of the diffusing adatoms and is exponentially dependent on temperature [127]. The exponential dependence on temperature implies that the diffusion length of the adatoms on the dielectric mask can be adapted based on the choice of the growth temperature. More specifically, if the growth temperature is high the surface diffusion is enhanced. However, such high temperatures also enhance the desorption of atoms from the surface as well as from the growing wires, which could result in shorter NWs. The enhanced desorption is captured by the direct incorporation coeffcient. It is expected to be smaller for enhanced desorption. In

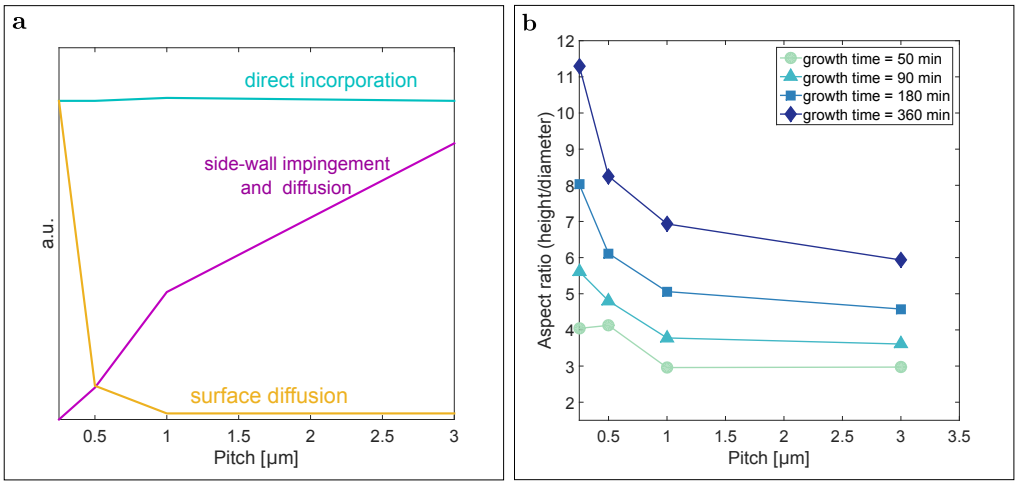

Figure 4.6: The three coefficients representing the different incorporation from the different adatom sources and their dependence on pitch

contrast, low growth temperatures, would result in shorter diffusion lengths on the mask surface and higher sticking coefficient of incoming atoms to the growth sample, resulting in the occurrence of parasitic clusters on the mask. This would imply the growing nanowires would compete with parasitic clusters for the incoming adatom supply, which could result in shorter nanowires compared to a parasitic clusters-free surface. Parasitic clusters are anticipated to mainly affect the surface diffusion coefficient and the side-wall contribution the NW growth. Particularly, surface diffusing adatoms would be captured readily in parasitic clusters and would be thus inhibited from reaching the growing NWs and contributing to both the axial and lateral growth. Side-wall impinging atoms on the other hand, are dependent on the cluster density and size. A high density of clusters with rather big sized clusters is predicted to promote shadowing and hence diminish the input of the side-facet incoming adatoms to the NW growth.

The influence of growth process parameters on the growth kinetics are thus accounted for in the derived model implicitly through the diffusion length, λ_s, as well as the three coefficients, describing the relative contributions to the NW axial growth.

4.3.3.2 Pitch and growth time dependence on nanowire aspect ratio

Seeing as the highest nanowires were obtained for the bigger pitches, it is rather counter-intuitive that nanowires grown on substrates with the smallest pitches would result in nanowires with the highest aspect ratios (height/diameter). As illustrated in Fig. 4.6b the aspect ratio saturates for pitches starting $p = 1$ μm, irrespective of the growth duration. Furthermore, smaller pitches exhibit high aspect ratio nanowires, which increase with growth duration. In fact, the highest aspect ratio is achieved for wires synthesized with a pitch equal to 250 nm for the longest growth duration investigated, namely six hours. This observation reveals that for rather limited inter-wire spacing, where nanowires compete for the incoming adatoms, adatoms supplied to the wire apex through direct impingement significantly contribute to the axial growth, as indicated in Fig. 4.6a. Additionally, the shadowing that plays a dominant role for reduced inter-wire spacing reduces the radial growth rate with time evolution. Thus leading to enhanced shadowing, where continuously less adatoms are able to reach the nanowire-side walls through direct impingement, as previously discussed. For bigger pitches, starting $p = 1$ μm, the aspect ratio seems to saturate, seeing as the contribution from the surface diffusion is negligible. Accordingly, the NW growth is driven by the direct incorporation from the top as well as the side-wall impingement and subsequent side-wall diffusion. Seeing as the direct direct incorporation from the NW is apex, is almost the same irrespective of pitch and the significantly reduced shadowing for bigger pitches, explains the almost constant aspect-ratio for the non-competitive regime. Another conclusion to be drawn from Fig. 4.6b is that the growth rate of NWs increases with growth time. This is expected since the integration of the fixed growth rate, which could be described by a uniform distribution function,

would yield more atoms in total if the integration interval, in this case the growth time, is longer.

4.4 Conclusion

The investigation of nanowires grown via SA-MBE deems to be a promising method for the bottom-up fabrication techniques and large scale manufacturing of semiconductor NWs. A theoretical model has been developed and accounts for both the axial and radial growth of nanowires. The adatoms driving the vertical growth of nanowires are divided into three main sources. The model captures a functional relationship between the process parameters, nanowire size and growth duration. The model is derived for nanowires grown via SAE in an MBE system. Fitting the model to experimental data confirms that the model provides an interpretation of the kinetics taking place during nanowire growth. Moreover, the model provides insights to SAE growth mechanisms as well as adatom diffusion in SAE-MBE synthesis. The diffusion length of the adatoms on the growth substrate as well as inter-wire spacing are found to be the key parameters for achieving high aspect ratio nanowires. It is shown that the smallest pitches result in nanowires with highest aspect ratios, although they exhibit the shortest wires. The clear pitch dependence of the synthesized wires indicates, that the pitch choice to achieve positon-controlled and ordered arrays of nanowires is found to be even more prominent than the actual growth parameters, such as temperature and V/III ratio. The model presented here is general for SA-MBE and can be applied to optimize the size of nanowires and achieve high aspect ratio wires. The analysis and investigation of InAs nanowires synthesized for different pitches and understanding the kinetics of the growth process serves as a potential for optimizing the integration of III/V devices on silicon.

5

Top-Down Approach for Fabricating In-plane InAs NWs

Epitaxial nanowires fabricated in a planar arrangement open potentials for large-scale device integration, while mitigating structural defects associated with free-standing vertical NWs. A top-down approach for the fabrication of horizontally-aligned InAs nanowires is discussed in this chapter. This approach provides a simple and versatile method for producing position-controlled and planar high-quality, crystalline NWs.

5.1 Challenges Associated with Bottom-Up Fabrication of Nanowires

Defect-free III−V material integration on Si is a holy grail, which has been persistently endeavoured for the past 40 years. As presented in the previous chapters, III − V NWs have certainly brought the semiconductor industry closer to this grail. Their ability to circumvent substantial defects associated with conventional thin film epitaxy of III−Vs on Si as well as the possibility to synthesize them utilizing bottom-up techniques, thus beating the fundamental physical limits of conventional lithography, has opened up opportunities for the monolithic integration onto the Si platform.

Grievuously, III − V NWs synthesized utilizing bottom-up techniques occassionally embody stacking faults (SFs), which originate due to alternation of different crystal structures along the NW axis. In particular, it is commonly observed that the crystallographic structure of InAs NWs and other III−V NWs is strongly prevailed by the hexagonal wurtzite (WZ) structure, in contrast to the bulk and two-dimensional growth which strictly exhibits the cubic zinc blende (ZB) structure [144]. Although in bulk form, III−V materials crystallize strictly either in the ZB or WZ crystal structure, the energy difference between the two crystal phases in many of these compounds is small, in the order of 10 meV/atom for bulk InAs, for instance [145]. As the dimensions of the system are reduced, the surface energy dominates, causing the WZ crystal structure to become energetically more favourable. In fact, this transition has been reported to occur for (111)-oriented InAs NWs at a critical diameter of 10 - 20 nm [146]. For NWs with somewhat larger lateral dimensions, variation between ZB and WZ may take place over nanometre length scales, yielding structural defects at the phase boundaries (twin-plane defects) [147]. Though preliminary studies indicate that SFs might be harmless to the electronic conduction, they are considered to be detrimental to carrier lifetime and ballistic transport along the NW axis as well as photoluminescence properties, thus degrading the performance of NW-based optical devices [144, 145, 148]. Although a lot of effort has been granted to synthesizing defect-free NWs, the quest for stacking-fault-free NWs remains a major challenge [144, 148].

Another major challenge associated with bottom-up out-of-plane NWs is related to post-growth processing required for large-scale device applications [149]. In particular, wafer-scale integration of vertically-aligned NWs necessitates the development of effective means for transferring NWs onto functional device substrates while maintaining control over position and alignment, to facilitate subsequent device fabrication steps. Although, *ex situ* assembly methods have been developed to transfer and coarsely align the NWs in plane on device substrates, they lack control over position of individual wires on the wafer scale [149, 150].

Developing top-down methods (producing minuscule nano- or micro-structures by carving or

etching bulk materials) for producing NWs can result in position-controlled and aligned planar NWs free from twin-plane defects. Etching NWs from high-quality epitaxial thin-film layers, provides thus the possibility of obtaining supreme-quality NWs with well-controlled crystallinities and dimensions. Subsequent transfer of these planar wires onto functional device substrates with good reservation of arrangement and crystallographic orientation opens opportunities for large-scale, high-performance electronic systems and devices that depend upon integration of enormously different material systems.

5.2 Top-Down Fabrication Process

The top-down approach applied to achieve aligned, positioned and planar high-quality InAs NW arrays, includes four major steps: the growth of high quality III − V epitaxial layers (epilayers) on a GaAs (100) wafer, from which the wires are etched, defining photoresist patterns on the (100) epitaxial layers and eventually chemically etching the epilayers through the photoresist patterend mask. Finally, transfer of the wire arrays from the source substrate to functional device substrates.

5.2.1 Epitaxial Growth of InAs Thin Films on (100) GaAs substrates

As discussed in chapter 1 (see section 1.2), the direct thin film growth of III − V materials on Si suffers from many structural defects as a result of thermal and lattice mismatches between both material systems. One possible way of successfully growing high-quality III − V epilayers, is to utilize substrates with similar lattice and thermal parameters. Gravely, the cost of such substrates is rather high, e.g. more than 1000$ for a 4-inch indium phosphide substrate [151]. Even though GaAs is not lattice-matched with most III − Vs, GaAs wafers are availabe in large diameter wafers and are less expensive than most of the III − V material substrates, e.g. a 6-inch GaAs wafer costs around 450$, thus are commonly used for growing hig-quality III − V epilayers [151–153]. In fact, a potential solution to the cost-quality predicament associated with the growth on the somewhat lattice-mismatched GaAs substrates, is to deposit the critical device layers (InAs in the given case) on top of a so-called metamorphic buffer. Metamorphic buffers are basically a few μm to mm-thick layers with compositionally graded indium content to allow for the expansion of the lattice constant from that of GaAs to the device layer [139, 153]. The metamorphic buffer absorbs the strain of the lattice mismatch and contains most of the structural defects created

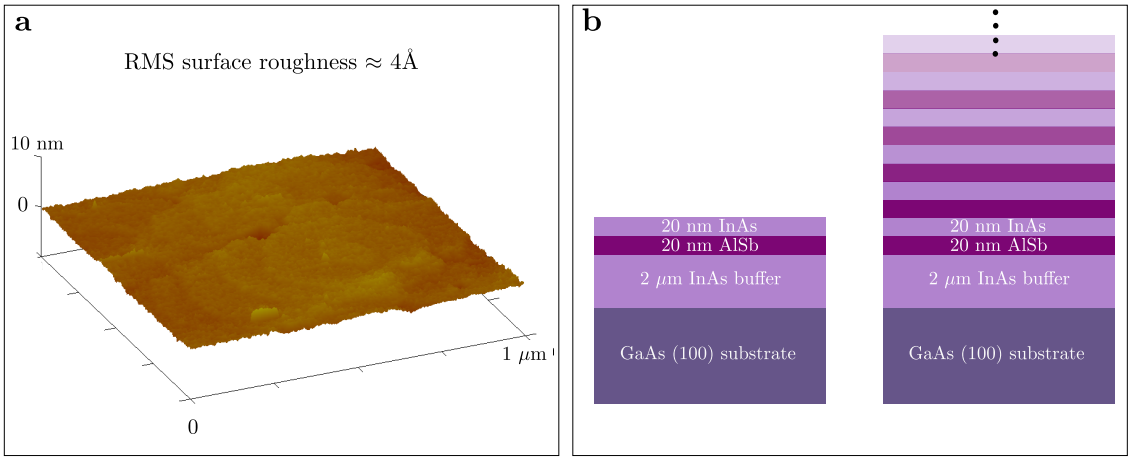

Figure 5.1: a. AFM measurement of the top InAs epilayer surface showing a root-mean-square (RMS) roughness of 4 Å, as determined by the AFM surface map. b. The right schematic depicts the epilayer structure of the substrates used to pattern the InAs NW arrays. The left schematic illustrates the possibility of creating several device layers per wafer, in which AlSb serve as sacrificial layers.

during the transformation of the lattice constants, thereby preventing the propagation of vertical dislocation defects and preserving the quality of the critical layers [152, 153]. It is worth noting, that although GaAs substrates are more cost effective with respect to other $III-V$ material substrates, the use of layered epitaxial films on top of non-silicon wafers for generating top-down nanowires typically increases the fabrication cost due to the high price associated with these kind of wafers, as compared to Si. Nevertheless, the process developed here allows for the multiple use of the GaAs wafers, thus effectively reduces the fabrication cost.

GaAs substrates with (100) crystal orientation are used to grow the desired epilayers using molecular beam epitaxy. A 2 μm-thick InAs metamorphic buffer is grown on top of the GaAs substrate surface. On top of the metamorphic buffer, is a 20 nm-thick aluminum antimonide (AlSb) sacrificial epilayer, followed by a 20 nm-thick InAs top layer, as illustrated in Fig. 5.1b. The AlSb epitaxial film is almost lattice-matched with InAs, as illustrated in Fig. 1.3, thus is expected to preserve the lattice constant of the few atomic top layers of the metamorphic buffer, hence yielding high quality InAs top layer, as signified by the low surface roughness (see Fig. 5.1a). Basically, the AlSb layer serves two main purposes. On the one hand, InAs can be etched with high selectivity with respect to AlSb [154, 155], allowing AlSb to act as an etch-stop layer during the chemical etching step, thus enabling the patterning of the InAs top layer. On the other hand, the etch selectivity between the AlSb and InAs material systems provides the possibility of creating multiple AlSb-InAs layers, in which AlSb merely serves as a sacrifical layer, thus yielding several device layers on the same GaAs substrate (see Fig. 5.1b). The latter thus effectively reduces the fabrication cost of the InAs NWs associated with one GaAs wafer.

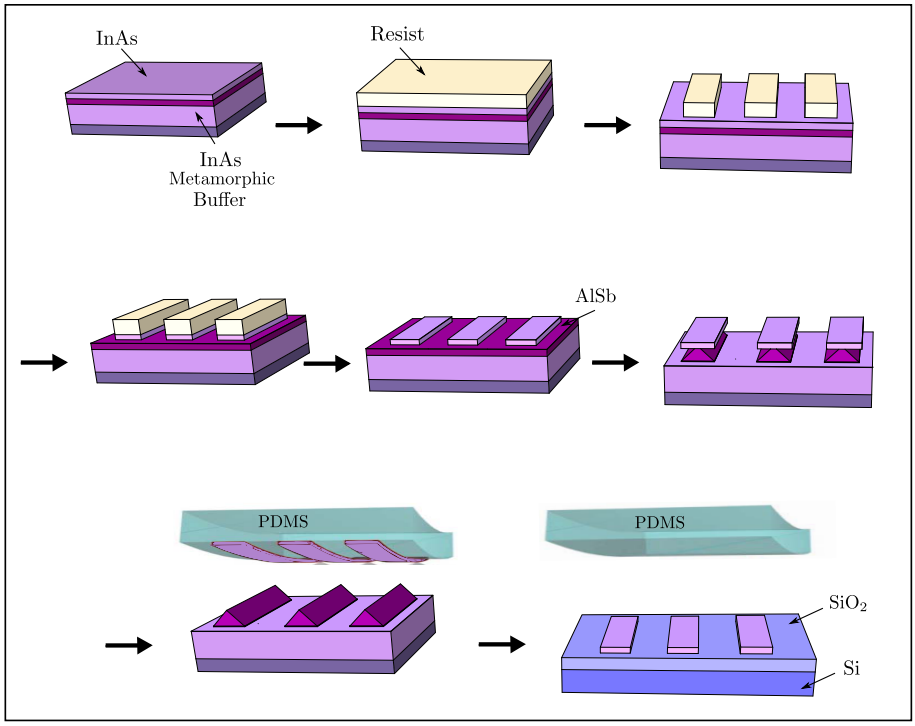

Figure 5.2: Fabrication Process. A resist covers the surface of the InAs epialyer via spin coating for subsequent patterning and exposure. After resist patterning via exposure and development, the resist patterns are used as an etch mask to selectively etch the underlying InAs film with respect to the sacrificial AlSb layer. The resist is subsequently removed in acetone, yielding planar-aligned InAs NWs on top of the AlSb etch stop layer. In order to release the etched NWs, the AlSb is etched selectively with InAs to yield an over etched profile in the lateral direction, thereby minimizing the contact area with the InAs structures. Next, an elastomeric PDMS slab is brought in contact with the InAs surface to peel off the etched wires. Finally, the etched wires are transferred to the SiO_2/Si functional device substrate.

5.2.2 Defining Photoresist Patterns

The fabrication process of the in-plane InAs NWs relies on a lithography step that will transfer the desired pattern onto a photoresist, which will eventually be used as an etch mask. Fig. 5.2 depicts the detailed fabrication process for producing the NWs from the high-quality InAs thin film and their subsequent transfer onto the functional device substrate. For further details regarding the fabrication process and materials, refer to Appendix B.

The pattern design is composed of parallel lines, whose size varies between $100 - 300$ nm in width, whereas their length is fixed at 2 μm. The inter-pattern spacing is 10 μm, to allow for facilitated probing of individual wires. The pattern drawing performed in a computer-aided design (CAD) tool was subsequently converted into file formats compatible with the electron-beam (e-beam) lithography tool. Once the substrates were cleaned and dried, an approxiamtely 300 nm-thick film of ma-N2403, a methacrylate-based negative e-beam resist, was uniformly applied to the substrate surface by spin-coating for 30 seconds at 3000 rpm. The coated substrates are then baked at 115°C for 1 minute prior to their loading into the e-beam lithography system. A JEOL JBX-9300FS e-beam system [156] with 50kV accelerating voltage gun emitter was used to transfer the pattern design by direct writing on the negative tone resist. The resist film was exposed with an exposure dose equal to 120 μC/cm^2, to achieve an array of parallel lines corresponding to the pattern design. After exposure, development of the resist in the alkaline developer, MF-CD-26, for 40 seconds and subsequent rinsing in deionized water took place. More specifically, developing the non-exposed regions (non-cross-linked resist regions) of the negative resist, yielded an array of parallel resist lines on the substrate surface. The resist thickness was confirmed after development by measurements performed on cross-shaped alignment markers on the substrate using a mechanical stylus profilometer. The obtained thickness is in agreement with the thickness given in the chart provided by the manufacturer for the same spin-rate [157]. The exposure dose and development time were chosen based on dose test experiments performed a priori.

The patterned lines act as an etch mask for the subsequent anisotropic wet chemical etching step. Thus the choice of the resist should account for the resists' ability to withstand the chemical etchant, which has been confirmed by performing etch resistance tests, during which wafers with patterned resists were immersed in the etchant for durations longer than required for the etching step. Pattern size was retained as in the original design and no erosion was observed, as previously reported [158]. One more consideration that should be accounted for is the adhesion of the resist to the substrate surface. Poor adhesion could result in the resist falling on its side, as indicated in Fig. 5.3. and more importantly, poor adhesion could lead to non-uniformities during the wet etching step, as the etchant would be able to reach poorly adhered surfaces more efficiently, yielding rough edges of the etched wires, as indicated in Fig. 5.3. In accordance with previous reports indicating poor adhesion of this resist on various substrates [159, 160], hexamethyldisilazane (HMDS) primer was spin-coated prior to resist coating to promote adhesion [161]. It is worth mentioning, that although the yield and adhesion of the bigger structures (width $= 200-300$ nm) was enhanced with the application of the HMDS, the 100 nm-wide structures did not show significant improvement in yield. This could be related to the smaller contact area with the substrate surface for the smaller structures, as well as the higher aspect ratio (resist thickness/structure width) for the 100 nm-structures, facilitating their collapse.

5.2.3 Etching the InAs Nanowires

The etchants for InAs are typically prepared by mixing acids (e.g. hydrofluoric acid, hydrochloric acid or citric acid) with oxidants, e.g. hydrogen peroxide (H_2O_2) [162]. The experiments in the work at hand utilized a mixture of citric acid ($C_6H_8O_7$) and hydrogen peroxide. The choice of this acid and mixture specifically is based on its compatibility with the used resist, its good etch selectivity with AlSb and uniform etching profiles [158, 162]. The etch rate is defined as the thickness of the material removed divided by the etch time. The etch selectivity on the other hand, is defined as the ratio between the etch rate of material 1 and material 2, where in the given case material 1 is InAs and material 2 is AlSb, implying that the higher the ratio, the better the etch selectivity.

The chemistry of etching a selection of $III - V$ semiconductors using acid-hydrogen-peroxide-mixtures has been reported to proceed by the oxidation of the semiconductor surface via H_2O_2

followed by a dissolution of the oxidized products by the acid [162–164]. In fact, DeSalvo et. al tested this claim by measuring the etching depths of $III-V$ materials soaked in each etchant component alone for a duration of 5-8 hours. No measurable etch depth was noted, thus confirming the chemistry of the etching process.

The etchant mixture was prepared by dissolving anhydrous citric acid crystals in deionized water at a ratio of 1g $C_6H_8O_8$: 1ml H_2O. Seeing as the dissolution reaction is endothermic and thus impedes rapid liquefaction, the mixture was prepared one day in advance to guarantee uniform dissolution and temperature stability of the mixture [162]. Roughly half an hour before performing any etch experiments, the prepared citric acid solution is mixed with 30% H_2O_2 at a volume ratio of 1 $C_6H_8O_7$: x H_2O_2, where x signifies that the volume fraction of H_2O_2 was varied. The waiting time of approximately 30 minutes is to ceritify the mixture is harmonized and its temperature is stabilized in case any temperature fluctuations occurred during the mixing procedure [162]. Furthermore, the variation of the volume fraction is performed to determine the optimum etch rate and selectivity for the InAs NWs. In fact, it has been reported that the volume ratio of the etch components has a direct influence on both etching criteria, as indicated in the plots of Fig. 5.3b. An examination of the plots indicates, that the etch rate initially increases with an increase of volume ratio. However, at a volume ratio equal to roughly 2, the etch rate shows the opposite behaviour for increasing volume ratios. This observation can be attributed to the processes governing the etch process. In particular, originally when the volume ratio is less than one, implying that the oxidizing agent is abundant, the etching rate is limited by the dissolution process performed by the acid. Accordingly, as the volume fraction of $C_6H_8O_7$ is increased, the etch rate is elevated. This remains valid, until the oxidizing rate and dissolution rate are comparable, which occurs at a volume ratio of about 2. As the the volume ratio is further increased, the etch rate goes down, seeing as it is limited by the oxidation of the semiconductor surface. More specifically, as the volume ratio increases, implying a decrease in the H_2O_2 volume fraction, less material is oxidized and ergo dissolved thus yielding a lower etch rate.

Additionally, observation of the plots stipulates that the highest etch selectivity is achieved for a volume ratio equal to 1. Applying this volume ratio in etching experiments of bulk InAs (2 μm layer) grown on top of GaAs (100), yielded an etch rate of approximately 80 nm/min in agreement with the data reported in [162]. Nevertheless, a volume ratio of 0.5 was chosen for all etch experiments presented in this work. The choice of this ratio, is attributed to previous studies reporting that etching that proceeds with the removal of an oxidized layer by the acid yields improved control on the etching process as well as reduces surface roughness [165, 166].

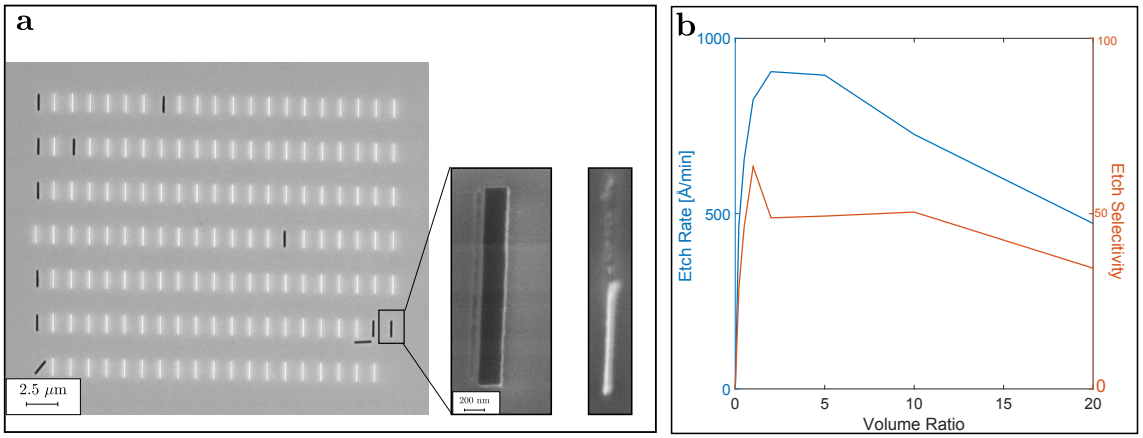

Figure 5.3: a. SEM image performed for a dose, indicating same fallen resists due to poor adhesion. A zoomed in image showing the resist collapsing. Furthermore, an SEM image is provided for showing the effect of poor adhesion on NW etching. In particular only the lower half of the wire survived the etching. Due to poor resist adhesion the etchant was able to successfully de-laminate the top half of the resist, causing the NW to be halfway etched. b. Etch rate and etch selectivity for InAs and InAs/GaSb respectively as a function of volume ratio (citric acid/hydrogen peroxide) , data extracted from [154]

Correspondingly, to maintain a high etch selectivity, while increasing the volume fraction of the oxidizing agent, 2 parts H_2O_2 were mixed with one part $C_6H_8O_7$. All etching experiments were performed at room temperature and yielded reproducible results. In fact, this volume ratio yielded a reproducible etch rate of about 30 nm/min, which is lower than what is reported in [162]. The difference in etch rates could be assigned to a difference in InAs film quality. As a matter of fact, in the proximity of structural crystal defects, the rate at which the material is etched can be higher in comparison to defect-free regions, due to a lower chemical stability of defective regions [165]. The quality of the InAs films etched in this work are expected to be significantly higher, as they were grown on top of a metamorphic buffer. In contrast, the etch rate reported in [162] for InAs is calibrated for layers grown directly on GaAs(100)surfaces, thus are expected to embody structural defects, which in turn could explain the higher etch rate. In regards, to etch selectivity between AlSb and InAs, this has shown to be extremely high. This was confirmed by measurements of the InAs nanostructures. The height of these structures was comparable to the layer thickness expected by the MBE thin film growth as calibrated by the In growth rate. More specifically, if the height of the nanostructures was measured to be higher than the layer thickness, this would have signified that AlSb is being substantially etched during the InAs etching. The high etch selectivity between the two material systems has been previously reported [162]. Although the etch selectivity depicted in Fig. 5.3b is for GaSb, even higher selectivities are expected for AlSb [162]. In fact, it has been outlined, that antimony containing semiconductors are etched with very low rates in citric acid/hydrogen perdoxide mixtures. This effect is further enhanced if the compound semiconductor contains aluminium, accordingly AlSb is expected to have extremely low etch rates in this solution [162]. Determination of the AlSb etch rate is not straightforward, seeing as this material oxidises fairly easy when exposed to air and OH^--ions, thus forming aluminum-oxides. The disintegration of this material results in the formation of an elemental antimony layer which oxidises more slowly, thus significantly reducing the etch rate of this material. In GaSb systems, the Ga atoms are more stable, yielding more stable reaction rates for both consitutent elements, yielding measurable etch rates [167]. Nevertheless, the high etch selectivity between InAs and Alsb, renders AlSb a very efficient etch stop layer, allowing controllable etching of InAs.

It is noteworthy that the crystal orientation plays a major role in the morphology of the etched structures due to different etch rates along the different crystallographic orientations. The anisotropy of etching (unequal etch rates in different directions) emanates from differences in energy and chemical resistance along the different crystal orientations [168]. In particular, crystal planes with the lowest energy and higher density of atoms are more stable, thus exhibit higher chemical resistance, and in turn lower etch rates [169]. For the zinc blende InAs crystal strucutre, where the atoms are arranged in the face-centred cubic lattice, the {111} planes show highest chemical stability [169]. Since the patterned resist lines were aligned along the $(01\bar{1})$ crystal direction of the GaAs (100) substrate, as depicted in Fig. 5.4, the anisotropic etching yielded mesa-shaped outlines (see Fig. 5.4). Particulrarly, as the etch rate is faster along the less stable and less atomically dense 100 planes as compared to the lateral etch rate of the more stable {111} planes. Furthermore, the schematic of Fig. 5.4 indicates that the nanowire surfaces are In-rich. As a matter of fact the In-rich {111} planes, commonly referred to as {111}A planes, are electron-deficient in comparison to As-rich {111} planes ({111}B). This electron-deficiency makes the surfaces more resistant to chemical oxidation, which renders them more difficult to etch, equivalently NW side-walls are In-rich [168]. In essence the anisotropic etching profiles are directly controlled by the choice of the orientation of the mask structures. Furthermore, the consensus of the acquired etching profiles with theoretical crystallography models signifies that the resist indeed is an efficient etch mask.

5.2.4 Transfer of the InAs on a Functional Device Substrate

As indicated in Fig. 5.2, in order to be able to transfer the InAs NWs, they need to be released from the source substrate. One way to achieve that, is to selectively etch the sacrificial AlSb layer with respect to InAs. Making use of the mesa-shaped etch profiles of the epitaxial AlSb layer, the etching can be carried out long enough, to reduce the contact area of the InAs NWs with the underlying AlSb layer, as indicated in Fig. 5.2, thus facilitating the release of the NWs from the surface. The etching of the AlSb was performed using a wet chemical etch step. The solution was prepared by diluting one part of hydrofluoric acid already diluted in 700 parts water, in five

parts ethanol [(1 HF : 700 H_2O_2): 1 : 5 ethanol]. The solution had a pH value of approximately 2.8. This solution specifically was reported to etch AlSb roughly 100 times faster than InAs, yielding very high etch selectivity [170]. The etch rate of this solution was easily determined, due to difference in colors between AlSb and the bottom InAs buffer. In fact, as the etching proceeds, the AlSb brown-reddish colored layer gradually fades and the etching stops at the InAs layer, which exhibits a a shiny faded blue-greenish color. Accordingly, this difference in morphology facilitates the identification of the AlSb layer. Moreover, further confirmation about the etch rate is acquired by performing profile measurements with a mechanical stylus profilometer on the cross-shaped alignment markers. These yielded a total height of roughly 40 nm, which correspond to the additive height of the two InAs and AlSb top layers (see Fig. 5.1). Consequently, the etch rate was determined to be about 0.5 nm/s, in agreement with the value reported in [170].

Following the partial etch of the underlying AlSb layer, an elastomeric polydimethylsiloxane (PDMS) slab was used to detach the partially released InAs NWs from the source substrate. The PDMS sheet was prepared by mixing a PDMS prepolymer with a curing agent (Sylgard 184, Dow Corning) at a ratio of 1:10. Next this mixture was poured onto a silicon wafer modified with a monolayer of (tridecafluoro-1,1,2,2-tetrahydrooctyl)-1-trichlorosilane. This monolayer serves the purpose of facilitating the subsequent releases of the PDMS sheet [171]. The silicon substrate with the PDMS layer was stored under ambient conditions away from direct light exposure for 38 hours. This yielded a sticky and elastic PDMS layer. It is worth noting, that curing the PDMS layer in an oven at 400°C for 4 hours, resulted in a much harder PDMS layer, that was relatively rigid and difficult to manage. Next, a rectangular slab was cut from the 38-hour-cured PDMS layer and brought into contact with the surface of the source substrate. The soft and compliant nature of PDMS allows its initimate contact with the source substrate. It has been reported that PDMS is able to stick to various materials and surfaces, as it relies on van der Waals interactions (non-specific interactions) [172]. Now that the PDMS slab is in contact with source substrate surface, bubbles forming between the PDMS and the surface are eliminated by gentle pressing and stroking of the PDMS. The PDMS slab was left on the surface for about 10 seconds. Next, the PDMS was peeled of the surface and transferred to a functional device substrate, SiO_2/Si substrate in the given case. Grievously, examination of the source substrate with optical microscope as well as SEM and the PDMS layer (now in contact with the functional device substrate), indicated that

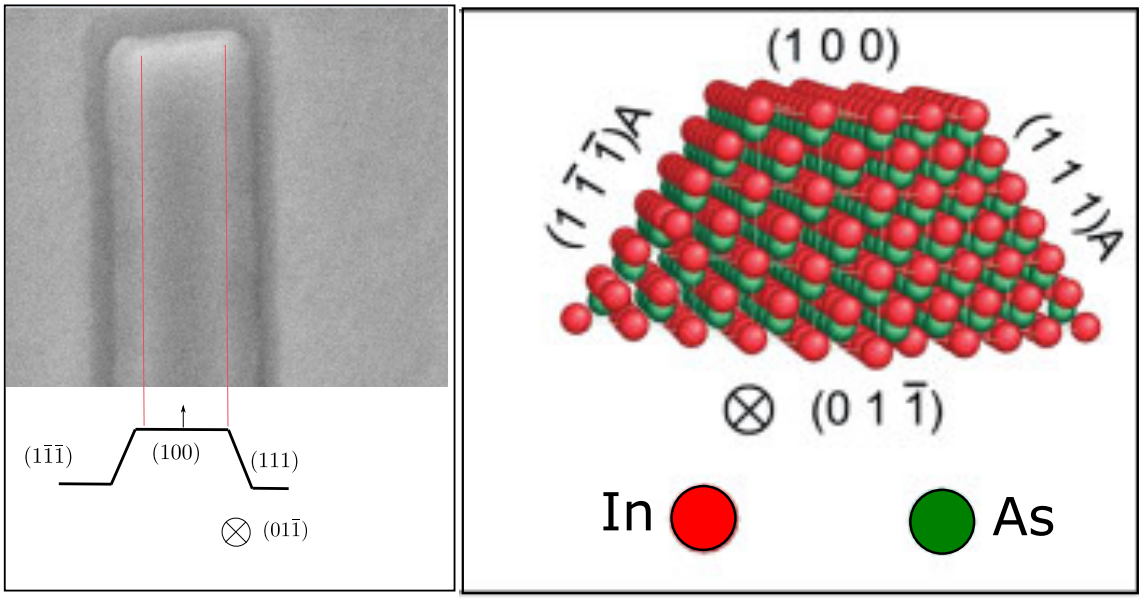

Figure 5.4: SEM image indicating the profile of the etched InAs NWs in confirmation with the crytal orientation. The schematic illustration below the SEM image is used as guidance and illustration purposes, indicating the different crystal planes. This illustrative schematic is further clarified using an illustration of the three dimensional arrangement of In and As atoms within the etched structure. Adapted from [168].

the etched NWs were not successfully released from the source substrate.

The unsuccessful transfer could be attributed to one of two factors, either the PDMS peeling step or the lateral over etching of the AlSb layer. In particular, Meitl et. al, performed various experiments to quantify the transfer efficiency of micro- and nanostructures via PDMS peeling. Their studies indicate that the transfer efficiency is highly dependent on the speed by which the PDMS slab is ripped from the surface. In fact, a slow peeling rate is not able release the structures from the source substrate because the separation energy for the interface between the nanostructures and is much greater than the separation energy between the PDMS and the structures. Thus, increasing the peeling rate, increases the separation energy between PDMS and the structures, while the substrate separation energy remains, fixed, allowing successful release [173]. In this regard, further optimization with the peeling process is needed. Nevertheless, the reason for the unsuccessful transfer is more likely attributed to the poor lateral over etching of the AlSb layer. In fact, although the observed and reported etch rate of the AlSb layer is quiet high (AlSb is removed within 40-45 seconds), longer etch times seem to have no measurable effect on the AlSb layer. As a matter of fact, the samples were soaked in the AlSb etch solution for one hour, which is expected to completely etch away the AlSb elongated pyramid shaped structures, on which the InAs structures reside (see Fig. 5.2), thus collapsing the completely removing the InAs NWs. However, after one hour of soaking the in the etchant, the structures were still intact, as confirmed by profiler measurements as well SEM analysis. Accordingly, it appears as though the lateral etching is extremely slow or even non-existent. In this regard, further investigation is required to explain the failed release of the etched InAs NWs.

6
Conclusion and Outlook

In this thesis both bottom-up and top-down synthesis of catalyst-free InAs nanowires (NWs) on Si substrates are demonstrated. In this regard, the growth technique used to synthesize the NWs, molecular beam epitaxy (MBE) is presented together with the associated *in situ* growth monitoring methods, namely reflection high-energy electron diffraction (RHEED) and quadrupole mass spectrometry (QMS).

The bottom-approach relies on selective-area epitaxy on lithographically patterned SiO_2-masked Si substrates. The substrate patterning is achieved via two techniques, colloidal lithography (CL) and hole-mask colloidal lithography (HCL). Both techniques rely on the self-assembly of colloidal nanometre-sized particles on a surface, yielding short-range ordered patterns. The size of the particles is easily controlled, yielding flexibility in fabricating masks with differently-sized nanoapertures. Specific to this work, the two techniques presented allow for fabricating masks composed of different oxide types. More specifically, CL provides a method for fabricating masks composed of evaporated silicon-dioxdie, whereas HCL allows for fabricating templates on high-quality thermally grown silicon dioxide. The effect of the oxide quality on the NW growth is investigated, showing that growth selectivity is enhanced for the high-quality oxide. Nevertheless, the oxide mask quality is not the sole contributor to the enhanced selectivity, the growth parameters have shown to have a prominent impact on selectivity as well.

In this context, the patterned Si samples using these large-scale, high-throughput, cost-efficient patterning techniques have been used for the growth of site-selective, vertically-oriented InAs NWs. The catalyst-free growth of NWs on patternd substrates proceeds via selective-area epitaxy, where the selectivity is mainly achieved due to different properties between the typically amorphous mask and the crystalline substrate, resulting in the preferential nucleation of NWs within the nanholes. Advantages of this growth technique include the possibility of acquiring positioned NWs, as well as the possibility to mitigate the dependence on a catalyst to drive the growth, thus ensuring high purity NWs. Basic investigations of the synthesized NWs by means of scanning electron microscopy (SEM), revealed that the NWs had a hexagonal cross-section and were vertically-oriented with respect to the horizontal, confirming the epitaxial relation with the underlying (111)-oriented Si substrates. Varying growth temperature, In-flux and V/III ratio provided insight on the size-scaling behavior of NWs in response to different growth parameters. In essence, lower growth temperatures and higher V/III ratios yield high-aspect ratio wires. Although low growth temperatures enhance the nucleation of parasitic clusters, these are observed to be reduced for growth under arsenic-rich conditions. Furthermore, under In-limited conditions, NWs are observed to scale proportionally with the In-growth rate.

Further investigations of the quality of the obtained NWs using post-growth analysis techniques is essential to evaluate the performance prospectives of the obtained wires in device applications. Post-growth analysis includes electrical transport measurements, x-ray diffraction (XRD) as well as cross-sectional transmission electron microscope (TEM) analysis to assess the crystalline quality of the grown NWs. Furthermore, photoluminescence response of the NWs should indicate their prospect in being utilized in optoelectronic-based devices. Such assessment should be able to provide a guideline for further optimizing the growth parameters to obtain high quality NWs.

Insights on the growth kinetics governing the bottom-up synthesis of InAs nanowires using selective-area molecular beam epitaxy are provided via the derivation and analysis of a theoretical growth model. This model accounts for the NW height and diameter evolution with time, as well as investigates their scaling trends in response to varying inter-wire spacing (pitch). In contrast to the majority of reported growth models in literature, where the NW lateral dimensions are considered

to be constant due to restriction by a catalyst-droplet or mask-opening size, this model accounts for the lateral overgrowth observed in SA-MBE. Hence, an analytical expression of the NW diameter as a function of time is derived. Within the framework of this model, NW axial growth is assumed to be driven by contributions from three main sources: direct incorporation of incoming atoms from the NW apex, side-wall impingement and diffusion as well as the contribution from surface-diffusing atoms on the NW mask. The model is fit to experimental data obtained from SAE of InAs NWs in an MBE system. Analysis of the model calls attention to three pitch-dependent regimes governing the NW growth kinetics, namely, a competitive regime, an intermediate regime and a non-competitive regime. The contribution from the direct incorporation of incoming atoms to the NW axial growth front is determined to be almost pitch invariant. In contrast, the side-wall contribution and contribution from mask surface-diffusing atoms are greatly dependent on the inter-wire spacing. More specifically, the side-wall contribution is rather insignificant for dense wire arrangements, where the pitch is rather small. In that case, the shadowing from neighbouring wires does not allow efficient side-wall impingement and subsequent diffusion. This shadowing effect is less prominent for bigger pitches, and thus allows the incoming atoms to have access to the NW side-facets. The contribution from mask surface diffusion is observed to show the opposite behavior. More specifically, for smaller pitches, surface diffusing atoms play a significant role in driving the NW growth, whereas for bigger pitches, the surface diffusion contribution becomes limited to the adatom surface diffusion length and thus is pitch-invariant for pitch values larger than double the adatom diffusion length.

Regarding the top-down approach developed for the catalyst-free, in-plane InAs NWs, this is based on the patterning and subsequent etching of high quality epitaxial InAs thin films. The InAs layers are epitaxially grown using MBE on top of a lattice-matched AlSb layer, which serves as an etch-stop layer in subsequent fabrication steps. The two thin films AlSb and InAs are grown on top of an InAs metamorphic buffer, which gradually bridges the lattice mismatch between the two epilayers and the underlying GaAs substrate. The InAs NWs are acquired via the patterning of a resist with electron-beam lithography. The wet chemical etching of the InAs top epilayer through the resist pattern yields horizontally aligned and ordered InAs NW arrays. The etching of the InAs NWs is stopped at the AlSb layer, due to a high etch selectivity between the two material systems. For the transfer of the obtained wires from the source substrate to a functional device substrate, the underlying AlSb is selectively etched with respect to InAs, in order to facilitate the release of the NW structures. An elastomeric PDMS slab is brought into contact with the sample surface to detach the InAs NWs from the source substrate via a peeling process. Grievously, the InAs NWs are not detached from the source substrate. This is likely attributed to an unoptimized peeling process, or more likely, to poor lateral over etching of the AlSb layer. The insufficient lateral over etch is assumed to maintain a large contact area between the NWs and the underlying substrate, impeding their detachment from the substrate. To confirm the latter, further investigations are required. One alternative, would be to examine the etching profile of the AlSb layer underneath the InAs via a cross-sectional SEM view.

The success of the transfer technique is expected to pave the way to wafer-scale integration of NWs, seeing as the wires are expected to be transferred without loss of arrangement or crystalline quality. Furthermore, it should allow the integration of enormously different material systems, thus opening up potentials towards novel device opportunities. In analogy to the InAs NWs obtained via the bottom-up synthesis technique, further characterization of the etched NWs is needed to evaluate their quality as well as physical properties, such as electron mobility and photoluminescence. Following these investigations, comparison between the structural and physical quality of NWs obtained via both the bottom-up and top-down techniques should be drawn and evaluated. This evaluation should provide a conclusion regarding the optimum utilization of the differently synthesized NWs depending on application requirements.

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A

Appendix

A.1 Fabrication of Nanohole Template on Si Substrates Using Colloidal Lithography

A.1.1 Substrate Preparation

A.1.1.1 Substrate Clean - Solvent Clean

Solvents are able to remove oily or organic residues that appear on Si or silicon dioxide surfaces. However, since solvents themselves leave their own residues on the sample surfaces (especially acetone), a two-solvent wash is used, accordingly:

- Soak Si samples in acetone-filled clean beaker for 5 minutes
- Transfer samples from acetone to isopropyl alcohol (IPA) and keep for 5 minutes
- Transfer the two-solvent-washed substrates in a beaker filled with deionized (DI) water and keep for 5 minutes
- Rinse the samples with DI water once more and dry with a nitrogen (N_2) flow

A.1.1.2 Oxygen Plasma Treatment for Enhancing Surface Hydrophilicity

Reactive oxygen O_2 plasma treatment with a Plasma Therm Batchtop RIE

- Power = 50 Watt
- Pressure = 250 mTorr
- O_2 flow rate = 10 standard cubic centimetre per minute (sccm)
- Duratioin = 60 seconds

A.1.1.3 Formation of the Colloidal Monolayer

Positively charge the sample surface in order to allow the self-assembly of the negatively charged colloidal beads. The surface is charged via a layer by layer process as follows:

- Drop-cast a triple layer of alternating polycation/polyanion solutions, while terminating with the polycation solution to ensure a positive surface charge, accordingly the layer labelled '1.' is the bottom layer:

1. Polyelectrolyte layer (positively charged): polydiallyldimethylammonium (PDDA) (Sigma Aldrich, 0.2 wt % in Milli-Q water, Millipore)

2. Polyelectrolyte layer (negatively charged) : Poly(sodium 4-styrene sulfate) (PSS) (Sigma Aldrich, 2 wt % in Milli-Q water, Millipore)

3. Polyelectrolyte layer (positively charged): PDDA

- After the deposition of each layer, let it adsorb for roughly 30 seconds. Carefully rinse the substrate after the adsorption of each layer with DI water to remove excessive, unadsorbed polyelectrolytes. The rinsing is followed by blow-drying the sample under a flow of nitrogen.

- A water suspended solution containing negatively charged spherical polystyrene (PS) nanoparticles with average diameter of about 100 nm (sulfate latex, Interfacial Dynamics Coorporation, 0.2 wt % in Mili-Q water) is pipetted on the polyelectrolyte positively- charged-Si surface and let it adsorb for roughly 2-3 minutes to ensure a uniform colloidal monolayer.

- Rinse the samples with DI water to expel unadsorbed and poorely adsorbed PS beads.

- Blow-dry the samples with an intense N_2 stream perpendicular to the sample surface to avoid colloidal aggregation via capillary or hydrodynamic forces.

- Expose the short-range ordered PS particles to reactive oxygen plasma (50 W - 250 mTorr - 10 sccm) for 30 seconds to shrink the PS bead size from about 100 nm to roughly 60 nm.

A.1.2 Nanohole Template Creation

The PS beads are used as an evaporation mask. Accordingly, a 24 nm-thick SiO_2 film is evaporated (deposition rate ≈ 0.2 Å/s) from vitreous quartz pieces contained in a tantalum crucible via at 4 kW electron beam in the vacuum environment ($P < 10^{-5}$ mbar) of the AVAC HVC600 multi-material evaporator system.

In order to get nanoholes within the evaporated SiO_2 film, the PS particles are stripped using tape (SWT-10 tape, Nitto Scandinavia AB). The tape stripping is repeated three times per sample to ensure the removal of all particles.

Following the tape stripping, the samples were exposed one final time to reactive oxygen plasma (50 W - 250 mTorr - 10 sccm) to remove residual polymers and organic residues originating from the charged layers.

Patterned samples are now ready for native oxide etching (please refer to section A.3) and subsequent loading to the molecular beam epitaxy (MBE) system for selective-area epitaxy (SAE) of nanowires (NWs).

A.2 Fabrication of Nanohole Template on SiO_2/Si Substrates Using Hole-Mask Colloidal Lithography

- Si samples with a 24 nm thick thermal oxide layer are used for the creation of the nanohole pattern.
- The samples are cleaned following the solvent clean procedure described in section A.1.1.1
- The thermal SiO_2 surface is activated in analogy to the procedure illustrated in section A.1.1.2
- Formation of the colloidal monolayer is likewise achieved via the process elucidated in section A.1.1.3

A.2.1 Hole-Mask Template Creation

In analogy to the colloidal lithography technique, the PS beads are used as an evaporation mask to define the hole-mask pattern. Hence, a 20 nm thick chromium (Cr) layer is thermally evaporated from a chrome-plated tungsten rod in the vacuum environment (($P < 10^{-6}$ mTorr) of the Lesker Nano 36 tool. Following the Cr evaporation, tape stripping is repeated three times to ensure the removal of PS beads, thus leaving behind a hole-mask pattern in the Cr layer. Analogous to the colloidal lithography procedure, tape stripping is followed by (50 W - 250 mTorr - 10 sccm) to remove residual polymers and organic residues originating from the charged layers.

A.2.2 Nanohole Template Creation

The nanohole pattern in the thermal SiO_2 layer is created via dry etching of the silicon dioxide through the Cr hole-mask. The dry etching is performed in an inductively coupled plasma/reactive ion etching (ICP/RIE) chamber of the Oxford Plasmalab 100 system. The etching of the SiO_2 layer through the Cr mask, was performed to ensure 1-3 nm SiO_2 are left in the bottom of the etched openings to avoid damage to the underlying Si substrate. A mixture of tetrafluoromethane (CF_4) and oxygen plasma are used to achieve anisotropic etching of the amorphous dielectric layer. The etch rate was calibrated for thermally grown oxide on Si. The following conditions were applied for the dry etching process:

- Power = 80 W
- Pressure = 10 mTorr
- O_2 flow rate = 10 sccm
- CF_4 flow rate = 50 sccm

- Duration = 65 seconds

Following the SiO_2 dry etch, a 3-minute reactive O_2 plasma (50 W - 250 mTorr - 10 sccm) is essential to remove the deposited fluorocarbon layer during the dry etching. The presence of this fluorocarbon layer inhibts the successful removal of the Cr mask.

The Cr mask is removed using a wet chemical etch based on a ceric ammonium nitrate solution, which is not reported to etch SiO_2 . Accordingly, the patterned, Cr masked samples are soaked in a Nickel-Chromium etchant for roughly 3 minutes (until change of color is observed, indicating complete removal of the Cr layer). The samples are then rinsed under a shower of DI water and blown-dry by a N_2 air flow.

After Cr removal, the samples are exposed one last time to reactive oxygen plasma (100 W - 500 mTorr - 40 sccm)for 3 minutes to ensure surface cleanliness and remove possible residual contaminants produced by the fabrication process.

Patterned samples are now ready for the few bottom nm oxide etching (please refer to section A.3) and subsequent loading to the MBE system for SAE NWs.

A.3 Substrate Preparation for MBE System Loading

The substrate patterning by either lithography technique requires the etching of the native/bottom oxide layer within the nanoapertures to allow the exposure of the underlying Si substrate. The exposure of the underlying Si substrate through the nanoholes is essential to SAE NWs. In fact, without this exposure NWs are not able to nucleate in the openings. The SiO_2 within the nanoholes is etched in a buffered hydrofluoric acid (BHF) ($HF:NH_4F:H_2O$) solution. In fact, this solution is diluted in DI water with a ratio of (1 $HF:NH_4F:H_2O$: 10 H_2O).

The etching rate is calliberated as follows:

The samples are soaked in 2-5 second intervals in the diluted BHF, until the Si layer is exposed. The exposure of the Si layer is confirmed by observing the clamped part of the samples. More specifically, during either the SiO_2 evaporation or the Cr evaporation, the samples are clamped to the substrate holder to immobilize them. For the SiO_2 evaporation, the clamped region is SiO_2-free, thus determination of the Si exposure is easily obtained due to the hydrophobic character of the Si surface in contrast to the hydrophilic SiO_2 layer. For the Cr evaporation on the other hand, the clamped region of the SiO_2 is not covered by Cr, thus is etched during the dry etching step. Accordingly, one can easily determine the exposure of the underlying Si substrate in analogy to the native oxide etch of the evaporated SiO_2 samples.

Based on this calibration technique, the native oxide is determined to be etched within 2-3 seconds, whereas the few nm of intentionally unetched SiO_2 within the holes are observed to be removed within 12-15 seconds.

Following the etching in the BHF, the samples are rinsed with DI water and blown-dry with a N_2 stream. The samples are now ready for MBE loading. In fact, the samples are loaded to the ultra-high vacuum environment of the MBE system within 30 minutes of the oxide etching, in order to avoid growth of a native oxide layer on top of the exposed Si openings.

B

Appendix

B.1 Top-Down Fabrication Process of InAs Nanowires

The epilayer structure composed of a thin film epixtaxial layer of indium arsenide (InAs) on top of aluminium antimonide (AlSb) grown on top of an InAs metamorphic buffer on top of a gallium arsenide (GaAs) (100) substrate are prepared for InAs NW patterning following the subsequent fabrication steps.

B.1.1 Substrate Preparation

The substrate composed of the described epitaxial structure is cleaned following the procedure described in A.1.1.1.

B.1.2 Resist Patterning

The negative tone electron-beam (e-beam) resist, ma-N2403 is used for the patterning of the InAs nanowires (NWs). Due to the observed poor adhesion of the resist to the used samples, a two-step procedure is followed to enhance the adhesion of the resist to the substrate:

1. Reactive oxygen (O_2) plasma step to enhance surface hydrophilicity. The plasma conditions are as follows
   - Power = 50 Watt
   - Pressure = 250 mTorr
   - O_2 flow rate = 10 standard cubic centimetre per minute (sccm)
   - Duration = 60 seconds
2. Spin coating hexamethyldisilazane (HMDS) primer to further enhance the adhesion of the resist to the substrate. The spin coating of HMDS is performed as follows:
   - Spin speed = 6000 rotation per minute (rpm)
   - Spin duration = 30 seconds

This two-step approach is followed by spinning the resist on top of the HMDS-coated substrate. The negative resist is spun and baked as follows:

- Spin speed = 3000 rotation per minute (rpm)
- Spin duration = 30 seconds
- Baking temperature = 115°C
- Baking duration = 60 seconds

This yields an approximately 300 nm-thick resist on top of the substrates. Following the resist coating, the samples are loaded into the electron-beam (e-beam) lithography system, JEOL JBX-9300FS for pattern exposure. The pattern design was completed on a computer-aided desing (CAD) tool and subsequently converted into compatible file formats to be read by the e-beam tool. The accelerating voltage of the e-beam gun provided in the used e-beam system is 50 kV. The electron beam is used to directly write the pattern design on the resist via an exposure dose equal to 120 $\mu C/cm^2$.

After exposure, the resist is developed in an alkaline-based developer, MF-CD-26 for 40 seconds. Transfer of the developed sample from the developer solution to a beaker filled with deionized (DI) water is preformed to rinse the sample. Rinsing is followed by a blow-drying the sample under a stream of nitrogen.

Before proceeding to the following fabrication steps, the sample is exposed to oxygen plasma (50 W - 250 mTorr - 10 sccm) for 30 seconds to remove the HMDS layer. The samples are now ready for InAs etching through the patterned resist.

B.1.3 InAs NWs Etching

The etching of the InAs NWs is performed with an anisotropic chemical wet etch mixture of citric acid ($C_6H_8O_7$) and a 30% concentrated hydrogen peroxide (H_2O_2). The citric acid solution is prepared by dissolving anhydrous citric acid crystals in DI water at a ratio of 1 gram (g) : 1 milliliter (ml). This solution is prepared at least one day in advance before use, due to its endothermic properties. The InAs layer is then etched in a solution of citric acid diluted in hydrogen peroxide with the following volume ratio: 1 $C_6H_8O_7$: 2 H_2O_2. This solution is prepared 30 minutes preceding the etching process to ensure its stability, in case of any fluctuation during the mixing process.

The samples are soaked in the prepared solution until a change is surface color observed, indicating the removal of the InAs layer through the pattern. The etching process is stopped at the AlSb layer, due to a high etch selectivity between both materials in this etchant. As soon as the color change (InAs, faint blue-green color as opposed to the dark-blue AlSb layer), the sample is transferred to a beaker filled with DI water to stop the etching process. Within seconds of transferring the samples to DI water, a color change is observed, where the dark blue tone is turned to a brown-reddish color, indicating the oxidation of the AlSb layer. The sample is then rinsed and blown-dry under a nitrogen flow.

After the completion of the etching process, veriefied by optical and scanning electron microscopes, the samples are soaked in heated (60°C) acetone for 20 minutes to remove the patterned resist layer. Next, the samples are washed with room-temperature acetone, followed by an isopropyl alcohol (IPA) wash and subsequent blow-drying with nitrogen.

B.1.4 AlSb Layer Etching

The underling AlSb layer is etched in order to facilitate the release of the patterned InAs NWs. The etchant of the AlSb layer is prepared by diluting one part of hydrofluoric acid already diluted in 700 parts water, in 5 parts ethanol [1 (1 HF : 700 H_2O) : 5 ethanol]. The pH value of the solution is measured to be close to 2.8. The sample is soaked in the solution until a change in color is observed. The brown-reddish color is turned into a shiny blue-green color as the etching proceeds. The etching is stopped at the surface of the InAs metamorphic buffer, due to a high selectivity between both materials. The etch rate was measured to be roughly 0.5 nm/s. The sample is soaked for different time durations after the change in color is observed with the intention to produce a laterally over etched profile in this anisotropic wet etch solution. The etching process is terminated by rinsing the sample in DI water and subsequent blow-drying with a nitrogen stream.

B.1.5 PDMS Preparation

The elastomeric polydimethylsiloxane PDMS sheet is prepared as follows:

- Mix a PDMS prepolymer with a curing agent (Sylgard 184, Dow Corning) at a ratio of 1:10
- Pour the mixture on a 4-inch silcion wafer pre-modified with a monolayer of (tridecafluoro-1,1,2,2-tetrahydrooctyl)-1-trichlorosilane
- Store the PDMS covered wafer away from direct light in ambient conditions for 38 hours

The PDMS sheet is cured after 38 hours of storage in the dark, yielding a flexible, rubber like layer.