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det	HV	spot	WD	tilt	mag 田	HFW		20 μm
ETD	5.00 kV	7.0	10.1 mm	52 °	3 500 x	59.2 μm		

Low Frequency Dispersion in InP HEMTs

Master's Thesis in Nanoscience and Nanotechnology

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Abstract

The InAlAs/InGaAs/InP HEMT is the state-of-the-art technology for design of ultra-low noise amplifiers for radio astronomy and deep space communication. One of the reasons that make this technology very attractive is the outstanding cut-off frequency f_T and maximum frequency of oscillation f_{max}. However, a low frequency dispersion problem has been found for InP HEMTs working at very low temperature. This is a concern for receivers working in cryogenic condition to achieve better noise performance. No study has been published on this phenomenon before.

In this thesis, a full study of low frequency dispersion in InP HEMTs is presented. The study is based on different measurement techniques including DC, RF and pulse characterization as well as analyzing spectrum measurements. Moreover, this thesis is focused on the influence of the temperature and device structure on the low frequency dispersion problem. Three mechanisms, traps, odd mode oscillation and impact ionization, have been found closely associated with the observation of low frequency dispersion in InP HEMTs.

Contents

Chapter 1

Introduction

The development of the HEMT (high electron mobility transistor) device was started after the experimental verification of electron mobility enhancement in AlGaAs/GaAs heterostructures by forming a 2D electron gas [1]. After this, the first generation of HEMTs based on AlGaAs/GaAs system was widely studied and utilized. Later the requirement of high frequency microwave application led to the emerging of InP HEMTs. It was found that the electron mobility can be largely improved by introducing indium to the channel as shown in Table 2.1. In the last 20 years, InP HEMTs have been holding the record for both noise and high frequency performance. Numerous works have been done to improve the device performance even further. The introduction of multi-finger lay-out for FETs is a very important technique to improve f_T and f_{max} by reducing the parasitic gate resistance R_g [2]. Moreover by aggressively scaling the gate length down to 30 nm, the cut-off frequency f_T has reached to more than 600 GHz and the maximum frequency of oscillation f_{max} is now more than 1.2 THz according to the report from W. Deal's group [3,4]. For low noise applications, a noise temperature of 1.6 K has been achieved in a 4-8 GHz cryogenic InP HEMT LNAs with 4.5 mW power consumption [5,6].

Recently a low frequency dispersion problem was observed for InP HEMTs working at cryogenic temperature. It appears on the DC characteristic as a sudden increase of drain current I_d at certain bias point and drops back to its normal level after further increase of the bias point to a certain value thus forming a "step zone" on the I_d-V_d curve and kinks on the g_m behavior. Abnormal RF performance has also been found at low temperature. For low-noise applications, when the bias point of the InP HEMTs used in LNAs falls into this "step zone", a large increase in noise is seen. The phenomenon is much more prominent for device with multi-finger design.

A large adverse effect on noise behavior of InP HEMTs has been observed at cryogenic temperature due to this dispersion problem. No investigation has been reported so far. Therefore research is very much in need to solve this problem. This would improve cryogenic applications where the low-noise receivers are working at very low temperature to achieve optimal noise performance.

This thesis will start with some background information of InP HEMTs including the epitaxial structure, working principle, noise model used to optimize noise temperature and pros and corns of multi-finger lay-out. In this chapter, knowledge of traps, different oscillation modes and impact ionization will also be provided since we believe that these three factors are in close relation with the problem under investigation. The following chapter will introduce the device structures used in this work and discuss the technology applied to do various measurements. It will continue with a full study of DC,

RF and pulse characterization as well as analyzing spectrum measurement in chapter 4. In the last chapter, a final discussion and conclusion of all the results obtained and a future outlook will be presented.

Chapter 2

Theoretical Background

This chapter first introduces the concepts of InAlAs/InGaAs/InP HEMTs. Then a description of theories of oscillation modes with a focus on odd mode oscillation in FETs will be presented. It will continue with trapping mechanism and then impact ionization effect in FETs. A co-work between trapping and impact ionization will also be discussed.

2.1 InP HEMTs

In this part, the epitaxial layer structure of InAlAs/InGaAs/InP HEMTs and material properties for each layer will be presented. Moreover, a discussion of the working principle of InP HEMTs will be provided. Since most of this work is focused on cryogenic-temperature which improves the low-noise performance of the device, a noise model at low temperature condition will be shown as one sub-part. As the low-frequency problem is more significant for multi-finger structure device, the issues of multi-finger layouts in FETs will be discussed.

2.1.1 Material and Structure of InP HEMTs

InP HEMTs with an InAlAs/InGaAs/InP structure is the second generation of HEMTs. High electron mobility and outstanding frequency performance has made this technology very attractive to high frequency application. Table 2.1 shows a comparison of material properties between different transistor technologies

Table 2.1 Material properties of different semiconductor channel material [7]

Properties	Si	2H-GaN	GaAs	$In_{53}Ga_{47}As$
$E_g(eV)$	1.12	3.4	1.42	0.74
$\mu[cm^2/Vs]$	14000	1000	8500	14000
$v_{sat}[10^7 cm/s]$	1.0	2.5	2.0	3.4
$m_e^*[m_0]$	0.19	0.2	0.067	0.041
$E_L(eV)$		1.1	0.3	0.7
$a[\text{Å}]$	5.43	3.19	5.65	5.87

Typically, an InP HEMT is formed by a thin layer of unstrained $In_{0.53}Ga_{0.47}As$ channel or a strained $In_xGa_{1-x}As$ channel (x>0.53), sandwiched between a lattice matched $In_{0.52}Al_{0.48}As$ buffer and barrier layer on top of an InP substrate. The former is called lattice matched InP HEMT and the later pseudomorphic InP HEMTs (InPpHEMT). The difference is the amount of indium in the channel layer [8]. The structure of these two types of InP HEMTs is illustrated in Figure 2.1. On top of the InP

substrate, the buffer layer which gives the crystalline base for epitaxial structure is grown. It can also provide room for the overgrowth of defects and dislocations. For the channel layer, more indium content gives higher electron mobility. However, too much indium will induce a negative strain. The purpose of the spacer layer is to separate the δ-doping and with this reducing remote scattering. The barrier layer has a great influence on the gate Schottky diode, and access resistance between channel and cap layer, thus affecting the device transconductance and threshold voltage. The cap layer should be designed for lowest possible access resistance achieved by high doping concentration [9].

In addition, the gate structure also plays a very important role in device performance. It has been demonstrated that gate-recess technology can improve device properties such as threshold voltage and transconductance [10]. Moreover, the T-shaped gate can be optimized for minimum noise performance by reducing R_g [11]. Figure 2.1 below shows the recess gate of an InP HEMT. Z.Y.Hui *et al.* did a further research on the influence of side-etch length L_{side} on device's DC and RF behavior [12]. It was found that for device with short enough L_{side}, the kink effect on the dc curve disappeared. However the trade-off between increasing C_{gd} and decreasing R_s and R_d when the value of L_{side} drops requires optimization of the L_{side} value for best f_T and f_{max}. Equation (1) below describes the relationship between f_{max} and C_{gd}, R_s and R_d.

$$f_{max} = \frac{f_t}{\sqrt{4g_{ds}(R_i + R_s + R_g) + \frac{2C_{gd}}{C_{gs}}\left[\frac{C_{gd}}{C_{gs}} + g_m(R_i + R_s)\right]}} \quad (1)$$

2.1.2 Working principle of InP HEMTs

The conduction band energy under the gate along the cutting line AĀ is presented in Figure 2.2 a). The small band-gap of InGaAs helps to form the potential well due to the large potential difference with adjacent layers and this can better confine the electron in the channel. Also the δ-doping has been separated by the spacer to reduce the remote scattering effect from impurities, and achieving very high electron velocity in the channel. The operation of HEMTs relies on the 2 dimensional electron gas (2-DEG) in the channel, the sheet density n_s of which is controlled by the gate-source voltage applied to the HEMT. When negative gate voltage is applied to the device, the electric field can penetrate deeper into the semiconductor and starts to deplete the InGaAs channel layer. This will result in a decreasing of 2-DEG sheet density in the channel shown as Figure 2.2 b). Slightly increasing the gate voltage to 0 *V* as illustrated in Figure 2.2 c), more electrons appear in the channel. The blue curve represents the electron confinement within the InP HEMT at a certain vertical cross section below the gate. By further increasing the gate voltage to 0.2 *V*, the electron density increases further and most of the electrons are attracted to the channel surface resulting in a big peak near the heterojunction interface.
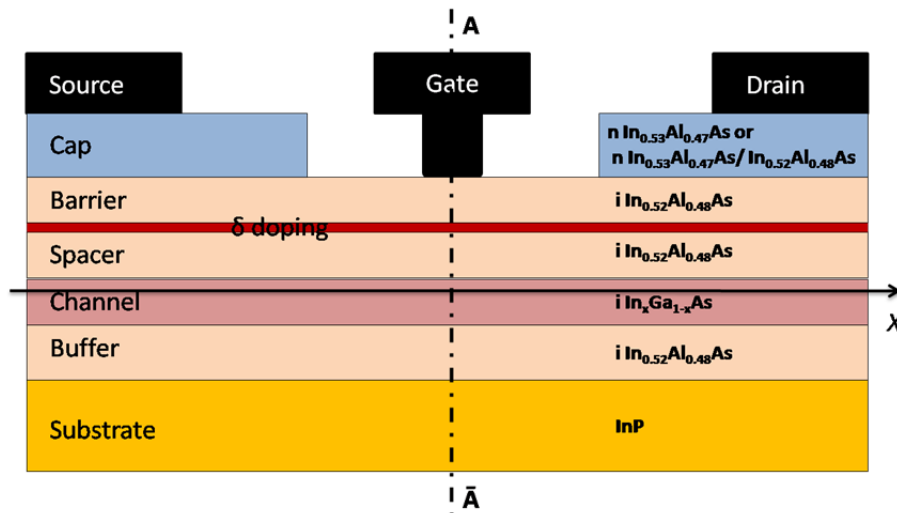
Figure 2.1 Epitaxial structure of InP HEMT

Moreover a positive drain-source voltage is a requirement for device operation. The channel potential $V(x)$ difference from source end to drain end moves the 2DEG from source to drain. Therefore, the electron sheet density at a certain point $n_s(x)$, which decrease towards drain, is the result of a co-work between source-gate voltage and source drain voltage. If $n_s(x)$ at the drain end is smaller than 0, the channel is considered to be pinch off. The voltage to open the channel for device operation is called threshold voltage.
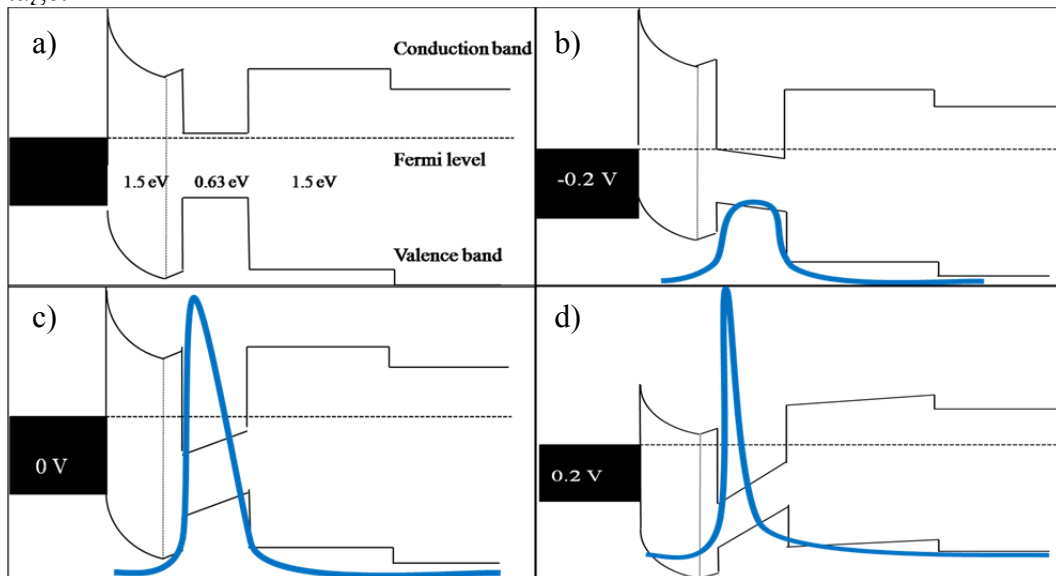

Figure 2.2 Band diagram for InP HEMTs at different bias

2.1.3 Noise Model

In satellite, space communication and radio astronomy, cryogenic cooling of receivers to reduce the noise temperature is very important [13]. However, the optimization for InP HEMTs used in receivers under cryogenic condition can be very different from that of room temperature [14]. To achieve the best noise performance of InP device, a close look at the relationship between noise behavior and temperature as well as frequency is needed. In many reports, noise model based on small signal model

was used. An accurate small signal model could be extracted from analyzing of S-parameter measurements and comparing simulated and measured data. An InP HEMT small-signal and noise model was shown in Figure 2.3. M. W. Pospieszalski [15] provided an approximate expression for minimum noise temperature of a FET chip expressed by

$$T_{min} \approx 2 \frac{f}{f_T} \sqrt{R_t T_g G_{ds} T_d} \quad (2)$$

where $R_t = R_s + R_g + R_i$. R_s and R_g are the parasitic source and gate resistance respectively, R_i represents the intrinsic gate-to-source resistance, C_{ds} is the source-drain out-put conductance and T_d is the equivalent temperature of channel resistance R_{ds}. The main reason that makes noise performance become so different for low temperature is the increased relative sensitivity of T_{min} as a function of T_d [14].A good agreement between Monte Carlo simulation and experiments on InP HEMTs suggested that by cooling down the device, contact resistance will decrease, electron velocity will increase and electrons can be better confined in the channel thus giving an outstanding noise performance [16]. Moreover, T_d and f_T are strongly bias dependent and the optimal point for minimum noise temperature at any frequency is given by minimizing

$$f(V_{ds}, I_{ds}) = \frac{\sqrt{T_d g_{ds}}}{f_T} \quad (3) .$$

For InP HEMTs, the bias point to achieve minimum noise temperature is very low, 75 *mA/mm* at 300 *K* and 15 *mA/mm* at 100 *K*. Therefore many investigations on low-noise performance optimizing are focusing on drain bias below 100 *mA/mm* [14].
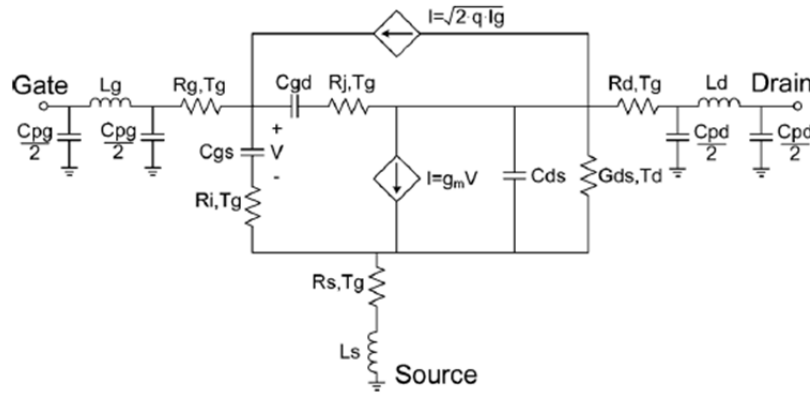

Figure 2.3 Small-signal and noise model of InP HEMT **[14]**

2.1.4 Multi-finger Structure

  Muti-finger lay out has been widely used in modern RF circuit design since it can reduce the parasitic gate resistance R_g, and thus increasing f_T, f_{max} and reducing noise temperature based on Equation (2) [17]. It was observed that the DC behavior and threshold voltage of multi-finger devices differs a lot from its equivalent single finger device due to different parasitic resistance, electric field around the fingers and edge current [18].S.L.Sui *et al.* studied on the impact of multi-finger lay out on subthreshold performance of MOS transistor [19,20]. It was found out that subthreshold channel resistance increased and drain inductance decreased with increasing number of gate fingers which results in more electron transport along the finger boundaries. This could hence enhance the frequency response for RF performance. DC behavior could be

enhanced by multi-structure as well but the dependence of the number of fingers is also closely related to the gate length. The influence from the number of gate fingers is more obvious for devices with shorter channel due to the poorer electrostatic integrity and drain-induced barrier lowering effect [19]. However, the decrease of R_g by increasing the gate finger numbers as well as reduction of gate width will result in a f_T degradation. One of the reasons is the increasing of parasitic gate capacitance stemming from the finger-end fringing capacitance. Another is the g_m decreasing due to the stress induced electron mobility degradation [21].

In addition, problems such as hot-carrier reliability [18]and accurate device model still exists in device with multi-finger structures [20].

2.2 Oscillation

Any amplifier with power gain can generate oscillation by introduction of external feedback. At microwave frequencies, oscillations can be induced by parasitic effects which are introduced during design and fabrication process. There are mainly five types of oscillation in RF/microwave amplifier: even mode, odd mode, parametric, spurious parametric and low frequency [22]. A two-port network is often used to simplify the oscillation analysis. In an even-mode case, there are both current flows in and out of the ports while for odd-mode, current is circling inside the device without current flow in and out of the two ports.

2.2.1 Even-Mode Oscillation

When a transistor is connected in between the input and output matching networks, even-mode oscillation can occur if the transistor is not unconditionally stable. Two-port S parameter models have been widely used to check the even-mode stability as shown in Figure 2.4. Rollett condition, K-factor or μ factor, which are expressed in terms of S parameter (Equation 4 and 5), are usually applied as criteria to check the stability. The active device is considered to be unconditionally stable for all passive source and load termination when $K>1$ or $\mu>1$ with

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \quad (4)$$

and

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{21}S_{12}|} \quad (5) \; .$$

where S_{12} and S_{21} are the transmission coefficient, S_{11} and S_{22} are the input and output reflection coefficient respectively.
The μ factor can also tell the relative level of device stability and a larger μ value often means more stable [22].
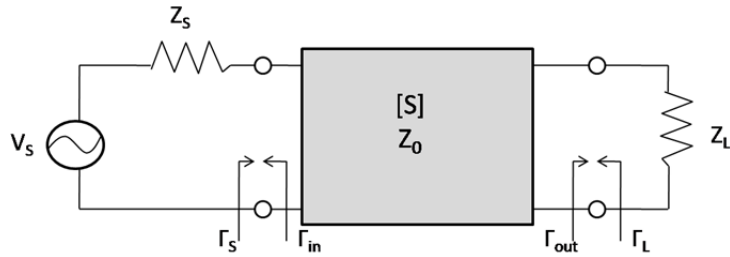
Figure 2.4 Two-port S-parameter model

2.2.1 Odd-Mode Oscillation

Odd-Mode oscillation usually occurs then transistors are put in parallel and each device has its own input and output match. For each device, the operation parameters I_{ds}, V_P, g_m and source or collector inductance can vary from each other. This mismatch will result in different RF voltage at drain locations between devices thus giving odd-mode oscillation or differential-mode excitation [22]. Let's consider the situation of one transistor with a parallel multi-finger structure. The signal can undergo different changes while propagating through each finger thus resulting mismatch at the edge of fingers. Under certain condition, a close loop can be formed between fingers, resulting in the odd-mode oscillation.

The possible physical model for a 4-finger FET is shown in Figure 2.5and the parameters L_{in}. L_{asy} and L_{out} play a very important role in simulate the odd mode oscillation where L_{in} and L_{out} are estimated inductance of one quarter of the loop between two fingers on gate side and drain side respectively shown as Figure 2.6.where L_{asy} comes from the difference between the propagation path for signal through each finger. It was observed that by changing the values of L_{in}, L_{asy} and L_{out}, the odd mode oscillation occurs or disappears and the result shows that an increasing value of L_{in}, L_{ays} and L_{out} will increase the risk for oscillations.
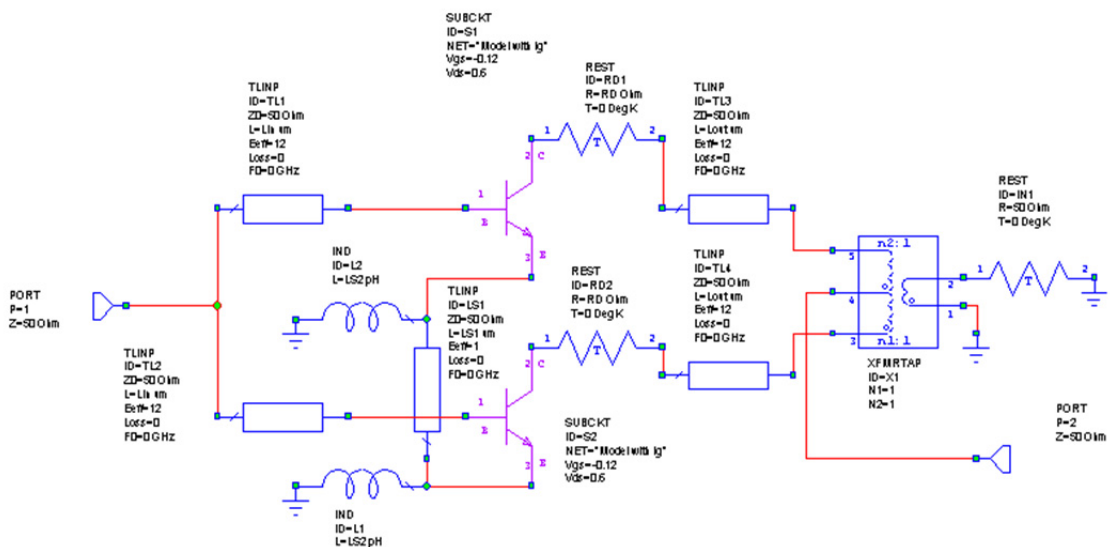

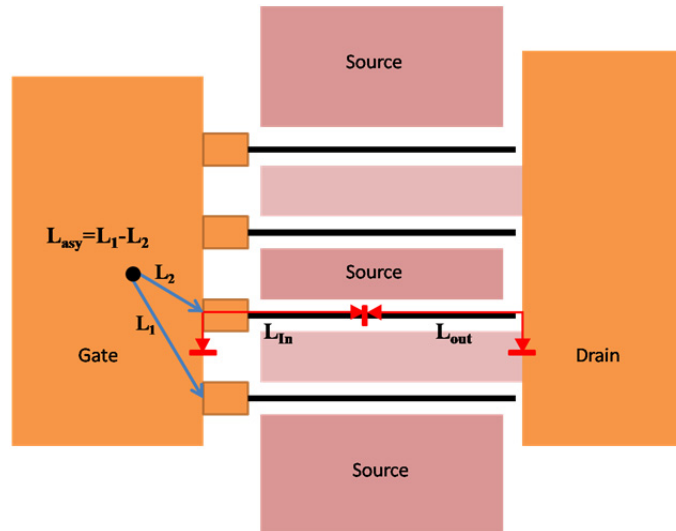**Figure 2.5** Physical Model for 4-finger InP HEMTs

Figure 2.6 Lay-out of InP HEMT. L_{in}, and L_{out} are inductance defined by the red lines. L_{asy} is the inductance difference between the propagation paths for signal through different gate finger

2.3 Traps

Charge trapping is considered to be one of the major issues that can affect device performance especially for broadband application. This is because wide range of frequencies in broadband signals can fall in the region of the microsecond time constants (Megahertz range) of trapping [23].The thermal activated traps have a large influence on the low frequency noise [24,25]. In HEMTs, trap can be the deep-level electron or hole states in the substrate or defects in the surface region. It was suggested that the substrate traps has a strong gate-bias dependence and a week drain-bias dependence [26,27,28]while surface trapping is more sensitive to drain-bias than gate-bias [23].

It was found by J.G.Rathmell *et al* that gate and drain bias potential had an impact on the charge trapping [23]. They measured the drain current I_d as a function of initial gate bias potential ranging from -4 *V* to 0 *V* and pulse to V_{GS}=0 *V* under three different drain biases. The result showed a linear relationship and I_d was smaller for lower initial pulse gate potential and got to a saturation when the initial bias approached V_{GS}=0 *V*.

A detailed study was done by S.Bouzgarrou *et al* on the electrically active defects in InAlAs/InGaAs/InP HEMTs by using current and capacitance Deep Level Transient Spectroscopy (I-DLTS and C-DLTS) as well as Photoluminescence (PL) technique [29]. Mainly two types of defects, type A and B with activation energy of 0.62±0,05*eV* and 0.38±0.04*eV* respectively, have been found in their investigation. Defect A represent the E1 trap reported by Luo *et al.* [30] and Souifi *et al.* [31]. For this type of defect, oxygen could be the reason. By studying the concentration profile, it's believed that defect A had substrate trap with a uniform distribution. Defect B could be attributed to defect E2 discovered by Souifi *et al.* [31] in previous work. They also observed that defect B is close related to oxygen impurities concentration. In addition, two other defects C and D with activation energy 0.1 *eV* and 0.03 *eV* were also found in their measurement but they only existed in InAlAs material. There are any sources for the introducing of traps and one very important factor is processing such as plasma etching [32], epitaxial growth [33], annealing process [34]and etc.

2.4 Impact Ionization

Impact ionization describes the phenomenon that one incoming carrier with enough kinetic energy collide with atom in crystalline lattice and loss its energy by creating one pair of electron and hole and this electron and hole will then create more electron and hole resulting in avalanche breakdown. This process usually happens in a region with high electrical field.

For InP HEMTs, impact ionization is a severe problem due to the small band-gap of InGaAs channel (0.751 eV for $In_{0.53}Ga_{0.47}As$) compared to the band-gap of Si (1.12 eV) [35][i4] and it can be even worse when scaling the device driven by Moore's law. Since there is no Schottky barrier prohibiting the hole from entering the gate, the generated holes will led to the gate-leakage current resulting in poor on- and off- performance for device. While for electrons, there is a potential barrier stopping them flow into gate. They will be attracted by drain. It was demonstrated by A. A. Moolji *et al* that impact ionization could happen in the channel of InP HEMTs under normal operation condition [36][i]. H. Wong *et al*'s work showed that impact ionization in InAlAs/InGaAs/InP HEMTs could adversely affect the noises performance of devices [37]. They found by biasing the device in the impact ionization region, that greatly increased noise signal was produced and they believed this was closely related to the recombination of holes in the channel. The negative gate current with bell-shape on I_g-V_g curve usually indicates impact ionization. This is because of the co-effect of drain current I_D, electric field and gate voltage V_{gs}. When V_{gs} is biased near pinch-off point and the channel starts to turn on, electric field is high but electron density is too small in the channel thus impact ionization current is small. After V_{gs} moves to high value, electron numbers increase but their mean energy drops because of the decreased electric field. Therefore, the impact ionization current increases initially with increasing V_{gs} till it reach a maximum and after this electric field starts to dominant thus bring impact ionization rate down again [36,38].

In addition to electric field, impact ionization can also be affected by temperature. It was found out by Neviani *et al.* that at a field of 125 kV/cm, the impact ionization rate α in $In_{0.53}Ga_{0.47}As$ increased with decreasing temperature. They suggested that this was related to the decreased band gap at higher temperature which then resulted in a decreased ionization threshold energy [39]. Later Ng *et al* studied the impact ionization in the same material under various temperatures and electric fields and discovered that α showed different correlation with temperature under different electric fields. Under high electric field, α was inversely related to temperature while under low electric field, α fell with decreasing temperature [40]. In C. H. Tan *et al*'s work, a three-valley analytical band Monte Carlo model was used to analyze the temperature and electric field dependence of α in $In_{0.53}Ga_{0.47}As$ [41].Since temperature dependence of α varied for low and high field, a two-component ionization rate equation was used in their work,

$$R_{ii}(E) = \sum_{k=1}^{2} \theta(E_i - E_{th}^{(k)})A^{(k)}(\frac{E_i - E_{th}^{(k)}}{E_{th}^{(k)}})^{\zeta(k)}s^{-1} \quad (6),$$

where θ was the step function, E_i represented the kinetic energy of electron. $A^{(k)}$ and $\zeta^{(k)}$ value were chosen based on Ng *et al.*'s work [42], fitting room temperature measurements of α, $E_{th}^{(k)}$ was the threshold energy related to Γ- and X- valley respectively. Figure 2.7 was the result in their work which shows high agreement with Ng *et al*'s argument.
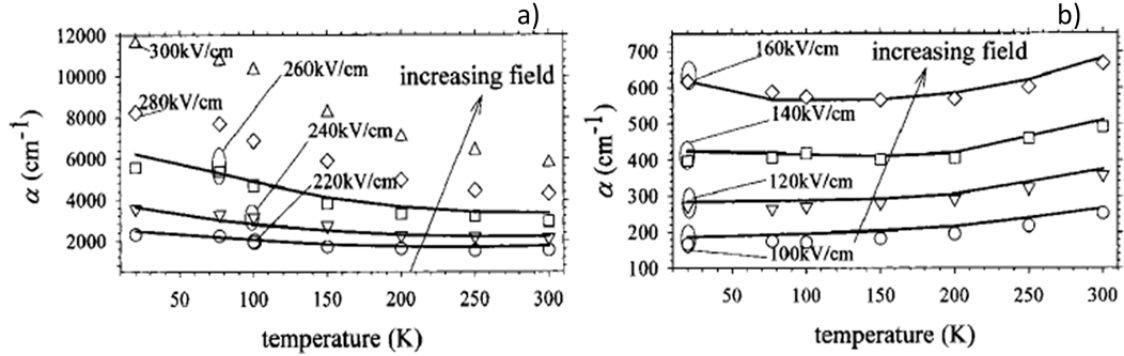

Figure 2.7 Impact ionization coefficient α as a function of temperature at a) high electric field and b) low electric field **[41].**

They proposed that a decrease in temperature gave rise to an increase in band-gap, followed by an increased threshold energy thus reducing the impact ionization rate. While at the same time, the electrons' energy tended to increase due to the decreasing phonon number and this acts as a positive force on impact ionization. The competition between these two mechanisms resulted in the temperature dependence of α at different electric field. At low electric field only the first ionization rate component in Equation 2 could be available since the electron distribution is relatively cool. But the electron energy increase was much slower than the ionization threshold energy increase when temperature dropped in this case due to low density of states in Γ-valley. At low fields, α exhibited a positive relationship with temperature while at high electric fields, hotter electron distribution made ionization accessible. The electron energy increased much faster in this case and dominated the threshold energy increase thus α increased as temperature fell.

To reduce impact ionization and improve device performance, many investigations have been done. Some people tried to increase the band-gap by reducing the InAs contents in the channel, using quaternary alloy like InGaAsP or using InGaAs/InP composite channels design. However, the degradation of transport properties such as electron mobility for device performance by using this technology largely overweighed the beneficial they brought to suppress the impact ionization. Recently, one more effective method, strain engineering, is explored [35].

Moreover, device problems such as kink effect in HEMTs are the contribution from both impact ionization and charge trapping. Kink effect shows on DC characteristics as a sharp increase of I_d at a specific drain-source voltage ($V_d=V_{kink}$) which can result in an increasing in the drain-source output conductance (G_{ds}). It was reported that this anomalous drain current increases due to the hole pile-up and surface traps in the gate recess region near gate [43,44,45]. In their model, deep acceptors were used as surface traps. Impact ionization created hole-electron pairs in the channel and holes tend to accumulate in the source side. Because the potential barrier to confine the holes is small,

some of the electrons will move to the surface and get trapped in the source-gate recess region. It was also proposed that the surface trap in the drain-gate recess region can increase the voltage drop, thus enhancing the weak impact ionization at low bias.

Chapter 3

Method

To better understand the low frequency dispersion problem of InP HEMT, three different batches of devices, H1005, H1006 and H1301, were investigated. Most work was first based on H1005 batch to map the dispersion problem of different device layouts as a function of temperature. The epitaxial structure of H1005 batch is described in Figure 3.1 and the devices measured in each batch are listed in Table 3.1. In the table, $12.5\mu m$, $25\ \mu m$ and $50\ \mu m$ represent the finger width while A, B and C describe the spacing between each finger where A, B and C are $11\ \mu m$, $21\ \mu m$ and $31\ \mu m$ spacing respectively. The H1006 batch was made with the same epitaxial structure and fabrication technology as H1005 except different passivation technology. For H1005, Si_3N_4 plasma enhanced chemical vapour deposition (PECVD) passivation technique was used, while the H1006 wafer was Al_2O_3 passivated using the atomic layer deposition method (ALD).
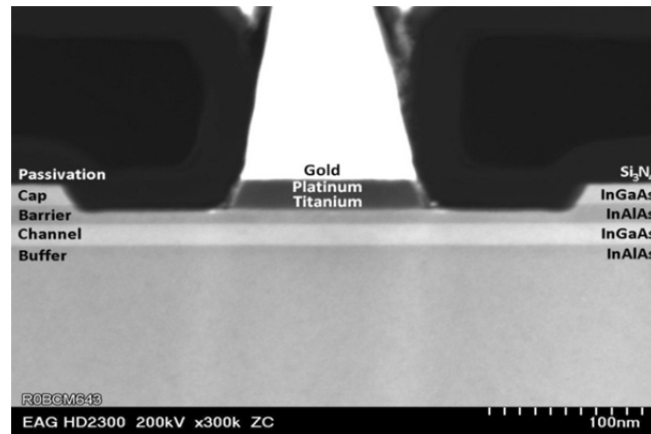

Figure 3.1 Cross sectional STEM image of gate region in a 130nm InP HEMT [6]

Table 3.1 List of the measured devices

Device Batch	Device Information	
H1005	2-finger	2 x 50 μm A, B
	4-finger	4 x 25 μm A, B, C
		4 x 50 μm A, B, C
	8-finger	8 x 12.5 μm A
		8 x 25 μm A, B
H1006	4-finger	4 x 50 μm A, B, C
	8-finger	8 x 12.5 μm A
		8 x 25 μm A, B
H1302	15 layouts: B, C, D, E, F, G, H, I, J, K, L, M, N, S, O	

After analyzing data obtained from these two batches, new structures were designed to verify the results (H1302 batch). In this new batch, devices with 15 different layouts were studied, labeled B, C, D, E, F, G, H, I, J, K, L, M, N, S, O. Among these layouts B is the reference layout with 4 gate fingers, 50 μm gate finger width and 11 μm gate finger spacing shown in Figure 3.2.
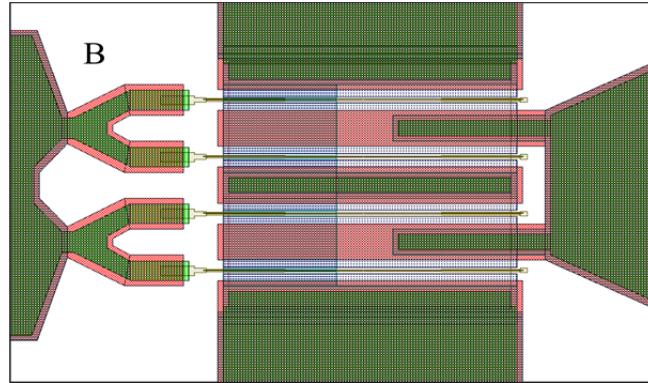

Figure 3.2 Layout for reference device (4X50 μm with 11 μm gate finger spacing)

All other layouts are designed based on this structure by changing parameters. The changed parameters are shown in the "layout information" column of Table 3.2 and Table 3.3. C, E, F, G, H and I structure are designed by changing the airbridge as shown in Figure 3.4 and D, J, L, M, N and S devices are fabricated by changing gate fingers illustrated by Figure 3.5. K layout, with a 90 degree rotation, and O layout which has a drain resistance are described in Figure 3.3.

Table 3.2 List of the layout information for different airbridge design

Layout Label	Layout Information
B	Reference layout
C	Airbridge outside on input side
E	Airbridge to the right
F	Drain airbridge over source
G	Gate airbridge over source
H	Broad airbridge
I	Double airbridge

Table 3.2 List of the layout information for different gate finger design

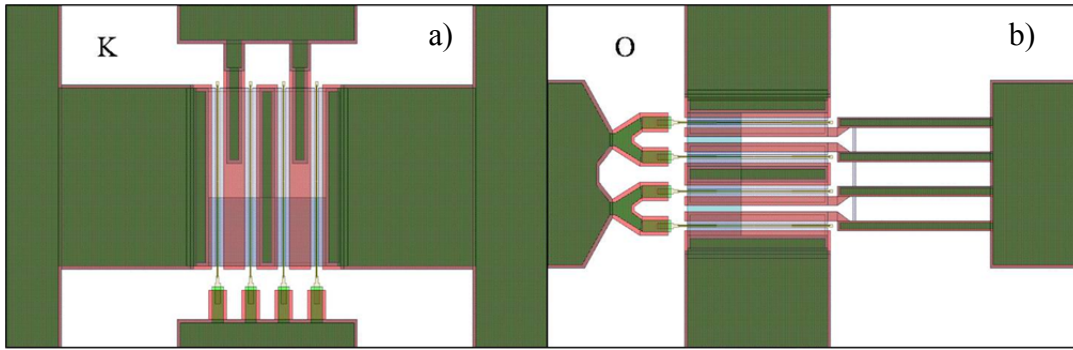| Layout Label	Layout Information
D	Vertical and separated gates
J	Asymmetric gate finger spacing
L	Increased L_{in} and L_{out} (trenches on the gate pad and drain pad)
M	7 um gate finger spacing
N	5.2 um gate finger spacing
S	5.2 um gate finger spacing and thin gate hat (250 nm instead of 500 nm)

Figure 3.3 a) K layout with 90 degree rotation and b) O layout with drain resistance
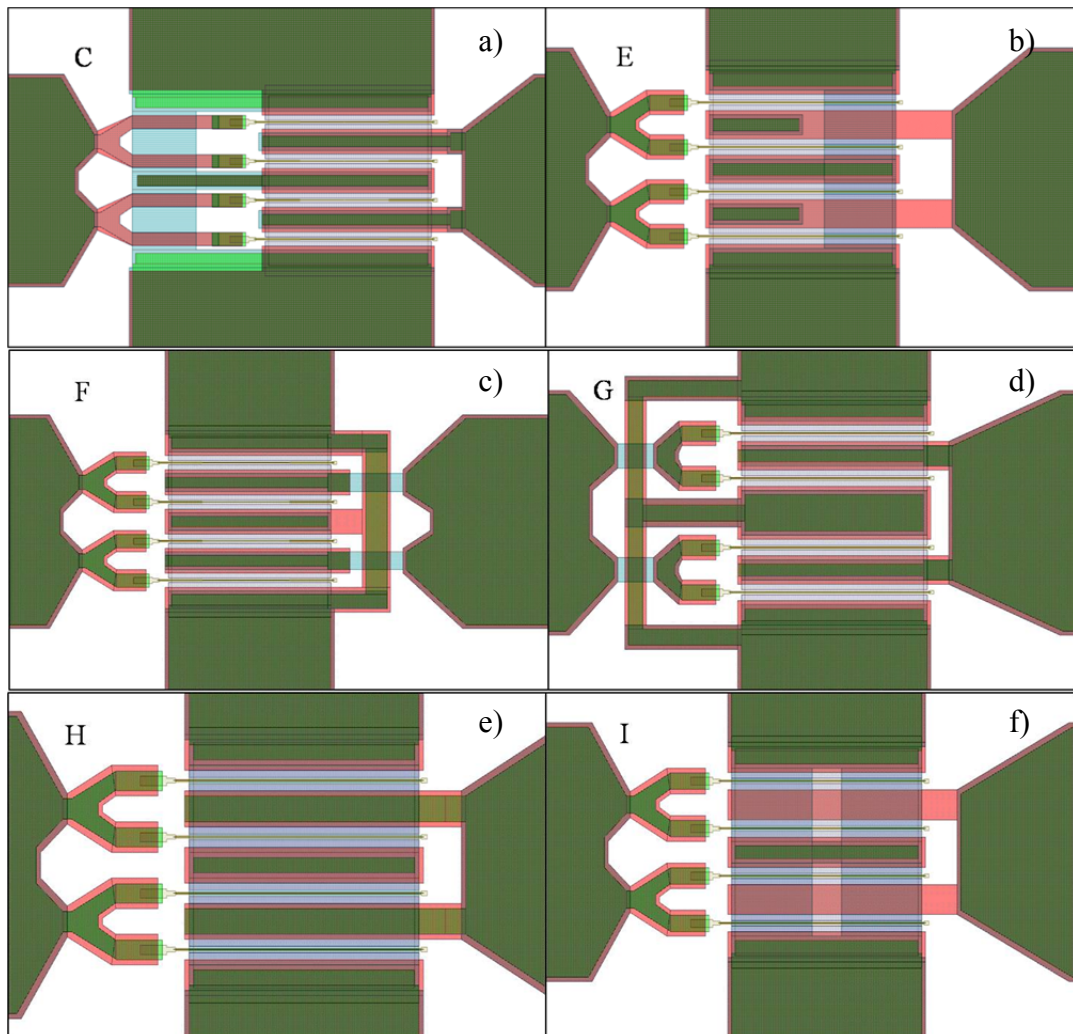

Figure 3.4 The layouts with different airbridge structure in which a) is C layout with airbridge outside on input side, b) is E layout with airbridge to the right, c) is F layout with a drain airbridge over source, d) is G layout with gate airbrige over source, e) is H layout with broadened airbridge and f) is I layout with doubled airbridge
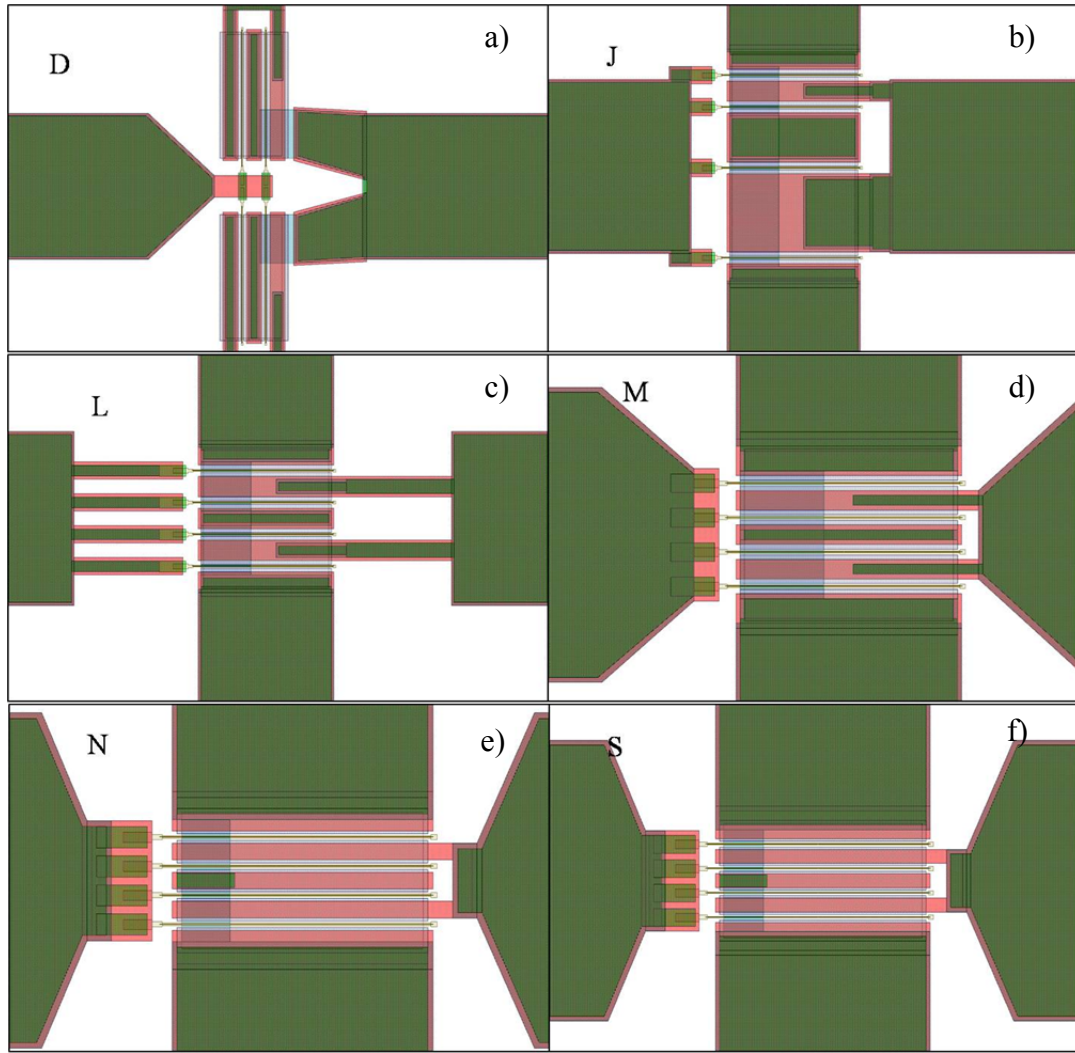
Figure 3.5 The layouts with different gate finger structures in which a) is D layout with vertical and separated gates, b) is J layout with asymmetric gate finger spacing, c) is L layout with increased L_{in} and L_{out}, d) is M layout with 7µm gate finger spacing, e) is N layout with 5.2 gate finger spacing and f) is S layout with 5.2 gate finger spacing but thinner gate hat (250 *nm* instead of 500 *nm*)

3.1 DC Characterization

A cryo-probe station combined with a parameter analyzer was used to do DC characterization. The cryo-probe station was connected to a vacuum pump, a cooling system, a microscope as well as an automatic temperature machine.

To assure good thermal conduction when doing cryogenic measurement, the devices were firstly glued using silver epoxy to a heat sink. Then the heat sink with glued devices on it was put inside the chamber of the cryo-probe station and screwed onto the second cooling stage for sufficient thermal conduction. After this the chamber would be sealed by pumping the vacuum and cooling down the whole chamber.

An Agilent Parameter Analyzer 4156B was connected to cryo-probe station through two ports, one connected to the drain side of the device while the other to the gate side. To control the measurements, a computer was linked to the parameter analyzer via the GPIB interface. The software utilized for DC measurements was Labview. V_g applied for standard DC sweep was from -0.6*V* to 0.6*V* with a step of 50*mV*. V_d was stepped between 0 to 1*V* also with 50*mV* step size.

3.2 RF Characterization

The cryo-probe station was also used in RF characterization to provide various temperature conditions. Besides a Agilent PNA 67 *GHz* with a model E8361A was employed together with probe station to measure the S parameters. The frequency sweeps from 10 *MHz* to 67 *GHz* with a bandwidth of 30 *Hz* for each bias point during measuring, gate voltage V_g from -0.7 *V* to 0.7 *V* and drain voltage V_d from 0 *V* to 1 *V*, both with 0.1 *V* step.

3.2.1 RF Calibration

To achieve a more accurate result, calibration needs to be done in S-parameter measurement to reduce the measurement errors which includes random and systematic errors. Systematic errors are repeatable measurement variation and attribute most to measurement uncertainty in most microwave measurements. There are many sources for systematic errors including impedance mismatch, system frequency response and leakage signals in the test setup [46].

A measurement calibration is mathematically deriving the systematic error model for VNA (vector network analyzer).To choose one suitable calibration, type of device, available calibration standards and the accuracy enhancement needed. The type of calibration used in this work was TRL calibration with three standards: TRL *thru*, *reflect* and *line*. These three standards are illustrated by Table 3.4 shown below. The impedance of line standard chosen in this work was 50Ώ.The Cal kit used was CS5-100.

Table 3.4 TRL standards mapping [46]

	Thru Class	Reflect Class	Line Class
TRL (thru/reflect/line)	Zero length thru with S11=S22=0, S21=S12=1	Unknown equal reflect on port i and port j. Phase approximately known	Line with S11=S22=0 phase approximately known. Bandwidth limited to avoid phase of $\pm 20°$

3.3 Pulsed Measurement

The instrument used in our research to perform the pulsed IV test was the Dynamic IV Analyzer (DIVA) made by Accent Optoelectronics together with the cryo-probe station [47]. By varying the pulse and bias condition, valuable information of dynamic process such as trap, self-heating etc which results in dispersion problems could be obtained. The parameters for the pulse were the pulse length, available from 100*ns* to 1*ms*, and pulse separation, from 0.5*ms* to 1*s* and initial bias point. It was reported that different initial bias could give rise to very different drain currents for dc curves at the same bias conditions [23]. The gate voltage ranged from -0.6*V* to 0.6*V* and drain voltage from 0*V* to 1*V* both with 0.1*V* interval in this work.

3.4 Spectrum Analyzer

The equipments utilized for this measurement were the cryo-probe station, AgilentN5250C 110 *GHz* PNA with the purpose of injecting a signal on the gate of device, and Agilent N9030A 26.5 *GHz* Spectrum Analyzer connected to the output.

Three tests were done in this experiment. First, the continues wave signal from the PNA was swept from 30 *GHz* to 110 *GHz* with the bias point set before, at and after the dispersion problem DC step to see if any output signal could be obtained on the Spectrum Analyzer. Actually by doing this the LNA becomes a mixer rather than an amplifier and this made it able to detect very high frequency oscillations. In the second test the power from the PNA was increased to maximum (+5 *dBm*) in case the oscillation looking for was too weak to detect. The third test was to set the PNA at a fixed frequency and slowly increasing the output power starting at very low level to see if the device was linear.

Chapter 4

Measurements

The low frequency problem was first discovered in InP HEMTs. This has pointed out several directions for us to investigate. One is material related. It can either be specific traps that only exist in the InP epitaxial structure or unknown material breakdown that can generate huge amount of carrier in a sudden (impact ionization). Another way of handling the problem is oscillation since it was observed that this dispersion problem is much more prominent for multi-finger devices. For other technologies, the cut-off frequency and power gain are much lower than InP HEMTs. They are hence simply not fast enough to induce oscillation between fingers.

4.1 DC Characterization

The dispersion problem presented in DC measurements as abnormal jumps in the I_d-V_d curves, a sudden increase of drain current at a certain bias. This jump gave rise to kinks on the g_m curves, a sudden drop of conductance and returning to its normal level at bias slightly higher, sees Fig 4.1 a) and b). These two phenomena have become basic criteria for devices to check the low frequency dispersion problem in this work. The V_{gs} where the step shows up and the extent of the kink on gm curve could tell how bad the problem was. To obtain an overall picture of the DC behavior for this problem, we extended our measurement range to V_d=2 V and decreased the V_g step while measuring. We observed a "step zone" or "forbidden zone" on I_d-V_d curve shown in Fig 4.1c). We also found that the size of step zone was also a good criterion to value the dispersion problem. As discussed before, to achieve low noise performance, the bias point for InP HEMTs operation is usually very low—below 100mA/mm. When the V_{ds} range of "step zone" increases, the possibility that the low noise bias fall into this range will largely increase which shows bad performance of device while being integrated into LNA circuit.

It has been observed that the low frequency dispersion problem for InP HEMT shows relationship with both temperature and device layout, including gate finger numbers, gate finger spacing and gate finger width, to a certain extent. To further investigate this relationship, DC measurements have been done for InP with different structures under different temperatures.
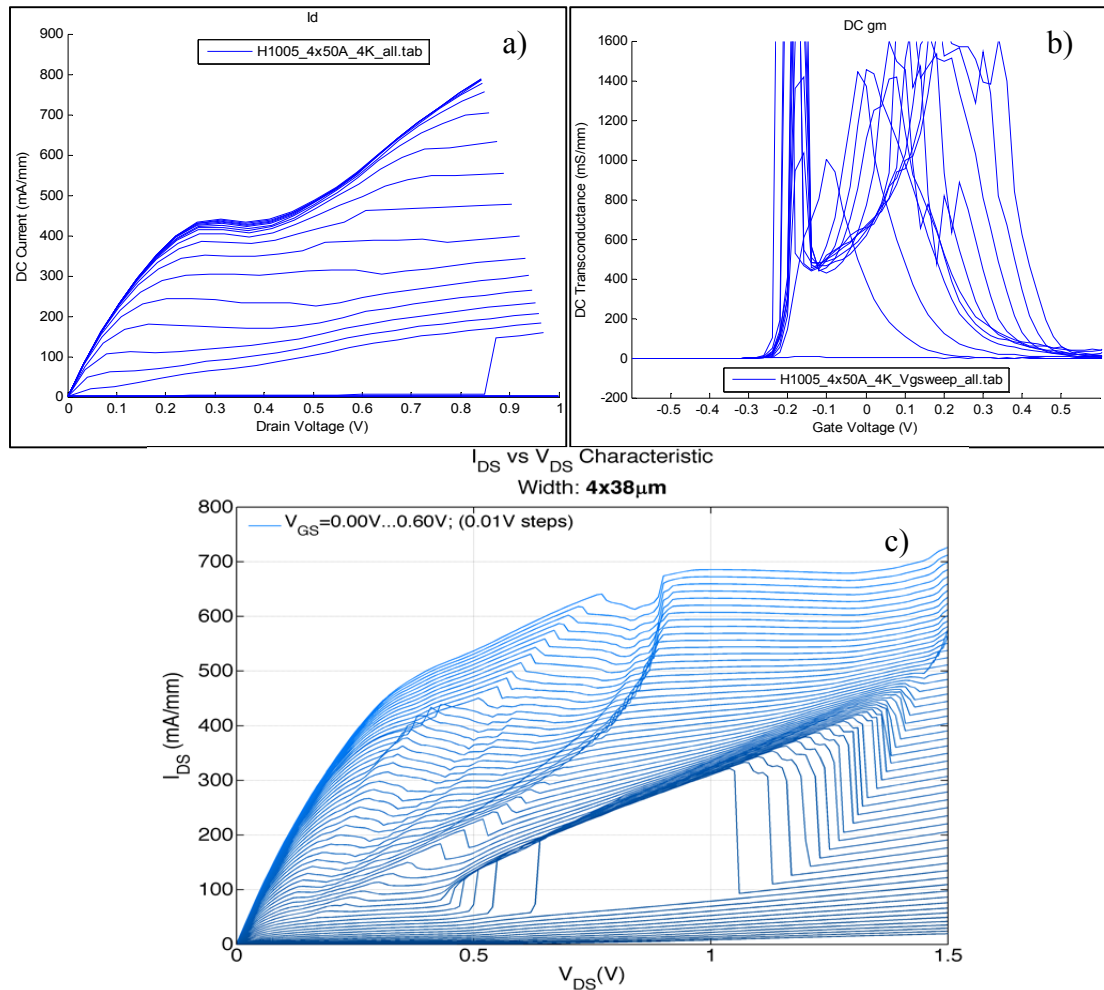
Figure 4.1 a) anonymous sudden drain current increase on I_d-V_d curve, b) abnormal kink on g_m - V_g curve and c) "step zone" or "forbidden zone" for low frequency dispersion problem

4.1.1 Temperature Dependence

The temperature dependence of this dispersion problem is showed in Figure 4.2. The example given here is the DC results of a 4-finger device with 50 μm gate finger width and 11 μm spacing (4X50 μmA device) under various temperatures. It can be observed from the graph that with a decreasing temperature, the "step zone" region increases which means a worse low frequency problem. This can also be seen from the g_m curve described in Figure 4.2 b), d), f) and h). At 300K, the g_m curve shows normal behavior but when temperature reaches 200K, the kink on top of the g_m curve starts to show up at higher V_d. With further decreasing of temperature, the kink becomes larger and extends to lower V_d. Moreover from the I_d-V_d curves at different temperatures shown in Figure 4.2 a), c) e) and g), a relationship between gate voltage V_g and low frequency dispersion problem can be found that with decreasing temperature, the V_g that needed for step to show up falls until it reaches the threshold voltage. This is also be proved by I_d-V_g curve obtained by a clear shift of V_g =V_{kink} to lower value till it overlap with the threshold voltage point.
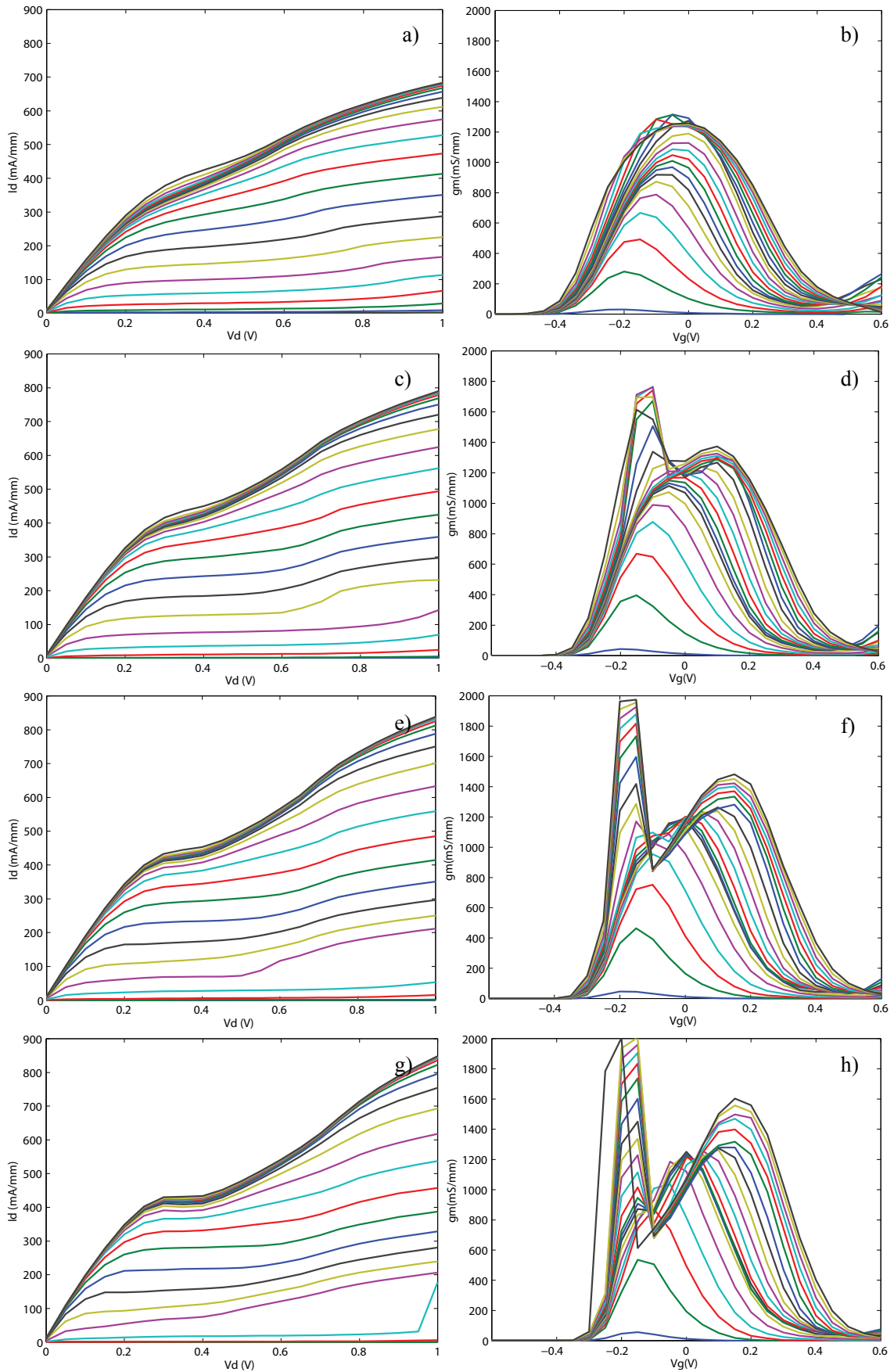
Figure 4.2 DC characteristics curve for 4X50 *μm* A device under a), b) 300 *K*, c), d) 200 *K*, e), f) 150 *K* and g), h) 100 *K* with a), c), e) and g) describe the I_d-V_d behavior and b), d), f) and h) show the g_m as s function of V_g.

4.1.2 Device Structure Dependence

The structure parameters explored in this work were gate finger spacing, gate finger width and gate finger numbers. By varying one of the three parameters each time while keep the other two the same, dependence of each parameter could be decided, based on which we could optimize device behavior.

4.1.2.1 Gate Finger Number Dependence

The influence of gate finger numbers is shown in Figure 4.3 where the dc performance of 4- and 8- finger device with the same spacing and gate finger width has been compared at room temperature. For the 4 x 25 μm B device, both I_d-V_d and g_m-V_g curve shows very good performance while for the 8 x 25 μm B device, there appears a strong low frequency dispersion problem on dc curves shown as large kink on g_m-V_d curve and largely increased step zone range. These results suggest that double the number of gate fingers has a detrimental impact on device. This is a support for oscillation in the device since more fingers usually gives more oscillation.
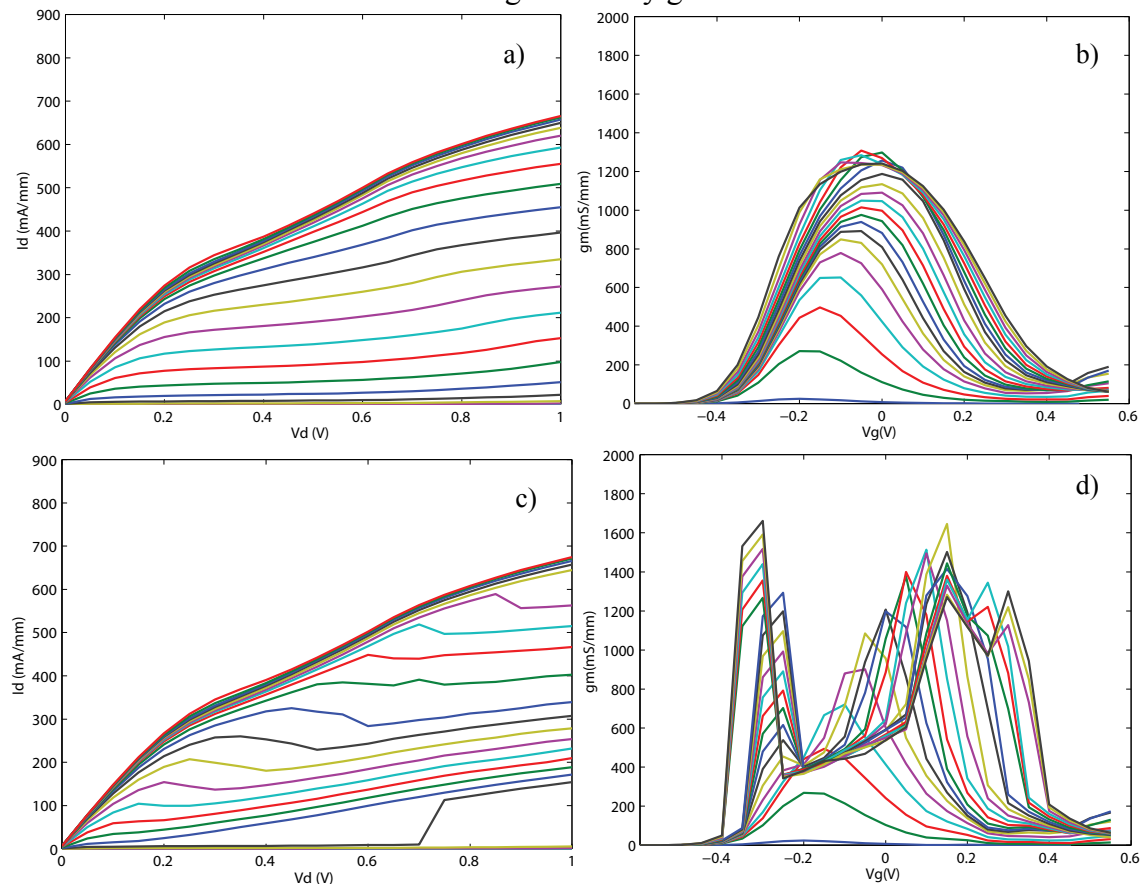

Figure 4.3 DC characteristics curve for a), b) 4-finger and c), d) 8-finger device with a gate finger width of 25 μm and spacing of 21 μm. a), c) describe the I_d-V_d behavior and b), d) show the g_m as s function of V_g.

4.1.2.2 Gate Finger Spacing Dependence

Figure 4.4 shows graphs for 4-finger devices with 50 μm gate finger width but with a spacing of 11 μm, 21 μm and 31 μm respectively at 300 K ambient temperature. For the device with smallest spacing, 11μm (A), both the I_d-V_d curve and g_m-V_g curve shows normal behavior as seen in graph a) and b). When the gate finger spacing was increased to 21μm, graph c) and d), dispersion problem appeared by showing the step at higher V_g

and kink on top of g_m-V_g curve. By further increasing gate spacing to 31 μm, the dispersion problem became much worse at the same measurement temperature since the affected V_d range increased and the V_g where the step starts to occur was already near threshold voltage. This suggests that the dispersion problem gets worse with increasing spacing. This points to the "odd mode oscillation" since larger spacing gives to a larger value of L_{in} which will result in more oscillation based on the model we explained before.
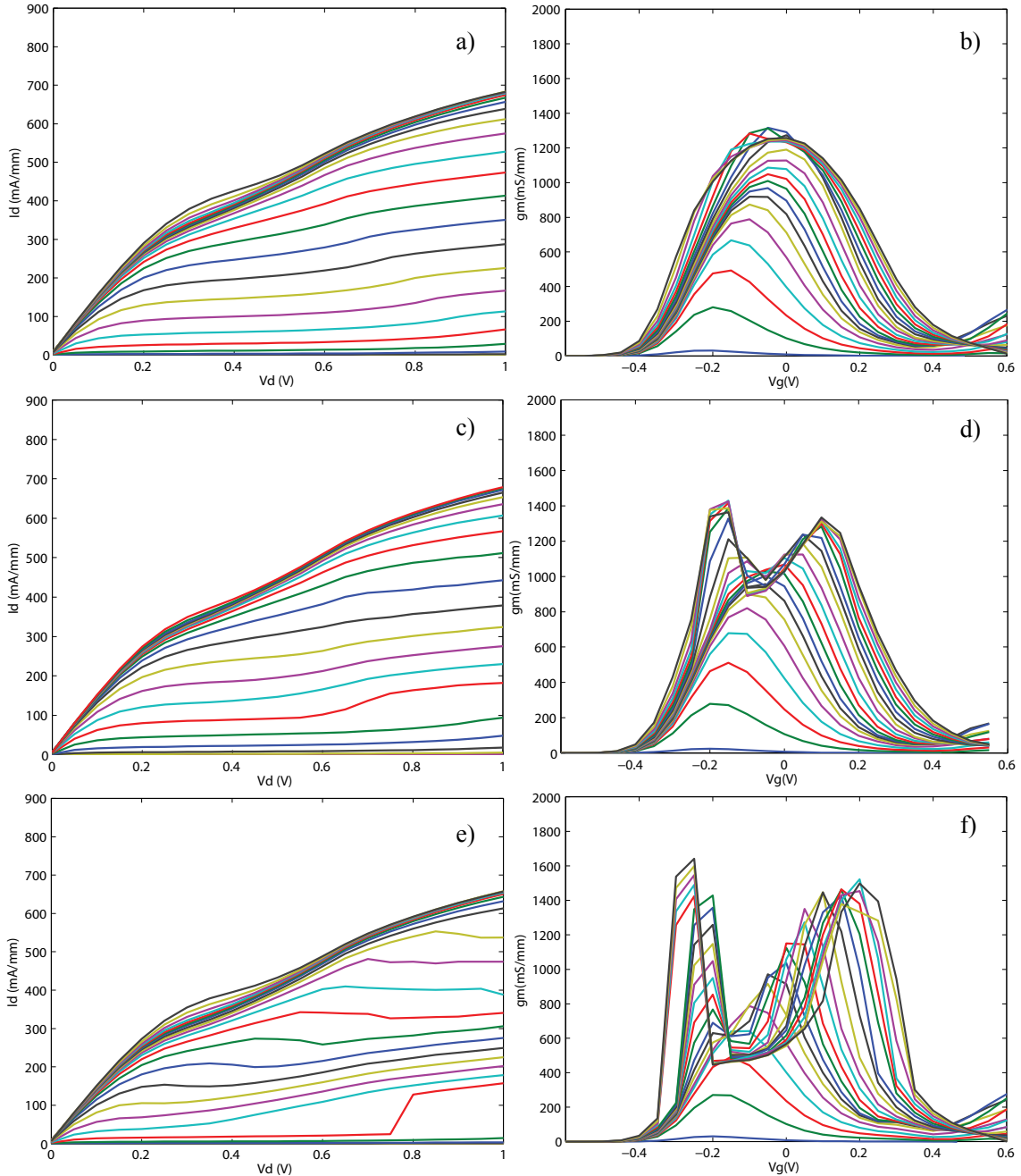

Figure4.4 DC characteristics curve for 4 x 50 μm device with spacing a), b) 11 μm (A), c), d) 21 μm (B) and e), f) 31 μm (C) at 300Kwith a), c), e) describe the I_d-V_d behavior and b), d), f) show the g_m as s function of V_g
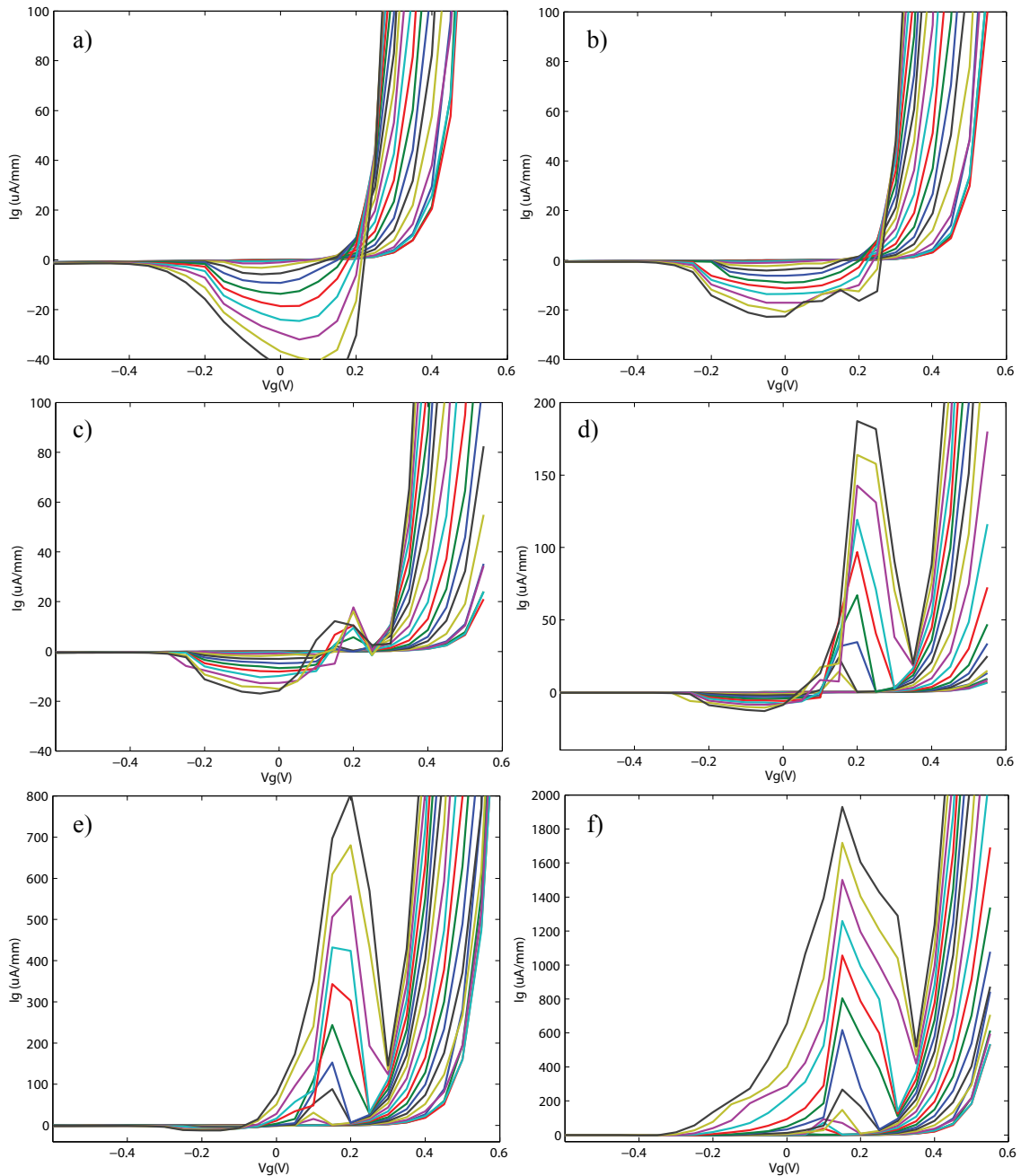
Figure 4.5 Unknown bump on I_g-V_g curve for 4x50μm B structure device under a) 300K, b)250K, c)200K, d)150K. and e) 4x50μm C structure device as well as f) 8x25μm B device

Moreover, a mysterious bump has been observed on the I_g-V_g curve from the measurement which hasn't been found by measurement on other types of transistors. The reason that we think it is related to the problem we study is that it only shows on the device with dispersion problem and the worse the dispersion, the larger the bump. For 4x50 μm devices with C (31 μm) spacing which shows much worse behavior than B (21μm) spacing as shown in Figure 4.4, the maximum bump current is 800 μA per mm. For a 8 x 25 B device, this maximum bump current can reach near 2000μA per mm. This phenomenon is also found to be associated to gate finger spacing. For A (11 μm) spacing device including 4-finger and 8-finer devices, this bump never shows up no matter how low the temperature is (the lowest temperature reached in this work was 6 K). Even though we do observe steps on *I-V* curves from A spacing devices at low

temperature, the bump never shows up. Therefore we suggest that between 21 μm and 11 μm spacing, there must be a point where the bump starts to disappear. The size of the bump increases with decreasing temperature and it starts after the negative bell shape I_g which proved by many researches is due to the impact ionization. Additionally, based on literature [41], the impact ionization should get worse with decreasing temperature shown on the *I-V* curve by an increasing negative I_g. While the negative I_g reduces with decreasing temperature, it seems that the increasing mysterious bump can cancel the negative gate current resulting from impact ionization.

4.1.2.3 Gate Finger Width Dependence

To understand the influence from gate finger width, DC measurements have been done on devices with different gate finger width. The DC comparison in Figure 4.6 between 25 μm gate finger width and 50 μm gate finger width 4-finger devices show that by increasing the gate finger width, the dispersion problem gets worse which is also proved by Figure 4.7, doubling the gate finger width for 8-finger device with the same spacing.
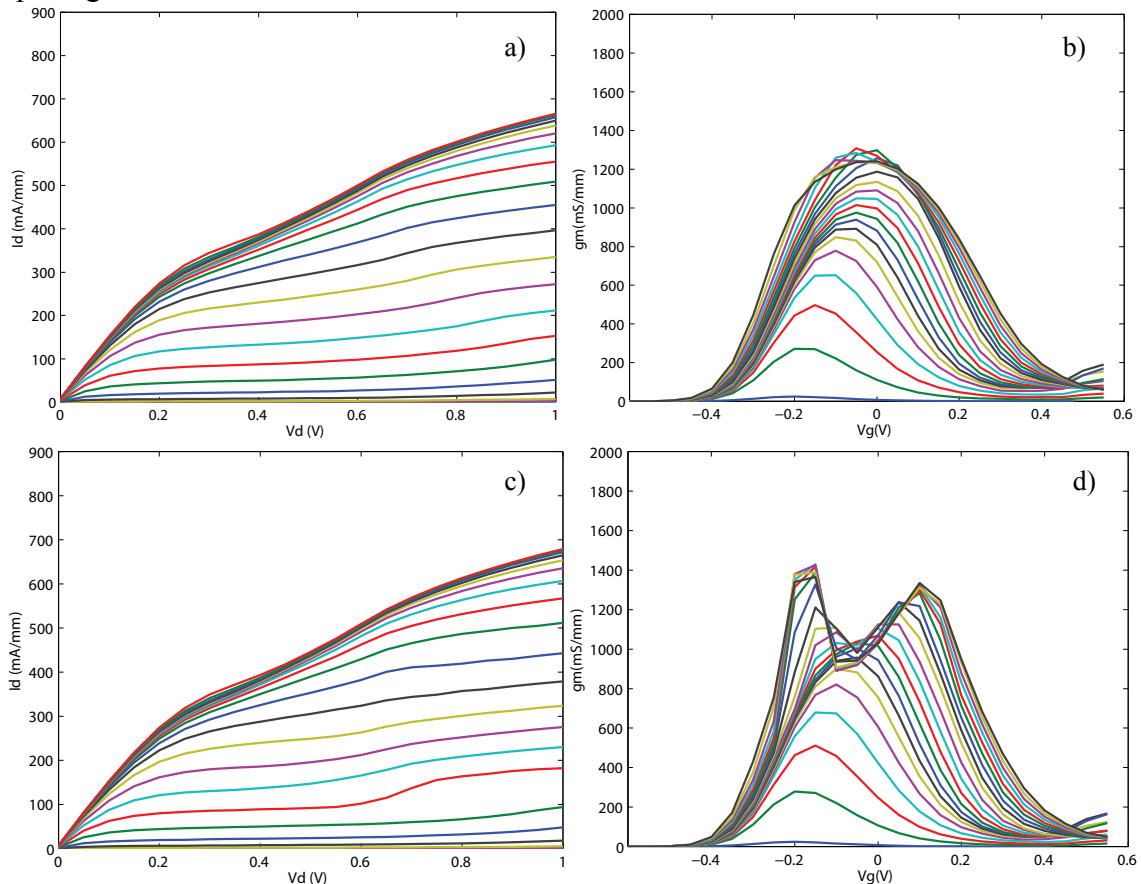

Figure 4.6 DC Characterization for a), b) 4 x 25 μm B device and c), d) 4 x 50 μm B device at room temperature.

However, if compared, the performance difference by doubling the gate finger width in 4-finger and 8-finger devices with the same spacing, it's quite obvious from Figure 4.6 and Figure 4.7 that for larger number of gate fingers, doubling the gate finger width is much worse. Similarly, we also observed the difference in DC behavior by double of the gate finger width between B spacing and C spacing with the same gate finger numbers and found that in C spacing case, increasing the gate finger width results in a

more serious dispersion problem. This can be the reason that 8-finger device and C spacing which has a larger L_{in} device are worse in odd mode oscillation base on the theory explained before and increasing gate finger width can somehow magnify this oscillation thus giving a more detrimental effect on device behavior.
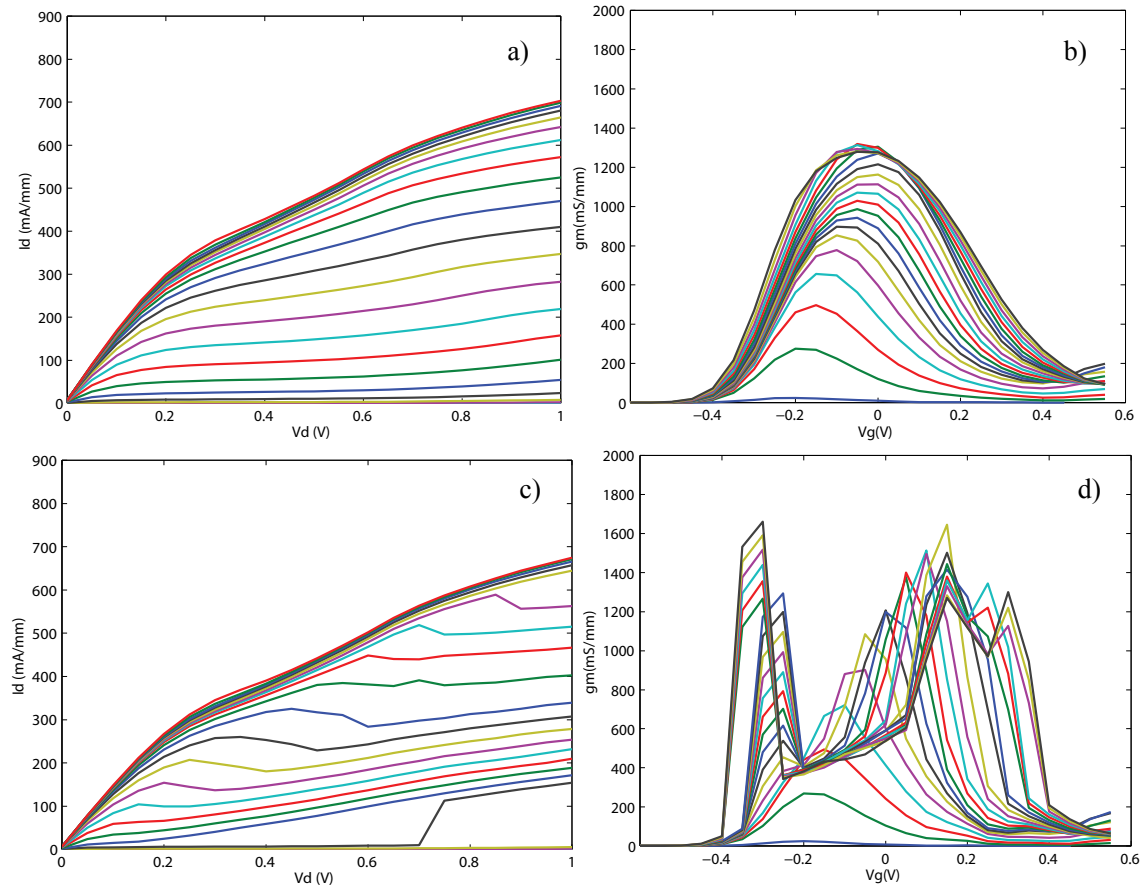

Figure 4.7 DC characterization for a), b) 8 x 12.5 μm B device and c), d) 8 x 25 μm B device at room temperature.

In Table 4.1 is the statistic summary of the DC results from different devices under different temperatures, and provides a more clear picture on how gate finger width, gate finger number and finger spacing influence the behavior of InP HEMTs. The table shows the temperature at which the devices start to show dispersion problem as steps on the I_d-V_d curve and abnormal kink on the g_m curves. If for a certain device the dispersion problem appears at higher temperature, the performance is worse. The results in the table shows obviously that the dispersion problem gets worse with increasing gate finger numbers, gate finger spacing or gate finger width.

Table 4.1 Mapping of the temperature at which dispersion problem starts to show up for devices with different layouts

S \ NXL	4X25 μm	4X50 μm	8X12.5μm	8X25μm
A	50K	200K	70K	250K
B	70K	300K (Higher V$_g$)	---	300K (V$_g$ already near treshold voltage)
C	100K	300K (V$_g$ already near treshold voltage)	---	---

4.2 RF Characterization

To check the oscillation of InP HEMTs, RF measurements were performed under various temperatures for 4X50 μm device with 21 μm spacing. From previous DC measurements, we already know that the threshold voltage increases when operation temperature falls for InP HEMT while the starting gate voltage for I_d jump decreases with decreasing temperature. In addition, we checked the I_d-V_d curve for 4X50 μm B devices before with a temperature range from 300 K to 70 K and found that starting V_g on I_d-V_d curve had moved down very close to the threshold voltage already at 250 K. This means that at this temperature, the threshold voltage overlaps with the starting V_g. With further decreasing the temperature, these two voltages continue to evolve in opposite direction with respect to operation temperature. It is possible that the threshold voltage V_g for InP HEMTs at 100 K and 70 K is already above the V_g where the step (oscillation) shows up, thus the devices we measured at 150 K, 100K and 70 K just starts to oscillate as soon as the channel is opened. However because the oscillation occurred too close to the threshold voltage and the current was too small, we couldn't observe big jump on I_d-V_d curves and instead it shows as ripples on the S_{21} curve for 150 K, 100 K and 70 K at low V_g shown in the green circle in Figure 4.8 b). Correspondingly, the S_{22} curve will show as a curl-up effect (Figure 4.8 a)). While for 200 K and 250 K operation, the threshold voltage needed is lower which provides can provide enough current level for a big jump on the I_d-V_d curve, showing on the S_{21} curve is a big spike highlighted by a red circle in Figure 4.8 b). The device will start to oscillate after this big jump and shown on the S_{21}curve with ripples at low frequency range as described in Figure 4.8 d).And on S_{22} curve we will see an abnormal spike at the low frequency range followed by a curl-up shown in Figure 4.8 c).

To make it more clearly, curves at higher V_g (0 V) are presented for different temperature. For 150 K, 100 K and 70 K measurements, this V_g can provide enough current to reach a jump. So what we can observe from the RF curves at V_g=0 V is that the curves at 70 K and 100 K first show big spike shown in Figure 4.9 a) and b). While with increasing V_d, curves at higher temperature starts to show big spikes as seen in Figure 4.9 c) and d). This corresponds with the temperature dependence in DC results. At higher temperature, the dispersion problem is less serious, so higher V_d is required at the same V_g level for the dispersion problem to show up. Table 4 also highlights this. For all curves, spikes will change to ripples on S_{21} and curl-up on S_{22} as in Figure 4.9 e)

and f) when further increases the bias. In addition Figure 4.9 c) can also tell us that how bad the RF result can be at certain bias. It can be observed that at low frequency range, the S_{22} curve shows very abnormal behave and some have even extended outside the reflection circle, meaning the reflection is larger than 1 which proves the oscillation.

Moreover, the "step zone" or "forbidden zone" region on I_d-V_d curve is also been proved by RF results. With further increase of V_g and V_d, RF curves for different temperature becomes synchronizing with each other again with spike at low frequency which is believed to be the result of impact ionization.

To further check our proposal, we compared the RF results at 300 K for 4X50 μm B device with 4X50 μm A which shows normal DC behave. For all V_g and V_d value, RF results shows no spike and ripple except when V_g and V_d are too high where impact ionization happens. This further proves that the abnormal spike and ripple on RF curves can be associated to the sudden jump on the I_d-V_d curve.
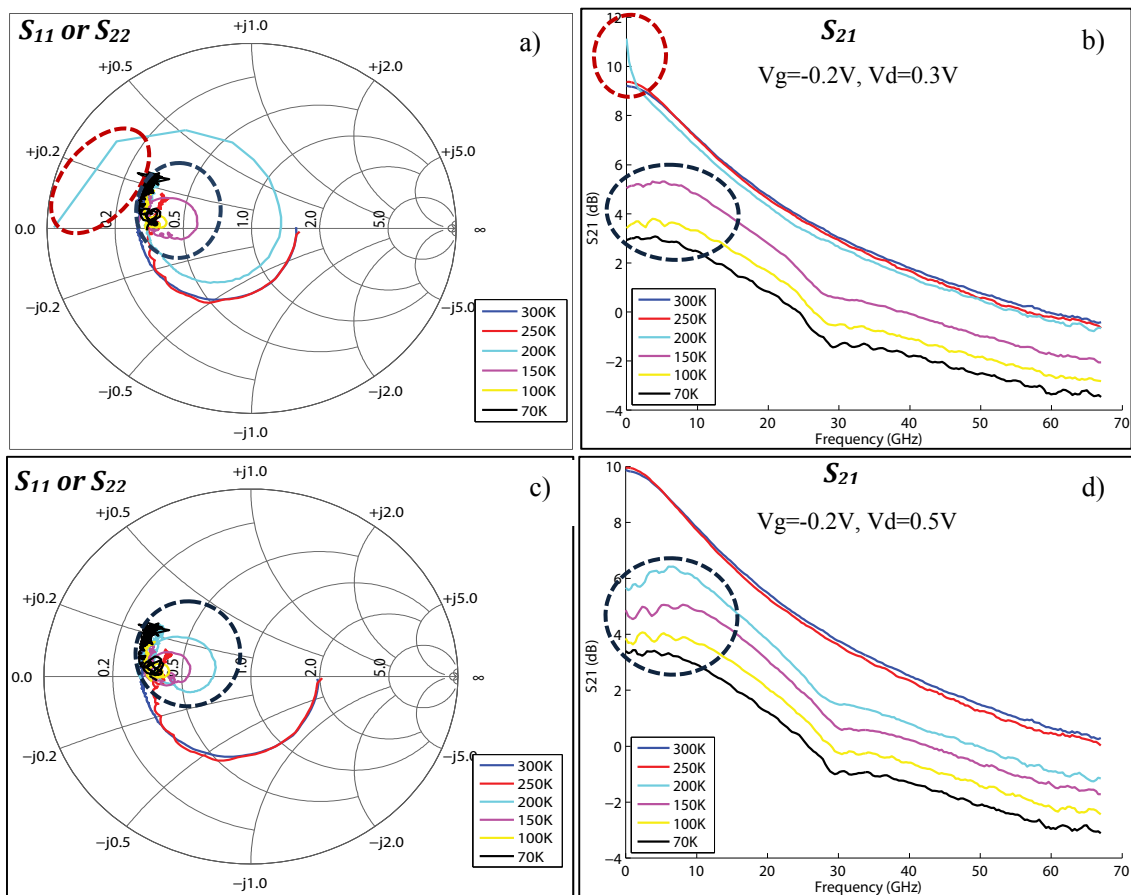

Figure 4.8 RF Characteristics for 4x50 B device at different temperature under gate bias of V_g=-0.2 V and drain bias a), b) V_d=0.3 V and c), d) V_d=0,.5 V
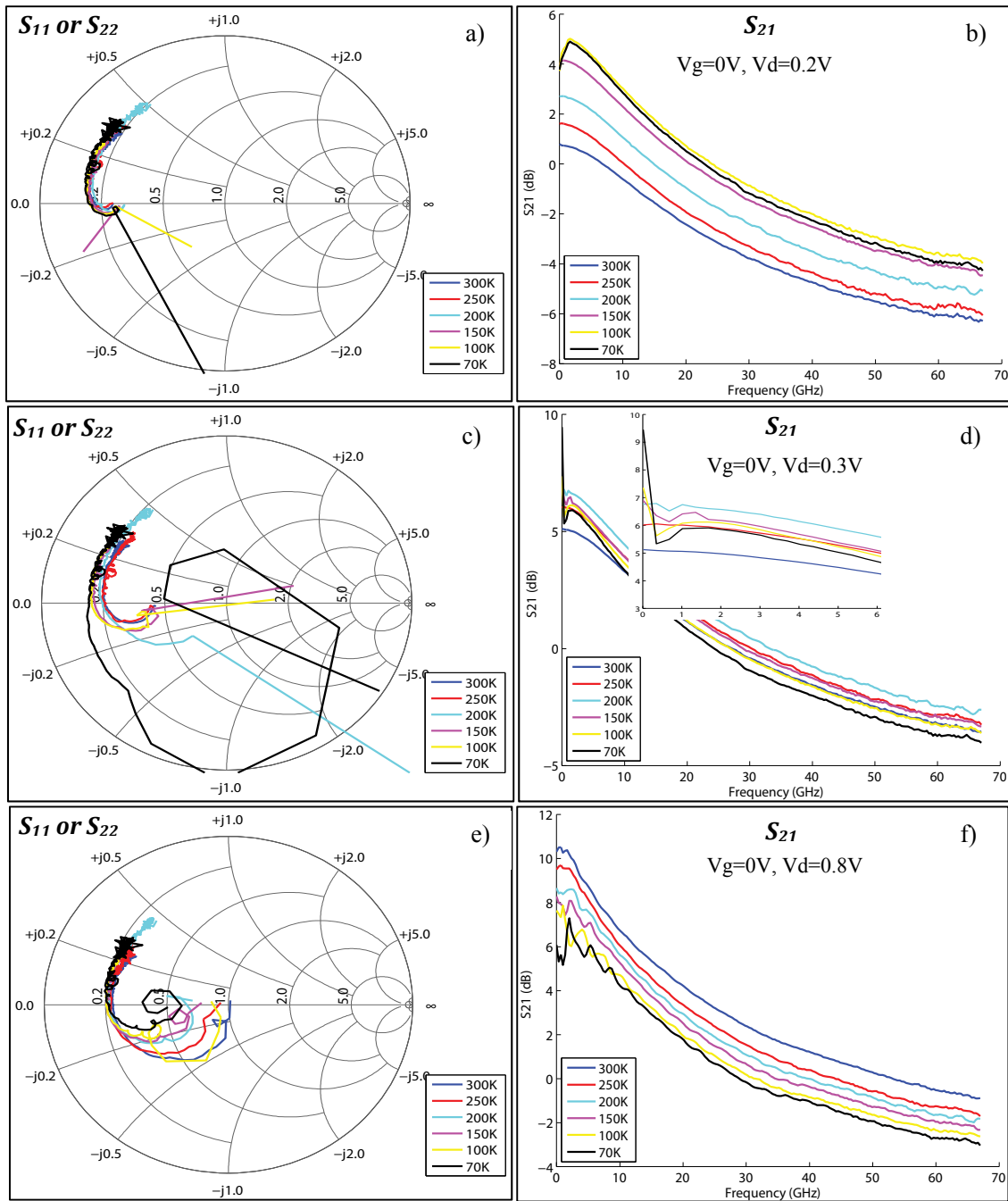
Figure 4.8 RF Characteristics for 4x50 B device at different temperature under gate bias of V_g=0 V and drain bias a), b) V_d=0.2 V, c), d) V_d=0,.3 V and e), f) V_d=0,.8 V

Table 4.2 The summary for S_{22} or S_{11} for 4 x 50 B device at V_g = -0.1 V as a function of V_d and operation temperature.

T (K) \ V_d (V)	70	100	150	200	250	300
V_d=0.1	Spike	Spike	Normal	Normal	Normal	Normal
V_d=0.2	Curl-up	Curl-up	Spike	Spike	Spike	Normal
V_d=0.6	Curl-up	Curl-up	Curl-up	Curl-up	Curl-up	Curl-up

4.3 Pulsed Measurement

Pulse measurements were done to prove or rule out the influence of traps which could result in undefined dispersion on device's behaviors. Figure 4.9a) shows the result of pulse measurement on 4 x 25 μm device with a spacing of 21 μm which has obvious steps on *I-V* curve when cool down to 50 *K*. From the graph, we can see that the result is closely correlated to the initial bias point of the pulse. When the pulse is starting from very low V_g, there is no obvious step on the *I-V* curve while steps show up at high starting V_g and the border V_g is -0.3 *V*. Figure 4.9 b) is a Monte-Carlo simulation of electron density as a function of channel depth for different V_g. When pulse the device from very low initial point, the electrons will have more probability to stay at the down part of the channel, more near the buffer layer. Moreover, when gradual increases the pulse length with fixed initial bias point, a left shift of steps is also observed. These results prove that the step on the DC curve has some relationship with traps in the device.

So the next step is to check the position of the step. A new batch of devices with Al$_2$O$_3$ surface passivation layer which is proved to possess a better surface passivation than Si$_3$N$_4$ used in previous batch has been made. But from the DC measurement I have done, it seems that the surface traps have a very minor effect on this specific dispersion problem. There is a very small V_g shift (increased around 0.05 *V*) at which the steps appears. Moreover, the temperature at which the steps show up on *I-V* curve is almost the same with the old batch. It seems this effect is less likely related to the traps in surface of passivation layer. Another suggestion is the deep-level trap in the buffer layer which could be explored by microscopy.
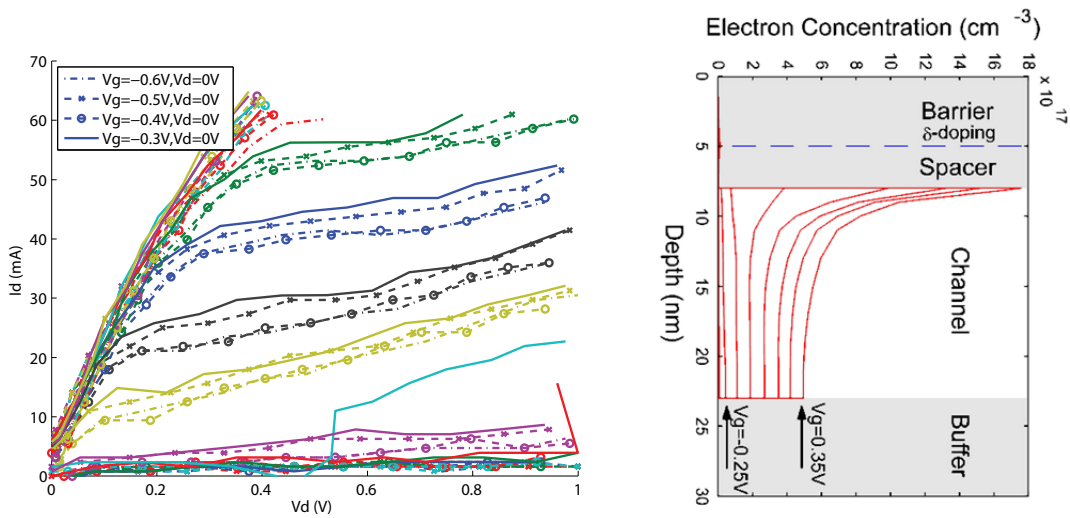

Figure 4.9 a) Id-Vd curve for device pulsed at 50K with 0.1 μs pulse but different initial bias point. Different line style means represent different initial bias from V_g=-0.6 *V*, V_d=0 *V* to V_g=-0.3 *V*, V_d=0 *V*. b) The Monte-Carlo simulation of electron density as a function of depth under different V_g [48].

However, when look back on the DC measurement, it's found that the device with the same working area behaves differently which is in conflict with the trap theory since the amount of traps should be similar for devices with the performing area.
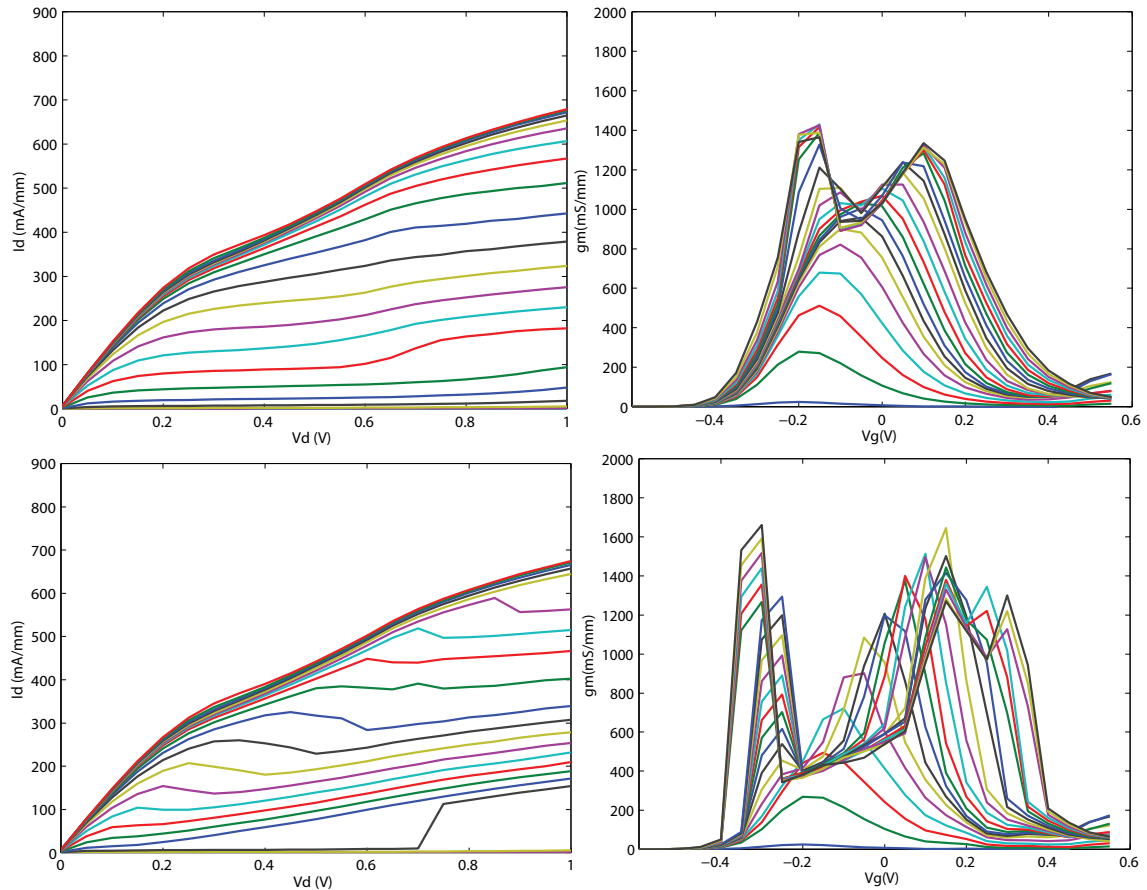
Figure 4.10 DC behavior for a), b) 4 x 50 B device and c), d) 2 x 25 B devices at room temperature. a), c) are the I_d-V_d curves and b, d) are the g_m-V_g curves

4.4 Spectrum Analysis

A spectrum analyzer is employed to check if this dispersion problem is induced by oscillation in InP HEMTs. If oscillation is the reason, it must be very strong and likely to saturate the device which will make the devices become non-linear and will start to create intermodulation products. Basically it becomes a mixer rather than an amplifier. In Chapter 3.4, a detailed description on how this measurement is setup has been presented is given.

In the first test, the frequency is changed from 30 *GHz* to 11 *GHz* with device biased just before and just after the jump at V_{ds}=0.85 *V* close to pinch off. It was suggested by the simulation in Chapter 2.2 that the odd mode oscillation in multi-finger InP HEMT is very likely to happen around 136 *GHz*. The non-linearality would create a 26 *GHz* harmonic signal which can be observed on spectrum analyzer. But no strong oscillation was found between 0-136 *GHz*.

The second test was performed to eliminate the possibility that the oscillation signal is too weak to detect by increasing the power from PNA. But still no strong oscillation was indicated by it.

In the last test, the output power is inceased with fix frequency in PNA to see the linearality and it shows that no non-linearality was observed up to +8 *dBm*. The result of this test proves that there are no strong oscillations (strong enough to bring it close to saturation) at any frequency.

It was suggested by these results that if odd oscillation is the reason for this sudden jump on I_d-V_d curve, then its frequency must be larger than 136 *GHz*.

4.5 Odd Mode Oscillation Investigation

Odd mode oscillation often happens between parallel transistors. The small variation I_{ds}, V_p and gm or different source (L_{in}) and collector layout (L_{out}) of each transistor can result in a mismatch between transistors, providing the condition for odd mode oscillation. This kind of oscillation can still happen even though $k<1$. Normally, odd mode oscillation can be suppressed by adding resistor between each two transistor. However, it would require a lot of work by adding resistor between each two gate fingers in one device. From Chapter 2.2 we already know that three parameters L_{in}, L_{out} and L_{asy} can influence odd mode oscillation a lot and larger value of L_{in}, L_{out} and L_{asy} can lead to an increased odd mode oscillation. Therefore by playing with these three parameters of device, the odd mode oscillation can be suppressed or induced. To achieve this, we used FIB (Focused Ion Beam) to modify the structure shown as Figure 4. b), c), and d). Figure 4.11 a) shows the image of 4 x 50 B structure before FIB.
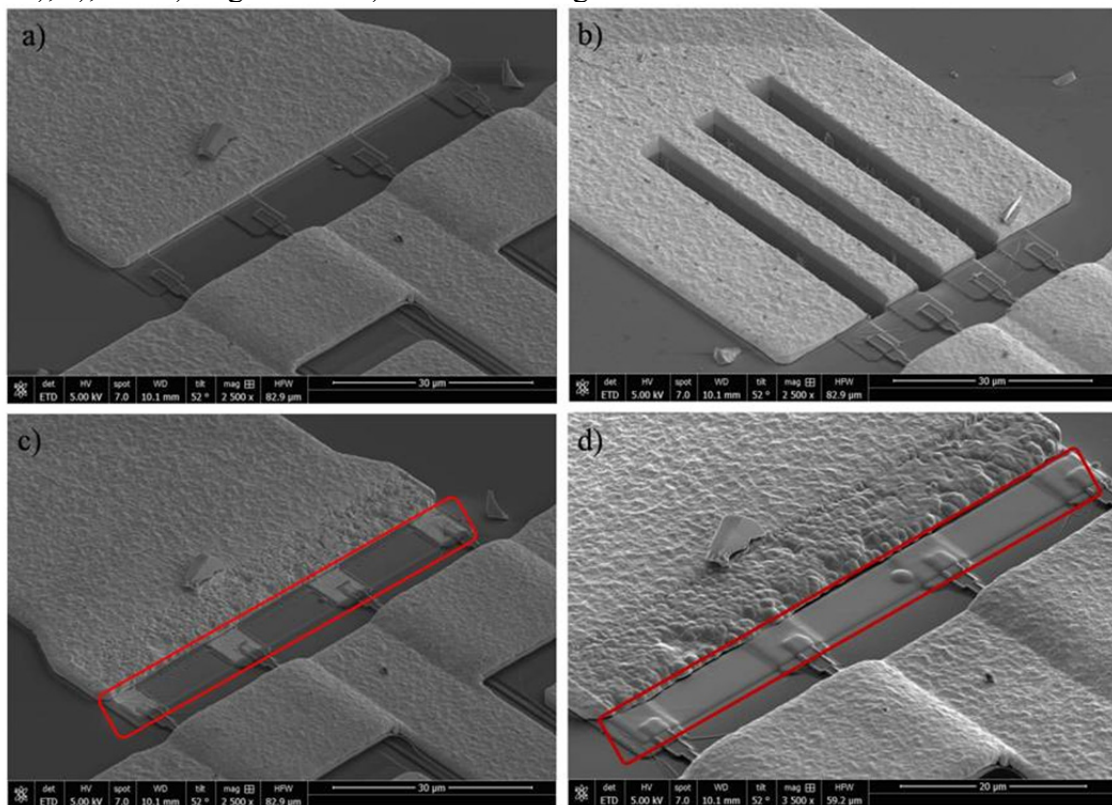

Figure 4.11 Images for device modification using FIB (Focus Ion Beam). a) is the image for 4 x 50 B device before FIB. b) shows the trenches made on 4 x 50 A device. c) is the image for 4 x 50 B device after removing the passivation layer in the red rectangle area. d) shows the metal layer deposition in red rectangle area.

In Figure 4.11 b), trenches are made between gate fingers on the gold pad to increase L_{in}. This was performed on 4 x 50 *μm* A (11 *μm* spacing) device which shows very good performance at room temperature, and by doing this we expected that it would show similar behavior as 4X50μm C (31*μm*) which had very serious dispersion problem at 300 *K*. The DC measurements comparison between devices before and after FIB are studied (Figure 4.12).To make the observation clearer, the V_g step is decreased to the

measurements. From Figure 4.12 a) and b), it can be seen that some small steps are introduced to the *I-V* curve after FIB though it is not significant. The difference is more obvious in g_m-V_g curve shown as Figure 4.12 c) and d) and a large abnormal kink appears on top of the curve. These results show that by increasing L_{in}, dispersion problem shows up.

Decreasing L_{in} is achieved by removing the passivation layer followed by a metal layer deposition to short the gate inputs shown as Figure 4.11 c) and d) respectively. This work was done on 4 x50 *μm* device with a B spacing (21 *μm*) with the aim to achieve similar performance as 4 x 50 *μm* A(11*μm* spacing) which shows no dispersion problem at room temperature. Figure 4.13 a) and c) are the DC results for 4 x 50μm B at room temperature and Figure 4.13 b) and d) are DC performance for the same device after FIB surgery. It can be observed that the steps which are the criteria for dispersion problem are reduced for device after decreasing L_{in}. Moreover, the bump on the I_g-V_g is disappeared which again shows an alleviated dispersion problem. However another possibility is that the large gate leakage current in the I_g-V_g curve after FIB overweighs the bump gate current and make it invisible in curve.

From the results we got above, it clearly that the odd mode oscillation does play a part in the dispersion problem even though not as significant as expected.
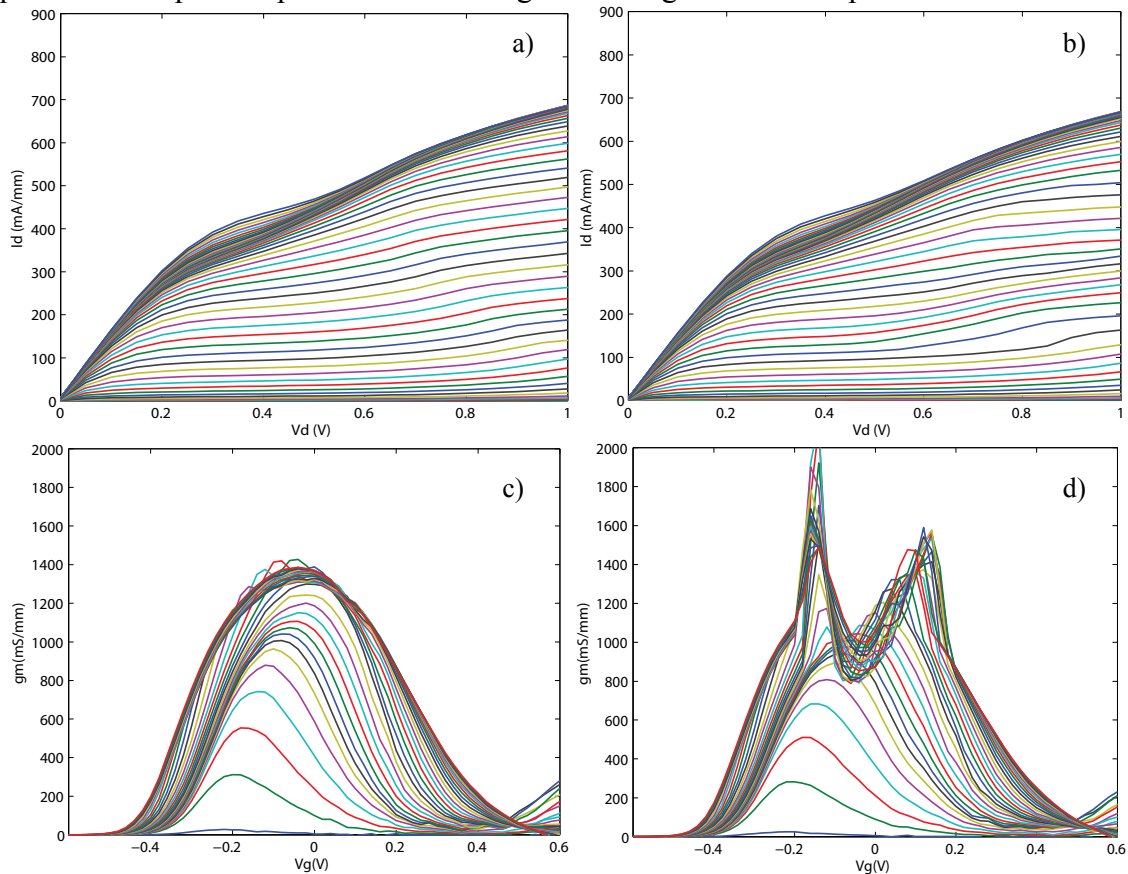

Figure 4.12 DC Characterization comparison for 4 x 50 A device a), c) before and b), d) after FIB experiment. a), b) are I_d-V_d curves and c), d) g_m-V_g curves.
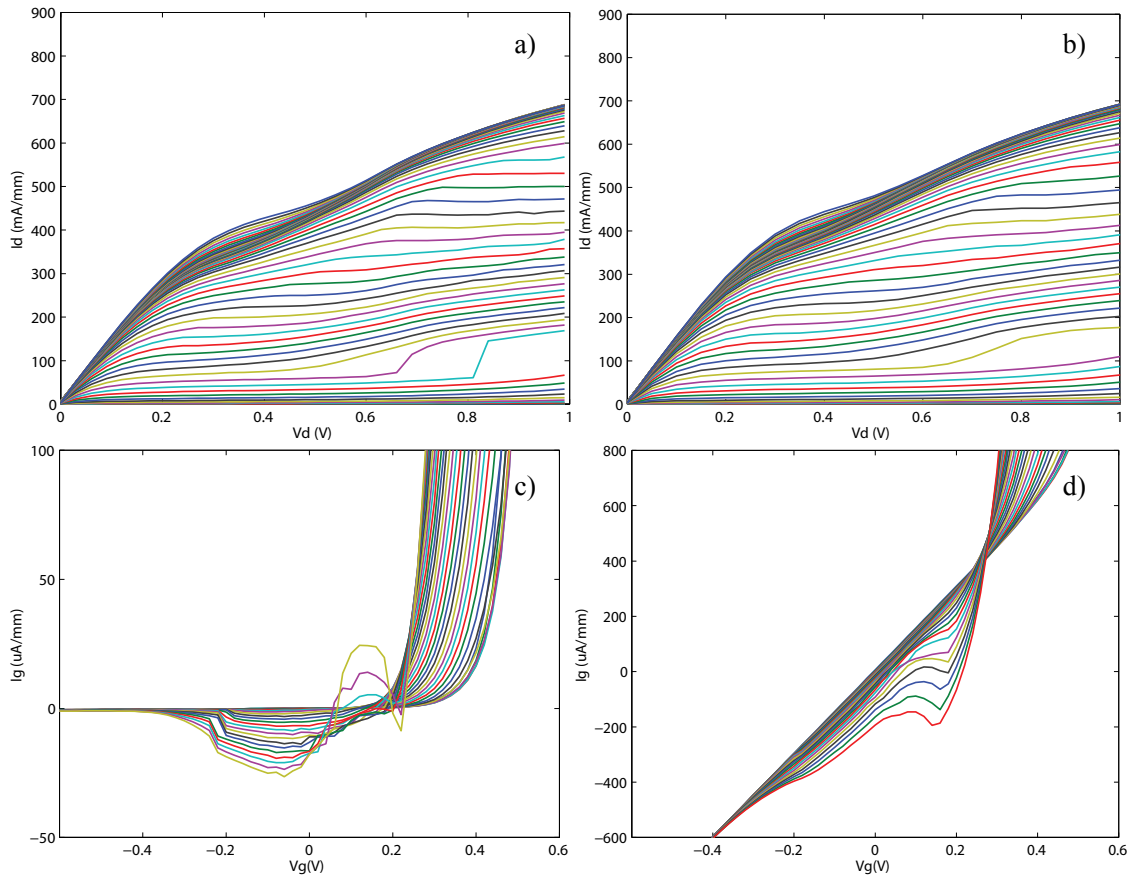
Figure 4.13 DC Characterization comparison for 4 x 50 B device a), c) before and b), d) after FIB experiment. a), b) are I_d-V_d curves and c), d) I_g-V_g curves.

4.5 Layout experiments

Based on the measurements done before, a new batch of devices with 15 different layouts was fabricated and measured. It is found that there were mainly two factors that could influent this dispersion problem a lot: airbridge design and gate finger lay-out. Images for all layouts were illustrated in Chapter 3.

4.5.1 Airbridge Design Influence

To obtain a full picture of the airbridge layout influence, devices with different sized and positioned airbridges have been investigated. Figure 4.13 a) and b) show the dc characterization of reference sample (B) which performs almost normal at 250*K*. It can be observed from Figure 4.13 c) and d) that the E layout with the airbrige moved away from the gate pad and towards the drain pad has an adverse effect on device's performance. Layout C which has an airbridge outside the gate area on the gate side, layout F with gate airbridges over the source conductor, and layout G with drain airbridges over the source conductor, all show similar behavior and temperature dependence. But more importantly, all these three structures have a more serious dispersion problem.
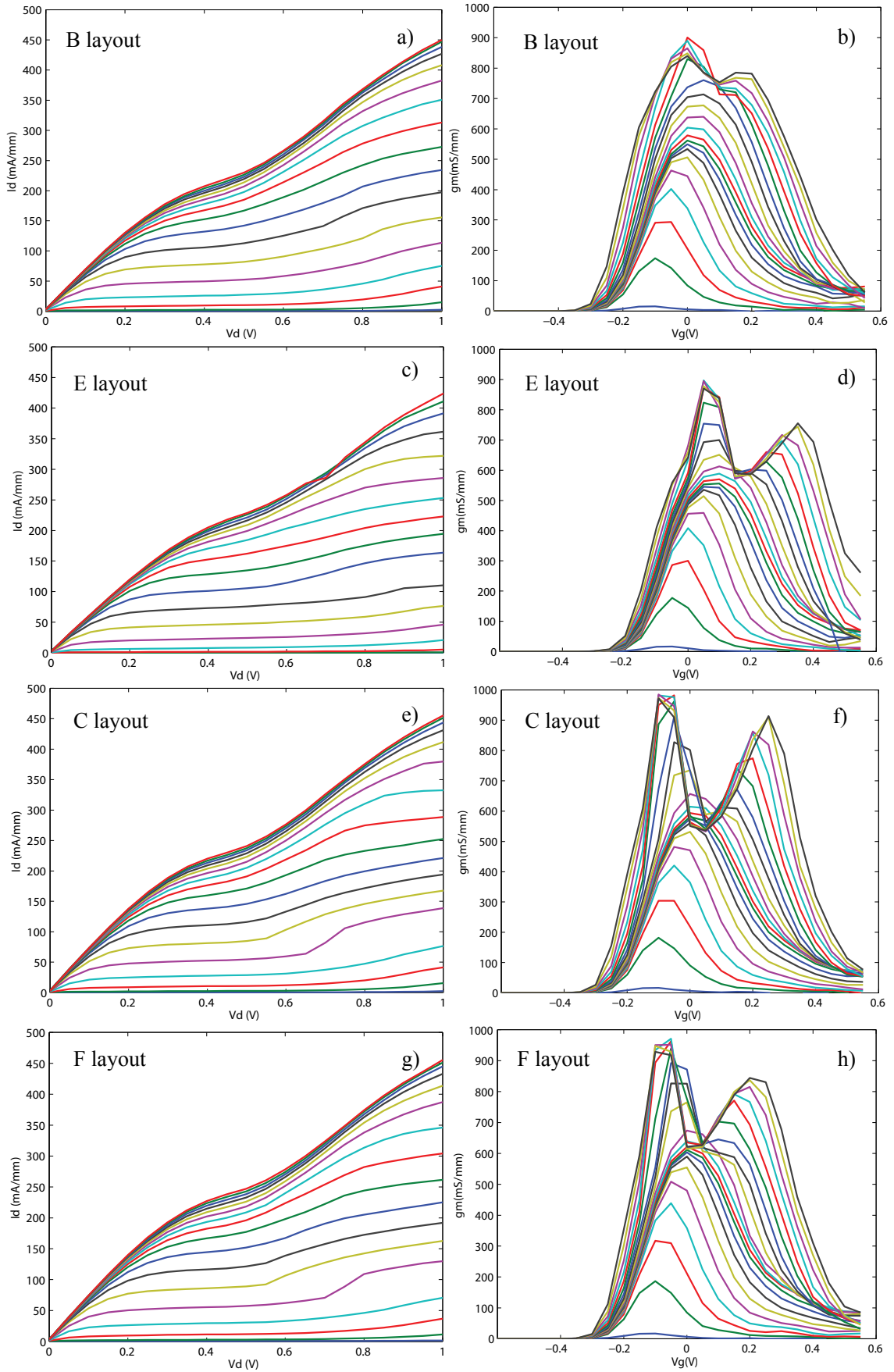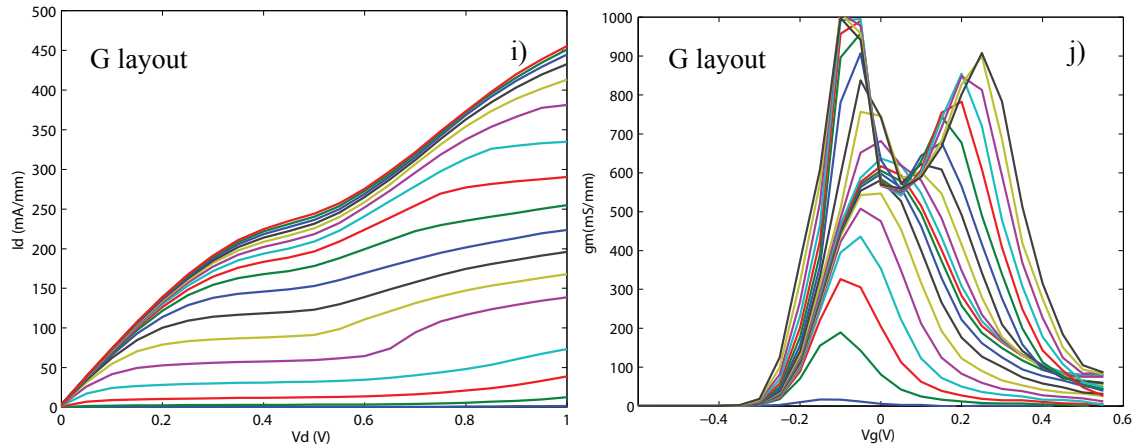
Figure 4.13 DC behavior for a), b) B (reference) layout , c), d) E layout, e), f) C layout, g), h) F layout, and i), j) G layout at 250 K. a), c), e), g), i) are the I_d-V_d curves and b, d), f), h), j) are the g_m-V_g curves

If the airbridge is instead broadened or doubled, as in layout H and I respectively, the dispersion problem is largely improved as shown in Table 4.3. Listed in the table is the comparison between the reference layout B, layout H and I. The starting T in the table means the temperature at which the problem starts to show up in *I-V* characterizations. The data obtained shows that by increasing the airbrige size, the starting temperature for dispersion problem is lowered down to 150K which indicates that the dispersion problem is suppressed. A comparison between H and I has also been done as illustrated by Figure 4.14 where graph a) and b) are the DC curves for H layout at 150K and graph c) and d) are that for I layout at the same temperature. It can be concluded that device with broadened airbridge possesses a more improved performance than device with a double airbridge.

Table 4.3 Comparison of dispersion problem starting temperature among B, H and I layout

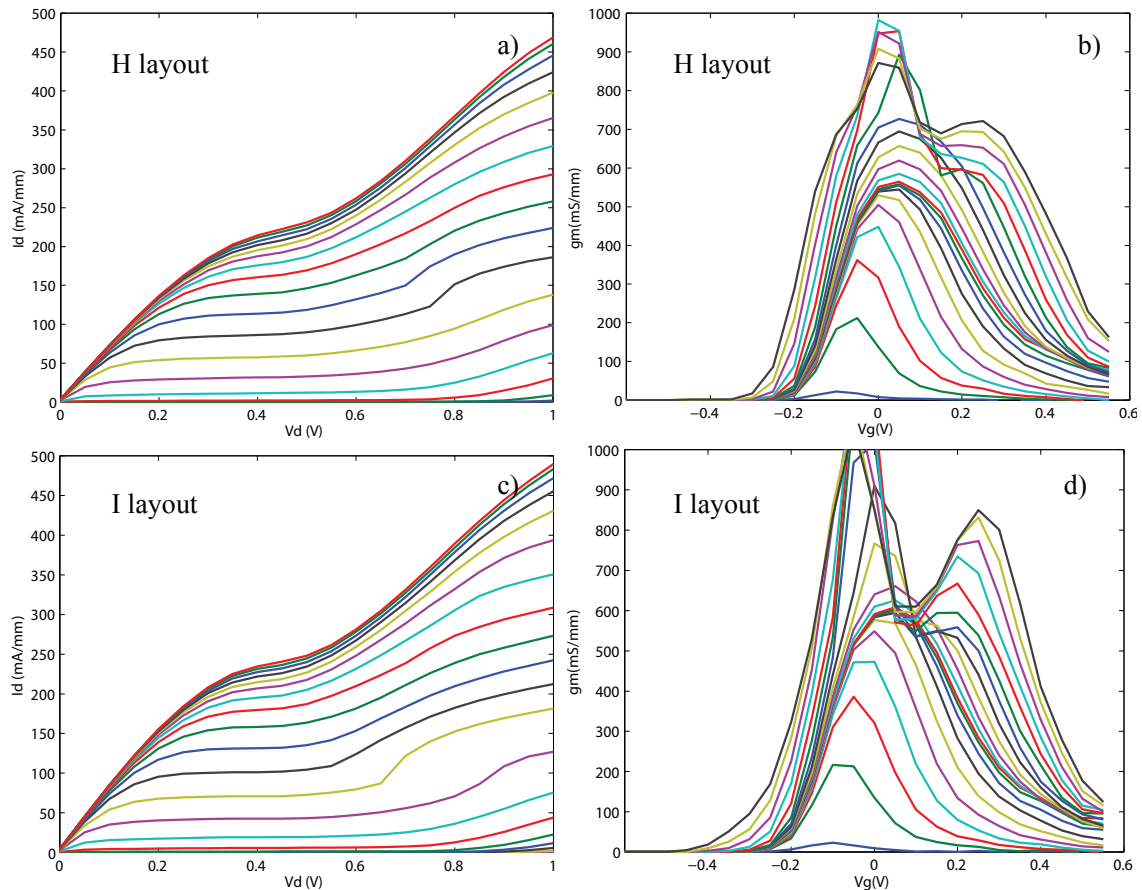| Lay-out	Starting T
H1302_4X50B	250K
H1302_4X50H	150K
H1302_4X50I	150K

Figure 4.14 DC behavior for a), b) H layout and c), d) I layout at 150 K. a), c) are the I_d-V_d curves and b, d) are the g_m-V_g curves

4.5.1 Gate Finger Design Influence

Inspired by DC measurements of the H1005 batch and of the devices obtained after FIB experiments, changes on gate finger design have been performed to further verify the results. Figure 4.15 a) and b) show the reference layout which has good behavior at room temperature.

By make the spacing between each two fingers asymmetric in Figure 4.15 c) and d), the dispersion problem becomes much worse even at room temperature. Moreover, making trenches on the gate pad to increase L_{in} has a more serious influence on device's performance shown in Figure 4.15 e) and f). It's obvious that the V_g needed for a dispersion step is very near the threshold voltage and the V_d range of the step zone is largely increased. The results by changing these two parameters points to the odd mode oscillation. It has been explained in Chapter 2.2.2 that the odd mode oscillation in muti-finger device is closely related to parameters L_{in}, L_{asy} and L_{out}. An increasing of L_{in} and L_{asy} can give a more serious odd mode oscillation. D layout changes the gate finger by rotating the gate finger with 90° and it also shows a worse dispersion problem. Moreover, the kink in the gm curve is very interesting since it occurs at earlier stage at the increasing part of gm curve.
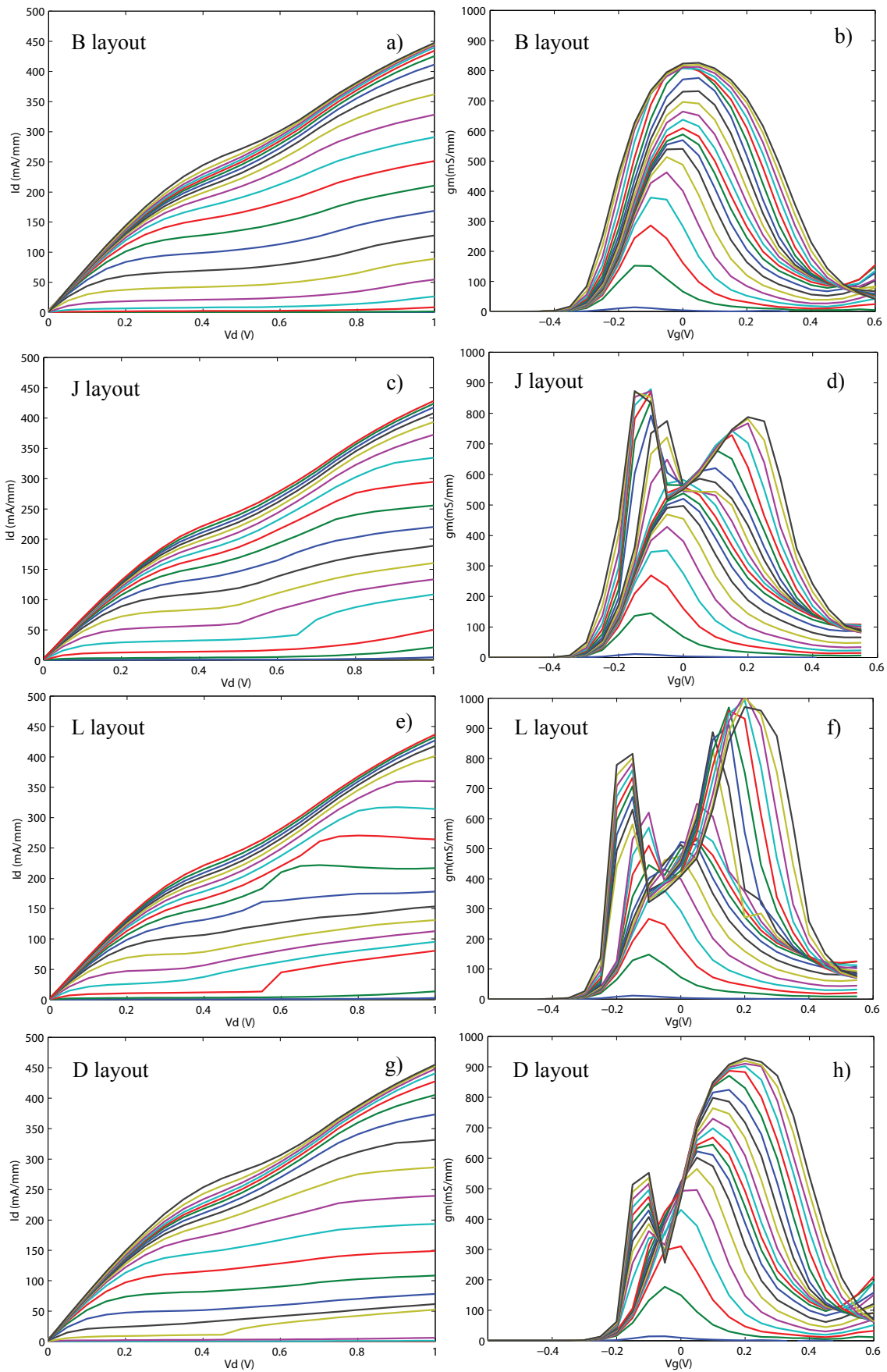
Figure 4.15 DC behavior for a), b) B (reference) layout, c), d) J layout, e), f) L layout and g), h) D layout at 300 K. a), c), e), g) are the I_d-V_d curves and b), d), f), h) are the g_m-V_g curves

Table 4.4 illustrates the influence of gate finger-spacing. B structure is the reference structure with $11\mu m$ spacing and the starting temperature for the dispersion problem is around 250K. By decreasing the gate finger spacing to $7\mu m$ (M layout), the dispersion problem is effectively suppressed. It behaves good even lower temperature down to 5K. However is further scaling down the finger spacing to 5.2 μm (N) structure, the dispersion problem doesn't get better but rather it shows up at 70K.

However, even though that by decreasing the finger spacing (M, N, and S), a significant improvement has been obtained on dispersion problem, the drain current and transconductance is very low which limits device performance. The maximum drain current can only reach near 300mA/mm for M layout and around 350mA/mm for N and S. Moreover, though other structures has a higher drain current and transconductance than these three. Still it's around 200mA/mm lower for the reference layout B than device with the same gate finger number, finger length and spacing in H1005 batch. The only difference is the added Y-connection which is supposed to function as an element to reduce the asymmetry in device thus improving the performance in this new batch. However, it seems that it doesn't really help to suppress the dispersion problem.

To further explore the reason for the low value of drain current and transconductance, measurements have been done to check the contact resistance and sheet resistance. It was found out that both the contact resistance and sheet resistance have an abnormally high value which indicates problems during processing. It's hard to say if the improvement by gate spacing scaling is also related to the low drain current and transconductance or if they are actually one important reason for suppressing the dispersion problem. But the difference for M and N dc behavior, both possessing similar level of drain current and transconductance, shows that gate spacing decreasing is one essential factor to improve device's performance.

One suggestion from the new batch results is to combine the airbridge influence with the gate finger spacing influence. Choosing a gate finger spacing around $7\mu m$ with broad airbrige might be an optimal lay-out to suppress the low frequency dispersion problem as well as obtaining a reasonable drain current and transconductance. Moreover, Y-connection could be removed since it doesn't add anything to the performance.

Table 4.4 Comparison of dispersion problem starting temperature among B, M, N and S layout

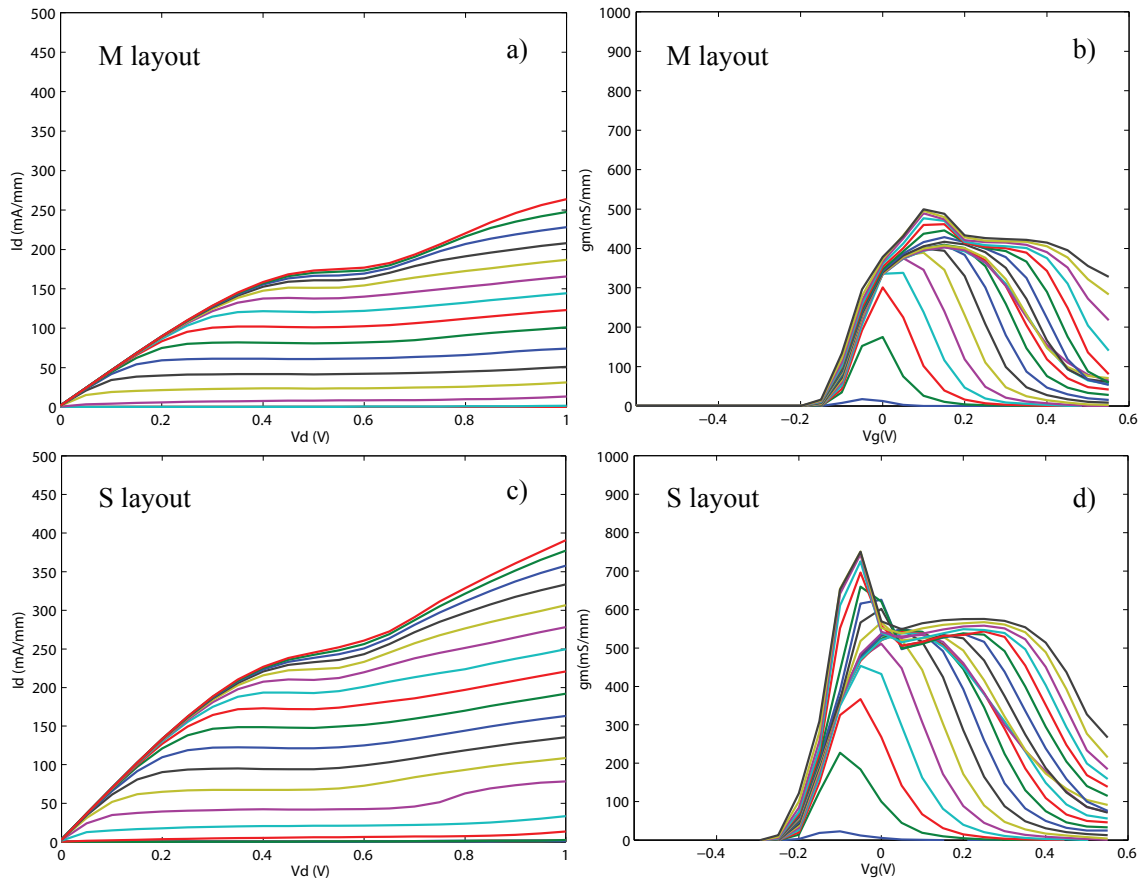| Lay-out	Starting T
H1302_4X50B	250K
H1302_4X50M	Good at 5K
H1302_4X50N	70K
H1302_4X50S	30K

Figure 4.16 DC behavior for a), b) M layout and c), d) S layout at 5 K. a), c) are the I_d-V_d curves and b, d) are the g_m-V_g curves

Chapter 5

Conclusion

A low dispersion problem was found for InP HEMTs at cryogenic temperature. DC, RF characterization, Pulsed Measurement, Spectrum Analysis and FIB experiments were done to investigate the low frequency dispersion problem.

The low frequency dispersion problem studied in this work presents on dc characterization as a sudden drain current jump in I_d-V_d curve and an abnormal kink in gm curves. Moreover, a "step zone" or "forbidden zone" shows in I_d-V_d curve when increases the V_d range and decreasing V_g sweeping step during measuring and it suggests that the size of this step zone indicates the extent of this dispersion problem.

5.1 DC measurements

Two dependences are found in DC measurements: temperature dependence and structure dependence.

The DC results obtained show that the dispersion problem gets worse with decreasing temperature presented as larger kink on g_m-V_g curve and increase step zone size. Gate voltage V_g needed for drain current jump shifts down in I_d-V_d curve when temperature falls until it reaches threshold voltage.

In structure dependence, three structure parameters, gate finger width, number and spacing, have been found out to be close related to the dispersion problem. It can be concluded from the obtained data that the devices shows a more serious dispersion problem when the gate finger width, gate finger number or finger spacing is increased.

A mysterious bump has been examined in I_g-V_g curve presents as an unknown positive gate current. This bump is believed to have a relationship with impact ionization. Moreover, this mysterious bump only shows up in device with gate finger spacing of $21\mu m$ and $31\mu m$. It never shows up for device with $11\mu m$ spacing no matter how low the temperature reaches.

5.2 RF measurements

In RF characterization, an abnormal spike has been seen at low frequencies in S_{21}. It seems that the low frequency dispersion problem presents in I_d-V_d curve as sudden drain current jump and presents in S-parameter curves as a corresponding spike. This will be followed by a curl-up effect in S_{11} and S_{22} curve and ripples in S_{21}.

5.3 Pulsed measurements

The pulsed measurement results differ with initial bias point and pulse length. When the pulse the device from low initial bias point (<-0.3 V), the step starts to disappear in the I-V curve.

The H1006 batch with better surface passivation technology was tested. However, no big difference was found in the DC characteristics compared to the old batch which indicates that if trap is the one of the reason for the dispersion problem, the position of the trap is not on the surface in connection with the passivation.

5.4 Spectrum Analysis

In spectrum analysis, three tests were performed to check the oscillation signal. In the first test no signal was observed with frequency sweeping from 30 *GHz* to 110 *GHz* and device biased around the drain current jump. In the second and third tests, the PNA power and out-put power was increased respectively, but still no signal was obtained. This indicates that either there is no oscillation or the frequency of oscillation is at very high frequency or really low frequency.

5.5 Odd Mode Oscillation Investigation

To indirectly check the odd mode oscillation, FIB surgeries were done on devices in H1005 batch. For 4 x 50 A device, trenches were made on the gate pad between the gate fingers to increase L_{in}. And for 4 x 50 B devices, the passivation layer was removed and a metal layer was deposited to short the gate inputs thus achieving reduced L_{in}. By comparing the DC characterization of these devices before and after FIB, differences were observed which indicate the existence of odd mode oscillation. However, the extent of improvement or degradation after FIB is far from expected.

5.6 Layout Experiments

Two designs have been found to play very important role in dispersion problem: airbridge design and gate finger design.

Both the size and position of the airbridge can influence the dispersion problem a lot and by broadening or doubling the airbridge, the device's performance can be largely improved.

Among different gate finger layout, device with asymmetric finger spacing layout or large L_{in} and L_{out} design have great adverse impact on the dispersion problem. While by reducing the gate finger spacing, the dispersion problem decreases. When the gate finger spacing is scaled to 7 *μm*, the dispersion problem is significantly suppressed. However, another problem, low drain current and transconductance pops up for structure with small finger spacing. It still not certain if this is because of processing problem.

Chapter 6

Future Work

Lots of measurements have been performed on investigation of this dispersion problem. Unfortunately no final conclusion has been achieved yet. But the results are very valuable for preceding the investigation. From the pulsed measurements, the dispersion problem was proved to be related to traps. So a look at the deep level trap in the buffer layer or the substrate would be worthwhile. Moreover, the new batch results showed a significant suppression of the dispersion problem. A layout of 4 x 50 μm with spacing around $7\mu m$ and broadened airbridge is suggested to obtain good performance at cryogenic temperature. In addition, since the airbridge structure and gate finger separation plays an important role in this dispersion problem, some kind of oscillation needs to be involved. Therefore an investigation of high frequency odd-mode oscillations and simulations of current flow and distribution in the airbridge would be interesting.

Acknowledgement

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