High-Speed VCSELs With Strong Confinement of Optical Fields and Carriers

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***Abstract*—We present the design, fabrication, and performance of our latest generation high-speed oxide-confined 850-nm vertical-cavity surface-emitting lasers. Excellent high-speed properties are obtained by strong confinement of optical fields and carriers. High-speed modulation is facilitated by using the shortest possible cavity length of one half wavelength and placing oxide apertures close to the active region to efficiently confine charge carriers. The resulting strong current confinement boosts internal quantum efficiency, leading to low threshold currents, high wall-plug efficiency, and state-of-the-art high-speed properties at low bias currents. The temperature dependent static and dynamic performance are analyzed by current-power-voltage and small-signal modulation measurements.**

***Index Terms*— Dynamics, high efficiency, high-speed modulation, optical interconnects, semiconductor lasers, vertical-cavity surface-emitting lasers (VCSELs).**

I. Introduction

VERTICAL-cavity surface-emitting lasers (VCSELs) are extensively used in short-reach multimode fiber (MMF) optical interconnects in data centers and supercomputers. Today, a single supercomputer may use several million optical interconnects and near-future systems are expected to employ tens or hundreds of million interconnects operating at 25 to 50 Gbit/s [1, 2]. Further into the future, terabit optical interconnects may require even higher channel rates. As no active cooling can be used due to high power consumption and cost, future optical interconnects require VCSELs with excellent high-speed properties also at high temperatures.

The last few years have seen an impressive improvement in the performance of high-speed short-wavelength VCSELs emitting at 850-980-1060 nm. Current records for back-to-back transmission (a few meters of multimode fiber) are compiled in Table I. Our previous generation high-speed VCSELs could transmit error-free (bit-error-ratio (BER)<10^{-12}) at bit rates up to 57 Gbit/s using non-return-to-zero on-off keying [3]. By using equalization, the bit rate could be boosted to 71 Gbit/s at room temperature (RT) and 50 Gbit/s at 90°C [4, 5]. Without equalization, high bit-rate, high-temperature transmission at 46 Gbit/s at 85°C has been demonstrated using 980 nm VCSELs with 23 GHz bandwidth at high temperature [6]. Research exploring unconventional VCSEL structures, with coupled cavities for multiple resonance peaks, have demonstrated bandwidths up to 37 GHz [7, 8]. So far only limited data transmission experiments have been presented using such devices [8].

TABLE I
SHORT-WAVELENGTH VCSELS FOR OPTICAL INTERCONNECTS

Group	λ (nm)	BW (GHz)/ BR (Gbit/s)	T (°C)	Energy eff.	Year [Ref.]
High bandwidth					
Chalmers[a]	850	30	RT		2015 [11]
UIUC[b]	980	37	RT		2015 [7]
TU Berlin	980	23	85		2014 [6]
High bit rate					
Chalmers	850	57	RT		2013 [3]
IBM-Chalmers[c]	850	71	RT		2015 [4]
TU Berlin	980	46	85		2014 [6]
IBM-Chalmers[c]	850	50	90		2015 [5]
Energy efficiency - VCSEL only					
TU Berlin	850	25	RT	56 fJ/bit	2012 [9]
Chalmers[a]	850	40	RT	73 fJ/bit	2015 [11]
Chalmers[a]	850	50	RT	95 fJ/bit	2015 [11]
TU Berlin	980	35	85	139 fJ/bit	2014 [12]
TU Berlin	980	38	85	177 fJ/bit	2014 [13]
Energy efficiency - full link					
IBM-Sumitomo	850	25	RT	1.0 pJ/bit	2013 [10]
IBM-Sumitomo	850	35	RT	2.7 pJ/bit	2013 [10]

[a]The VCSEL design presented in this paper. [b]With a coherent VCSEL array. [c]Using equalization.

In addition to high bit rates, the massive number of interconnects in data centers makes energy efficiency and low cost pressing issues. The energy efficiency of VCSELs is commonly quantified as the dissipated heat energy in the VCSEL per transmitted bit, denoted as the heat-to-data-ratio (HDR), and calculated as $HDR = \left(P_{\mathrm{el}} - P_{\mathrm{opt}}\right)/BR$, where P_{el} is the electrical DC power fed to the VCSEL, P_{opt} is the optical output power, and BR is the bit rate [9]. To make future systems feasible, the entire optical interconnect (laser driver, VCSEL,

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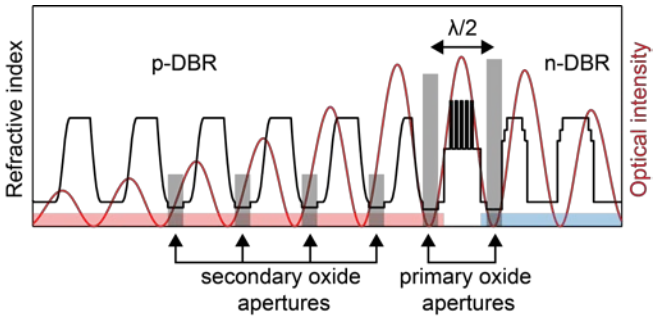

Fig. 1. Refractive index profile and simulated optical field intensity inside the VCSEL cavity. The position of the 30-nm-thick primary $Al_{0.98}Ga_{0.02}As$ and four secondary $Al_{0.96}Ga_{0.04}As$ oxide apertures are indicated. The *p*- and *n*-DBRs feature graded and step-index interfaces respectively.

photodetector, and receiver electronics) should consume at most 1 pJ/bit even at high bit rates [1]. Previously, the energy consumption of the electronics have vastly exceeded that of the VCSEL, but energy-efficient circuits in 32-nm SOI CMOS have recently been demonstrated that make even the few 100 fJ/bit dissipated by the VCSEL important. Researchers at IBM and Sumitomo have demonstrated a full 850-nm VCSEL-based link at 25 Gbit/s with a total energy consumption of 1 pJ/bit, of which the VCSEL dissipated 36% (357 fJ/bit) [10]. Recent published results have demonstrated VCSELs dissipating less than 100 fJ/bit at 25 to 50 Gbit/s at RT [9, 11]. However, at higher temperatures energy dissipation is still more than the twice the values at RT, as seen in Table I [12, 13].

Many of the advantages of VCSELs stem from the fact that their modal and active region volumes are small compared to edge emitting lasers. This enables VCSELs to reach high modulation bandwidths at low bias currents and low power consumption, making them ideal for the massive number of optical links in a data center or a supercomputer. In this paper we explore the limits of optical and electrical confinement by using the shortest possible cavity length and placing the current aperture as close as possible to the active region. High-speed data transmission using 980 nm VCSELs with similar confinement have previously been demonstrated [6, 14]. We investigate the temperature dependent dynamic and static performance of our latest generation of high-speed oxide-confined 850-nm VCSELs with a focus on the impact of the short cavity and strong current confinement. These devices have recently demonstrated record-high small-signal modulation bandwidths of 30 GHz at RT using a 3.5 µm oxide aperture [11]. High bandwidths at low currents enabled data transmission at record energy efficiencies with HDRs of 73 fJ/bit at 40 Gbit/s and 95 fJ/bit at 50 Gbit/s, using direct current modulation and on-off keying, in a back-to-back configuration.

The paper is organized as follows. Section II details the VCSEL design and fabrication. The static performance and effects of the strong carrier confinement are covered in Section III. The dynamic characteristics are presented and analyzed in Section IV, followed by a conclusion in Section V.

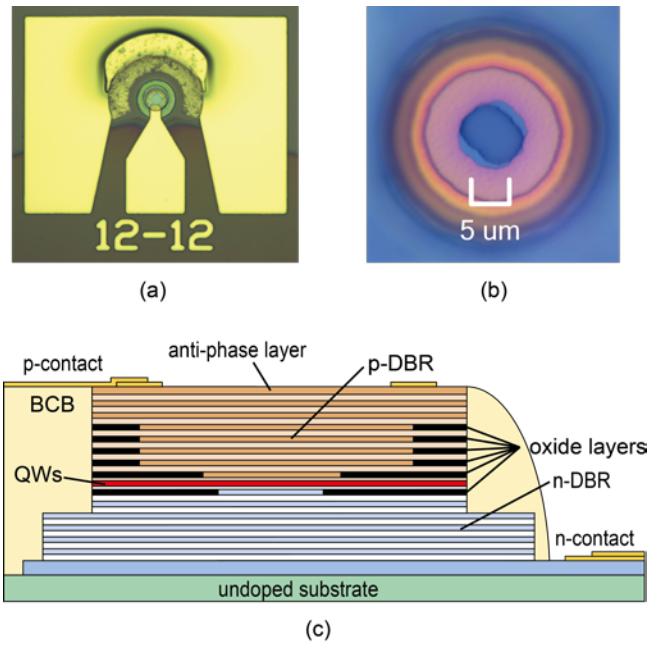

Fig. 2. (a) Microscope picture of fully processed high-speed VCSEL with high-frequency GSG-bondpads. (b) Etched mesa with visible upper (light blue) and lower (dark blue) oxide apertures showing different oxidation lengths. (c) Schematic cross-section of the VCSEL structure.

II. Design and Fabrication

A. Design

The VCSEL design is a further development of our previous generation high-speed VCSELs [3, 4, 5, 15]. The VCSEL structure was grown by MOCVD at IQE Europe on a semi-insulating GaAs substrate. For high differential gain, the active region consists of five compressively strained 4-nm-thick $In_{0.10}Ga_{0.90}As$ quantum wells (QWs), separated by 6-nm-thick $Al_{0.37}Ga_{0.63}As$ barriers. The photoluminescence peak (PL) is at 837 nm, whereas the etalon wavelength is 849 nm, giving a -12 nm PL-to-etalon wavelength offset. The active region is positioned in a thin separate confinement heterostructure at the center of a half-wavelength ($\lambda/2$) thick cavity, see Fig. 1. This means that the distance between the *p*- and *n*-DBR is $\lambda/2$, which is the shortest possible cavity length (the next possible cavity length is $3\lambda/2$). The short cavity improves the longitudinal confinement factor (Γ=0.033) and reduces the transport time across the intrinsic region compared to a $3\lambda/2$ cavity [15].

The top distributed Bragg reflector (DBR) is *p*-doped with carbon and features 21 pairs of mainly $Al_{0.90}Ga_{0.10}As/Al_{0.12}Ga_{0.88}As$ with graded interfaces and modulation doping optimized for low free-carrier absorption and low resistance. The top GaAs contact layer has an optical thickness of $\lambda/2$ for an anti-phase reflection at the surface to enable post-fabrication tuning of the photon lifetime [16] as well as mode-filter integration [17]. The bottom *n*-doped DBR has 29 pairs with step-index interfaces and modulation doping with silicon. The first four pairs are $Al_{0.90}Ga_{0.10}As/Al_{0.12}Ga_{0.88}As$ to avoid oxidation of the bottom DBR during fabrication. The remaining 25 pairs are binary-

ternary AlAs/$Al_{0.12}Ga_{0.88}As$, where AlAs is used to improve thermal conductivity, as compared to using an all ternary DBR.

Transverse optical and current confinement is provided by two primary oxide apertures formed by selective wet oxidation of 30-nm-thick $Al_{0.98}Ga_{0.02}As$ layers. These are positioned as close to the QWs as possible; at the first nodes of the standing optical field on either side of the QWs, see Fig. 1. This design minimizes the lateral spreading of carriers in the intrinsic region and thereby promotes a high internal quantum efficiency. In our previous high-speed VCSEL generation we used a short $\lambda/2$-cavity and oxide layers positioned further away from the QWs (at the second and third field nodes in the *p*-DBR). This lead to a relatively large current spreading under the oxide aperture, thereby preventing those carriers from contributing to the stimulated emission process, and resulted in larger threshold currents and lower internal quantum efficiency [15]. Relative to the previous design a large strain gradient is likely present in the short space between the compressively strained InGaAs QWs and the tensile strained oxide layers, see Fig. 1. Whether this compromises reliability remains to be investigated. Four 30-nm-thick $Al_{0.96}Ga_{0.04}As$ layers form shallow, secondary oxide apertures which reduce the mesa capacitance [16, 18].

B. Fabrication

The VCSELs (Fig. 2) were fabricated using standard processing steps for oxide-confined GaAs-based VCSELs. First, Ti/Pt/Au top contact rings were evaporated on the highly doped ($5.5 \cdot 10^{19}$ cm^{-3}) *p*-type GaAs contact layer. VCSEL mesas with diameters of 22, 24, 26, and 28 µm were dry etched by inductively coupled plasma (ICP) reactive ion etching (RIE) using a $SiCl_4$/Ar gas mixture. An *in-situ* laser interferometer end-point system was used to precisely control the etch depth. This is necessary in order to expose the $Al_{0.98}Ga_{0.02}As$ layers without etching into the binary AlAs layers in the bottom DBR, which would oxidize rapidly if exposed during the oxidation process. Prior to oxidation Si_xN_y was deposited on the sample in order to prevent undesired oxidation of the mesa and chip surfaces. The Si_xN_y on the mesa sidewalls was removed using NF_3 plasma etching and the oxide aperture was formed in a wet oxidation furnace at 420°C. Different oxidation rates were observed on the *p*- and *n*-side, resulting in two primary oxide apertures with slightly different size, see Fig. 2(b). In addition, an angular dependence of the oxidation rate was seen on the *n*-side, resulting in an elliptical oxide aperture. Non-circular oxide apertures have previously been reported in e.g. [19, 20]. The somewhat larger *p*-side oxide aperture was found to be circular. The oxide aperture diameter mentioned in this paper refers to the effective diameter of a circle with the same area as the smaller, elliptical aperture on the *n*-side. The $Al_{0.90}Ga_{0.10}As$ layers surrounding the oxide layers oxidize vertically from the $Al_{0.98}Ga_{0.02}As$ layer, increasing the oxide layer thickness from ~30 nm to ~50 nm. This helps in further reducing mesa capacitance. After oxidation, a 50-µm-diameter second mesa was dry etched through the bottom DBR down to the 1-µm-thick GaAs *n*-contact layer. A Ni/Ge/Au *n*-contact was deposited using electron beam evaporation and annealed in a rapid thermal annealing system at 430°C for 30 s in an inert N_2 atmosphere. After this the remaining contact layer underneath the signal bondpad was etched away using the ICP dry etch, exposing the semi-insulating GaAs substrate, in order to reduce the parasitic bondpad capacitance. Before planarization with a thick layer of benzocyclobutene (BCB), a layer of Si_xN_y was deposited to improve BCB adhesion. After hard cure, the BCB was patterned with photoresist and etched back to expose the top mesa and bottom contact using CF_4/O_2 ICP/RIE etching. To avoid burning of the resist during the BCB etch, the chip was attached to a sapphire carrier using thermally conductive cooling grease and the carrier backside was cooled by a He-flow during the etch. The cooling grease significantly improves the thermal conductivity between the chip and carrier and facilitates a high BCB etch rate and effortless resist removal. Ti/Au bondpads in a ground-signal-ground (GSG) layout were sputtered onto the planarized VCSEL structure. As a final step, the chip was cleaved into four pieces for fine tuning of the photon lifetime by a shallow etch of the top DBR. This was done in order to optimize the top DBR reflectivity (top mirror transmission loss) for optimal bandwidth and output power [16]. A precise Ar-ion milling etch was used to etch 11, 20, 37, and 54 nm with an estimated accuracy of ±1 nm. To keep a good correlation between the simulated and experimental characteristics for extraction of internal parameters, it is essential to protect the mesa surface during fabrication to avoid unintentional etching or contamination with, for instance, resist residues. The mesa surface was protected by Si_xN_y during most of the processing steps and the chip was thoroughly cleaned during resist removal using standard solvents, O_2 ashing and ozone cleaning.

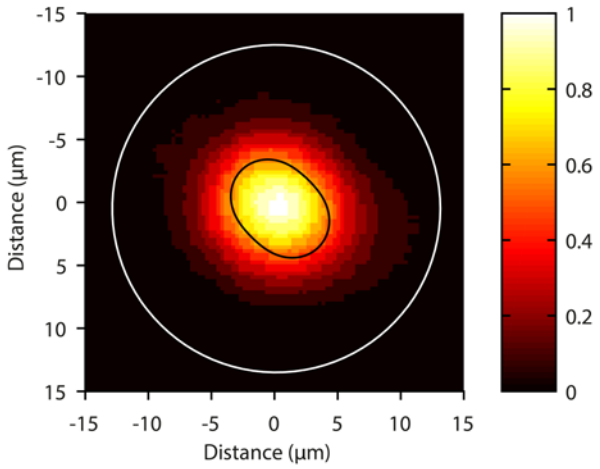

Fig. 3. Normalized intensity near-field image of a 7.5 µm oxide aperture VCSEL biased at 0.75 times the threshold current. The VCSEL mesa is outlined in white and the approximate oxide aperture is shown in black.

III. Static Performance

The static performance was analyzed by measuring the current-power-voltage (IPV) using a large-area calibrated silicon photodetector with the VCSELs on a temperature-controlled heat-sink. The VCSELs with a surface etch depth of 20 nm were chosen for a more detailed study as they had the highest bandwidth at room temperature (see Section IV). When

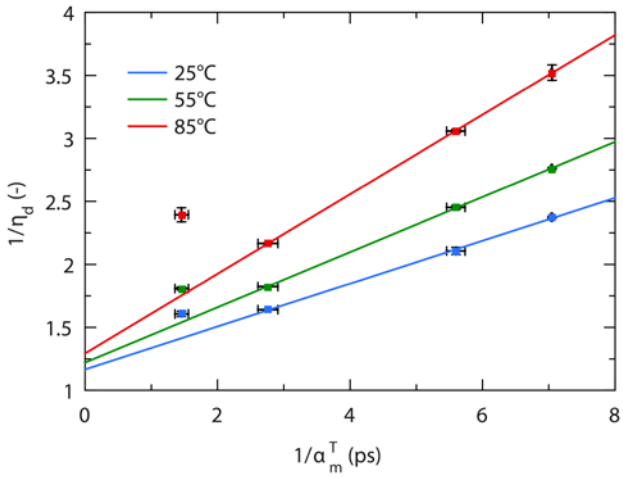

Fig. 4. The inverse of the differential quantum efficiency vs. the inverse of the top mirror loss rate with linear fits to extract internal quantum efficiency and optical loss for 7.5 µm aperture VCSELs. Several devices were measured at each point, shown by standard deviation vertical error-bars. Horizontal error-bars represent an uncertainty in etch depth of ±1 nm.

VCSEL with other etch depths are discussed, this will be explicitly stated.

A. *Effects of Strong Carrier Confinement*

The strong transverse confinement of charge carriers was investigated by near-field imaging of the VCSEL below threshold. By measuring the spontaneous emission below threshold using a microscope with a CCD camera, the transverse carrier distribution in the QWs can be indirectly observed. As seen in Fig. 3, the spontaneous emission is well confined within the oxide aperture. The spontaneous emission profile closely resembles a Gaussian with a full-width-at-half-maximum at the oxide aperture edge, albeit with an elliptic perturbation caused by the oxide aperture. The tight confinement leads to a carrier distribution with a good overlap with the optical mode, increasing the stimulated recombination efficiency. This is in contrast to our previous generation short-cavity VCSELs with oxide layers positioned further away from the QWs, where a significant lateral leakage current was observed [15].

The static characteristics of VCSELs with four different surface etch depths (i.e. four top mirror reflectivities) were measured in order to extract the internal optical loss α_i and internal quantum efficiency η_i from the slope efficiency SE. First, the differential quantum efficiency was calculated as $\eta_d = q\lambda/(hc) \cdot SE$, with the elementary charge q, Planck's constant h, and speed of light c. The measured differential quantum efficiency η_d can be related to the cavity losses as

$$\frac{1}{\eta_d} = \frac{1}{\eta_i}\left(1 + (\alpha_i + \alpha_m^B)\frac{1}{\alpha_m^T}\right) \quad (1)$$

where α_m^T and α_m^B are the top and bottom mirror transmission loss rates. Using a 1-dimensional effective-index model to calculate α_m^T and α_m^B [21], the internal optical loss and internal quantum efficiency can be extracted from a linear fit of (1) as seen in Fig. 4. The devices etched only 11 nm (the leftmost points in Fig. 4) were omitted from the fit since the high cavity losses associated with the anti-phase layer results in a large threshold carrier density, which in turn leads to excessive carrier leakage from the QWs and reduced η_i. Values from the fits are shown in Table II. The high internal quantum efficiency of 86% at room temperature for a 7.5 µm oxide aperture VCSEL indicates that the close proximity of the oxide layers to the QWs effectively confines the carriers to the active region. This is a significant improvement compared to the 65 to 70%

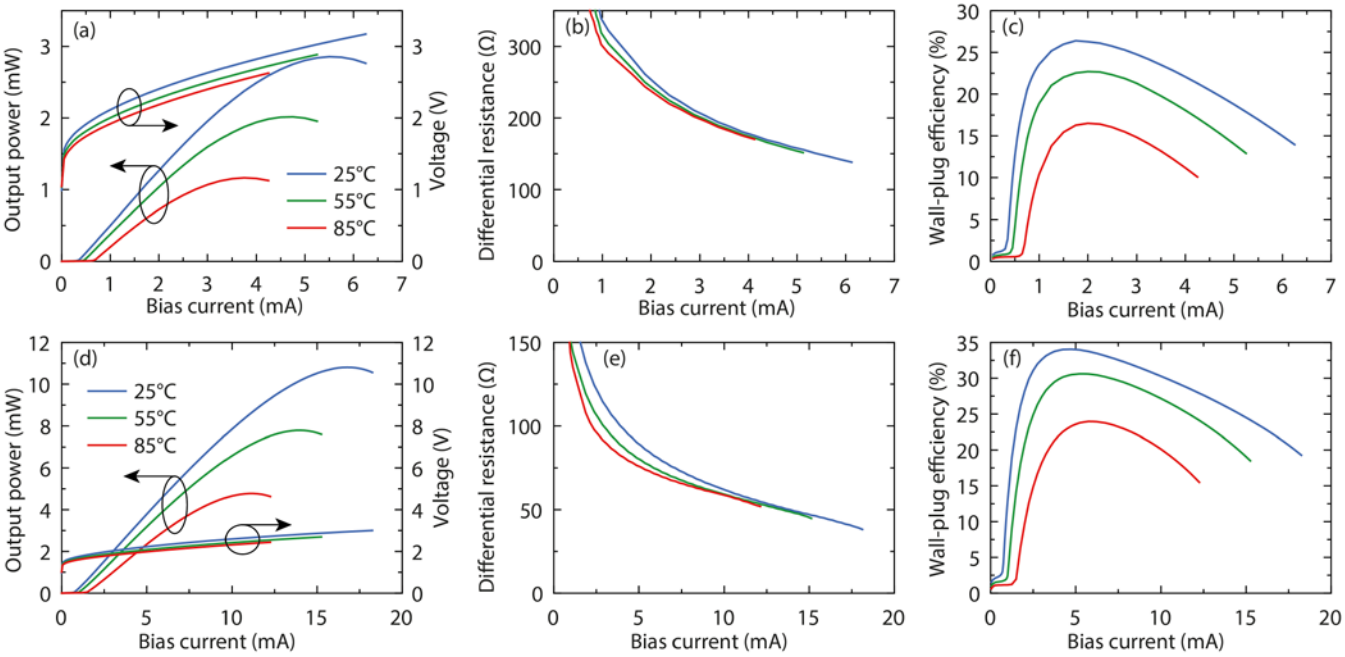

Fig. 5. Temperature dependent static characteristics as a function of bias current for a 3.5 (a)-(c) and a 7.5 µm (d)-(f) oxide aperture VCSELs. Left: output power and voltage. Middle: differential resistance. Right: wall-plug efficiency.

TABLE II
STATIC CHARACTERISTICS FOR DIFFERENT OXIDE APERTURES AND AMBIENT TEMPERATURES

	3.5 µm			5.5 µm			7.5 µm		
	25°C	55°C	85°C	25°C	55°C	85°C	25°C	55°C	85°C
Threshold current (mA)	0.34	0.45	0.65	0.50	0.65	0.93	0.78	1.05	1.52
Slope efficiency (W/A)	0.76	0.69	0.57	0.86	0.78	0.66	0.89	0.80	0.67
Max. output power (mW)	2.9	2.0	1.2	7.0	5.2	3.3	10.8	7.8	4.8
Roll-over current (mA)	5.5	4.8	3.8	11.5	9.8	8.0	16.8	14.0	11.3
Differential resistance[a] (Ω)	178	216	244	80	97	108	55	66	73
	149	187	216	65	85	99	43	58	68
Max. power efficiency (%)	26	23	17	33	30	24	34	31	24
Internal quantum efficiency (%)	81	84	80	81	77	72	86	82	77
Internal optical loss[b] (ps^{-1}/cm^{-1})	0.22	0.32	0.44	0.12	0.16	0.22	0.13	0.17	0.23
	27	40	55	16	20	28	17	21	29
Photon lifetime (ps)	1.7	1.4	1.2	2.0	1.9	1.7	2.0	1.8	1.6

[a]Measured at half roll-over current / at roll-over current. [b]Converted from ps^{-1} to cm^{-1} assuming a group velocity of $8.0 \cdot 10^9$ cm/s.

estimated for our previous VCSEL design [15]. It should be noted that the linear fit assumes η_i and α_i to be constant with respect to etch depth (photon lifetime). In reality, the 68-nm-thick highly-doped GaAs contact layer will contribute to excess absorption loss through inter-band absorption for the VCSELs with a small etch depth (thick GaAs layer), resulting in an underestimation of η_i. However, inter-band absorption close to the bandgap is difficult to model. By using only the two rightmost data points in Fig. 4 for the fits (where most of the GaAs contact layer is etched away), this effect can be minimized, resulting in an η_i as high as 94% at RT (using six VCSELs for each point to reduce measurement uncertainty). Therefore, the η_i listed in Table II should be regarded as conservative estimates as the real values are likely higher.

The extracted internal optical loss was found to be similar for the 5.5 and 7.5 µm aperture VCSELs, at 0.12 and 0.13 ps^{-1} at RT. This is only slightly higher than the 0.11 ps^{-1} calculated from the 1D simulation. The model only includes free-carrier absorption, but diffraction loss does not seem significant for the 5.5 and 7.5 µm devices, since they have very similar losses. As expected, the 3.5 µm VCSELs experience higher losses which we attribute to increased diffraction loss from the small oxide aperture. The extracted η_i and α_i for the 3.5 µm VCSELs should be regarded as rough estimates, since a small variation in the oxide aperture diameter on the order of ~0.1 µm, makes the fit unreliable for small-aperture VCSELs. For the larger devices, the relative variation in oxide aperture area is much smaller, making the fits more reliable. The internal optical loss is approximately doubled from RT to 85°C due to larger free-carrier absorption coefficient at higher temperatures. Similar results have previously been reported in [16], and is connected with increased phonon scattering rates resulting in shorter carrier relaxation times. Using the extracted α_i, the photon lifetime τ_p in Table II was calculated as $\tau_p = (\alpha_i + \alpha_m^B + \alpha_m^T)^{-1}$. By assuming a group velocity of $8.0 \cdot 10^9$ cm/s, the loss rates can be converted to loss per unit length, see Table II.

B. Static Characteristics

IPV measurements for typical 3.5 and 7.5 µm oxide aperture VCSELs can be seen in Fig. 5, and figures-of-merit for three oxide aperture sizes (3.5, 5.5, and 7.5 µm) are summarized in Table II. The strong confinement of carriers yields low threshold currents at room temperature of 0.34 mA for the 3.5 µm (3.5 kA/cm^2) and 0.78 mA for the 7.5 µm VCSELs (1.8 kA/cm^2). It should be noted that even lower threshold currents are obtained for VCSELs with a larger part of the anti-phase layer removed (i.e. higher top DBR reflectivity). Etching away the full anti-phase layer gives around 35% lower threshold currents with 0.23 mA for a 3.5 µm oxide aperture (2.4 kA/cm^2) and 0.50 mA for a 7.5 µm aperture (1.1 kA/cm^2). At higher temperatures, the threshold current increases due to increased absorption, reduced internal efficiency, and an increase of the gain-wavelength detuning (lower gain), and is close to twice the RT value at 85°C. The minimum threshold current was measured to be at between 0 and 5°C, indicating that we have a positive gain-wavelength detuning above this point. This is disadvantageous for high-temperature static characteristics since the VCSEL needs to be pumped harder to reach threshold gain than for a negative gain-mode detuning [22]. It may, however, be beneficial for the dynamics, especially at room temperature, since this means operating the VCSEL at the short-wavelength side of the gain peak, where the differential gain is higher [23, 24].

High efficiency due to the strong confinement of carriers contributes to high slope efficiencies for the 5.5 and 7.5 µm VCSELs, exceeding 0.86 W/A at RT. The smaller 3.5 µm device has a lower slope efficiency because of the increased internal losses. Even with the tight confinement of carriers, the differential resistance is only ~50 Ω for the 7.5 µm and ~160 Ω for the 3.5 µm aperture device, see Fig. 5(b) and (e). A low differential resistance is beneficial for both the static characteristics, since it reduces resistive heating, and for the dynamic characteristics as an impedance close to the standard 50 Ω impedance minimizes unwanted microwave reflections, without the need for a customized broadband matching network. The differential resistance is about 30% lower than our previous generation of high-speed VCSELs which use the same DBR designs [15]. This may partly be explained by somewhat higher doping levels than intended, which is consistent with the larger than expected absorption losses.

High internal quantum efficiency, large slope efficiency, low threshold currents, and low differential resistance translates into high output power at low power consumption. This is also seen in the high wall-plug efficiencies (WPE) in Fig. 5(c) and (f).

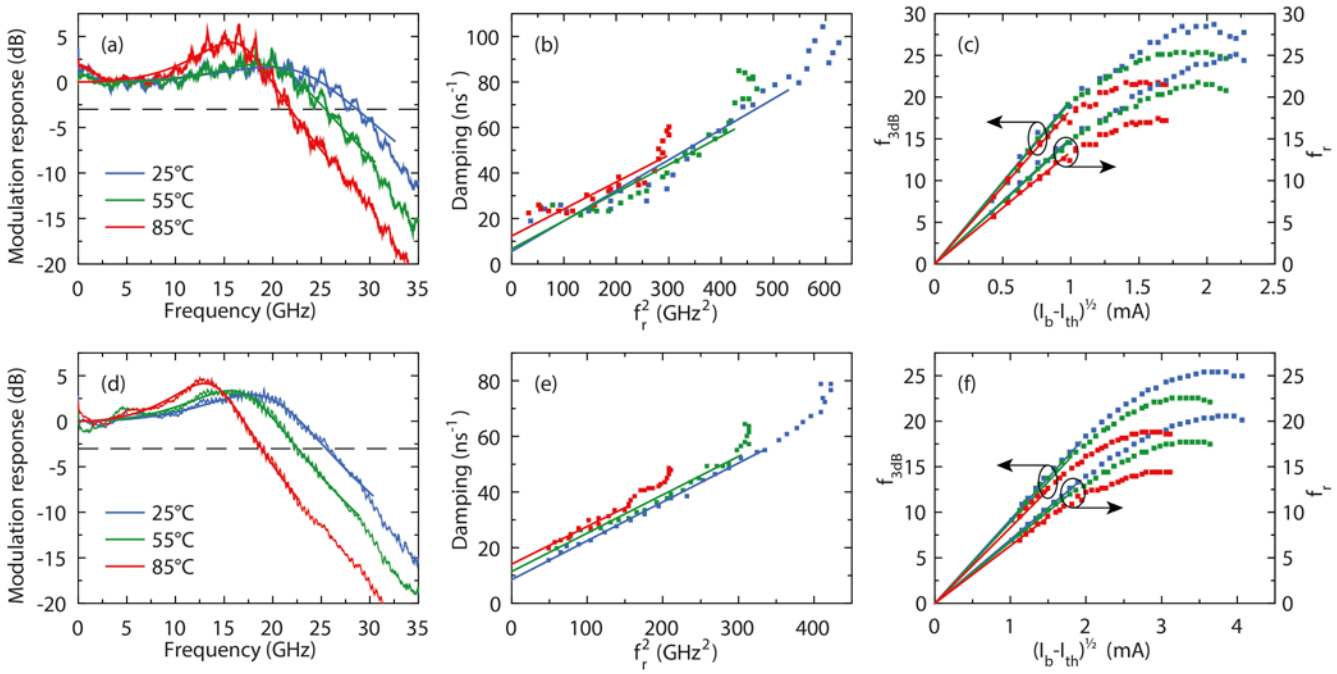

Fig. 6. Temperature dependent dynamic characteristics for a 3.5 (a)-(c) and a 7.5 µm (d)-(f) oxide aperture VCSELs. Left: Small-signal modulation response at maximum bandwidth. Middle: Damping rate vs. resonance frequency squared with linear K-factor fits. Right: 3-dB bandwidth and resonance frequency vs. square root of bias current above threshold with linear D-factor and MCEF fits.

For the 7.5 µm VCSEL, the WPE peaks at 34% at 5 mA and exceeds 32% up to half the roll-over current. The smaller 3.5 µm device WPE peaks at 26% at 2 mA. For energy-efficient data transmission, the VCSELs should be biased at as low current as possible, preferably below half the roll-over current, where these devices show high efficiencies. Placing an oxide layer below the active region was not found to have a significant negative impact on the heat extraction from the active region. A thermal resistance of 2.3 K/mW was measured at RT for the 7.5 µm VCSEL, which is about 10% higher than our previous generation VCSELs with oxide layers only above the active region [5].

IV. Dynamic Characteristics

A. Theory

The dynamics of the resonant photon-carrier interaction in VCSELs is investigated by a small-signal modulation analysis. The small-signal modulation response (S_{21}) can be modelled as a second order damped system described by a resonance frequency f_r and a damping rate γ [25]. The VCSEL parasitics are included by adding an extra pole with a cut-off frequency f_p, giving the full three-pole transfer function

$$H(f) = \text{const} \cdot \frac{f_r^2}{f_r^2 - f^2 + j(f/2\pi)\gamma} \cdot \frac{1}{1 + j\left(f/f_p\right)} \quad (2)$$

where f is the modulation frequency. The parasitic transfer function may also be determined by S_{11} measurements, which also allow fitting values of the parasitic elements to an equivalent circuit model [18]. Intrinsically, the VCSEL bandwidth is damping limited, with the damping increasing linearly with the square of the resonance frequency multiplied by the K-factor as

$$\gamma = Kf_r^2 + \gamma_0 \quad (3)$$

where the offset γ_0 is approximately equal to the inverse differential carrier lifetime [25], and the K-factor can be related to internal VCSEL parameters by

$$K = 4\pi^2\left(\tau_p + \frac{\varepsilon\chi}{v_g(\delta g/\delta n)}\right) \quad (4)$$

where ε is the gain compression, χ the transport factor, v_g the group velocity of light, and $\delta g/\delta n$ the differential gain. The resonance frequency increases linearly with the square root of bias current above threshold according to

$$f_r = D\sqrt{I_b - I_{th}}. \quad (5)$$

VCSELs with a large D-factor and low threshold current reach high resonance frequencies at low bias currents, which enables energy-efficient high-speed modulation. A large D-factor is also important in order to reach a high maximal VCSEL bandwidth, equivalent to reaching a large resonance frequency before current induced self-heating and thermal saturation deteriorates performance. The D-factor can be related to basic internal VCSEL parameters as

$$D = \frac{1}{2\pi}\sqrt{\frac{\eta_i\Gamma v_g}{qV_a}\cdot\frac{\delta g/\delta n}{\chi}} \quad (6)$$

where Γ is the optical confinement factor, V_a the active region volume, and χ the transport factor. Equation (6) clearly shows that the small VCSEL active region volume contributes to high resonance frequencies at low bias currents. It is also obvious

TABLE III
DYNAMIC CHARACTERISTICS FOR DIFFERENT OXIDE APERTURES AND AMBIENT TEMPERATURES

	3.5 µm			5.5 µm			7.5 µm		
	25°C	55°C	85°C	25°C	55°C	85°C	25°C	55°C	85°C
K-factor (ns)	0.13	0.12	0.12	0.14	0.13	0.12	0.14	0.13	0.14
Damping offset (ns^{-1})	5.5	6.6	12.3	7.3	9.1	14.9	8.5	12.4	14.1
Differential carrier lifetime (ps)	180	150	80	140	110	70	120	80	70
MCEF (GHz/mA^{½})	19.6	19.4	18.4	12.7	12.5	11.7	9.2	8.9	8.3
D-factor (GHz/mA^{½})	15.0	14.8	13.4	9.8	9.6	8.9	7.0	6.8	6.3
Max. modulation BW (GHz)	29	26	22	27	24	22	26	23	19
Parasitic pole (GHz)	20	17	17	19	18	21	20	18	19
Max. intrinsic BW (GHz)	63	74	81	63	68	74	63	68	63
Max. thermal BW (GHz)	39	33	27	36	32	26	32	27	22

from (6) that strong optical confinement from the short $\lambda/2$-cavity is advantageous. Analogous to the D-factor, the modulation current efficiency factor (MCEF) describes the increase of the small-signal modulation bandwidth with bias current as

$$f_{3dB} = \mathrm{MCEF}\sqrt{I_b - I_{th}}. \quad (7)$$

B. Measurements and Analysis

The temperature dependent dynamic performance was evaluated by S_{21}-measurements at different heat-sink temperatures using a 67 GHz Agilent E8361A network analyzer. The VCSELs were probed on-chip with a 40 GHz Picoprobe 40A GSG high-frequency probe. The output light was collected by an AR-coated lens package and focused into a short multimode OM4 fiber connected to a 25 GHz New Focus 1481-S-50 photodetector. The measured VCSEL response was corrected for probe insertion loss and frequency response of the detector. S_{21}-measurements with fits of (2) for the 3.5 and 7.5 µm VCSELs can be seen in Fig. 6, and dynamic performance parameters are listed in Table III. The ripples in the S_{21}-measurement for the 3.5 µm oxide aperture VCSEL are attributed to reflections in the measurement setup.

K-factors were extracted from linear fits of (3) as seen in Fig. 6(b) and (e), and were found to be relatively temperature insensitive at 0.11-0.14 ns for the three VCSELs at 25 to 85°C. Small oxide aperture VCSELs have smaller photon lifetimes, but not significantly smaller K-factors. The reason is likely a lower differential gain due to the higher threshold carrier density, as has previously been reported [16]. The intrinsic VCSEL bandwidth can be roughly estimated as $f_{3\mathrm{dB}}^{\mathrm{intrinsic}} \approx 2\pi\sqrt{2}/K$, yielding intrinsic bandwidths exceeding 60 GHz for all VCSELs at all temperatures [25]. This is far above the obtainable small-signal modulation bandwidths, as the VCSEL modulation speed is limited by thermal and parasitic effects. Low damping is, however, crucial to reach high modulation bandwidths since the resonance peak in the intrinsic response helps lifting the total VCSEL small-signal response [16]. However, a too small damping may result in excessive ringing and timing jitter for various bit rates [26]. The VCSEL damping was adjusted for maximum small-signal modulation bandwidth by adjusting the photon lifetime via a shallow surface etch as previously described.

The high optical confinement factor and the high internal quantum efficiencies contribute to large D-factors, with up to 15 GHz/mA^{½} for the 3.5 µm VCSEL, see Fig. 6(c) and (f). Even higher D-factors were obtained for VCSELs with longer photon lifetimes (larger etch depth), with D-factors exceeding 19 GHz/mA^{½} at RT for 3.5 µm VCSELs with an etch depth of 54 nm (close to in-phase top DBR reflection). This larger etch depth also gives reduced threshold current (0.23 mA), but has the drawbacks of lower maximum bandwidth (25 GHz) due to excessive damping, and reduced maximum output power by almost 50% (to ~1.4 mW) due to lower out-coupling of light from the cavity associated with the higher mirror reflectivity (all values at RT). The D-factor is relatively temperature stable, dropping only 10% from 25 to 85°C. By using the extracted η_i, Γ=0.033 from the simulations, V_a equal to the total quantum well thickness ($5 \cdot 4$ nm) times the oxide aperture area, and assuming $\chi = 1$ and $v_g = 8.0 \cdot 10^9$ cm/s, the differential gain $\delta g/\delta n$ can be calculated from (6). The VCSELs have differential gains at RT of 12 to $13 \cdot 10^{16}$ cm^2, decreasing about 10% up to 85°C. Therefore, the reduction in D-factor with temperature can be attributed in equal parts to the reduction in differential gain and internal quantum efficiency. In addition to high D-factors, large MCEFs of almost 20 GHz/mA^{½} was measured for the 3.5 µm VCSEL at RT, indicative of the large modulation bandwidths at low bias currents.

The thermal limit of the maximum modulation bandwidth originates from the thermal saturation of the resonance frequency, as seen in Fig. 6(c) and (f). An estimate of the thermally limited bandwidth can be calculated as $f_{3\mathrm{dB}}^{\mathrm{thermal}} \approx 1.55 \cdot f_r^{\max}$ and are listed in Table III [25]. For the 7.5 µm VCSEL, the thermal bandwidth is 32 GHz at RT, 6 GHz larger than the modulation bandwidth of 26 GHz, indicating that the maximum modulation bandwidth is not significantly limited by thermal effects at room temperature. At higher ambient temperatures, the thermal saturation of the resonance frequency sets in earlier and the thermally limited bandwidth is reduced to just a few GHz above the achievable maximum modulation bandwidths. This implies that thermal effects are a limiting factor for the maximum bandwidth at higher temperatures.

The parasitic pole f_p fitted from (2) was measured as 17 to 21 GHz for all three VCSELs and shows no significant temperature dependence. Even though VCSELs with smaller oxide aperture have smaller capacitance over the oxide layer, the smaller current aperture also translates into a larger resistance, in effect making the parasitic pole relatively independent on oxide aperture diameter [18]. The maximum

bandwidth is mainly limited by parasitics at room temperature. At elevated temperatures, the maximum modulation bandwidth is limited by both parasitics and thermal effects. However, at lower bias currents, parasitics are the main limiting factor even at high temperatures. Hence, to further improve bandwidths at low bias currents, parasitics must be reduced.

V. Conclusion

To summarize, we have demonstrated a new generation of high-speed VCSELs with strong confinement of optical fields and carriers. The use of a short $\lambda/2$ cavity improves the longitudinal confinement factor and the dynamic properties. By positioning oxide layers as close to the QWs as possible, the internal quantum efficiency is improved, facilitating low threshold currents, high wall-plug efficiency, and state-of-the-art dynamics at low bias currents. At room temperature, the maximum bandwidth is mainly limited by parasitics, whereas at 85°C ambient temperature, thermal effects also become important. At low bias currents used for energy-efficient data transmission, thermal effects are less pronounced and the dynamic performance is mainly limited by parasitic effects. Nevertheless, large bandwidths are reached at low bias currents over 25 to 85°C, with a record-high 30 GHz bandwidth achieved at room temperature for certain devices [11].

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