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An Antenna Integrated Low-Noise Receiver for mm-Wave Wideband, High-Datarate Communication

Master's Thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
Chalmers University of Technology
Gothenburg, Sweden 2015

Thesis for the Degree of Master of Science in Wireless, Photonics and Space Engineering

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Abstract

The continued growth in mobile network data traffic, forecast to increase at a compound rate of 54 % annually, has created the need for wireless networks which can handle data rates orders of magnitude greater than is possible with current systems. This growth in data traffic necessitates the use of advanced techniques such as carrier-aggregation and MIMO in order to increase the capacity of wireless networks. In spite of these techniques, current wireless networks are insufficient to handle the predicted future levels of data traffic as their capacity is inherently limited by their narrow bandwidth. This dilemma has led to a surge in interest in the creation of wireless links at carrier frequencies far higher than currently used, where wide swathes of continuous bandwidth are readily available. One such band of frequencies, known as the H-band, lying between 200-325 GHz, has recently been allocated for use in wireless communication links by the Federal Communications Commission in the United States of America. The development of compound semiconductor materials, such as Indium Phosphide (InP), and advances in fabrication and processing techniques over the course of the past decade has enabled the creation of solid-state circuits at such frequencies. To date, many front-end low-noise amplifiers (LNAs) targeting H-band frequencies have reported noise figures of the order of 10 dB, with only moderate values of gain, thereby limiting the potential capacity of receiver systems.
In light of this, this thesis presents the design of a mixer-first receiver for use at H-band frequencies which contains no front-end RF amplifier. Instead, the proposed receiver utilises a single-balanced topology consisting of an input RF quadrature hybrid, a single-balanced transconductance mixer, a pair of IF amplifiers and an active IF balun to perform down-conversion and amplification. An antenna is also integrated on chip to provide the input RF signal. The proposed receiver has IF and RF bandwidths of 42 and 138 GHz respectively and requires only 0 dBm of LO drive power to operate. Careful co-design of the transconductance mixer and IF amplifier ensures wideband IF operation of the receiver. The total conversion gain of the receiver is 23 dB and the simulated noise figure is between 13-15 dB over the entire IF bandwidth. The theoretical capacity of the receiver is somewhat greater than previously reported H-band receiver designs as a result of its wide IF bandwidth. The receiver is implemented using the TSC 250 InP double-heterojunction bipolar transistor (DHBT) process from Teledyne Scientific Corporation and consumes an area of 0.9×1.19 mm^2. The design of each component of the receiver is presented, as well as a discussion of the trade-offs made in the design of the complete receiver, followed by a characterisation of the complete receiver and discussion of its performance.

Keywords: InP DHBT, H-band, Transconductance Mixer, Mixer-First Receiver, Wideband, Integrated Antenna

Notation and Abbreviations

Notation

B Channel Bandwidth.

C Channel Capacity.

F Noise Factor.

G_c Conversion Gain.

$IIP3$ Input Referred 3rd Order Intercept Point.

L_e Emitter Length.

NF Noise Figure.

NF_{min} Minimum Noise Figure.

NF_{sys} System Noise Figure.

$OIP3$ Output Referred 3rd Order Intercept Point.

P_{1dB} 1 dB Gain Compression Point.

SNR Signal-to-Noise Ratio.

T Temperature.

V_{BE} DC Base-Emitter Voltage.

V_{CE} DC Collector-Emitter Voltage.

V_{be} AC Base-Emitter Voltage.

V_{ce} AC Collector-Emitter Voltage.

Δ_{E_G} Bandgap Energy Difference.

β_0 Common-Emitter Forward Current Gain.

τ_b Base Transit Time.

τ_c Collector Transit Time.

τ_e Emitter Transit Time.

f Frequency.

f_T Unity Current-Gain Frequency.

f_{max} Maximum Frequency of Oscillation.

g_m Transconductance.

k Boltzmann's constant.

Abbreviations

BCB Benzocyclobutene.

BJT Bipolar Junction Transistor.

CB Common-Base.

CC Common-Collector.

CE Common-Emitter.

DC Direct Current.

DHBT Double Heterojunction Bipolar Transistor.

FET Field Effect Transistor.

HBT Heterojunction Bipolar Transistor.

HEMT High Electron Mobility Transistor.

IF Intermediate Frequency.

IMN Input Matching Network.

InP Indium Phosphide.

LNA Low Noise Amplifier.

LO Local Oscillator.

MBE Molecular Beam Epitaxy.

MIM Metal Insulator Metal.

MOCVD Metal Oxide Carbon Vapour Deposition.

RF Radio Frequency.

SiGe Silicon Germanium.

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Chapter 1

Introduction

The past decade has seen a dramatic shift in how people use mobile devices and in turn the types of media they transfer to and from such devices. With this change in usage has come an extraordinary growth in the quantity of data transmitted via wireless links. As the capabilities of mobile devices have continued to develop so have the demands placed on the supporting wireless communications systems. In fact, in the year 2014, 30 exabytes of data was transferred through mobile/wireless networks - approximately 30 times the total amount of data transferred via the internet in the year 2000 [1]. Reports indicate that this growth in data shows no signs of slowing, and is expected to continue to grow at a compound growth rate of 54 % as far as 2019, when global mobile data traffic will reach approximately 24.3 exabytes per month [1]. Put simply, in 2019, mobile networks will be expected to handle an equivalent amount of data per month as was transferred over the course of all of 2014. This expected increase in traffic will only be possible if the capacity of wireless communications systems is sufficient.
Theoretically, the upper bound on the capacity of any communication channel is defined by the Shannon-Hartley theorem [2], as given by

$$C = B \log_2(1 + SNR) \tag{1.1}$$

where C is the channel capacity in bits per second (bits/s), B the channel bandwidth (Hz) and SNR the signal-to-noise ratio in the channel. Currently, mobile communications systems operate according to the LTE-advanced standard, which defines 44 seperate bands for use in mobile communications sytems, with a maximum bandwidth of 100 MHz [3]. Modern wireless communications systems take advantage of advanced modulation schemes and novel techniques such as carrier aggregation [4] and multiple-input-multiple-output (MIMO) systems [5] to enhance their data capacity. Ultimately, however, the maximum achievable capacity is limited by the inherently narrow bandwidth of the channel. Due to the logarithmic dependency of C on SNR, the simplest method of increasing the maximum capacity of a communication channel is to increase its bandwidth. Doing so requires both available spectrum and circuits capable of handling the increased bandwidth. The former is tightly limited by various regulatory bodies such as the Federal Communications Commission (FCC) and National Telecommunications and Information Administration (NTIA), which govern spectrum allocation in the United States of America. These regulations allocate portions of the radio spectrum to specific applications, often in fairly narrow bands [6], thereby limiting the potential channel capacity. The latter is restricted by semiconductor technology and transistor size. In recent years, advances in semiconductor design and processing technology have led to a massive reduction in the feature sizes of transistors and enabled the use of complex compound semiconductor materials. These factors have contributed to a continuous increase in the operating speed of electronic circuits and their potential bandwidth. Modern compound semiconductor material such as Silicon Germanium (SiGe) and Indium Phosphide (InP) enable the creation of electronic circuits which

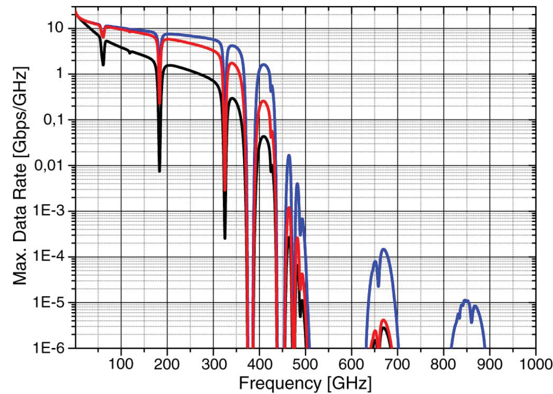


Figure 1.1: Theoretical capacity of a 1 km line of sight wireless link for various atmospheric conditions versus carrier frequency. Blue trace: clear sky conditions; red trace: fog with 50 m visibility; black trace: 50 mm/hr rainfall. Transmit power of 10 dBm and transmit/receive antenna gains of 40 dBi assumed. Adapted from [8].

operate well above 200 GHz [7]. These advances have opened the possibility of transmitting data at previously unachievable frequencies, where large amounts of continuous spectrum are currently available. The latest FCC regulations have allocated frequencies between 200-275 GHz for fixed communication, satellite communication, mobile communication and radio astronomy purposes [6], making use of part of what is known as the *H-band* (220-325 GHz). The bandwidth available at such frequencies is well in excess of that used in current communications systems, which operate at frequencies up to 5 GHz [3]. Clearly, this massive increase in potential channel bandwidth opens the door to realising the high-speed data links required for next generation communication networks.

Recent theoretical studies [8, 9] have demonstrated the promise of wireless communication links at H-band frequencies, despite the issue of increased atmospheric attenuation at such frequencies. In [8], the theoretical capacity of a 1 GHz band (Gbps/GHz) was derived for various weather conditions, as shown in Figure 1.1. In clear sky conditions, the maximum capacity of H-band links is between 6-8 Gbps/GHz, a factor of two less than that of current LTE-advanced frequencies. This value decreases rapidly in adverse weather conditions, particularly at frequencies above 200 GHz. Overcoming the increase in path loss and atmospheric attenuation at high frequencies requires a corresponding increase in transmit/receive antenna gains. However, due to the squared dependency of the gain of an antenna on its operational frequency [10], high-gain antennas are relatively compact at H-band frequencies, making them practically feasible. By means of example, a parabolic reflector antenna with 40 dBi gain and 70 % radiation efficiency requires a diameter of $\sim$ 4.5 cm at 250 GHz, as opposed to $\sim$ 2.2 m at 5 GHz. This fact, coupled with the wide continuous bandwidth available (negating the need for techniques such as carrier-aggregation) at H-band frequencies and above have led to a large surge in interest in this area over the past five years. In [8], it was found that the potential capacity of the band between 300-376 GHz is in excess of 300 Gbps (for antenna gains $\geq$ 60 dBi), even in the case of 50 mm/hr rainfall and with a total transmit power of just 10 dBm spread across the entire band. Clearly, such capacity cannot be achieved at current wireless communication frequencies, where the required bandwidth is simply not available. H-band wireless links are therefore well suited to applications such as wireless backhaul, where the available bandwidth can be used to enable the high-datarates required.

In order to properly utilise the available bandwidth at H-band frequencies, the signal-to-noise

Ref.	f_0 (GHz)	Gain (dB)	NF (dB)	Technology
[12]	210	17	9.4	100 nm mHEMT
[13]	290	16	8.4	30 nm mHEMT
[14]	325	11	8.7	35 nm mHEMT
[15]	295	10	9.7	250 nm DHBT
[15]	240	19	10.8	250 nm DHBT
[16]	200	16	~ 11	250 nm DHBT
[17]	265	24	10.4	250 nm DHBT

Table 1.1: Comparison of reported H-band amplifiers in various technologies and feature sizes.

ratio of the wireless link must be maximised. For any received signal, the SNR is defined as [11]

$$SNR = \frac{P_{rx}}{FkTB} \tag{1.2}$$

where k is the Boltzmann constant, T the physical temperature of the receiver, P_{rx} the received signal power and F the noise factor of the receiver. The noise factor of any component is a measure of the degradation in signal-to-noise ratio of a signal as it passes through the component:

$$F = \frac{SNR_{in}}{SNR_{out}}. \tag{1.3}$$

An ideal noiseless component has a noise factor of 1; that is, the component adds no noise to the signal. Commonly, noise factors are expressed in logarithmic scale, which is then denoted as the noise figure of the component:

$$NF = 10\log_{10}(F). \tag{1.4}$$

Thus, for a given received power level and fixed temperature, the SNR can be maximised by minimizing the noise factor of the receiver. The total noise factor of a cascaded system of components can be calculated via Friis' formula, where F_n and G_n represent the noise factor and transducer gain of the nth component in the cascade, respectively:

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \tag{1.5}$$

In the design of a receiver system, the standard approach is to utilise a Low Noise Amplifier (LNA) with significant gain as the first component in the cascade, such that the noise contributions of any following components is by in large neglected. In this case, assuming $G_1 \gg F_2, F_3$, the noise figure of the cascade is determined by F_1 alone. As will be discussed at later stages in this thesis, the design of low-noise amplifiers at frequencies above 200 GHz is challenging due to the limited gain available from a single transistor and the inherently high noise figure of transistors at such frequencies. A selection of such amplifiers reported in the literature to date is presented in Table 1.1. Of these, only a 5-stage amplifier design had a gain in excess of 20 dB [17], a value high enough to effectively negate the noise contribution of any following receiver stages (provided they are not excessively noisy.) This design required a large chip size ($0.5 \times 1.6\text{mm}^2$), which is undesirable due to cost and physical size concerns. It can be seen that amplifiers implemented in High Electron Mobility Transistor (HEMT) processes reported lower noise figures than those utilizing DHBT technology. Amplifiers implemented in the process used in this thesis [15–17] were all found to have noise figures of the order of 10 dB. Given the values of G and NF contained in Table 1.1, it is interesting to consider alternative receiver designs.

In any down-converting receiver some form of mixing component must be present to perform the necessary frequency conversion. Historically, mixers have had significantly higher noise figures than those achievable by LNAs [18] (an ideal noiseless mixer has a single-sideband noise figure of

3 dB). This fact, coupled with the need to amplify received signals prior to processing/digitizing them, caused the LNA-first receiver topology to become prevalent. If, instead, the mixing component can be designed in such a way that it has a comparable noise figure to that of an LNA while also having decent conversion gain (or sufficiently low conversion loss) to negate the noise contributions of the latter stages of the receiver chain (F_2, F_3, ...) it is possible to achieve comparable receiver performance without the need for an LNA preceding the mixer. At very high frequencies (> 200 GHz), where previously published LNAs have reported relatively high noise figures, this so-called *"mixer-first"* receiver toplogy becomes practically feasible.

As such, this thesis is focused on the implementation of a complete receiver at H-band frequencies using a mixer-first topology with the aim of achieving comparable noise figure to the amplifiers of Table 1.1. The receiver is designed to achieve simultaneously low-noise and wide bandwidth (in so far as is possible) in order to maximise its potential capacity. An antenna is integrated into the receiver to overcome the inherent bandwidth limitations of metallic bondwires [19]. The antenna is a modified dual-slot antenna which utilises shielded microstrip lines to enhance its impedance bandwidth and ensure its radiation patterns are circularly symmetric.

1.1 Thesis contribution

In light of previously completed work on LNA design at the frequencies of interest here (Table 1.1) this thesis investigates the noise performance of a receiver with no low-noise amplifier. Instead, the receiver designed as part of this thesis uses a mixer-first topology, consisting of a single-balanced transconductance mixer, wideband Intermediate Frequency (IF) amplifier and active IF balun, designed to achieve as low noise as possible using the TSC 250 InP DHBT process from Teledyne Scientific Corporation [20]. As amplifiers using this process documented in [15–17] were found to be considerably noisy and require large multiple-stage designs, this thesis seeks to demonstrate that an equivalent, or lower, receiver noise figure can be achieved through the use of a single-balanced mixer-first receiver topology. Such a design would allow the realisation of compact, wide-band, high-datarate communication circuits and could be adopted to create multi-pixel receivers for use in THz imaging.

1.2 Thesis outline

The structure of this thesis is as follows: Chapter 2 outlines the underlying theory behind heterojunction bipolar transistors, frequency conversion and electronic device noise. Chapter 3 delves further into the characteristics of the DHBTs used throughout this thesis and includes simulation results for all major bipolar transistor figures-of-merit. Following this, Chapter 4 documents the design of all receiver components (mixer, IF amplifier, RF hybrid and IF balun). The performance of the proposed receiver is presented in Chapter 5. Finally, the thesis concludes with a discussion of the presented results and an outlook on future work in Chapter 6.

Chapter 2

Theory

In this chapter, the underlying theory behind the performance of modern day heterojunction bipolar transistors is outlined, along with a discussion of frequency conversion and electronic noise. Understanding the operating principle behind the Heterojunction Bipolar Transistor (HBT) provides insight into the performance and design of the proposed receiver. As the receiver is designed for low-noise operation a description of electronic circuit noise is given, followed by an HBT equivalent noise model. Frequency conversion and the operating principle of transconductance mixers are also described in depth to reveal various dependencies and trade-offs that must be considered in the design of the receiver.

2.1 Heterostructures & Heterojunction Bipolar Transistors

A heterostructure is defined as a structure consisting of two or more layers of different semiconductor materials. The junction between any two different materials is known as a heterojunction. At a heterojunction, the composition of the two different semiconductor materials (each with its own bandgap and Fermi level) leads to discontinuities in both the valence and conduction bands. The difference in bandgap between the two materials in a heterojunction is denoted Δ_{E_G}, and is given by

$$\Delta_{E_G} = \Delta_{E_C} + \Delta_{E_V} \tag{2.1}$$

where Δ_{E_C} and Δ_{E_V} are the offsets in conduction and valence band energy levels between the two materials. This difference in energy gap acts as an added degree of freedom in transistor design, one which opens up many new possibilites for optimizing the performance of microwave transistors. Three basic types of heterostructure exist: lattice-matched, pseudomorphic (or strained) and metamorphic heterostructures. A lattice-matched heterostructure utilizes two materials which have the same lattice constant, thus allowing the creation of a high-quality interface between them. Poor lattice-matching creates surface defects, leading to interface traps at the heterojunction [21]. Pseudomorphic structures are composed of materials with different lattice constants but require that the thickness of the grown layer (i.e. the layer on top of the substrate material) be less than a certain critical value (below which the grown layer can be physically strained in order to have the same lattice constant as the substrate) [22]. Metamorphic heterostructures make use of a thick buffer layer between substrate and grown layer to reduce the effect of lattice-mismatching on the on electrical properties of the grown layer. Due to the finite number of suitable semiconductor materials in existance, lattice-matching constraints restrict the possible candidates for heterostructures to only a few well-known combinations. Pseudomorphic and metamorphic heterostructure techniques help to relieve these material constraints and open up a wider range of materials for use in heterostructures.
HBTs are a modified form of the basic Bipolar Junction Transistor (BJT) that has been prevalent in both digital and analogue circuit design for over 50 years. As the name suggests, HBTs

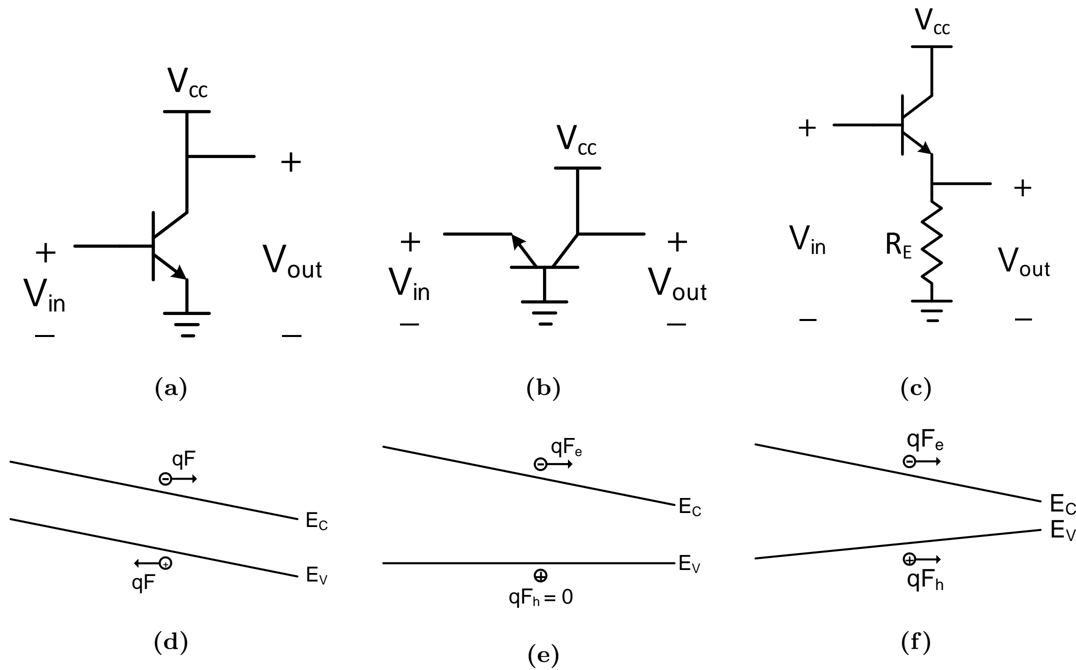


Figure 2.1: (a)-(c) Basic HBT configurations. (a) Common-Emitter (b) Common-Base and (c) Common-Collector. Biasing networks not shown. (d)-(f) Band diagrams for (d) forces in a standard homojunction, (e) quasi-electric fields in a heterojunction, where no force is exerted on holes and (f) quasi-electric fields in heterojunction forcing both electons and holes to move in the same direction.

make use of heterostructure techniques to achieve significant performance improvements over the standard BJT. The basic structure of an HBT is the same as a BJT; that is, it consists of a base, emitter and collector region, each with its own respective terminal. A standard HBT contains a single heterojunction between the base and emitter of the device while a Double Heterojunction Bipolar Transistor (DHBT) utilises heterojunctions between both base-emitter and collector-base regions. Three standard configurations exist, as shown in Figure 2.1a-2.1c: Common-Emitter (CE), Common-Base (CB) and Common-Collector (CC), where the term "common" defines the terminal that is common to both the input and output network of the transistor. The resistor R_E is included in the CC output network to convert the output emitter current to a voltage. Each of these configurations has different characteristics, making them suitable for different applications. All three configurations were used at some point in the design of the proposed receiver. The following discussion refers to a CE transistor unless specified otherwise.

The central idea behind the HBT is this: use of a wide band-gap emitter allows for a significant increase in injection efficiency, in turn leading to greater forward current gain. The forward Direct Current (DC) current gain β_0 of a CE transistor is defined as the ratio of the output DC collector current I_C to the input DC base current I_B:

$$\beta_0 = \frac{I_C}{I_B}. \tag{2.2}$$

The increase in current gain from the use of a wide band-gap emitter is not very useful in and of itself, however. Instead, excess current gain can be traded off to vastly alter other characteristics of the transistor, allowing for improved high-speed performance. In this way, HBTs can achieve significantly better high-frequency performance than standard BJTs. Two common metrics used to benchmark the high-frequency performance of any transistor are its unity current-gain frequency (also known as the cut-off or transit frequency), f_T, and maximum frequency of

oscillation, f_{max}, defined as:

$$|H_{21}(f_T)| = 1; \tag{2.3}$$

$$|U(f_{max})| = 1 \tag{2.4}$$

where H_{21} is the forward current gain β of the transistor and U Mason's unilateral gain [23]. f_T and f_{max} represent the highest frequency at which a transistor can provide useful current and power gain, respectively. HBTs development over the past decade has led to transistors with values of f_{max} approaching 1 THz [24], far beyond anything possible with standard BJTs. Although the idea of incorporating a wide band-gap emitter was originally proposed by William J. Shockley in his 1951 patent entitled "Circuit Element Utilizing Semiconductive Material" [25], much of the credit for the idea goes to Herbert Kroemer, thanks to his 1957 paper "Theory of a Wide-Gap Emitter for Transistors" [26]. Writing in 1982, Kroemer said that the HBT was "an idea whose time has come" [27]. The invention of new manufacturing techniques such as Molecular Beam Epitaxy (MBE) and Metal Oxide Carbon Vapour Deposition (MOCVD) finally enabled the precise control of layer thickness and doping levels required to fabricate HBTs, over 30 years after Kroemer's initial proposal of the underlying theory. Kroemer envisaged that HBTs would enable the development of microwave transistors with f_{max} above 100 GHz, a prediction that seems somewhat conservative in light of the performance of modern day HBTs. A thorough analysis of the operation of HBTs and DHBTs will now be given.

In standard bipolar devices, barring their opposite polarity, the forces acting on the electrons and holes are equivalent (if magnetic forces are ignored). The force acting on both charge carriers is determined by the slope of the energy band in which they lie (see Figure 2.1d), and is given by the electrostatic force qE, where E is the applied electric field. If the energy gap is constant throughout the semiconductor, the force acting on electrons and holes is exactly equal and opposite. Heterostructures allow for the energy gap in a semiconductor to vary with position and hence remove this restriction from the behaviour of holes and electrons. Therefore, in a heterostructure, the slopes of the two band edges need not be the same, as shown in Figure 2.1e. In Figure 2.1f, the slopes of the conduction and valence bands are equivalent in magnitude but opposite in sign, resulting in both charge carriers experiencing a force in the same direction, despite their opposite polarity. Kroemer dubbed the effective forces of such structures "quasi-electric fields", given that purely electrostatic forces in a homojunction device can never produce such effects [28]. Modern heterostructure devices make use of both static electric fields and the quasi-electric fields imposed by energy gap variations to control the distribution and flow of holes and electrons. Heterostructures are particularly suited for use in bipolar devices precisely because they require control over both electrons and holes - heterostructures allow the forces acting on each to be controlled independently. For this reason, heterostructures have found little application in Field Effect Transistors (FETs) and other field-effect devices. By combining semiconductor materials with different band gaps or altering doping levels depending on position (so called graded gap/drift transistors), HBTs allow for significant performance improvements over standard bipolar transistors. Due to the difficulty in fabricating structures with graded doping levels, the first HBTs utilised wideband emitters only, leading to the significant delay between the proposal of the HBT and its widespread adaptation mentioned previously.

Wide band-gap emitter structures help to minimise majority carrier reverse injection between base and emitter by creating a significant potential barrier over which charges must pass. A graphical representation of such a barrier can be found in Figure 2.2a. This potential barrier can be made such that it is greater than the one faced by charges travelling from the emitter into the base (minority carriers). As a result, the reverse-injection current density is reduced by a factor of $\exp(-\Delta E_G/kT)$, where E_G is the difference in band gap energy between the emitter and base

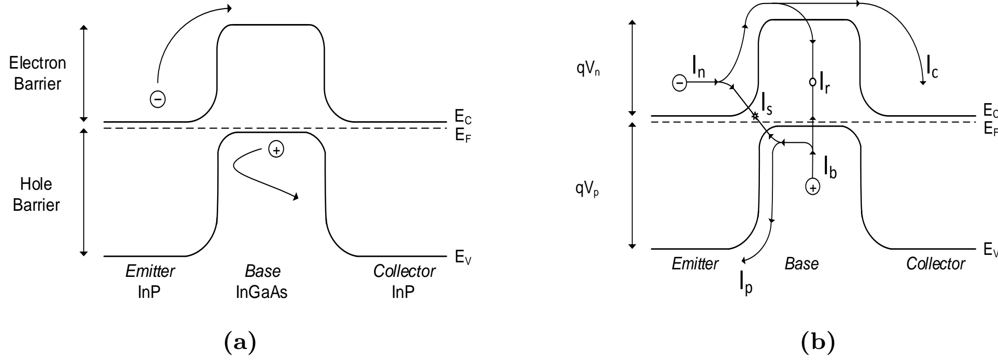


Figure 2.2: Simplified band diagram for an InP/InGaAs DHBT with graded junctions at thermal equilibrium. (a) Behaviour of charge carriers at the base-emitter junction. (b) Current components.

materials. In turn, this reduction leads to a substantial increase in injection efficency and hence forward current gain. Considering Figure 2.2b, the currents flowing in a n-p-n transistor can be broken down into the following terms (neglecting all capacitive currents and any other currents generated by electron-hole pair generation) [27]:

- Electron current I_n injected from the emitter into the base
- Hole current I_p injected from the base into the emitter
- Current I_s due to electon-hole recombination in the forward-biased emitter-base space charge region
- Electron injection current lost to bulk recombination, I_r

Under idealised operation, only the current I_n is desired - we wish to simply inject electrons from the emitter through base and on to the collector with 100% efficiency. Standard application of Kirchoff's Current Law leads to expressions for the three terminal currents and the DC forward current gain, β_0:

$$I_E = I_n + I_p + I_s \tag{2.5}$$

$$I_C = I_n - I_r \tag{2.6}$$

$$I_B = I_p + I_r + I_s \tag{2.7}$$

$$\Longrightarrow \beta_0 = \frac{I_C}{I_B} = \frac{I_n - I_r}{I_p + I_r + I_s} \tag{2.8}$$

In the limit as $I_r,\ I_s \to 0$, the maximum current gain is therefore

$$\beta_{max} = \frac{I_n}{I_p} \tag{2.9}$$

Assuming uniform doping levels of N_e and P_b in the emitter and base, respectively, the electron and hole current densities are given by

$$J_n = N_e v_{n_b} \exp(-qV_n/kT) \tag{2.10}$$

$$J_p = P_b v_{p_e} \exp(-qV_p/kT) \tag{2.11}$$

where v_{n_b} and v_{p_e} are the average velocities of electrons and holes at the emitter-base junction and qV_n, qV_p the potential energy barrier heights between emitter and base for electons/holes, as

depicted in Figure 2.2b. Expressing the ratio of the electron and hole currents leads to

$$\beta_{max} = \frac{I_n}{I_p} = \frac{J_n}{J_p} = \frac{N_e}{P_b}\frac{v_{n_b}}{v_{p_e}} \exp\left(\frac{-qV_n + qV_p}{kT}\right) \tag{2.12}$$

$$q(V_p - V_n) = \Delta E_G \tag{2.13}$$

$$\implies \beta_{max} = \frac{N_e}{P_b}\frac{v_{n_b}}{v_{p_e}} \exp(\Delta E_G/kT) \tag{2.14}$$

The term ΔE_G represents the difference in energy band-gap between the emitter and the base region. Equation 2.14 outlines both the limitations of homojunction devices and the key advantage of heterostructures. In a homojunction device, ΔE_G is zero and hence the maximum current gain is dependent only on the ratios N_e/P_b and v_{n_b}/v_{p_e}, the latter of which is usually fairly restricted [27]. In order to achieve a high level of current gain, a homojunction bipolar transistor must therefore have significantly higher doping concentration in the emitter than the base. Low base doping levels increase the base resistance R_b, leading to higher base transmit time τ_b and reduced operating speed, as will be explained below. This is the primary speed limitation of standard BJTs. On the other hand, if a heterojunction is used, high levels of β_{max} can be achieved by choosing the base and emitter materials such that $\exp(\Delta E_G/kT)$ is large, while simultaneously relieving the constraint on N_e/P_b. Although it appears that arbitrarily high values of β could potentially be achieved through band-gap engineering it should be noted that a useful transistor still requires $I_r << I_n$.

As mentioned previously, the potential of HBTs to achieve vary large values of β is not massively useful in many applications. Instead, it is the freedom to choose the levels of base and emitter doping, while still maintaining acceptable levels of β, that is the greatest advantage of the HBT. This added degree of freedom allows the transistor to be re-optimised and achieve far greater f_T and f_{max} than previously possible. High-frequency operation of a bipolar transistor is, in general, limited by the aggregated delay encountered by the majority charge carriers as they travel from the emitter to the collector. The main sources of delay in a BJT/HBT are the emitter, base and collector transit times, τ_e, τ_b and τ_c, respectively. Of these, the base transit time is the most significant. Parasitic RC delays and capacitance charging times also increase the total transit time from emitter to collector. The total transit time between the emitter and collector of HBT can be expressed as

$$\tau_{ec} = \frac{1}{2\pi f_T} = \tau_b + \tau_c + \frac{kT}{qJ_C A_E}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb} \tag{2.15}$$

where k is Boltzmann's constant, T physical temperature, C_{je} the base-emitter junction capacitance, C_{cb} the total collector-base capacitance and R_{ex}, R_c the parasitic emitter and collector resistance, respectively [7]. Base transit times can be reduced by grading the bandgap of the base region and vertical scaling of the device, while collector transit times are largely determined by the electron saturation velocity in the collector region, making the choice of collector material important [7]. There are several factors that contribute to the increased f_{max} of HBTs, chief of which is the potential reduction of base resistance R_b [29]. Due to the added degree of freedom provided by the wide-gap emitter, the doping level of the base region can be increased significantly (still limited by technological constraints, however), thereby reducing the RC time constant formed by the combined base resistance and collector-base capacitance, C_{cb}. The f_{max} of an HBT can be approximated from its f_T via the equation [29]

$$f_{max} \simeq \sqrt{\frac{f_T}{8\pi R_b C_{cb}}}. \tag{2.16}$$

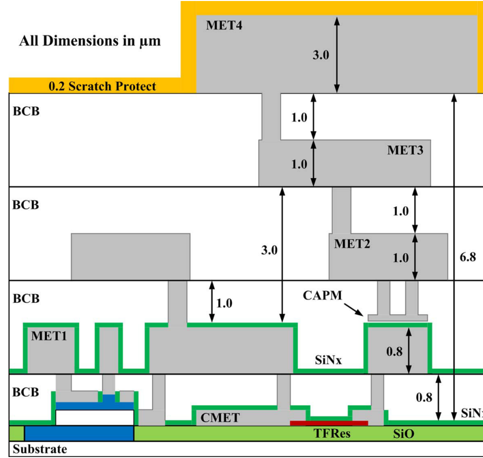


Figure 2.3: Detailed layer stack of the 250 nm DHBT from Teledyne Scientific Corporation.

It is clear that a reduction in R_b will result in a corresponding increase in f_{max}. Reduced R_b also has benefits in terms of the noise generated by the transistor, as will be discussed further in Section 2.3.

The InP DHBT process utilised in this thesis (TSC 250 nm InP DHBT, hereafter referred to as "TSC 250") is provided by Teledyne Scientific Corporation [20] and has been developed over the past decade in collaboration with researchers at the University of California, Santa Barbara [30–32]. Both emitter-base and collector-base junctions are Indium Phosphide/Indium Gallium Arsenide (InP/InGaAs) heterojunctions. Historically, InP has been used for the creation of hetetostructure devices due to its high carrier mobility, high saturation velocity (leading to reduced τ_e, τ_c) and wide band-gap. A wide-band gap collector allows for high-power device operation by increasing the collector-emitter breakdown voltage V_{BCE}, which increases the maximum output signal swing. InGaAs is commonly used in the base region of HBTs as it has very high electron mobility and peak electron velocity [22]. A 30 nm carbon-doped base layer with 50 meV of compositional grading is incorporated to further reduce base transit time, as discussed previously. The collector is 150 nm thick. The base-collector junction doping has been optimised to ensure high current density (> 10 mA/µm^2) operation is possible [33]. The emitter width is fixed to 250 nm while a range of emitter lengths up to 20 µm are available. The size of the transistor should be carefully chosen depending on the intended purpose, as will be described in Chapter 3.
A total of four metallization layers are incorporated in the process. The lower three metal layers (M1, M2 and M3) are 1 µm thick, each separated by 1 µm . Of these, either M1 or M2 must be used as signal ground as back-side vias are not included in the process (the substrate is kept relatively thick (50 µm) to make the wafer more robust, which precludes the use of back-side vias). The upper metal layer (M4) is 3 µm thick and separated from M3 by 1 µm . All interlayer dielectrics are made of Benzocyclobutene (BCB), a material with much lower dielectric constant ($\varepsilon_r = 2.5$) than standard semiconductor materials [34]. With either M1 or M2 as ground, the added thickness and spacing of M4, combined with the low dielectric constant and loss tangent of BCB enables low-loss, high-Q transmission lines to be achieved. An image of the complete layer stack is presented in Fig. 2.3. As described in [32], the DHBTs are fabricated using a combination of MBE, electron-beam lithography, dry/wet etching and photolithography. The process also includes Metal Insulator Metal (MIM) capacitors and thin-film resistors (TFRs), without which it would be impossible to create functional circuits. In comparison to SiGe BJTs, HBTs and Si MOSFETs, DHBTs using InP emitter/collector and InGaAs base regions have achieved notably higher values of f_T and f_{max} [32]. For a 0.25×4 µm^2 device, f_T and f_{max} are

of the order of 475 and 750 GHz, respectively [32]. Further scaling of existing DHBT technology may enable the creation of amplifiers operating in excess of 1 THz. Future HBT devices are performance limited by the need to keep contact resistances at an acceptable level, breakdown voltage requirements and device/IC thermal resistances [24].

A modified version of the Agilent HBT model [35] has been developed to model the behaviour of the fabricated DHBTs and it is this model that is used throughout the design process. All relevant static and small-signal transistor parameters are presented in Chapter 3.

2.2 Transconductance Mixing

The fundamental principle of mixing involves the conversion of a signal from one frequency to a different, desired frequency. Frequency conversion is possible only through the use of either a non-linear or a time-varying system. Linear, time-invariant systems cannot perform frequency conversion. This section is devoted to the theory of operation of transconductance mixers, a type of mixer which takes advantage of time-varying mechanisms in an HBT to perform frequency conversion.

The mixer circuit implemented in this thesis is based on the theory of transconductance mixing - whereby a time varying transconductance is used to perform frequency conversion. The simplest mixer of this type is shown in Figure 2.4a, consisting of a single transistor in CE configuration. Here, the mixer is used to perform downconversion, that is, to convert a Radio Frequency (RF) to a lower-frequency signal by mixing it with a fixed frequency reference signal. The low frequency output signal is referred to as the intermediate-frequency signal and hence will be denoted IF. In a practical mixer, the reference signal is provided by a local oscillator Local Oscillator (LO) and is denoted as such here. For a purely small-signal input the incident RF signal has no effect on the operating point of the mixer. The network shown in Figure 2.4a then acts as a standard CE amplifier cell, performing no frequency conversion. It is the addition of the large LO signal that causes the desired mixing operation. The large-signal LO modulates the base-emitter voltage (V_{be}) of the transistor. To implement the desired mixing effect, the transistor must convert the input RF waveform to create the IF signal at the collector. This action is performed by the transconductance of the transistor, the DC value of which is given by

$$g_m = \frac{I_C}{V_T};\ V_T = \frac{q}{kT} \approxeq 25 \text{ mV for T} = 300\text{K} \tag{2.17}$$

where V_T is the thermal voltage of the device and I_C the DC collector current. The time-varying LO signal at the base of the transistor leads to a time-varying transconductance due to the non-linear I/V characteristic of the HBT, as shown in Figure 2.4b. The time-varying transconductance can be expressed as

$$g_m(t) = dI_c/dV_{be}|_{V_{be}(t)} \tag{2.18}$$

Expanding this waveform into a Fourier series representation gives:

$$g_m(t) = G_0 + 2G_1\cos(\omega_{LO} + \phi_1) + 2G_2\cos(2\omega_{LO} + \phi_2) + 2G_3\cos(4\omega_{LO} + \phi_3) + \ldots \tag{2.19}$$

where $G_n\underline{/\phi_n}$ are the complex Fourier coefficients of the transconductance waveform. The output IF signal is then

$$i_c(t) = g_m(t) \cdot v_{be}(t) \tag{2.20}$$

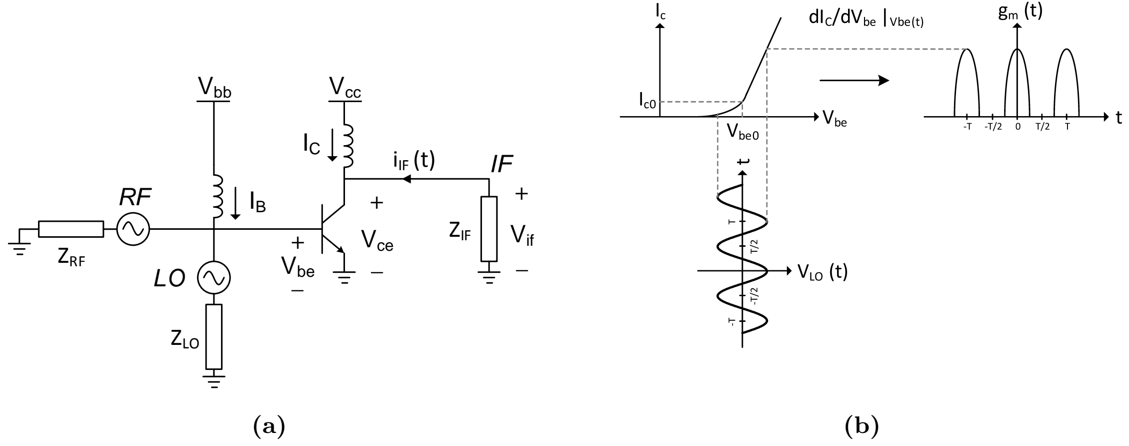


Figure 2.4: (a) Idealized transconductance mixer. Bias networks, DC blocking capacitors and RF/LO combiner network have been omitted for clarity. (b) Illustration of the operating principle of a transconductance mixer.

where $i_c(t)$, $v_{be}(t)$ and $g_m(t)$ are the small-signal, time-varying collector current, base-emitter voltage and transconductance, respectively. This operation produces mixing products at all frequencies which satisfy

$$\omega_n = \omega_{RF} + n\omega_{LO} \ ; \ n = 0, \pm 1, \pm 2, \pm 3, \dots \ . \tag{2.21}$$

In the ideal case, the input LO signal will be a single-frequency tone and thus create mixing products at only two frequencies, $\omega_{RF} \pm \omega_{LO}$. In reality, the LO signal will inevitably contain some harmonics, each of which will create its own pair of IF output signals at the collector. In a down-converting fundamental mixer, the only signal of interest is that at $\omega_{IF} = |\omega_{RF} - \omega_{LO}|$ and unwanted tones should be removed via a low-pass filter at the output of the mixer. The efficiency of the frequency conversion process is defined by the ratio of the output IF power to the input RF power, denoted the conversion gain (G_c):

$$G_c = \left| \frac{P_{IF}}{P_{RF}} \right| \tag{2.22}$$

where P_{IF} is the output signal power at the IF frequency and P_{RF} is the input RF signal power. Assuming a sinusoidal waveform, the IF output power is

$$P_{IF} = \frac{1}{2} |V_{IF} \cdot I_{IF}^*| \tag{2.23}$$

where V_{IF} and I_{IF} are the voltage and current at ω_{IF}. The magnitude of the desired fundamental tone is proportional to the value of G_1, the fundamental LO component of the time-varying transconductance. Maximizing the conversion gain of the transconductance mixer is therefore related to maximizing the fundamental transconductance component G_1, which is dependent on HBT device size, bias point, LO drive power and frequency. Due to the multiple dependencies of both $g_m(t)$ and G_1, a simplified analysis, as outlined by Johansen *et. al* [36], will be used to develop an expression for the conversion gain of an idealized transconductance mixer.

In order to develop an expression for G_c, a linearization of the mixer circuit is made at a single operating point. The simplified equivalent circuit of an ideal transconductance mixer is presented in Figure 2.5. Here it is assumed that only $g_m(t)$ is time-varying. All other element values are assumed to be time-invariant. The emitter-base capacitance C_{be} is represented by its time-averaged value and base and emitter resistances are combined to simplify the analysis. The

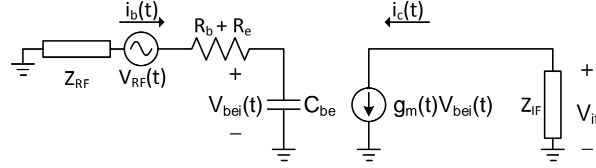


Figure 2.5: Simplified small-signal equivalent circuit of the transconductance mixer of Figure 2.4a, as developed in [36].

total base-emitter capacitance is the sum of the time-varying depletion capacitance $C_d(t)$ and diffusion capacitance $g_m(t)\tau_f$:

$$C_{be}(t) = \left.\frac{dQ_{be}}{dV_{be}}\right|_{V_{bei}(t)} = C_d(t) + g_m(t)\tau_f \tag{2.24}$$

$$\overline{C_{be}} = \frac{2}{T_{LO}}\int_0^{T_{LO}/2} C_{be}(t)dt = C_{d0} + G_0\tau_f \tag{2.25}$$

Equation 2.25 represents the time-averaged value of this capacitance. G_0 represents the DC component of $g_m(t)$. Looking into the circuit from the RF source, the input impedance is

$$Z_{in}(\omega) = R_b + R_e + \frac{1}{j\omega(\overline{C_{be}})} \tag{2.26}$$

If R_b and R_e are bias-invariant, the input impedance of the mixer has a constant real part. As C_d and g_m are both bias and LO drive level dependent, the imaginary part of $Z_{in}(\omega)$ also displays these dependencies. As described in [36], the internal drive voltage V_{bei} cannot be assumed to be sinusoidal in nature due to the voltage drop caused by harmonic currents flowing through parasitic resistances in the HBT and subsequently its Fourier coefficients cannot be described using modified Bessel functions. This precludes the use of the further simplified theoretical approach proposed by Maas in [37] and [18]. Instead, the conversion gain of the HBT mixer is analysed using conversion matrices.

If I_{IF_n} refers to the currents at the mixing frequency ω_n excited by input voltage V_{bei_m} at input frequency ω_m, their relationship can be expressed in terms of the Fourier coefficients of the HBT's transconductance:

$$\begin{bmatrix} I_{IF_{-1}}{}^* \\ I_{IF_0} \\ I_{IF_1} \end{bmatrix} = \begin{bmatrix} G_0 & G_1\angle\phi_1{}^* & G_2\angle\phi_2{}^* \\ G_1\angle\phi_1 & G_0 & G_1\angle\phi_1{}^* \\ G_2\angle\phi_2 & G_1\angle\phi_1 & G_0 \end{bmatrix} \times \begin{bmatrix} V^*_{bei_{-1}} \\ V_{bei_0} \\ V_{bei_1} \end{bmatrix}. \tag{2.27}$$

The desired IF component I_{IF_0} is excited by the input at RF frequency V_{bei_1}. If feedback is neglected (as is the case for the unilateral equivalent circuit of Figure 2.5) and all other mixing products are assumed to be short-circuited by the terminating network, the relation between these two terms is then

$$I_{IF_0} = G_1\angle\phi_1{}^* \cdot V_{bei_1}. \tag{2.28}$$

The internal base-emitter voltage for an ideal sinusoidal input $v_{RF} = V_{RF}\cos(\omega_{rf}t)$ can be determined from Figure 2.5 via voltage division as

$$V_{bei} = \frac{1/j\omega_{RF}\overline{C_{be}}}{Z_{RF} + R_b + R_e + 1/j\omega_{RF}\overline{C_{be}}} \cdot \frac{V_{RF}}{2} = \frac{V_{RF}/2}{1 + j\omega_{RF}(Z_{RF} + R_b + R_e)(C_{d0} + G_0\tau_f)}. \tag{2.29}$$

Therefore, the resulting fundamental current is

$$I_{IF_0} = \frac{G_1\angle\phi_1{}^*(V_{RF}/2)}{1 + j\omega_{RF}(Z_{RF} + R_b + R_e)(C_{d0} + G_0\tau_f)} \tag{2.30}$$

If a conjugate input match is assumed (i.e. $Z_{RF} = Z_{in}^{*}$), the final expression for the conversion gain of a simplified transconductance mixer is then

$$G_c = \frac{{G_1}^2}{{\omega_{RF}}^2 (R_b + R_e)(C_{d0} + G_0 \tau_f)^2} \cdot \mathbb{R}(Z_{IF}) \tag{2.31}$$

where $\mathbb{R}(Z_{IF})$ is the real part of the load impedance at ω_{IF}.
Equation 2.31 reveals numerous dependencies of the conversion gain. Firstly, it is clear that the fundamental LO component of the transconductance should be maximised to achieve good G_c, as stated previously. Given the dependence of g_m on I_C and the constraint that $G_1 \leq |max(g_m(t))|$, it seems that a large device (which can handle high values of I_C without exceeding current density limits) should thus be utilised to achieve high values of G_c. Secondly, the DC component of $g_m(t)$ and parasitic resistances R_b, R_e should be minimised where possible. Due to the squared dependency on ω_{RF}, G_c can be expected to exhibit a 20 dB per decade roll-off. Finally, it appears that arbitrarily high values of G_c can be achieved by using a large load impedance. While this is perhaps theoretically true, in practice Z_{IF} will often be limited due to constraints on stability, impedance matching and bandwidth. Due to the inherently large output impedance of a pumped HBT [18], large Z_{IF} values will create a significant RC network at the collector, which will effectively low-pass-filter the IF output, limiting its bandwidth. Furthermore, very high values of G_c may not necessarily be desirable - higher gain often results in increased intermodulation products, leading to intermodulation distortion and creating spurious responses at the mixer output which are then fed into the next stage of the receiver. These trade-offs will be discussed further in Section 4.1 with reference to the mixer designed as part of this thesis.

2.3 Electronic Noise

Any discussion of noise must first begin by answering the question: what is noise? In general, noise in an electronic circuit can be defined as any unwanted signal, containing no information. Noise has many different sources (some of which are still not completely understood) and causes distinct problems in both transmitters and receivers. Section 2.3.1 will provide an outline of the various types of noise encountered in electronic circuit. A complete analysis of noise in solid state devices can be found in [38]. Following this, an equivalent noise model for modern HBTs will be presented in Section 2.3.2.

2.3.1 Types of Noise

There are four main types of electronic noise: shot noise, thermal noise, phase noise and flicker noise. Of these, the main concerns in the design of the proposed receiver are shot noise and thermal noise. As a result, phase noise and flicker noise are only discussed in brief.

In a transmitter, phase noise is the primary concern. Phase noise arises from the frequency instability of any LO. This instability causes the LO, which should ideally be a single frequency delta function, to have "skirts" in the frequency domain. These skirts can cause neighbouring signal tones to become smeared and prevent proper detection of each tone. In a communications system, where modulated signals are utilised to transmit information, phase noise causes a rotation of the signal constellation. If the phase noise is significant enough to move a symbol from its original decision region to that of a neighbouring symbol this will lead to a symbol error upon demodulation. As frequency conversion is not possible without the use of an LO signal, phase noise is an issue for all upconversion transmitters. Likewise, any receiver that performs downconversion must utilise an LO with low phase noise to avoid symbol detection errors.
The problem of phase noise is often exacerbated by what is known as low-frequency (or flicker,

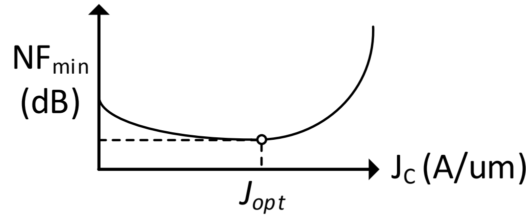


Figure 2.6: Collector current density dependency of the minimum noise figure of a typical bipolar transistor. The optimum collector current is denoted J_{opt}.

1/f) noise, the origins of which are still not completely understood. Many studies of flicker noise have reached the consensus that it is caused by impurities in conductive channels and the generation/recombination of electron-hole pairs within semiconductor devices. Flicker noise causes the skirts of an LO signal to be significantly higher close to the carrier, thereby worsening the issues of phase noise highlighted above. In a mixer, flicker noise causes a separate issue: low-frequency noise around the LO signal can be up/down converted to around the band of interest [18].

Shot noise is generated when current flows across a potential barrier (such as a heterojunction) and is caused by random fluctuations in the flow of charge carriers across the barrier. Shot noise is defined as the stochastic variation in the number of charge carriers crossing a given potential barrier per unit time. The average number remains constant however. The diffusion of charge carriers through a potential barrier follows a Poisson distribution [39]:

$$\sigma_i = \sqrt{2eI\Delta f}; \quad \Longrightarrow \ P_{shot} = 2eI\Delta fR \tag{2.32}$$

Here, Δf is the noise bandwidth. In a 1 Hz bandwidth, shot noise is sometimes referred to as spot noise. The shot noise generated within a device can be modelled as a noise current source, the rms current of which is given by the Schottky equation:

$$I_{sh} = \sqrt{2qI\Delta f} \tag{2.33}$$

where I is the DC current flowing across the potential barrier. Equation 2.33 indicates that the noise performance of any device is dependent on the DC current flowing through it. As a result, it appears that for the best noise performance, a device should be operated at the minimum possible current level which will produce the desired function. This, however, is not strictly true. Figure 2.6 shows the minimum noise figure of a typical HBT versus the DC collector current density flowing through it. Note that a clear minimum occurs at a point away from the vertical axis. At low current levels fewer charge carriers flow in the device and hence any fluctuations play a bigger role in the macroscopic current, thus increasing the amount of noise generated. At high current/energy levels there is a greater chance of random charge carrier fluctuations taking place, again increasing the amount of noise. This leads to the minimum noise factor occurring at some point between these two extremes, at what is termed the optimum noise current, I_{opt} (or optimum noise current density J_{opt}).

Thermal noise occurs due to inherent random vibrations of electrons in a resistive material at a given physical temperature. Thermal excitation of the electrons causes them to vibrate, resulting in a random motion of the electrons. This motion causes a correspondingly random voltage to appear across the device, the rms value of which is given by Planck's black body

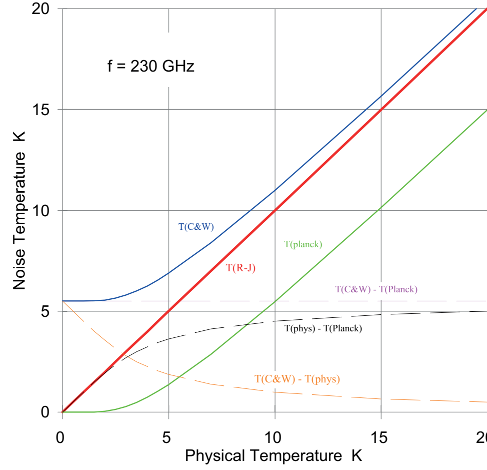


Figure 2.7: Comparative plot of noise temperature vs. device physical temperature for Callen & Welton, Planck and Rayleigh-Jeans definitions [40].

radiation law as

$$V_n = \sqrt{\frac{4hfBR}{\exp(hf/kT) - 1}} \tag{2.34}$$

$$\implies P_n = kTB\left(\frac{hf/kT}{\exp(hf/kT) - 1}\right) \tag{2.35}$$

where h is Planck's constant, f frequency, B the signal bandwidth and R the resistance of the material. From this noise voltage the output noise power P_n can be calculated via Eq. 2.35. The power spectral density of thermal noise is thus

$$S(f) = 8\pi\frac{f^2}{c^3}\left(\frac{hf}{\exp(hf/kT) - 1}\right). \tag{2.36}$$

Equations 2.34-2.36 reveal a clear dependency of the thermal noise generated in a device on both its physical temperature and operational frequency. Two interesting extremes are evident: $f \to \infty$ and $T \to 0\ K$. It appears that if a device can be cooled to absolute zero or operated at infinite frequency, the thermal noise generated in it would disappear entirely. In reality, this is not the case. In the limit as $T \to 0\ K$, thermal noise is limited by what is known as zero-fluctuation noise, first defined by Callen & Welton [41]. Planck's black body law does not account for zero-fluctuation noise and hence requires a simple modification:

$$P_n{}^{CW} = kTB\left(\frac{hf/kT}{\exp(hf/kT) - 1}\right) + \frac{hfB}{2} = \cdots = \frac{hfB}{2} \times \coth\left(\frac{hf}{2kT}\right) \tag{2.37}$$

where the term $^{hfB}/_2$ is the zero-fluctuation noise. It is clear that this definition of noise power can never be zero, regardless of T or f. If $hf/kT << 1$, a simplification can be made to P_n, V_n and $S(f)$:

$$hf/kT << 1 \implies \exp(hf/kT) \approx 1 + hf/kT; \tag{2.38}$$

$$\implies S(f) = 8\pi\frac{f^2}{c^3}kT;\ V_n = \sqrt{4kTBR};\ P_n = kTB \tag{2.39}$$

This formulation of $S(f)$, V_n and P_n is known as the Rayleigh-Jeans approximation. At frequencies in the mm-wave or sub mm-wave band and above, this approximation may not always be valid. However, as can be seen from Fig. 2.7, at temperatures in excess of 15 K, the Rayleigh-Jeans

approximation provides an accurate estimate of the equivalent noise temperature of a device for a frequency of 230 GHz, similar to that of interest here. As this thesis is primarily concerned with the design of room temperature (15° C) electronics, the Rayleigh-Jeans approximation is therefore valid and will be used throughout. Figure 2.7 also highlights the difference between the Callen & Welton and Planck equivalent noise temperatures due to zero-fluctuation noise.

2.3.2 HBT Noise Model

An equivalent small-signal model for modern HBTs was recently proposed by Bardin *et. al* in [42] to describe the noise behaviour of HBTs above the corner frequency of $1/f$ noise (so called broadband noise). The model, shown in Figure 2.8, includes four thermal noise sources:

- $v_{n,Rbx}$; generated by the extrinsic base resistance R_{bx}.
- $v_{n,Rbi}$; generated by the intrinsic base resistance R_{bi}.
- $v_{n,Re}$; generated by the extrinsic emitter resistance R_e.
- $v_{n,Rc}$; generated by the extrinsic collector resistance R_c.

Capacitor C_{cbx} represents the capacitive coupling between the extrinsic base and collector terminals of the HBT, which acts as a feedback capacitance, coupling the base of the HBT to its collector. Shot noise generated by carrier diffusion across the base-emitter and collector-base junctions is accounted for by a pair of current noise sources ($i_{n,b}$ and $i_{n,c}$). The shot noise generated by these sources is partially correlated, having spectral densities

$$\overline{|i_{n,b}|^2} = 2q(I_B + |1 - \exp(-j\omega\tau_n)|^2 \cdot I_C) \tag{2.40}$$

$$\overline{|i_{n,c}|^2} = 2qI_C \tag{2.41}$$

$$\overline{i_{n,b}i_{n,c}^*} = 2qI_C(\exp(j\omega\tau_n) - 1) \tag{2.42}$$

where τ_n is known as the noise delay; typically equivalent to 50% of the transistors base-collector forward transit time τ_f and bias dependent [43]. At low frequencies, where the product $\omega\tau_n$ is small, the expression in Eq. 2.40 equates to the standard definition of shot noise (Eq. 2.33) over a 1 Hz bandwidth. At such frequencies, where $\exp(j\omega\tau_n) \approx 0$, there is no correlation between the noise sources. However, as $f \to \infty$, the minimum noise temperature of the transistor begins to deviate from its low frequency value. As noted in [43], incorporating the effect of correlation between the base and collector shot noise improves the accuracy of the noise model with regards to measured data. Using the equivalent small-signal model of Figure 2.8 an approximate expression for the minimum achievable noise temperature of an HBT was developed in [42]:

$$T_{min} \approx T_a n_c \sqrt{\frac{1}{\beta_0}(1 + 2\zeta) + 2\zeta\left(\frac{f}{f_T}\right)^2} \tag{2.43}$$

$$\zeta = g_m(R_{bx} + R_{bi} + R_e)/n_c \tag{2.44}$$

$$f_c = f_T T_{min,LF}/T_a n_c \sqrt{2\zeta} \tag{2.45}$$

where β_0 is the DC current gain, T_a the ambient temperature and n_c the collector current ideality factor. From this expression it is clear that for current densities where $2\zeta \ll 1$, the low-frequency noise performance of an HBT is limited by its DC current gain β_0. In HBTs designed primarily for high-speed operation, where β_0 is traded with an increase in f_{max} and f_T, the low-frequency noise performance will be poor compared to devices designed specifically for low-noise operation. However, due to the inverse proportionality between T_{min} and f_T, transistors

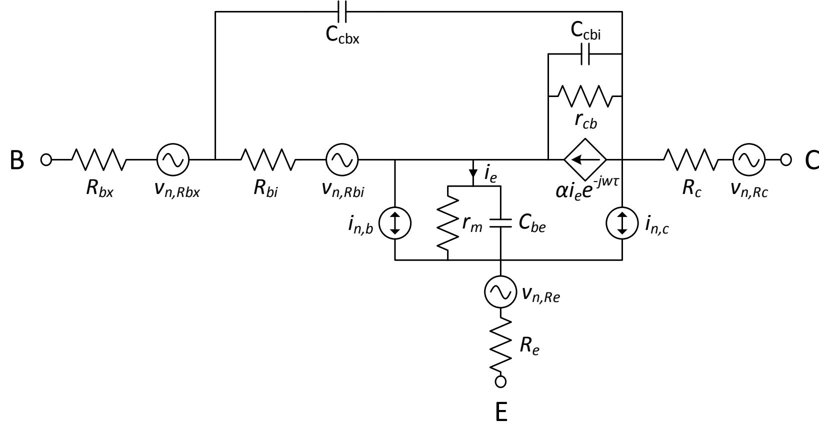


Figure 2.8: Equivalent small-signal HBT noise model, as developed in [42].

designed for high-speed operation offer improved high-frequency noise performance. As current densities (and hence g_m) increase, the value of resistors R_{bx}, R_{bi} and R_e play a significant role in the value of T_{min}. Low frequency noise is scaled by a factor of $(1+2\zeta)$ while high-frequency noise increases as $(f/f_T)^2$. Reducing the noise performance at all frequencies is therefore a matter of minimising the HBT's base and emitter resistances. In a HBT the base-emitter heterojunction provides an extra degree of freedom over a standard BJT, allowing the base to be heavily doped to minimise R_b while maintaining sufficient β_0. Equation 2.45 represents the corner frequency at which the noise temperature of the HBT begins to deviate from its low frequency value $T_{min,LF}$. Again, it is clear that an increase in f_T extends the region for which $T_{min} \simeq T_{min,LF}$.

As discussed in [44], although the small-signal noise models for HBTs are satisfactory, large-signal noise models are still deemed to be lacking in accuracy. As opposed to small-signal operation, HBTs operating under large-signal conditions have time-varying base and collector currents which may contain signals at multiple frequencies. Although this has no effect on the thermal noise sources in the HBT, the time-dependence of i_b and i_c leads to a time dependece in $i_{n,b}$ and $i_{n,c}$. However, given that the time constants involved in the generation of shot noise (random fluctuations of charge carriers across a potential barrier), it can be assumed that any large-signal variation in i_b and i_c occurs much more slowly than the shot noise process and will still appear as white noise. In this case the previous expression for shot noise (Eq. 2.33) is still valid but simply becomes time dependent.

In all simulations performed as part of this thesis noise was simulated using the Agilent HBT model provided by the foundry. This model has been found to be quite accurate in previous work incorporating both small-signal [17] and large-signal simulations [45]. All simulations involving large-signal processes made use of the harmonic balance noise simulator within ADS, which allows the output noise voltage generated by each noise source to be extracted. These values will be used in later sections of this report to examine the noise performance of the receiver.

Chapter 3

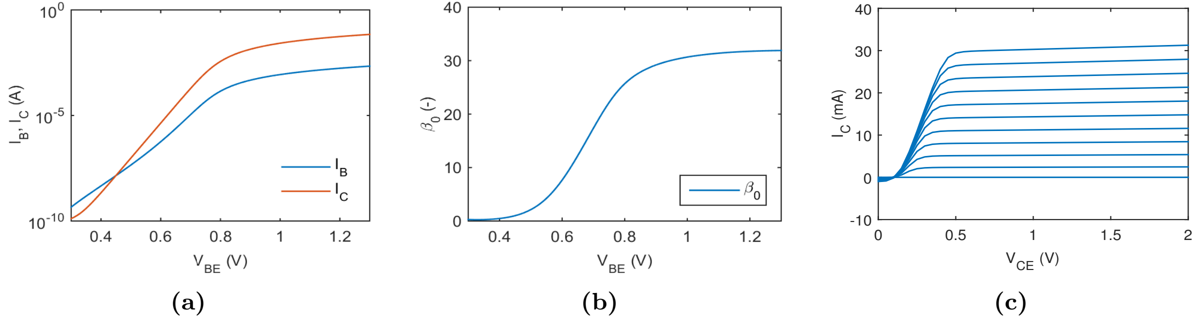
DHBT Characterisation

This chapter details the key static and small-signal parameters of the DHBTs used throughout this thesis, with an emphasis placed on the noise performance of the devices. As will be shown, the noise performance of HBT transistors configured in common-emitter configuration is largely determined by the base resistance of the device, which is in turn related to the emitter length L_e of the device. As such, simulations were performed to determine the dependency of various parameters on L_e. The results of these simulations have a large influence on the design choices made throughout this thesis, as will be outlined in each of the following design sections.

Two of the standard characteristics of any bipolar device that are of great importance in circuit design are its I_C-V_{BE} and $I_C - V_{CE}$ relationships. The former relationship is plotted in Figure 3.1a, a so called Gummel plot, while the latter is plotted in Fig. 3.1c. From Fig. 3.1a, it can be seen that at low values of DC base emitter voltage V_{BE} the DC collector current I_C is less than its input DC base current I_B and as such it provides no forward current gain. This is also evident in Fig. 3.1b, which plots the value of the forward current gain β_0 (I_C/I_B) versus V_{BE}. It can be seen that the device switches on and provides current gain for base-emitter voltages greater than approximately 0.4 V, which is defined as the threshold voltage of the device V_t. For $V_{BE} < V_t$ the operation of the device is dominated by recombination effects and the base current is greater than the collector current. Above this voltage the device switches on rapidly in accordance with the exponential $I_C - V_{BE}$ relationship, leading to a large increase in I_C and hence B_0. However, this increase is not sustained for very high values of V_{BE}, where both I_C and I_B become significantly large. Instead, it is limited by various high-current effects that limit the performance of the transistor and cause I_C and I_B to saturate. The most significant of these effects is the Kirk effect, of which more detail can be found in [29]. Further to the saturation of I_C and I_B, high-current effects also lead to a degradation of the device's f_T, f_{max} and transconductance g_m, as will be outlined below.

Both the mixer and IF amplifier designed as part of this thesis utilise transistors operating in the forward-active region, where the transistor acts as a current-controlled current-source, providing forward current gain. In order for this condition to hold, the transistor's DC collector-emitter voltage V_{CE} must be greater than its knee voltage, the value of V_{CE} which divides the saturation and forward-active regions. For a 0.25×5 µm device, the knee voltage is approximately 0.5 V, as seen in Fig. 3.1c. The relative flatness of the device's $I_C - V_{CE}$ curves above the knee voltage is thanks to a large Early voltage, minimising the output conductance of the transistor. There is little evidence of self-heating issues at high values of V_{CE} and I_C, which would lead to a decrease in I_C with increasing V_{CE} (i.e. a negative output resistance).

For wideband operation, as desired here, it is of upmost importance to bias the device such that its transit frequency f_T is maximised. The f_T of an HBT device with an emitter length



(a) **(b)** **(c)**

Figure 3.1: (a) Gummel plot for a 0.25×5 µm transistor and (b) the corresponding common-emitter DC current gain β_0. $V_{CE} = 1.5$ V. (c) Simulated DC I_C/V_{BE} characteristics of the transistor.

significantly greater than its emitter width is largely determined by the value of the collector current density J_C [29]. This dependency is obvious from examination of Eq. 2.15 and Figure 3.2a, where the $f_T(J_C)$ relationship of a 0.25×5 µm^2 transistor is plotted for various values of V_{CE}. The maximum simulated f_T of such a device is in excess of 400 GHz. At low current densities, where τ_f is approximately constant, the second term in Eq. 2.15 dominates and f_T increases with J_C. At higher J_C, this same term then becomes smaller than the sum of the other two terms, leading to a saturation of f_T. The current density at which peak f_T occurs is denoted J_1. J_1 represents the point at which the concentration of minority carriers entering the collector is equivalent to its doping concentration. For current densities greater than J_1, the large quantity of free carriers act to neutralise the depletion charge at the collector, thereby eliminating the depletion region and increasing the effective width of the base significantly. This increase in base width is also termed "base pushout" and causes an increase in the base transit time τ_b, which then corresponds to a decrease in f_T. The maximum current level J_1 increases with respect to V_{CE} due to a corresponding increase in the DC collector-base voltage V_{CB}, which is directly proportional to J_1 [21]. As reported in [29], for transistors with $L_e >> W_e$, f_T is independent of L_e to a first order approximation. Devices with extremely short emitters have previously been found to have slightly lower peak f_T and somewhat higher values of J_1 [29]. In general, however, J_1 scales with L_e. Therefore, when choosing a suitable transistor size, the total DC collector current required for peak f_T biasing must be considered to ensure that noise figure and power consumption concerns are within suitable levels The transistor's total emitter-collector forward transit time can be determined from its f_T by inverting the data and scaling by a factor of $1/2\pi$. The result of such a procedure is shown in Figure 3.2b, where τ_{EC} is plotted as a function of $1/I_C$. At high current levels, $\tau_E C$ deviates from its otherwise linear characteristic due to the high-current effects discussed previously. The total forward transit time of the simulated DHBT is of the order of 0.5-1.5 ps, depending on both V_{CE} and I_C.

Another key performance metric of any transistor is its maximum available gain (MAG), which represents the maximum possible transducer power gain that can be provided by a single transistor under conjugate matching conditions. The MAG of a transistor can be determined from its S-parameters as

$$\text{MAG} = G_{T_{max}} = \left|\frac{S_{21}}{S_{12}}\right|(K - \sqrt{(K^2 - 1)}) \tag{3.1}$$

where K is the stability factor of the network. If $K < 1$ (i.e. if the transistor cannot be said to be unconditionally stable), the term inside the square root operator is purely imaginary and hence MAG is undefined under such conditions. In this case, the maximum stable gain (MSG) is used instead, defined as the ratio $|S_{21}/S_{12}|$. The MSG and MAG of a variety of transistors is plotted in Fig. 3.2c, for two different values of collector current ($I_C = 0.6$ mA and $I_C = 8$ mA). In this

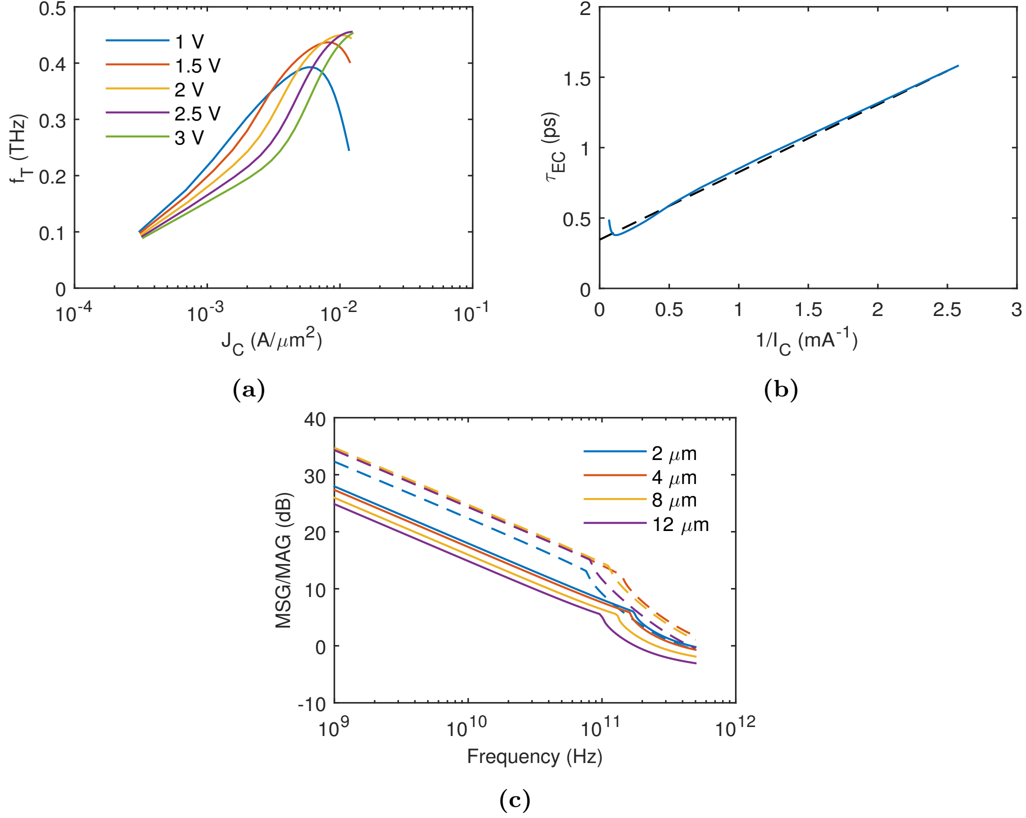


Figure 3.2: (a) Simulated $f_T(J_C)$ of a 0.25×5 µm InP DHBT with different values of DC collector-emitter voltage (V_{CE}). (b) Emitter-collector transit time of the same transistor, extracted from the simulated $f_T(J_C)$ curve of (a); $V_{CE} = 1.5$ V. (c) MSG/MAG of multiple transistors in a common-emitter configuration. Solid traces: $I_C = 0.6$ mA; dashed traces: $I_C = 8$ mA.

figure, the MSG of the transistors is plotted for frequencies where $K < 1$, leading to a linear slope at low frequencies. Thus this plot provides an indication not only of the achievable gain but also the stability of the transistor. To give a better understanding of the relation between the S-parameters of the transistor and its device parameters, the transducer power gain and MAG can be expressed as [21]

$$G_T = \frac{\beta^2 Z_L}{4R_b} \tag{3.2}$$

$$\text{MAG} = \frac{f_T}{8\pi R_b C_c f^2} \tag{3.3}$$

where Z_L is the load impedance presented to the transistor (50 Ω here) and C_c the total collector capacitance. At low current levels the MAG is greater for smaller devices as they are biased closer to peak f_T, as seen in Fig. 3.2c. As I_C increases, the larger transistors offer higher MAG due to their smaller base resistance R_B. The difference in gain between the two current regimes (0.6 mA and 8 mA) can be explained by the difference in β for each I_B.

In order to verify the HBT noise model presented in Section 2.3.2, the minimum noise figure of a selection of DHBTs was evaluated at low and high current levels ($I_C = 0.6$ mA, 8 mA), as shown in Fig. 3.3a. Here, the total collector current flowing in each transistor is set to the same value to ensure the generated collector current shot noise is equivalent. Any differences in the noise figure of the device can then be said to be related to a change in $v_{n,Rbi}$ and/or $i_{n,b}$ only. Under low current operation (the solid traces of Fig. 3.3a) it can be seen that the minimum noise

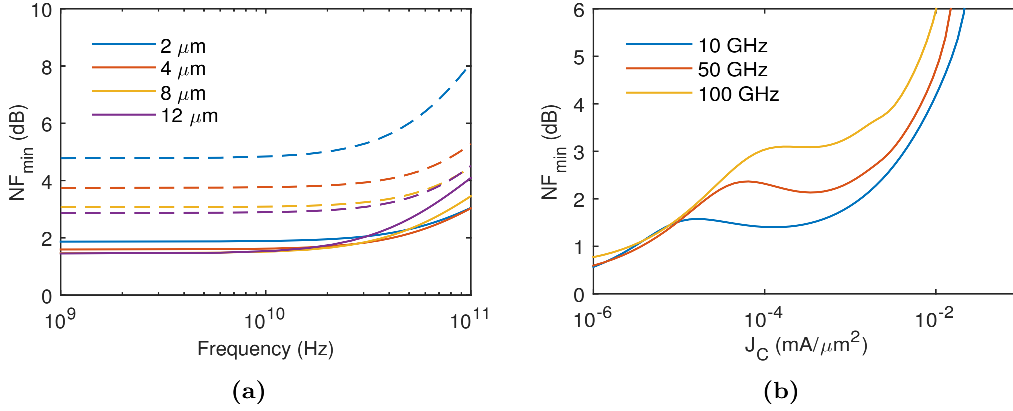


Figure 3.3: (a) Minimum noise figure of multiple DHBTs with varying emitter lengths for two values of collector current. Solid traces: $I_C = 0.6$ mA; dashed traces: $I_C = 8$ mA. (b) Minimum noise figure of a 0.25×5 μm^2 transistor versus collector current density at three different frequencies.

figure of each of the transistors is largely similar at low frequencies. Each transistor exhibits a distinct corner frequency at which its minimum noise temperature (and hence minimum noise figure) begins to deviate from this low frequency value. The value of this corner frequency is inversely proportional to the emitter length of the transistor, due to the reduction in f_T as L_e increases, as predicted by Eq. 2.45. At higher current levels, where the terms in Eq. 2.44 are no longer negligible, the effect of the thermal noise generated in each transistors' base resistance is immediately evident: the noise figure of smaller transistors (i.e. those with larger base resistance) is significantly higher than that of larger transistors. This conclusion greatly influenced the design of the IF amplifier, as is documented in Section 4.2. Again, a clear corner frequency exists but is no longer solely determined by f_T. Figure 3.3b highlights the increase in NF_{min} with f_{RF}, as predicted by Eq. 2.43. From here, it is clear that at higher frequencies, the classic "bathtub" shaped $NF_{min}(J_C)$ of Fig. 2.6 ceases to exist and there is no clear optimum collector current density. Instead, for low noise operation, the transistor should be biased such that its collector current density is minimised. Clearly, this concern must be balanced with that of achieving sufficient gain in the transistor, as explained previously.

Chapter 4

Receiver Design

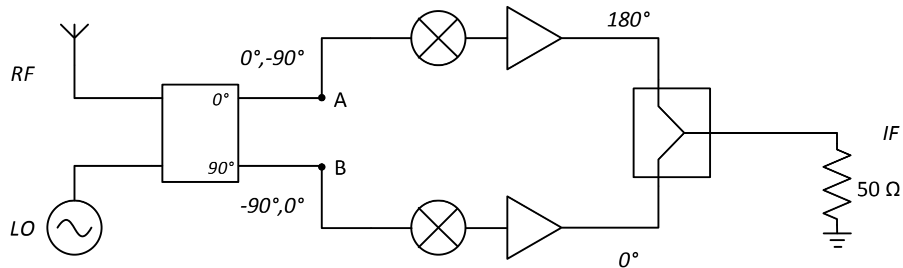


Figure 4.1: Block diagram of the proposed single-balanced receiver. Phase relationships of RF, LO and IF signals are also detailed.

As explained in Section 2.2, transconductance mixers require the input RF and LO signals to be combined prior to injecting them into the base of the mixing transistor. In order to make use of the proposed integrated antenna (see Section 4.5) this must be performed on the receiver chip itself. This requires the realisation of a suitable combining network, the design of which is outlined in Section 4.3. This requirement lends itself to the use of a single-balanced receiver topology. A single-balanced mixer structure consisting of two identical mixers will have an equivalent G_c and NF as that of one of the mixers acting alone, as detailed in [18]. As will be described in Section 4.1, the use of a single-ended receiver topology, consisting of a single mixer and the required combining network, resulted in a 3 dB increase in receiver noise figure and corresponding decrease in G_c. The chosen single-balanced receiver topology is shown in Figure 4.1 and consists of an RF quadrature hybrid, a pair of mixers and IF amplifiers and an active IF balun. In this topology the input RF and LO signals are fed individually to separate ports of the RF hybrid, where each is split equally and fed to both of the output ports. The isolation of the two input ports prevents one input signal from passing directly to the other input port. In this way the RF and LO signals are combined. The balanced operation of the receiver is due to the phase relationships between the RF and LO signals in each branch of the receiver. These are detailed in Figure 4.1. At the node labelled A, the LO signal has undergone a 90° phase shift when passing through the quadrature hybrid while the phase of the RF signal is unchanged. The two are therefore 90° out of phase. The same is true at node B but in this case it is the RF signal that has been shifted by 90° in phase. The IF signals created by the down-converting mixers are then out of phase and require a 180° hybrid or balun to convert them back to a single-ended signal. An active balun is used here for reasons that will be explained in Section 4.4. Two identical IF amplifiers are connected to the mixer to increase the conversion gain of the receiver and neglect the noise contribution of any following receiver stages. The design of this amplifier is discussed in Section 4.2. The mixer and amplifier are carefully co-designed to optimize the noise and bandwidth of

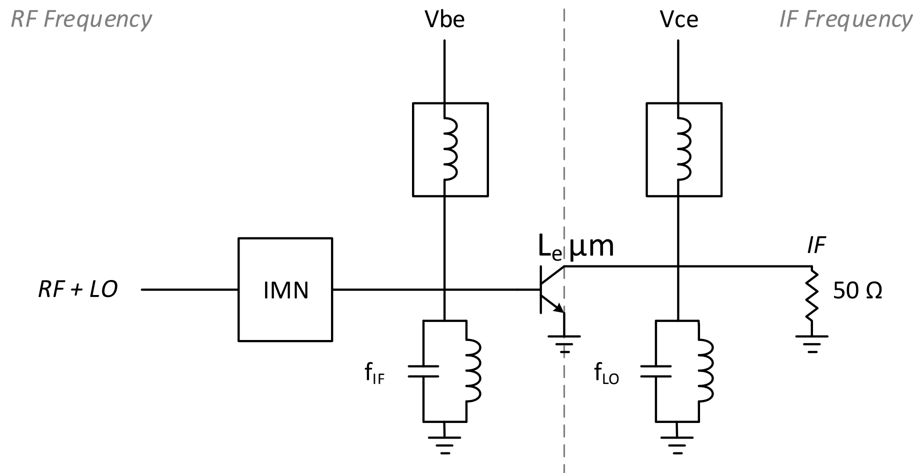


Figure 4.2: Block diagram of idealized transconductance mixer utilised in the design of the single-ended mixer. components are ideal. Harmonic IF and LO terminations are incorporated at the base and collector, respectively. Input RF and LO signals are provided by an ideal two-tone source.

the receiver. The co-design elements of each will be discussed in their relevant sections. Initially, the design of all receiver components is presented individually in order to clearly explain the design strategy and trade-offs involved in each. Thereafter, the co-design of the system components is presented to provide an understanding of the interaction between all stages of the receiver.

The entire receiver design was performed using Keysight Technologies' Advanced Design System (ADS) [46], utilising design kits and models provided by the foundry (Teledyne Scientific Corporation [20]) and developed in-house at the Microwave Electronics Laboratory.

4.1 Mixer Design

The design of the downconversion mixer was undertaken in accordance with the transconductance mixing theory outlined in Section 2.2. The mixer design process involves the determination of optimum transistor size, bias point, matching networks, LO power and terminating impedances. Each of these factors will now be discussed. For the purpose of determining all optimum parameters, the mixer design was first performed using ideal passive components (resistors, capacitors, transmission lines etc.) and then adapted to incorporate real components.

4.1.1 Single-Ended Mixer

When choosing the transistor to be used in the transconductance mixer, numerous factors must be considered:

- Conversion Gain
- RF Bandwidth
- LO Power
- Input Impedance
- Noise Figure
- IF Bandwidth
- DC Power
- Output Impedance

In the TSC 250 process, numerous transistor sizes are available with emitter lengths ranging from 2 µm to 20 µm , each having different characteristics. In essence, the transistor size in an integrated circuit design can effectively be treated as a design variable, allowing the designer to find the optimum transistor size for the intended purpose. In order to compare the performance

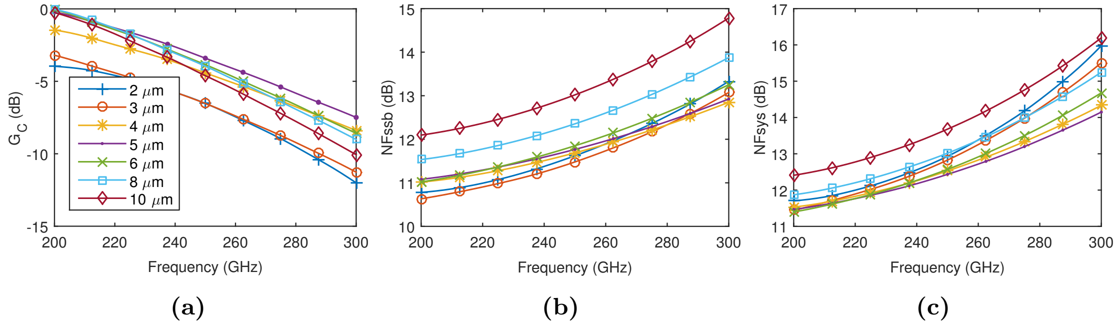


Figure 4.3: (a) Conversion gain, (b) single-sideband mixer noise figure (c) calculated system noise figure versus f_{RF} of an ideal transconductance mixer for various emitter lengths. f_{IF} fixed to 10 GHz.

of the various transistor sizes, an ideal transconductance mixer was designed for a selection of emitter lengths, each matched to a 50 Ω source (the impedance of the RF antenna) by an Input Matching Network (IMN) and connected to a 50 Ω load impedance. The bias point of each was optimized individually and each was driven with its optimum LO power to allow a fair performance comparison. Biasing was performed via ideal DC feeds at the base and collector. Ideal DC blocking capacitors were inserted at the source and load terminals. A schematic of the idealised mixer can be found in Figure 4.2. One point of note is the inclusion of ideal harmonic IF and LO short circuits at the base and collector of the transistor, respectively. These terminations play a key role in the behaviour of the transconductance mixer, as will be explained in detail below. The inclusion of ideal IF and LO terminations allows the optimum performance of the mixer to be determined. The effect of non-ideal IF and LO terminations on the performance of the mixer is then immediately evident. As the parameter of interest is the achievable system noise figure, rather than the individual values of G_c and NF, the amplifier following the mixer was assumed to have a noise figure of 4 dB (corresponding to that of the proposed IF amplifier, c.f. Section 4.2), allowing NF_{sys} for each G_c, NF to be determined. All parameters were optimized to the point of minimum NF_{sys}. All simulations of the single-ended mixer were performed using an ideal two-tone source, to avoid the need for some form of combining network to combine the RF and LO input signals. This allowed the performance of the mixer alone to be examined, independent of any other networks.

Figure 4.3 shows the simulated G_c and NF of each of the mixers between 200-300 GHz, with a fixed IF frequency of 10 GHz. It can be seen that due to the low impedance load, each mixer demonstrates conversion loss across the whole band, increasing with f. Larger transistors offer higher conversion gain due to their larger collector current and therefore greater g_m (a consequence of increased LO drive power, see Figure 4.5) but are also significantly more noisy, due to increased collector and base shot noise contributions. The RF bandwidth of each mixer is approximately equivalent. The noise figure of the mixer can be seen to increase in proportion to the decrease in conversion gain. From a system noise figure perspective, an emitter length between 4-6 µm is optimum. The IF bandwidth of each mixer and its respective noise figure is plotted in Fig. 4.4. As before, each mixer has similar bandwidth, with larger transistors offering higher conversion gains and simultaneously higher noise figures. Again, an emitter length of 4-6 µm offers the best system noise figure performance.

The difference in emitter lengths has a more significant effect on the LO drive power required to achieved minimum NF_{sys}, as can be seen in Figure 4.5. At the frequencies of interest here, LO signals are often generated by multiplying a lower frequency LO source to the desired frequency. As a result, LO power is scarce at H-band frequencies. Figure 4.5c shows that comparable system noise figures can be achieved using transistors with an emitter length between 3 and 6 µm , but with different requirements in terms of LO power. Choosing an emitter length of 5 µm requires

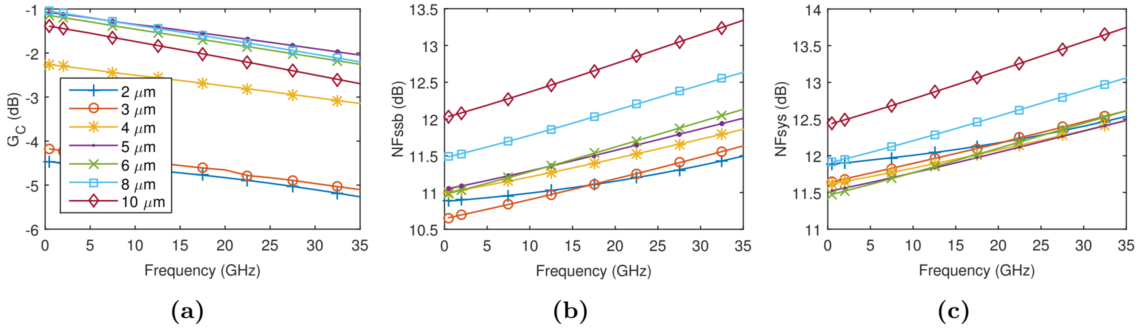


Figure 4.4: (a) Conversion gain, (b) single-sideband mixer noise figure and (c) calculated system noise figure versus f_{IF} of an ideal transconductance mixer for various emitter lengths. f_{LO} fixed to 210 GHz.

an LO drive power of 0 dBm to achieve minimum NF_{sys}, a suitable level for frequency multiplier LO sources. Increasing the transistor size simply heightens the demands on the LO source with no noticeable performance improvement.

The final factor that must be considered when choosing the emitter length of the transistor is the impedance seen looking into the base of the transistor, where both the LO and RF signal are injected. Typically, transconductance mixers driven from the base terminal are matched across the RF band of interest, with little effort made to properly match the LO source [18]. The resulting LO return loss is simply accepted as a design trade-off and the LO power is increased to account for it. However, if the mixer is carefully designed, a suitable impedance match can be achieved across both RF and LO frequencies. Correct choice of the mixing transistor can allow a simple, wideband matching network to be utilised. The large-signal input reflection coefficient (normalized to 50 Ω) of each of the idealized mixers between 150-300 GHz is plotted in Figure 4.6a, extracted from large-signal harmonic balance simulations in ADS. The input impedance is capacitive across a very wide frequency band and that its magnitude decreases with increasing L_e, due to a decrease in the base resistance R_b with L_e.This behaviour corresponds to the transconductance mixing model presented in Section 2.2. In a heterodyne receiver system with an LO frequency reasonably close the RF frequency, the small variation in Γ across such a wide frequency band allows and excellent match to be achieved at both LO and RF frequencies. Due to their proximity to the 1 + jS constant conductance circle, all the transistors can be matched using a simple series transmission line and/or shorted stub. The series transmission line serves to rotate Γ to the 1 + jS constant conductance circle, which is then rotated along 1 +jS towards the centre of the Smith chart by the shorted stub. Transistor base bias can be fed through the shorted stub (which acts as RF ground, decoupling RF from the DC supply). This solution is both compact and broadband and is suitable for use in integrated circuits, where physical space is at a premium. It also neglects the need for any large inductances to provide base bias. In such a matching network, there will inevitably be some losses associated with the transmission line sections (particularly at 200-300 GHz). As there is no gain element preceding the matching network in the proposed receiver, any loss in these sections will trade directly into an increase in system noise figure. Hence the matching network should be kept as compact as possible. From a matching point of view, the larger transistors are closest to the 1 + jS circle and allow for the most compact match, requiring only a shunt stub. The 4 and 5 µm transistors can be matched without incurring too much loss, however.

Following the characterisation of the idealised mixers and the considerations outlined above, an emitter length of 5 µm was chosen, as it provides near optimum performance in terms of bandwidth, system noise figure and input impedance. Once this had been determined the

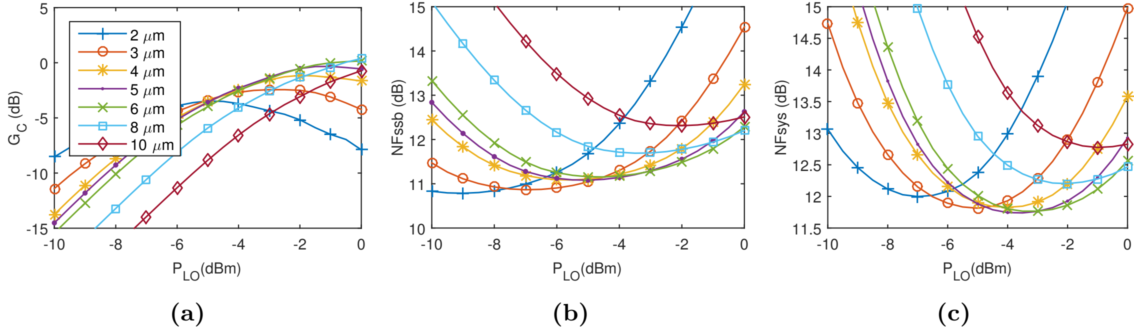


Figure 4.5: (a) Conversion gain, (b) single-sideband mixer noise figure and (c) calculated system noise figure versus P_{LO} of an ideal transconductance mixer for various emitter lengths. f_{RF} = 220 GHz, f_{IF} = 10 GHz.

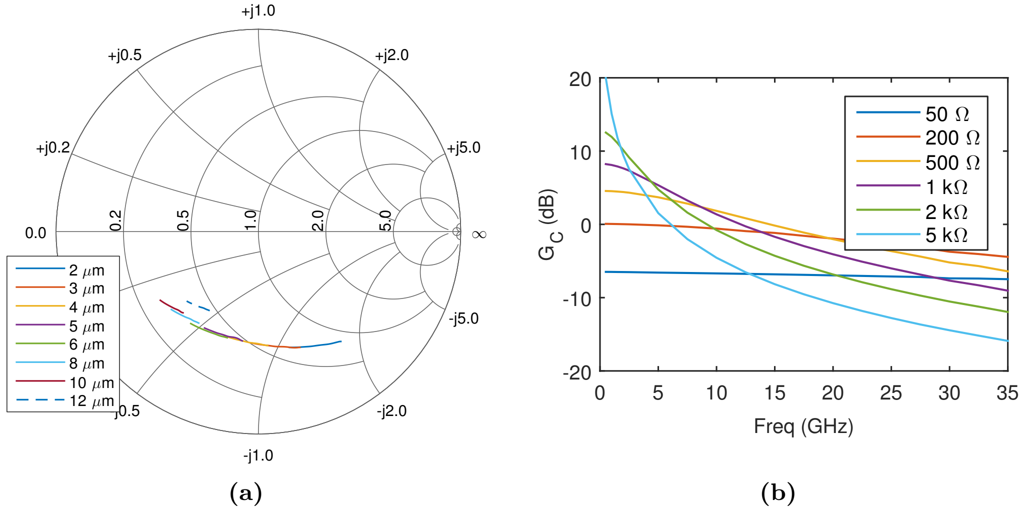


Figure 4.6: (a) Large-signal input RF reflection coefficient (Γ) of an ideal unmatched transconductance mixer for various emitter lengths. f_{RF} = 150-300 GHz. (b) Mixer conversion gain vs. IF frequency for increasing values of load impedance. f_{LO} = 210 GHz.

practical mixer circuit could be realised, with ideal passive components being replaced by real transmission line models. A schematic diagram of the mixer is presented in Figure 4.7. The transmission line elements of the network are implemented on the top layer metal (M4) of the process to minimise losses. This layer offers a thickness of 3 µm , whereas the other metal layers are only 1 µm thick. As a result, the conductor losses in M4 are lower. Generally, it is good practice to connect DC blocking capacitors to any external ports to prevent DC from entering RF sources/supplies. However, at H-band frequencies, large capacitance values result in a significant RC delay and should be avoided in practice. Furthermore, due to the difficulty of accurately modelling the available MIM capacitors (the value of which will impact the input match of the mixer) at very high frequencies, using DC blocks at all may yield poor results in practice. The parasitic inductances of the extra vias required to transition from M4 down to M2 and back up from M1 to M4 again is also difficult to model correctly. These vias will add further loss to the input network of the mixer, thus increasing its noise figure. As a result of these factors, the decision was made to omit DC blocks at the RF ports entirely, thereby seeking to minimise losses and reduce uncertainty in the design. External DC blocks can be used in their stead.

In a transconductance mixer the common-emitter transistor used for frequency conversion can have significant gain at IF frequencies due to the non-zero DC component of its $g_m(t)$. As a consequence, any noise at IF frequencies present at the input of the mixer will actually be

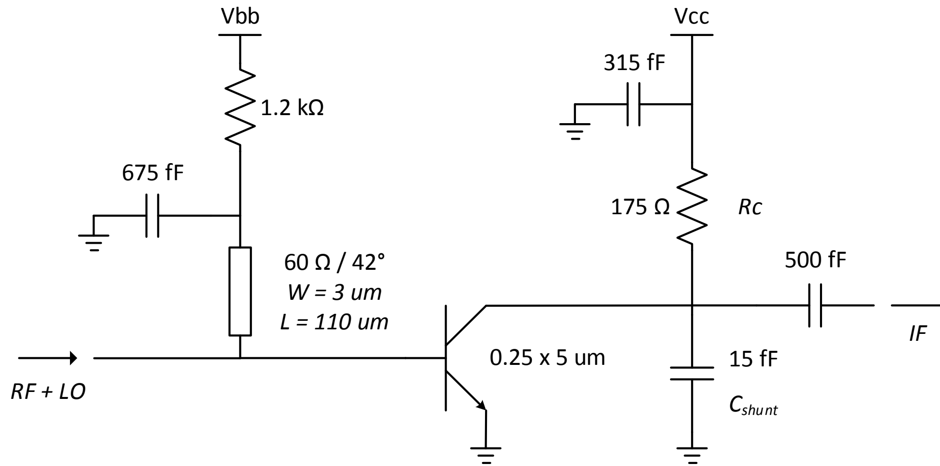


Figure 4.7: Finalised transconductance mixer schematic. The large shunt capacitor at the base serves to short the IF gain of the mixer network.

amplified by the mixer and pass directly to its output [18]. For this reason it is imperative that the IF gain of the network be reduced as much as possible. This is achieved by ensuring that the shunt capacitor of the base bias network is sufficiently large that it acts as an effective short circuit at IF frequencies. For low IF operation this capacitor must therefore be quite large. A value of 0.675 pF was found to give an effective short circuit at the input of the mixer across the IF band of interest. Larger capacitances improve both the noise figure and conversion gain of the mixer, as will be demonstrated in Section 4.1.2, but space constraints limit the maximum practical capacitance value.

As noted in [18], one crucial concern in the operation of a transconductance mixer is the behaviour of its collector-emitter voltage over the period of the input LO signal. Both V_{be} and hence V_{ce} are modulated by the input LO signal (it is this behaviour that causes mixing in the first place.). If the mixer is biased close to the knee region and the LO signal is sufficiently large it may cause the transistor to swing into the linear operating region, where it behaves as a current controlled resistor rather than a current controlled current source. Operating the mixer in this region greatly reduces its performance. Consequently, it is vital that the LO signal does not cause V_{ce} to move towards the knee region at any point over an input cycle. Ideally, a harmonic LO short should be placed at the collector terminal to completely remove the dependency of V_{ce} on the LO signal. In practice, realising an ideal LO short circuit at the collector requires a high-Q resonant circuit, which can be difficult to implement in integrated circuit technologies, where the Q of transmission line sections is often quite low. Instead, a simple shunt capacitor is placed at the collector terminal to provide an LO short, as seen in Fig. 4.7. This approach is well suited to integrated circuit designs due to its compact nature. Another advantage of this approach is that it also shorts higher-order harmonics of the LO signal. The value of this capacitor (C_{shunt}) has a significant effect on the performance of the mixer, as will now be discussed.

Figure 4.8a shows the extrinsic load-line of the mixer for various values of shunt capacitance. It is clear that when no attempt is made to short the LO signal the mixer operates in class A, with a large variation in the V_{ce} over the input LO cycle. A higher power LO signal could drive the mixer into linear operation in this configuration. As the value of C_{shunt} increases, the variation in V_{ce} decreases and the operating class changes from A to AB. The clamping effect of C_{shunt} on V_{ce} causes I_c to change in response to V_{be}, with little change in V_{ce}. This effect is also evident in the collector current waveforms of Figure 4.8b, where it can be seen that the peak-to-peak amplitude of I_c increases with C_{shunt}, leading to a corresponding increase in transconductance. If the fundamental component of the transconductance waveform (G_1) is increased, the addition

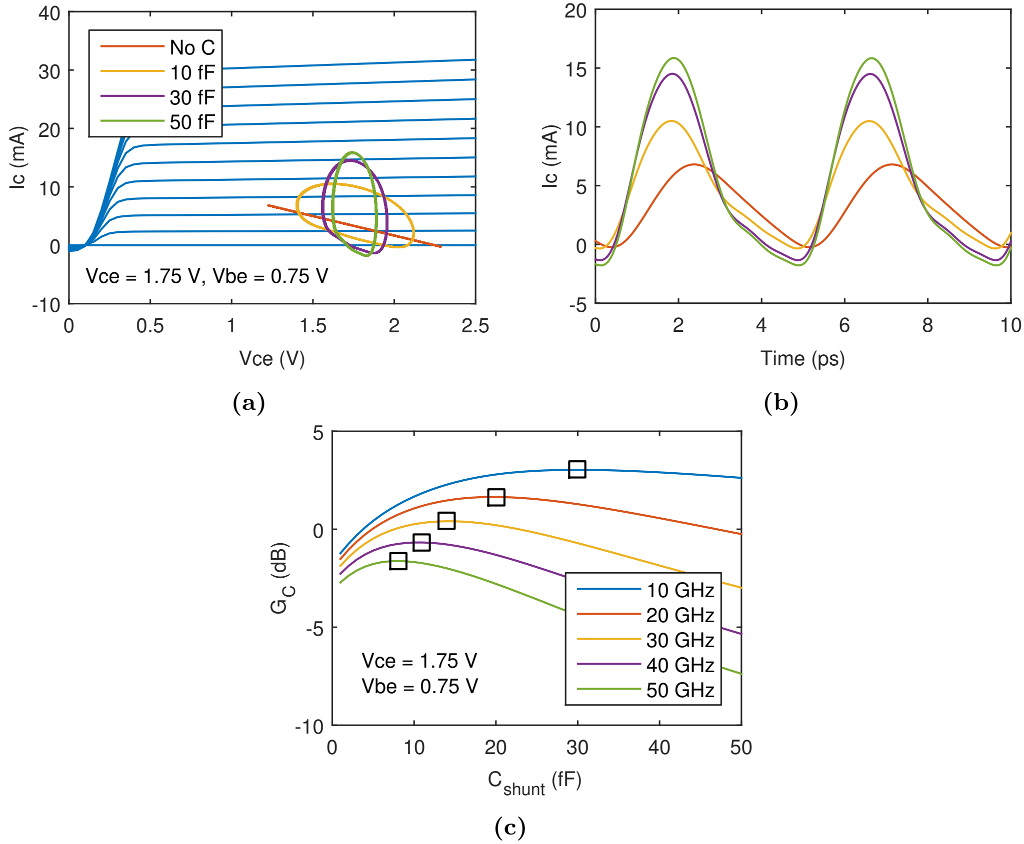


Figure 4.8: (a) Extrinsic load line of the transconductance mixer and (b) time domain collector current waveforms for multiple values of C_{shunt}. The transistor is biased for maximum G_c, as determined in Figure 4.9a. $P_{LO} =$ dBm. (c) Simulated conversion gain of the mixer at multiple IF frequencies for varying C_{shunt}. The transistor is biased for maximum conversion gain with $P_{LO} = 0$ dBm. The optimum capacitance value for each If frequency is indicated by the black markers.

of C_{shunt} leads to an increase in conversion gain, in accordance with Equation 2.31. There are some caveats, however. C_{shunt} cannot be chosen arbitrarily if wideband IF operation is desired as larger values will begin to filter high frequency IF signals, reducing G_c at those frequencies. The value of C_{shunt} also has effect on the interstage match between the mixer and IF amplifier and must be carefully chosen to allow a good match to be achieved. In order to determine a suitable value of C_{shunt} the conversion gain of the mixer was simulated at IF frequencies between 1-50 GHz for varying shunt capacitance values. The results of these simulations are plotted in Fig. 4.8c. The optimum value of C_{shunt} is inversely proportional to f_{IF}, due to the filtering effect of large C_{shunt}. Excessively high values of C_{shunt} (> 20 fF) result in poor performance above 10 GHz. A value of 15 fF was chosen to ensure the operating bandwidth of the mixer was not degraded. This choice of C_{shunt} ensures that the conversion gain at all IF frequencies of interest is greater than if the collector was left un-terminated.

Resistive biasing is used to generate the required base bias current from an external voltage supply. Attempts were made to realise an integrated current source via a standard current mirror architecture but this proved unsuccessful due to the large LO signal power, which was seen to leak back through the current mixer to the reference voltage terminal. A substantial resistance (1.2 kΩ) is used for base biasing to ensure that none of the input LO signal reaches the pins used to connect the external voltage supply. The required collector bias voltage is fed through a 175 Ω resistor connected to the collector of the mixer. This resistor forms part of the load network and matching network used to transform the output impedance of the mixer to a level suitable for driving the IF amplifier. As such, its value must be carefully determined in order to

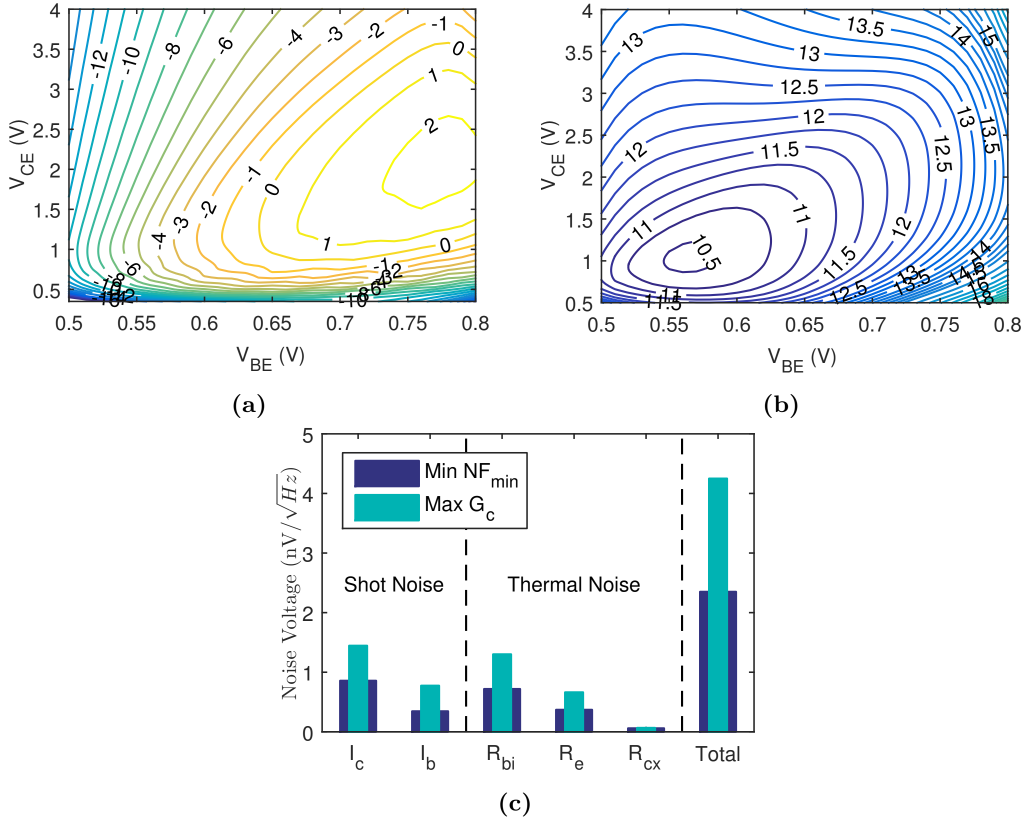


Figure 4.9: (a) Conversion gain (dB) and (b) minimum noise figure (dB) dependency of an idealized transconductance mixer on its base-emitter and collector-emitter bias voltage. (c) Output noise voltage contributions of an idealised transconductance mixer biased in two opposing regimes: for minimum noise figure (Min NF_{min}) and maximum conversion gain (Max G_c). $L_e = 5$ µm , $f_{RF} = 220$ GHz, $f_{IF} = 10$ GHz, $P_{LO} = 0$ dBm, $C_{shunt} = 15$ fF.

maximise the performance of the mixer while allowing for a good impedance match between the stages. The determination of this value and other aspects of the mixer/amplifier co-design will be discussed at a later stage of this section.

When seeking to optimize the conversion gain and noise figure of the mixer it is important to determine the optimum bias conditions for the transistor. Here, as the base bias current will be supplied through the large 1.2 kΩ resistor from an external voltage source, the optimum bias point is defined in terms of the transistor's DC base-emitter (V_{BE}) and collector-emitter (V_{CE}) voltage. Figure 4.9 shows the dependency of the conversion gain and minimum noise figure of the idealized transconductance mixer on V_{BE} and V_{CE}, with the LO signal correctly terminated at the collector as previously discussed. It can be seen that a clear minimum/maximum exists for both NF_{min} and Gc, respectively. However, the two do not occur concurrently. Examining Figure 4.9b, NF_{min} reaches a global minimum when the transistor is biased slightly above threshold and in the active region. Low noise operation occurs for low V_{BE} and V_{CE}, when the shot noise contributions of base and collector current are kept to a minimum. One point of note is the difference in the gradient of the contour plot along its horizontal and vertical axes. For base-emitter voltages above 0.7 V the minimum noise figure of the mixer is seen to increase rapidly (by > 1 dB over a 100 mV change in V_{BE}). An equivalent increase in V_{CE} results in approximately 0.05 dB higher noise figure. It can be concluded that the noise performance of the mixer is significantly more sensitive to the value of V_{BE}. This result is to be expected due to the non-linear I_C-V_{BE} characteristic of transistor, which leads to an exponential increase in I_C

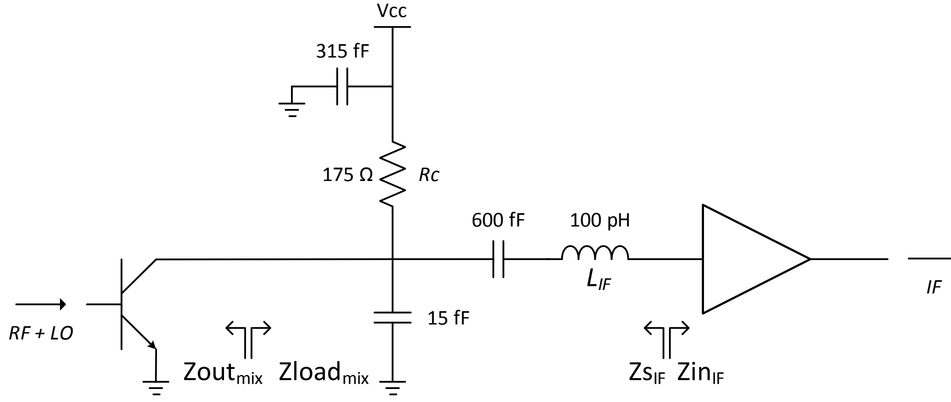


Figure 4.10: Impedance notation for the mixer - IF amplifier interstage matching network.

above the threshold voltage of the device and thus a corresponding increase in collector current shot noise. At voltages below the optimum V_{BE} and V_{CE} the total noise voltage was found to decrease but this was offset by a further reduction in G_c. Analysis of the noise contributions of each component of the mixer, as outlined in Figure 4.9c, confirms that collector current shot noise is the major noise contributor and hence collector current should be kept at a minimum for low noise operation. When biased for minimum noise ($V_{BE} = 0.6$ V, $V_{CE} = 0.85$ V) the total contributions of shot and thermal noise are approximately equivalent. If the mixer is biased for maximum conversion gain (($V_{BE} = 0.75$ V, $V_{CE} = 2$ V)) the noise voltage contributed by each source is seen to approximately double and hence the total noise voltage generated at the output of the mixer is increased by roughly a factor of two, which corresponds to the 3 dB increase in minimum noise figure seen in Figure 4.9b. It should be noted that the thermal noise sources (R_{bi}, R_e and R_{cx}) contribute a similar total noise voltage as shot noise sources (I_c and I_b) in both cases. Increasing the emitter length of the transistor, with a view to reducing its base resistance, was found to result in a higher noise figure overall, due to the increase in I_C caused by higher LO drive powers.

Examination of Figure 4.9a leads to the opposite conclusion. To maximise the conversion gain the mixer should be biased at higher V_{CE} and V_{BE}, away from the knee of the device's I-V curve. It can be seen that the conversion gain of the mixer is largely dependent on the value of V_{CE}. The gradient of the contour is significantly steeper along its vertical axis for $V_{CE} < 2$ V than $V_{CE} > 2$ V, as the peak-to-peak amplitude of the collector current waveform ($I_{c_{p-p}}$) and hence $g_m(t)$ quickly reaches its maximum value. Above 2 V the conversion gain of the mixer can be seen to roll-off gradually. The cause of this was not fully determined but it was found that this reduction in conversion gain corresponded to a reduction in $I_{c_{p-p}}$. This reduction in collector current at higher values of V_{CE} did not occur when the large LO signal was removed. It is unclear whether this characteristic is related to a change in the device's parasitics or its DC I_C/V_{BE} relationship as $V_{CE} \to \infty$.

Given the contours of Figures 4.9a & 4.9b, it can be said that the optimum bias point, in terms of minimum NF_{sys}, lies somewhere on the line between the point of minimum NF_{min} and maximum G_c, depending on the noise figure of the following stage of the receiver. In the ideal case, if the following stages of the receiver were noiseless, the mixer should be biased to achieve NF_{min}. If, instead, the following stages are extremely noisy, the mixer should be biased to provide maximum conversion gain; thereby negating the noise contribution of the latter stages as much as possible. In this sense the mixer can be co-designed with the IF amplifier to achieve minimum NF_{sys}.

As is evident from Figure 4.6b and Equation 2.31, increasing the load impedance of the mixer results in greater conversion gain. The penalty of doing so comes in the reduction of

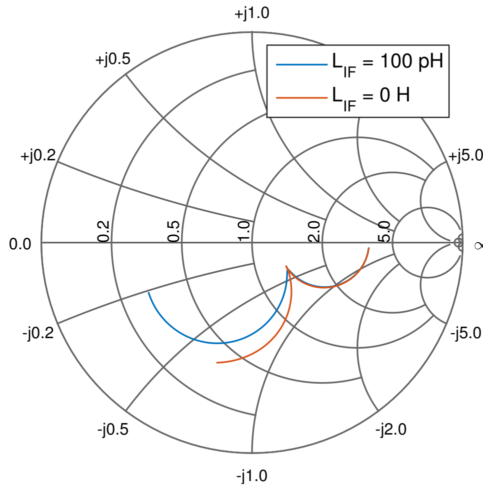


Figure 4.11: Load impedance seen by the mixer circuit ($Zload_{mix}$) with and without inductance L_{IF}, normalized to 50 Ω.

IF bandwidth as $\mathbb{R}(\mathrm{Z_{IF}}) \rightarrow \infty$. Connecting a high value real impedance to the output of the mixer forms a large RC pole at the HBT's collector due to the output capacitance of the HBT and effectively low-pass filters the IF output of the mixer. Consequently, achieve wideband IF operation, the load impedance presented to the mixer must be no higher than approximately 200 Ω. This consideration places an inherent limit on the achievable conversion gain of the mixer. As a result, it is not possible to simultaneously achieve extremely wide IF bandwidth and large conversion gain using a single transconductance mixer.

In order to maximize the performance of the mixer and amplifier each was carefully co-designed following their initial design. The most crucial part of the co-design process is the relation between the output impedance of the mixer and input impedance of the IF amplifier. These impedances must be well matched in order to minimize the return loss between the stages. However, the impedance of each is inherently opposed: the output impedance of the mixer, seen looking into its collector terminal, is quite large (of the order of multiple kΩ) due to the pumped nature of the circuit [37], while the input impedance of the IF amplifier must be kept low to minimize the noise contribution of R_b in the common-emitter input transistor. Furthermore, as previously discussed, both the gain and bandwidth of the mixer stage are directly related to the magnitude of $\mathbb{R}(\mathrm{Z_{IF}})$. In essence, the gain of the mixer is directly opposed to its bandwidth and the noise performance of the IF amplifier. As a result, a trade-off must be made between these factors while also ensuring the return loss between the stages is kept to a minimum.

Achieving a wideband match to the high output impedance of a pumped HBT is quite difficult. If a suitably low noise amplifier with high input impedance were available this combination would result in a very narrow IF mixer bandwidth, as seen in Figure 4.6b. In order to enable wideband operation of the mixer, the approach taken here is to transform the output impedance of the mixer to an impedance similar to that seen looking into the IF amplifier. In this way the return loss between the stages can be minimised while also allowing the mixer bandwidth to remain high. This transformation is performed using the network in Figure 4.10. As $|Zout_{mix}| >> Rc$, the parallel combination of the two shifts the impedance inwards on the Smith chart to Rc on the real axis. C_{shunt} reduces this impedance at high frequencies. The series capacitance and inductance (provided by a length of transmission line) then transform the impedance to its final value. The series capacitor is required to seperate the biasing of the mixer and IF amplifier (series biasing the two was attempted but was found to worsen the performance of the receiver). The value of this capacitor must be sufficiently high that it does not overly attenuate low frequency IF

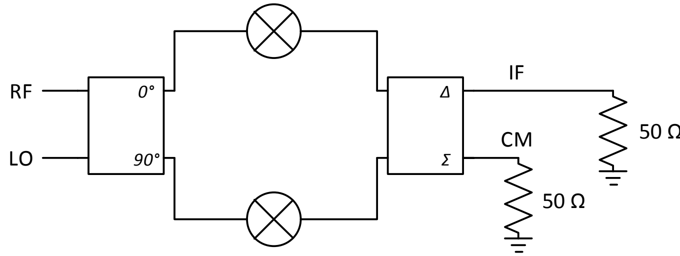


Figure 4.12: Single-balanced testbed used to characterise the performance of the single balanced mixer. Both hybrids are ideal.

signals. The large impedance of this capacitor at low frequencies serves to boost the conversion gain of the mixer. The impedance of this network, in series with the input impedance of the amplifier (Zin_{IF}) acts as the load impedance of the mixer.

The impedance seen looking back into this network, Zs_{IF} forms the source impedance of the IF amplifier. If the input impedance of the IF amplifier is carefully chosen, a good match can be achieved across a very wideband. However, as seen in Figure 4.18a, the input impedance of the IF amplifier in its lowest noise configuration is below 100 Ω at all frequencies. Using the amplifier in this configuration requires the output impedance of the mixer to be shifted to a very low value. As the gain of the mixer is proportional to $Zload_{mix}$ this then results in a large mixer conversion loss, which significantly increases the noise contribution of the IF amplifier. If a smaller transistor is used for Q1 of the IF amplifier the value of R_c can be increased while maintaining low return loss. Unfortunately, as will be described in Section 4.2, this has the affect of increasing the noise figure of the IF amplifier. To optimize the performance of the receiver a compromise between the gain of the mixer and the noise figure of the amplifier must be reached. In the design of the IF amplifier it was found that achieving an input impedance greater than 150 Ω (Zin_{IF}) while maintaining sufficiently low noise operation was not possible. Hence the IF amplifier was designed to have as high input impedance as possible while keeping its noise figure at an acceptable level. This allowed a value of 175 Ω to be used for R_c.

4.1.2 Single-Balanced Mixer

As the proposed receiver is based on a single-balanced topology, a single-balanced mixer was implemented once the optimum parameters of the single-ended mixer had been determined. The performance of the single-balanced mixer was characterised using the testbed shown in Figure 4.12, where both mixers were identical copies of the single-ended mixer circuit from Figure 4.7. In accordance with the theory presented in [18], RF and IF responses of both the single-balanced (SB) and single-ended (SE) mixers were found to be equivalent, as seen in Figures 4.13a and 4.13b. Due to the 3 dB power split in the RF hybrid of the SB topology, the required input LO power of the SB mixer is seen to be 3 dB higher than that of the SE mixer, c.f. Fig. 4.13c. It is expected that, due to this input power split, the linearity of the SB mixer will be 3 dB better than that of the SE mixer. However, this was not found to be the case here. Instead, the input 1 dB gain compression point P_{1dB} of the SB mixer was found to be approximately 10 dB greater, as seen in Figure 4.13d. The reason for this unexpected increase was not fully understood at the time of writing. A similar effect was seen in terms of the Input & Output Referred 3rd Order Intercept Points ($IIP3/OIP3$) of the two mixers, plotted in Fig. 4.13e & 4.13f. Again, the cause of this increase was not fully resolved at the time of writing.
It is important to emphasise that Figure 4.13 compares a single-balanced mixer (simulated with seperate RF and LO sources) to a single-ended mixer without the combination network required

to combine the RF and LO input signals (simulated with an ideal two-tone source). In practice, some form of combining network must be used prior to injecting the RF and LO signals into the base of the transconductance mixer. As previously discussed, the simplest method of combining the RF and LO signals is to use a quadrature hybrid or 3 dB power splitter. In this case, the 3 dB power split at the input would lead to a 3 dB decrease in conversion gain and corresponding increase in noise figure of the single-ended mixer. As such, a single-ended mixer is not suitable for use here as it results in a serious degradation of receiver performance. The single-balanced topology essentially allows the input power lost in the combining network to be "recovered" and therefore has equivalent performance to an ideal single-ended mixer with no combining network.

Following the implementation of the finalized single-balanced mixer, its performance was compared to that of the idealized single-ended mixer of Fig. 4.2. In order to allow a fair comparison, a 175 Ω resistor was connected to the collector of the ideal mixer to ensure an equivalent load impedance was presented to both mixers. The results of this comparison are shown in Figure 4.14. It can be seen that the conversion gain of the final mixer is approximately 2 dB lower than that of the ideal SE mixer, while its noise figure is roughly 0.5 dB higher. Also plotted is the conversion gain of the ideal SE mixer without the harmonic IF base short circuit and LO collector short circuit. From these, it is clear that the degradation in performance between the ideal and final mixer is due to the non-ideal terminations at its base and collector terminals. As previously described, the LO termination of the final mixer, implemented by C_{shunt}, was designed such that the IF bandwidth of the mixer was not degraded. This results in a lower conversion gain than when the LO signal is ideally terminated at the collector, as is evident from Fig. 4.14a. The same is true of the IF termination at the mixer's base terminal, which is limited by the value of the shunt capacitance connected to the input matching stub. As a result, the conversion gain of the mixer is decreased slightly at low IF frequencies, where the base is not ideally shorted. The effect of the improper base termination is especially evident in Figure 4.14b, where it is evident that the noise figure of the mixer increases significantly at low IF frequencies. Overall, it is the inability to properly terminate the mixer at IF/LO frequencies that limits both its conversion gain and noise figure.

An image of the completed single-balanced mixer can be found in Figure 4.15, which includes the RF hybrid design discussed in Section 4.3.

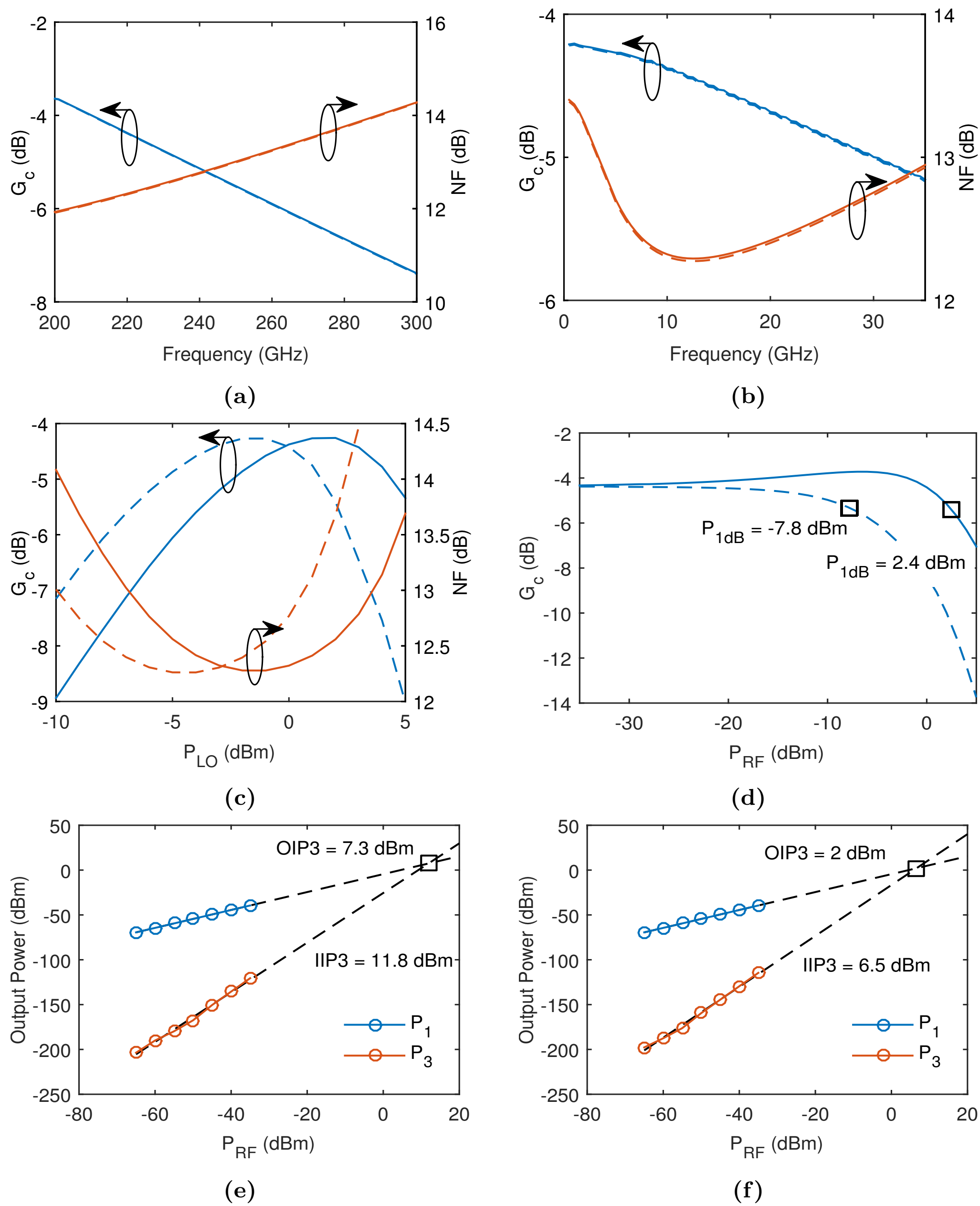


Figure 4.13: (a) - (c) Comparison of the conversion gain and single-sideband noise figure of the proposed mixer in single-ended configuration (with no RF/LO combining network; dashed traces) and single-balanced configuration (solid traces). (a) RF response (b) IF response (c) LO power dependency. (d) $G_c(P_{RF})$ of both mixers; input 1 dB gain compression points indicated by the black markers. (e) and (f) Output power of the fundamental and 3rd order intermodulation tones for the single-balanced and single-ended mixer, respectively. Extrapolated $IIP3/OIP3$ points indicated by the black markers.

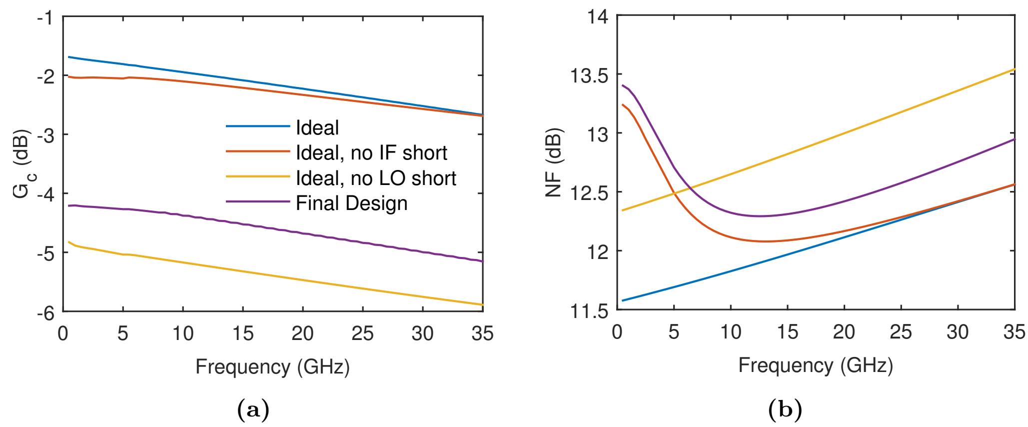


Figure 4.14: Comparison of the final single-balanced mixer to an equivalent circuit with ideal IF and LO terminations, as shown in Fig. 4.2. Simulated performance without IF/LO terminations also shown for emphasis; $f_{LO} = 210$ GHz. (a) Conversion gain. (b) Noise Figure.

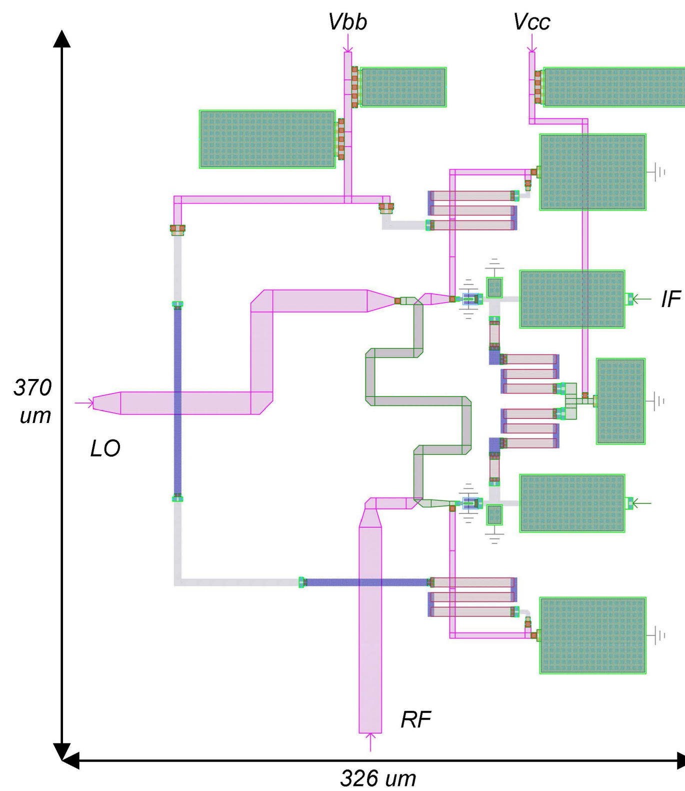


Figure 4.15: Layout view of the completed single balanced mixer, including input RF hybrid (see Section 4.3.) DC/RF pads not shown for clarity.

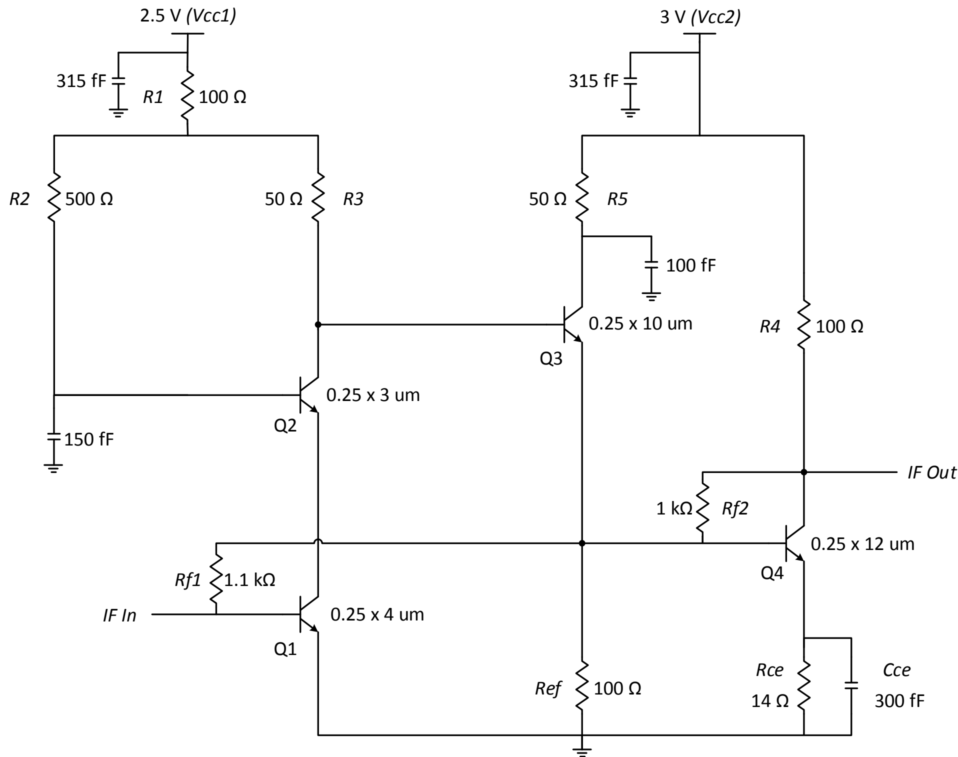


Figure 4.16: Simplified schematic of the cascode based 2-stage low-noise IF amplifier.

4.2 Amplifier design

This section describes the design of the IF amplifier which follows the down-conversion mixer described in the previous section. Two potential amplifier designs were considered:

- A modified Cherry-Hooper differential amplifier
- A cascode based LNA utilising emitter-follower feedback

An initial design (details not included here for the sake of brevity) of the Cherry-Hooper amplifier, with a topology similar to that proposed in [47], found that although it offered excellent bandwidth and gain, its large input impedance resulted in a poor receiver IF bandwidth, for the same reasons as discussed in the design of the mixer load network. As seen in Figure 4.6b, connecting a high impedance load to the transconductance mixer severely limits its IF bandwidth; thereby degrading the IF bandwidth of the complete receiver as a result. A shunt-feedback CE input stage was added to the Cherry-Hooper amplifier in an attempt to decrease its input impedance. This addition had the unwanted effect of inceasing the noise figure of the amplifier to $\sim$ 6.5 dB, far above the minimum noise figure of a single transistor at IF frequencies, as plotted in Figure 3.3a. Due to the low conversion gain of the proposed mixer, the resulting system noise figure was found to be of the order of 16 dB. For this reason, the decision was made to abandon the Cherry-Hooper topology. Instead, a modified version of the wideband, low-noise amplifier developed by Bardin *et. al* in [48] was used. A schematic of the finalised IF amplifier including all element values can be found in Figure 4.16. The theory of operation of this amplifier and the design process behind its implementation will now be described.

The amplifier consists of two stages: an input cascode stage, followed by a common-emitter output buffer stage. Emitter-follower feedback is utilised to connect the output of the cascode stage back to its input, allowing a broadband match to be achieved. A standard common-emitter

amplifier stage generally has limited bandwidth due to the Miller effect. The Miller effect causes the collector-base capacitance C_{cb} of a CE transistor to appear as a much larger capacitance at its base, as given by

$$C_M = R_S(1 - A_V) \cdot C_{cb} \tag{4.1}$$

where A_V is the voltage gain of the CE amplifier (i.e. the gain between its input at the base and output at the collector) and R_S the source resistance at the base terminal. This large capacitance increases the time constant of the input network and effectively low-pass filters the input of the amplifier, thus limiting its bandwidth. In the amplifier designed here, a cascode stage (Q1 & Q2) is used to overcome this inherent bandwidth limitation. A cascode amplifier consists of a CE (Q1) transistor, series connected with a CB (Q2) transistor. The common-base transistor acts as a current buffer, reducing the load on the lower CE transistor. If the transistors are biased such that they have equivalent g_m, the effective voltage gain from the base of the CE transistor to its collector is approximately unity, thereby reducing the Miller effect and increasing the bandwidth of the CE transistor. Assuming $\beta \gg 1$, the transfer function of the CB transistor can be approximated by [49]

$$\frac{i_o}{i_i} \approx \frac{\beta}{\beta + 1} \cdot \frac{1}{1 + j\omega C_{be}/g_m} \tag{4.2}$$

and hence the circuit has a dominant pole at $p = -g_m/C_{be} \approx -\omega_T$, the cut-off frequency of the transistor. Again, if $\beta \gg 1$, the low frequency gain of the cascode amplifier is then

$$\frac{v_o}{v_i} \approx -g_{m_{CE}} R_L. \tag{4.3}$$

The use of a suitably high R_L thereby allows the cascode amplifier to simultaneously achieve decent gain and wide bandwidth. The high output impedance of the CB stage also enables the cascode amplifier to be connected to a large R_L without the need for any impedance matching network. To this end, the output of the cascode amplifier is connected to an emitter-follower stage (Q3). The terminal impedances of the emitter-follower can be expressed as [49]

$$R_{in} = R_b + (\beta + 1)(R_L || r_o) \tag{4.4}$$

$$R_{out} \approx \frac{1}{g_m} + \frac{R_S}{\beta + 1} \tag{4.5}$$

where R_S is the source impedance of Q3 and r_o the output resistance of Q3. Given that r_o is generally significantly larger than R_L, the input and output impedances of the emitter-follower can therefore be determined by the source and load impedances to which it is connected. In general, an emitter-follower transistor has high input impedance and low output impedance. The gain of an ideal emitter-follower can be approximated by

$$\frac{v_{out}}{v_{in}} \approx \frac{g_m R_L}{1 + g_m R_L} \approx 1. \tag{4.6}$$

Hence the emitter-follower provides approximately unity gain but allows for a simple impedance transformation between its terminals. In the amplifier topology implemented here, the emitter-follower serves to provide a high load impedance to the output of the cascode stage (thereby increasing its gain), which is then transformed to a lower impedance, suitable for driving the output CE transistor Q4. Resistive generation is applied to Q4 via R_{ce} and acts as a source of negative-feedback to the transistor (the voltage at the emitter decreases in response to increasing input base voltage due to the drop across R_{ce}), increasing its input and output impedance and decreasing its transconductance [49]. The reduction in g_m leads to a reduced voltage gain, which in turn increases the bandwidth of the CE stage (c.f. Equation 4.1). The degeneration resistor is bypassed by the capacitor C_{ce} to preserve the gain of the CE stage at higher frequencies.

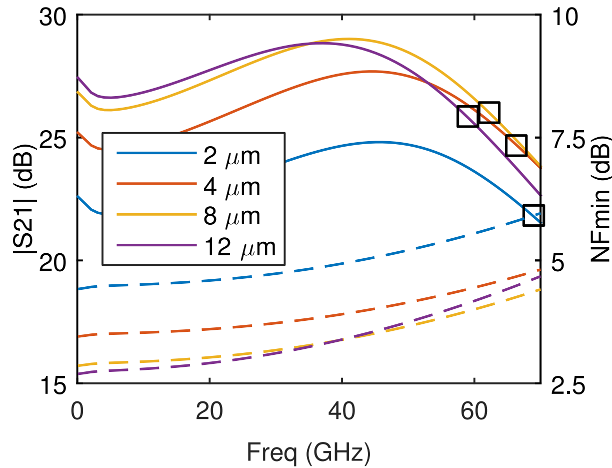


Figure 4.17: Simulated S_{21} of the IF amplifier for varying L_e of Q1. The black squares indicate the 3 dB cut-off frequency of the amplifier for each L_e. All other circuit parameters are equivalent for each L_e.

Resistive shunt feedback is applied to both Q1 and Q4 to allow for wideband matching, a standard technique in the design of wideband amplifiers [50]. This allows wideband matching of Q1 and Q4 to be achieved. In order to reduce the footprint of the amplifier, resistive biasing is utilised throughout to avoid the need for large spiral inductors. The drawback of this approach is that it increases the power consumption of the amplifier. Transistors Q1 and Q2 are biased via resistors R_1, R_2 and R_3 and Q3, Q4 via R_4 and R_5. The value R_5 affects both the gain of the CE output buffer and the amplifier's output match and so is tuned to provide a good trade-off between both. The amplifier is biased by two seperate voltages (2.5 V and 3 V) to optimise the performance of each stage of the amplifier. The cascode amplifier is biased from a 2.5 V supply to minimise the noise figure of the amplifier by reducing the shot noise contribution of Q1 and Q2. Q1 and Q2 are biased with a collector current of 4.5 mA and V_{CE} of 1.2 and 0.72 V, respectively. The CC stage and output CE buffer are biased from a 3 V supply. The increased supply voltage of these stages increases the gain of the amplifier and also increases the maximum voltage swing at the output of the amplifier, which improves the linearity of the amplifier, as will be discussed at the end of this section. Q3 is biased at $V_{CE} = 1.45$ V, $I_C = 10$ mA, while Q4 has a collector current of 14 mA and 1.2 V V_{CE}. All bias points were optimised to provide a trade-off between gain and noise figure.

A 150 fF capacitor is placed at the base of Q2 to provide an RF short. Two 265 fF capacitors are connected to the bias lines for RF decoupling. The IF amplifier is AC-coupled to the preceding and following stages of the receiver through a pair of 500 fF capacitors to ensure the operating point of the amplifier is not affected by the biasing of the other stages. At the IF frequencies of interest here (0-50 GHz), small series capacitances attenuate the desired signal and hence these DC blocking capacitors must be reasonably high in value, increasing their physical size significantly.

As with the mixer described previously, the length of the emitter of each transistor in the amplifier can be treated as a design variable and optimized in order to achieve the desired performance. In the amplifier designed here, the strongest dependencies are on the emitter lengths of transistors $Q1$ and $Q4$, the input and output CE transistors. Q1 largely determines the input impedance of the amplifier, its 3 dB bandwidth and its total noise figure (Q1 has sufficient gain to negate the noise contribution of the other stages of the amplifier). Q4 effects the amplifiers' bandwidth and low frequency gain. In both cases, the size of the transistor was carefully optimized to maximize bandwidth while simultaneously keeping the noise figure as low as possible. The results of this optimisation process are shown in Figure 4.17. As expected,

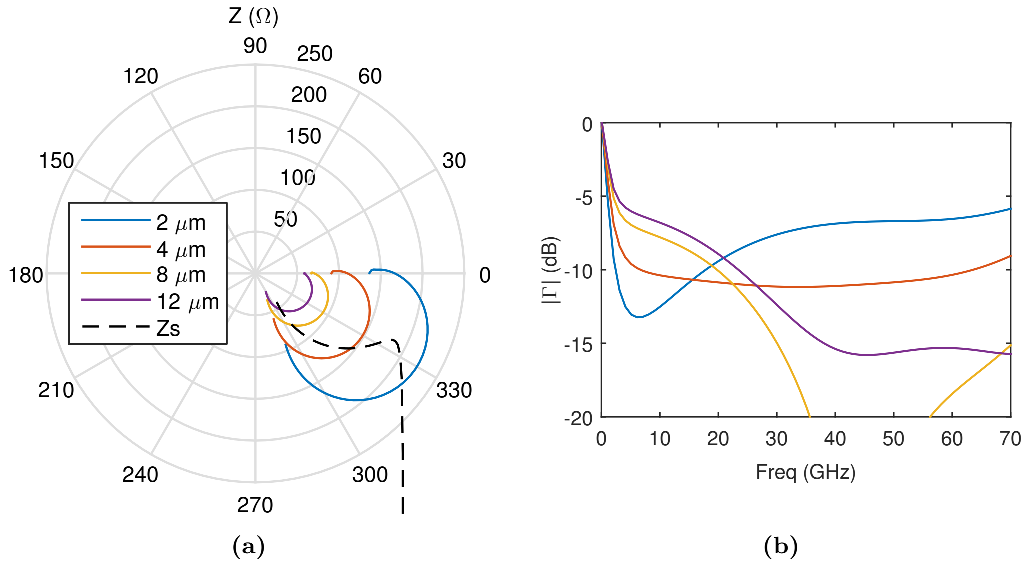


Figure 4.18: (a) Small-signal input impedance of the amplifier between 1 - 70 GHz for varying L_e of Q1. The source impedance seen by the amplifier (Zs) is represented by the dashed black trace. (b) Simulated impedance match between the mixer and IF amplifier.

the bandwidth of the amplifier is at its highest for small values of L_e - given the bias point of Q1 ($V_{CE} = 1.2$ V, $I_C = 5$ mA), these transistors are biased closer to peak f_T, see Fig. 3.2a. However, it can be seen that an emitter length of up to 8 µm increases the low-frequency gain of the amplifier without significantly decreasing its bandwidth, due to a reduction in R_b. An emitter length of 8 µm is also the optimum in terms of the noise performance of the amplifier. Shorter emitter lengths have a higher minimum noise figure across all frequencies due to their larger base resistance. This behaviour corresponds to the equivalent noise model outlined in Section 2.3.2. As seen in Fig. 3.3a, at collector current levels where the terms in Eq. 2.44 are non-negligible, larger transistors are seen to have significantly lower NF_{min}. Increasing the size of the emitter reduces R_b, thereby decreasing the noise figure of the amplifier. As discussed in Section 4.1, another factor that must be considered in the design of the IF amplifier is its input impedance. The IF amplifier and interstage matching network forms the load network of the mixer and hence the value of its input impedance effects both the conversion gain and bandwidth of the mixer. The input impedance of the amplifier must also be of a suitable value to keep the return loss between the stages at an acceptable level. Hence the small-signal input impedance of the amplifier was also considered when designing the IF amplifier. Figure 4.18a shows the dependency of Z_{in} on the emitter length of Q1. The simulated return loss between the stages is plotted in Fig. 4.18b, where the source impedance is Zs_{IF}, seen looking back into the impedance matching network of Figure 4.10. It is clear that a 4 µm emitter provides the best performance in terms of return loss. As previously stated, there is an inherent opposition in the choice of Q1 between the gain and noise figure of the IF amplifier, the IF bandwidth of the receiver and the return loss between the stages. Careful co-design of the mixer, the interstage matching network and the IF amplifier itself allows a compromise between each of these concerns to be reached.

Considering the factors described above, an emitter length of 4 µm was chosen for Q1, to provide wide IF bandwidth, reasonable noise figure and suitable Z_{in}. Transistors Q2 and Q3 were optimised in a similar manner but overall have a less significant effect on the performance of the amplifier. As the overall gain of a cascode amplifier is approximately equivalent to that of the CE transistor acting alone, the emitter length of Q2 was set to 3 µm in order to maximise the bandwidth of the cascode amplifier. A value of 6 µm was chosen for Q3 to increase the low frequency gain without limiting the bandwidth of the emitter follower. The emitter length of Q4

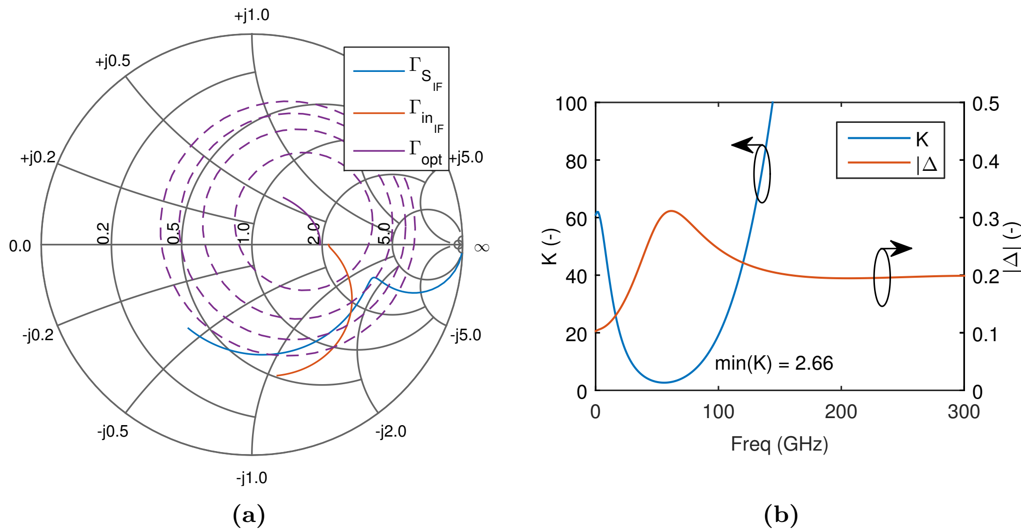


Figure 4.19: (a) Source, input and optimum source reflection coefficient of the IF amplifier, normalized to 50 Ω. Dashed traces indicate constant noise figure circles, plotted in 0.25 dB steps. (b) Stability factor and $|\Delta|$ of the IF amplifier for frequencies up to 1 THz.

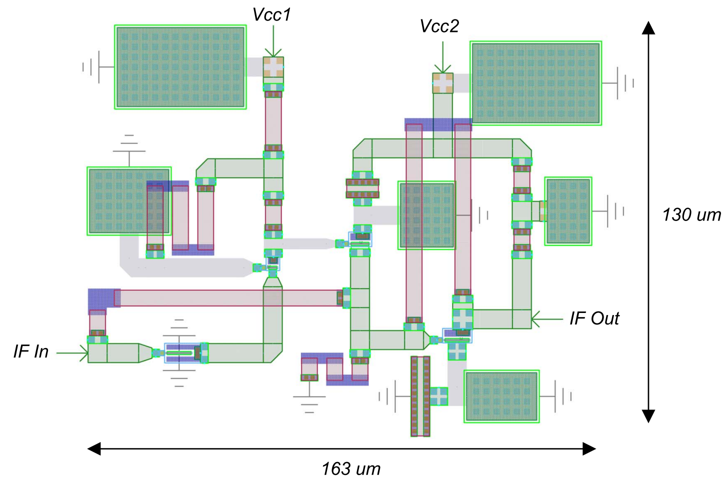


Figure 4.20: Layout of the IF amplifier. DC pads omitted for clarity.

was set to 12 µm to increase the low-frequency gain of the network and improve the linearity of the amplifier, as will be discussed below. The addition of L_{IF} to the interstage matching network serves to improve the source match of the amplifier, as detailed in Figures 4.19a and 4.11. When simulated in a 50 Ω system, the IF amplifier therefore has a bandwidth 3 dB bandwidth in excess of 60 GHz, gain of 27 dB and noise figure between 4-4.5 dB (see red traces in Figure 4.17). As the IF amplifier was not designed to operate in a standard 50 Ω system these values are purely indicative and do not reflect its performance when connected in the complete receiver system, as is outlined in Chapter 5.

Figure 4.21 details the simulated $IIP3$, $OIP3$, P_{1dB} and load-lines of the IF amplifier. Depending on the value of V_{cc2}, the amplifier begins to go into compression for input power levels above -30 dBm. The load-lines in Figure 4.21c reveals that the voltage swing of Q4 is the limiting factor of P_{1dB}. Q4, which operates as a class A output stage, causes the amplifier to go into compression as its V_{ce} enters the knee region, preventing the transistor from performing amplification. Increasing the DC collector-emitter voltage of Q4, in an attempt to increase the maximum voltage swing, was found to offer little improvement, as shown in Figure 4.21b. Given

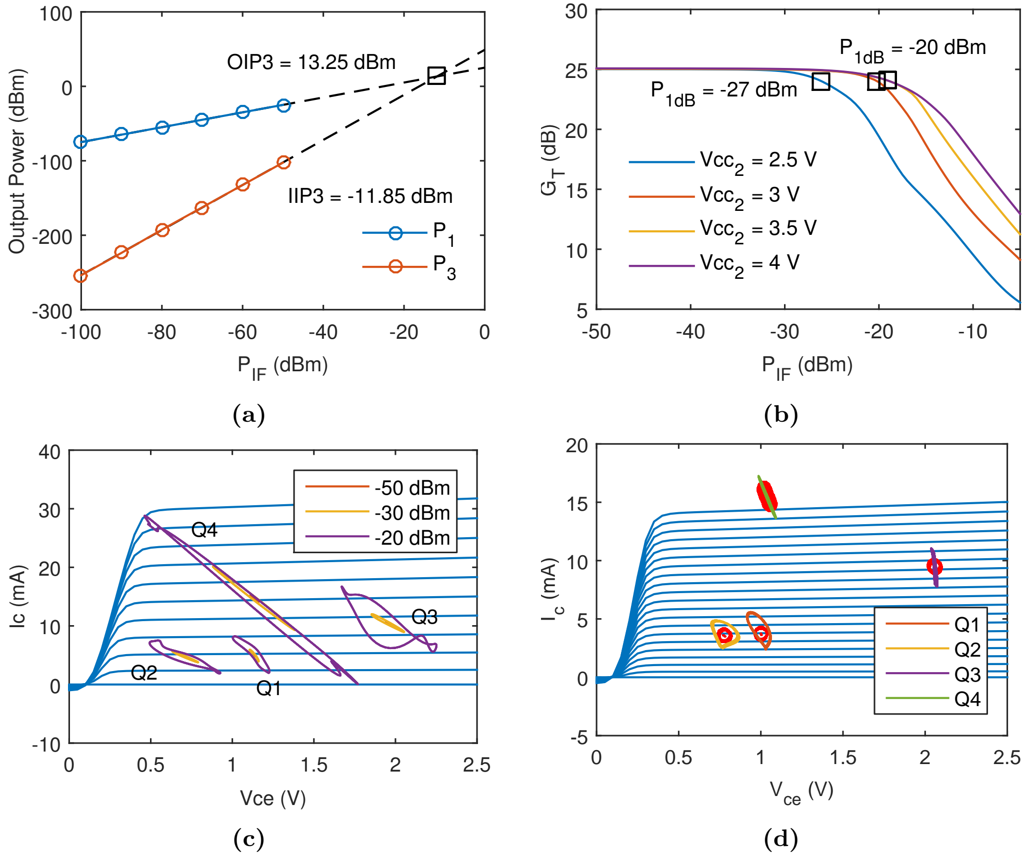


Figure 4.21: (a) Third-order intercept point of the IF amplifier, extrapolated from simulation data. $f_{IF} = 10$ GHz, $\Delta f = 1$ GHz. (b) Dependency of the amplifier's 1 dB compression point on the value of V_{cc2}. (c) Extrinsic load lines of Q1-Q4 for swept input power level; $V_{cc_2} = 3$ V. (d) Extrinsic load line of each transistor when the amplifier is connected to the output of the mixer. Red circles indicate the simulated load lines when an ideal LO short is placed at the output of the mixer (i.e. when no LO leakage to the amplifier input occurs). $P_{IF} =$ -50 dBm.

the intended RF frequency of operation of the receiver (where free-space path loss is extremely high) and the fact that the preceding mixer exhibits conversion loss, it is unlikely that any received signal will have a power level close to P_{1dB} and hence such values of P_{1dB} are sufficient. One issue that may arise in the complete receiver is the presence of the large-signal LO tone at the input of the amplifier due to LO leakage in the mixer, which could drive the amplifier into compression regardless of the IF power level. This large-signal tone modulates the operating point of each transistor in the amplifier, as is visible in Figure 4.21d. If an ideal LO short-circuit is placed at the output of the mixer, thereby preventing the LO signal from entering the amplifier, the quiescent point of transistors Q1, Q2 and Q3 is seen to be invariant. However, the load-line of Q4 is largely unchanged when the LO leakage is removed. Gain compression simulations performed with an additional 210 GHz LO tone at -25 dBm (the power of the LO leakage signal at the input of the amplifier) showed little to no change in P_{1dB} so this was not deemed to be a concern.

4.3 RF hybrid design

Due to the requirement in transconductance mixers of combining RF and LO prior to injecting them into the base of the mixer, some form of combining network must utilised. As the receiver's antenna is integrated on chip an internal combining network must be implemented. One of the simplest and most broadband ways to combine the signals in the desired manner is to use a quadrature hybrid - providing both the necessary power combining and 90 degree phase shift for a single balanced topology. An ideal quadrature hybrid has the scattering matrix:

$$[S_{90}] = \begin{bmatrix} 0 & 0 & -j & 1 \\ 0 & 0 & 1 & -j \\ -j & 1 & 0 & 0 \\ 1 & -j & 0 & 0 \end{bmatrix} \tag{4.7}$$

that is, the signal at the outputs from a single input are 90 degrees out of phase with each other. One of the most common forms of quadrature hybrid is the branch line coupler, which is composed of two parallel Z_0 sections and two perpendicular $Z_0/\sqrt{2}$ sections. The branch line coupler is suitable for planar integration and can provide wideband performance if well designed. However, in integrated circuit technologies with multiple metal layers, a more compact quadrature hybrid can be realised if the coupled line sections are placed vertically over one another, creating a so called *broadside* hybrid coupler. Much work has been published on the design of such structures and there are design equations available to allow the synthesis of coupling networks with a wide range of coupling factors [51], [52]. For an equal power split between the outputs, a coupling factor of 3 dB is desired. The coupling factor (C) is defined as the ratio of the power at the input to the power at the coupled port. The other parameters of interest are the isolation (I), directivity (D), insertion loss (IL), amplitude balance (ΔA) and phase balance ($\Delta\phi$) of the coupler:

$$C = P_1/P_3 = S_{31} \tag{4.8}$$

$$I = P_1/P_4 = S_{41} \tag{4.9}$$

$$D = P_3/P_4 = S_{31}/S_{41} \tag{4.10}$$

$$IL = P_1/P_2 = S_{21} \tag{4.11}$$

$$\Delta A = |S_{21}| - |S_{31}| \tag{4.12}$$

$$\Delta\phi = \phi(S_{21}) - \phi(S_{31}). \tag{4.13}$$

Ideally, the amplitude and phase balance of the coupler will be zero and 90 ° across the entire frequency band of interest. Any deviation of these parameters from the ideal will degrade the balanced operation of the mixer, resulting in a reduced conversion gain and increased noise figure, as is evident from Figure 4.23. Similarly, the insertion loss of the coupler will translate directly into a further increase in noise figure as it is the first component of the receiver. The isolation of the coupler will determine the level of LO - RF leakage in the receiver. Poor LO-RF isolation can result in significant LO power reaching the integrated antenna. If the LO is within the bandwidth of the antenna it will be re-radiated by the antenna and will prevent signals at that frequency from being properly received. This problem could potentially be worsened by any phase noise on the LO signal - broadening the spectrum of the LO away from an ideal delta function. The issue of LO leakage to the RF port could potentially lead to notches in the received spectrum as a result. However, in heterodyne receiver systems where the LO frequency is suitably far away from the RF signal band this is not be a potential concern.

The design of the broadside coupler was initially performed using transmission line models in ADS and then fine tuned via electromagnetic simulations in Keysight Momentum. Numerous

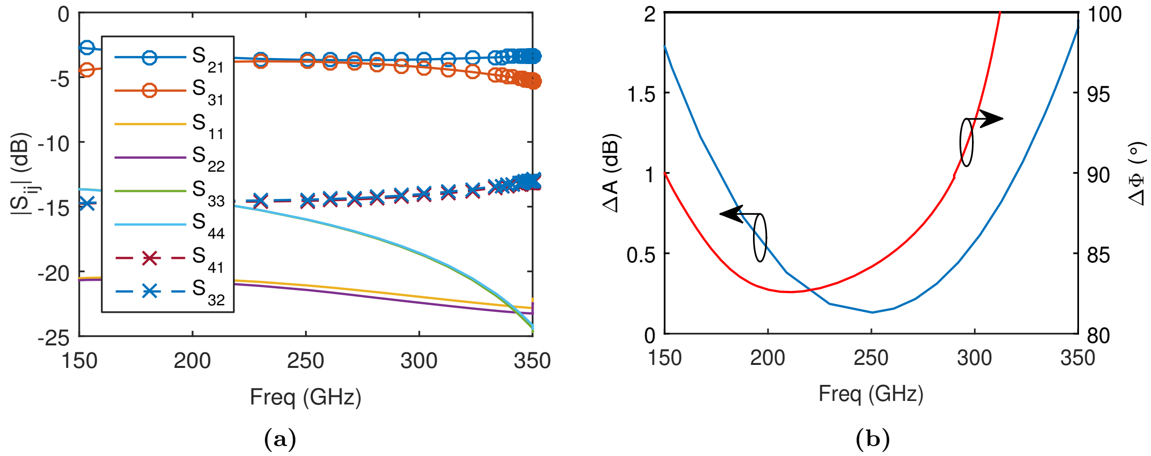


Figure 4.22: (a) EM simulated S-parameters and (b) amplitude and phase balance of the proposed coupler.

types of broadside coupled structure are presented in [52] but it was found that a simple structure consisting of two equal width tranmission line sections placed directly over each other provided the desired coupling factor. The electrical length of each line was initially set to be 90 degrees ($\lambda/4$) at the design frequency (250 GHz). The lengths were then adjusted until sufficient performance was achieved. In order to make the coupler more compact the transmission line sections were then meandered and their lengths re-adjusted to account for any capacitive couplings between the parallel meander sections. Finally, the feed lines, visible in Figure 4.25a, were added to allow the coupler to be fed from either side rather than along the same axis as the coupler. The entire structure was then re-simulated and optimised for a final time. One crucial design parameter is the choice of ground plane below the coupler. If M2 is chosen, the seperation between the lower transmission line (M3) and ground is then equivalent to that between M4 and M3 (see TSC 250 layer stack, Figure 2.3). As a result, a large proportion of the signal flowing in M3 couples directly to ground, rather than into M4, and 3 dB coupling cannot be achieved. If, instead, M1 is chosen as the ground plane, the increased distance from M3 to ground decreases the capacitive coupling between M3 and ground, thus enabling 3 dB coupling to be readily achieved.

The simulated S parameters, amplitude balance and phase balance of the final broadside coupler are presented in Figure 4.22. It can be seen that all four ports are well matched over an extremely broad frequency range. The impedance match of ports 3 and 4 is somewhat worse than that of ports 1 and 2, however. This is due to the fact that an equivalent transmission line width (5 µm) was used for both M4 and M3. This width corresponds to a 55 Ω impedance in M4 but somewhat greater in M3, due to its reduced thickness. The insertion loss of the coupler is approximately 3.8 dB between at 250 GHz. The additional 0.8 dB is due to conductive and is unavoidable. The noise figure of the receiver will be increased by over 0.8 dB as a result of this loss (0.8 dB from the insertion loss itself and a further increase due to the multiplication of the NF of the other receiver components). The isolation between ports 4/1 and 3/2 is between 13-15 dB across the entire frequency band. As previously discussed, the limited isolation of the coupler will lead to an LO signal 15 dB below the input LO power appearing at the antenna input. This may be problematic depending on the proximity of f_{RF} and f_{LO}.

During the design of the coupler a trade-off was made between its amplitude and phase balance. This was informed by the simulated performance of an ideal single-balanced transconductance mixer (Figure 4.12) with an RF hybrid whose amplitude and phase balance was varied. The results of these simulations are contained in Figure 4.23. It is clear that from a noise figure perspective the amplitude imbalance of the coupler should be kept as low as possible - the gradient of the contour plot is significantly steeper along its x-axis - and that phase imbalances of up to ± 10° have little effect on either G_c or NF. The amplitude imbalance of the coupler was

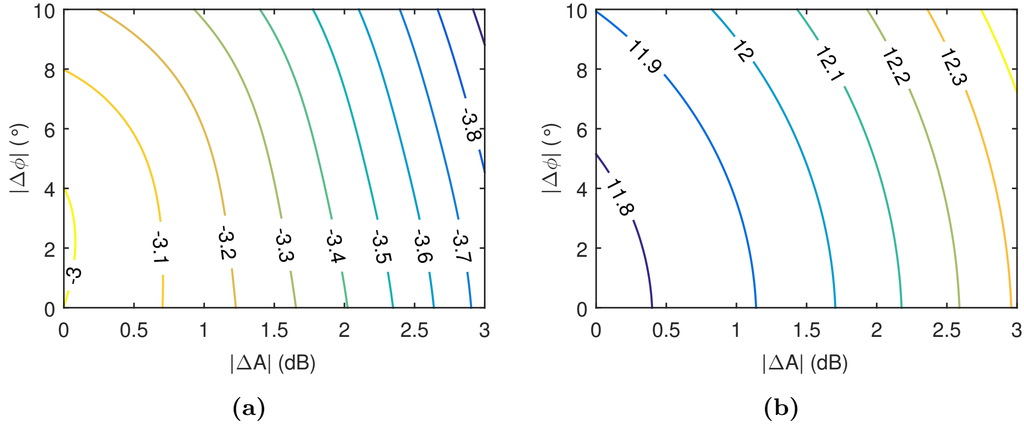


Figure 4.23: RF hybrid amplitude and phase balance dependency of (a) conversion gain and (b) noise figure of the ideal single-balanced transconductance mixer.

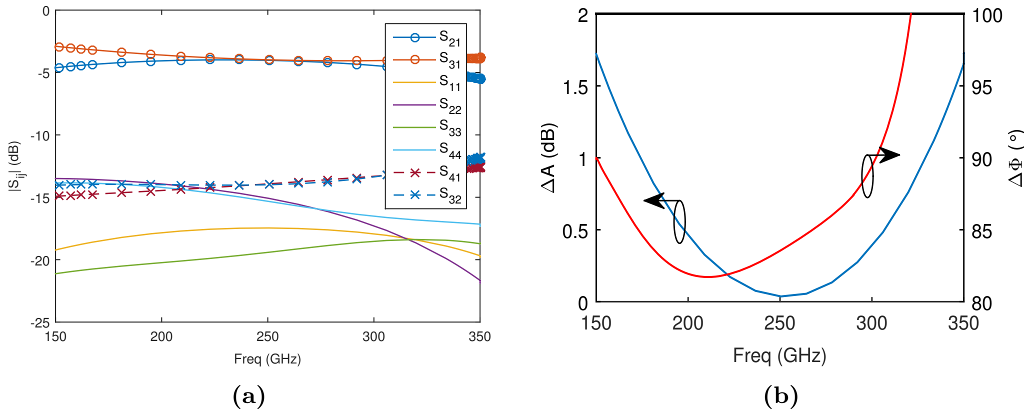


Figure 4.24: (a) EM simulated S-parameters and (b) amplitude and phase balance of the combined receiver input network.

therefore prioritised. Figure 4.22b contains a plot of the simulated amplitude and phase balance of the coupler. The amplitude balance of the coupler reaches a minima at 250 GHz (the design frequency) and is below 1 dB across the entire H-band, indicating that the coupler operates as intended. The phase balance is within ± 8° over the same band. An increase in system noise figure of approximately 0.1 dB can be expected as a result of the amplitude and phase imbalance of the hybrid. Plan and isometric views of the final coupler design can be found in Figure 4.25. The coupler measures 117 x 57.5 μm^2 .

In the final layout of the receiver transmission line sections were added to the inputs of the coupler to connect it to the LO input pad and antenna feed. Proper care was taken to ensure that these feed sections degraded the performance of the coupler as little as possible. The amplitude/phase balance and S parameters of the combined feed network and coupler are plotted in Figure 4.24. An additional 0.2 dB of insertion loss is incurred due to the addition of the RF/LO feed lines, which degrades the noise performance of the receiver and increases the required LO drive power. Both sections were kept to a minimum to reduce this loss in so far as possible while still maintaining good amplitude and phase balance. As before, the amplitude balance was prioritised and remains with 1 dB over the entire H-band. The phase balance of the network is again within ±10°.

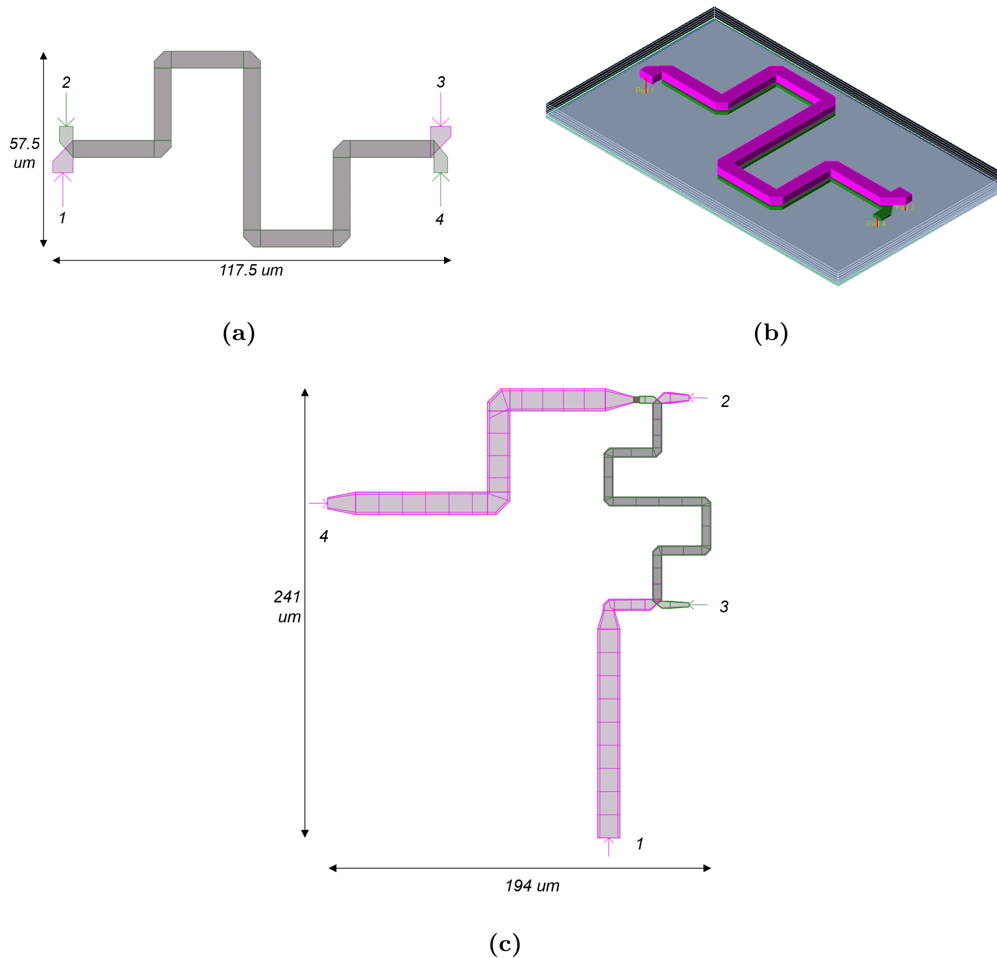
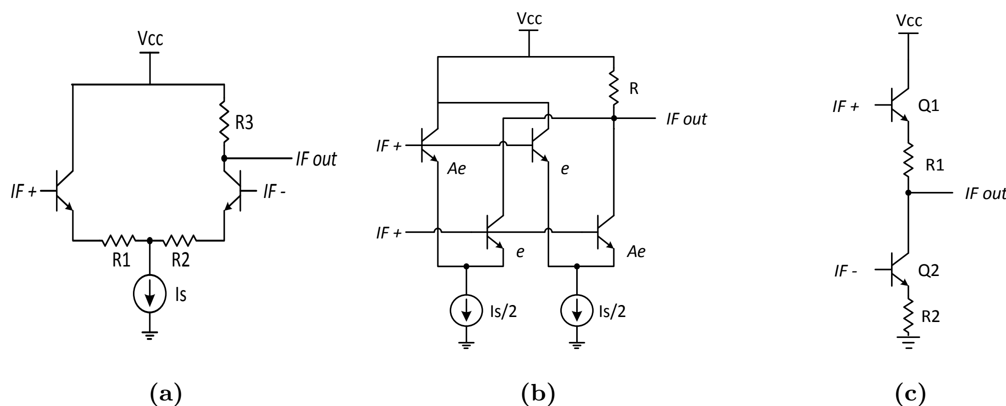


Figure 4.25: (a) Plan and (b) isometric views of the broadside coupler. (c) Plan view of the final receiver input network. Port 1 is connected to the integrated antenna, Port 4 to an LO probe pad and Ports 2 and 3 to the single balanced mixer.

4.4 IF Balun Design

In the chosen receiver topology the IF signals generated at the output of each IF amplifier must be combined using a network that can sum two differential signals. Often, this task is performed by a passive 180° hybrid coupler or balun network. Many such designs have been proposed and offer wideband performance with low insertion loss and good amplitude and phase balance [53], [54]. The primary issue with the use of a passive hybrid or balun is one of size. Most passive hybrids are based on $\lambda/4$ transmission line sections. At low IF frequencies such structures become excessively large and are not suitable for use in extremely compact integrated circuits. One alternative to distributed hybrids/baluns is to use a lumped-element balun, such as the type proposed in [55]. The drawback of this approach is that it may require large inductors and/or capacitors, which are again too large for use here. In integrated circuit technologies with small feature sizes, where transistors can be used quite freely, the use of an active balun is therefore quite attractive. Figure 4.26 contains simplified schematics of three such circuits proposed in the literature to date [56], [57]. Of the three, the push-pull topology (Fig. 4.26c) is the most suitable for use here. It offers the highest linearity of the three [57] whilst also being a relatively simple circuit to integrate. The differential structure in Figure 4.26a is equally as simple but suffers from poor linearity.

The push-pull balun is comprised of a pair of transistors, one in common-collector (Q1)



(a) (b) (c)

Figure 4.26: Simplified schematics of three types of active balun: (a) Differential, (b) Multi-TanH and (c) Push-Pull.

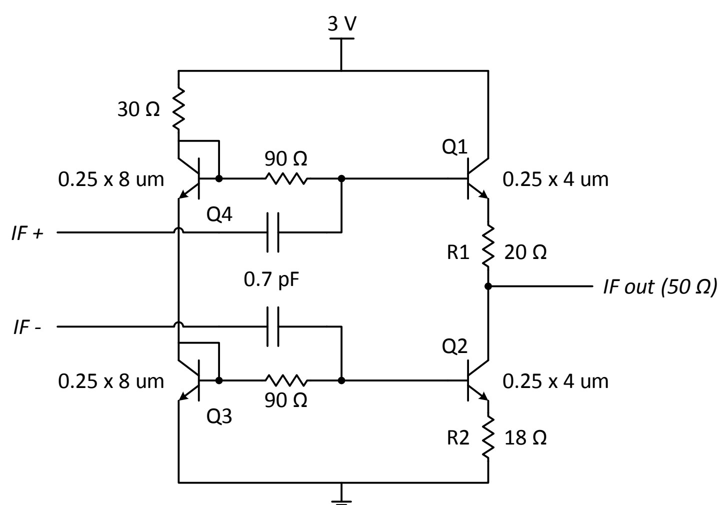


Figure 4.27: Schematic diagram of the finalised IF balun design. Port impedances are detailed in brackets.

configuration and the other common-emitter (Q2). The operating principle of the active balun is based on this difference in configuration: the CC transistor provides non-inverting gain between its base and emitter, while the CE transistor provides inverting gain between its base and collector. The input differential IF voltage is therefore converted to two in phase signals which are then combined at the IF output pin. The overall gain of the balun is the sum of the two individual signal path gains. Resistor $R2$ acts a degenerating resistor for Q2, reducing its gain to the required level to ensure equivalent gain in each signal path. This also increases the bandwidth of the CE transistor. Due to its common-collector configuration, Q1 is inherently wideband [49]. Resistor $R1$ allows the output impedance of the balun to be set and also provides some control over the gain in the CC signal path.

Initially, the balun was designed independently to find the optimum values of L_e, $R2$, $R1$ and Vcc. The balun was then co-designed with the IF amplifier to optimize the performance of the receiver chain. In the initial design, it was found that the optimum base-emitter voltages for Q1 and Q2 are of the order of 0.8 V. This value is somewhat below the collector voltage of the preceding IF amplifier ($\sim$ 1.1 V). This discrepancy precludes series biasing the base of Q1 and Q2 from the collector voltages of the two IF amplifiers. Instead, the biasing of the two stages must be separated and supplied independently. This is achieved through the use of two DC blocking capacitors at the IF inputs of the balun. These capacitors must be as large as possible to reduce the attenuation of low frequency IF signals and to facilitate a proper match between

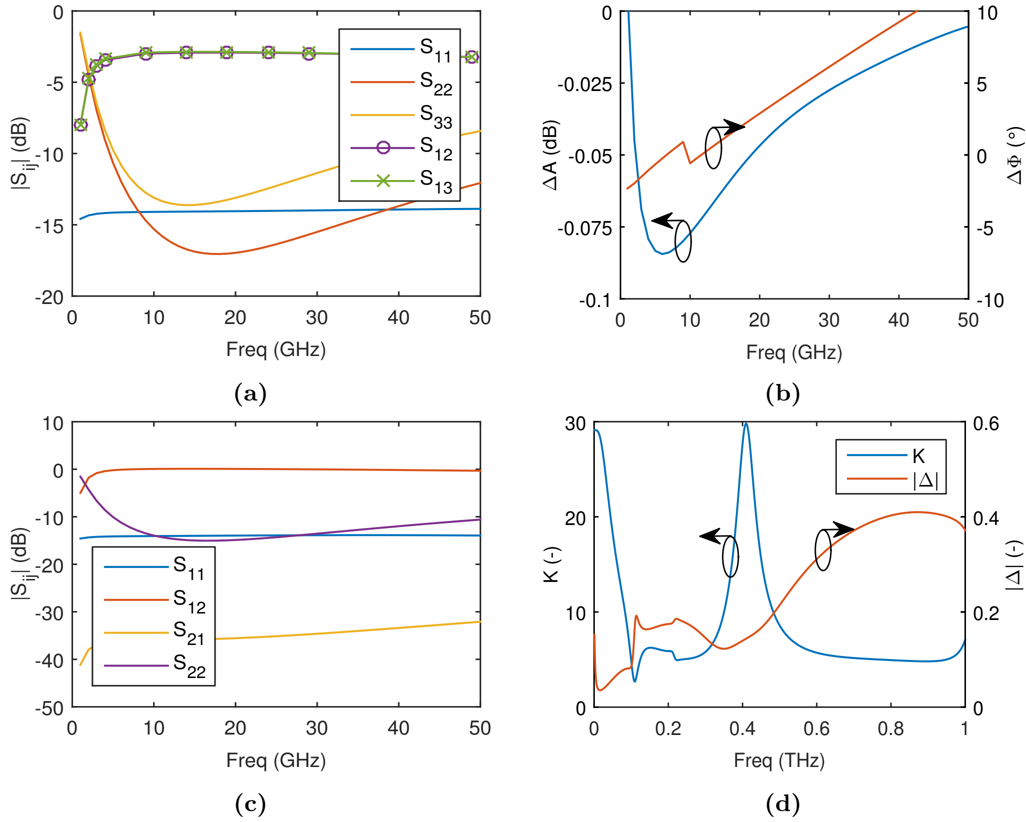


Figure 4.28: (a) Single-ended S parameters of the IF balun. Port numbering is as follows: Port 1 - IF output; Port 2 - Q1 input; Port 3 - Q2 input. (b) Amplitude and phase balance of the IF balun. (c) Differential S parameters of the IF balun. Port 1 - IF output, Port 2 - differential IF input. (d) Stability factor (K) and $|\Delta|$ of the balun.

the output of the IF amplifier and the input of the balun. Hence a value of 0.7 pF is used. The necessary base bias is then supplied by two diode connected transistors (Q3 and Q4) through 90 Ω resistors. Each transistor pair (Q1/Q4 and Q2/Q3) therefore effectively forms a current mirror. The value of each component in the circuit affects the input match of both IF inputs and was carefully chosen to provide the desired performance. Due to the non-idea DC blocking capacitors, achieving a good impedance match across the entire IF band is not possible. In the design of the IF amplifier the gain of the ouptut CE was found to be dependent on its collector resistance ($R4$). Careful selection of $R4$ allows for an increase in gain and good impedance match between the IF amplifier output and IF balun input. For this reason the output of the IF amplifier was matched to 100 Ω and the two base resistances were chosen as 90 Ω to provide a good match. The emitter lengths of Q1 and Q2 were chosen to maximise the bandwidth of the balun by ensuring peak f_T biasing. The single-ended S parameters of the balun are plotted in 4.28a, where port 1 refers to the IF output and ports 2 and 3 to the IF inputs at Q1 and Q2, respectively. Due to the different configuration of each transistor (CC/CE) their input impedances are slightly different and hence the return loss between IF amplifier and balun is not equivalent for each signal path. The value of the resistor at the base of Q2 could be altered to improve its return loss but this would alter the gain in that signal path and degrade the amplitude balance of the balun. Currently, the amplitude balance of the balun is within 0.1 dB between 1-50 GHz. Thus it is evident that the gain in each signal path is equivalent, as desired. The excellent amplitude balance of the balun ensures that any common-mode signals present at its inputs will be largely cancelled out. The phase balance of the two signal paths is within 15° (Figure 4.28b). When driven from a single differential port (with 180 Ω impedance), the gain of the two signal paths results in a

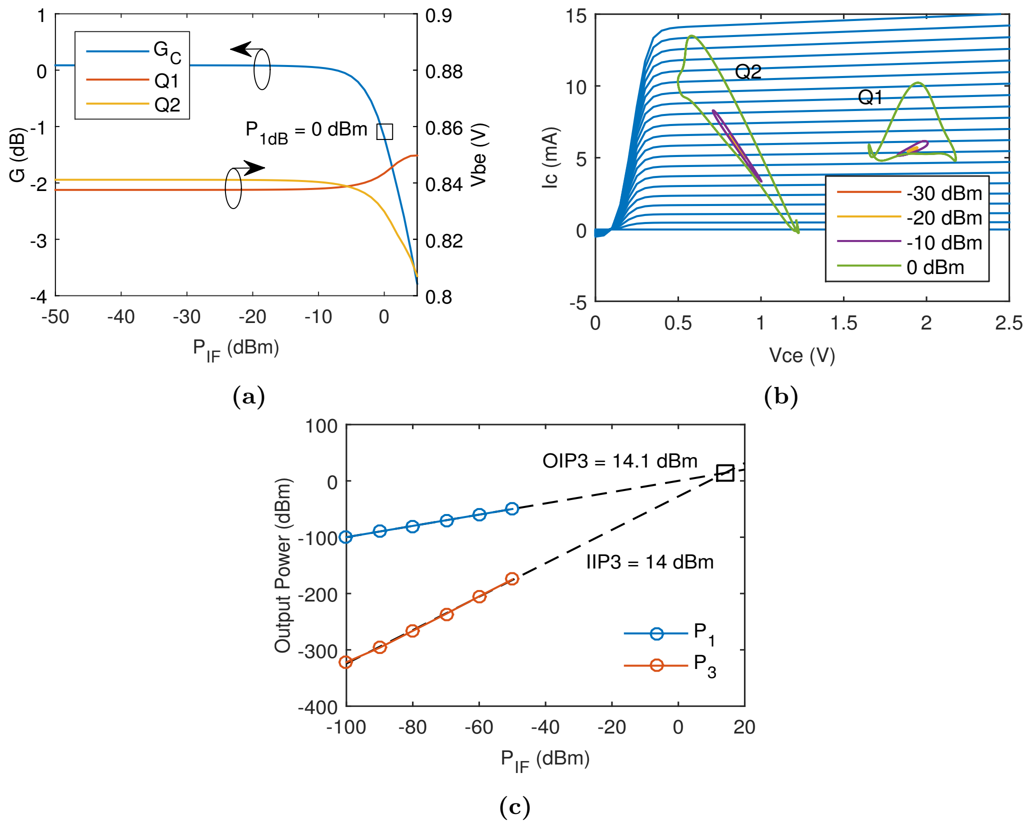


Figure 4.29: (a) Transducer power gain and base bias voltages of Q1, Q2 of the IF balun for swept input power level. The black marker represents the input 1 dB compression point of the balun. (b) Load lines of Q1 and Q2 for swept input power level. (c) Simulated 3rd order intercept point of the IF balun, as indicated by the black marker.

overall gain of approximately 0 dB, as seen in Figure 4.28c. The bandwidth of the balun is well in excess of 50 GHz. The attenuation at low frequencies is a result of the insertion loss of the 0.7 pF capacitors. As some higher order mixing products may leak from the mixer through the IF amplifier and reach the input of the balun it is important that the balun is unconditionally stable up to several multiples of the fundamental LO frequency. Figure 4.28d shows that $K > 1$ and $|\Delta| > 0$ and hence the balun is unconditionally stable for all frequencies up to 1 THz.

The linearity of the balun was examined via large-signal simulations in ADS. The results of these simulations can be found in Figure 4.29. The input 1 dB gain compression point of the balun is approximately 0 dBm, significantly higher than either of the preceding stages of the receiver. As the input IF power increases, the base-emitter diodes in Q1 and Q2 rectify a portion of the incident signal, altering the base-emitter voltages of each transistor. By this mechanism the operating point of the balun is altered, moving away from its nominal value. The effect of this compression is visible in the load lines of Q1 and Q2, as plotted in Figure 4.29b. The transistors operate in class A for input powers below 0 dBm, conducting across the full input cycle. Near the point of compression (0 dBm) and beyond, both transistors deviate from class A, resulting in a distorted output waveform. As is the case with P_{1dB}, both the input and output 3rd order intercept point also occur at power levels far greater than those of the previous amplifier stage, see Figure 4.29c. It can thus be concluded that the linearity of the complete system will not be limited by the linearity of the balun - other parts of the receiver will go into compression long before the power level is high enough to drive the balun into compression or towards its IP3 point.

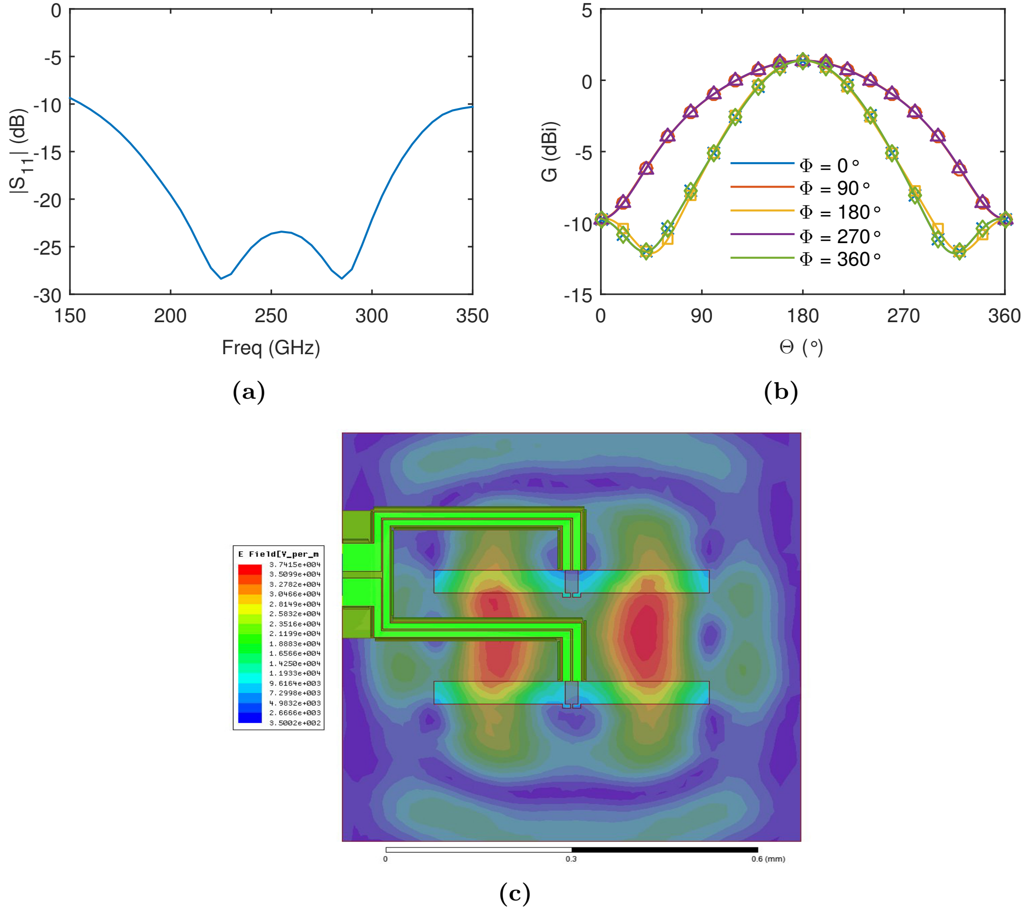


Figure 4.30: (a) Input reflection coefficient of the amplifier, normalized to 50 Ω. (b) Simulated beam pattern versus Θ, Φ. (c) Electric field distribution of the antenna's radiated field (V/m).

4.5 Antenna Design

The design of the on-chip antenna incorporated in the final receiver design was not completed as part of this thesis. The antenna was designed by Dr. D Cavallo of the THz Sensing Group at Delft University of Technology. Brief simulation results are included here to outline the performance of the antenna.

The antenna is based on a novel double-slot structure which utilises shielded microstrip feed lines to achieve extremely wide impedance bandwidth. The antenna acts as a hybrid between a leaky-wave and resonant type structure. The radiating slots are etched into the top layer metal (M4) and radiate down through the remaining layers of the structure and out the backside of the chip. The antenna is designed for use with a dielectric lens, which focuses the divergent beam that emerges from the backside of the chip to improve the gain of the antenna. The theory of operation of a double-slot antenna with dielectric lens can be found in [58]. The shielded microstrip lines are implemented by the use of densely placed vias between M4-M3 and M3-M2, which act as artifical metallic walls, and a ground plane on the lowest metal layer (M1). Feeding of the slots is performed on M4. The simulated impedance bandwidth of the antenna, shown in Figure 4.30a, is approximately 80 %. The 3 dB beamwidth of the antenna is approx. 45°. The simulated magnitude of the electric field at 250 GHz is shown in Figure 4.30c.

Chapter 5

Receiver Characterisation

The key performance parameters of the proposed single balanced receiver are presented in Figures 5.1, 5.2 & 5.3. The complete receiver has an IF bandwidth of 42 GHz, as shown in Figure 5.1a. The mid-band conversion gain of the receiver is approximately 23 dB, high enough to enable further components to be cascaded to the IF output (e.g. IF gain blocks, filters etc.) without degrading the system noise figure. The minimum single sideband noise figure of the receiver is approximately 13.6 dB and occurs at f_{IF} = 10 GHz. For IF frequencies either side of 10 GHz, the noise figure of the receiver rises in response to the decreased conversion gain of the mixer, see Figure 5.1b. The addition of the inductance L_{IF} between the mixer and IF amplifier extends the bandwidth of the receiver by approximately 5 GHz due to the increased bandwidth of the mixer, as is evident from the dashed traces of Figure 5.1. The decrease in low frequency mixer conversion gain is compensated for by a corresponding increase in IF amplifier gain, giving equivalent low-frequency gain in both cases. L_{IF} also reduces the noise figure of the receiver and decreases the rate at which the noise figure increases as $f_{IF} \rightarrow \infty$ thanks to an improved source reflection coefficient (c.f. Figure 4.19a). The noise figure of the receiver is seen to be below 15 dB over its entire IF bandwidth. Careful co-design of the mixer and IF amplifier ensured that the gain of the amplifier peaks at a high frequency than the conversion gain of the mixer begins to roll off and thereby leading to a flat overall response. The RF bandwidth of the receiver, visible in Figure 5.1c, is in excess of 135 GHz (175-313 GHz), covering almost the entire H-band. Optimum performance occurs at the lower end of the H-band, where the noise figure of the mixer is at its lowest. Above this point, parasitic effects limit the conversion gain of the mixer which in turn results in an increase in noise figure. The RF port of the receiver is well matched over the entire H-band due to the wideband performance of the RF hybrid presented in Section 4.3. In terms of LO power, the performance of the receiver is optimised for input power levels between 0-2 dB, making it suitable for use with frequency multiplier sources. The LO-IF isolation of the receiver is between 13-15 dB across this range, as seen in Figure 5.1d. This isolation could be improved by increasing the value of C_{shunt} to realise a lower impedance LO short circuit at the output of the mixer. Doing so would result in a decrease in both RF and IF bandwidth however. As the output of the receiver is matched to 50 Ω, any standard low pass filter can be used to remove this LO tone before passing the IF signal into further receiver components.

Figure 5.2a shows the dependency of the receiver's conversion gain on the input RF power level. It is clear that the linearity of the receiver is limited by that of the IF amplifier: a 1 dB compression point of -24 dBm is of the order found in Figure 4.21b. As discussed in Section 4.2, input power levels in excess of -24 dBm are unrealistic at such high RF frequencies and hence this value of P_{1dB} is likely sufficient. The same can be said of the simulated $IIP3$ of the receiver, which occurs for input powers somewhat beyond the expected level (-13.6 dBm).

An image of the layout of the receiver can be found in Figure 5.5. The complete receiver measures 0.9×1.19 mm^2, of which approximately two-thirds is consumed by the integrated

Ref.	f_0 (GHz)	G_c (dB)	NF_{ssb} (dB)	B_{IF} (GHz)	B_{RF} (GHz)	P_{LO} (dBm)	P_{DC} (mW)	Area (mm^2)	Tech.
[59]	220	16	18	-	30	0	216	0.6×1.1	SiGe HBT
[60]	220	3.5	$10.4 - 12.3$	10	14	4	110	1.75×2.75	GaAs mHEMT
[61]	220	1.5	$6.5 - 7.5$	20	-	12	-	0.75×2	InGaAs mHEMT
This Work	220	23.3	$13.5 - 15.3$	42	138	0	305	0.9×1.19	InP DHBT

Table 5.1: Comparison of the proposed single-balanced receiver to previously published receivers at similar operating frequencies.

antenna. The antenna is located as close as possible to the input port of the RF hybrid to minimize feeding losses. Multiple decoupling capacitors of various capacitance values were placed close to the DC pads of the receiver to help ensure no oscillations occur due to RF signals leaking to the DC supply. The entire receiver consumes 305 mW of DC power, most of which is drawn by the IF amplifiers.

In order to benchmark the simulated performance of the proposed receiver, a comparison of previously published complete receivers operating at the same frequency as the one designed here was made. The results are documented in Table 5.1. In the creation of this table some data was inferred from graphs/figures in the relevant papers. Using this data, the SNR of a simple communication link based on each of the receivers was calculated to compare the theoretical capacity for varying received power levels, the details of which will be discussed below. The results are shown in Fig. 5.4. Of the four designs, only the receiver proposed here contains no front-end LNA.

It is clear that the proposed receiver has significantly greater bandwidth (both RF and IF) than other designs, largely due to the use of InP DHBT technology. As previously reported [17], the TSC 250 process allows for the creation of extremely wideband circuits, thanks to its small feature size and highly engineered band structure/back end process, which lead to unparalleled values of f_T and f_{max}. InP DHBT technology is not completely free of drawbacks, however. As discussed in Section 2.3.2, the noise performance of a HBT in a common-emitter configuration is limited by its DC forward current gain (β_0). Modern HBTs, such as those in the TSC 250 process, often trade β_0 with R_b or other parameters in order to increase f_T and f_{max}. As such, the value of β_0 in such transistors is often quite moderate, as found in Chapter 3. This places an inherent limit on the noise performance of any circuit implemented with HBT technology. From Table 5.1, it can be seen that designs based on HEMT technologies offer lower noise figures than the proposed receiver, as is expected. It should also be noted that the noise figure of the proposed receiver is largely determined by that of the single-balanced mixer alone. During the design of the mixer, certain trade-offs were made to maximize the IF bandwidth, at the cost of G_c and NF. The noise figure of the mixer could be reduced somewhat (but by no more than ~ 1 dB) by sacrificing some of its IF bandwidth. It is instructive to compare the theoretical capacity of each receiver, as shown in Figure 5.4. From this figure, it is clear that the maximum capacity of the proposed receiver is significantly greater than that of [60] or [61]. As the received power level increases, the capacity of the system is limited not by the system noise figure but rather its IF bandwidth (as expected given the logarithmic dependency on SNR in the Shannon-Hartley theorem). The receivers published elsewhere offer higher capacity at lower values of P_{RF} thanks to their lower noise figures. Ultimately, however, the massive bandwidth offered by InP DHBT technology is difficult to match. It can be concluded that if sufficient received power is available

the IF bandwidth of a receiver should be prioritised in order to maximise C, not the noise figure. Due to its relatively high noise figure, the proposed receiver is not well suited for applications where a high receiver sensitivity is required. Rather, it is better suited for applications such as wireless backhaul, where sufficient received power may well be available to make use of the high IF bandwidth. By way of example, for a received power level of -40 dBm, the theoretical capacity of the previously outlined SISO link is of the order of 200 Gbps (c.f. Fig 5.4). Assuming a transmit power level of 10 dBm, clear sky conditions and a 1 km path length, achieving $P_{rx} > -40$ dBm requires transmit and receive antenna gains in excess of 40 dBi (for $\eta = 0.7$). At H-band frequencies this corresponds to an antenna diameter of the order of 10 cm, a value well below that required at current LTE frequencies. The Shannon-Hartley theorem represents the maximum theoretical capacity of any link. In reality, due to difficulties in modulation/de-modulation, this upper bound is never practically feasible. The excess theoretical C of the receiver presented here allows for the use of simpler modulation techniques while while still maintaining very high link capacity.

The proposed receiver also requires far less LO drive power than either of the designs in [60] or [61], thanks to the use of a transconductance mixer topology as opposed to a resistive mixer, which typically requires higher LO power. The proposed design is thus well suited for use with frequency multiplier LO sources.

In terms of noise figure, the receiver presented here has approximately 2-3 dB higher noise figure than the amplifiers documented in Table 1.1. As previously discussed, only one of the designs using the TSC 250 process reported gain in excess of 20 dB and this required a chip size approximately 1.5 times that of the proposed receiver. Again, if the received power is sufficient this increase in noise figure may not be significant. Future receiver designs in the TSC 250 process intended for use at H-band frequencies could potentially omit the front-end LNA, without an overly large penalty in terms of noise figure. This would lead to more compact, less power hungry receiver circuits. The mixer-first receiver topology is therefore very promising for the design of receiver circuits at very high frequencies, where truly "low-noise" amplifiers are no longer possible.

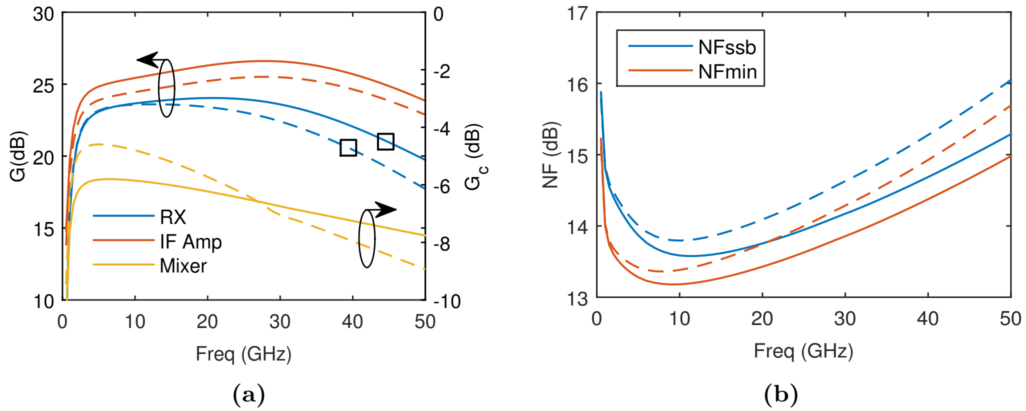


Figure 5.1: (a) Transducer power gain of the final single-balanced receiver, IF amplifier and mixer. The 3-dB cut-off frequency of the receiver is indicated by the black markers. (b) Single-sideband and minimum noise figure of the receiver. Solid traces: with L_{IF}. Dashed traces: without L_{IF}.

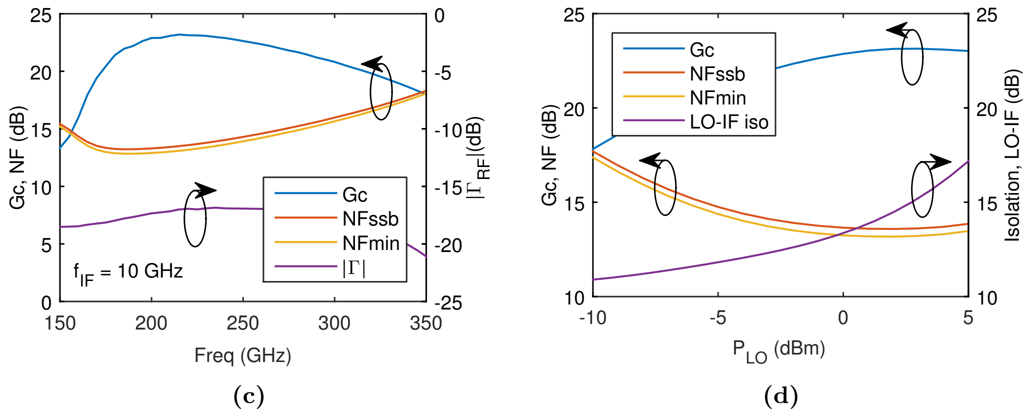


Figure 5.2: (a) RF frequency response of the complete receiver's conversion gain, noise figure and input match. f_{IF} fixed to 10 GHz. (b) Conversion gain, noise figure and LO-IF isolation of the complete receiver versus LO power level. f_{RF} = 220 GHz, f_{LO} = 210 GHz.

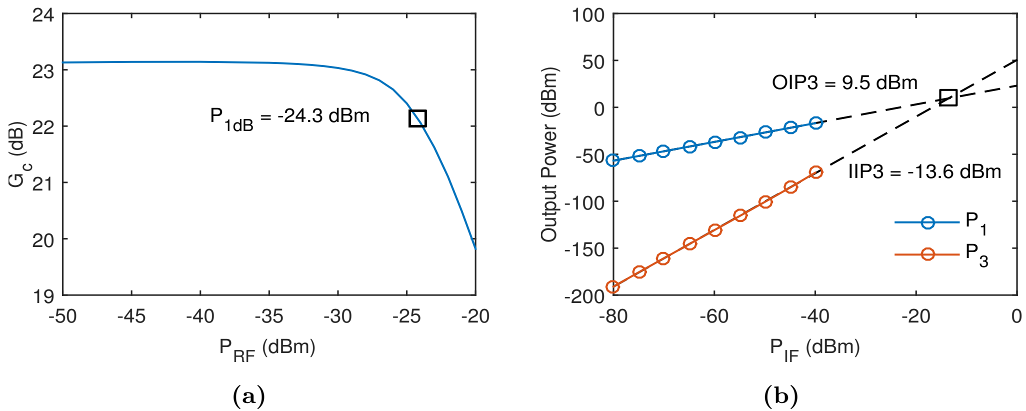


Figure 5.3: (a) Conversion gain of the receiver versus input RF power level. Input 1 dB compression point indicated by the black marker. (b) Extrapolated third order intercept point of the receiver. f_{IF} = 10 GHz, Δf = 1 GHz.

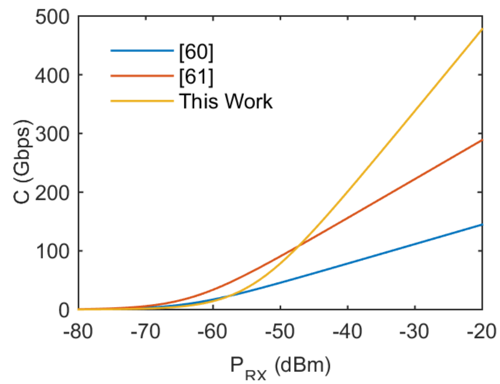


Figure 5.4: Theoretical capacity of a communication link based on the proposed receiver and others reported in the literature for varying received power levels. $T = 290$ K.

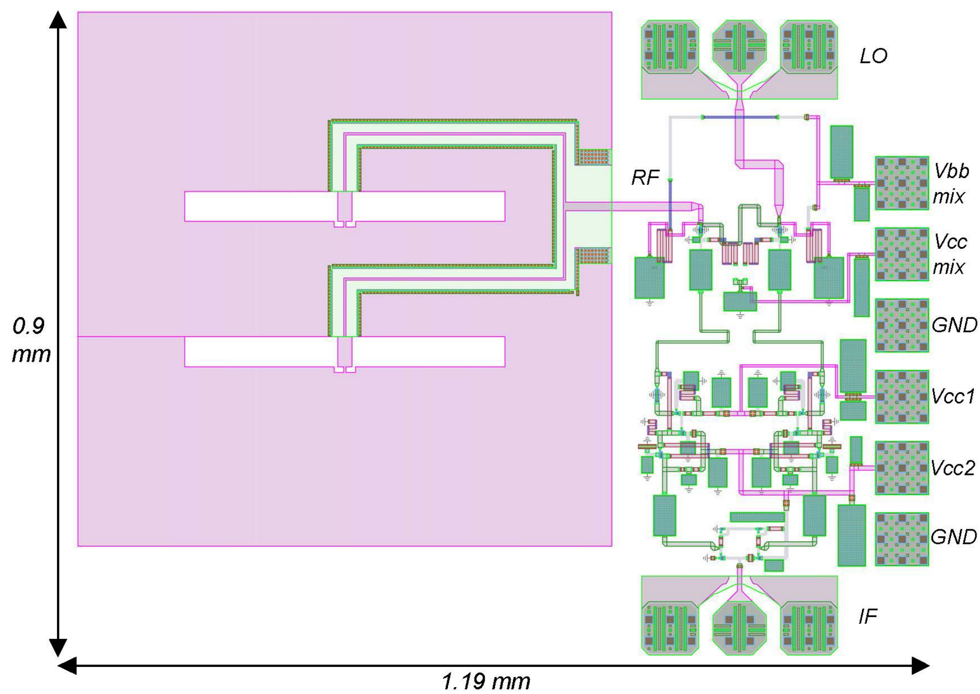


Figure 5.5: Layout of the completed single balanced receiver.

Chapter 6

Conclusions and future work

6.1 Conclusions

In this thesis, the design of a mixer-first wideband receiver for use at H-band frequencies has been presented. The proposed receiver uses no front-end LNA. Instead, it utilises a single-balanced topology, composed of a broadside coupled RF quadrature hybrid, single-balanced transconductance mixer, wideband IF amplifier and active IF balun.

The proposed receiver has IF and RF bandwidths of 42 and 138 GHz and requires only 0 dBm LO drive power, thanks to the use of a transconductance mixer topology. The total conversion gain of the receiver is 23 dB, a value large enough to neglect the noise contribution of any following receiver stages.
The noise figure of the receiver was found to be largely determined by that of the single-balanced mixer itself, due to the lack of any gain element preceding the mixer. It was found that there was no clear optimum bias point for the mixer - instead, a trade-off was made between its conversion gain and noise figure to minimize the overall system noise figure of the receiver. Careful co-design of the mixer, IF amplifier and interstage matching network allowed for wideband operation of both the mixer and IF amplifier, leading to a very wide receiver IF bandwidth. The inability to properly terminate the LO signal and its harmonics at the collector terminal of the transconductance mixer led to a reduction in conversion gain of approximately 2 dB. The collector LO termination was tuned to maximise the IF bandwidth of the receiver, at the cost of G_c and NF. As a result of this non-ideal termination a portion of the input LO signal was found to leak to the IF terminal of the receiver. Proper impedance matching between the mixer and IF amplifier ensured that the return loss between the stages was kept to an acceptable level over the entire IF bandwidth.

The total chip size of the receiver measured 0.9×1.19 mm^2, significantly smaller than front-end LNA designs utilising the same process presented in [15–17]. As the system noise figure of the complete receiver is only 2-3 dB higher than LNA designs reported in the literature at these frequencies (Table 1.1), the mixer-first topology is a promising receiver design at frequencies above 200 GHz, where truly low-noise room-temperature amplifiers no longer exist. The maximum capacity of the proposed receiver was found to be notably higher than that of previously reported H-band receiver designs (c.f. Table 5.1). Due to its extremely wide IF bandwidth, the proposed receiver is well suited for use in high-datarate systems such as wireless backhaul networks. The compact nature of the receiver also makes it well suited for the creation of multi-pixel receivers, which could be used in THz imaging systems.

6.2 Future work

The primary limitations of the proposed receiver design are related to the mixer's LO termination and impedance transformation between the output of the mixer and input of the IF amplifier. It would be of interest to further investigate the IF amplifier topology with a view to achieving a better impedance match without the need for interstage matching. Whether this is possible given the large output impedance of the mixer is not immediately obvious. Achieving a better mixer LO termination may be possible through the use of arbitrary impedance synthesis techniques or filter networks and should also be investigated further.

Implementing an active power combining network to provide the necessary combination of RF and LO signals would negate the need for a single-balanced architecture and could lead to a significantly more compact receiver. This should be done without further degradation of the receiver's noise figure or bandwidth, however.

More work is needed to properly evaluate and enhance the transconductance mixing model developed by Johansen *et. al* in [36]. Doing so could potentially allow for a rigorous derivation of optimum transistor sizing and biasing conditions, resulting in an improvement in overall receiver performance.

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James Campion, September 2015

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