



**CHALMERS**  
UNIVERSITY OF TECHNOLOGY

---

# **DC/DC Converters for High Conversion Ratio Applications**

A comparative study of alternative non-isolated DC/DC converter topologies for high conversion ratio applications

Master's thesis in Electrical Power Engineering

**JOHANNES BROBERG**  
**KIMON SFIRIS**



# DC/DC Converters for High Conversion Ratio Applications

Master's Thesis in Electric Power Engineering

JOHANNES BROBERG  
KIMON SFIRIS

Department of Energy & Environment  
Division of Electric Power Engineering  
CHALMERS UNIVERSITY OF TECHNOLOGY  
Gothenburg 2015

DC/DC Converters for  
High Conversion Ratio Applications  
Master's Thesis in Electric Power Engineering  
JOHANNES BROBERG  
KIMON SFIRIS

© JOHANNES BROBERG  
KIMON SFIRIS, 2015.

Department of Energy & Environment  
Division of Electric Power Engineering  
Chalmers University of Technology  
SE-412 96 Gothenburg  
Sweden  
Telephone +46 (0)31-772 1000

Chalmers Reproservice  
Gothenburg 2015

DC/DC Converters for  
High Conversion Ratio Applications  
Master's Thesis in Electric Power Engineering  
JOHANNES BROBERG  
KIMON SFIRIS  
Department of Energy & Environment  
Division of Electric Power Engineering  
Chalmers University of Technology

### **Abstract**

This thesis investigates how alternative topologies to the standard buck converter can be used in applications with a high voltage conversion ratio. The purpose is to match high demands on voltage conversion ratios and efficiency without a considerable increase in cost and footprint size. Five alternative topologies are identified, four of these are compared through simulations. Simulation models were built with component models from manufactures and the setup where focused on comparing characteristics dependent on topology design. Two topologies show an improved performance compared to the standard buck converter. One topology is the tapped inductor buck which is based on different effective inductance during the charge and discharge phases of the converter. The other topology, SEPIC fed buck, a parallel converter technology which creates multiple paths for the energy which reduces the  $I^2$  losses. The thesis concludes that it is possible to increase the efficiency with approximately 1% with an alternative topology and it also result in a longer duty cycle. The trade-off is a slightly increased size and increased cost due to the use of coupled inductors which needs to be custom made.

**Keywords:** POL, DC/DC converter, Standard Buck Converter, LTspice



## Acknowledgements

First of all we would like to thank our supervisor Andreas Karvonen for all feedback and help during our thesis work. We would also like to thank the Radio Unit Team at Ericsson Lindholmen for sharing their technical expertise and for letting us use their office space.

Johannes Broberg & Kimon Sfiris  
Gothenburg June 18, 2015





# Contents

<b>Abstract</b>	<b>v</b>
<b>Acknowledgements</b>	<b>vii</b>
<b>Contents</b>	<b>ix</b>
<b>Symbols and Glossary</b>	<b>xiii</b>
<b>Abbreviations</b>	<b>xv</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Problem Background . . . . .	1
1.2 Purpose of the Thesis . . . . .	2
1.3 Delimitations . . . . .	2
<b>2 Technical Background</b>	<b>3</b>
2.1 Buck Converter . . . . .	3
2.2 Charge-Pump Buck Converter . . . . .	5
2.3 Switched Inductor Buck Converter . . . . .	6
2.4 Tapped Inductor Buck Converter . . . . .	9
2.5 Three Level Buck Converter . . . . .	11
2.6 Single-Ended Primary-Inductor Converter . . . . .	12
2.7 SEPIC fed Buck Converter . . . . .	14
<b>3 Circuit design</b>	<b>17</b>
3.1 Basic Implementation Models . . . . .	18
3.1.1 Standard Buck Converter design . . . . .	18
3.1.2 Charge-Pump Buck Converter design . . . . .	20
3.1.3 Switched Inductor Buck Converter design . . . . .	21

---

3.1.4	Tapped Inductor Buck Converter design . . . . .	23
3.1.5	Three Level Buck Converter design . . . . .	25
3.1.6	SEPIC fed Buck Converter design . . . . .	27
<b>4</b>	<b>Selection of Components</b>	<b>29</b>
4.1	Switches . . . . .	29
4.2	Inductors . . . . .	30
4.3	Capacitance . . . . .	30
4.4	Diodes . . . . .	31
4.5	Drive Circuit . . . . .	31
<b>5</b>	<b>Verification of Simulation Model</b>	<b>35</b>
<b>6</b>	<b>Results</b>	<b>37</b>
6.1	Implementation models . . . . .	37
6.1.1	Standard Buck Converter . . . . .	37
6.1.2	Switched Inductor Buck Converter . . . . .	40
6.1.3	Tapped Inductor Buck Converter . . . . .	43
6.1.4	Three Level Buck Converter . . . . .	46
6.1.5	SEPIC fed Buck Converter . . . . .	49
6.1.6	Load dependence . . . . .	52
<b>7</b>	<b>Discussion</b>	<b>55</b>
7.1	Pros and Cons with Different Topologies . . . . .	55
7.1.1	Standard Buck Converter . . . . .	55
7.1.2	Switched Inductor Buck Converter . . . . .	56
7.1.3	Tapped Inductor Buck Converter . . . . .	56
7.1.4	Three Level Buck Converter . . . . .	57
7.1.5	SEPIC fed Buck Converter . . . . .	57
7.2	Efficiency . . . . .	58
7.3	Size Comparison . . . . .	59
7.4	Cost Discussion . . . . .	60
<b>8</b>	<b>Future work</b>	<b>63</b>
8.1	Transient response . . . . .	63
8.2	Control Circuit . . . . .	63
8.3	Inductor verification . . . . .	64
8.4	Prototype verification . . . . .	64
8.5	Gate-Charge extraction . . . . .	64
<b>9</b>	<b>Conclusions</b>	<b>67</b>

<b>Bibliography</b>	<b>70</b>
<b>A LTspice schematics</b>	<b>A1</b>
A.1 Standard Step Down Converter . . . . .	A1
A.2 Switched Inductor Buck Converter . . . . .	A2
A.3 Tapped Inductor Buck Converter . . . . .	A3
A.4 Three Level Buck Converter . . . . .	A4
A.5 SEPIC fed Buck Converter . . . . .	A5



# Symbols and Glossary

$C$	Capacitance.
$D$	Duty Cycle.
$I_{in}$	Input Current.
$I_{out}$	Output Current.
$K$	Coupling Coefficient.
$L$	Inductance.
$P_{in}$	Input Power.
$P_{out}$	Output Power.
$Q_g$	Gate Charge.
$R_{DC}$	DC Resistance.
$R_{DS(on)}$	Conduction Resistance.
$T_{sw}$	Switch Time Period.
$V_{in}$	Input Voltage.
$V_{out}$	Average Output Voltage.
$\Delta I_L$	Current Ripple in Inductance.
$\Delta V_{out}$	Output Voltage Ripple.
$\eta$	Efficiency.
$f_{sw}$	Frequency.
$n$	Turns Ratio.
$t_{off}$	Switch Off Duration.
$t_{on}$	Switch On Duration.
$v_{out}$	Output Voltage.



# Abbreviations

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
IC	Integrated Circuit
PCB	Printed Circuit Board
POL	Point of Load
RMS	Root Mean Square
RRU	Remote Radio Unit
SEPIC	Single-Ended Primary-Inductor Converter





# 1

## Introduction

### 1.1 Problem Background

Electric power production is seldom at the same location as the load and as a result power needs to be distributed from the source to the load. Transmission from the source to the load is usually done with high voltage to minimize the conduction losses. The voltage is stepped up at the source and then gradually stepped down closer to the load. This principle is the same both for electric grids and for power distribution on circuit boards. Different consumers on a circuit board have different demands on the power supply. To meet these demands, power converters that convert the power to meet the specified demands are needed. Today these power converters normally consist of switched power electronics that can be designed with transformers. However the use of transformers increase cost, volume and losses [1], instead non-isolated converters are preferred where electrical isolation is not needed. The standard step down DC/DC converter, or buck converter, has a limited voltage conversion ratio and the efficiency decreases significantly for large ratios [2]. There are a number of articles suggesting modifications to the standard buck converter topology in order to increase its voltage conversion capacity [3, 4, 5, 6, 7]. These topologies increase the number of components and complexity of the converter which needs to be weighed against other factors such as increased efficiency, decrease in size and improvement in transient response if implemented in a real product.

## 1.2 Purpose of the Thesis

The purpose of this thesis is to investigate how the topology of a standard buck converter can be modified to match high demands on voltage conversion ratio and efficiency without a considerable increase in footprint size. The aim is to contribute with knowledge regarding characteristics, advantages and drawbacks of the investigated topologies.

## 1.3 Delimitations

This thesis will investigate different step-down DC/DC converter topologies. The evaluation will be based on the criteria efficiency, footprint size and cost. To evaluate how the topology affects the criteria mentioned, other affecting parameters will be as similar as possible in the evaluated topologies. The design will be based on the specifications of a conversion block for a Remote Radio Unit, RRU, system. The following limitations are set:

- Advances in component technology and comparisons between different components such as switches, inductors and capacitors will not be done.
- The results will be based on simulations. The results will not be verified in practice, i.e. no prototypes will be made.
- The simulation will only be in continuous conduction mode, CCM, which means that discontinuous conduction mode, DCM, will not be investigated.
- To reduce complexity and focus the evaluation on characteristics dependent on topology, the converter control circuit is considered to be out of the scope. As a result of this, the simulations will be done as open-loop without control and the transient response will not be evaluated.
- Drive circuits will not be investigated, a simple drive circuit based on a few assumptions will be used.
- Input capacitors will not be investigated. The voltage source in the simulations will be ideal without source impedance and input capacitors will not be needed in the simulations.

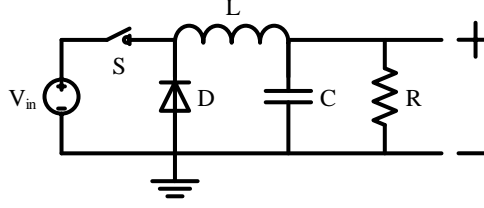
# 2

## Technical Background

Industries such as automotive and telecommunication all require the DC/DC converter to operate with a high input and low output voltage with various loads, causing a high demand on the voltage conversion ratio. Loads such as microprocessors requires low voltages and high currents [8] which give high conversion ratios in the Point of Load, POL. Converters are needed to minimize the losses and increase the efficiency by decreasing the bus current. High voltage conversion ratio results in a low duty cycle in order to convert the high voltage to the demanded low voltage in a POL. When the duty cycle decreases, the stresses on the components increases due to the short on- and off times causing high currents during short times. A conversion ratio below 0.1 – 0.15 is considered impractical due to the increase in losses depending on the high current. A low duty cycle also result in switching problems caused by MOSFETs rise and fall times [2]. Theory describing different topologies of a buck converter that addresses these disadvantages will be discussed in this section.

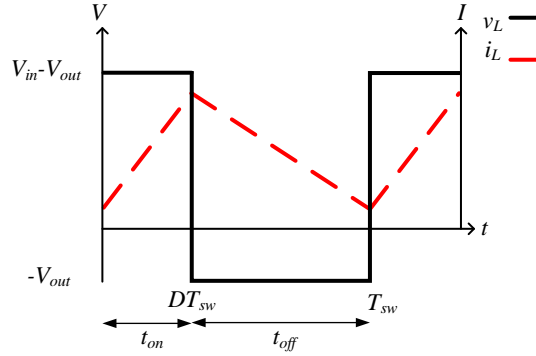
### 2.1 Buck Converter

A buck converter, or a standard step down converter, is a DC/DC converter used to decrease DC voltage. A schematic of a buck converter can be seen in Figure 2.1 and consists of one switch, one diode, one capacitor and one inductor.



**Figure 2.1:** Standard Buck Converter circuit design

The buck converter either store energy in the inductor or discharge the stored energy to the load, which is done in two different phases. To store energy, the switch connects the input voltage to the inductor which results in a positive voltage over the inductor, this phase is called on-time,  $t_{on}$ . When the switch is disconnected, the positive side of the inductor is connected to the ground via a diode which results in a negative voltage over the inductor. The energy is then discharged from the inductor to the load, referred to as off-time,  $t_{off}$ , seen in Figure 2.2.



**Figure 2.2:** Inductor current and voltage of a Standard Buck Converter

The capacitor is used to decrease the fluctuations in output voltage caused by the inductor charge and discharge. The average output voltage,  $V_{out}$ , can be calculated as

$$V_{out} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_{out}(t) dt = \frac{t_{on}}{T_{sw}} V_{in} = DV_{in} \quad (2.1)$$

where  $T_{sw}$  is the switching time period,  $v_{out}$  is the output voltage and  $V_{in}$  is the input voltage. The on- and off-time for the switches can be calculated as

$$t_{on} = \frac{1}{f_{sw}} \cdot D \quad (2.2)$$

$$t_{off} = \frac{1}{f_{sw}} \cdot (1 - D) \quad (2.3)$$

where  $f_{sw}$  is the switching frequency. The total ripple current through the inductor,  $\Delta I_L$ , can be calculated as

$$\Delta I_L = \frac{V_{out}(1 - D)}{L f_{sw}} \quad (2.4)$$

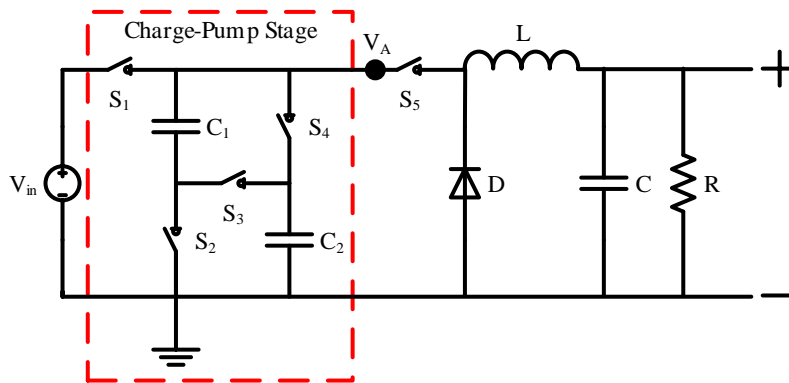
where  $L$  is the inductance. The output voltage ripple is determined by the output voltage capacitor,  $C$ . The needed capacitor can be calculated as

$$C = \frac{\Delta I_L}{8 \Delta V_{out} f_{sw}} \quad (2.5)$$

where  $\Delta V_{out}$  is the desired maximal output voltage ripple.

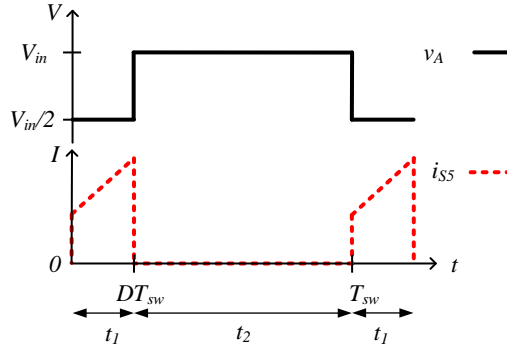
## 2.2 Charge-Pump Buck Converter

The charge-pump buck converter consists of a buck converter with a charge-pump stage in front [4], see Figure 2.3. A charge-pump stage consist of a minimum of two capacitors and four switches. By changing the connection in the charging and discharging phase, the capacitors can be charged in series and discharged in parallel which result in a output voltage from the charge-pump stage that is half the input voltage. As a result, the output voltage can be controlled with high efficiency [9].



**Figure 2.3:** Charge-Pump Buck Converter circuit diagram

In the charge phase ( $t_2$  in Figure 2.4) the switches  $S_1$  and  $S_3$  are closed and  $S_2$  and  $S_4$  are open. The input capacitors  $C_1$  and  $C_2$  are charged in series with a voltage across of  $V_{in}$ . In the discharge phase ( $t_1$  in Figure 2.4)  $S_1$  and  $S_3$  are open and  $S_2$  and  $S_4$  are closed.  $C_1$  and  $C_2$  are then discharged in parallel. Figure 2.4 shows the voltage from the charge-pump stage and the current through the high-side switch,  $S_5$ , of the buck stage. As Figure 2.4 shows, the voltage over the switch,  $V_A$ , when the switch is closed and the current passes through is half of the input voltage. This is the voltage that is seen by the buck stage of the converter and is equal to  $V_{in}/2$ .

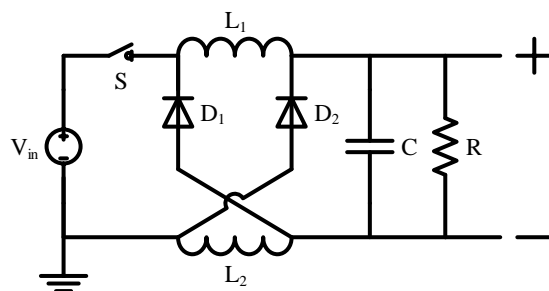


**Figure 2.4:** Current and voltage seen by the buck stage in the Charge-Pump Buck Converter

The capacitance value, inductance values and duty cycle can be calculated with the same equations as for the buck converter in Section 2.1 but with  $V_{in}$  replaced by  $V_{in}/2$ .

## 2.3 Switched Inductor Buck Converter

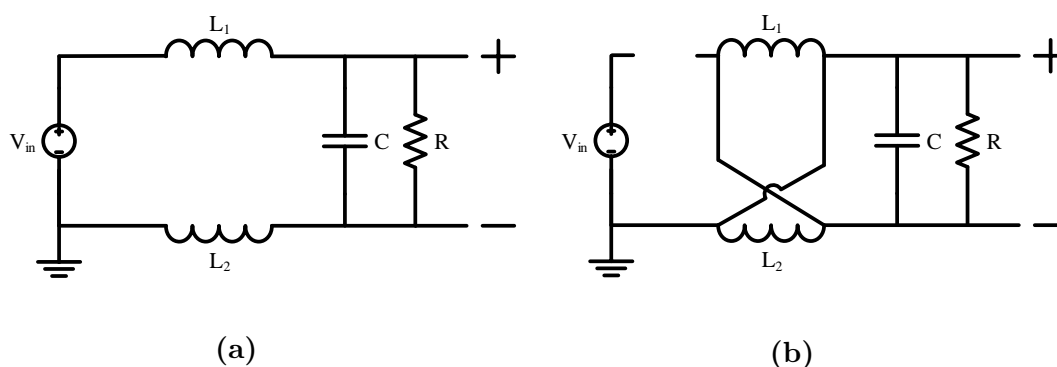
The switched inductor buck converter uses switches to change the configuration of two inductors between series and parallel connections, see Figure 2.5. In this way it is possible to change the inductance in the converter.



**Figure 2.5:** Switched Inductor Buck Converter circuit design

By changing the connection in the charging and discharging phase, the inductors can be charged in series and discharged in parallel [3]. As a result, there will be a different inductance during the charge and discharge phase. The series connected inductors will result in a increased inductance during the charge phase as seen in Figure 2.6a. The increased inductance means that a longer time is needed to charge the inductors. The parallel discharge seen in Figure 2.6b will provide a lower inductance resulting in a faster discharge compared to the buck converter. The duty cycle will be longer for the same conversion ratio and an analysis of the circuit results in a duty cycle defined as

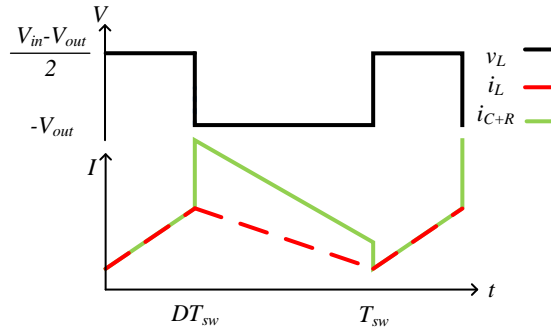
$$D = \frac{2V_{out}}{V_{out} + V_{in}}. \quad (2.6)$$



**Figure 2.6:** Charging (a) and discharging (b) state for a Switched Inductor Buck Converter

The output current alternates between the current from the inductors in series and

in parallel. When the inductors are switched to parallel connection, the output current is doubled and when they are switched back to series connection the output current also switches back. This results in a very large output current ripple as seen in Figure 2.7. The output capacitor needs to store the excess energy when the current is above the average current and release energy when it is below. The current through an inductor does not change instantaneously and as a result the current will continue to flow through the inductor even during the short time interval between  $t_{on}$  and  $t_{off}$  when the inductor is connected to a floating potential resulting in a voltage spike in the floating node. To limit the voltage spike, diodes, snubbers or clamping circuits can be used. The diode have a forward voltage drop which results in losses during overvoltages. Snubbers and clamp circuits instead store the voltage-spike energy temporary and reuse it later which decreases the losses.



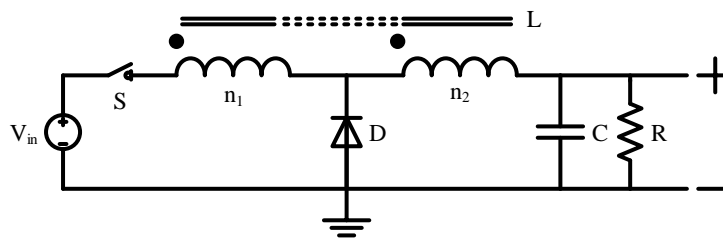
**Figure 2.7:** Inductor current and voltage of a Switched Inductor Buck Converter

The switched inductor converter utilize two inductors and inductors tend to be one of the largest components in a converter. The use of several discrete inductors would result in a significant increase in size compared to the buck converter topology. A way to solve this is to use coupled inductors. A coupled inductor consist of two inductor windings on the same core. Since the windings are wound on top of each other, the resulting footprint for two coupled inductances is typically the same as one standard inductor with the same inductance. However, the height for a coupled inductor is typically higher [10]. Since the windings are wound on top of each other, they share the same magnetic flux which creates a mutual inductance between them. As a result the inductance when the inductors are connected in series is due to the mutual inductance more than twice the rated inductance. The use of coupled inductors can significantly reduce cost and footprint size of converter circuits with multiple inductors [11].



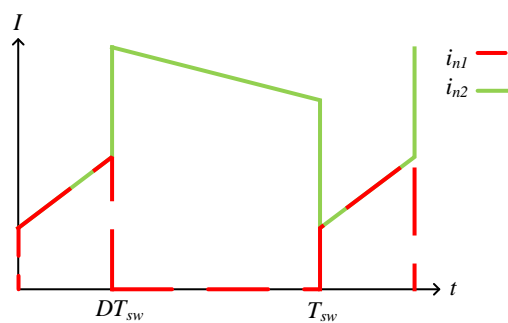
## 2.4 Tapped Inductor Buck Converter

The tapped inductor buck converter works in a similar way as the switched inductor converter and utilizes a different inductance during the charge and discharge phases. The basic topology can be seen in Figure 2.8.



**Figure 2.8:** Tapped Inductor Buck Converter circuit design

Instead of two inductors, the tapped inductor converter uses one tapped inductor. The tapped inductor is an inductor with a tap along the inductor winding which creates a second connection point and two windings,  $n_1$  and  $n_2$ , wound on the same core. In this way, another connection point with a different inductance is created. During charge both windings are charged in series whilst during discharge only winding  $n_1$  is connected in parallel to the load. Therefore there will be a very large current ripple which can be seen in Figure 2.9.



**Figure 2.9:** Inductor currents in Tapped Inductor Buck Converter

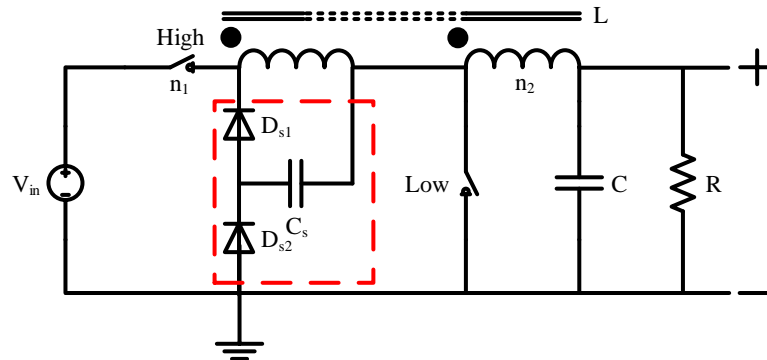
The turns ratio,  $n$ , between the windings is defined as

$$n = \frac{(n_1 + n_2)}{n_1}. \quad (2.7)$$

For a buck converter,  $n$  should always be greater than 1 [5]. This results in a ratio between the charging and discharging inductance that can be selected in the design phase. The voltage drop over each inductor during the charging phase will be proportional to the winding ratio which results in a duty cycle that equals to

$$D = \frac{n V_{out}}{V_{in} + (n - 1) V_{out}}. \quad (2.8)$$

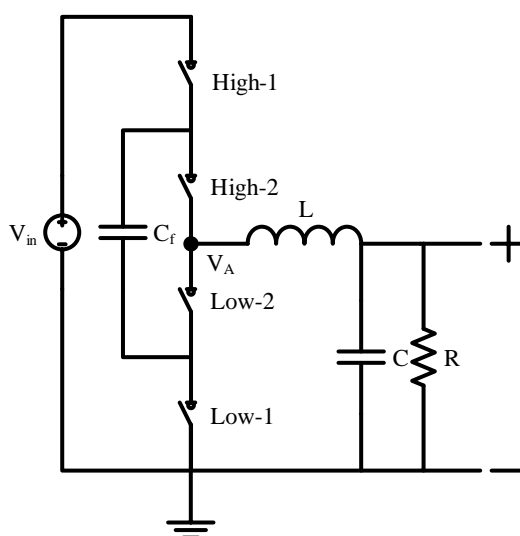
Winding  $n_1$  needs to completely discharge through  $n_2$  to avoid a voltage spike across the high-side switch. This requires perfect coupling between the windings. In real circuits the coupling is not exactly 1 which results in leakage inductance. The leakage inductance will cause a voltage-spike in the node between the inductance and the switch which can be handled with a clamping circuit, see Figure 2.10 [5]. Instead of charging the small drain-source capacitance of the switch, the leakage current from the inductor will flow through diode  $D_{s1}$  and the clamping capacitance,  $C_s$ . When the switch opens the energy will be released back through  $C_s$  and  $D_{s2}$ . If the clamping capacitance is sufficiently large, the voltage spike can be reduced significantly.



**Figure 2.10:** Clamping Circuit in Tapped Inductor Buck Converter

## 2.5 Three Level Buck Converter

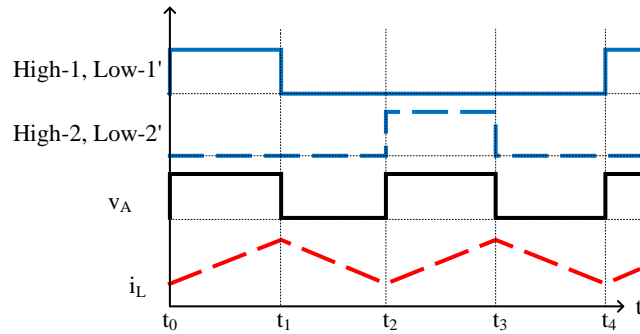
The three level buck converter was originally designed for high power applications but have later on been more and more used in a larger range of applications. The three level buck converter offers high efficiency and high power density [6]. The first stage of the converter is built up by four switches and one flying capacitor,  $C_f$ , see Figure 2.11.



**Figure 2.11:** Three Level Buck Converter circuit diagram

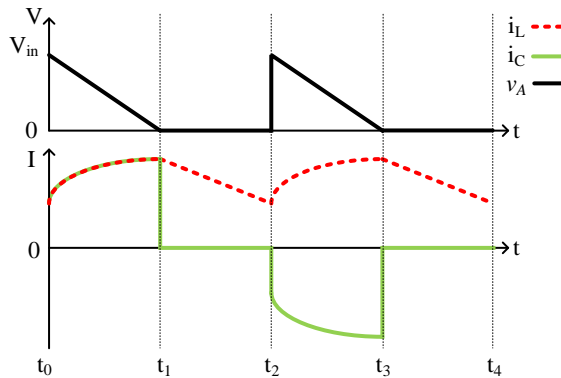
The operation of the three level buck converter can be divided into four different operation phases ( $t_0$  to  $t_4$ ), see figure 2.12

- During the first phase ( $t_0-t_1$ ) *High* – 1 and *Low* – 2 are conducting which will charge the flying capacitor,  $C_f$ , and deliver power to the load. This results in an average voltage in  $v_A$  of  $V_{in}/2$  during the first phase.
- In the second phase ( $t_1-t_2$ ) *Low* – 1 and *Low* – 2 are conducting.  $v_A$  is connected to ground and the current will freewheel in the circuit.
- In the third phase ( $t_2-t_3$ ) *High* – 2 and *Low* – 1 are conducting. The flying capacitor is discharged and power is delivered to the load. The load sees the voltage  $V_{in}/2$ .
- The last phase ( $t_3-t_4$ ) is the same as the second phase and the current free-wheels through the circuit.



**Figure 2.12:** Control voltages, inductor current and voltage in the Three Level Buck Converter

The topology is capable of producing different voltages in  $v_A$  depending on the duty cycle. The duty cycle calculation is the same as for the buck converter and can be calculated as (2.1). With a duty cycle less than 0.5, the voltage in  $v_A$  is  $0V$  or  $V_{in}/2$ . With a duty cycle greater than 0.5,  $v_A$  can be  $V_{in}/2$  or  $V_{in}$  instead. Due to the scope of the thesis focus will further on be on duty cycles of less than 0.5. Capacitor current, inductor current and  $v_A$  node voltage can be seen in Figure 2.13 for the different phases.

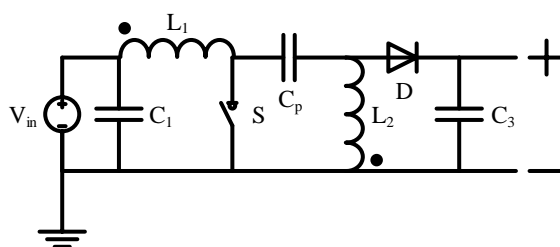


**Figure 2.13:** Charging and discharging in Three Level Buck Converter

## 2.6 Single-Ended Primary-Inductor Converter

The Single-Ended Primary-Inductor Converter, SEPIC, can be described as a boost converter followed by a buck-boost converter, see Figure 2.14. The converter consist of two inductors, one switch, one diode, one coupling capacitor and

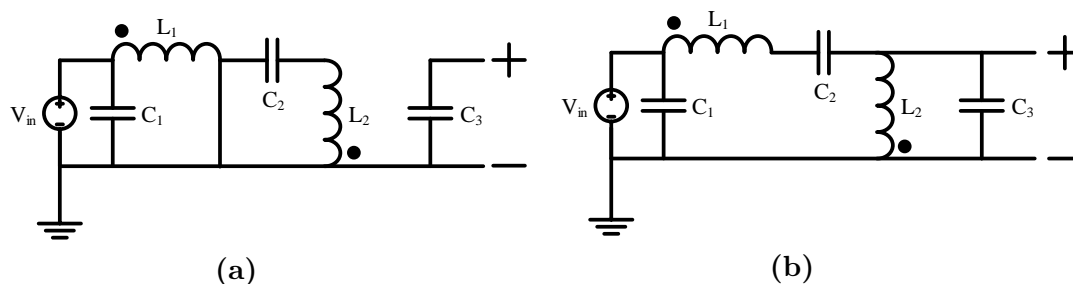
one output capacitor. The voltage over the coupling capacitor,  $C_p$ , will be an average voltage of  $V_{in}$  and with a large capacitor it will be close to constant.  $C_p$  prevents any DC current from flowing between the high- and low-voltage side and it also enables the output voltage to be lower than the input voltage. Without  $C_p$ , the diode would be forward biased and nothing would prevent a current flowing from  $V_{in}$  to  $V_{out}$  when  $V_{in} > V_{out}$ . The diode needs to be connected to a known potential; this is accomplished with the second inductance,  $L_2$ , which connects the diode to ground [12].



**Figure 2.14:** SEPIC circuit diagram

In the first phase, during on-time, the inductance  $L_1$  has a constant voltage of  $V_{in}$  applied and energy is stored in the inductor, see Figure 2.15a. Since the high-voltage side of  $C_p$  is connected to ground via the conducting switch, the low-voltage side will be kept at  $-V_{in}$ . The voltage over the second inductance,  $L_2$ , which is connected between the low-voltage side of  $C_p$  and ground will be  $-V_{in}$ . This makes the diode reverse biased and as a result,  $L_2$  will be charged by  $C_p$ .

During the switch off-time,  $L_1$  charged  $C_p$  and  $L_2$  which are in parallel with the load, see Figure 2.15b. The voltage over  $L_2$  will then become equal  $V_{out}$  which makes the diode forward biased and conducting,  $L_2$  then supplies energy to the load through the diode [11].



**Figure 2.15:** Charging (a) and discharging (b) state for a SEPIC

The duty cycle for the converter is defined as

$$D = \frac{V_{out}}{V_{in} + V_{out}}. \quad (2.9)$$

The inductance needed to limit the current ripple to  $\Delta I_L$  can be calculated as

$$L_1 = L_2 = \frac{1}{2} \frac{V_{in} D}{\Delta I_L f_{sw}}. \quad (2.10)$$

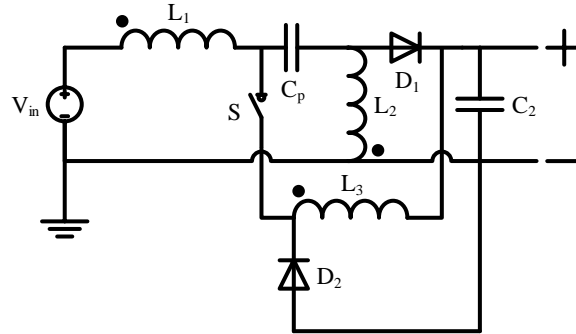
The voltage ripple,  $\Delta V_{C_p}$ , over  $C_p$  contributes to the RMS current in the capacitor resulting in losses.  $C_p$  can be chosen to limit  $V_{C_p}$  according to

$$\Delta V_{C_p} = \frac{I_{out} D}{C_p f_{sw}} \quad (2.11)$$

The main usage area of a SEPIC is applications where the output voltage overlap the specified range for the input voltage. The increased availability of coupled inductors have significantly reduced the footprint size for SEPIC circuits which previously has been one of the major factors preventing a wider use [10].

## 2.7 SEPIC fed Buck Converter

The SEPIC fed buck converter is a topology aimed to improve efficiency and transient response of the buck converter whilst keeping the low cost and simplicity. The SEPIC fed buck converter solves these problems by creating multiple paths for the energy and it also reduces voltage stresses on the components. The converter consists of a SEPIC in parallel with a buck converter which creates an alternative path for the energy which reduces the conduction losses, see Figure 2.16 [7]. The buck converter section is connected to the SEPIC high-side switch, S, meaning that the SEPIC and buck converter share the switch.



**Figure 2.16:** SEPIC fed Buck Converter circuit diagram

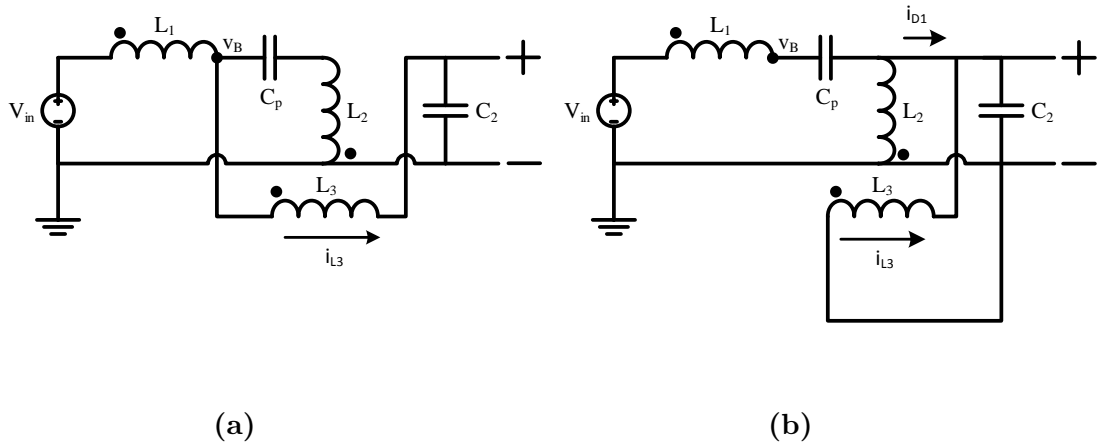
The converter operates in two phases, during the on-time seen in Figure 2.17a, the switch connects  $L_1$  to the high-side switch of the buck converter which creates a voltage division between  $L_1$  and  $L_3$ . The voltage over  $L_1$ ,  $C_p$  and  $L_2$  equals to  $V_{in}$ . Consequently, the voltage over  $L_2$  will have the same magnitude as the voltage over  $L_1$  and  $L_3$  but with negative polarity.

During the second phase, off-time seen in Figure 2.17b, the inductances  $L_2$  and  $L_3$  are discharged in parallel and  $L_1$  charges  $C_p$ . The duty cycle can be calculated as

$$D = \frac{2V_{out}}{V_{in} + V_{out}}. \quad (2.12)$$

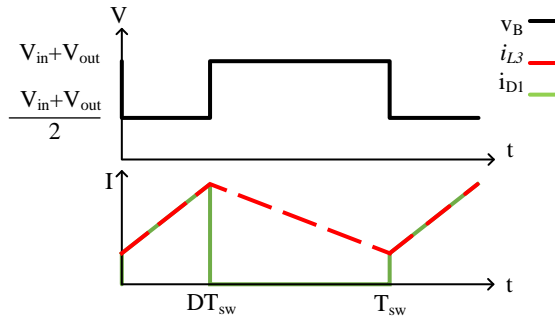
For simpler analysis of the ripple current, consider the inductors  $L_1$  and  $L_3$  to be connected in series during the switch on-time. The ripple current in  $L_3$  can then be calculated as

$$\Delta I_{L_3} = \frac{V_{in} - V_{out}}{(L_1 + L_3)f_{sw}} D. \quad (2.13)$$



**Figure 2.17:** Charging (a) and discharging (b) state of SEPIC fed Buck converter

The SEPIC section continuously draws current from the source but only supplies the load during the off-time while the buck converter section delivers energy to the load continuously. As a result, the output current prior to the output capacitor will contain a large ripple since the current will consist of both SEPIC and buck converter current during off-time and only buck converter current during on-time, see Figure 2.18. The output current from the converter will then have the same shape as the switched and tapped inductor converters.



**Figure 2.18:** Voltage at the buck connection point together with SEPIC and buck currents in a SEPIC fed Buck Converter



# 3

## Circuit design

This thesis is based on theoretical evaluations and comparisons of different DC/DC step-down converter topologies. The evaluation is based on results from LTspice simulations. The specification for the converters is presented in Table 3.1 and with the specification as a base, Section 3.1 describes component dimensioning for the different investigated topologies.

**Table 3.1:** Parameters for simulation application

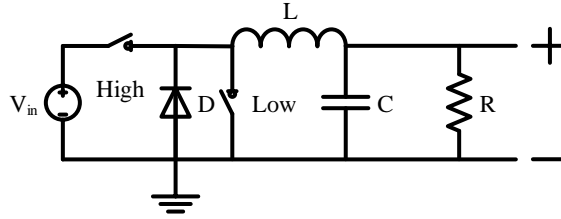
Parameter	Value
Nominal Input Voltage	55V
Nominal Output Voltage	5.2V
Nominal Output Current	10A
Maximum Output Current	17.2A
Maximum Inductor Current Ripple	30%
Nominal Output Voltage Ripple	50mV <sub>p-p</sub>
Switching Frequency	300kHz

In the end of each section tables with the required component ratings are presented. These ratings are based on the simulation data where switching transients are neglected. Since it is a close to ideal circuit there is no damping and default slew rate in the switches causes, in some cases, significant transients which will be attenuated in a real circuit.

## 3.1 Basic Implementation Models

### 3.1.1 Standard Buck Converter design

As mention in Section 2.1, the buck converter consists of one capacitor ( $C$ ), one inductor ( $L$ ), one diode and one switch. Figure 3.1 shows the synchronous buck converter which is implemented in LTspice. In the synchronous buck converter the freewheeling diode from the standard buck is replaced with a switch. A diode ( $D$ ) is also connected in parallel to reduce conduction losses in the MOSFET body diode. The switch which replaces the diode will be referred to as the low-side switch ( $Low$ ). The switch connected to the voltage source will be referred to as the high-side switch ( $High$ ).



**Figure 3.1:** Synchronous Buck converter as implemented in LTspice

To calculate the impedance values, the charging and discharging times are needed. These are dependent on the duty cycle and switching frequency of the high-side and low-side switch. The inductor needs to have time to charge and therefore the minimum on-time or minimum duty cycle together with switching frequency is critical when dimensioning the inductance. The duty cycle can be calculated from (2.1) as

$$D = \frac{V_{out}}{V_{in}} = \frac{5.2V}{55V} = 0.0945. \quad (3.1)$$

The inductance should limit the ripple current to the specified maximum current ripple,  $\Delta I_L$ , which normally is set 30% of the maximum current[13]. From (2.4) the inductance is calculated as

$$L = \frac{V_{out}(1 - D)}{\Delta I_L \cdot f_{sw}} = \frac{5.2V(1 - 0.0945)}{5.16A \cdot 300kHz} = 3.0\mu H. \quad (3.2)$$

The output capacitor should limit the nominal output voltage ripple. To achieve this, the excess energy transferred from the inductance during the charging phase needs to be stored in the capacitor. (2.5) defines the needed capacitance as

$$C = \frac{\Delta I_L}{8\Delta V_{out} \cdot f_{sw}} = \frac{5.16A}{8 \cdot 50mV \cdot 300kHz} = 43\mu F. \quad (3.3)$$

These values are used as initial values in the LTspice simulations. LTspice is not fully ideal which results in that some small tuning needs to be done to match the specification in Table 3.1. The non-ideal part in LTspice is the predefined values for series resistance in capacitors and inductors and voltage drop over the diodes. The resulting component values that meets the specified demands are shown in Table 3.2 and compared with the calculated values.

**Table 3.2:** Duty cycle and component values for the implemented Standard Buck Converter

	Calculated	Tuned
Duty Cycle	0.0945	0.1020
Inductance, $L$	$3.0\mu H$	$3.1 \mu H$
Capacitance, $C$	$43\mu F$	$50 \mu F$

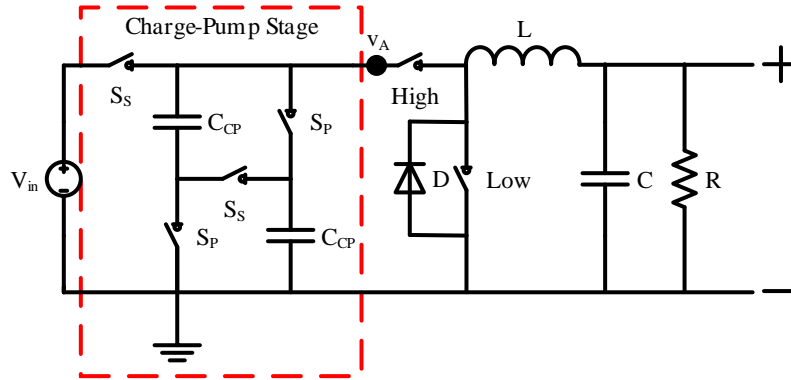
To be able to choose the most suitable components for real circuit investigation the limitations of different components needs to be investigated. The important parameters that needs to be investigated for the basic model to ensure that the correct components are selected is the RMS- and peak- currents and also the peak voltage. The components needs to be rated to handle the current and voltage stress that they are subjected to. The RMS current through the different component, peak current and peak voltage are extracted from LTspice and presented in Table 3.3.

**Table 3.3:** Maximal component stress for Standard Buck Converter components

	RMS Current	Max Voltage
Inductor, $L$	17.3 A	49.8 V
Capacitor, $C$	1.47 A	5.20 V
High-side Switch	5.34 A	55.0 V
Low-side Switch	16.4 A	55.0 V

### 3.1.2 Charge-Pump Buck Converter design

The same parameters as in Section 3.1.1 needs to be calculated in the same way as in Section 2.2 for the charge-pump buck converter. The calculation procedure is the same except for the input voltage in (2.1) which should be the nominal input voltage divided by two,  $V_{in}/2$ , due to the charge-pump stage. Figure 3.2 shows the implemented model of the charge-pump converter with high-side switch (*High*), Low-side switch (*Low*) in parallel with the diode (*D*). In the charge-pump stage, the series switches ( $S_S$ ) and parallel switches ( $S_P$ ) conducts in pairs together with the input capacitors ( $C_{cp}$ ).



**Figure 3.2:** Charge-Pump Buck Converter circuit as implemented in LTspice

The resulting values that meets the demands in Table 3.1 are shown in Table 3.4 together with the tuned values from LTspice. The tuning is needed due to non-ideal parameters in the simulation program.

**Table 3.4:** Duty cycle and component values for Charge-Pump Buck Converter

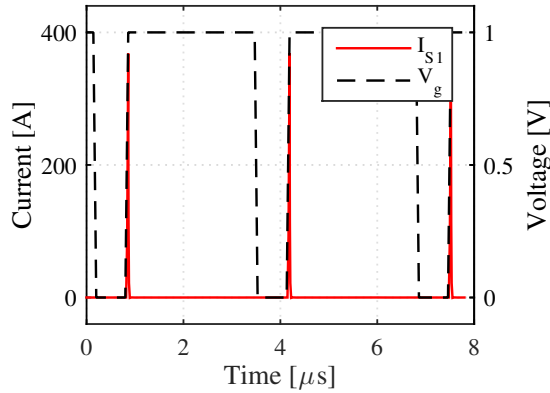
	Calculated	Tuned
Duty Cycle	0.1891	0.1802
Inductance, $L$	$2.7\mu H$	$3.1\mu H$
Capacitance, $C$	$29\mu F$	$28\mu F$

The RMS current, peak current and peak voltage in the different components are presented in Table 3.5. These limiting parameters are extracted from LTspice.

**Table 3.5:** Maximal component stress for Charge-Pump Buck Converter components

	<b>RMS Current</b>	<b>Max Voltage</b>
Inductor, $L$	17.3 A	22.3 V
Capacitor, $C$	1.36 A	5.26 V
High-side Switch	7.58 A	55.9 V
Low-side Switch	15.5 A	27.5 V
Diode	1.42 A	27.5 V
Series Switches $S_S$	18.9 A	37.0 V
Parallel Switches $S_P$	3.80 A	27.5 V
Charge-Pump Capacitors $C_{CP}$	19.3 A	27.5 V

As seen in the Table 3.5 and Figure 3.3, there will be high currents in both the series switches and in the charge-pump capacitors. The capacitors charges in series and for ideal capacitors, there will be a short circuit when the capacitors are connected in series before they are charged. This initial short circuit will cause the current spikes seen in the Table 3.5. This will be damped in a real circuit where the PCB traces are slightly inductive and the capacitors will have internal resistance. However it is still considered to be a problematic circuit and will therefore not be evaluated further.

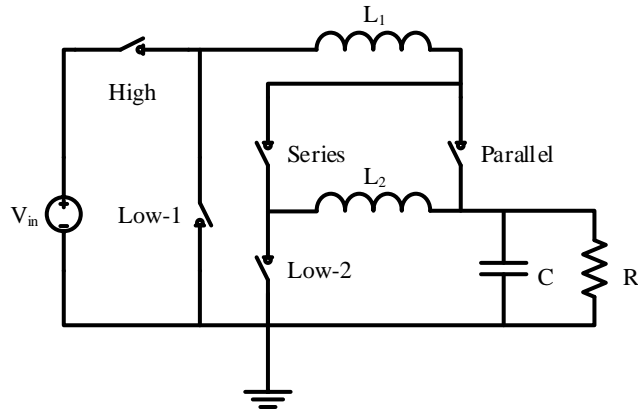
**Figure 3.3:** Current through and the gate control voltage for switch  $S_S$  in the Charge-Pump Buck Converter

### 3.1.3 Switched Inductor Buck Converter design

To reduce the converter size, coupled inductors as described in Section 2.3 are used for the switched inductor buck converter. The coupling coefficient,  $K$ , is set to 95% which is a common coupling coefficient[10]. In the circuit described in Section

2.3 it is not possible to connect the negative side of both the supply and the load to ground. Instead, both inductors are connected prior to the load and two low-side switches are used together with two switches which change the connection between series and parallel, see Figure 3.4. The switches *Low - 1* and *Low - 2* are the low-side switches used for freewheeling and the switches *Series* and *Parallel* are used to switch between series and parallel connection.  $D$  is calculated according to (2.6) as

$$D = \frac{2V_{out}}{V_{out} + V_{in}} = \frac{2 \cdot 5.2V}{55V + 5.2V} = 0.1728. \quad (3.4)$$



**Figure 3.4:** Switched Inductor Buck Converter circuit as implemented in LTspice

The switch between parallel and series connection results in a large output current ripple. When the inductor connection is switched from series to parallel, the output current will be doubled and when the connection, is switched back to series connection the output current will be reduced again. This means that it is not possible to limit the ripple to the desired 30%, instead the ripple during one phase is limited to 30%. The needed inductance and capacitance is found through simulations and the values are presented in Table 3.6.

**Table 3.6:** Duty cycle and component values for Switched Inductor Buck converter with 95% coupling

	Calculated	Tuned
Duty Cycle	0.1728	0.166
Inductance, $L$	n/a	$2.9\mu H$
Capacitance, $C$	n/a	$67\mu H$

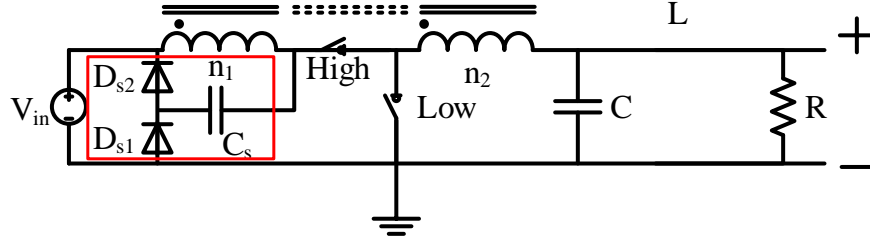
As in previous sections the current and voltage stresses that the components are subjected to have been extracted from the LTspice simulations. The maximal stresses forms the needed component ratings which are presented in Table 3.7

**Table 3.7:** Maximal component stress for Switched Inductor Buck Converter components with 95% coupling

	RMS Current	Max Voltage
Inductor, $L_1$	7.36 A	55.8 V
Inductor, $L_2$	11.7 A	24.9 V
Capacitor, $C_1$	3.85 A	5.23 V
High-side Switch	4.02 A	55.9 V
Low-side 1 Switch	6.26 A	55.0 V
Low-side 2 Switch	6.26 A	50.7 V
Series Switch	4.02 A	56.7 V
Parallel Switch	10.8 A	30.1 V

### 3.1.4 Tapped Inductor Buck Converter design

The tapped inductor buck converter can be implemented in several ways and in the circuit in Figure 2.8, the high-side switch is located prior to the windings in the tapped inductor. In this way, a negative voltage on the source of the high-side switch appears. This will also cause problems for the drive circuit since a change of source voltage will change the gate-source voltage which controls the MOSFETs. Instead is the circuit in Figure 3.5 implemented. By placing the high-side switch between the two inductor windings, the voltage spike due to the inductance in winding  $n_1$  will appear as a positive voltage spike on the drain instead. The clamp circuit described in Section 2.4 is then used to clamp the voltage spike. The clamp capacitor is dimensioned to limit the drain to ground voltage in the high-side switch (*High*) to 60V and with spikes below 85V.



**Figure 3.5:** Tapped Inductor Buck Converter with clamp circuit as implemented in LTspice

The duty cycle can be calculated from (2.8) which is the same equation as (2.6) used for the standard buck converter when  $n$  equals 2. The resulting duty cycle for the tapped inductor buck converter when  $n = 2$  is then the same as the duty cycle for the switched inductor buck converter. The current ripple described in Section 3.1.3 also appears in the tapped inductor buck topology. Instead of a parallel discharge, the discharge of both windings are made in  $n_2$  where  $n_1$  discharges via the magnetic coupling. As a result, the output current will be significantly greater during the discharge phase. The clamp circuit described in Section 2.4 is used to limit the voltage spike at the high-side switch drain to  $85V$ . The losses and the size of the clamp circuit can be reduced with better coupling but better coupling also results in larger output current ripple. The coupling used for the simulations is 95% and to limit the voltage spike on the *High* drain to  $85V$  the the clamping capacitor,  $C_s$ , was found to be  $50nF$ . Table 3.8 presents the design parameters used.

**Table 3.8:** Duty cycle and component values for Tapped Inductor Buck Converter with 95% coupling

	Calculated	Tuned
Duty Cycle	0.1728	0.171
Inductance, $L$	n/a	$2.6\mu H$
Capacitance, $C$	n/a	$87\mu F$
Clamping Cap, $C_s$	n/a	$50nF$

The needed ratings for all the components used in the converter are extracted from LTspice and the results are presented in Table 3.9.

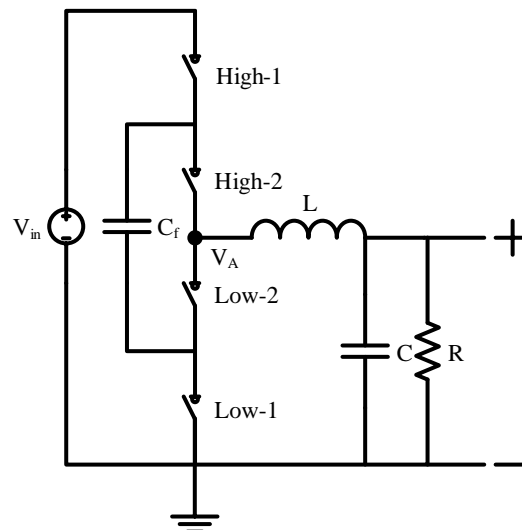


**Table 3.9:** Maximal component stress for Tapped Inductor Buck Converter components with 95% coupling

	RMS Current	Max Voltage
Inductor, $L_1$	4.25 A	36.7 V
Inductor, $L_2$	17.6 A	37.9 V
Capacitor, $C_1$	3.65 A	5.23 V
High-side Switch	4.53 A	37.4 V
Low-side Switch	17.0 A	40.1 V
Clamping Cap, $C_s$	2.15 A	33.5 V

### 3.1.5 Three Level Buck Converter design

The three level buck converter consists of two sets of switches working in parallel causing the effective switching frequency to be doubled and the average voltage over the inductance to be half the input voltage. With double switching frequency, the size of the inductor can be reduced and the total footprint of the converter reduced [6]. The duty cycle for the three level buck converter is calculated in the same way as for the standard buck converter and can therefore be calculated as (2.1) [6]. The circuit can be seen in Figure 3.6.

**Figure 3.6:** Three Level Buck Converter circuit as implemented in LTspice

By reducing the the voltage across the inductance, the current ripple for a fixed inductance will be reduced. For a fixed current ripple, the inductance can instead

be reduced which results in smaller size. The magnetic size is an important role in the total footprint size of the converter. The inductance with a duty cycle less than 0.5 can be calculated as

$$L = \frac{V_{out}(0.5 - D)}{\Delta I_L f_{sw}} = \frac{5.2V(0.5 - 0.0945)}{5.16A \cdot 300kHz} = 1.4\mu H. \quad (3.5)$$

With double effective switching frequency the capacitance can be calculated as

$$C = \frac{\Delta I_L}{8\Delta V_0 2f_{sw}} = \frac{5.16A}{16 \cdot 50mV \cdot 300kHz} = 22\mu F. \quad (3.6)$$

To calculate the needed capacitance value of the flying capacitance, the voltage ripple over the flying capacitors is set to the same value as the predefined value for the output voltage, seen in Table 3.1. The capacitance value can be calculated as:

$$C_f = \frac{DI_0}{\Delta V_{C_f} f_{sw}} = \frac{0.0945 \cdot 10A}{50mV \cdot 300kHz} = 63\mu F. \quad (3.7)$$

These theoretically calculated values are used as initial values and are tuned using LTspice simulations. The resulting values that meets the demands in Table 3.1 are shown in Table 3.10 and compared with the calculated values based on a switching frequency of 300kHz.

**Table 3.10:** Duty cycle and component values for Three Level Buck Converter

	Calculated	Tuned
Duty Cycle	0.0945	0.0945
Inductance, $L$	1.4 $\mu$ H	1.4 $\mu$ H
Capacitance, $C$	22 $\mu$ F	14 $\mu$ F
Flying Cap, $C_f$	63 $\mu$ F	60 $\mu$ F

The components needs to be dimensioned to handle the current and voltage stresses they are subjected to. These limiting stresses are extracted from LTspice and presented in Table 3.11.

**Table 3.11:** Maximal component stress for Three Level Buck Converter components

	RMS Current	Max Voltage
Inductor, $L$	17.4 A	49.6 V
Capacitor, $C$	2.03 A	5.32 V
High-side Switches	5.57 A	56.6 V
Low-side Switches	16.3 A	54.4 V
Flying Cap, $C_f$	7.93 A	55.9 V

### 3.1.6 SEPIC fed Buck Converter design

In the SEPIC fed buck converter, there is a SEPIC section and a buck section. The over all duty cycle for the converter is given by (2.12) which is the same as (2.6) and (2.8). (2.13) gives the minimum inductance needed to limit the current ripple in the inductors. With two inductors of equal inductance the required inductance can be calculated as

$$L = \frac{(V_{in} - V_{out})D}{2\Delta I_L f_{sw}} = \frac{(55V - 5.2V) \cdot 0.1728}{2 \cdot 5.16A \cdot 300kHz} = 2.8\mu H. \quad (3.8)$$

In the SEPIC converter (2.11) is used to calculate the size of the coupling capacitance which needs to store all energy from the input inductor. The capacitance in a SEPIC converter needs to be

$$C_p = \frac{I_{out}D}{\Delta V_{C_p} f_{sw}} = \frac{17.2A \cdot 0.1728}{50mV \cdot 55V \cdot 300kHz} = 3.1\mu F. \quad (3.9)$$

In the SEPIC fed buck converter energy is transferred both through the coupling capacitor and the buck inductor and as a result, the coupling capacitor can be smaller. The buck section provides a continuous current to the load and the SEPIC section delivers the current in pulses. As a consequence, the current prior to the output capacitor will have the same ripple shape as the current in the switched- and tapped inductor buck converters. The parameters for the converter are presented in Table 3.12.

**Table 3.12:** Duty cycle and component values for SEPIC fed Buck Converter

	Calculated	Tuned
Duty Cycle	0.1728	0.1946
Inductance, $L_1, L_2 \& L_3$	2.8 $\mu H$	2.1 $\mu H$
Capacitance, $C$	<i>n/a</i>	80 $\mu F$
Coupling Capacitor, $C_p$	3.1 $\mu H$	3.3 $\mu F$

The needed component ratings can be seen in Table 3.13. The ratings are based on the maximal stresses on the components.

**Table 3.13:** Maximal component stress for SEPIC fed Buck Converter components

	RMS Current	Max Voltage
Inductor, $L$	8.92 A	24.7 V
High-side Switch	5.37 A	61.6 V
Low-side Switch	7.31 A	30.5 V
SEPIC Switch	10.0 A	30.6 V
Capacitance, $C$	4.35 A	5.24 V
Coupling Capacitor, $C_p$	6.49 A	56.2 V

# 4

## Selection of Components

To be able to compare the different topologies as real circuits, the components need to be selected carefully in order to get a good setup that enables a fair comparison between the topologies. Components are selected based on the calculated minimum ratings in Section 2 which is based on the maximal load case in Table 3.1. Components where manufacturer models were not available were selected with parameters from a preferred component list which is made by Ericsson. This list is based on components used by Ericsson. The components which need to be selected are the switches, inductors, capacitors and diodes.

### 4.1 Switches

To make a fair comparison regarding losses and suitability in the circuit, it is important that the selected switches are selected to work well with the specific topology and still with a comparable overall performance. To achieve this, switches from the same manufacturer and from the same series have been selected. This is considered to provide enough freedom to make switch selections to optimize the losses and still have comparable solutions. The technology regarding MOSFETs has been improved significantly over the last years. To present results that represent a real optimized design as close as possible the most recent MOSFET series will be used. Complete LTspice simulation models can be downloaded from the manufacturers webpage and contain information of the component regarding losses and temperature increase. The choice has been to use Infineon MOSFETs since they provide good simulation models and the parameter that have been set are:

- Model – Infineon OptiMOS 5

- Package – SuperSO8
- $V_{DS}$  – 120% of Maximum voltage from ideal simulation

Infineon provides four different models of the same switch with different temperature dependence. Three are based on physical temperature dependence and one is based on empirical data which is faster to simulate but not that accurate. Due to simplicity, the selected model is one of the models based on physical temperature but without temperature input. The model will assume a constant temperature for the entire circuit and suits calculations for transient response, switching losses and efficiency calculations. When selecting MOSFETs within the specified set, the relationship between switching losses and conduction losses needs to be evaluated. Low conduction resistance,  $R_{DS(on)}$ , will result in more gate charge,  $Q_g$ , which is a measure of the energy needed to charge the capacitance in the MOSFET. A large  $Q_g$  results in longer switch times which in turn gives more switching losses.

## 4.2 Inductors

The inductors will be chosen with the focus on the calculated value in Section 3. Other important parameters are peak current and series resistance. The peak current is the current level at which the inductor core is saturated to a predefined level and the effective inductance decreases. To limit the possible options and still have enough freedom to choose inductors that fit the specific topology the decision was made to only choose inductors from the component list. The parameters of interest are:

- Inductance value - From calculations
- Peak current - From ideal simulations
- $R_{DC}$  - 120% of Value from Component List <sup>1</sup>

## 4.3 Capacitance

The capacitance will be selected with the same argument as the switches. To limit the possible options and get as fair result as possible, the decision was taken to use one manufacturer. This since all manufacturers have there own simulation models with different information which makes it hard to compare different simulation

---

<sup>1</sup>to account for the increase in  $R_{DC}$  caused by elevated temperatures

models from different manufacturers. The choice of manufacturer has been to use Murata and the chosen parameters of interest are:

- Housing – Ceramic Capacitors
- Series – GRM series
- Size – 3.2x1.6 (1206) <sup>2</sup>
- Tolerance –  $\pm 20\%$
- Temperature characteristics – X7R <sup>3</sup>

## 4.4 Diodes

The diode that will be used is chosen from the Component List, used by Ericsson, and are the same as in the predefined buck converter. The diode is a power schottky diode from ST Microelectronics which also is providing the simulation model. Parameters of interest are:

- Repetitive peak reverse voltage – 100V
- Average forward current – 6A
- Forward voltage drop – 0.64V

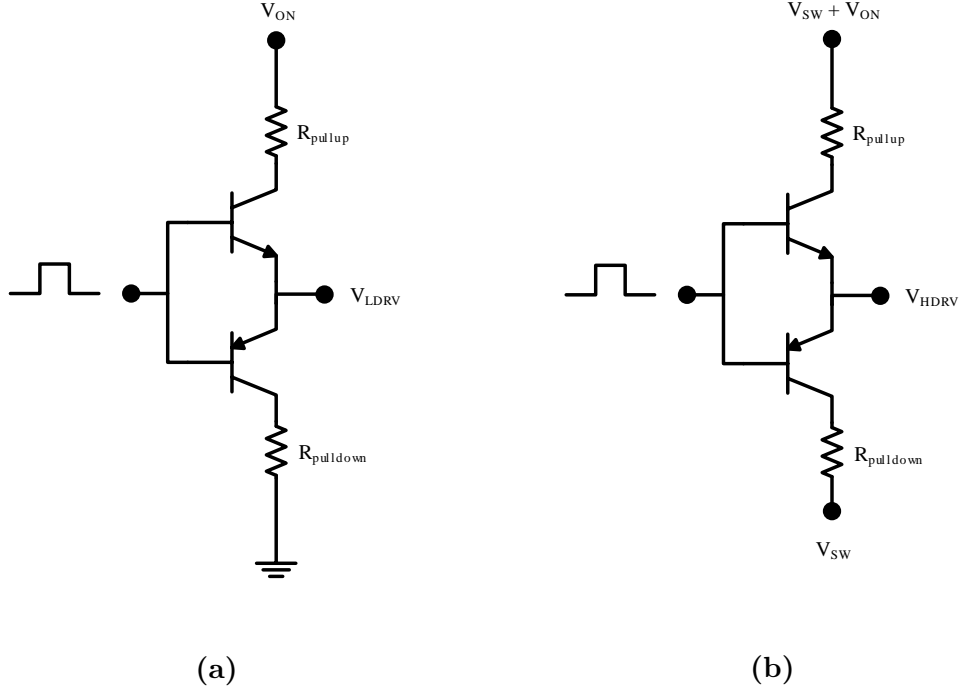
## 4.5 Drive Circuit

To obtain a fair representation of the switching losses it is important that the performance of the simulated drive circuit is comparable to a real drive circuit. To achieve this a simple totem pole drive circuit is implemented, see Figure 4.1.

---

<sup>2</sup>LxW in mm

<sup>3</sup>for use in applications up to 125C°



**Figure 4.1:** Drive circuits for the low-side MOSFETs (a) and high-side MOSFETs (b)

To get a circuit that resembles an actual drive circuit, values such as blanking times, drive voltages and resistor values are based on the Texas Instruments controller tps40170. The key parameters for the controller are extracted from the controller datasheet [14] and presented in Table 4.1.

**Table 4.1:** Typical drive circuit data from tps40170

Parameter	Value
High side driver pull up resistance	2.64 $\Omega$
High side driver pull down resistance	2.40 $\Omega$
Low side driver pull up resistance	2.40 $\Omega$
Low side driver pull down resistance	1.10 $\Omega$
Gate on voltage $V_{on}$	8V
Blanking time	60ns

The low-side driver is a simple circuit with two ideal switches which connects the low-side gate drive voltage,  $V_{LDRV}$ , to ground or the on-voltage depending on the control voltage. The high-side driver is implemented in the same way but



---

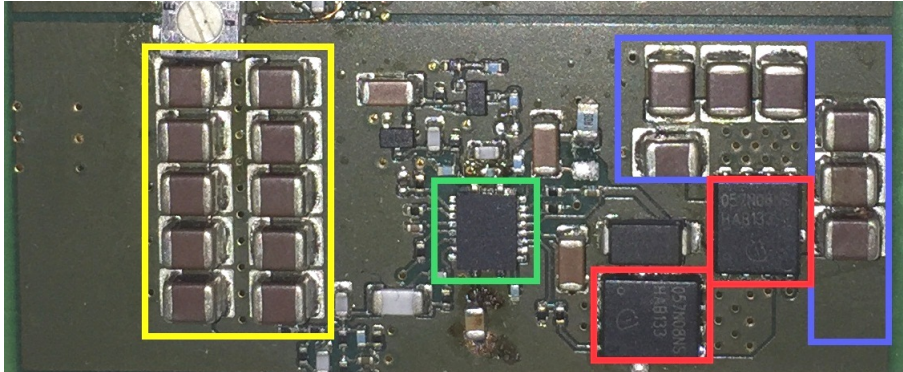
since the source of the MOSFET is connected to the switching node,  $V_{SW}$ , a zero gate-source voltage then results in a gate voltage of  $V_{SW}$ . The  $V_{HDRV}$  on-voltage needs to be  $V_{ON}$  above the voltage  $V_{SW}$ . During switch on-time,  $V_{SW}$  is equal to the input voltage. As a result the on-voltage for the high-side driver needs to be  $V_{ON} + V_{SW} = V_{ON} + V_{IN}$ . This means that the gate voltage needs to be higher than the input voltage. This can easily be implemented in LTspice but in a real application this is usually done with a bootstrap circuit. Bootstrap circuits are out of the scope for this thesis but a description of a bootstrap circuit can be found in [15].



# 5

## Verification of Simulation Model

To verify the simulation model in LTspice, a comparison between a real circuit and the LTspice simulation has been made. The real circuit, seen in Figure 5.1, is a standard buck converter.



**Figure 5.1:** Measurement circuit for a Standard Buck Converter

The real circuit uses Infineon MOSFETs both as high-side and low-side switches, marked with red. It has an inductor mounted on the backside of the circuit and the total output capacitance is  $940\mu F$ , marked with blue. The yellow segment on the PCB is the input capacitors and the green square marks the controller IC. The specifications of the buck converter can be seen in Table 5.1.

**Table 5.1:** Specifications of the measured Standard Buck Converter

<b>High-side switches</b>	<i>BSC057N08NS3</i>
<b>Low-side switches</b>	<i>BSC057N08NS3</i>
<b>Inductance</b>	<i>22<math>\mu</math>H</i>
<b>Series Resistance</b>	<i>27m<math>\Omega</math></i>
<b>Peak Current</b>	<i>26A</i>
<b>Output Capacitance</b>	<i>940<math>\mu</math>F</i>
<b>Input Capacitance</b>	<i>132<math>\mu</math>F</i>

The circuit implemented in LTspice is a simple synchronous buck converter with component values as defined in Table 5.1. Measurement data from measurements made previously on this circuit at Ericsson have been used for verification.

To compare the efficiency of the real circuit and the simulated, five different simulation were performed and analyzed against the measured values. The results can be seen in Table 5.2.

**Table 5.2:** Measurements V.S. Simulation results for Standard Buck Converter

	$V_{in}$ [V]	$I_{in}$ [A]	$P_{in}$ [W]	$V_{out}$ [V]	$I_{out}$ [A]	$P_{out}$ [W]	$\eta$ %
Measurements 1	35.2	0.5	17.8	17.0	0.98	16.7	<b>93.8</b>
Simulation 1	35.0	0.5	17.8	17.2	0.99	17.0	<b>95.7</b>
Measurements 2	35.1	1.0	35.1	17.0	1.99	33.8	<b>96.2</b>
Simulation 2	35.0	1.0	34.7	17.0	1.98	33.7	<b>97.4</b>
Measurements 3	35.0	1.5	52.5	17.0	2.99	50.9	<b>96.9</b>
Simulation 3	35.0	1.5	51.5	17.0	2.98	50.6	<b>98.3</b>
Measurements 4	34.9	2.0	69.7	17.0	3.98	67.7	<b>97.1</b>
Simulation 4	35.0	2.0	69.0	16.9	3.98	66.5	<b>97.5</b>
Measurements 5	34.8	2.5	87.1	17.0	4.98	84.7	<b>97.2</b>
Simulation 5	35.0	2.4	85.4	16.9	4.96	83.7	<b>98.0</b>

As seen in Table 5.2, the simulation model results are fairly close to the results from the real circuit. The simulation has higher efficiency in all five cases which can be explained by elements which is not included in the model, such as parasitics in the PCB and the controller. The measurements have also been performed with large external input and output capacitors and the losses in these are not included in the simulations. The results from this verification indicate that the assumptions made does not have a great impact on the results. It is also assumed that the assumptions made are valid for the other investigate topologies and the simulations alone can therefore be used as the only evaluation.

# 6

## Results

### 6.1 Implementation models

The results are based on simulations made with non-ideal component models from manufacturers or models based on data from manufacturers. The component values together with the maximal component stress presented in section 3.1 is used for selection of components. These components and component values are then used for initial simulations. The component values are then adjusted to ensure that the conditions specified in Table 3.1 still are met. In the cases where changes have been made these changes are specified for each topology. In the simulation there are several high frequent transients which will be dampened in a real system. To suppress these, a 3<sup>rd</sup> order butterworth filter have been used to filter the LTspice results in Matlab. The full schematics which is implemented in LTspice together with all components and drive circuits can be seen Appendix A.

#### 6.1.1 Standard Buck Converter

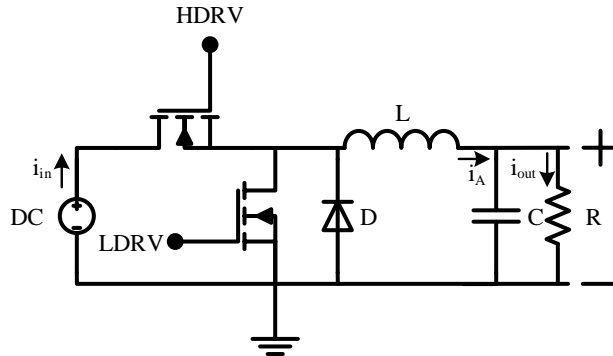
The final model of the buck converter can be seen in Figure 6.1. The signals LDRV and HDRV are the gate drive signals as described in Section 4.5. As a result of the parasitics introduced in the manufacturer models, more inductance and capacitance than what was suggested in Table 3.2 is needed. The values used can be seen in Table 6.1.

**Table 6.1:** Component values for Standard Buck Converter with non-ideal components

Inductance, $L$	$3.6 \mu H$
Capacitance, $C$	$66 \mu F$

The switching frequency demands easy driven MOSFETs with a small  $Q_g$ , both for high-side and low-side switches. As high-side switch the Infineon BSC117N08NS5 have been used. It is the switch in the specified selection range with the smallest  $Q_g$  and also the fastest switch providing the lowest switching losses. Even if the energy is transferred through the high-side switch in a shorter time compared to the low-side switch, the voltage is higher on the primary side. As a result the RMS current is lower in the high-side switch compared to the low-side. Therefore is the  $R_{DS(on)}$  in the high side switch of lesser importance in relation to  $Q_g$  compared to the low-side switch. As low-side switch the BSC061N08NS5 is used. It has a lower  $R_{DS(on)}$  and larger  $Q_g$  compared to the high-side switch but is still one of the more easy driven MOSFETs in the selection range.

The simulation results presented in Table 6.2 indicates more losses compared to the real converter measurements presented in Section 5. One of the reasons is the change in  $f_{sw}$  from  $200kHz$  to  $300kHz$  which results in higher switching losses as well as a lower duty cycle due to a higher conversion ratio.

**Figure 6.1:** Standard Buck Converter implemented in LTspice

**Table 6.2:** Simulation results for a Standard Buck Converter at nominal load

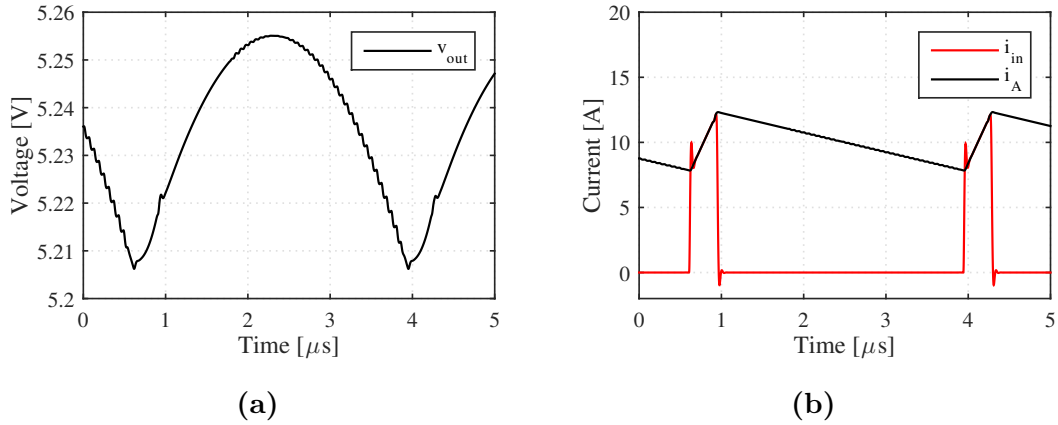
$D$	0.0975
$P_{in}$	55.5W
$P_{out}$	52.3W
$V_{in}$	55.0V
$V_{out}$	5.2V
$\Delta V_{out}$	50mV
$I_{out}$	10.0A
$\eta$	94.2%
Losses $L$	0.72W
Losses MOSFETs	2.49W
Total losses	3.2W

These results meets the specification regarding output current and output voltage. Efficiency is considered to be the most interesting parameter and the focus in the topology comparison will therefore be on efficiency. In total the standard buck converter has total loss of 3.2W and the total losses in the MOSFETs can be seen in Table 6.3.

**Table 6.3:** MOSFETs losses for Standard Buck Converter at nominell load

	Turn on	Conduction	Turn off	Total
High-side Switch <i>BSC117N08NS5</i>	994 mW	93 mW	273 mW	1360 mW
Low-side Switch <i>BSC061N08NS5</i>	82 mW	643 mW	405 mW	1130 mW
				2.49 W

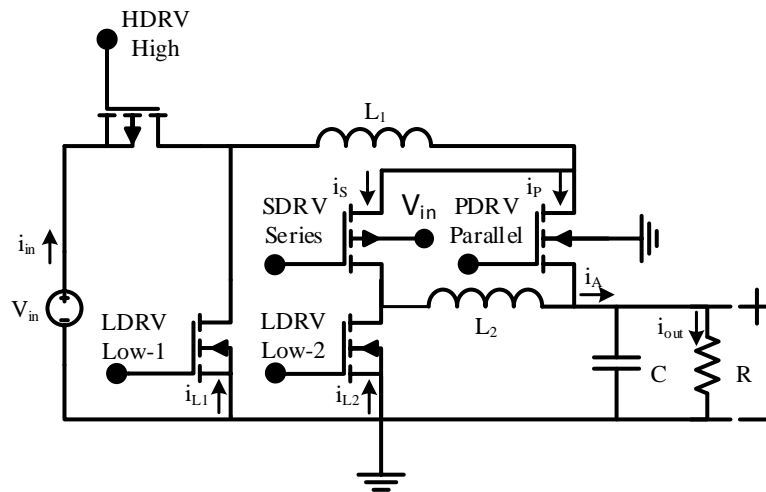
As can be seen from Table 6.3, the switching losses is dominant for the high-side switch and the conduction losses are dominant for the low-side MOSFET. With the calculated values of capacitance and inductance, the output voltage can be seen in Figure 6.2a and the continuously deliver current to the load as can be seen in Figure 6.2b. An output current with lower ripple reduces the need for large output capacitors. -note that, the buck converter draws a pulsed input current during the short on-time for the high-side switch which increases the size of the input capacitors.



**Figure 6.2:** Output voltage (a) and input and output currents prior output capacitors (b) in a Standard Buck Converter

### 6.1.2 Switched Inductor Buck Converter

The final model of the switched inductor buck converter can be seen in Figure 6.3. The circuit has in total five MOSFETs which needs in total four different gate drive signals, HDRV, SDRV, PDRV and LDRV. LDRV can control both the low-side switches because the MOSFETs have the same gate drive signal.



**Figure 6.3:** Switched Inductor Buck Converter implemented in LTspice

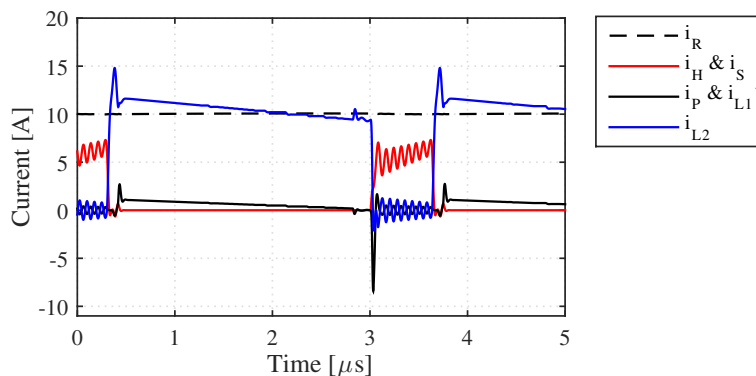


To be able to implement the converter with the switches from the selected range external diodes have been used. This implementation can be seen in A.2. From the simulations it can be seen that the duty cycle is improved from the theoretical values in Section 3.1.3, but the inductance and capacitance needs to be increased to meet the specifications. The value used in the simulation can be seen in Table 6.4.

**Table 6.4:** Component values for Switched Inductor Buck Converter with non-ideal components

Inductance, $L_1 \& L_2$	$4.1 \mu H$
Capacitance, $C$	$70 \mu F$

The switching frequency demands easy driven MOSFETs with a small  $Q_g$  for all switches except for the Low-2 switch. For the switches which demands small  $Q_g$  the Infineon BSC117N08NS5 have been chosen. It is the switch in the specified selection range with the smallest  $Q_g$  and therefore also the fastest which the lowest switching losses. The switch Low-2 carries most of the output current during the on-time (see Figure 6.4) which means that the switch needs a combination of low  $R_{DS(on)}$  and small  $Q_g$ . By simulation with different MOSFETs in the specified selection range the Infineon BSC040N08NS5 has been chosen as switch for Low-2.



**Figure 6.4:** Currents in the different MOSFETs in Switched Inductor Buck

From Figure 6.4 it can be seen that the RMS current in the Low-2 switch is relatively high compared to the current in the other switches. The RMS current is  $9.28 A$  where the other switches have RMS currents between  $0.8$  and  $2.8 A$ . The big difference in RMS current between the Low-2 switch and the other switches is the

reason why the Low-2 switch needs a switch with lower  $R_{DS(on)}$ . The over all result of the simulation of the switched inductor buck is presented in Table 6.5.

**Table 6.5:** Simulation results at nominal load for the Switched Inductor Buck Converter

$D$	0.187
$P_{in}$	55.5W
$P_{out}$	52.5W
$V_{in}$	55.0V
$V_{out}$	5.22V
$\Delta V_{out}$	50mV
$I_{out}$	10.0A
$\eta$	94.6%
Losses $L_1$ & $L_2$	0.73W
Losses MOSFETs	2.36W
Total losses	3W

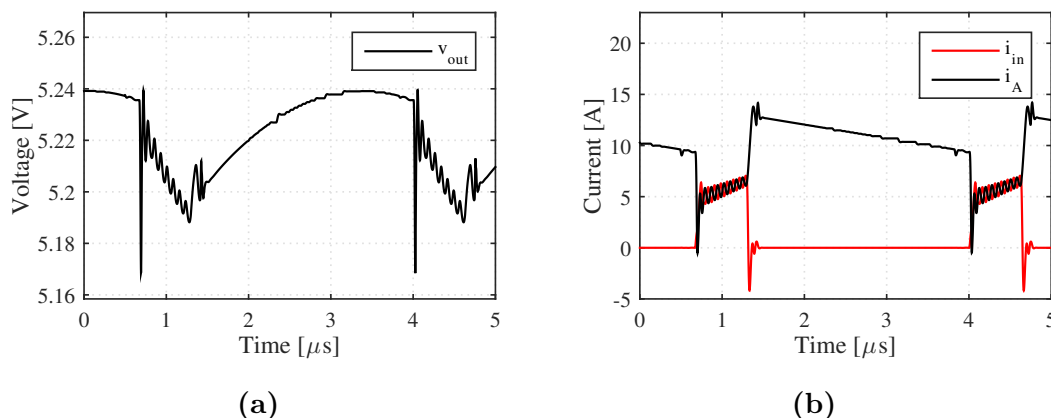
The existing setup meets the specified requirements and the increase in duty cycle is a positive quality which increases the control property of the converter. The total loss of the converter is 3W where the total losses in the MOSFETs can be seen in Table 6.6.

**Table 6.6:** MOSFET losses for Switched Inductor Buck Converter at nominell load

	Turn on	Conduction	Turn off	Total
High-side Switch, High BSC117N08NS5	159mW	82mW	115mW	355mW
Series Switch, Series BSC117N08NS5	164mW	4mW	118mW	285mW
Parallel Switch, Parallel BSC117N08NS5	39mW	72mW	35mW	146mW
Low-side 1 Switch, Low-1 BSC117N08NS5	12mW	5mW	112mW	129mW
Low-side 2 Switch, Low-2 BSC117N08NS5	106mW	449mW	894mW	1449mW
				2.364W

As can be seen in Table 6.6, the primary losses are in the Low-2 switch which is taking care of almost the whole current when it is conducting. Half of the

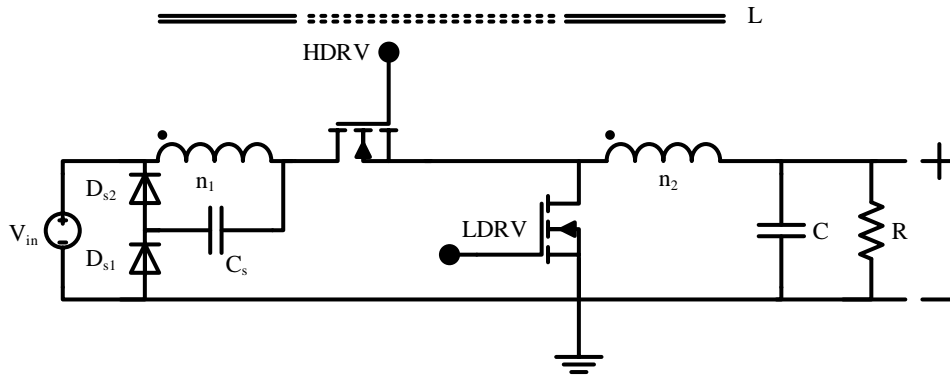
total losses are in this switch. The inductor which has a series resistance of  $7m\Omega$  contributes with almost  $0.7W$  losses, this is around 20% of the total losses and it is caused by the high RMS current. The output voltage is presented in Figure 6.5 and as can be seen, the ripple is approximately  $71mV$  which is considered to be within the limits. There is also a high frequent ripple which is caused by the unfiltered switching transients. Since the parallel switch in Figure 6.3 is connected after the inductor, the transient from the switch will be seen directly on the output. This is caused by parasitic impedances in the capacitors which will make the capacitors unable to filter out the high frequent switch noise. Figure 6.5b shows the input current and the current after the inductor. The longer duty cycle would result in a slightly smaller input filter. The output current however fluctuates significantly due to the series/parallel operation which increases the size of the output filter.



**Figure 6.5:** Output voltage (a) and input and output currents prior output capacitors (b) in a Switched Inductor Buck Converter

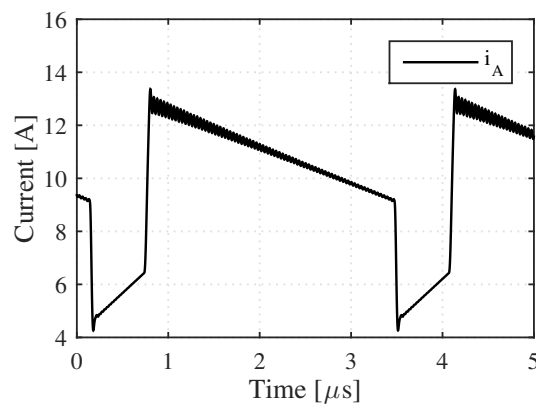
### 6.1.3 Tapped Inductor Buck Converter

The implementation of the tapped inductor buck converter is similar to the standard buck converter. The topology also utilizes a high- and low-side MOSFET and the same control signals can be used. The circuit implemented in LTspice can be seen in Figure 6.6.



**Figure 6.6:** Tapped Inductor Buck Converter implemented in LTspice

The component values for the implemented converter can be seen in Table 6.7. The needed inductance is higher due to high current ripple during the discharge phase, see Figure 6.7.



**Figure 6.7:** Inductor current in Tapped Inductor Buck Converter

This ripple can be reduced with better coupling between the inductor windings. The larger output capacitors is needed to reduce a voltage spike which occurs when winding  $n_1$  is connected in series with  $n_2$  again.

**Table 6.7:** Component values for Tapped Inductor Buck Converter with non-ideal components

Inductance, $L_1$ & $L_2$	3.3 $\mu H$
Capacitance, $C$	300 $\mu F$

The topology utilizes a high-side and a low-side MOSFET like the standard buck converter which gives that the same high-side MOSFET, Infineon BSC117N08NS5, is used. Since the low-side MOSFET transfer the energy during discharge, when both windings discharge through  $n_2$ , a MOSFET with lower  $R_{DS(on)}$  is needed. The BSC040N08NS5 is used as low-side MOSFET. The over all result of the simulation of the tapped inductor buck is presented in Table 6.8.

**Table 6.8:** Simulation results at nominal load for the Tapped Inductor Buck Converter

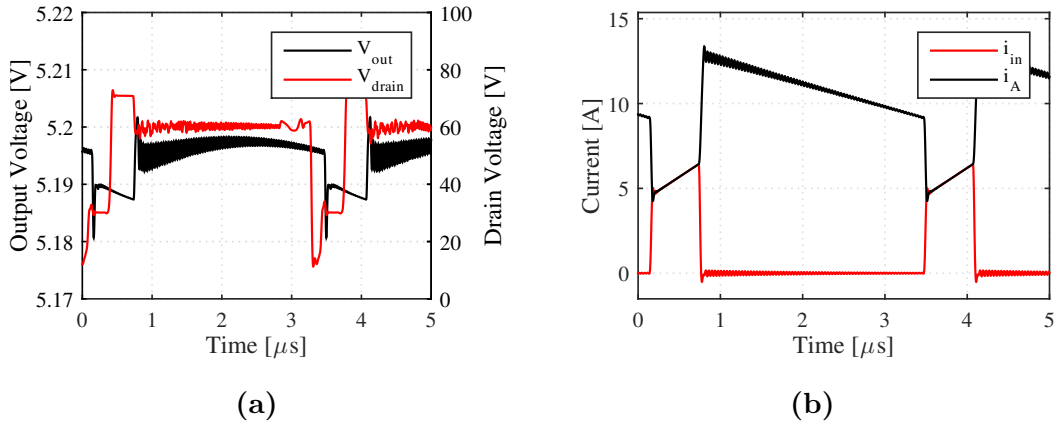
$D$	0.1836
$P_{in}$	54.4W
$P_{out}$	51.9W
$V_{in}$	55.0V
$V_{out}$	5.20V
$\Delta V_{out}$	21mV
$I_{out}$	9.99A
$\eta$	95.2%
Clamping circuit losses	0.2W
Losses $L_1$ & $L_2$	0.78W
Losses MOSFETs	1.5W
Total losses	2.6W

Simulations were performed at both maximal load and nominal load which show that the specifications are met. The efficiency is better than for the standard buck converter and as can be seen from Table 6.8 and 6.9, most of the losses are concentrated to the MOSFETs so component selection of MOSFETs are of utmost importance.

**Table 6.9:** MOSFET losses for Tapped Inductor Buck Converter at nominal load

	Turn on	Conduction	Turn off	Total
High-side Switch <i>BSC117N08NS5</i>	377mW	75mW	172mW	624mW
Low-side Switch <i>BSC040N08NS5</i>	98mW	521mW	285mW	904mW
				1.528W

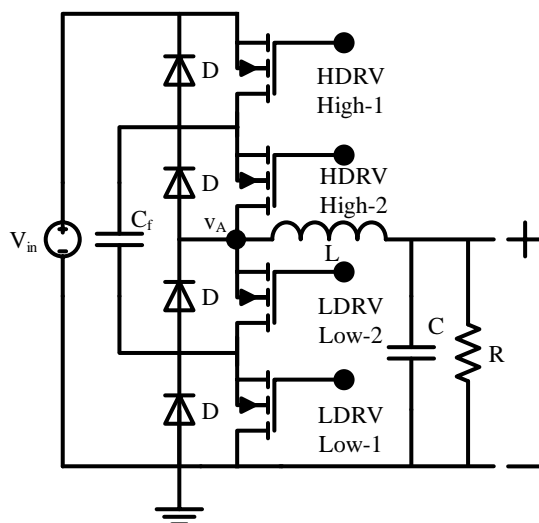
The high-side MOSFET drain voltage is presented in Figure 6.8a where it can be seen that the drain voltage spikes are effectively clamped at 73V. From Figure 6.8b it can be seen that the output current ripple is significantly larger compared to the standard buck and this is partly a reason for the larger output capacitors. The need for input capacitors is however slightly less since the duty cycle is longer.



**Figure 6.8:** Output voltage and high-side switch drain voltage (a) and input and output current prior to the output capacitors in the Tapped Inductor Buck Converter

### 6.1.4 Three Level Buck Converter

The final model of the three level buck converter implemented in LTspice together with the four control signals to the MOSFETs, can be seen in Figure 6.9. The topology demands a combination of easily driven MOSFETs and MOSFETs with low  $R_{DS(on)}$  due to the different RMS currents in the MOSFETs.



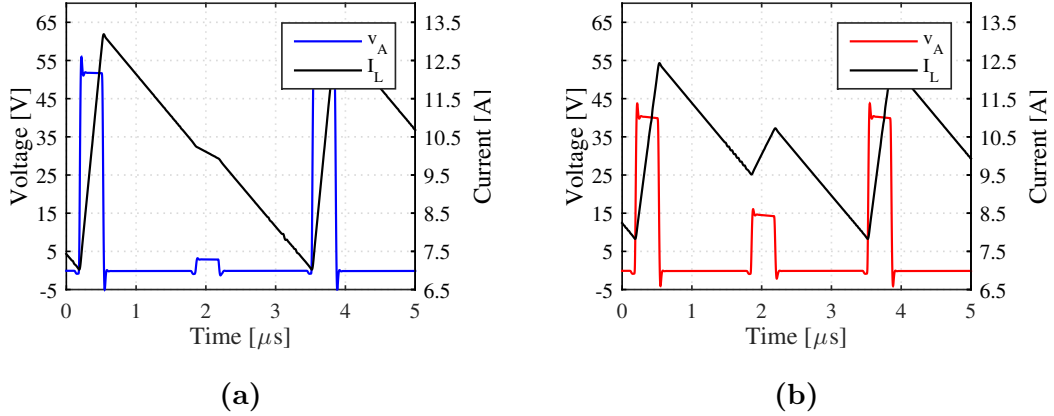
**Figure 6.9:** Three Level Buck Converter circuit as implemented in LTspice

The non-idealities in LTspice has a large effect on the calculated values and to meet the specified values for the converter in Table 3.1, both the capacitances and the inductance needs to be increased and the flying capacitance needs to be decreased. The values for the different components can be seen in Table 6.10. The inductance value needs to be almost double the calculated value to match the specified value on the current ripple. The series resistance and current limit were taken from similar inductances in the component list.

**Table 6.10:** Component values for Three Level Buck Converter with non-ideal components

Inductance, $L$	$2.5\mu H$
Capacitance, $C$	$88\mu F$
Flying Capacitance, $C_f$	$6.6\mu F$

From simulation it can be observed that an increase in flying capacitance also increases the current ripple inside the inductance. This is due to that a larger capacitance has a lower impedance causing a lower voltage drop over the capacitance, see Figure 6.10a. With a lower voltage drop over the flying capacitor,  $v_A$  gets almost the full input voltage. When the inductance in the next phase is discharged the current ripple will be larger then in the specifications. By increasing the value of the flying capacitance, the ripple in the inductance can be decreased, see Figure 6.10b.



**Figure 6.10:** Current through the inductance and voltage over the flying capacitors with  $66\mu F$  flying capacitor (a) and  $6.6\mu F$  flying capacitor (b) in the Three Level Buck Converter

The output parameters from simulations with values from Table 6.10 can be seen in Table 6.11. It can be seen that the total losses for the system is approximately  $4.5W$  which is larger than for the standard buck converter.

**Table 6.11:** Simulation results for Three Level Buck at nominell load

$D$	0.108
$P_{in}$	57.4W
$P_{out}$	52.9W
$V_{in}$	55.0V
$V_{out}$	5.24V
$\Delta V_{out}$	40mV
$I_{out}$	10.1A
$\eta$	92.16%
Losses $L$	0.73W
Losses MOSFETs	3.8W
Total losses	4.5W

The total losses in the MOSFETs can be seen in Table 6.12. Due to that the system has two switches working with high currents, High-1 and Low-1, the losses in this switches is dominant.



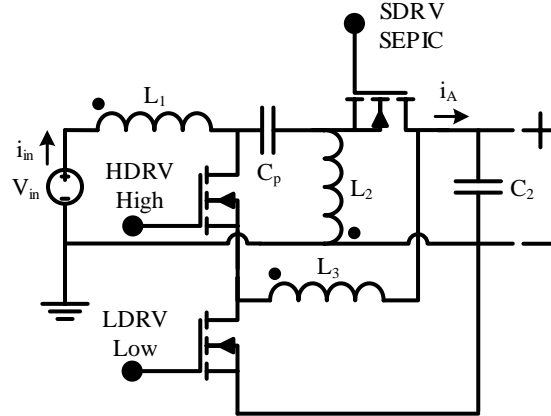
**Table 6.12:** MOSFETs losses for Three Level Buck at nominell load

	Turn on	Conduction	Turn off	Total
High-side Switch, High-1 <i>BSC117N08NS5</i>	936mW	160mW	146mW	1242mW
High-side Switch, High-2 <i>BSC032N04LS</i>	56mW	41mW	35mW	132mW
Low-side Switch, Low-2 <i>BSC010N04LS</i>	118mW	262mW	234mW	614mW
Low-side Switch, Low-1 <i>BSC061N08NS5</i>	60mW	670mW	1112mW	1842mW
				3.830W

The High-1 MOSFET has been chosen to Infineon BSC117N08NS5 which is the most easily driven MOSFET in the specified selection range and there for has the lowest  $Q_g$ . The RMS current through the MOSFET is 3.46A and from Table 6.12 it can be seen that the turn on losses are dominant. This MOSFET has the full input voltage across which has led to that a voltage limit of 80V is used. The High-2 MOSFET has a maximum of  $V_{in}/2$  across and has a RMS current through of 3.31A which has resulted to that Infineon BSC032N04LS has been chosen. This MOSFET has a low  $R_{DS(on)}$  which decreases the conduction losses and has a voltage limit of 40V. The RMS current through the Low-2 MOSFET is 9.67A which has resulted in to that a MOSFET with the lowest  $R_{DS(on)}$  has been chosen. Infineon *BSC010N04LS* has a voltage limit of 40V and has the lowest  $R_{DS(on)}$  in the selection range which reduces the conduction losses. Low-1 also has full input voltage across and a RMS current of 9.71A through but also needs a easily driven MOSFET due to the long on-time which has resulted in that the Infineon *BSC061N08NS5* is chosen. By this component selection, the losses are divided between conduction losses and turn-off losses. The high current through many MOSFETs contributes to that the total losses increases.

### 6.1.5 SEPIC fed Buck Converter

The SEPIC fed buck converter uses three MOSFETs and each MOSFETs needs its own gate drive signal, see Figure 6.11. The SEPIC fed buck converter provides two parallel paths for the energy, either through the coupling capacitor  $C_p$  or through the inductor  $L_3$ .



**Figure 6.11:** SEPIC fed Buck Converter circuit as implemented in LTspice

The inductors and capacitors used in the simulations are larger than the ones specified in Table 3.12. The capacitor and inductor models used in these simulations take the parasitic impedance into account which results in inferior performance, thereby the need for larger components, see Table 6.13.

**Table 6.13:** Component values for SEPIC fed Buck Converter with non-ideal components

Inductance, $L_1, L_2, L_3$	$3.2\mu H$
Capacitance, $C_2$	$1mF$
Coupling Capacitance, $C_p$	$6.9\mu F$

There are three different MOSFETs in the SEPIC fed buck topology. There is the high-side MOSFET which is shared by the SEPIC section and the buck section. The Low-side MOSFET used for freewheeling of the buck section. Lastly the SEPIC MOSFET on the low-voltage side of the converter which is used for freewheeling of the SEPIC section. The Infineon BSC117N08NS5 is used as high-side and low-side MOSFETs and the BSC072N08NS5 is used as SEPIC MOSFET. The MOSFETs losses can be seen in Table 6.14 and it can be seen that the switching losses are dominant in the SEPIC fed buck converter. The easy driven MOSFETs contribute to lower switching losses which results in a better efficiency. It can also be seen that the losses in each MOSFET is significantly lower compared to the losses presented in Table 6.3. As a result the converter can handle higher power with the same MOSFET ratings. The heat will also be distributed over more components which will simplify cooling.

**Table 6.14:** MOSFET losses for SEPIC fed Buck Converter at nominell load

	Turn on	Conduction	Turn off	Total
High-side Switch <i>BSC117N08NS5</i>	509mW	71mW	133mW	713mW
Low-side Switch <i>BSC117N08NS5</i>	27mW	277mW	446mW	750mW
SEPIC Switch <i>BSC072N08NS5</i>	43mW	218mW	424mW	685mW
				2.148W

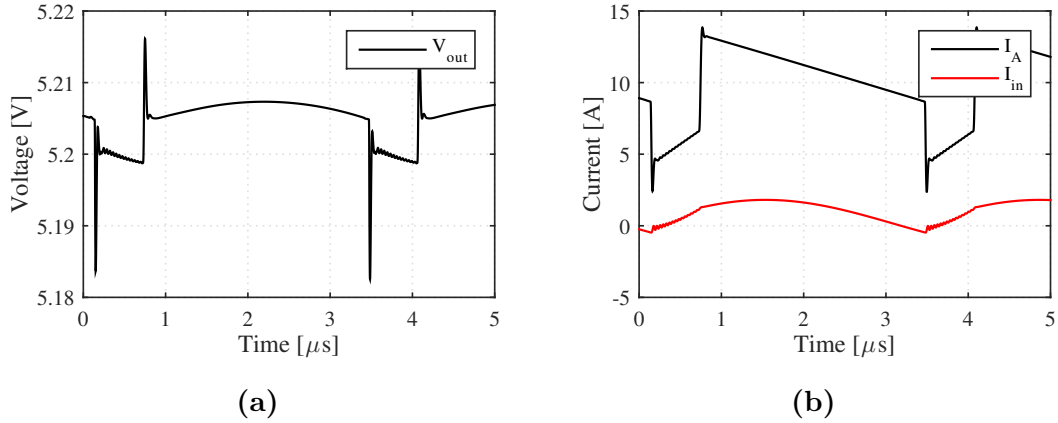
The simulation results of the SEPIC fed buck converter indicates a very good efficiency compared to the standard buck converter, see Table 6.15. The losses are concentrated to the MOSFETs as presented in Table 6.14. As seen from the table, the losses in all MOSFETs are significantly lower compared to the standard buck. The distribution of losses makes it easier to handle heat and components with lower power rating can be used. Note that there are significant voltage spikes due to the SEPIC MOSFET which is connected directly to the output which creates transients. The parasitic impedances in the capacitors make them unable to absorb the high frequent transients.

**Table 6.15:** Simulationresults at nominell load for SEPIC fed Buck Converter

$D$	0.1761
$P_{in}$	54.71W
$P_{out}$	52.11W
$V_{in}$	55.0V
$V_{out}$	5.21V
$\Delta V_{out}$	34mV
$I_{out}$	10.0
$\eta$	95.2%
Losses $L_1, L_2$ & $L_3$	0.37W
Losses MOSFETs	2.1W
Total losses	2.6W

One of the advantages with the combination of a SEPIC and a buck converter is how the converter draw and deliver current. The SEPIC continuously draws current from the source which reduces the need for a input filter whilst delivering current in pulses. The buck on the other hand delivers current continuously

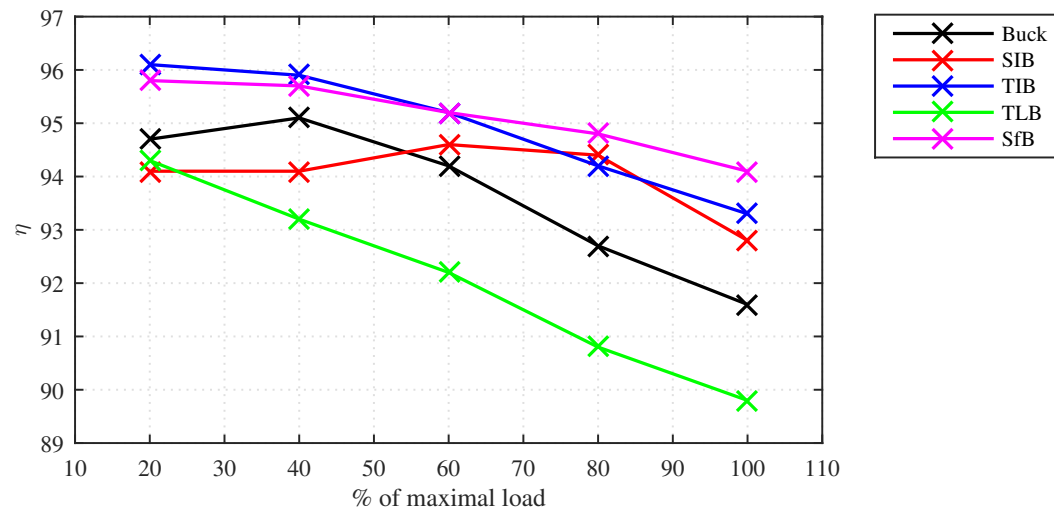
but draws current in pulses. The combination of the two results in a converter which both draw current continuously and delivers current continuously resulting in smaller filters, both for input and output compared to the conventional standard buck converter.



**Figure 6.12:** Output voltage (a) and input and output current prior to the output capacitors (b) in the SEPIC fed Buck Converter

### 6.1.6 Load dependence

The results so far have been based on operation at nominal load which is the operating point which the converter mainly will operate at. However, it is also interesting to evaluate how the load current effects the efficiency. Figure 6.13 shows the efficiency as a function of the load current expressed as percentage of the rated current. As seen from the figure, the efficiency for all converters drop for loads close to the rated load. Both the tapped inductor and the SEPIC fed Buck converter shows a high efficiency over the entire interval, where the SEPIC fed buck converter only decreases from 95.8% to 94.1% in the 20% – 100% load current span. The abbreviations used in the table are SIB for switched inductor buck, TIB for tapped inductor buck, TLB for Three level buck and SfB for SEPIC fed buck.



**Figure 6.13:** Efficiency at different load levels



# 7

## Discussion

### 7.1 Pros and Cons with Different Topologies

#### 7.1.1 Standard Buck Converter

The standard buck converter is a cheap, compact and simple circuit and there is a wide selection of controllers available. The standard buck converter offers good efficiency in a large range of operation which makes it a suitable topology in many applications. However, for applications with a high voltage conversion ratio the duty cycle becomes very low and as it approaches its minimum value the controllability decreases. There is no margin for regulation close to the minimal duty cycle.

The main advantages are:

- Simple
- Cheap
- Off the shelf controllers

The main disadvantages are:

- Low duty cycle

### 7.1.2 Switched Inductor Buck Converter

The switched inductor buck converter offers a slightly improved efficiency and a longer duty cycle compared to the standard buck converter. The increased duty cycle improves the controllability for operation close to what would be close to the minimal duty cycle in a standard buck converter. The converter utilizes five MOSFETs and in the simulations the losses have been concentrated to one of the low-side MOSFETs. A better distribution and an even more easy driven MOSFET on the low-side would likely increase the efficiency. Off the shelf controllers have not been found for this topology which makes it problematic to implement.

The main advantages are:

- Longer duty cycle

The main disadvantages are:

- Custom control circuit
- Increased number of MOSFETs
- Custom inductor
- Large footprint

### 7.1.3 Tapped Inductor Buck Converter

The tapped inductor converter offers high efficiency with a longer duty cycle. The longer duty cycle is achieved by changing the effective inductance between the charge and discharge phases. This change causes a large output voltage ripple which increases the size of the output filter. There are also controllers available off the shelf.

The main advantages are:

- Few components
- High efficiency
- Off the shelf controllers are available
- Longer duty cycle

The main disadvantages are:

- Large output ripple



- Custom inductor needed

#### 7.1.4 Three Level Buck Converter

In order to perform better than the standard buck converter, the three level buck converter demands a switching frequency in the  $MHz$  range. As can be seen in [6], with a switching frequency of  $2MHz$  the three level buck perform better than the standard buck both with better efficiency and with lower inductance. By increasing the frequency the three level buck converter can decrease in total footprint size but still have a high efficiency. However, with a switching frequency at  $300kHz$  the three level buck is a poor alternative.

The main advantages are:

- Less inductance needed
- Higher duty cycle
- Performs well with high frequencies

The main disadvantages are:

- Lower efficiency
- Twice the amount of MOSFETs
- Complex controller needed
- High conduction losses in High-1 and Low-1 MOSFETs

#### 7.1.5 SEPIC fed Buck Converter

The SEPIC fed buck converter offers high efficiency over a large load span but the expected size of the inductor makes it significantly larger compared to both the standard buck converter and the tapped inductor buck converter. The inductor is also a three winding coupled inductor which is not available off the shelf and a custom inductor is needed instead. The increased cost of a custom solution is greatly dependent on the volume and is hard to estimate but it will result in increased costs. The topology is also patented by CUI which most likely also increases the cost. The multiple energy paths reduces the component stresses which makes it easier to design a converter with higher power rating.

The main advantages are:

- High efficiency over large load span
- Reduced input and output filters
- Distributed losses
- Longer duty cycle

The main disadvantages are:

- Large output ripple
- Patented
- Custom inductors needed

## 7.2 Efficiency

The efficiency has been the main focus for this thesis and in focus when simulation models were built up and components selected. The efficiency has been used to compare the different topologies and to be able to do a fair comparison, the models used needed to be comparable. This has resulted in an efficiency for each topology which has been maximized with the available components. For better efficiency than the presented, components need to be selected outside of the specified range. If the selection range would have been too broad the possibility to compare the different topologies would be lost.

**Table 7.1:** Efficiency results over load current sweep

	20%	40%	60%	80%	100%
Buck	94.7	95.1	94.2	92.7	91.6
SIB	94.1	94.1	94.6	94.4	92.8
TIB	96.1	95.9	95.2	94.2	93.3
TLB	94.3	93.2	92.2	90.8	89.8
SfB	95.8	95.7	95.2	94.8	94.1

The load current dependence, see Table 7.1, shows a weaker dependence on loading for the SEPIC fed buck which makes it suitable for applications with operating points close to the rated. An other interesting characteristic is for which load current the maximal efficiency is achieved. Less losses result in a less heat dissipation which might reduce the overall size since less cooling is needed. This is an interesting aspect to consider when designing a system.

## 7.3 Size Comparison

An important parameter that needs to be taken into consideration is the physical size of the converter. The size comparison can be done in many ways depending on how many parameters that are included. One way is to investigate the footprint size of the different components needed for each topology, excluding the drive and control circuit. The footprint size comparison of the different topologies can be seen in Table 7.2.

**Table 7.2:** Size comparison between the investigated topologies

	<b>MOSFET</b> ( $mm^2$ )	<b>Ind</b> ( $mm^2$ )	<b>Cap</b> ( $mm^2$ )	<b>Diode</b> ( $mm^2$ )	<b>Tot</b> ( $mm^2$ )	<b>Normalized</b> <b>Score</b>	<b>Efficiency</b>
<b>Buck</b>	70	169	15	12	266	1	94.2%
<b>SIB</b>	175	178	35	n/a	388	1.46	94.6%
<b>TIB</b>	70	178	20	24	292	1.1	95.2%
<b>TLB</b>	140	188	35	n/a	363	1.36	92.2%
<b>SfB</b>	105	306	60	n/a	471	1.77	95.2%

The comparison in Table 7.2 is based on size data from the different manufactures and the presented values are the total size of all components. The size of the capacitor is based on its total capacitance value, see Table 7.3. The size of the inductor is based on the inductance value and the maximal RMS current which flows through the inductor. For the coupled inductors in the switched inductor buck, tapped inductor buck and the SEPIC fed buck, the inductor size was estimated to be equal to an inductor with a current rating of the total RMS current in all windings and with the same inductance value. This results in a total heat dissipation and magnetic flux from all windings which is seen as it comes from a single inductor and can therefore be compared against standard inductors. Based on these assumptions, a normalized score, where the standard buck converter is the reference, is determined and compared together with the efficiency of the different topologies. The inductors are the component with the greatest impact in the size comparison but it is also the component which is the hardest to get reliable information about. As can be seen in Table 7.2, the size difference between the standard buck converter and the tapped inductor buck is not significant. The tapped inductor buck is 8% bigger but has an efficiency which is one percent better. Depending on the area of application this topology can be a good replacement. The inductor for the SEPIC fed buck was hard to find due the three coupled inductors. This needs to be custom made and is not available off the shelf. It might be possible for manufactures to provide smaller inductors and in such a case this topology can be an interesting replacement to the standard buck converter due to the high

efficiency. The three level buck which has both bigger footprint size and lower efficiency, is from this point of view a poor replacement. The same conclusion can be drawn regarding the switched inductor buck which has an efficiency which is just 0.4% better and a footprint size which is 85% bigger than the standard buck converter.

**Table 7.3:** Capacitance and inductance values for the different topologies

	Cap ( $\mu F$ )	Ind ( $\mu H$ )
Buck	66	3.6
SIB	70	2 · 4.1 <i>coupled</i>
TIB	300	2 · 3.3 <i>coupled</i>
TLB	88	2.5
SfB	1000	3 · 3.2 <i>coupled</i>

## 7.4 Cost Discussion

Another important parameter which needs to be taken into consideration is the total cost of the converter. The cost comparison can be done in many ways depending on how many parameters that are included. This comparison is made with the different components needed for each topology without drive and control circuits. No considerations have been taken regarding the topology design effects on production and development costs. The cost comparison of the different topologies can be seen in Table 7.4.

**Table 7.4:** Cost comparison between the investigated topologies

	MOSFET	Ind	Cap	Diode	Tot	Normalized Score	Efficiency
<b>Buck</b>	1	1.6	0.7	0.4	3.7	1	94.2%
<b>SIB</b>	2.5	1.4	1.5	n/a	5.4	1.46	94.6%
<b>TIB</b>	1	1.4	0.9	0.7	4	1.08	95.2%
<b>TLB</b>	2	1	1.5	n/a	4.5	1.22	92.2%
<b>SfB</b>	1.5	2.1	2.6	n/a	6.2	1.68	95.2%

To get a relevant cost comparison between the different component, prices was taken from a major reseller of electrical component and with a price based on an order of 1000 components. The price for the different components where summed up and given a normalized score and presented together with the efficiency. As in the size comparison where the tapped inductor buck was the smallest topology

except from the buck, the tapped inductor buck is the cheapest topology besides the standard buck. The reason the tapped inductor buck can meet the price of the standard buck converter is the lack of expensive components which makes the tapped inductor buck a good replacement regarding both price and efficiency. The three level buck is a more expensive alternative and has a lower efficiency, it is therefore considered to be a poor replacement. The switched inductor buck and the SEPIC fed buck both have higher efficiency, especially the SEPIC fed buck which have an efficiency increase of one percent. However both the converters have significantly higher cost compared to the the standard buck converter. The small efficiency increase of the switched inductor together with both an increase in cost and footprint size makes it a less interesting topology compared to the tapped inductor converter. The SEPIC fed buck has an improved efficiency compared to the standard buck converter which makes it an interesting topology. The reason for the high price is the need of an expensive inductor and the need of much output capacitance due to the voltage spikes created by the MOSFET directly on the output. There is also a cost for using the patented technology in the SEPIC fed buck which has not been accounted for.



# 8

## Future work

This comparative study was focused on what is considered to be the most important parameters when selecting a topology. However there are assumptions made and the scope has been limited to fit the time frame available. To get even better comparisons several areas could be evaluated as mentioned below. The simulations have not been focused on achieving the highest efficiency possible, instead it has been focused on how to achieve a high efficiency under similar conditions. By expanding the scope and investigating different component technologies the efficiency could likely be increased.

### 8.1 Transient response

The transient response of a converter supplying digital and non-linear loads is a key parameter but it has been considered to be out of the scope of this thesis due to time restrictions. An investigation that quantify the problems surrounding a low duty cycle and the impact of increased control margin on the duty cycle would contribute to more knowledge of the advantage of the investigated topologies. Other key factors which has a large impact such as filter size would also need to be investigated.

### 8.2 Control Circuit

To focus the evaluation on the topology, simplifications regarding control circuits have been made. Both regarding control algorithms and drive circuits. For some

topologies of the shelves controllers are available and these could be evaluated directly whilst some controllers would need to be custom designed to be able to make a comparison of the topologies.

### 8.3 Inductor verification

In this thesis simple inductor models with only a series resistance have been used. In a real inductor there are several more parasitics which cause losses and change in inductance throughout the operating area. Core losses caused by the changing magnetic flux is one of the major parasitics and can be a significant contributor to losses. However with a properly selected core material the losses can be limited. In the investigated topologies the ripple in the inductor flux should be comparable. The large output current ripple is caused by connection changes which effects the output current but thanks to the coupling the magnetic flux causing the core losses should be comparable in the investigated topologies. Investigation of the impact of core losses would however contribute to more accurate results. The inductors are assumed to operate linearly, real inductor cores will be saturated as the current approaches the rated saturation current resulting in decreased inductance at higher currents. This can be taken into account with non-linear models to make sure the inductor selection is appropriate. Errors from the neglected saturation will mainly effect the filter (capacitor and inductor) size.

### 8.4 Prototype verification

Due to time restraints, no physical verification was performed. A real circuit would introduce several unknown parasitics which will both dampen voltage spikes and increase losses. It would also provide greater insight into the inductor performance. A real implementation would also provide valuable insight regarding the implementation complexity of the different topologies. Simplifications regarding control and drive would have to be investigated.

### 8.5 Gate-Charge extraction

The SEPIC fed buck converter in this thesis utilizes 3 drive circuits. However the topology as implemented by CUI have a fourth winding on the coupled inductor which performs a gate charge extraction. The potential over the inductor will be



different during the charge and discharge phases and this voltage change is used to move the gate charges between the gates of the low-side MOSFET and the SEPIC MOSFET. According to CUI, this circuit will increase the efficiency and an investigation of such a circuit would probably contribute to a more accurate efficiency result.



# 9

## Conclusions

This thesis has shown that there are alternative converters topologies to the standard buck converter topology which can improve the efficiency. The results also improve the duty cycle which might improve controllability for the investigate voltage ratio.

It is the tapped inductor buck converter and the SEPIC fed buck converter which has demonstrated the best performance in simulations, the switched inductor buck has also shown a small improvement in efficiency. The two investigated topologies with the highest efficiency indicate that it is possible to obtain an efficiency which is one percent higher compared to the standard buck converter at the investigated operating point and even more at lower and higher load currents. Since all simulations were done with a switching frequency at  $300kHz$  and with components from the same manufacturers. The final efficiency results should only be viewed as comparative figures. By focusing on selecting components with better performance instead of components with similar performance it is likely that an even higher efficiency can be achieved.

The trade-off of with using the tapped inductor buck and the SEPIC fed buck are the increased size and the utilization of coupled inductors. With a custom made coupled inductor, the size may be improved compared to the inductor size used in the evaluation. With such a custom inductor, the size difference between the suggested topologies and the standard buck converter may become negligible. Also, the SEPIC fed buck converter is patented which may increase the cost.



# Bibliography

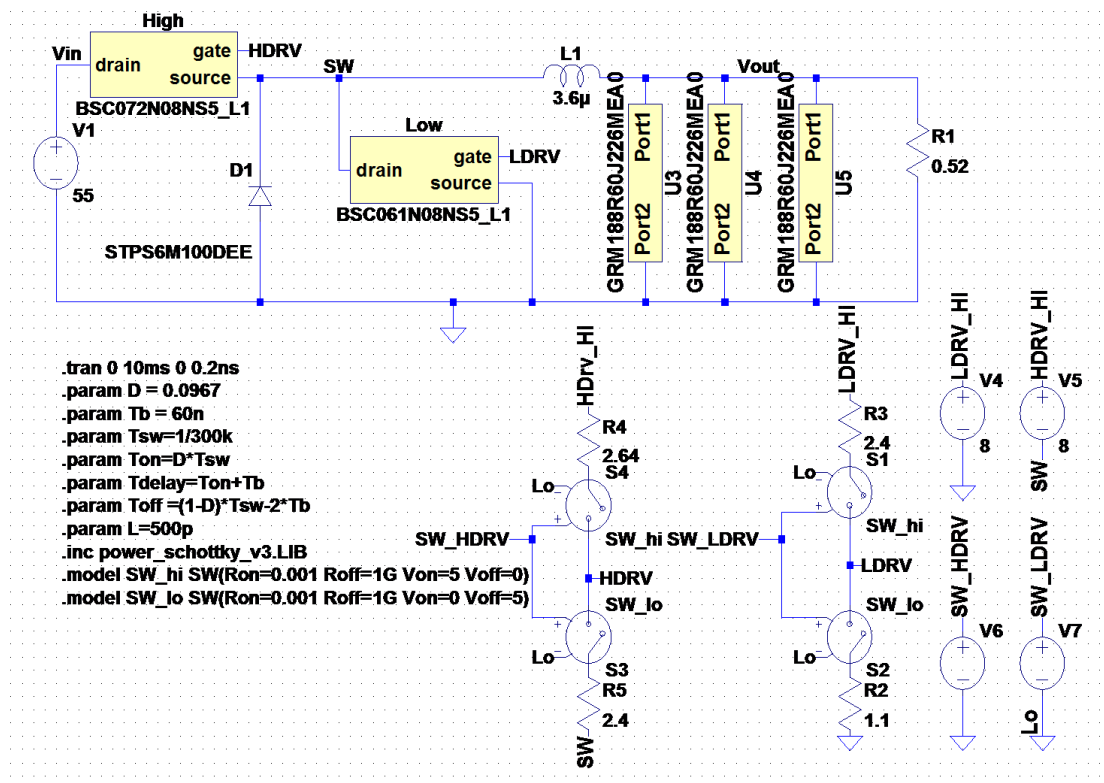
- [1] B. Axelrod, Y. Berkovich, A. Ioinovici, Switchedcapacitor/switched-inductor structures for gettingtransformerless hybrid dc–dc pwm converters, *IEEE Transactions on Circuits and Systems.I, Regular Papers* 55 (2) (2008) 687–696.
- [2] H. Cheng, K. Smedley, A. Abramovitz, A wide-input-wide-output (wiwo) dc–dc converter, *Power Electronics, IEEE Transactions on* 25 (2) (2010) 280–289.
- [3] I. Rezaei, M. Akhbari, Transformerless hybrid buck converter with wide conversion ratio, in: *Power Electronics, Drive Systems and Technologies Conference, 2011 2nd*, 2011, pp. 599–603.
- [4] M. M. Fouly, M. M. Aboudina, F. A. Hussien, Novel buck converter architectures for large step-down conversion ratio, in: *Circuits and Systems (MWS-CAS), 2014 IEEE 57th International Midwest Symposium on*, IEEE, 2014, pp. 773–776.
- [5] K. Yao, F. C. Lee, Y. Meng, J. Wei, Tapped-inductor buck converter for high-step-down dc–dc conversion, *Vol. 20*, 2005, pp. 775–780.
- [6] D. C. Reusch, High frequency, high power density integrated, point of load and bus converters, Ph.D. thesis, Blacksburg, Virginia, *http : //scholar.lib.vt.edu/theses/available/etd – 04162012 – 151740/unrestricted/Reusch\_4\_15\_12Final.pdf* (2012).
- [7] D. Li, J. Smoot, A sepic fed buck converter, in: *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 2333–2339.
- [8] J. Wei, P. Xu, H.-P. Wu, F. Lee, K. Yao, M. Ye, Comparison of three topology candidates for 12 v vrm, in: *Applied Power Electronics Conference and Expo-*

- sition, 2001. APEC 2001. Sixteenth Annual IEEE, Vol. 1, 2001, pp. 245–251 vol.1.
- [9] R. Guo, Z. Liang, A. Huang, A family of multimodes charge pump based dc-dc converter with high efficiency over wide input and output range, *Power Electronics, IEEE Transactions on* 27 (11) (2012) 4788–4798.
- [10] J. Fallin, Coupled inductors broaden DC/DC converter usage, *Texas Instruments* (2010).
- [11] J. Fallin, Designing dc/dc converters based on sepic topology, *Analog Applications Journal*.
- [12] Maxim Integrated, APP 1051, SEPIC Equations and Component Ratings (April 2002).
- [13] B. Hauke, Basic calculation of a Buck Converter’s Power Stage, *Texas Instruments*.
- [14] Texas Instruments, TPS40170 4.5 V to 60 V Wide Input Synchronous PWM Buck Controller (November 2013).
- [15] Fairchild Semiconductor Corporation, AN-6076 Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC (2008).

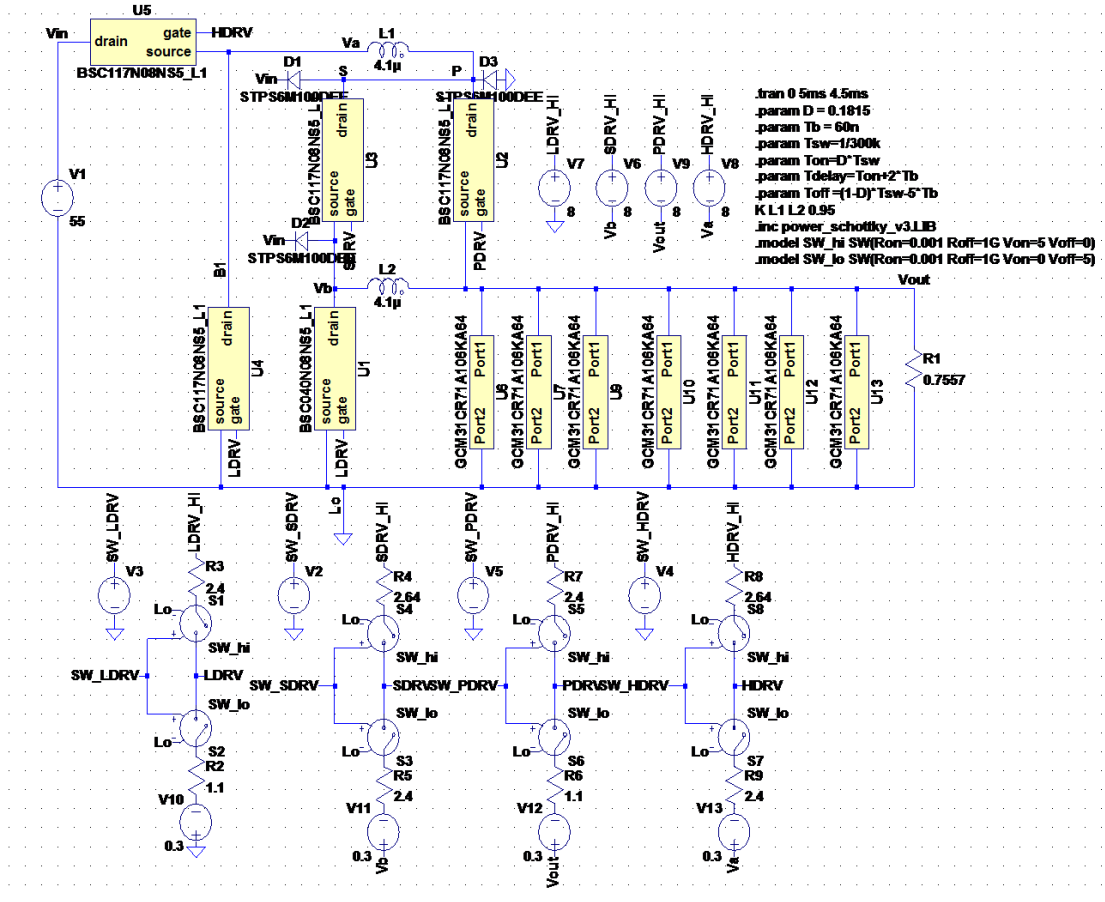
# A

## LTspice schematics

### A.1 Standard Step Down Converter

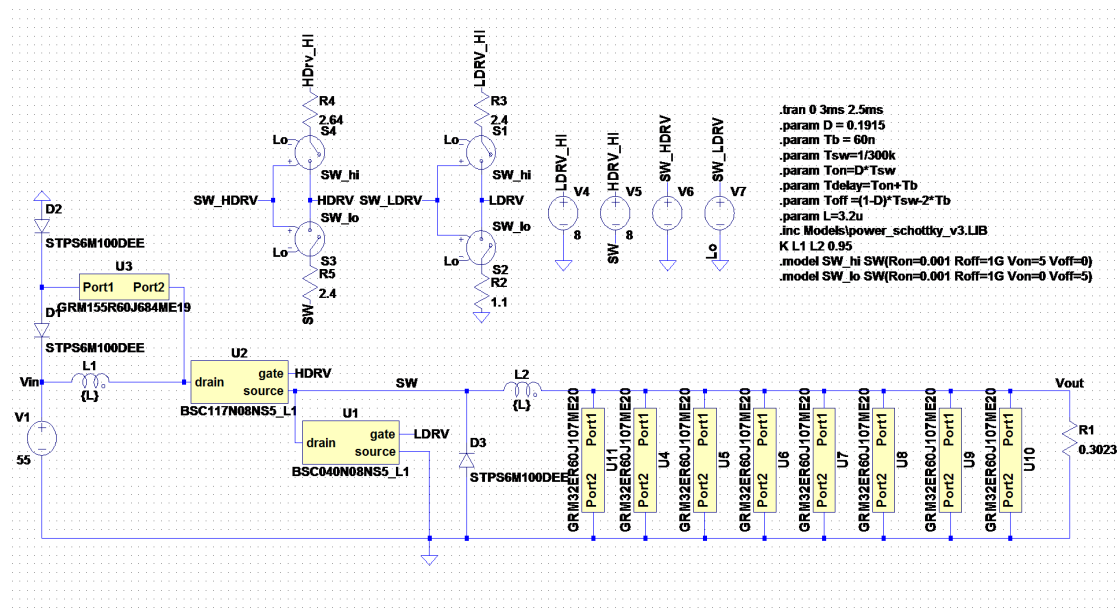


## A.2 Switched Inductor Buck Converter

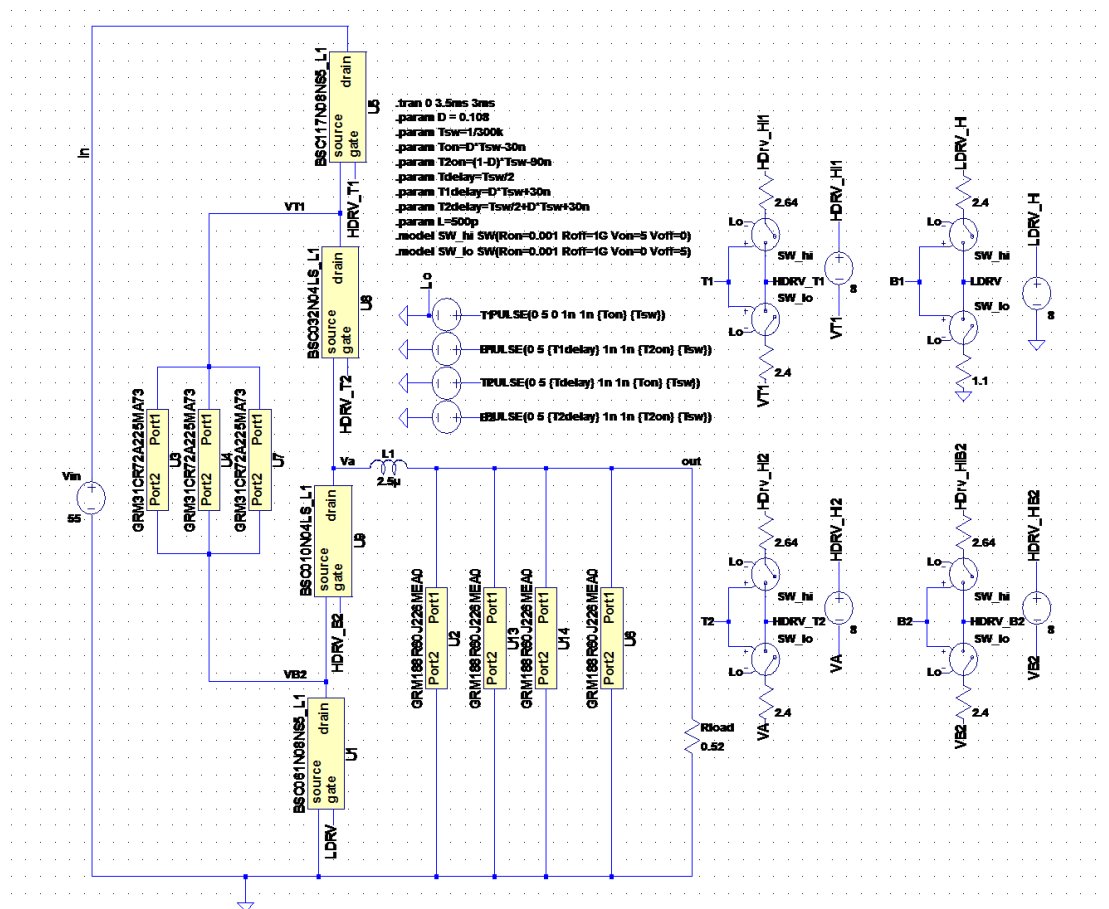




# A.3 Tapped Inductor Buck Converter



## A.4 Three Level Buck Converter



# A.5 SEPIC fed Buck Converter

