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Design and Realization of a 6 GHz Doherty Power Amplifier from Load-pull Measurement Data

Master's thesis in electrical engineering

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Abstract

In this report, a Doherty power amplifier (DPA) design method is developed based on load-pull measurement data. The developed approach is particularly suitable for realization of high frequency hybrid DPAs. This is enabled by including the bias and stability networks in the characterization test board as well in addition to the transistor. Thereby, the design method avoids having to rely on discrete component models being highly accurate. The described design method was used to fully realize a hybrid DPA.

For characterization a passive load- and source-pull setup was built around two tuners and two power meters. After finding the optimal impedances for the transistor and surrounding circuitry, the results are de-embedded to a reference plane which includes said circuit elements, thereby automatically including their effects into the design. The components of the DPA are then designed based on the measurement results. An analytical approach was used for the combiner synthesis.

The resulting amplifier exceeds 45 % power-added efficiency (PAE) for 38 dBm of output power at 6 GHz, with 42 %, 32 % and 23 % PAE at 3, 6 and 9 dB of output back-off respectively. The small-signal gain exceeds 14 dB. This high gain is attributed to careful source-pull measurements enabling a very good input match. The gain is well-centered around 6 GHz.

We conclude from the good performance of the demonstrator unit that the design method is a viable approach for DPA design even at such high frequencies, which is of interest when a MMIC design would be impractical such as in the case of low-volume production.

Keywords: Doherty, power amplifier, GaN, load pull, microwave amplifier, DPA, efficiency.

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Anders Sandström, Gothenburg, November 2015

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1

Introduction

Microwave power amplifiers (PA) are essential components in modern wireless communication systems. In a radio base station, the power amplifier alone is responsible for a large fraction of the total energy expenditure [1]. Consequently, there are significant economic and environmental motives for design and realization of highly efficient power amplifiers. Energy efficiency is also crucial in handsets to achieve a long battery life.

The instantaneous power of transmitted radio frequency (RF) signals were constant for earlier wireless communication standards, e.g. GSM. However, this is not the case for the signals used in many modern systems. Orthogonal frequency-division multiplexing (OFDM) is a commonly used modulation type today, which results in a large ratio between the average power of a signal and its peak power [2]. This is problematic because the PA still needs to be designed to handle the peak power level, even though the average output power is much lower.

For a classical class AB power amplifier, the efficiency can be very high when it is running at its full, saturated, output power. However, the efficiency rapidly drops with increasing output power back-off. This results in a low efficiency when such an amplifier is used in a system utilizing high peak-to-average power ratio signals.

There a number of techniques found in the literature to enhance the back-off efficiency of class AB PAs. One of the well-known efficiency enhancement techniques is the envelope-tracking technique, in which the drain supply voltage is not constant but varied according to the envelope of the RF input signal. This makes it possible for the amplifier to operate near saturation for a wide range of power levels [3]. Another well-known efficiency enhancement technique is the outphasing architecture. In an outphasing PA, the signal is split into two phase modulated components with constant envelopes [1], [4]. The signals are then used to drive two separate PAs which are operating in the efficient saturation region [1]. The output signal is controlled by modulating the phase relationship of the input signals [1].

The Doherty PA (DPA) is the most popular efficiency enhancement technique [1] due to its simplicity and high performance. The DPA consists of two combined amplifiers, where one is only active for high power levels [5]. Importantly, the load impedances become modulated by the arrangement, in a way that they remain optimal for a wide power range [5], [6]. A more detailed description is given in Chapter 2.1.

Today, mobile communications standards such as LTE can utilize frequencies up to 3.8 GHz, with most bands being around or below 2 GHz [7]. There is a desire for upcoming systems such as 5G to additionally make use of significantly higher frequencies, such as several potential new bands up to 6 GHz and possibly even some millimeter wave bands, where more bandwidth is available to support the increasing demand for data rates [8]. Therefore, efficient amplifiers at these frequencies are needed.

A general obstacle to circuit design at microwave frequencies is parasitics. Components, including simple passives, behave further and further from their ideal counterparts when the frequency is increased. This is especially problematic when a circuit is to be realized with a hybrid module, as opposed to a MMIC design where the whole manufacturing process can be controlled and the circuit elements can be modelled with relatively good accuracy. When the frequency is more than a few gigahertz, designing a hybrid circuit based on simulations alone becomes difficult because of inaccurate models. However, for low volume production, a MMIC design would lead to a high cost per unit because of the larger initial investment. Therefore, the design of hybrid PAs at these frequencies is still of interest.

1.1 Thesis contribution

In this thesis, a load-pull based Doherty PA design methodology is developed that is particularly suitable for realization of high frequency hybrid DPAs. In the design procedure, load-pull characterization is not only performed on the transistor itself, but on a partially complete PA that includes bias lines and the stability networks. This way, the optimal impedances are found independent of any inaccuracies of passive models, which can be a serious issue at high frequencies. The design procedure is demonstrated in a 6 GHz Doherty PA prototype, fully verifying the feasibility of the design approach.

1.2 Outline

The rest of this thesis report is organized as follows: In Chapter 2, a description of what data needs to be measured is given, and how the measurements were carried out. The results from the characterization are presented in Chapter 3. Then the Doherty PA is designed based on those figures in Chapter 4. The measured Doherty PA performance is presented and discussed in Chapter 5. Finally, the conclusion of the thesis is given in Chapter 6.

2
Characterization method

This chapter begins with a short description of the amplifier topology. This is followed by the design of test boards containing the transistor with biasing and harmonic terminations. Then the measurement setup is described together with its calibration and de-embedding scheme.

2.1 The Doherty power amplifier

In 1936, an amplifier topology aimed at improving the efficiency at back-off by using two combined amplifiers was presented by W. H. Doherty [5]. The basic idea behind the workings of the Doherty amplifier, described in [5] and [6], is to combine the output of two amplifiers, termed main and auxiliary, in such a way that the main amplifier alone amplifies low-amplitude signals, and the auxiliary amplifier is "switched on" in addition when needed at the peaks, typically by the signal itself reaching a large enough amplitude to overcome a low (class C) bias of the auxiliary device. Crucially, the arrangement of the amplifiers and the combiner network also act together to modulate the load impedances seen by the devices when the power level changes, in such a way that it is kept optimal for efficient operation. At back-off when the auxiliary cell is inactive, the impedance seen by the main amplifier becomes optimal for back-off, by the design of the combiner. At full output power, the load impedance seen by each amplifier changes to values optimal for this power level. This active load modulation is the key to how the DPA can maintain a high efficiency for a range of power levels. In the ideal case, this results in two efficiency peaks. These are located at a full power and at a back-off power level, which is 6 dB for the classical Doherty.

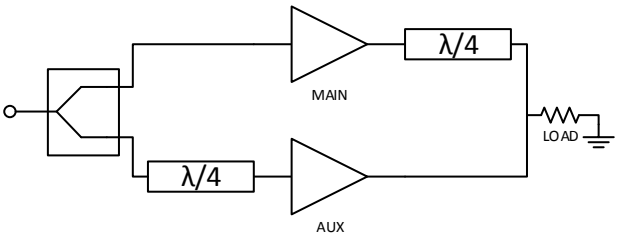


Figure 2.1: Block diagram of a classical DPA [6] in its simplest form.

A Doherty PA block diagram is shown in Fig. 2.1. If the transistors were to be ideal, this architecture would have been simple to realize [9]. However, device parasitics complicate the design, because the optimal output impedance becomes complex instead of real [9], [10], as would have been the case for an ideal current source. The load modulation in the

classical DPA only works for real impedances [10]. To solve it, in addition to conventional output matching networks, offset lines can be inserted before the output quarter wave impedance transformer [9], [10], illustrated in Fig. 2.2. The use for these lines enable the load modulation to function properly also for reactive impedances [10].

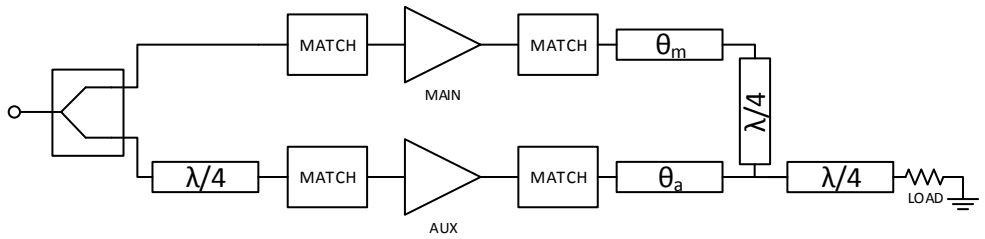


Figure 2.2: More practical block diagram of a DPA [10].

In [11] a new design approach was presented which achieves a high efficiency over a wider dynamic range compared to the classical Doherty. Additionally, the design approach integrates the matching network, offset lines and the output transformer all into one unit [11]. A block level illustration if found in Fig. 2.3. The DPA realized in this report will make use of this method.

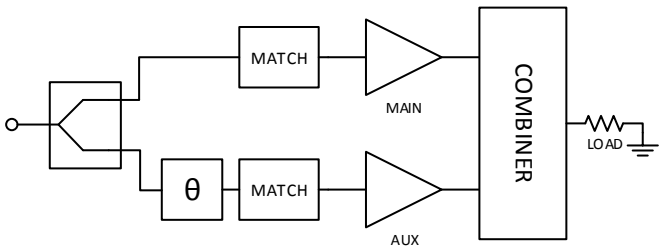


Figure 2.3: Block diagram of the Doherty PA design approach [11] used in this work.

2.2 Required data for the PA design

In order to realize the Doherty PA, certain characterization data concerning impedances are needed [11]. The key values that need to be determined by measurements are:

- Optimal load impedances at full output power for both amplifiers
- Optimal load impedance at back-off for the main amplifier
- Source impedances for optimal input matching, for both amplifiers
- The output impedance of the auxiliary amplifier in the off-state

The last item is straightforward to measure with a VNA once a test board has been manufactured, but the others require a characterization setup to be built. In the setup, tuners are placed on the source and load side of the test fixture, and these are used to vary the impedances seen by the Device Under Test (DUT). Gain and efficiency is then plotted versus impedance and optimal values can be selected. The setup will be described in further detail in later sections.

The source impedance that gives the highest gain will be considered optimal. Which load impedance is optimal is more of a trade-off, since PAE and gain peaks at different impedances, as later seen in Chapter 3.

2.3 Transistor and frequency choice

The transistor used in this project, CGHV1F006S, is an unmatched gallium nitride device specified for operation at 40 V with a nominal output power of 6 W, packaged in a 3x4 mm dual-flat-no-lead (DFN) package [12]. A model from Cree was used in simulations.

The chosen center frequency for this project is 6 GHz, because of its relevance for communication systems, such as point-to-point links and potential future interest for mobile phone networks.

2.4 Design of test boards

In this section, the design of test boards is covered. The purpose of the boards was to be a complete amplifier unit, but without any matching network, so that load- and source-pull measurements can be used to find the optimal fundamental impedances. Stability as well as bias networks were included on the boards. While the design of these were based on simulations, it would also have been possible to base the design of the stability networks on measured S-parameters of the transistor. All microstrip elements were simulated in Momentum.

2.4.1 Choice of bias voltage

In order to use the model to design the stability networks and harmonic terminations, a gate bias point needs to be selected. For the latter purpose, a deep class AB bias should be used, because this is what the final amplifier will use. The result of a DC sweep is shown in Fig. 2.4. The point -2.8 V was selected so that the device still has a bit quiescent current (about 12 mA) when there is no signal. It later turned out that this bias point is about the deepest that makes the gain reasonably flat at low power levels, and thus a good choice.

For simulating stability, the bias point that makes the transistor the least stable should be used, since it should be designed for the worst case. Coincidentally, this turned out to be the same gate bias voltage as was selected for the other simulations, -2.8 V.

2.4.2 Circuit design and stability

Typical bias tees consisting of quarter wave lines and radial stubs were designed. The overall circuit is shown in Fig. 2.5, in which it has been slightly simplified for clarity. Only one decoupling capacitor per supply voltage is shown (in reality, a range of values were used to decouple a wide frequency range). Harmonic terminations are covered later in Chapter 2.4.5.

As usual, coupling capacitors at the input and output were needed to prevent the bias and supply voltage from being present at the connectors. The capacitors that were used are 0603 SMDs from the 600S series made by ATC. Models supplied by Modelithics Inc were used to examine the self-resonance frequency of different values. 3.3 pF capacitors

were used for both input and output coupling, since this was the largest value whose self-resonance occurred at a frequency with a good margin to the highest frequency of interest.

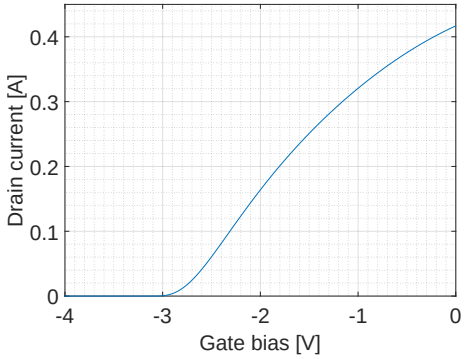


Figure 2.4: Simulated DC characteristics of the transistor. Drain current versus gate bias voltage at $V_{DS} = 40\,\mathrm{V}$.

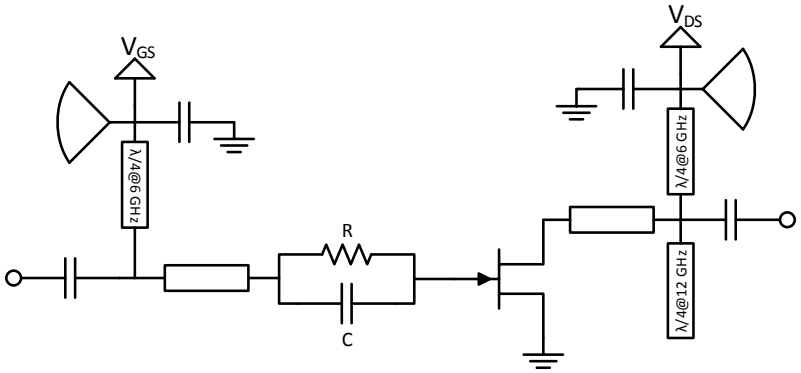


Figure 2.5: Simplified schematic of the test circuit for load-pull measurements. The characterization not only includes the transistor, but the whole amplifier unit including bias lines, stability network and coupling capacitors.

The transistor itself showed very high gain at lower frequencies and was initially unstable. A parallel RC network was added in series with the gate for stability. The initial goal was to select R and C such that the amplifier became unconditionally stable, but simulations using capacitor models from Modelithics showed that it was very hard to reach unconditional stability while keeping component values reasonable and without compromising too much gain. It was then decided to settle for a conditionally stable amplifier, with R and C having values of $12\,\Omega$ and $0.5\,\mathrm{pF}$ respectively. Simulations showed that this arrangement should be stable at the expected source and load reflection coefficients with good margin.

2.4.3 Simulated load-pull

Although the final amplifier will be designed based on measured load-pull data, load-pull simulations were carried out to get a first impression about where the optimal load impedances are located. Furthermore, this data is needed for simulations to determine the second harmonic terminations. The results of a load-pull of a transistor, excluding any stability network and with ideal biasing, are shown in Fig. 2.6 as a reference for the tran-

sistor's performance. The source impedance was conjugately matched at the fundamental frequency and the second harmonic source and load impedances were set as short circuits.

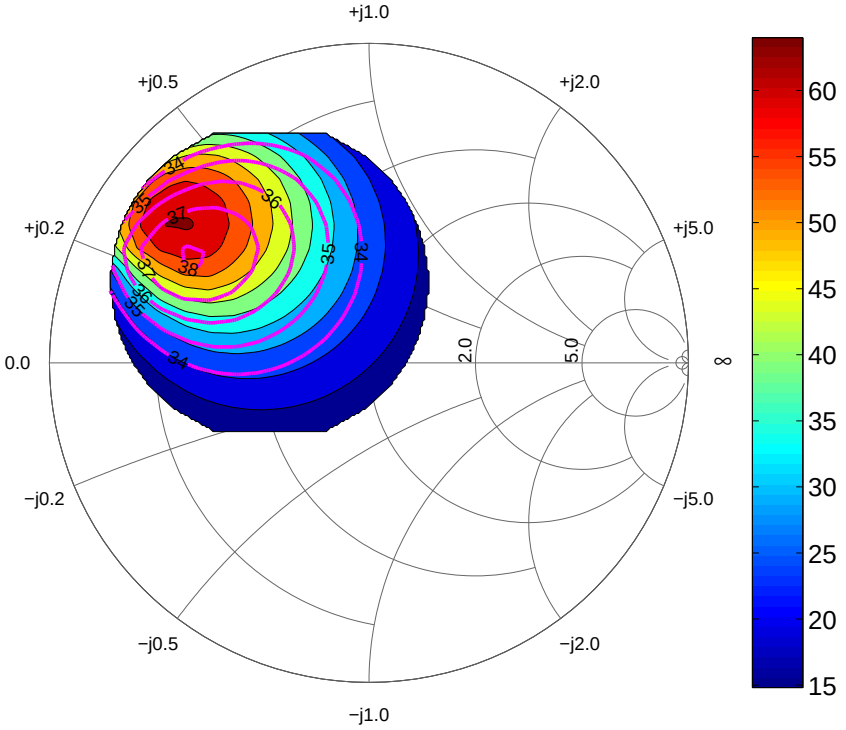


Figure 2.6: Simulated load-pull of the transistor at 6 GHz with 21 dBm of input power. The color bar indicates PAE in percentage and the violet lines show delivered power contours in dBm.

2.4.4 Second harmonic load-pull and source-pull simulations

While load- and source-pulls were experimentally performed to find the optimal fundamental impedances, the second harmonic terminations were fixed on the circuit boards because it greatly simplified the measurement setup, and because the effects of the termination will automatically be included into the characterization. To find the optimal phase angles, the fundamental load and source impedances found from simulations (Chapter 2.4.3) were used and the second harmonic reflection coefficients were swept around the edge of the Smith chart. For the load sweep, the source second harmonic was terminated by a short (180°), and for the source harmonic phase sweep, the load was terminated by a reflection coefficient of $0.99\angle 110°$, both about as far away from their worst case values. These values were determined after some initial simulated load-pull, i.e. the whole procedure is iterative.

Fig. 2.7 shows that PAE and delivered power depend quite strongly on phase of the load termination. It would be beneficial if the amplifier could be designed to operate just at the peaks around 230°, but this would also be the riskiest, since a small discrepancy between simulation and reality could mean ending up in the deep dip around 290°.

For lower input powers, the PAE and gain are not affected as much between different harmonic terminations (i.e. the curves are flatter). Fortunately, the location of the peaks and

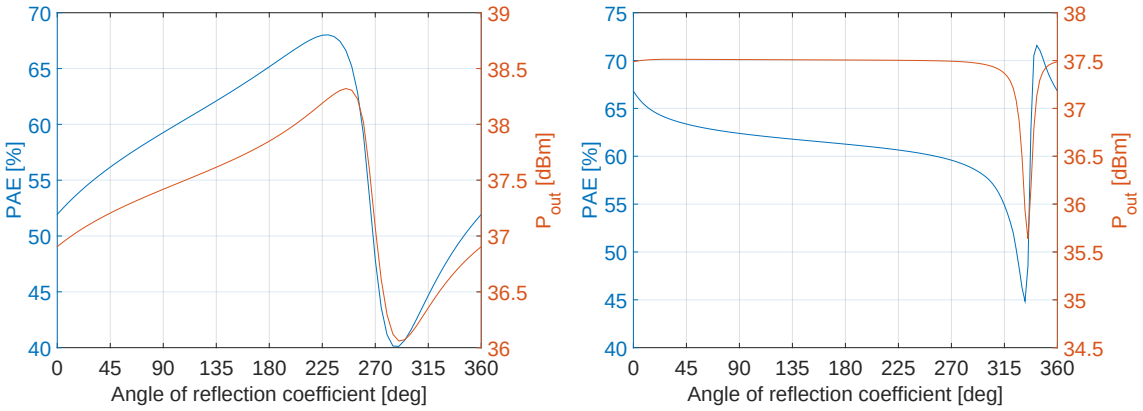


Figure 2.7: Sweep of the phase of the second harmonic termination for the load (left) and source (right). The input power was 21 dBm.

valleys remained at practically the same phase angles regardless of input power. Furthermore, they were also relatively insensitive to changes in the fundamental load impedance. It can also be seen that the second harmonic source termination is not as important, with the delivered power (and gain) being almost entirely flat except for a narrow dip. The narrow peak in the PAE as function of harmonic source impedance is considered unusable. Note that it is significantly narrower than the peak in the PAE for the harmonic load termination.

2.4.5 Test boards

Since the load-pull and source-pull will only done on the fundamental, the second harmonic reflection coefficients were controlled by the test boards. As shown in the previous section, the performance varies considerably versus the phase angles of the second harmonic load and source terminations. However, a higher performance would be associated with a higher risk of failure, which would not be correctable because of the fixed nature of the boards. Therefore three versions of the board were created, with different trade-offs.

To present a high reflection coefficient at a certain phase angle to the device, a quarter wave (at 12 GHz) open stub was designed. This presents a short circuit at the point where it is connected to the circuit, so the length of the transmission line between it and the transistor is chosen such that the reflection ends up at the desired angle. Such stubs were included on two of the test boards.

The three boards are shown in Fig. 2.8. The main difference is the length of the transmission line at the drain. The **"SAFE"** board is designed such that the phase of the second harmonic reflection coefficient is 147°, far away from the worst case value of about 290°. This required a rather long transmission line to make an almost complete rotation around the Smith chart, since otherwise, the transmission line would be so short that the 12 GHz quarter wave stub would not fit.

The **"SHORT"** version is similarly far away from the worst case value (although a bit more risky) at 158°. In this version, the open circuited stub is skipped, and the second harmonic short is only created by the bias line. It also shorts 12 GHz, at the junction

between the bias feed line and the drain transmission line, since the quarter wave line at 6 GHz becomes a half-wave line at 12 GHz. For this version, the length of that line was also tuned for this purpose. This resulted in a slightly shorter line, which is visible in the figure. However, the short is not as good, since it relies on the decoupling capacitors being reasonably shorted at 12 GHz and the bias line has higher losses due to its length and thinness. Additionally, the long electrical length also makes the short less wideband. Simulations indicated that the performance of this version should be better than the "SAFE" version, probably as a result of less microstrip loss and a harmonic termination which is closer to the peak.

By controlling the transmission line length to achieve a near-optimal second harmonic impedance, the **"RISKY"** board was created. The phase is about 200°, so the margin of error is smaller. Unlike the other boards, the source termination also differs. The transmission line at the load side is shorter, but the same length was instead added at the source side, which made the source reflection coefficient slightly more risky as well as conveniently preserving the outer dimensions of the "SAFE" board.

Initially, a stub for harmonic termination was also present on the source side, but simulations indicated that the fundamental input impedance would in those cases become undesirable and the stability was also worsened. The simulated magnitude of the input reflection coefficient would have had to be over 0.9 for a conjugate match. This high magnitude would perhaps be unreachable by the tuners. For these reasons, the stub was not included on the source side and the harmonic reflection coefficient is only controlled by being shorted to ground through capacitors at the DC feed point[1]. This results in a lower magnitude for the second harmonic reflection coefficient at the gate of 0.90. Anyway, the stub would have been located behind the RC stability network, which introduces losses and therefore the magnitude would still not have been as close to one as on the load side.

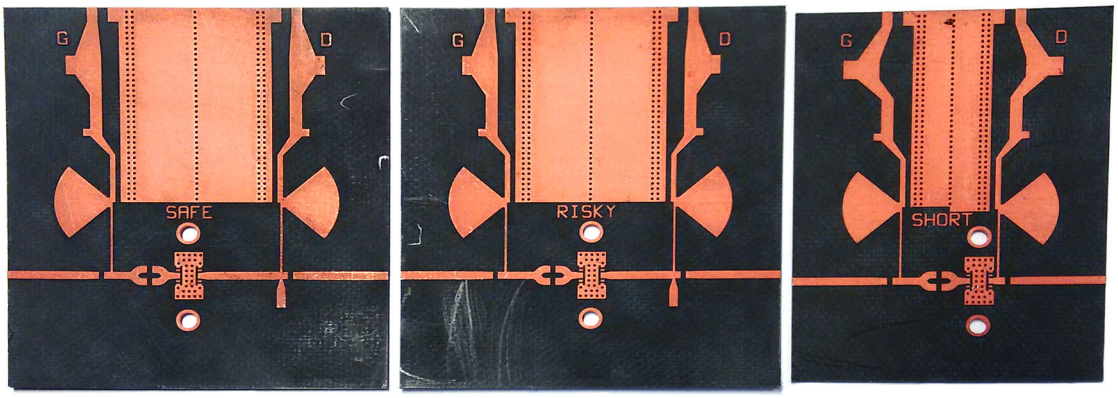


Figure 2.8: The three test boards before assembly. (The non-straight appearance of the edges, especially visible in the right board, is just a result of lens distortion).

Aside from these three boards, a fourth board consisting only of the transistor with transmission lines to connect it to the test fixture was manufactured. This was to be used with external bias tees in case something did not work as expected with the other boards.

[1]The quarter wave line in the bias tee is very nearly half a wavelength at the second harmonic, thus "invisible" and therefore shorts the second harmonic there as well.

2.5 Measurement setup

A passive load-pull setup was built for the characterization. An overview of the setup is shown in Fig. 2.9. Two power meters were used to measure the input and output power levels, by using directional couplers. An amplifier was added between the signal generator and the rest of the setup to achieve a higher input power. Tuners are placed on both the input and the output, to vary the source and load reflection coefficients seen by the DUT. The measurements were done at different planes of reference than the DUT plane. In this section, the setup and de-embedding procedures will be explained in detail.

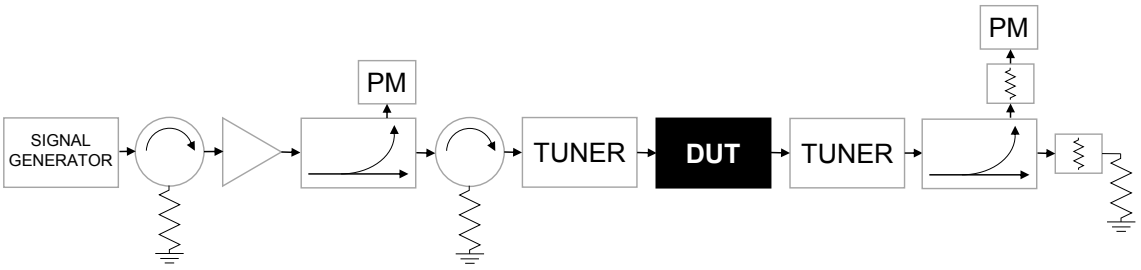


Figure 2.9: Characterization setup for load-pull and source-pull measurements.

2.5.1 Tuners

The tuners were MT982B01, manufactured by Maury Microwave. These tuners basically consists of a transmission line with movable probes. The distance of the probes to the transmission line can be varied, as can the position of the probes along the line [13]. The former affects the magnitude of the reflection coefficient, and the latter affects the phase. They were controlled by specifying the probe locations, as opposed to specifying a given reflection coefficient[2]. Therefore, a VNA (Agilent E8361A) was used to pre-characterize the tuners for a large number of states. The process was repeated after all measurements were completed to verify that the reflection coefficient for a given tuner state is repeatable with insignificant variation.

2.5.2 Tuner characterization

The S-parameters of the tuners are needed, both for calculating the delivered power levels (see Chapter 2.5.5) and for knowing what load and source impedances are seen by the DUT. Each tuner (including relevant adapters) was measured both by itself as a two-port (needed for power de-embedding) and as a one port terminated by the actual circuit elements from the measurement setup, see Fig. 2.9. This was done because the impedances seen looking into the tuners in the one port measurement are the actual ones that are presented to the amplifier under test. However, simply taking S_{11} (or S_{22}) from the two-port measurement would have assumed that the coupler, dummy load and the isolators present highly accurate $50\,\Omega$ loads, which would degrade the accuracy.

[2]The driver software does have a functionality to synthesize a given reflection coefficient if properly supplied with data from pre-characterization [14], but in this project it was unnecessary to set it up this way.

2.5.3 VNA Calibration

For the one port measurements of the tuners, a standard short-open-load calibration was performed. The two-port measurements needed a more complicated calibration. The different ports had incompatible connector types (2.4 mm and 3.5 mm), meaning a single calibration kit containing short-open-load-thru standards could not be used, and no defined thru standard was available. In this case, there are two calibration options available, which are Unknown Thru (also known as short-open-load-reciprocal, SOLR) and Adapter Removal [15]. The last method is cumbersome, since it involves making two separate full two-port calibrations with the adapter mounted on each end. On the other hand, SOLR uses only one set of normal one port calibrations, and many two-port devices can be used as the thru, provided some basic requirements are met [15], [16]:

- It needs to be reciprocal.
- The losses should be less than 40 dB.
- The electrical length needs to be known within $\pm\frac{1}{4}$ wavelength.

The two first requirements are easily met with any adapter. The third requirement is only needed to resolve an internal sign ambiguity for the calibration, and since a 180° span is allowed, accuracy is not needed [16].

2.5.4 Fixture de-embedding

The measurements were done at different planes of reference than the wanted reference plane at the DUT. This section describes how the power levels and the reflection coefficients were shifted to these planes.

2.5.4.1 Load and source reflection coefficients

The reflection coefficients looking into the tuners were measured, but what is of interest is naturally the reflection coefficients seen at the desired plane of reference, which is on the outer edge of the coupling capacitors. This has been illustrated in Fig. 2.10. The de-embedding should remove two blocks on each edge: one is the long microstrip line on the PCB going from the capacitor to the board edge, and the other is the fixture itself.

For the microstrips, EM simulations in Momentum were used to find the S-parameters, which are expected to be highly accurate because of the simple geometry of these parts. The fixture had previously been characterized in-house, and therefore its S-parameters were already available.

After obtaining the network parameters, the two blocks that exist between the DUT plane and the measurement plane can be merged easily using ABCD matrices to obtain a single block, illustrated in Fig. 2.11.

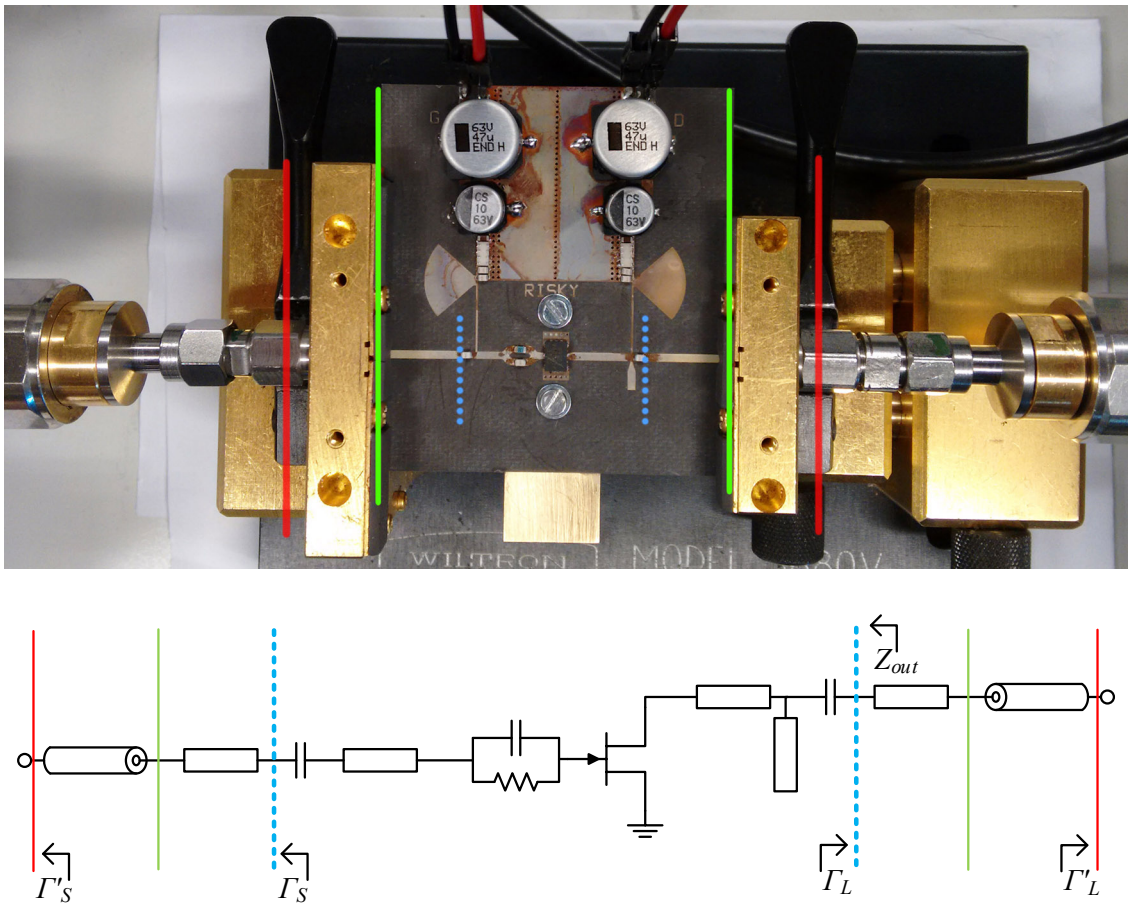


Figure 2.10: Simplified schematic and desired reference planes drawn as dashed blue lines (DUT plane). The red lines show the impedance measurement reference plane. The solid green lines represent the extent of the circuit board.

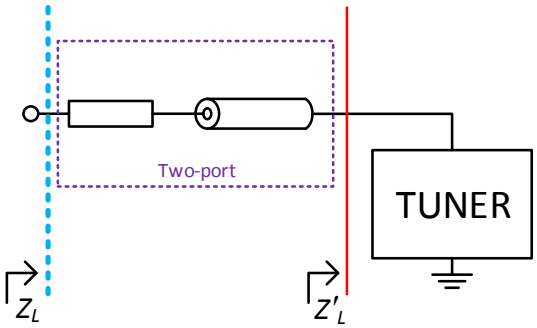


Figure 2.11: Output impedance de-embedding. The output transmission lines (microstrip and fixture connector) can be merged into one two-port terminated by the tuner.

The load impedance seen at the DUT reference plane, Z_L, is directly given by using the formula for the input impedance of a terminated two-port [17],

$$Z_L = z_{11} - \frac{z_{12}z_{21}}{z_{22} + Z'_L} \tag{2.1}$$

where z_{ij} are the Z-parameters for the two-port. Similarly, this also applies to the source tuner.

2.5.4.2 Output impedance

The output impedance of the class C amplifier in the off-state is also needed for the design. It was measured with the VNA connected to the output of the fixture, through an attenuator (to prevent damage in case of oscillations[3]). The input was terminated with a 50 Ω load.

The same two blocks as in the previous section are located in reverse order between the DUT reference plane and the measurement plane. However, the difference is that now the impedance looking into the whole system is known, but not the terminating impedance, which is sought after. Therefore (2.1) is rearranged and ports one and two are interchanged to give

$$Z_{out} = -\frac{z_{12}z_{21}}{Z_{measured} - z_{22}} - z_{11} \tag{2.2}$$

2.5.5 Power measurement and calibration

The power level on the output side may reach approximately +40 dBm. Because the absolute maximum allowed input power for the power meters is +23 dBm [18], a 20 dB attenuator was used on the output side. When this is combined with the 20 dB coupler, the resulting power level will leave a good margin of safety.

The reading from the power meters will not directly correspond to the power levels at the DUT reference planes because of losses in the couplers, attenuators, tuners and adapters. The characteristics of these components were measured separately using a VNA and corrected for.

Besides losses, there will also be small reflections along the signal path. To measure these, bidirectional couplers would be needed. Nevertheless, since the desired figure of merit is the transducer power gain G_T, the data provided from unidirectional couplers is sufficient. G_T is the ratio of the delivered load power and the available source power [19], which means that no knowledge is needed about the reflected power at the input side or any reflections from the load. The placement of the couplers is such that ideally no power would be reflected anyway.

2.5.5.1 Calibrated input power

To find the available source power from the tuner, first the power entering the isolator is needed. Since the coupler is matched at every port, the calculation is straightforward and simply depends on the magnitudes of the transmission coefficients. The S-parameters of the isolator and tuner, which were measured together as one block, can then be used to calculate the available power to the DUT.

S_{31} and S_{21} of the coupler, illustrated in Fig. 2.12, were measured using a two port VNA. This was done in two steps, by terminating the unused port with 50 Ω. The power at the thru port, P_{THRU}, can be found from (2.3).

[3] Oscillations would be highly unexpected in the off-state, but because the results could be disastrous in this case, an attenuator was preferred.

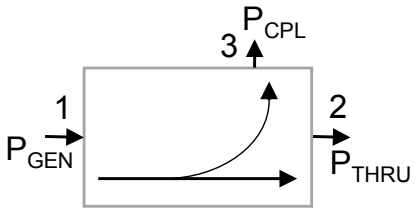


Figure 2.12: Directional coupler at input.

$$P_{THRU} = |S_{21}|^2 P_{GEN} = \frac{|S_{21}|^2 P_{CPL}}{|S_{31}|^2} \tag{2.3}$$

The power leaving the coupler is now known, but $|S_{21}|^2$ of the isolator and tuner (see Fig. 2.9) does not represent the loss of the tuner since it will generally not see a 50 Ω environment. Instead the available power gain[4] G_A can be used, since this applies generally to two port networks. The S-parameters in the following two equations refer to the input tuner and isolator (characterized together as one unit).

$$G_A = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2(1 - |\Gamma_{out}|^2)} \tag{2.4}$$

where

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.5}$$

as shown in [19]. This is the power that would be delivered into a conjugate matched load [19], and therefore the available power to the DUT. To truly refer everything to the plane at the coupling capacitor, the calculations also included the parameters for the fixture and input microstrip in the S-parameter two-port block to remove their effects, although they were nearly ideal. The complete relationship between the meter reading and DUT input power is thus

$$P_{in} = G_A \frac{|S_{21}|^2 P_{CPL}}{|S_{31}|^2} \tag{2.6}$$

where P_{CPL} is the meter reading.

2.5.5.2 Calibrated output power

The input of the coupler should represent an almost perfect 50 Ω load (although it was not verified with the actual dummy load, the coupler itself had a return loss better of around or better than 30 dB at the frequencies of interest when terminated by a non-precision 50 Ω load), so using the unidirectional coupler to measure only the forward travelling wave should be an accurate way of measuring the delivered power to the dummy load. However, losses in the tuner, attenuator and coupler needs to be calibrated out. Fig. 2.13 shows how powers and ports are defined in this section.

The coupler was characterized together with the attenuator. The transmission parameter between the input port and the output of the attenuator (connected to the coupled port). Since the impedance looking into the coupler can be assumed to be 50 Ω, the attenuation

[4] G_A is naturally not an actual gain above unity for this passive device.

is simply the square of the magnitude of the transmission coefficient.

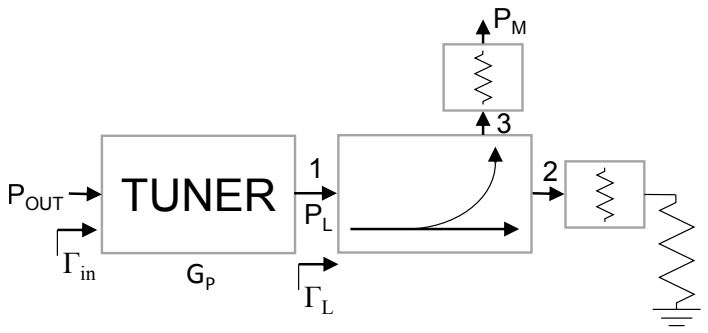


Figure 2.13: Tuner and coupler on the output side.

Since the S-parameters of the tuner are known, power delivered from the DUT can be calculated from the now known power that entered the coupler. Because the tuner can be treated like any two-port network, the operating power gain formula can be used to find what loss it introduces. It is defined in [19] as

$$G_P = \frac{P_L}{P_{OUT}} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} \tag{2.7}$$

where

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{2.8}$$

The S-parameters in these equations refers to the tuner. Notice that G_P is independent of the source impedance [19], which means it is not necessary to know the output impedance of the DUT. Γ_{in} is the input impedance of the output tuner, which reduces to S_{11} in this case because the network is terminated with a matched load ($\Gamma_L \approx 0$). This reduces G_P to

$$G_P = \frac{|S_{21}|^2}{1-|S_{11}|^2}. \tag{2.9}$$

Once G_P was found for each tuner state, the power entering the tuner from the fixture is related to the power entering the coupler according to

$$P_{OUT} = \frac{P_L}{G_P} = \frac{P_M}{G_P|S_{31}|^2} \tag{2.10}$$

where S_{31} comes from the coupler characterization.

P_{OUT} represents the power delivered at the fixture reference plane. Some power is also lost in the fixture and the 50 Ω transmission line, and this is also compensated for using the same set of equations.

3

Characterization results and discussion

This chapter summarized the findings from the measurements. Of the three test boards, the "RISKY" version was the best performer, thus it was selected for the final design. Therefore, data in this chapter refers to this version unless otherwise stated.

3.1 Bias sweeps

The first set of measurements that was performed was gate bias voltage sweeps. Aside from serving the purpose of testing basic instrument control, they also provide information on how to bias the device. The drain voltage was kept fixed at 40 V.

3.1.1 Measurement results

Drain current as a function of gate bias voltage for three different transistors (one on each version of the board) is shown in Fig. 3.1.

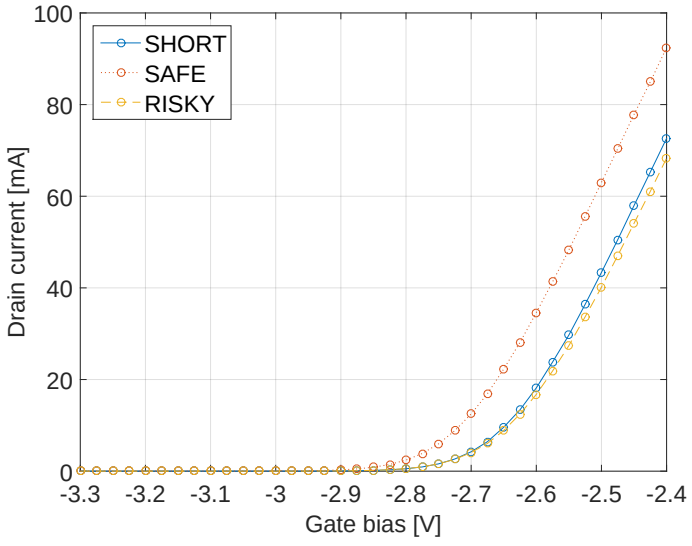


Figure 3.1: Bias sweeps of the three transistors used on the test boards.

3.1.2 Bias point selection for class B cell

Since the pinch-off voltages differed somewhat between the simulation and all the measurements, the gate bias voltage of the physical device was selected mostly based on quiescent

current. In table 3.1, the numerical values are shown. In later RF power sweep measurements, it was verified that the selected point is indeed suitable for the class B cell and a suitable bias point for the class C cell was determined.

Table 3.1: Bias points that were evaluated (for the "RISKY" version).

V_{GS} [V]	I_{DS} [mA]
-2.65	8.9
-2.70	4.1
-2.75	1.6

Based on power sweeps (as those shown in Chapter 3.4), the −2.65 V point was selected, since deeper bias points resulted in the gain dropping much at low power levels. This is a slightly deeper bias than the 12 mA that was used in the simulations.

3.1.3 Class C gate bias

To help find a suitable bias voltage for the class C amplifier, RF input power at a fixed level was applied while sweeping the gate bias voltage. At this stage, approximate load and source impedances had been selected.

The goal is to find the voltage where the amplifier would switch on when the power would be on the threshold of the Doherty region, in this case being designed for being located at 9 dB output back-off. This means in effect that the C cell should switch on when the output power from the B cell is 6 dB below its peak value (since 50 % of the power should come from each amplifier, the final 3 dB). The input power in this measurement was 14.2 dBm, a number found to be suitable by analyzing the power sweeps of the B cell (Chapter 3.4).

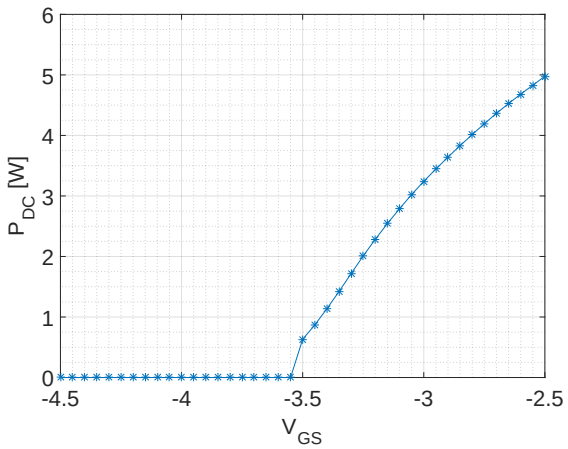


Figure 3.2: DC power consumption for a fixed input power level while sweeping V_{GS}, for finding the point at which the amplifier shuts off.

The sharp drop below −3.5 V is caused by the power supply rounding currents below 15 mA to zero (this instrument was not used to measure current in the previous sections, where greater accuracy was needed). The device was assumed to be switched off at −3.6 V, as can be found by visually extending the curve downwards. This would become the selected bias voltage for the auxiliary cell, but in personal communication with Dr. Mustafa Özen

it become known that the auxiliary amplifier would switch on too early with this voltage, due to some power from the main cell leaking through the feedback capacitance of the auxiliary transistor. Therefore, the actual voltage should be selected as somewhat lower. By reducing it by one volt, the selected bias voltage then becomes −4.6 V. This may be optimized after the Doherty PA has been completed.

3.2 Load-pull

Load-pull measurements were performed for a wide range of power levels. Fig. 3.3 shows the de-embedded results from the high-power case (output power of 5 W at its peak) using class B biasing. For this figure, the actual input power was 22.7 dBm.

Note that the impedances referred to in this section are the ones seen from the desired plane of reference, the coupling capacitors (see Fig. 2.10). In all cases, the transducer power gain is shown by the overlaid magenta lines, with a contour interval of 0.5 dB. The power added efficiency is shown by the filled contour plots.

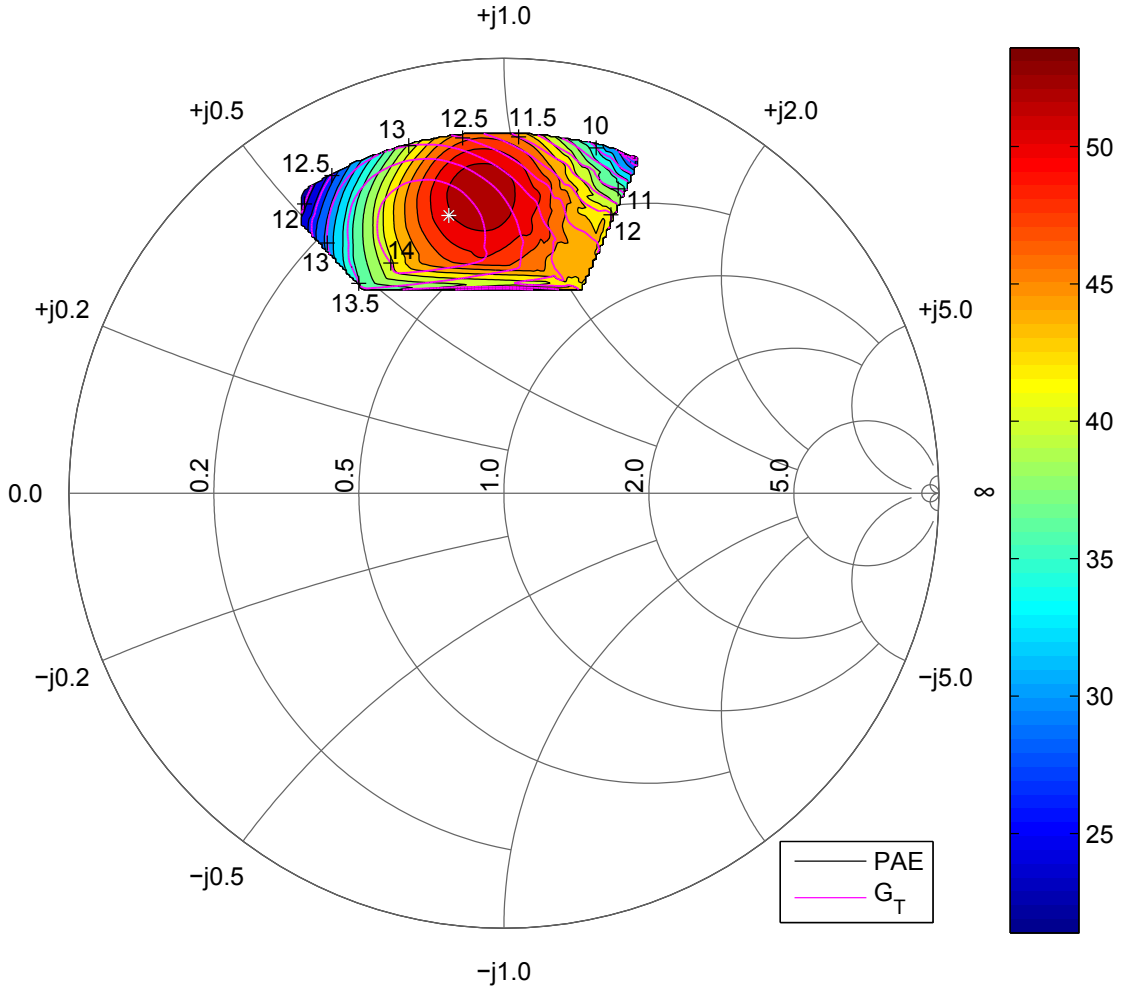


Figure 3.3: Load-pull at high power for the main amplifier. The PAE contour interval is 2 percentage points.

The chosen impedance is marked with a white asterisk. The value was selected as a trade-

off between PAE, gain linearity and gain. As with the rest of the selected impedances in this section, their numerical values are summarized in Chapter 3.8.

Fig. 3.4 shows load-pull results when the output power was backed off by approximately 6 dB compared to Fig. 3.3 (for a targeted final output back-off of 9 dB for the complete amplifier). In this case, the input power was 13.4 dBm. Notice that the optimal load reflection coefficient moved to a higher magnitude.

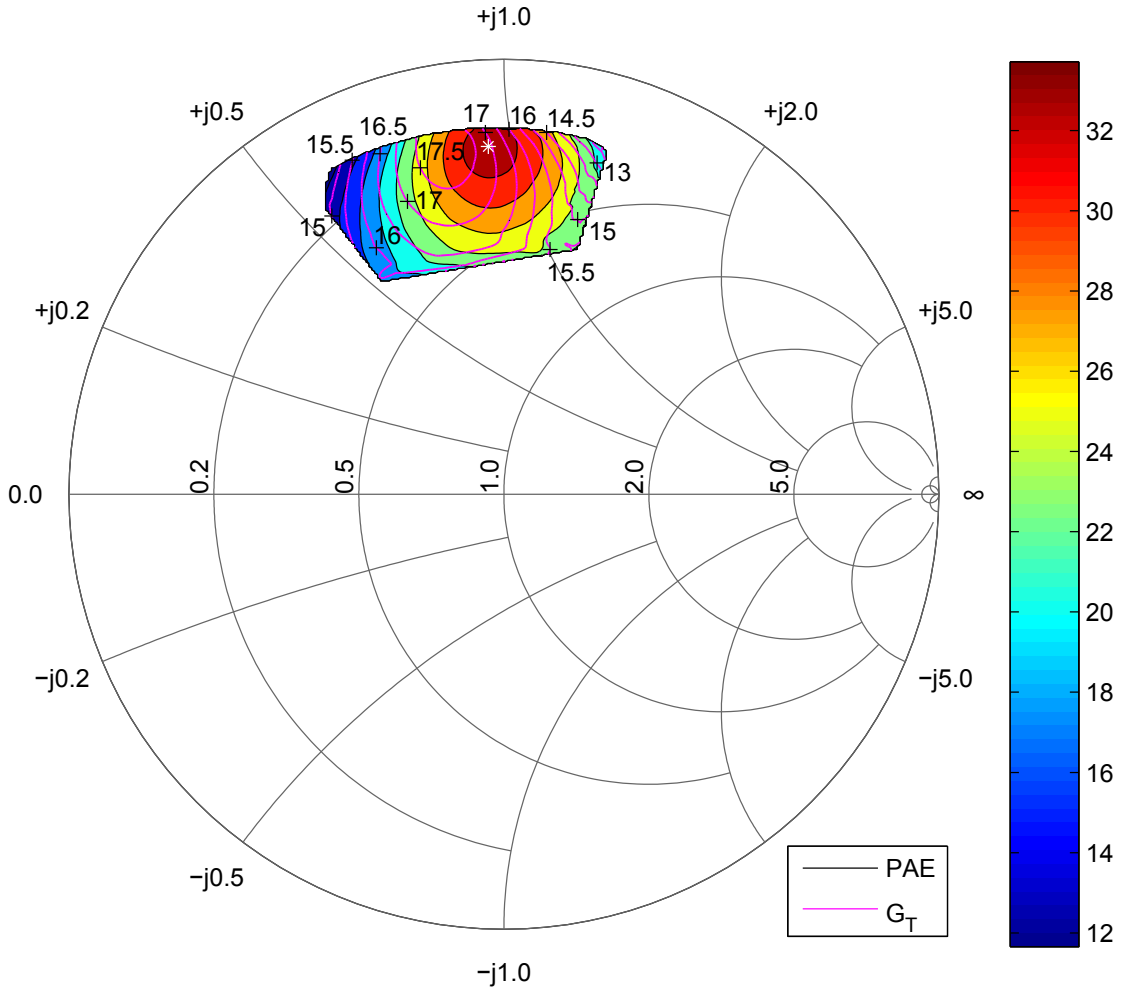


Figure 3.4: Load-pull at back-off for the main amplifier. The PAE contour interval is 2.5 percentage points.

Fig. 3.5 shows a class C load-pull measurement with $V_{GS} = -4.2\,\mathrm{V}$. This is slightly less deep than the $-4.6\,\mathrm{V}$ which was later selected (see Chapter 3.1.3), but the dataset for that bias point was too small[1] to make a clear figure. In either case, the end results were very similar with regards to the location of optimal loads, but with the deeper biasing naturally having lower gain. The input power for this figure was the same as for the full power class B plot, 22.7 dBm, which was chosen with the goal of using an equal power splitting ratio in the final amplifier for simplicity (see Chapter 4.1).

[1]Performed only in a small region around the center of the plot to save time (the center was already known from previous measurements by then).

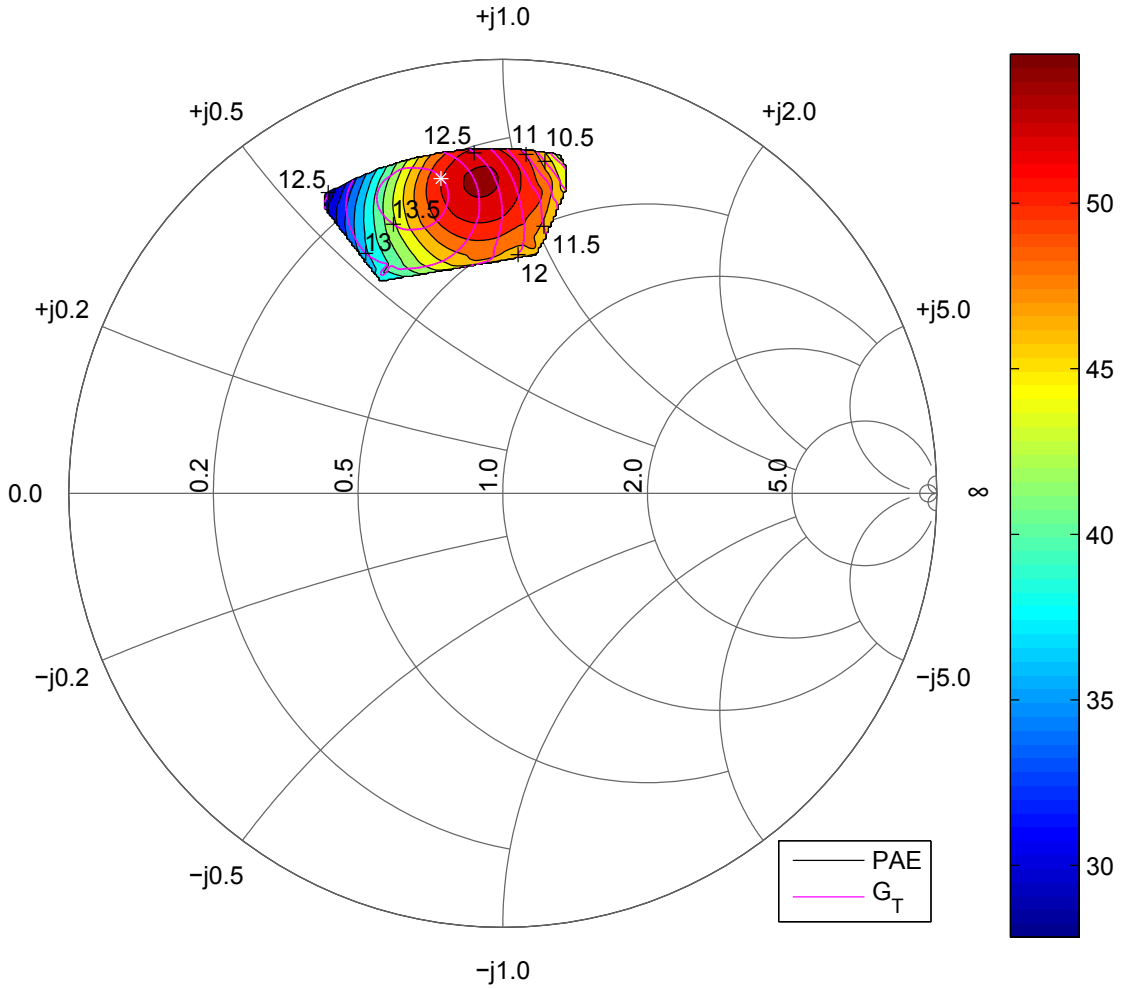


Figure 3.5: Load-pull with class C biasing, for the auxiliary amplifier. The PAE contour interval is 2 percentage points.

A general observation is that the optimal load impedances did not vary much when changing the biasing, but they did vary with the power level. This is behavior is different from the optimal source impedance, as shown in the next section.

3.3 Source-pull

As with the load-pull measurements, source-pull measurements were performed for a range of power levels and bias points. However, it is more complex to interpret the results, because the state of the source tuner not only affects the impedance seen by the DUT, but also its own losses and therefore the input power to the device. The losses were higher for higher reflection coefficients, about 1.7 dB higher for $|\Gamma| = 0.8$ than for $|\Gamma| = 0.5$. Since the main goal is find the source matching by looking at where the gain peaks, it is important to have a constant input power, since otherwise, the amplifier would be driven into compression by varying amounts, which would skew the results by changing the gain.

This means that unlike the load-pull measurements, looking at a single set of values having a constant generator power level would be misleading. For this reason, the power was

stepped in fine steps (down to 0.33 dBm[2]) and after de-embedding the true input power, a set of values having a roughly constant *true* input power could be plotted.

Fig. 3.6 shows the results from this method for the class B amplifier. The contour interval is 0.1 dB. The source-pull was performed for both the full power and back-off cases, but unlike the load impedance, the source impedance is naturally fixed (not modulated) in the final DPA. It was chosen to optimize the source matching for the high power case, since its gain is lower and thus more valuable there than at back-off (see Chapter 3.8). The difference in optimal impedance in these cases was not large. The white asterisk shows the selected source impedance. The results from the low power source-pull is not shown.

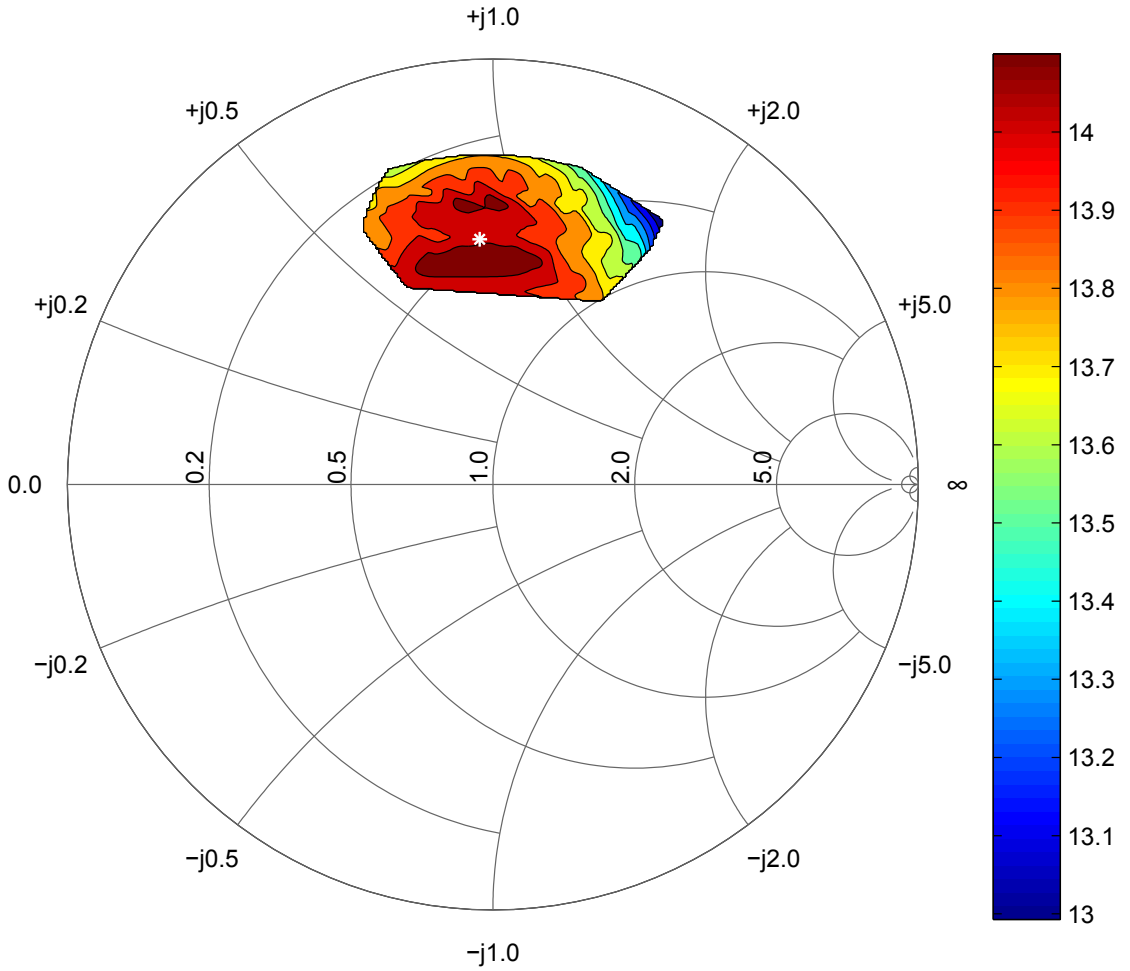


Figure 3.6: Source-pull results for class B biasing. The transducer power gain is plotted when the true input power was between 23.00 dBm and 23.35 dBm.

The source-pull results from when class C biasing ($V_{GS} = -4.6\,\mathrm{V}$) was used is shown in Fig. 3.7. When compared with Fig. 3.6, it can be seen that the location of the optimal source impedance varied greatly. This is as expected, since changing the gate bias voltage affects the AC characteristics of the gate. In this case the contour interval is 0.05 dB.

[2]Even finer steps could have been used for increased accuracy at the expense of measurement time, but since the source matching was found to be less important than the load impedance, this step size was found to be sufficient.

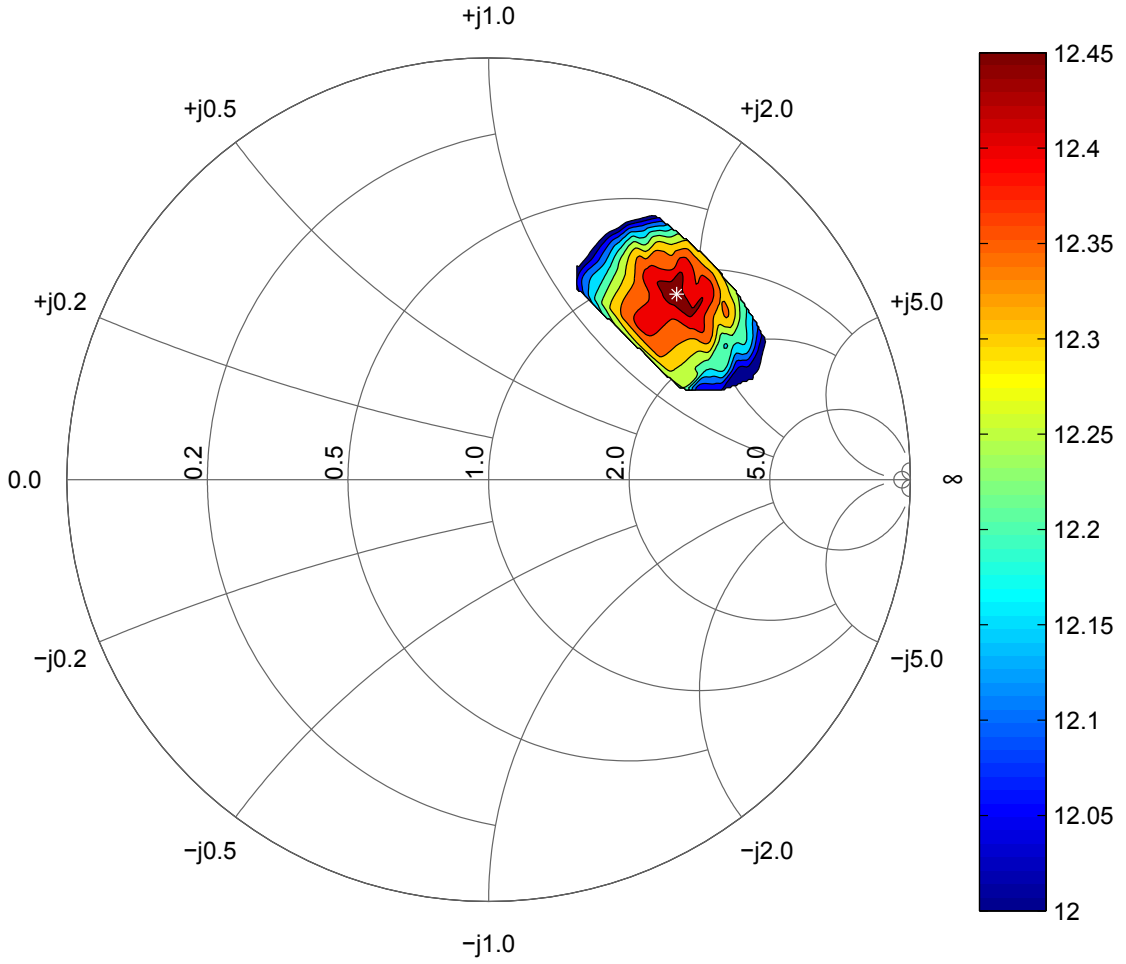


Figure 3.7: Source-pull results for class C biasing. The transducer power gain is plotted when the true input power was between 23.00 dBm and 23.33 dBm.

An observation from the load-pulls and source-pulls is that the source impedance does not matter as much as the load impedance. For example, if the source match would be shifted so that the gain drops by 1 dB, the corresponding shift on the load side would cause the gain to drop by several dB.

When compared with simulated values, the load-pull results agreed quite well, but the source matching did not.

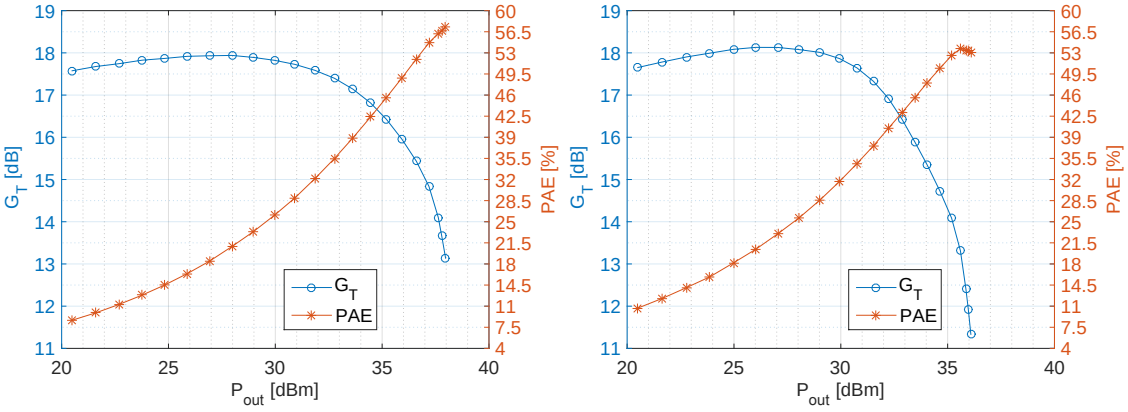
3.4 Power sweeps

In Fig. 3.8, the power was swept and the performance recorded. The selected load impedances here are very close to the ones that were finally selected, although not exactly the same[3].

The data comes from pulsed measurements, with the pulses being about 1.5 s long with a 10 % duty cycle. This meant the transistor was warmer for the higher power levels, and

[3] An interpolated point was selected for the high power case.

heat was observed to slightly degrade the gain. This signifies that the gain at low power levels, which is high, would have been slightly lower if the temperature had been the same.



(a) Optimized for high power

(b) Optimized for back-off

Figure 3.8: Power sweeps using approximately final load and source impedances for class B.

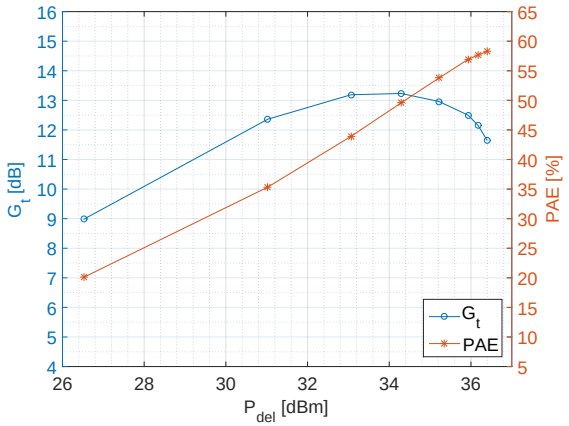


Figure 3.9: Power sweep for class C. Note that the scales are different. When the power level is decreased further, the device soon shuts off.

3.5 Off-state class C output impedance

The output impedance was measured for a range of class C biases, shown in table 3.2. For these large negative biases, the impedance was practically constant.

Table 3.2: De-embedded output impedance for several class C bias points.

V_{GS} [V]	Z_{out} [Ω]
−4.0	$8.509 - j51.16$
−4.2	$8.509 - j51.22$
−4.4	$8.568 - j51.37$
−4.6	$8.574 - j51.41$

3.6 Amplifier stability

As known from Chapter 2.4.2, the amplifier is not unconditionally stable. However, from the measurements, the transistor was found to be more stable than the simulations indicated. When the tuners were connected, reflection coefficients above 0.9 at multiple phase angles could be presented to the device without any sign of oscillations. This might be a result of the gain generally being somewhat lower than simulated. Since the final load and source reflection coefficients have magnitudes significantly below 0.9, the final device is expected to be stable with a good margin of tolerance. Oscillations were only observed when no load or source terminations were connected at all, a case where the magnitude of the reflection coefficients is expected to be close to one.

3.7 Tuner repeatability

In addition to being pre-characterized, the tuners were also characterized after all other measurements were complete, to verify the reproducibility of the tuner characteristics versus tuner state. Table 3.3 shows the measured differences of the source and load reflection coefficients at 6 GHz. The measurements were taken several weeks apart.

Table 3.3: Average and RMS differences between measured tuner characteristics before and after the device characterization.

Tuner	Positions	Avg. magnitude	Avg. phase	RMS magnitude	RMS phase
Load	600	0.0120	0.14°	0.0123	0.16°
Source	378	0.0048	0.50°	0.0053	0.53°

These are considered very good results and no further consideration regarding tuner repeatability needed to be taken.

3.8 Summary of selected impedances

The optimal load reflection coefficients were determined from the load-pull measurements. For the class B cell, the reflection coefficient for the full power case was not selected as an exact measurement point. Instead it was a trade-off between two adjacent samples. This was done since it was judged to give a better PAE versus gain flatness trade-off.

Tables 3.4 and 3.5 give the final reflection coefficients that were selected. For comparison purposes, the values that would result from a simulation where they were selected by similar criteria are also given. Overall, the load impedances are close, but they have some discrepancy, especially for class C operation. The simulated source impedances were markedly different from what was found by measurements.

That there are differences between simulations and measurements is considered a desirable result, because if the results had been in perfect agreement, there would have been no point in carrying out the measurements. Instead, the discrepancies mean that the design approach most likely led to increased accuracy.

Table 3.4: Optimal load impedances determined from measurements, compared to simulated values.

Case	Γ_L	Z_L [Ω]	Simulated Γ_L
B, full	$0.651\angle 101.2°$	$17.2 + j38.1$	$0.739\angle 101.0°$
B, back-off	$0.801\angle 92.7°$	$10.4 + j46.6$	$0.813\angle 90.4°$
C	$0.739\angle 101.1°$	$12.4 + j39.6$	$0.800\angle 99.2°$

The optimal source impedance varied not just between the class B and C biases, but there was also a small variation depending on the power level for the class B cell. Since the matching network is fixed, the impedance that was optimal for the full power case was used, since it only means there will be slightly more reflected power at back-off, which is not a problem since the gain there is plentiful. The net effect was only a reduction of about 0.15 dB of gain at back-off when the source impedance was held at the value optimal for full power, which is considered insignificant.

Table 3.5: Optimal source matching determined from source-pulls, with simulated values as comparison.

Case	Γ_S	Z_S [Ω]	Simulated Γ_S
B, full (used)	$0.577\angle 93.2°$	$23.9 + j41.3$	$0.754\angle 99.5°$
B, back-off	$0.652\angle 98.3°$	$17.8 + j40.0$	$0.796\angle 101.1°$
C	$0.613\angle 45.3°$	$60.7 + j87.9$	$0.798\angle 78.0°$

Perhaps the most significant discrepancy between simulation and measurements is the in the source matching, particularly the difference in the magnitudes of the reflection coefficients. For class C biasing, the phase angle is also markedly different.

4

Doherty amplifier design

This chapter describes the design procedure of the complete Doherty amplifier, based on the characterization data found in Chapter 3. The design of the input matching networks and the power splitter are outlined. The output combiner and the phase shifter will be explained in detail.

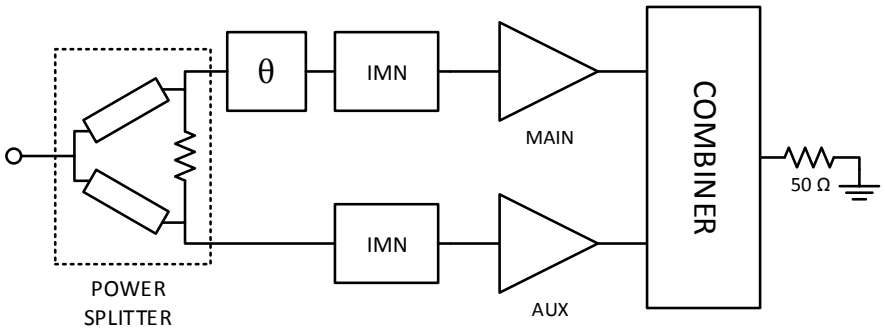


Figure 4.1: Block view of complete amplifier. IMN stands for input matching network. θ represents the phase shifter.

4.1 Power splitter design

A 3 dB Wilkinson power divider is implemented as input splitter. It was used because of its simplicity in design and its good attributes such as isolation and port matching. The power splitter was placed right at the input, before the input matching networks, which is still a 50 Ω environment, which makes its design uncomplicated.

An equal-split Wilkinson divider consist of two $\lambda/4$ transmission lines with characteristic impedances of $\sqrt{2}Z_0$, joined at their outputs with a resistor of value $2Z_0$ [19]. These features can be seen in the layout in Fig. 4.2, where the resistor is to be located between the pads at the outputs. ADS LineCalc was used to find initial lengths and widths of the lines. A problem is that the lines cannot simply be straight and parallel, since they need to join up (with some spacing) at the end, for connecting the resistor. This was solved by making each line shaped approximately like a half-circle. The shape also helps reducing the total length. Internally, each half circle consist of two 90° bends with slightly different diameters, which causes the spacing at the right side suitable for a 0603 resistor.

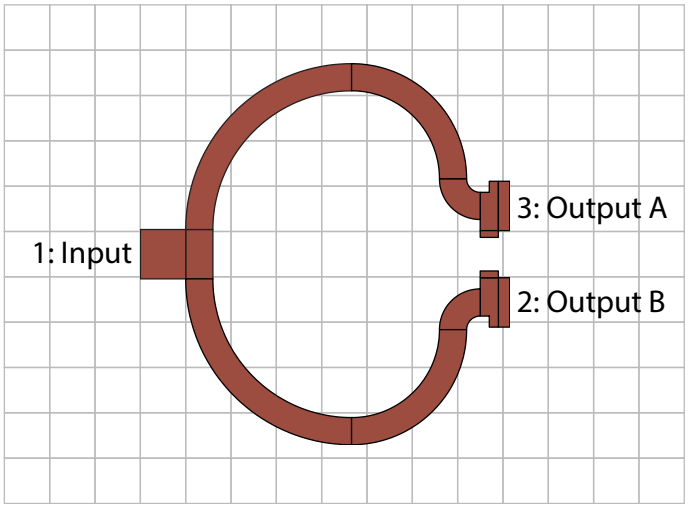


Figure 4.2: Equal-split Wilkinson power divider geometry. Outer dimensions of splitter 7.2x8.4 mm, grid size 1x1 mm.

Initially, the radii of the half-circles were selected so that their arc lengths would correspond to the linear lengths for 90° lines. Optimization with the actual geometry was later carried out to find the optimal radii for centering the power splitters amplitude response on 6 GHz. A Modelitics model from the CLR library is used to simulate the isolation resistor. The pad effects in the model were disabled, since the pads were included in the Momentum simulation in this case.

The performance figures after optimization are shown in Fig. 4.3. The outer dimensions of the splitter itself are 7.2x8.4 mm. For the 5−7 GHz frequency range, isolation and return losses are around or better than 20 dB, and the power lost through the splitter is better than 0.1 dB (aside from the 3 dB that occur because of the power division).

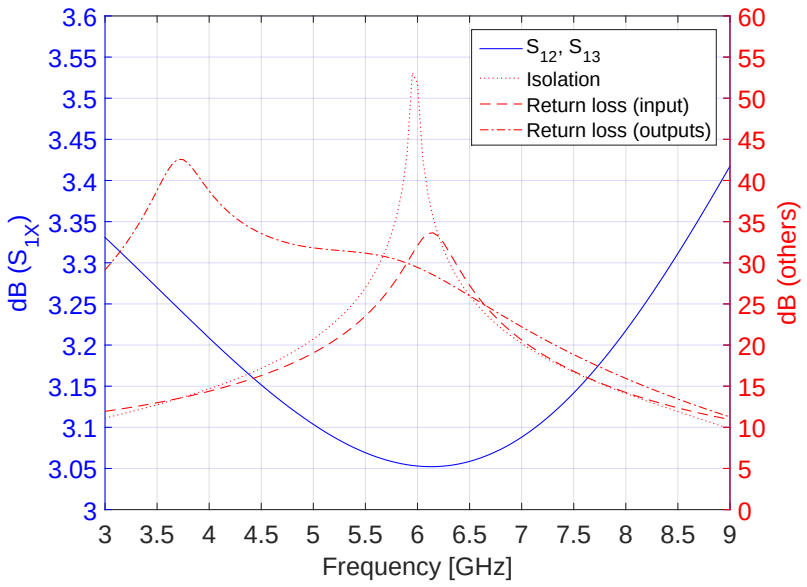


Figure 4.3: Simulated performance of the input power splitter, after optimization.

4.2 Matching networks

Conventional single stub matching networks, see Fig. 4.4, were used to present the desired source reflection coefficient to the transistors, found in Chapter 3. For both amplifiers, a short circuit stub followed by a length of transmission line formed compact networks. Alternatively open stubs could have been used, but this resulted in comparatively long stubs and narrower bandwidths. The topology is shown in Fig. 4.4.

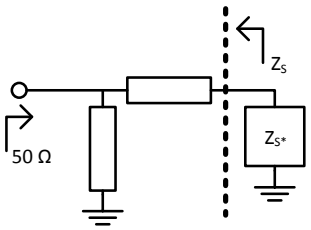


Figure 4.4: Matching network topology for the transistors.

A characteristic impedance of 65 Ω was used for the stubs to reduce the required lengths and thus make the circuit more compact. A 65 Ω line has slightly higher losses per unit of length than a 50 Ω line. However, it also yields shorter lengths and therefore lower losses in the end, according to values obtained from LineCalc. Initially, ideal components were used with values calculated from Smith charts. More realistic models for the T-junction and the ground via were introduced and the values were retuned to bring network parameters back towards the desired values. From the resulting dimensions, layouts were generated and a final optimization could be performed based on EM simulations. The final networks are shown in Fig. 4.5. The outer dimensions of the main and auxiliary matching networks are 2.1x4.3 mm and 4.6x4.1 mm respectively.

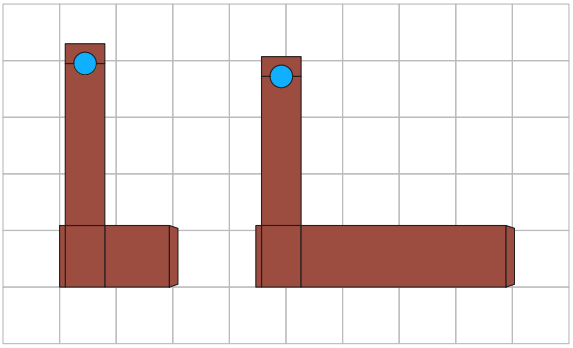


Figure 4.5: Input matching networks for the main amplifier (left) and the auxiliary amplifier (right). The left side of each network is the 50 Ω input. Grid size 1x1 mm.

4.3 Combiner

The combiner design follows several steps. From the point of view of the main and auxiliary amplifiers, the combiner may be viewed as a two-port network containing the load, illustrated in Fig. 4.6 [11]. The S-parameters for this block are determined so that the combiner may be realized as a lossless 3-port, terminated by the actual load, while still presenting the same impedances on its two other ports [11]. This three-port network can be realized as two simple two-port networks [20]. If using lumped components had been a feasible option at this frequency, the two-ports could have been directly realizable by this point, but instead, it is shown how the realization is carried out using only transmission lines.

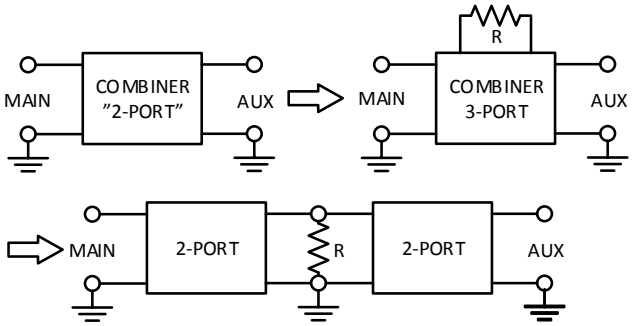


Figure 4.6: Combiner design process, going from a lossy two-port representation of the output combiner to equivalent lossless two-ports terminated by the load. Later, the latter is realized using microstrips.

4.3.1 Required S-parameters

The Z-parameters for the combiner are calculated from the signal's voltages and currents of the fundamental in three different cases, shown in (4.1) [11]. These cases are and their notations are

- Auxiliary cell at peak power, V_{aP}, I_{aP}
- Main cell at peak power, V_{mP}, I_{mP}
- Main cell at back-off, V_{mB}, I_{mB}

The off-state output impedance of the auxiliary cell, denoted as Z_a, is also needed.

Because the measurement setup results in only a power and an impedance, a current and a voltage needs to be calculated from these using (using basic formulas, such as Ohm's law and $P = \frac{\Re\{Z\}I_{peak}^2}{2}$). The method for finding the network parameters does not require knowledge of the phase relationship between the different cases. Phase shift between the *inputs* of main and auxiliary is covered in Chapter 4.4.

Two-port network parameters follows as [11]

$$Z = \begin{bmatrix} \dfrac{I_{aP}V_{mB}C_1 - e^{j2\theta}V_{mP}C_2}{I_{aP}I_{mB}C_1 - e^{j2\theta}I_{mP}C_2} & \dfrac{e^{j\theta}C_1C_2}{C_2e^{j2\theta}I_{mP} - C_1I_{aP}I_{mB}} \\ z_{12} & \dfrac{I_{mB}V_{aP}C_1 + e^{j2\theta}I_{mP}Z_aC_2}{I_{aP}I_{mB}C_1 - e^{j2\theta}I_{mP}C_2} \end{bmatrix} \tag{4.1}$$

where $C_1 = I_{aP}Z_a + V_{aP},\ C_2 = I_{mP}V_{mB} - I_{mB}V_{mP}$ [11].

4.3.2 Determination of phase offset θ

So far, the two-port network parameters are known as a function of phase offset θ as seen from the outputs of the amplifier cells. In this section, the θ value that achieves a full description of the two-port network parameters will be determined.

In order for the calculated network parameters to be realizable as a lossless three port with a resistive termination on one port, the following equation needs to be fulfilled [11]:

$$\Re\{z_{12}\}^2 = \Re\{z_{22}\}\Re\{z_{22}\} \tag{4.2}$$

z_{ij} are all functions of the phase offset θ. Four roots of θ are found from (4.2): {-134.8°, -84.3°, 45.2° 95.7°}. While they should all provide the same efficiency at the efficiency peaks, the first and third solutions have been observed to exhibit poor efficiency between the peaks [20]. This leaves -84.3° and 95.7°. Of these, the former root is selected, because its lower absolute value should translate into a shorter electrical length. The Z-parameters are then found by evaluating (4.1) with $\theta = -84.3°$. The results have been converted to S-parameters, which are shown in table 4.1.

Table 4.1: Required S-parameters for the combiner.

Parameter	Goal
S_{11}	0.898/89.8°
S_{12}/S_{21}	0.290/156.4°
S_{22}	0.515/118.5°

4.3.3 Two-port subnetworks

It is already ensured in the previous section that the combiner can be realized as a lossless network terminated by the load. Although it is possible to empirically design microstrip circuits that meet these S-parameters, there is an analytical approach. The three-port network can be realized as two two-port networks, either Π or T or a combination thereof [20]. Fig. 4.7 shows the possible solutions.

At microwave frequencies, distributed realizations are preferred over the lumped element realizations to achieve lower losses and a better simulation accuracy. Therefore, in the next sections, a method will be presented to convert lumped element realizations in Fig. 4.7 to distributed realizations.

4.3.4 Shunt reactance realization

A purely imaginary shunt impedance can easily be realized by an open or shorted transmission line, for which the characteristic impedance and electrical length determine the apparent reactance [21]. This is illustrated in Fig. 4.8. These equivalents are well known and exact (for a single frequency), and they were used for all shunt reactances.

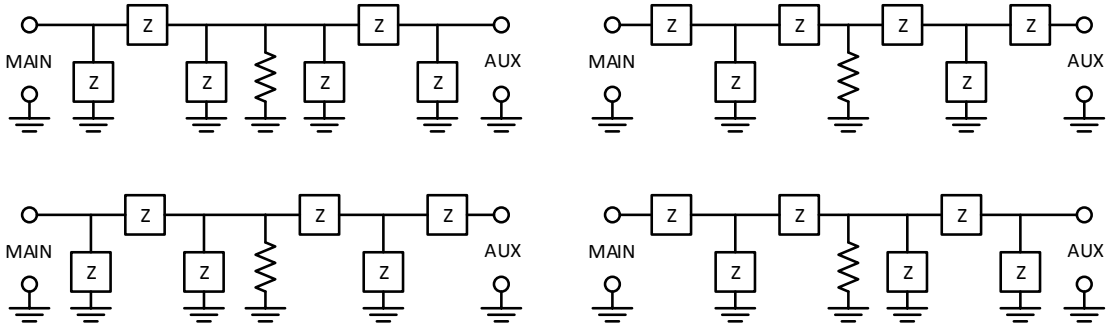


Figure 4.7: The four different combiner topologies. The symbols are used to represent impedances; they are not necessarily of the same value.

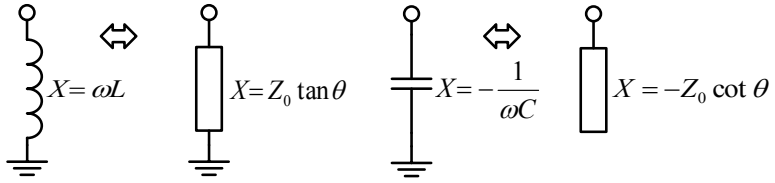


Figure 4.8: Reactive shunt elements can easily be replaced by stubs.

4.3.5 Series reactance realization

Unlike reactive shunt elements, the series reactive components are not straight forward to realize as transmission lines. A series inductor can be approximated with a short high-impedance transmission line, with $X = Z_0 \sin\theta$ [21]. The approximation works better the higher the line impedance is. However, the minimum acceptable line width set an upper limit of the practical characteristic impedance of the line, which was about $100\,\Omega$ in this project for a 0.3 mm wide line. For sufficiently small reactances (roughly below $15\,\Omega$) this approximation was quite good, but no solution consisting only of such low values could be found, and most values were over $50\,\Omega$ were the approximation was not good at all. Thus it would be desirable to use a more general approach.

From personal communication with Dr. Mustafa Özen, it became apparent that it is possible to exactly realize a series reactive element with a series transmission line and two certain shunt impedances. Fig. 4.9 shows the topology. This works for both capacitive and reactive elements, although as later explained, it is more useful in the inductive case.

In (4.3), the ABCD-parameters for the series reactance are set equal to the parameters of the replacement network (right hand side).

$$\begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ jY_0 \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \tag{4.3}$$

Multiplying the matrices on the right hand side and simplifying yields the following matrix equation:

$$\begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} \cos\theta + jYZ_0 \sin\theta & jZ_0 \sin\theta \\ 2Y\cos\theta + j\left(Y^2 Z_0 + Y_0\right)\sin\theta & \cos\theta + jYZ_0 \sin\theta \end{bmatrix} \tag{4.4}$$

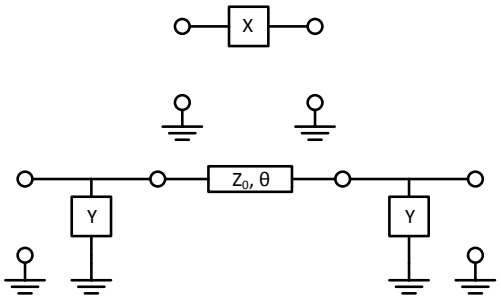


Figure 4.9: The upper network, a series inductance, will be replaced by the lower network, which is realizable using only transmission lines.

The matrix equation above yields the following equations:

$$\begin{cases} jZ_0 \sin\theta = jX & \text{(4.5a)} \\ \cos\theta + jYZ_0 \sin\theta = 1 & \text{(4.5b)} \\ 2Y\cos\theta + j\left(Y^2 Z_0 + Y_0\right)\sin\theta = 0 & \text{(4.5c)} \end{cases}$$

The first condition gives the electrical length of the transmission line, based on the desired reactance X. The characteristic impedance of the line can be selected by the designer. The second condition determines the value of the shunt admittances Y, which depends on the electrical length and the characteristic impedance of the transmission line.

$$\begin{cases} \sin\theta = \dfrac{X}{Z_0} & \text{(4.6a)} \\ Y = \dfrac{1-\cos\theta}{jZ_0 \sin\theta} & \text{(4.6b)} \end{cases}$$

Condition (4.5c) will be automatically fulfilled when the two above conditions are fulfilled. The proof of this is shown in Appendix A.

With these results, series reactive elements can be exactly realized at one frequency, with the reactance allowed to be as high as the highest permissible line impedance, a limit set by (4.6a). In this project, the upper limit was about $100\,\Omega$. Note that with the classical approach, the maximum realizable inductive reactance was only about $15\,\Omega$.

A noteworthy special case for inductive reactance values is when the transmission line is chosen to be 90°. Then the characteristic impedance of the series line (Z_0) and the reactance of the two shunts get the same numerical values as the desired series reactance. The characteristic impedance may be chosen to a higher value, which enables the use of electrically shorter lines than 90° in most cases.

The method works best for replacing series inductors, but it can also be used for capacitors. However, the practical use of this is limited, because very long transmission lines would be needed: If a certain inductive reactance required an electrical length of θ, the corresponding capacitive reactance would require an electrical length of $360° - \theta$, and consequently the match would be very narrowband.

When the series elements in the different combiner topologies (Fig. 4.7) are replaced using this method, the number of elements become rather large. However, many of the shunts end up in parallel, so they can be replaced by a parallel combination of values. As an example, for a combiner consisting of a Π network on the main side and a T network on the auxiliary side, the replacement of equivalent circuits are shown in Fig. 4.10.

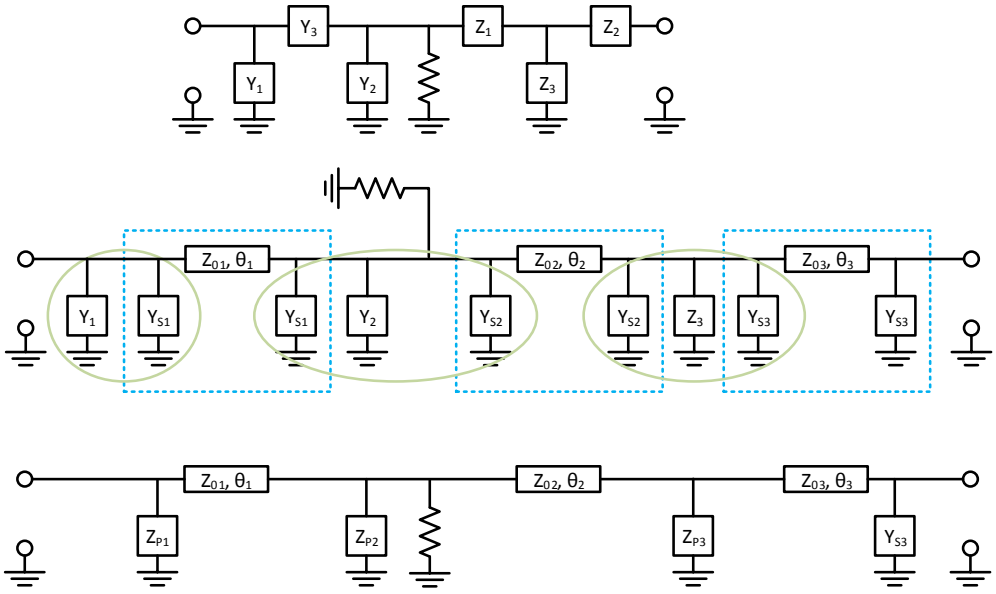


Figure 4.10: Illustration of the conversion process from lumped element network to transmission line network. The dotted rectangles outline the replaced series elements, and the ovals outline elements suitable for parallel combination. The Z-blocks and Y-blocks are used to represent impedances/admittances, they are not all identical. The same applies to the transmission lines.

The remaining impedance blocks are easily replaced by open or shorted stubs, as in Fig. 4.8, yielding a network consisting purely of transmission lines. The other three topologies were also adopted to microstrip using this method.

4.3.6 Realization

Using the previously outlined method, a Matlab script was used to calculate parameters for complete microstrip realizations of the four topologies. This way, it could easily be examined which solutions give dimensions suitable for manufacturing. Many of the solutions contained series capacitors, which were immediately ruled out because of the long transmission lines and narrow bandwidths.

Since the method for deriving the impedances (Chapter 4.3.3) does not require the load impedance to be 50 Ω, it was beneficial to choose a lower value. This tended to give more practical microstrip dimensions for realization. A number of different solutions were simulated in ADS to see how well-performing they were, but the solutions that were examined presented similar losses and RF bandwidths. For the combiner that was finally chosen, a load impedance of 15 Ω was used. This is just the impedance seen by the combiner. The output is still 50 Ω, achieved by the use of a quarter wave transformer.
The method gives straight transmission lines that join up ideally. However, in reality the

circuit has to contain junctions and also bends, since the amplifiers need to line up more or less in parallel, so that their inputs are also close together. While the combiner had the exact S-parameters when ideal components were used, the introduction of junctions, bends, end tapers and ground vias (for some of the stubs) changes this. To correct for it, the changes were introduced one by one and the values were optimized after each change. For the later design stages, EM simulations and optimizations were carried out using ADS Momentum to achieve a good agreement with the desired values. Ultimately, the match was considered practically perfect at the center frequency.

The finished combiner is shown in Fig. 4.11. The outer dimensions of the circuit are 14.5x13.8 mm. In table 4.2, the desired S-parameters are compared to the final values obtained from Momentum simulations. Frequency sweeps were performed during the design process to verify that the S-parameters were not very sensitive to frequency, because such sensitivity would also indicate a poor tolerance to manufacturing variations. The frequency behavior of the combiner is shown in Fig. 4.12.

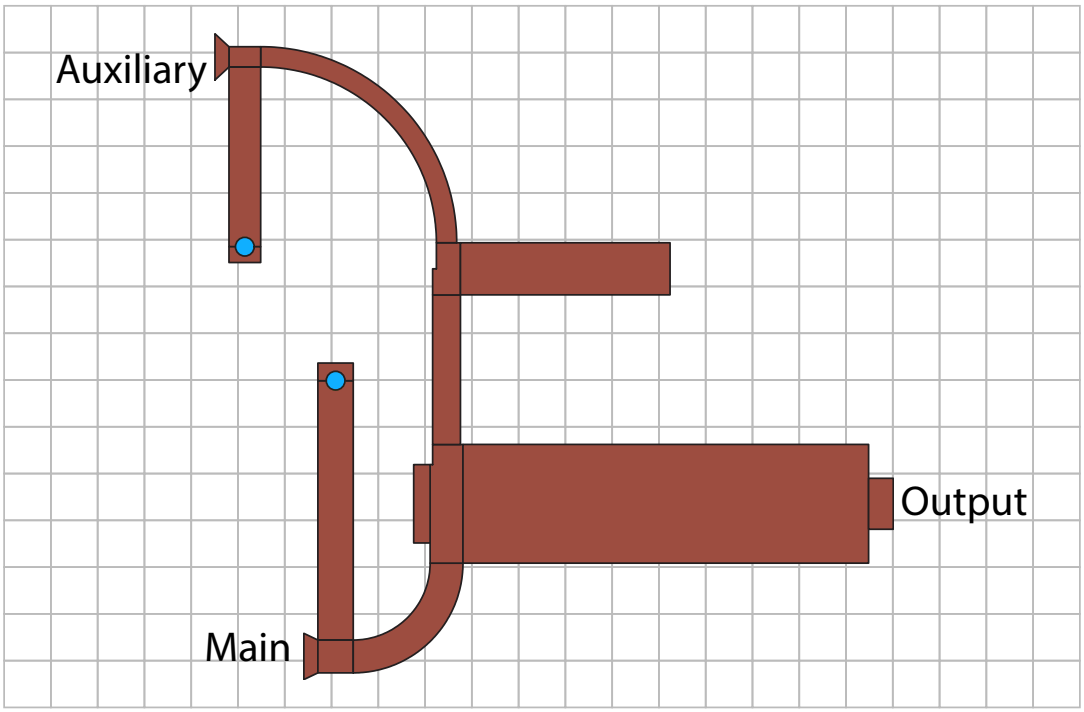


Figure 4.11: Layout of the final output combiner for the 6 GHz DPA, including the quarter wave transformer for 50 Ω output. Outer dimensions 14.5x13.8 mm, grid size 1x1 mm.

It may be noted that the region of good agreement between desired and simulated S-parameters (hundreds of megahertz) is a quite small fractional "bandwidth", but it should be remembered that the optimal S-parameters is a function of frequency as well, so a wideband match here would not necessarily lead to a broadband amplifier.

Table 4.2: Desired and achieved combiner parameters, and the discrepancy presented as a distance in the complex plane.

Parameter	Goal	Achieved	|Difference|
S_{11}	$0.898\angle 89.8°$	$0.880\angle 90.5°$	0.021
S_{12}/S_{21}	$0.290\angle 156.4°$	$0.286\angle 156.8°$	0.005
S_{22}	$0.515\angle 118.5°$	$0.527\angle 119.6°$	0.016

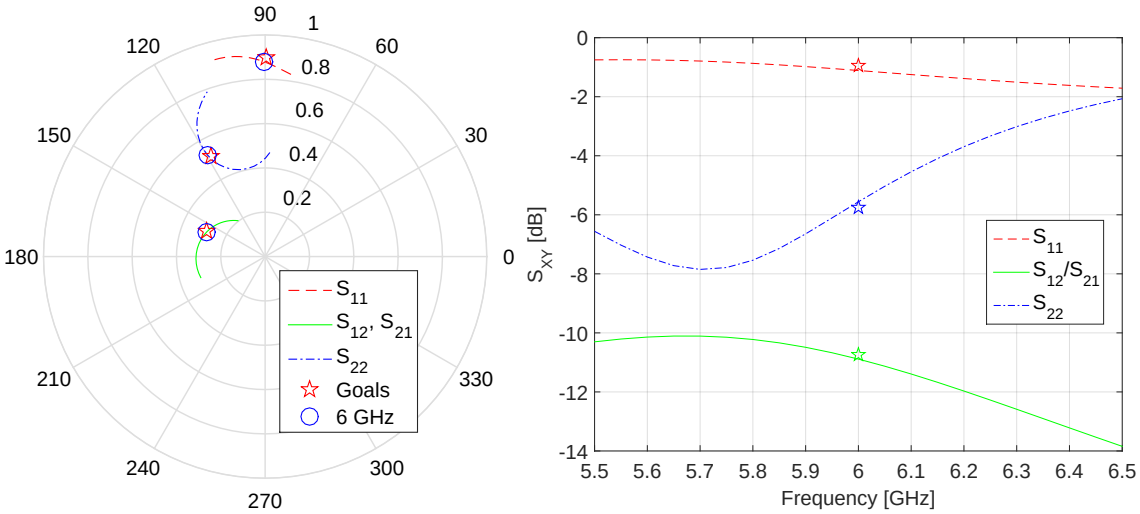


Figure 4.12: Combiner S-parameter simulation results between 5.5−6.5 GHz. Left: comparison of achieved values at the center frequency (circles) with targeted values (stars). Right: S-parameters in dB compared with the target values at 6 GHz.

4.4 Phase shifter

The output from the main and auxiliary branches needs to be out of phase by a certain amount in a Doherty amplifier, e.g. 90° for the classical DPA [5]. For this design approach, the phase offset was determined to be -84.3° in Chapter 4.3.1 (i.e. the main branch being delayed 84.3° with respect to the auxiliary branch). Note that this is the phase offset at the output, which is for both amplifiers connected to the combiner. There is therefore the need to shift the phase at the input by an amount that causes the phases at the outputs to reach their desired relationship (i.e. not only θ, but also compensating for the difference). This is made complicated by the fact that the phase shift depends on the bias class (and to some extent power level) of the amplifier, resulting in different phase shifts along each cell. Additionally, because the input impedances differ, so do the matching networks and thus their phase shifts. Furthermore, the input impedance of main and auxiliary cells are different due to different biasing. This causes the voltage and the current phase shifts to be different as well. These factors, particularly the latter, make the task of systematically determining the correct phase shift a difficult problem that was not resolved in a fully satisfactory way. Some ideas regarding future improvement are presented in Chapter 6.2.2.

Simulations of the complete amplifier were done, but some problems occur because of the mixing of simulation data and measurement data. Perhaps most importantly, the source matching differs, especially for the class C cell. This caused less power to be delivered to it, with a significant reduction in output power compared to the class B cell, disturbing

the load modulation.

It would seem usable to simulate the DPA with source matching for the transistor model, but keeping the measurement derived combiner. This did in fact result in the amplifier satisfyingly showing that the load modulation worked (i.e. having the typical PAE versus power behavior of a Doherty). However, this creates another problem, which is that the simulated matching networks now differ from the actual ones. This means that if the length of the phase shifter were to be optimized based on these simulations, it would not be optimized for the real matching networks which have different electrical lengths and impedances.

Eventually, the phase shift was decided based on simulations with the measurement based matching networks, but with unequal input power to compensate for the bad source matching. The DPA was simulated for different phase shifts and the PAE and gain profiles were compared. It was decided that a value of -131° should be roughly centered on the truly desired value. While this may not be fully accurate, simulations indicated that the value was not very critical, with the performance not changing much even when varying the phase offset by tens of degrees. While -131° seems large compared to -84.3°, it should be remembered that the physical length of the auxiliary matching network is also longer than that of the main cell.

The phase shift at the input was achieved by simply having different lengths of transmission lines between the power splitter and each amplifier's matching network, shaped in a way that was suitable for the PCB layout. The layout of the phase shifter can be found in Fig. 4.13. Extra pads were added with the goal of having an adjustable electrical length, where the existing bridge could be cut and copper tape used to form a longer or shorter transmission line.

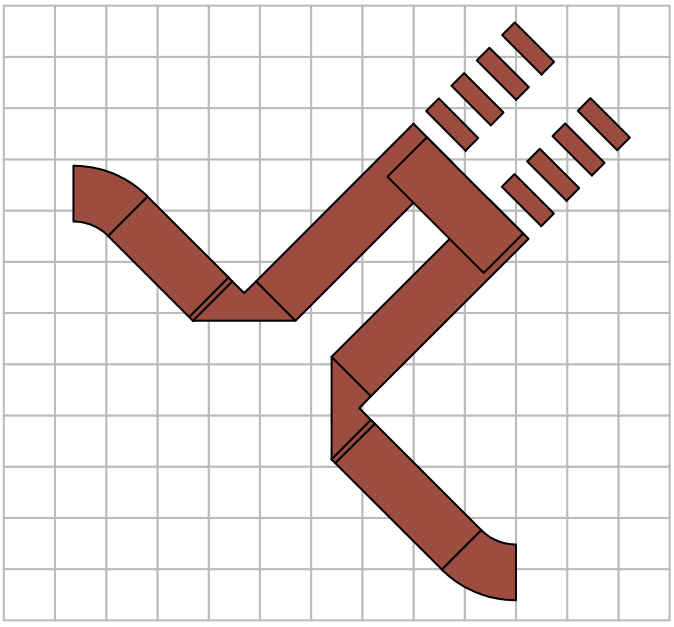


Figure 4.13: Trimmable phase shifter for the DPA. Grid size 1x1 mm.

4.5 Complete layouts

The main and auxiliary amplifiers were placed in parallel with one of them vertically flipped. They had to be aligned so their outputs connect to the combiner. On the input side, before the matching networks, the impedances are still 50 Ω, so here the length of the microstrips connecting the inputs can be any length that suits the layout (as long as the difference in electrical length gives the required phase shift). The completed layout is shown on the left in Fig. 4.14.

Additionally, a second board was designed without the power splitter. Because it has separate inputs, the phase relationship can be freely selected by a suitable signal generator. This is done as a backup solution that can be used to easily examine the phase offset behavior in case the normal amplifier would not work.

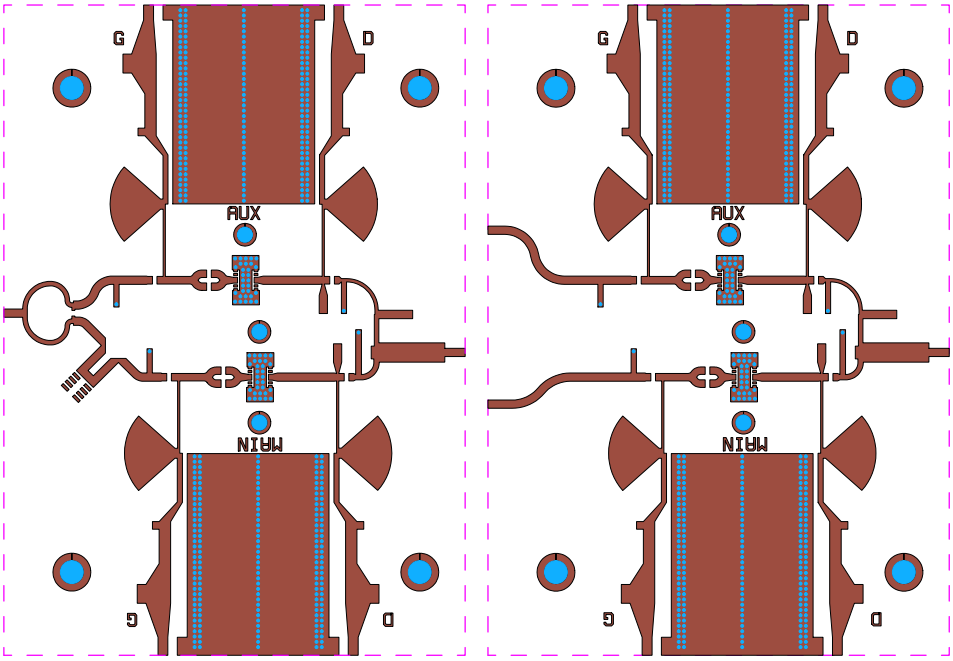


Figure 4.14: Final PCB layouts, natural size (on A4 paper). The outer dimensions of a board is 61x86 mm.

In the next chapter, the measurement results from the amplifier, once assembled, are shown. A comparison to similar amplifiers is also given.

5

Doherty amplifier measurement results

In this chapter, the measurement setup first described, followed by an evaluation of bias voltages. The selected voltages are then used for performing power and frequency sweeps of the amplifier. Finally, a comparison to similar amplifiers are made.

A photograph of the complete amplifier is shown in Fig. 5.1. On the lower end, the input connector is located. Going upwards, the power splitter and phase shifter are seen, followed by single stub matching networks. The upper connector is the output, which follows the combiner.

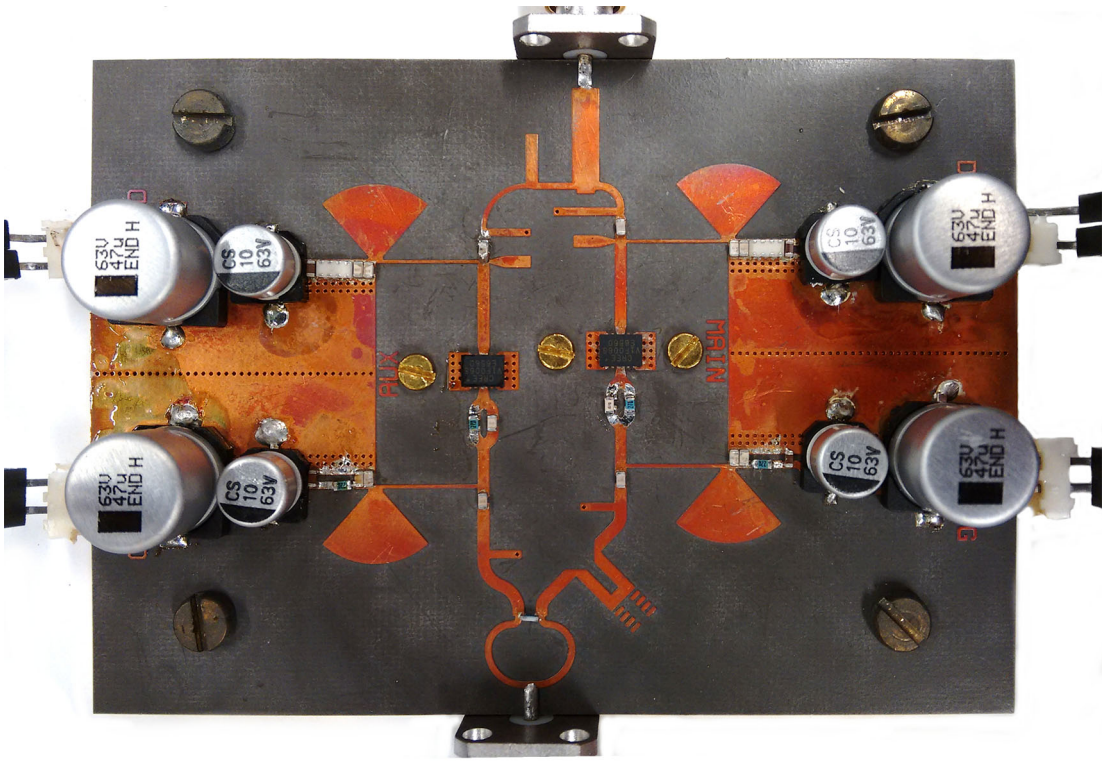


Figure 5.1: Assembled 6 GHz Doherty PA prototype developed from load-pull measurement data. PCB dimension are 61x86 mm.

5.1 Measurement setup

The measurement setup is essentially the same as the setup used for the device characterization, but without the tuners. One noteworthy difference is that since frequency sweeps will be done, the delivered input power to the DPA should be constant for the whole frequency range. Since the gain of the preamp, as well as the losses in the coupler and isolator, are frequency dependent, the power at the DUT plane would vary. To overcome this, the power at the DUT plane was measured as a function of frequency for a fixed synthesizer power, and the difference was used for calibrating the output power from the generator for the actual measurements. This resulted in an almost flat input power for the DUT, instead of a variation of 1 dB.

5.2 DC sweeps and bias voltages

Initial sweeps of the gate bias voltages for the main and auxiliary amplifiers were done to find the appropriate bias voltages. The curves are presented in Fig. 5.2, which also includes the DC behavior of the transistor on the "RISKY" test board. The pinch-off voltages of both main and auxiliary transistors are different than the sample used in load-pull measurements as seen from the figure. The gate bias is therefore re-adjusted, from $-2.65\,\mathrm{V}$ to $-2.85\,\mathrm{V}$[1], to have the same quiescent current as in load-pull measurements. For class C biasing, the voltage choice is less clear. The optimal auxiliary gate voltage is therefore found by performing sweeps in large signal measurements as will be shown in the next section.

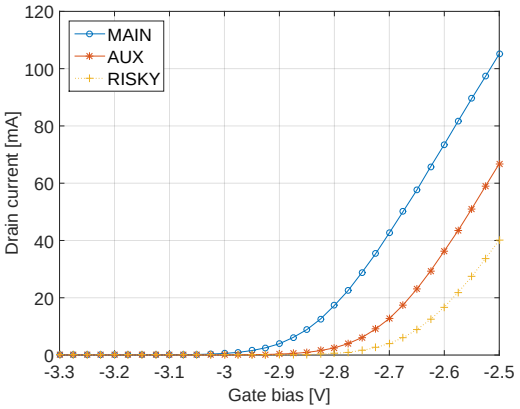


Figure 5.2: Gate bias sweeps of the transistors on the final DPA, with previous sample as comparison. $V_{DS} = 40\,\mathrm{V}$.

Initially, the amplifier was oscillating around 700 MHz. It turned out that a deep dip of the K-value around this frequency was missed due to bad interpolation of the EM simulation data by ADS. It was solved by increasing the value of the resistor in the stability networks from $12\,\Omega$ to $27\,\Omega$ and inserting a series resistor in the gate bias supplies, after the high-value, low-frequency decoupling capacitors but before the smaller pF-range capacitors. This way, they only affect lower frequencies. It was later found that the series resistors alone were enough to stop the oscillations for any bias voltage combination, so the $12\,\Omega$ resistors were reinserted for optimal source matching. Since the series resistors do not significantly affect the input impedance at the center frequency because of their placement in the circuit, the effectiveness of the input matching is practically unaffected. The results in this chapter are taken using the $12\,\Omega$ gate resistors, except for figures 5.3 and 5.4.

[1] Some early measurements used $-2.84\,\mathrm{V}$.

5.3 Power sweeps

In this section, power sweeps were performed with different bias voltages. The main purpose is initially to examine how the choice of gate biases affects the gain and PAE profiles of the Doherty, and to verify and fine tune the predicted values. Note that the scales are different for gain and efficiency plots. In Fig. 5.3, the auxiliary gate bias voltage has been stepped between $-3.8\,\mathrm{V}$ and $-5.4\,\mathrm{V}$. As can be seen in the upper chart, a higher bias is clearly associated with higher large signal gain. From the lower chart, it can be seen that a deeper bias causes the location of the back-off efficiency "peak" to shift as well. This behavior is in nice agreement with expectations.

Based on these results, the class C gate bias was selected to $-4.5\,\mathrm{V}$, as a trade-off between gain and back-off PAE improvement. For a comparison, recall from Chapter 3 that the class C cell was supposed to shut off at $-3.6\,\mathrm{V}$ in the test setup, and the final bias voltage would be expected to be $0.5-1\,\mathrm{V}$ below this. In addition, the threshold voltage of the actual transistor is some tenths of a volt lower than for the sample device.

The main gate bias voltage was examined as well, in in steps from $-2.75\,\mathrm{V}$ and $-3.0\,\mathrm{V}$. The gain and PAE are shown in Fig. 5.4. It can be seen from these diagrams that the amplifier has a non-linear behavior, with a large peak in gain between 20 and 30 dBm. As is normally the case, the gain compresses for higher powers, but it also drops off at very low power levels. While this might seem to indicate a too deep bias voltage for the class B cell, the figure shows that increasing the voltage beyond $-2.85\,\mathrm{V}$ does not improve the situation. Therefore, the voltage choice of $-2.85\,\mathrm{V}$ may be optimal, since increasing quiescent current would in this case mainly lead to a reduction of efficiency with no further advantages.

Clean power sweeps for the final bias voltages of $-2.85\,\mathrm{V}$ (main) and $-4.5\,\mathrm{V}$ (auxiliary) are shown in Fig. 5.5, done with the $12\,\Omega$ resistors reinserted. The measurement points are not equidistant; the input power was stepped in small steps of 0.5 dBm for high power levels, but in larger steps up to 2 dBm for low power levels (where not much was changing anymore and the high sampling density was unnecessary).

As seen from Fig. 5.5, the prototype PA satisfyingly exhibits a a very distinct Doherty PA behavior, proving the feasibility of the design approach developed in this master thesis project.

The highest power level in these measurements was limited by the measurement setup, specifically the power handling capability of the preamplifier[2], which means the amplifier would likely have been capable of higher output power if the input power level could have been increased (no appreciable gate current was flowing).

When comparing the efficiency of the DPA with the efficiency of the test board, it should be remembered that there are additional losses in the combiner and input matching networks in the DPA, and the de-embedding had also removed the effects of the fixture connectors and parts of the PCB (to get to the desired reference planes at the coupling capacitors). This is in contrast to this data, which is for a complete amplifier.

[2]No preamp with higher power suitable for this frequency range was available.

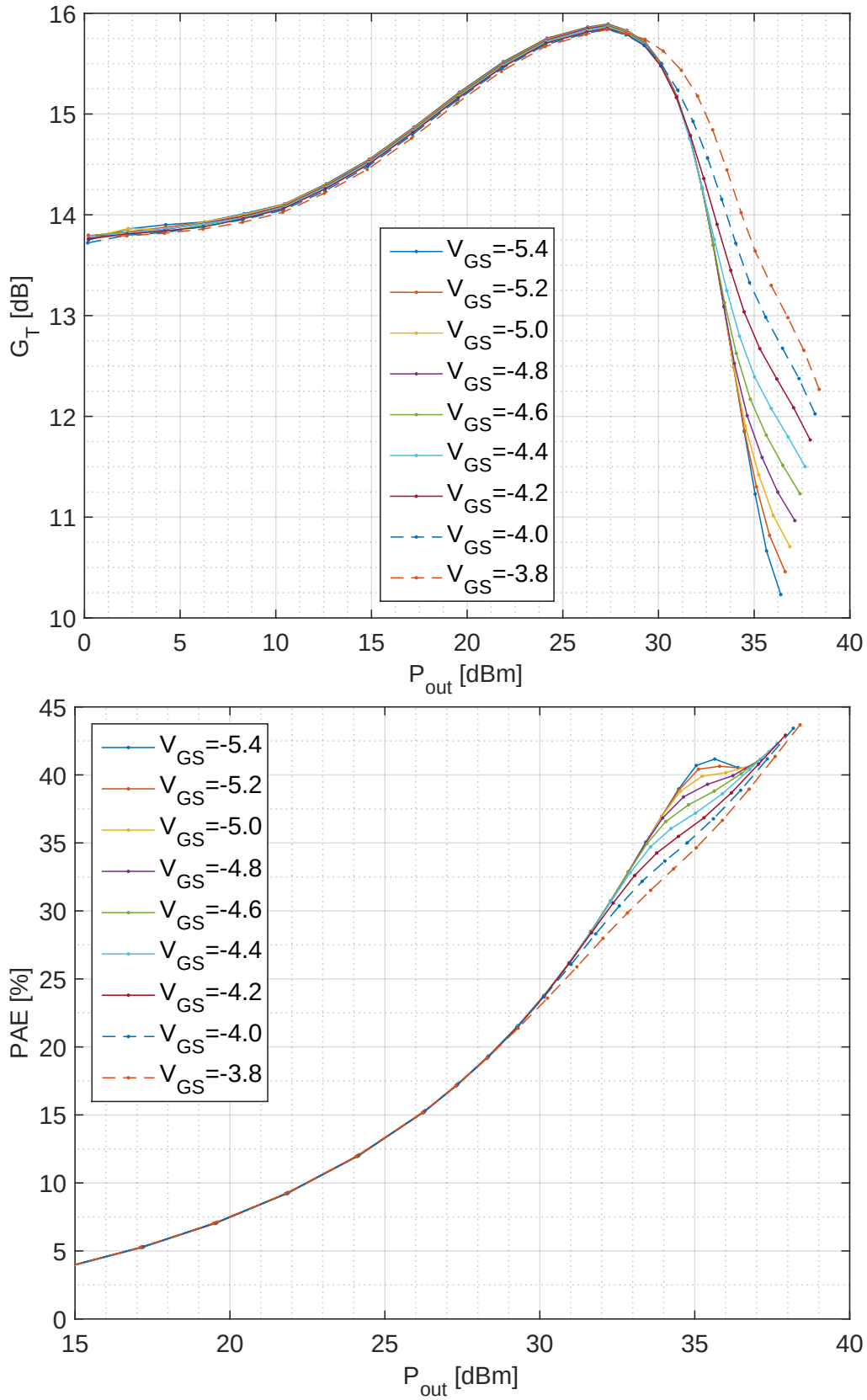


Figure 5.3: Measured transducer gain and power added efficiency results versus output power at 6 GHz for different **aux.** gate bias values. $V_{DS} = 40\,\mathrm{V}$ and $V_{GSmain} = -2.84\,\mathrm{V}$.

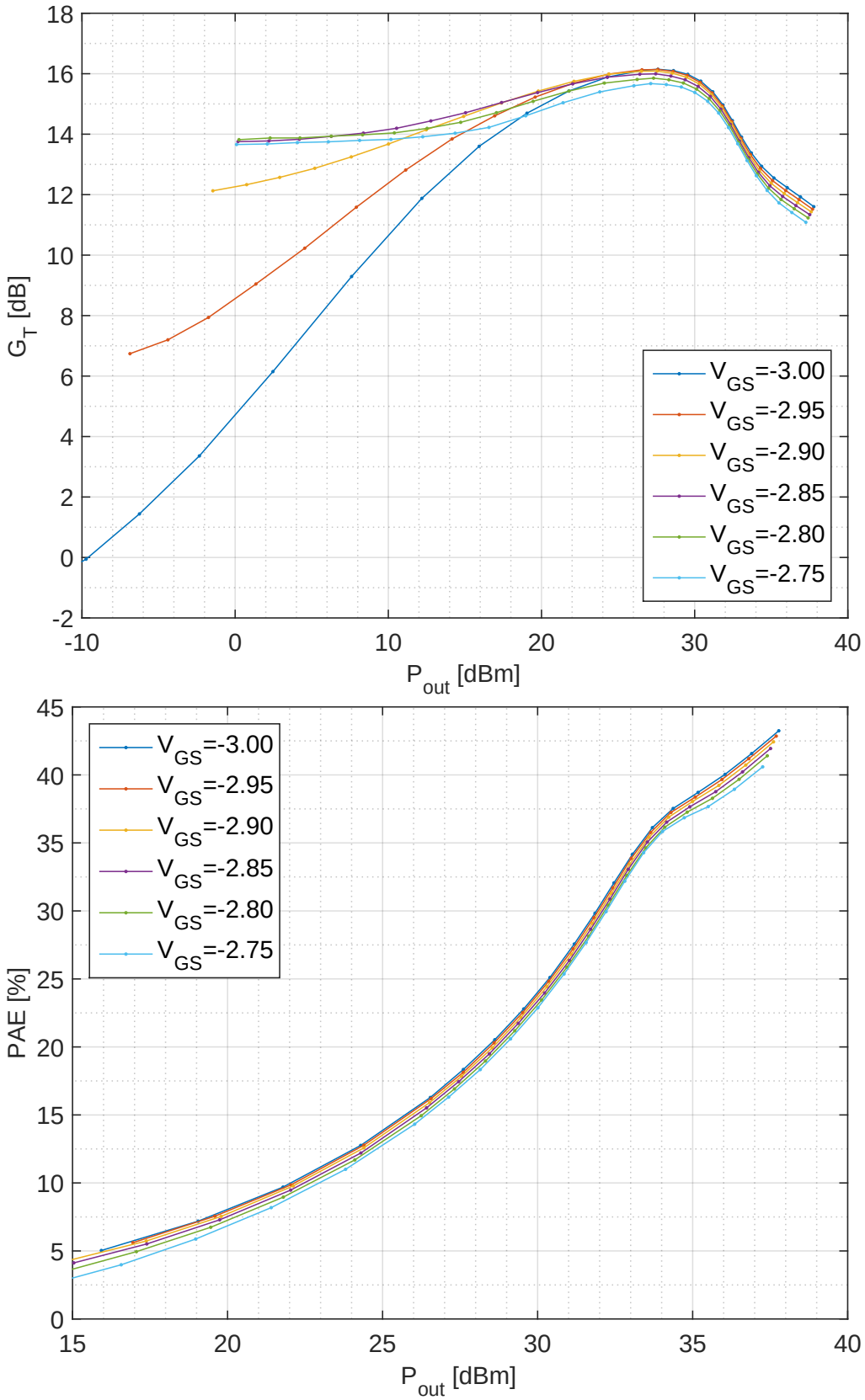


Figure 5.4: Measured transducer gain and power added efficiency results versus output power at 6 GHz for different **main** gate bias values. $V_{DS} = 40\,\mathrm{V}$ and $V_{GSaux} = -4.5\,\mathrm{V}$.

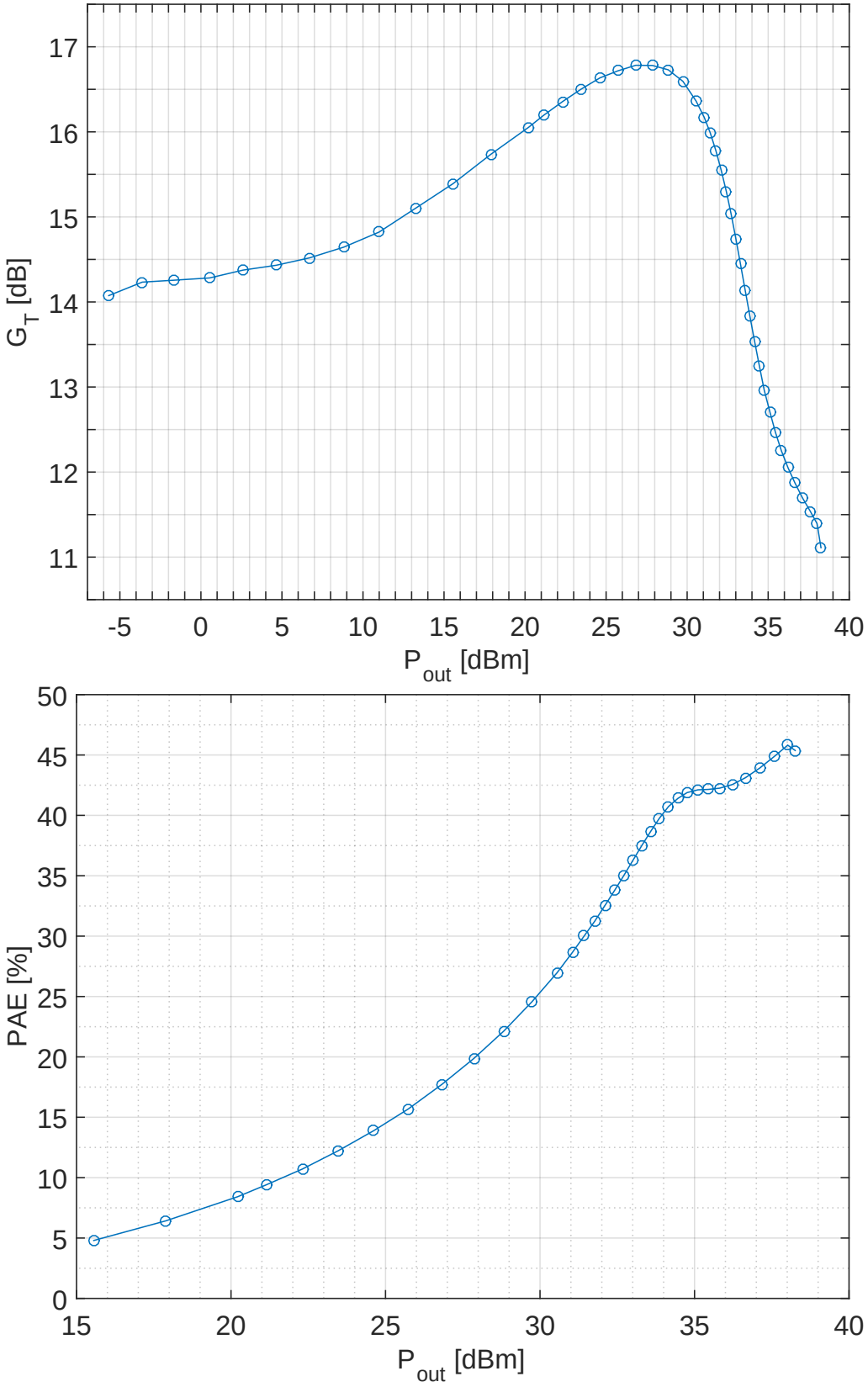


Figure 5.5: Final power sweeps of the DPA at 6 GHz. $V_{DS} = 40\,\mathrm{V}$, $V_{GSmain} = -2.85\,\mathrm{V}$, $V_{GSaux} = -4.5\,\mathrm{V}$.

5.4 Frequency sweeps

The result of frequency sweeps performed for a range of fixed input power levels are shown in Fig. 5.6.

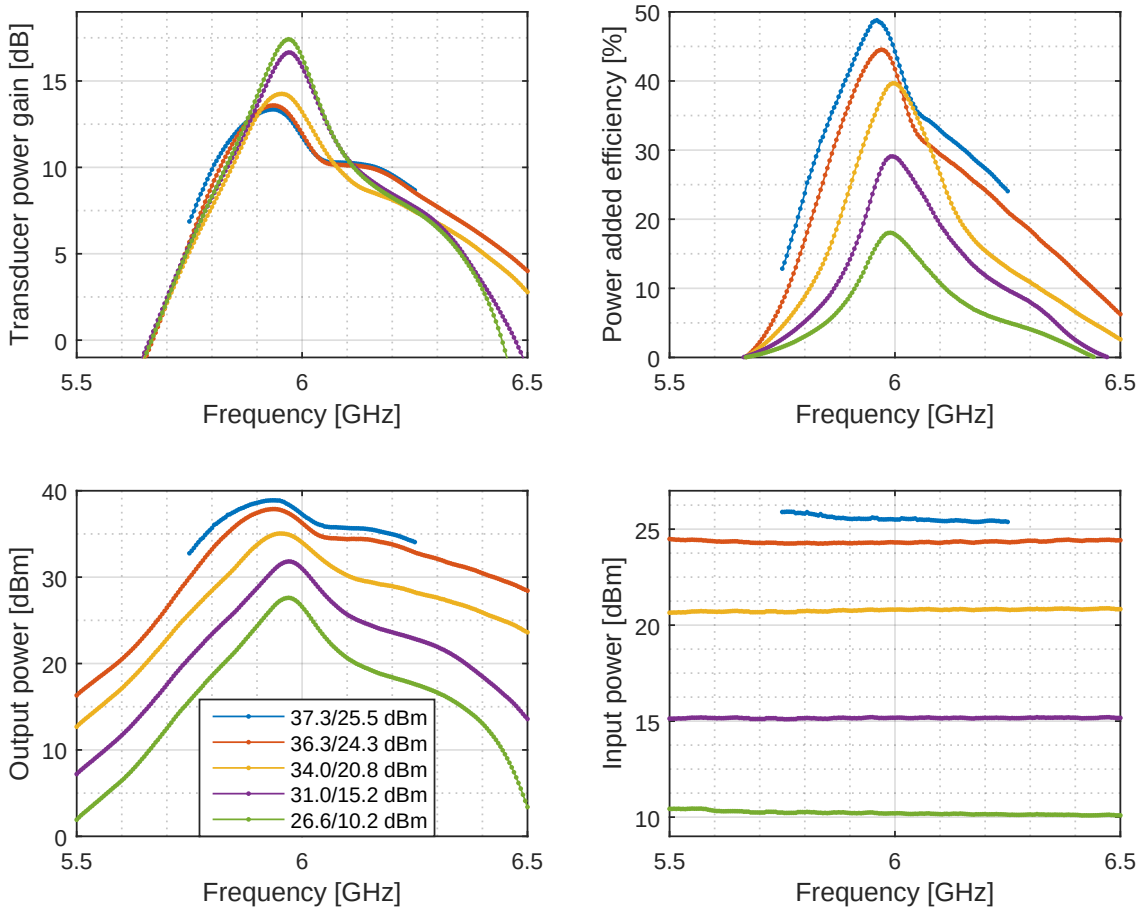


Figure 5.6: Frequency sweeps for a selection of power levels. The legend entries give the output and input powers at the center frequency. $V_{DS} = 40\,\mathrm{V}$, $V_{GSmain} = -2.85\,\mathrm{V}$, $V_{GSaux} = -4.5\,\mathrm{V}$.

The 3 dB fractional bandwidth is 4 % at maximum output power, shrinking to 2 % at 11 dB output back-off. This corresponds to 120-240 MHz of bandwidth. If instead the window where the gain exceeds 10 dB is considered, the bandwidth is a bit better at about 4-6 % depending on the input power. This is not wide, but it should be remarked that the DPA was not designed to maximize bandwidth. The performance is quite well centered around the target frequency, which is a nice result especially when considering the narrow bandwidth. Both PAE and gain for the higher output powers are slightly off-center though, and for any power, P_{out} is clearly peaking below 6 GHz. If this could be improved by tweaking the phase shifter would be an interesting issue to examine, but was not done because of time constraints.

The sweep with the highest power was performed for a narrower frequency range. This was done because the gain and the output power of the preamplifier were noticeably higher before it was warmed up after some minute of being switched on, so it was only possible

to reach this power level for a short measurement run. Even though, the gate current was never higher than a few microamperes, indicating the PA should still be capable of handling more power if it had been available.

The expected output power from the DPA consisted (ideally) of 37 dBm from each amplifier cell, for a total of was 40 dBm. At 6 GHz, the DPA falls short of this, but at a somewhat lower frequency, the output power reaches 38.9 dBm, which is not far below the goal, especially when considering the additional losses in the combiner. All of this data is from the fixed phase shift Doherty PA without adjustments to the phase offset. Perhaps adjustments could have centered the design perfectly on the intended frequency.

5.5 Performance comparison with other Doherty PAs

Table 5.1 shows a comparison with other Doherty PAs at similar frequencies. [22] and [23] are MMICs, unlike the PAs in [24], [25] and in this project. No hybrid DPA at a frequency exceeding 6 GHz was found.

In comparison to the other amplifiers, this one has two main weaknesses. First, the gain is significantly non-linear. Second, the fractional bandwidth of only 2-4 % is very narrow. For comparison, [22] and [23] achieve 22 % and 41 % of bandwidth respectively. However, a strong point of this amplifier is that the gain is high, especially when compared to [22], [23] and [25], and at most powers generally higher than for the DPA in [24], which is at a lower frequency. Aside from the gain peak of over 16 dB at around 10 dB OBO, the gain at heavy output back-off (>35 dB) is well over 14 dB, and over 11 dB at full power.

Table 5.1: Results of this work compared to other Doherty PAs at similar frequencies. PAE is given in percent, transducer gain in dB, frequency in GHz and power in dBm. The values for the other works are read from graphs, possibly resulting in slight inaccuracies. Values from [24] from two-tone measurement. G_T for [25] interpolated from different bias voltages to match the bias voltage used for its PAE measurements.

			Full power		3 dB OBO		6 dB OBO		9 dB OBO	
DPA	Freq	P_{out}	G_T	PAE	G_T	PAE	G_T	PAE	G_T	PAE
This work	6.0	38.3	11.1	45.4	12.6	42.1	15.4	33.2	16.7	23.4
[22], MMIC	6.8	35	9	40	11.5	40	11.5	37	11.5	34
[22], MMIC	7.2	34.7	9	42	10.3	42.5	10.3	40	10.3	37
[23], MMIC	6.4	36	6	35	8.7	40	9.5	43	9.8	36
[24]	5.0	36.5	11.5	60	12.7	47	12.5	37	12.5	28
[25]	5.8	41.5	5.5	44	6.8	46	8.2	42	9.6	38

6
Conclusion

The design procedure and final performance of a 6 GHz Doherty power amplifier constructed on PCB using packaged devices based on load-pull measurement results have been shown. Some findings and difficulties with this design approach will now be presented.

6.1 Conclusions

Even for simulation based Doherty PA designs at significantly lower frequencies, such as a few gigahertz, the center frequency is typically shifted in measurements. However, the design approach developed in this thesis enabled the realization of a 6 GHz DPA at the intended center frequency, without requiring tuning[1]. This clearly shows the robustness of the method.

The final amplifier achieves more than 45 % power-added efficiency (PAE) for 38 dBm of output power at 6 GHz, with 42 %, 32 % and 23 % PAE at 3, 6 and 9 dB of output back-off respectively. The gain of the amplifier was high compared to other Doherty PAs at similar frequencies. This shows that MMIC designs are not necessary for this type of circuitry even at such high frequencies, where parasitics play an important role. Therefore, high-frequency Doherty PA designs may be economical even for low-volume production where the high initial cost of a MMIC design would be prohibitive. Additionally, the design approach would be useful if there is no device model available (the measurements would then also have to involve S-parameters for stability calculations, and the load-pull measurements should also include at least the second harmonic).

The optimal impedances found from the measurements differed from simulated optimal impedances. This indicates that there was a point in performing the measurements as opposed to doing the design entirely based on simulations.

It was discovered that the selection of the input phase offset was a more complex task than initially thought. This is covered under Future work, Chapter 6.2.2.

A wideband design was not a goal of this project, but still the narrow fractional bandwidth was lower than what would have been expected even without it being a design consideration. One possible cause could be the long delay lines that where included to achieve the second harmonic reflection coefficient on the load side. This could be limiting bandwidth by causing a rapid rotation of the impedance presented to the transistors by the combiner. In this case, this is a limitation of the particular circuit, not necessarily of the

[1] Apart from the stability related mistake which occurred because of a detail in ADS was overlooked, but the required modification should not significantly have affected RF behaviour.

design procedure. However, the combiner itself is also not electrically small. Nonetheless, even a few percent of bandwidth at this frequency corresponds to hundreds of megahertz, a definitely usable bandwidth.

6.2 Future work

In this chapter, ideas about future work and how identified obstacles can be solved are presented.

6.2.1 Combiner synthesis and simulation

In Chapter 4.3, a method for creating combiners in microstrip was shown. Since the method yields several solutions and also contain several variables that can be freely chosen (such as impedances of transmission lines), picking the optimal combination involved going back and forth between calculations in Matlab and simulations in ADS. It would be convenient if the method could be implemented directly in ADS scripting language. Then solutions could quickly be examined for bandwidth and tolerances without having to manually transfer sets of values into ADS. Even automatic optimization could be carried out. Alternatively, the circuits could be simulated in Matlab using RF Toolbox.

6.2.2 Phase shift issue

One of the most difficult parts of the design process has been determining the required phase shift at the input. The circumstances are quite complex, since each of the amplifier cells are not only expected to cause somewhat different phase shifts, but their impedances at input and output also differ, as well as their matching networks. This makes the problem hard to grasp. By optimizing the phase offset using simulations (with a mix of simulated and measured parameters), an workable value was obtained. However, it would be desirable to use a more elegant approach to the selection of the phase shift.

The device characterization did not include any measurements of the phase shift that occurred through the DUT. One possible strategy of reducing the uncertainty about how the input phase shift should be selected could be to experimentally measure the phase offsets through the DUT for the different bias classes. This could be done after the tuners have been set to the desired input and output reflection coefficients. Since the two-port network parameters of the tuners were measured, the information needed to find the phase shifts that the amplifier cells cause should be obtainable from this. For optimal accuracy, this should be a large-signal measurement.

One accurate approach for finding the optimal phase shift would be to introduce a second characterization step in the design process, consisting of manufacturing a dual-input version of the DPA. Since the inputs are then independently controllable and the matching networks are included in the design, the actual amplifier can be characterized with regard to phase offset. Once the optimal impedance has been found, the final Doherty PA can be manufactured based on this information.

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A

Inductor replacement method, continued proof

What needs to be shown is that

$$2Y\cos\theta + j\left(Y^2 Z_0 + Y_0\right)\sin\theta = 0 \tag{4.5c}$$

holds when

$$\sin\theta = \frac{X}{Z_0} \tag{4.6a}$$

$$Y = \frac{1-\cos\theta}{jZ_0\sin\theta} \tag{4.6b}$$

First, we substitute Y with the expression in (4.6b). This gives

$$2\left(\frac{1-\cos\theta}{jZ_0\sin\theta}\right)\cos\theta + j\sin\theta\left(\frac{1^2 - 2\cos\theta + \cos^2\theta}{-Z_0^2\sin^2\theta}Z_0 + \frac{1}{Z_0}\right) = 0$$

Y_0 was also replaced by $1/Z_0$. By simplifying until the two left hand terms have the same denominator we get

$$\frac{2\cos^2\theta - 2\cos\theta}{Z_0\sin\theta} + \frac{-\cos^2\theta + 2\cos\theta - 1}{Z_0\sin\theta} + \frac{\sin\theta}{Z_0} = 0$$

After summarizing the two first terms, the equation looks much simpler:

$$\frac{\cos^2\theta - 1}{Z_0\sin\theta} + \frac{\sin\theta}{Z_0} = 0$$

Now, we use that $Z_0\sin\theta = X$ and that $Z_0 = X/\sin\theta$, which is given by our first result, 4.6a. With this, we can write everything as one fraction:

$$\frac{\cos^2\theta - 1}{X} + \frac{\sin^2\theta}{X} = \frac{\cos^2\theta - 1 + \sin^2\theta}{X} = 0$$

The equation has now boiled down to showing that the numerator equals zero. The Pythagorean trigonometric identity, $\cos^2\theta + \sin^2\theta = 1$ is easily identifiable in the expression, reducing it to

$$1 - 1 = 0$$

and thus proving the equality.