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Analysis and improvement of phase noise performance of a PLL-based RF synthesizer

Accurate modeling including voltage noise generated in the active loop filter

Master's thesis in Wireless, Photonics and Space Engineering

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

The goal of this thesis work was to analyze, model and improve the phase noise performance of a wideband synthesizer prototype. The analyzed synthesizer is based on a phase-locked loop (PLL) with an active loop filter, where the output frequency range is 2340 MHz − 4420 MHz in steps of 260 MHz.

The noise analysis carried out in the thesis places emphasis on the loop filter and proposes a model for a model for simulation of phase noise at the output of the PLL. The model is verified through measurements and a new filter design is proposed. The new filter is designed for reduced thermal noise which reduces the PLL output phase noise.

At an output frequency 3120 MHz, the simulated phase noise of the synthesizer with the new filter design is −124.4 dBc/Hz at offset frequency 1 MHz, which is an improvement of more than 7.5 dB compared to the synthesizer with the original filter design.

Keywords: PLL, synthesizer, phase noise, active loop filter, wideband

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Björn Persson, Gothenburg 2015-09-15

Abbrevations & Notations

Abbreviations

DSB Double-sideband

ESA European Space Agency

IEEE Institute of Electrical and Electronics Engineers

KCL Kirchoff's current law

LNA Low noise amplifier

OP AMP Operational amplifier

PD Phase Detector

PLL Phase-locked loop

RF Radio frequency

RHP Right half plane

rms Root mean square

SSA Signal Source Analzer

SSB Single-sideband

VCO Voltage controlled oscillator

Nomenclature

A Voltage amplitude [V]

α Constant representing the level of flicker noise in Leeson's oscillator phase noise model

C Capacitance [F]

Δf Offset frequency [Hz]

F Noise figure

f Frequency [Hz]

f_0 Frequency of operation [Hz]

$F(s)$ Loop filter transfer function

$G_{\mathrm{hp}}(s)$ High-pass filtering gain function

$G_{\mathrm{lp}}(s)$ Low-pass filtering gain function

$G_{\mathrm{ol}}(s)$ Open-loop gain function

$G(s)$ Gain function

$H(s)$ Feedback transfer function

I DC current [A]

i Current [A]

k Resistor reduction factor

k_{B} Boltzmann's constant (k_{B}=1.3806·10^{-23}J K^{-1})

K_{pd} Phase detector constant [rad V^{-1}]

K_{vco} VCO sensitivity [Hz V^{-1}]

$\mathscr{L}$ Phase noise [dBc/Hz] or [Hz^{-1}]

N Division number

P Power [W] or [dBm]

Q Quality factor

R Resistance [Ω]

s Complex number frequency in the Laplace domain [rad]

S Power spectral density [W] or [dBm]

T Temperature [K]

t Time [s]

θ Phase deviation [rad]

V DC voltage [V]

v Voltage [V]

Contents

Chapter 1

Introduction

This chapter defines the topic of the thesis, provides the background and presents the motivation for this work. It also describes the scope of the project and includes a brief outline of this report.

1.1 Context

Satellite communication has become an important part of our everyday life. Today, there are over 1000 satellites in orbit around Earth used for e.g. television broadcasting, mobile telephony, remote sensing and navigation[1]-[3]. Naturally there are some technologies which are competing with satellite communication. For instance, cellular telephone networks with base-stations located throughout populated areas dominate the usage of mobile telecommunication in most countries today. Another example is fiber-optical and electrical transmission which to some extent has replaced satellite television. Despite the competing technologies, the use of satellite communications is still increasing and there is no doubt that the demands on high performance systems that can handle higher data-rates will continue to grow in the foreseeable future.

A key component in satellite communication systems is the radio frequency (RF) synthesizer, a device which works very much like the commonly known audio synthesizer, but for higher frequencies. An RF synthesizer produces one or several different output frequencies from a few or a single reference frequency source[4]. One of the most critical properties of the synthesizer is the spectral purity. The reason for this is that high spectral purity can increase the data-rate of the system. In microwave technology, spectral purity is often quantified in frequency domain as phase noise, a measure of random fluctuations in the phase at frequencies close to the carrier frequency. Phase noise is of great importance in communication systems and this property is thoroughly studied in this thesis.

1.2 Background

Several different topologies of synthesizers have been developed throughout the years. The first versions consisted of a crystal-controlled oscillator where the output frequency could be adjusted by manually switching to a different crystal[4]. The next step in the development was a synthesizer with a few different crystal-controlled oscillators which were mixed, multiplied and divided to generate the desired output frequencies. The accuracy and stability of these synthesizers is determined by a combination of the accuracy and stability of each oscillator. Thus, a highly accurate synthesizer of this type requires multiple high performance crystal-controlled oscillators[4]. Such oscillators were very expensive a few decades ago and therefore it was natural that a synthesizer using only one high-performance crystal-controlled oscillator was eventually developed.

The above mentioned techniques using mixers, multipliers and dividers are categorized as direct frequency synthesis. Naturally these kind of topologies generate a spurious output, i.e. it contains unwanted frequencies in the output signal. This is not necessarily the case for indirect synthesis, which utilizes a feedback loop to adjust the output frequency. This topology can use the same components as in direct synthesis but also voltage controlled oscillators (VCOs), phase detectors and programmable dividers. One of the main advantages of indirect synthesis, apart from producing a less spurious output, is that the noise floor is generally lower than in direct synthesis. The disadvantage of indirect synthesis is that it can be more challenging to achieve high performance in properties such as loop stability, acquisition and spectral purity close to the carrier[4].

Indirect synthesis methods almost exclusively use phase locked loops (PLLs) as feedback systems. Frequency-locked loops also exist, but these cannot achieve as high performance as its phase-locked counterpart[5]. Therefore, this thesis is focuses on a PLL-based design.

PLLs can be either analogue or digital and the definition varies among different authors. In [6], a digital PLL is defined as a PLL where the phase detector is built up by digital components such as gates and flip-flops. By this definition, the PLL studied in this thesis is analogue since a mixer is used as phase detector. The main advantage of an analogue PLL design is that it allows for higher output frequencies than a digital design[7].

1.3 Objective

This thesis investigates the phase noise performance of a synthesizer prototype developed by RUAG Space AB. The synthesizer is designed on a request from the European Space Agency(ESA) and is at the moment in an early prototype stage. The investigation is carried out on a synthesizer which is a part of a bigger frequency generating system for satellite communication, where the total performance is partly limited by the synthesizer's phase noise.

The synthesizer has a reference signal of 260 MHz and an output signal of frequency

between 2340 MHz and 4420 MHz in steps of 260 MHz. Measurements have shown a phase noise that is higher than expected at offset frequencies above 100 kHz. For instance, at an output frequency of 3120 MHz and offset frequency 350 kHz, the phase noise was measured to be -113.6 dBc/Hz compared to the expected phase noise that was -118.3 dBc/Hz. This increase is caused by the loop filter and the objective of this work is to find an accurate model which explains it and also to design a new loop filter with better phase noise performance.

1.4 Motivation

There are plenty of textbooks and articles describing the phase noise theory of PLLs and synthesizers, for instance [4]-[6],[8]. All of these provide the theory of designing a loop filter for optimal phase noise performance with respect to the PLLs main components, but without taking the noise generated in the loop filter into account. The loop filter is normally built up by resistors, capacitors and operational amplifiers (OP AMPs) which all contribute noise to the system. This noise modulates the carrier signal of the VCO and adds to the total phase noise of the PLL, as will be shown in this thesis. The filter noise theory is rarely found in the literature and the reason is, to the authors understanding, that this noise is often low enough to be negligible. However, a highly sensitive VCO converts a low filter noise to significant output phase noise. Therefore it is important to keep this in mind when designing a PLL and to have an accurate model when the filter noise cannot be considered negligible. During the literature review in this work only three papers describing this filter noise could be found, [9]-[11], and in those papers it was not thoroughly investigated. Consequently there is a need for a deeper analysis of the phase noise contribution of the loop filter.

1.5 Outline

In Chapter 2 some basic PLL theory is discussed and the theory of phase noise in a PLL, with extra focus on the loop filter, is thoroughly investigated. Chapter 3 presents the design of the synthesizer followed by a description of the measurements performed during the project. In Chapter 4 the results are presented and discussed and Chapter 5 summarizes the conclusions of the whole project and suggest topics for future analysis.

Chapter 2

Theory

This chapter starts by defining phase noise after which some fundamental concepts of PLLs are introduced. This is followed by studying the the phase noise contribution from the different components in the PLL, with extra focus on the active loop filter.

2.1 Phase noise theory

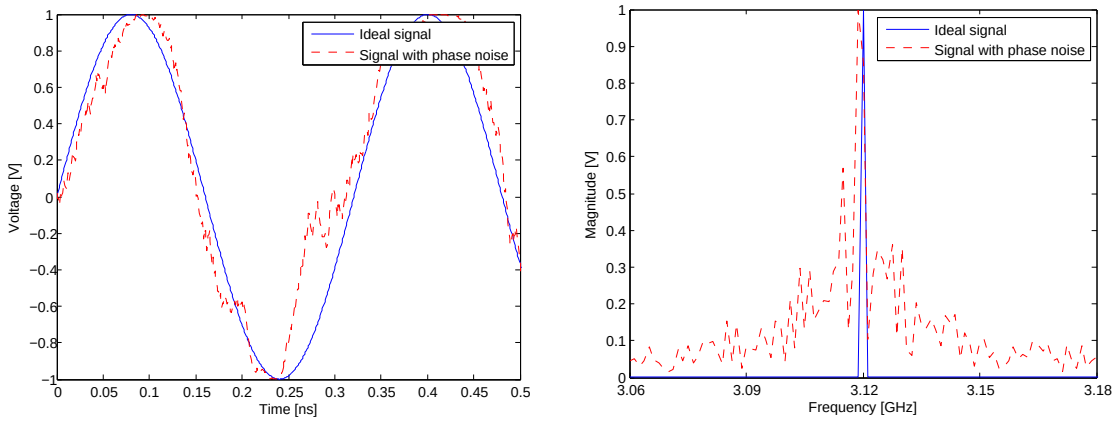
The noise performance of a synthesizer is very important because it can degrade the performance of the complete system severely. There is for instance thermal noise which adds to the noise floor and limits the performance of highly sensitive systems[5]. A certain kind of noise is called phase noise which refers to random fluctuations in the phase of the signal. Phase noise is very important in frequency generating systems because it can for instance increase bit error rates in digital systems or contaminate adjacent frequency channels and thereby limit the number of usable channels[5],[12].

To illustrate phase noise, a signal with amplitude 1 V and frequency 3120 MHz was created with and without uniformly distributed phase fluctuations in MATLAB . The signal is shown in time and frequency domain in Fig. 2.1. Note that, for readability, the phase noise in time domain has been made 10 times larger than in frequency domain.

The Institute of Electrical and Electronics Engineers (IEEE) definition of phase noise is half of the double-sideband (DSB) power spectral density of phase fluctuations[13]. Phase noise is generally expressed in decibels below the carrier in a 1 Hz frequency band, dBc/Hz, for a certain offset frequency. This defintion will be used throughout this thesis and the phase noise will be denoted $\mathscr{L}$:

$$\mathscr{L}(\Delta f)\ [\text{dBc/Hz}] = 10\log_{10}\left(\frac{S_{\text{DSB}}(\Delta f)/2}{P_{\text{c}}}\right), \tag{2.1}$$

where Δf is the offset frequency relative to carrier, P_{c} is the carrier power and S_{DSB} represents the double-sideband spectral density of phase fluctuations.



(a) **(b)**

Fig. 2.1: An illustration of the difference between an ideal signal and a signal with phase noise in (a) time domain and (b) frequency domain.

2.1.1 Phase noise in time domain

In time domain, the output frequency of a synthesizer or oscillator can be expressed by the equation

$$v(t) = (A_0 + A(t)) \cos[2\pi f_0 t + \theta(t)] \, , \tag{2.2}$$

where f_0 is the frequency of operation, A_0 and $A(t)$ are the amplitude and amplitude variation and $\theta(t)$ is the phase variation or phase noise[6]. Oscillators have an amplitude limiting mechanism when the transistor or transistors are in compression which makes it relatively easy to design amplitude stable oscillators and synthesizers. $A(t)$ will therefore be assumed to be zero in this thesis. The phase noise can be represented as a frequency modulation of the carrier[14]

$$\theta(t) = \theta_\mathrm{p} \sin(2\pi f_\mathrm{m} t) \, , \tag{2.3}$$

where θ_p is the peak phase deviation and f_m is the modulation frequency. The peak phase deviation is also called modulation index and can be represented by

$$\theta_\mathrm{p} = \frac{\Delta f}{f_\mathrm{m}} \, . \tag{2.4}$$

Assuming $A(t) = 0$ and inserting (2.3) into (2.2) gives the expression

$$\begin{aligned} v(t) &= A_0 \cos[2\pi f_0 t + \theta_\mathrm{p} \sin(2\pi f_\mathrm{m} t)] = \\ &= A_0 \big[\cos(2\pi f_0 t) \cos[\theta_\mathrm{p} \sin(2\pi f_\mathrm{m} t)] - \sin(2\pi f_0 t) \sin[\theta_\mathrm{p} \sin(2\pi f_\mathrm{m} t)] \big] \, . \end{aligned} \tag{2.5}$$

By further assuming that the phase deviations are small, $\theta_\mathrm{p} \ll 1$, the small angle approximation, $\sin(x) \approx x$ and $\cos(x) \approx 1$, can be used to simplify (2.5). The expression

then becomes

$$\begin{aligned} v(t) &= A_0[\cos(2\pi f_0 t) - \theta_\mathrm{p}\sin(2\pi f_\mathrm{m} t)\sin(2\pi f_0 t)] = \\ &= A_0\big[\cos(2\pi f_0 t) - \frac{\theta_\mathrm{p}}{2}\big(\cos[2\pi(f_0+f_\mathrm{m})t] - \cos[2\pi(f_0-f_\mathrm{m})t]\big)\big] \ , \end{aligned} \tag{2.6}$$

where it can be seen that small phase or frequency deviations result in modulation sidebands at $f_0 \pm f_\mathrm{m}$[14]. The ratio between noise power in a single-sideband(SSB) and the carrier power can then be expressed as

$$\frac{S_\mathrm{SSB}}{P_\mathrm{c}} = \frac{|v(t)|^2/2}{A_0^2/2} = \frac{|v(t)|^2}{A_0^2} = \frac{(A_0\theta_\mathrm{p}/2)^2}{A_0^2} = \frac{\theta_\mathrm{p}^2}{4} \ , \tag{2.7}$$

where θ_p is the peak phase deviation. The IEEE definition of phase noise was in the beginning of Section 2.1 defined by half the double-sideband spectral density. By assuming that the noise spectrum is symmetric around the carrier frequency, i.e. the double-sideband noise power is twice the noise power in a single-sideband, the phase noise can be expressed as

$$\mathscr{L} = \frac{S_\mathrm{DSB}/2}{P_\mathrm{c}} = \frac{S_\mathrm{SSB}}{P_\mathrm{c}} = \frac{\theta_\mathrm{p}^2}{4} \ . \tag{2.8}$$

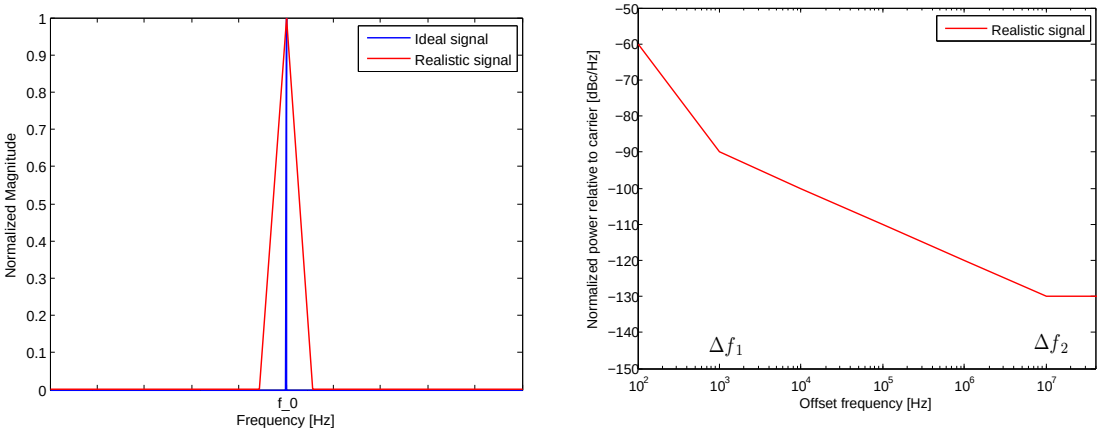
2.1.2 Phase noise in frequency domain

In the frequency domain an ideal signal is a delta function while in reality the signal is a band of frequencies, as is illustrated in Fig. 2.2 (a). This spectral broadening is caused by phase noise. The most commonly used way of representing phase noise is shown in Fig. 2.2 (b) where one sideband of the realistic signal in Fig. 2.2 (a) is plotted in logarithmic scale versus offset frequency. The phase noise in the graph is based on the oscillator phase noise model proposed by Leeson in 1966:

$$\mathscr{L}(\Delta f) = \left(\frac{\alpha}{\Delta f} + \frac{2k_\mathrm{B}TF}{P_\mathrm{s}}\right)\left[1 + \left(\frac{f_0}{2Q\Delta f}\right)^2\right] \ , \tag{2.9}$$

where k_B is Boltzmann's constant, T is the physical temperature, P_s is the oscillator input signal level, F is an effective noise figure and Q is the quality factor of the oscillator. α is a constant representing the level of up-converted flicker noise. In this graph the quality factor was chosen relatively high so that $\Delta f > f_0/2Q$ while the additional parameters were chosen to reach a noise floor at $\mathscr{L} = -130\,\mathrm{dBc/Hz}$. This choice of Q results in the respective slopes that can be seen in Fig. 2.2 (b):

Close to the carrier:	−30 dB/decade
Between Δf_1 and Δf_2 :	−10 dB/decade
Above Δf_2 :	0 dB/decade



(a) **(b)**

Fig. 2.2: An illustration of phase noise in (a) linear scale and (b) logarithmic scale.

If Q would have been been relatively low so that $\Delta f < f_0/2Q$ instead, the slope between Δf_1 and Δf_2 would be -20 dB/decade.

By comparing the spectrum of an ideal and a realistic signal, as shown in Fig. 2.2 (a), it is intuitive that the phase noise limits how closely channels can be spaced, as was stated in the beginning of the section.

From (2.9) it can be seen that the phase noise scales quadratically with frequency of operation:

$$\mathscr{L}(f_2) = \mathscr{L}(f_1)\left(\frac{f_2}{f_1}\right)^2 . \tag{2.10}$$

2.2 The PLL principle

A PLL is a feedback loop where the phases of the reference and output signal are compared. A block schematic of the PLL used in this study is shown in Fig. 2.3. As can be seen in the figure, the phase detector (PD) compares the phase of f_0 divided by the division number N with the phase of f_{ref}. Hence, if $f_{\text{ref}} = f_0/N$ the filter will not receive any signal from the phase detector. If $f_{\text{ref}} \neq f_0/N$ the filter will receive a signal of frequency equal to the difference of the two signals. The filter is designed so that the signal delivered to the VCO adjusts the output signal to the desired frequency.

There are three key performance limiting properties in a PLL: Lock-time, spurious frequencies and phase noise[15]. The lock-time is determined by the loop bandwidth[16]. A large loop bandwidth gives a fast locking time, which is one reason why a large loop bandwidth is generally desired. Another reason is that the VCO's phase noise is better suppressed near the carrier with a wider loop bandwidth. However, for a wider

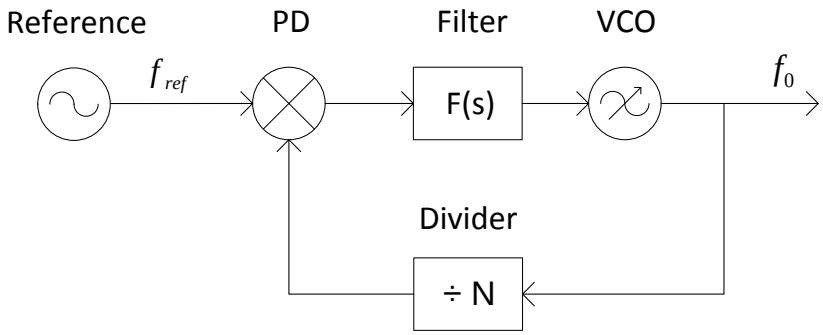


Fig. 2.3: A block schematic of the PLL.

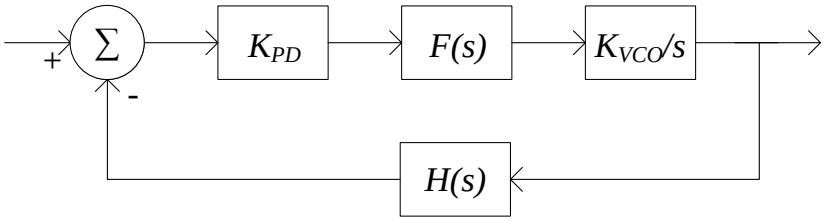


Fig. 2.4: A block schematic of the PLL in Laplace domain.

bandwidth the phase noise of the reference, phase detector and frequency divider is less suppressed far away from the carrier. Hence, there is a trade-off which needs to be considered when designing a synthesizer. Spurious frequencies are unwanted frequency components in the signal. In PLLs these are normally not a problem as long as they are located outside the loop bandwidth where they are filtered. Phase noise is the property which will be investigated thoroughly in this thesis, while the lock-time and spurious output will be discussed only briefly.

2.2.1 Linear PLL-model

In this thesis a linear PLL-model is used[4]-[6], a block diagram of this model in Laplace domain is shown in Fig. 2.4. The linear model can be found in several textbooks and articles where it has been verified to be a very accurate[7],[9],[16]-[18]. As can be seen in the diagram, the VCO is modeled as an integrator which adds a $1/s$-factor in the Laplace domain[6]. The phase detector is modeled as a linear device, which means that it has the same output amplitude for all input frequencies. This is generally not true, but has been used as a rule of thumb in many PLL calculations with only a few percent error[6]. Therefore the linear phase detector model will also be used in this thesis.

PLL transfer functions

There are a few important transfer functions in a PLL which will be presented below. The first one is the feed-forward function, which is the transfer function for a signal going from the input to the output, see Fig. 2.4. It is defined in the Laplace domain by:

$$G(s) = 2\pi \frac{K_{\mathrm{pd}} K_{\mathrm{vco}}}{s} F(s) \ , \tag{2.11}$$

where K_{pd} is the phase detector constant, K_{vco} is the VCO gain or sensitivity and $F(s)$ is the loop filter transfer function[6].

The feedback transfer function is the transfer function from the output back to the phase detector, see Fig. 2.4. Assuming that there is no time delay in the divider this function is simply a division by N:

$$H(s) = \frac{1}{N} \ . \tag{2.12}$$

The open-loop function is determined by the feed-forward and the feedback function[9] and is defined as

$$G_{\mathrm{ol}}(s) = G(s)H(s) = 2\pi \frac{K_{\mathrm{pd}} K_{\mathrm{vco}}}{sN} F(s) \ . \tag{2.13}$$

Once the open-loop transfer function has been defined, the transfer functions which will be used for phase noise calculations can be presented. The transfer function which describes how phase noise generated in the phase detector, reference source or frequency divider appears at the PLL-output will have low-pass characteristics[9],[11],[17] and it is known as the closed loop transfer function. It can be expressed as

$$G_{\mathrm{lp}}(s) = \frac{G_{\mathrm{ol}}(s)}{1 + G_{\mathrm{ol}}(s)} \ . \tag{2.14}$$

The phase noise generated in the VCO will be reduced by the gain of the loop filter at low frequencies and will therefore have high-pass characteristics[9],[11],[17]. It can be expressed as

$$G_{\mathrm{hp}}(s) = \frac{1}{1 + G_{\mathrm{ol}}(s)} \ . \tag{2.15}$$

Loop stability

The criterion for closed loop stability is that there should be no pole in the right half plane (RHP) of the complex closed loop transfer function[19]. Closed loop stability can be verified from the Nyquist stability criterion, which states that if $G_{\mathrm{ol}}(s)$ does not have poles in RHP, then the closed loop transfer function is stable if the Nyquist curve of $G_{\mathrm{ol}}(s)$ does not encircle the critical point -1[19]. The Nyquist curve of a function is the function plotted in the complex plane versus frequency. Some authors prefer to analyze the stability through phase and gain margin, which can be determined from the Bode

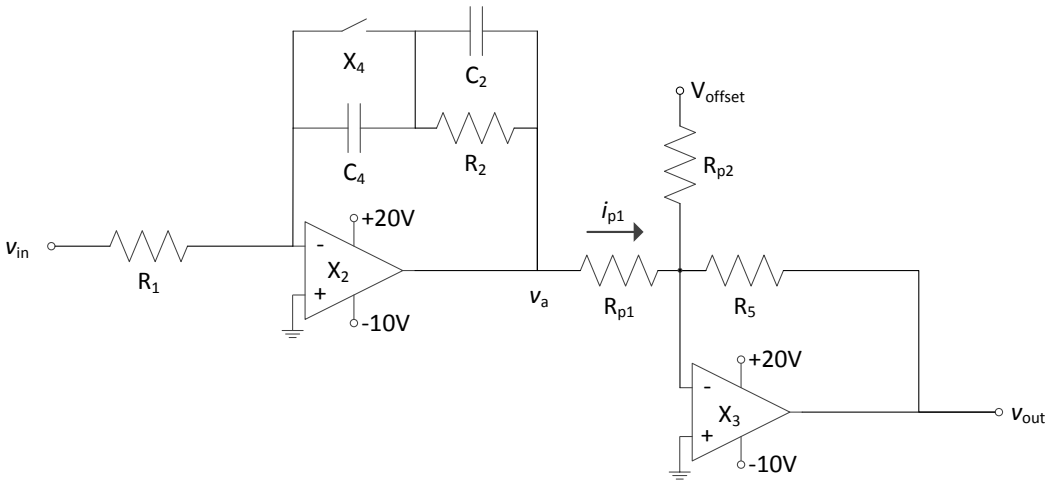


Fig. 2.5: A simplified schematic of the loop filter used in this design.

plot of $G_{\text{ol}}(s)$[20],[21]. This method is valuable for finding a good trade-off between stability and response time but is not applicable on all systems. For instance, if the phase of $G_{\text{ol}}(s)$ does not reach $-180°$, the gain margin cannot be calculated. This is the case in this thesis, because $\angle G_{\text{ol}}(s) \to -180°$ only when $f \to \pm\infty$ which makes it impossible to determine the gain margin. Therefore, Nyquist stability criterion is used to verify the stability of this PLL.

2.2.2 The loop filter

The loop filter is an important part of the PLL which determines phase noise performance of the PLL and the loop bandwidth which in turn, as mentioned in Section 2.2, determines the lock-time. There are many different topologies of both active and passive loop filters, some general examples can be found in e.g. [5],[6],[20]. A PLL is often described by its order which is determined by the filter. For example, a simple low-pass RC-filter, which has one pole, together with an integrating VCO provides a second order PLL.

The PLL studied in this thesis is a combination of a second and a third order with an active loop filter. The simplified schematic of the filter is shown in Fig. 2.5. The switch X_4 is what makes this a combination of second and third order loop. When the PLL is unlocked, X_4 is digitally closed so that C_4 is short-circuited. Then the loop filter has one pole which makes it a second order PLL. When the PLL is locked, X_4 is opened so that an extra pole is introduced by C_4, which makes it a third order loop. This topology makes it possible to achieve a high loop bandwidth and fast lock-time before the PLL is locked and a high gain and low phase noise when the PLL is locked.

The resistors R_{p1} and R_{p2} in Fig. 2.5 are variable in the sense that they both consist of eight parallel resistors with digitally controlled switches. Since R_{p1} is variable it will

be possible to digitally adjust the gain of the loop filter and thereby optimize the phase noise performance for every output frequency. Since R_{p2} is variable it will be possible to add an offset DC voltage output by using the summing OP AMP X_3. This is easily realized by applying Kirchoff's current law (KCL) in the input node of X_3:

$$\frac{v_{\mathrm{out}}}{R_5} + \frac{V_{\mathrm{offset}}}{R_{\mathrm{p2}}} + i_{\mathrm{p1}} = 0 \quad \Rightarrow \quad v_{\mathrm{out}} = -\left(\frac{V_{\mathrm{offset}}}{R_{\mathrm{p2}}} + i_{\mathrm{p1}}\right) R_5 \ . \tag{2.16}$$

This can be re-formulated to

$$v_{\mathrm{out}} = V_{\mathrm{out}} + v'_{\mathrm{out}} \ , \tag{2.17}$$

where $V_{\mathrm{out}} = V_{\mathrm{offset}} R_5 / R_{\mathrm{p2}}$ represents the offset DC voltage and $v'_{\mathrm{out}} = i_{\mathrm{p1}} R_5$ represents the small signal voltage. The variable DC offset will make it possible to digitally set the signal level at the input of the VCO and thereby reduce the lock-time considerably.

Filter transfer function

The filter transfer function is found by circuit analysis. Since V_{offset} only adds a DC offset it is assumed to be zero in the small signal transfer function. The transfer function will be derived only for the case when X_4 is open, which is when the PLL is locked. The reason for this is because the phase noise has only been analyzed in locked state since this is the state of concern. The loop filter transfer function is found by applying KCL to the circuit in Fig. 2.5:

$$\begin{cases} \dfrac{v_{\mathrm{in}}}{R_1} + \dfrac{v_{\mathrm{a}}}{1/sC_4 + R_2/(1 + sC_2R_2)} = 0 \\ \dfrac{v_{\mathrm{a}}}{R_{\mathrm{p1}}} + \dfrac{v_{\mathrm{out}}}{R_5} = 0 \end{cases}$$

$$\Rightarrow \ F(s) = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{R_5}{R_{\mathrm{p1}}}\left(\frac{1}{sC_4R_1} + \frac{R_2}{R_1 + sC_2R_1R_2}\right) . \tag{2.18}$$

Here it can be seen that the gain of the loop filter can be adjusted by the factor R_{p1}/R_5 as was mentioned in the previous section.

By looking at (2.11)-(2.15) it can bee seen that the filter function $F(s)$ determines the break point in the low-pass and high-pass transfer functions. For low offset frequencies $G_{\mathrm{lp}} \approx 1$ but after the break point $G_{\mathrm{lp}} < 1$. This means that phase noise from the reference, phase detector and divider will remain the same for low offset frequencies but be suppressed for high offset frequencies. However $G_{\mathrm{hp}} < 1$ for low frequencies and $G_{\mathrm{hp}} \approx 1$ for high frequencies, which means that the phase noise from the VCO will be suppressed for low offset frequencies and remain the same for high offset frequencies. This breakpoint, where the phase noise from the VCO starts to dominate over the phase noise from the reference, phase detector and divider is what defines the loop bandwidth of the PLL.

Filter gain and offset voltage constant

From (2.18) it can be seen that R_5/R_{p1} represents a proportional gain factor. This gain factor is constant for each output frequency selected, which means that R_{p1} is proportional to R_5:

$$R_{\mathrm{p1}} \propto R_5 \ . \tag{2.19}$$

In a similar way it can bee seen from (2.16) that R_5/R_{p2} represents an offset constant and that

$$R_{\mathrm{p2}} \propto R_5 \ . \tag{2.20}$$

2.3 Synthesizer output phase noise

The total phase noise at the output of the synthesizer will be the sum of the contribution from all its components. As was explained throughout Section 2.2, each component has a specific transfer function depending on where in the PLL it is located. With these transfer functions the phase noise of a component can be measured when it's not connected in a PLL and then its contribution at the output of the synthesizer can be calculated. This method has been verified in many previous works, a few examples are [9]-[11]. The different transfer functions that can be used to calculate each component's phase noise contribution at the synthesizer output are:

Reference source:	$\mathscr{L}_{\mathrm{ref,\ pll}} = \mathscr{L}_{\mathrm{ref}} \lvert G_{\mathrm{lp}}(s) \rvert^2 N^2$	(2.21)
Phase detector:	$\mathscr{L}_{\mathrm{pd,\ pll}} = \mathscr{L}_{\mathrm{pd}} \lvert G_{\mathrm{lp}}(s) \rvert^2 N^2$	(2.22)
Frequency divider:	$\mathscr{L}_{\mathrm{div,\ pll}} = \mathscr{L}_{\mathrm{div}} \lvert G_{\mathrm{lp}}(s) \rvert^2 N^2$	(2.23)
VCO:	$\mathscr{L}_{\mathrm{vco,\ pll}} = \mathscr{L}_{\mathrm{vco}} \lvert G_{\mathrm{hp}}(s) \rvert^2$	(2.24)

The transfer functions $G_{\mathrm{hp}}(s)$ and $G_{\mathrm{lp}}(s)$ were derived in (2.14) and (2.15). The division number N has been included in the low-pass transfer functions to up-convert the phase noise at the device's operation frequency to the PLL output frequency according to (2.10).

2.3.1 Voltage noise in the loop filter

The voltage noise generated in the loop filter, e.g. thermal noise from resistors and voltage and current noise from OP AMPs will add fluctuations to the control voltage on the VCO's input. These fluctuations will appear as a phase deviation at the VCO's output and can be calculated by:

$$\theta_{\mathrm{p}}(\Delta f) = \frac{\sqrt{2}\, K_{\mathrm{vco}}\, v_{\mathrm{rms}}}{\Delta f} \ , \tag{2.25}$$

where v_{rms} is the root mean square (rms) voltage noise at the input of the VCO[9],[10]. From (2.8), the loop filter phase noise can then be calculated from the phase deviation:

$$\mathscr{L}_{\text{filter}}(\Delta f) = \frac{1}{4}\left(\frac{\sqrt{2}\,K_{\text{vco}}\,v_{\text{rms}}}{\Delta f}\right)^2 = \frac{1}{2}\left(\frac{K_{\text{vco}}\,v_{\text{rms}}}{\Delta f}\right)^2 . \tag{2.26}$$

Since this phase noise is at the output of the VCO it will have the same transfer function as the VCO phase noise, i.e. (2.15). The total phase noise contribution of the filter at the output of the synthesizer then becomes

$$\mathscr{L}_{\text{filter, pll}}(\Delta f) = \mathscr{L}_{\text{filter}}(\Delta f)|G_{\text{hp}}(s)|^2 \tag{2.27}$$

Thermal noise from resistors

At baseband, the thermal noise, or Johnson–Nyquist noise, from a resistance is generally expressed as a voltage noise source with rms voltage equal to

$$v_{\text{rms}} = \sqrt{4k_{\text{B}}TR}\,, \tag{2.28}$$

where R is the resistance[10]. The thermal noise is uncorrelated and different voltage noise sources will add as the root mean square of each noise voltage[22], that is

$$v_{\text{rms, tot}} = \sqrt{v_{\text{rms, 1}}^2 + v_{\text{rms, 2}}^2 + v_{\text{rms, 3}}^2 + \dots}\,. \tag{2.29}$$

The thermal noise of parallel and series resistors will be the thermal noise of the total equivalent resistance of the parallel or series combination.

Noise from operational amplifiers

The noise from OP AMPs is generally provided in the data-sheet as rms voltage and current noise at the input. The voltage noise can be modeled as a voltage noise source placed at the input of the amplifier and treated in the same manner as resistors, as was described in (2.29). The current noise will cause a voltage noise when it flows through the surrounding resistors. Looking at the example in Fig. 2.6, the current noise will spread out through all the surrounding resistors[22]. The equivalent voltage noise can be found from the parallel combination of R_{A}, R_{B} and R_{C}:

$$v_{\text{current, rms}} = \left(\frac{1}{R_{\text{A}}} + \frac{1}{R_{\text{B}}} + \frac{1}{R_{\text{C}}}\right)^{-1} i_{rms}\,. \tag{2.30}$$

Now the current noise can be modeled as a voltage noise source and treated in the same manner as was described in (2.29).

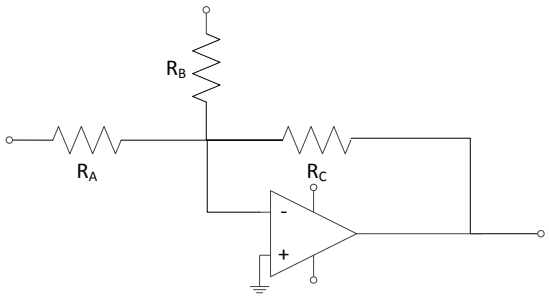


Fig. 2.6: Example of an operational amplifier circuit.

Chapter 3

Synthesizer design verification

This chapter motivates and discusses the choice of components in the synthesizer. It also displays measurement results performed on individual components, explains measurement procedures and presents the instruments used during this work.

3.1 PLL design

The synthesizer analysed in this thesis consists of a reference source, phase detector, VCO, frequency divider and loop filter, configured as was described in section 2.2. Aside from these components, passive filters, attenuators and some DC-feed networks are located throughout the circuit. There are also Low noise amplifiers (LNAs) placed on the phase detector's inputs to increase the power level of the signal for better performance. These LNAs were selected with minimal phase noise contribution in mind and were therefore assumed to not add any phase noise to the PLL's output. The signal to noise ratio was however considered so that the LNA did not amplify the noise floor to unreasonable levels. All components are matched to $50\,\Omega$ so there is no need for matching networks, only $50\,\Omega$ transmission lines. The only exception to this is the input of the VCO which is high impedance, but since the signal after the mixer is DC or very low frequency there is no need for a matching network there either.

The reference, phase detector, VCO, divider and loop filter are the components which are important from a phase noise perspective and they will be presented in detail below. The layout and a list of additional components can be found in Appendix A and B. The phase noise for some of the components will be given for the offset frequency $\Delta f = 1\,\text{MHz}$ and scaled to an operating frequency of $f_0 = 3120\,\text{MHz}$. The reason for this is that the complete synthesizer has shown a large increase of phase noise at offset frequencies above $100\,\text{kHz}$, which makes $\Delta f = 1\,\text{MHz}$ a good frequency for comparison. The reason to choose to compare phase noise at operation frequency $f_0 = 3120\,\text{MHz}$ is simply because it is the frequency which has been most closely analysed throughout this project.

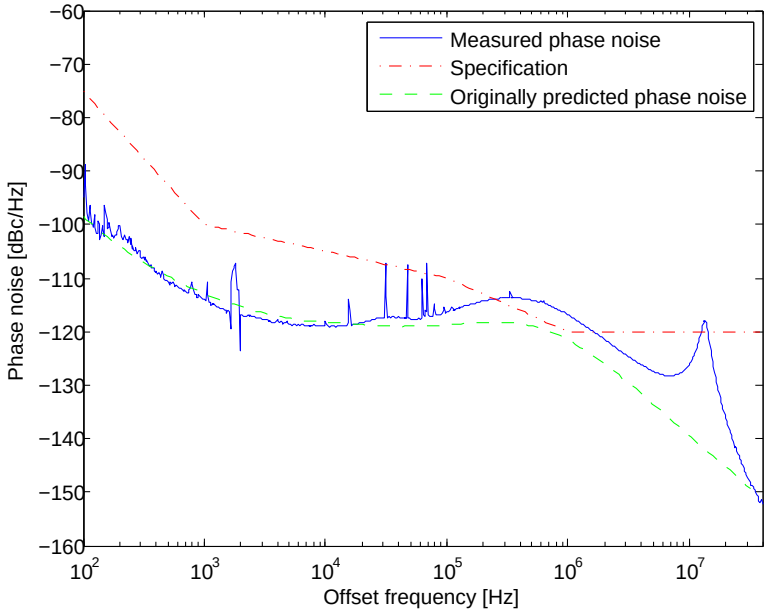


Fig. 3.1: Measured phase noise for $f_0 = 3120\,\text{MHz}$, originally predicted phase noise for $f_0 = 3120\,\text{MHz}$ and the design specification for $2340\,\text{MHz} < f_0 < 4420\,\text{MHz}$.

The goal of this work is to achieve a phase noise lower than ESA's specification for the whole frequency band, $2340\,\text{MHz} < f_0 < 4420\,\text{MHz}$. The phase noise specification is shown in Fig. 3.1 together with measured phase noise of the original design at $f_0 = 3120\,\text{MHz}$. In the same graph the original phase noise model, where phase noise contribution from the filter is not taken into account, is also plotted for $f_0 = 3120\,\text{MHz}$. As can be seen in the graph, the measured phase noise is several decibels higher than predicted for offset frequencies above 100 kHz, as was stated above. It is also worth noting the peak around $\Delta f = 13.5\,\text{MHz}$, which showed up on several measurements and is not caused by the synthesizer itself. It is most likely interference from other measurement equipment and was disregarded in this analysis.

3.1.1 Reference source

In this study the reference signal is generated from a QuickSyn FSW-0010 synthesizer from National Instruments. The spectral purity of this synthesizer is not comparable with state-of-the-art oscillator crystals, but unlike a crystal it is tunable and easily controlled from a PC using USB cable.

The phase noise at the required reference frequency $f_{\text{ref}} = 260\,\text{MHz}$ was measured to be $-141.7\,\text{dBc/Hz}$ at $\Delta f = 1\,\text{MHz}$. Using (2.10) this can be scaled to a phase noise of $\mathscr{L} = -120.1\,\text{dBc/Hz}$ at operating frequency $f_0 = 3120\,\text{MHz}$. One example of a reference source with similar phase noise behaviour can be found in [23], which at operating frequency $f_{\text{ref}} = 100\,\text{MHz}$ measured a phase noise of $\mathscr{L} = -174.0\,\text{dBc/Hz}$ at offset

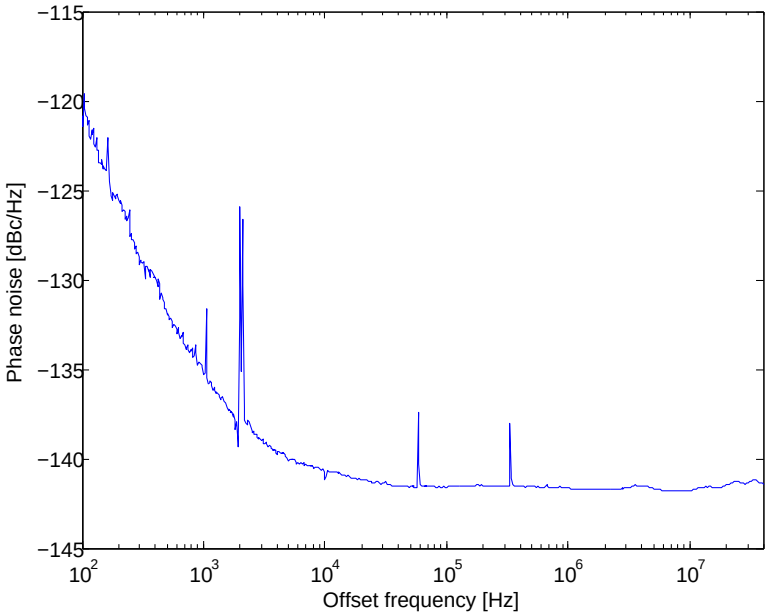


Fig. 3.2: Measured phase noise of reference signal at $f = 260\,\text{MHz}$.

frequency $\Delta f = 1\,\text{MHz}$. By again using (2.10), this can be scaled to a phase noise of $\mathscr{L} = -144.1\,\text{dBc/Hz}$ at the operating frequency $f_0 = 3120\,\text{MHz}$. Hence, there are reference sources with better phase noise performance, but since the phase noise in the QuickSyn synthesizer is sufficient to verify the accuracy of the model developed in this thesis, while it also can be easily controlled via PC, it is a suitable choice for this prototype.

The power level of the reference signal was $P = -2\,\text{dBm}$ at the input of the LNA during all measurements. This power level was chosen as high as possible without pushing the LNA into compression.

Improved reference signal for simulations

The reference source presented above will be replaced with a higher performance reference in the final synthesizer design. In order to be able to illustrate the complete PLL's performance in the final design, an improved reference was used in some of the simulations. The data from this improved reference was taken from measurements performed on a 250 MHz oscillator used in other products at RUAG. The fact that these references are in the same frequency region suggests that it is reasonable to assume that a similar performance could be achieved for 260 MHz. The measured phase noise of the improved reference is shown in Fig. 3.3. This phase noise was scaled to 260 MHz, using (2.10), in the simulations.

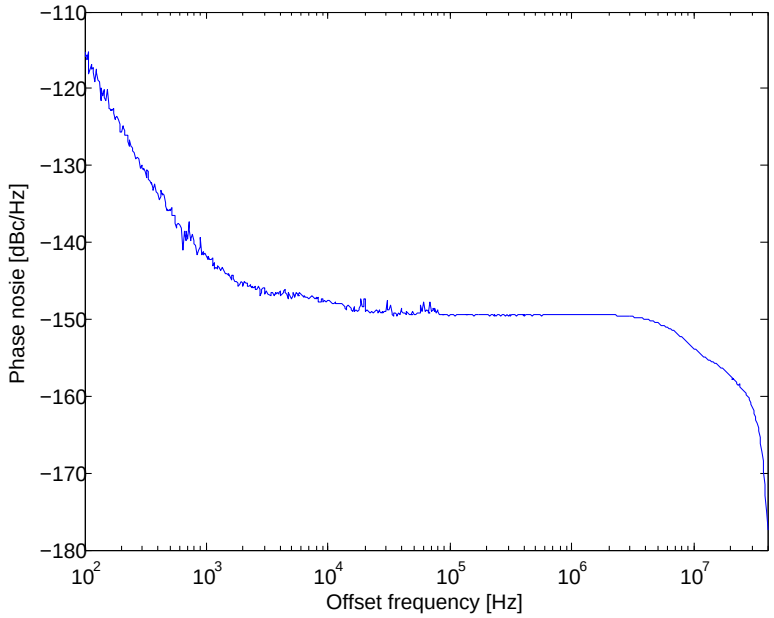


Fig. 3.3: Measured phase noise of improved reference signal at $f = 250\,\mathrm{MHz}$.

Tab. 3.1: Some parameters from the HMC3589LC4B data-sheet.

Parameter	**Specification**	**Unit**
Frequency range	$2.25 - 4.5$	GHz
Output power	$0 - 7$	dBm
Phase noise at $\Delta f = 100\,\mathrm{kHz}$	-95	dBc/Hz
Tuning voltage	$-0.5 - 20$	V
Tuning sensitivity	$70 - 175$	$\mathrm{MHz\,V^{-1}}$

3.1.2 Voltage controlled oscillator

The VCO used in this synthesizer is a wide-band VCO from Hittite which, at the time of writing, has not yet been made available for purchase. The VCO's product ID is HMC3589LC4B, some of its parameters according to the data-sheet are listed in Table 3.1.

In this design the most critical requirement on the VCO is that tuning range should cover $2340\,\mathrm{MHz} < f_0 < 4420\,\mathrm{MHz}$. After meeting this criteria the only concern is to have as low phase noise as possible. HMC3589LC4B was chosen because it was found to best meet these specifications. The phase noise of the VCO was measured for three different frequencies, the result is shown in Fig. 3.4. As can be seen in the graph, the phase noise is around $\mathscr{L} = -128.9\,\mathrm{dBc/Hz}$ at $\Delta f = 1\,\mathrm{MHz}$ for $f_0 = 3120\,\mathrm{MHz}$. It can also be seen that the phase noise is below $\mathscr{L} = -104.3\,\mathrm{dBc/Hz}$ at $\Delta f = 1\,\mathrm{MHz}$

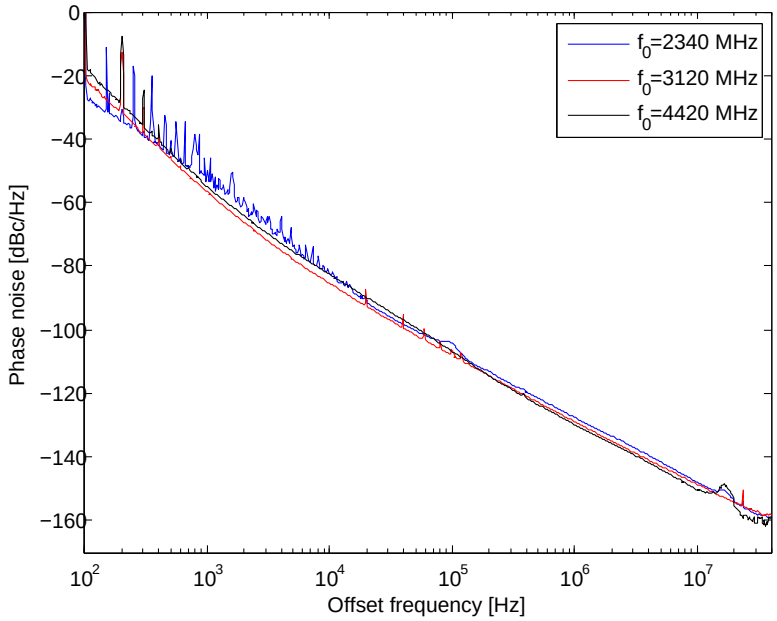


Fig. 3.4: Phase noise measurements of free-running VCO for three different output frequencies.

for all three frequencies, which is 9.3 dB better than specification. The sensitivity was also measured and is shown in Fig. 3.5. As can be seen in the graph, the sensitivity is fairly constant within the band, $2340\,\mathrm{MHz} < f_0 < 4420\,\mathrm{MHz}$. At $f_0 = 3120\,\mathrm{MHz}$ it was measured to be:

$$K_{\mathrm{vco}} = 154.1\,\mathrm{MHz\,V^{-1}}\ .$$

For comparison, a few different VCOs are presented in Table 3.2, where it can be seen that the performance of the VCO is comparable with state-of-the art designs, especially considering the wide tuning range.

3.1.3 Phase detector

This design utilizes the mixer ADE-1 from Mini Circuits as phase detector. When the PLL is in locked state, the output of the mixer is DC or very low frequency. Hence, there is no carrier out from the mixer and therefore the transfer function (2.22) cannot be used to calculate this phase noise contribution. Instead, the noise added from the mixer must be modeled as a noise voltage source and added to the voltage noise in the loop filter according to the theory in Section 2.3.1. However, this analysis could not be performed during this work. The noise generated in the mixer could not be measured because it was below the noise floor of the measurement system, which was $30\,\mathrm{nV}\,\sqrt{\mathrm{Hz}}^{-1}$ at baseband frequency 100 Hz and $300\,\mathrm{pV}\,\sqrt{\mathrm{Hz}}^{-1}$ at 100 kHz. This is very low compared to the noise in the loop filter and it is therefore negligible and should not have any significant effect in noise analysis of the complete PLL.

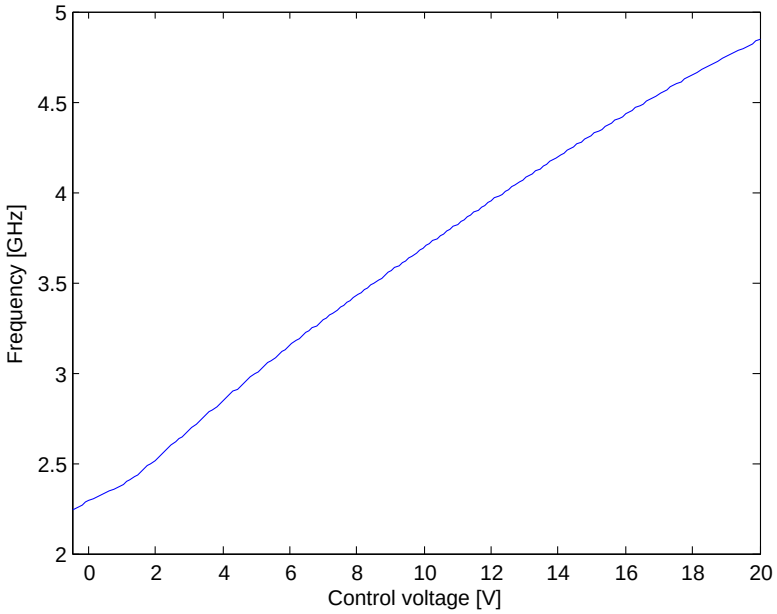


Fig. 3.5: Measurement of the VCO sensitivity.

Tab. 3.2: A comparison between different VCOs.

	Freq. range [GHz]	**Freq. range** [%]	$\mathscr{L}$ [dBc/Hz]	**Δf** [kHz]	**Ref.**
CMOS	1.14 – 2.46	73.3	−123.5	600	[24]
Si BJT	5.4 – 7.5	32.6	−90.5	100	[25]
InGaP/GaAs HBT	6.1 – 7.6	21.9	−101	100	[26]
SiGe HBT	3.85 – 4.40	13.3	−106	100	[27]
AlGaN/GaN HEMT	5.7 – 6.3	10	−92	100	[28]
AlGaN/GaN HEMT	6.5 – 7.5	14.3	−81	100	[29]
HMC3589LC4B	2.25 – 4.5	66.7	−104.3	100	This work

The phase detector constant, K_{pd} in (2.11), describes how much the phase detector output voltage is changed for a change in the phase at the input. K_{pd} can be determined by looking at the output of the phase detector with two different input frequencies. For a mixer, K_{pd} is the peak-to-peak voltage, $v_{\text{p-p}}$, divided by $\pi/2$ radians. The output of the mixer was measured with an oscilloscope for a few different f_{RF} while f_{LO} was held at the reference frequency $f_{\text{LO}} = 260\,\text{MHz}$. The power level of the two signals were $P_{\text{LO}} = 14\,\text{dBm}$ and $P_{\text{RF}} = -2\,\text{dBm}$ which are approximately the same power levels as in the actual PLL at $f_0 = 3120\,\text{MHz}$. The result is shown in Fig. 3.6. As can be seen in the graph, $v_{\text{p-p}} = 260\,\text{mV}$ and it remains fairly constant for all the frequencies. This

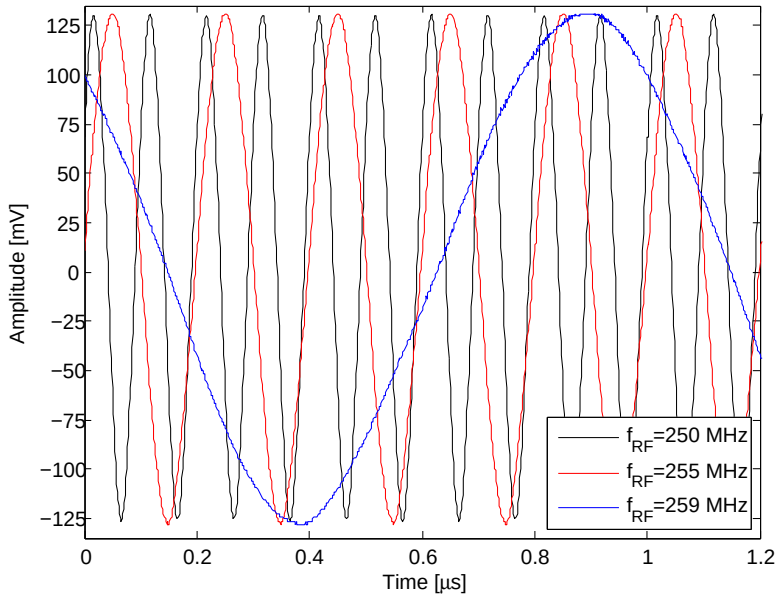


Fig. 3.6: Measurements of phase detector IF output for $f_{\mathrm{LO}} = 260\,\mathrm{MHz}$ and three different f_{RF}.

results in a phase detector constant of

$$K_{pd} = \frac{v_{\mathrm{p-p}}}{\pi/2} = \frac{260}{\pi/2} = 166\,\mathrm{mV\,rad^{-1}}$$

3.1.4 Frequency divider

The frequency divider used in this synthesizer is a low noise GaAs HBT programmable divider from Hittite, HMC705LP4, with division number between $1 < N < 17$ for operation frequencies up to 6.5 GHz. The phase noise performance according to the data-sheet of this divider is shown in Fig. 3.7 for $f_{\mathrm{div,in}} = 6\,\mathrm{GHz}$ and $N = 17$, which corresponds to an output frequency of $f_0 = 353\,\mathrm{MHz}$. As can be seen in the figure, the phase noise is $\mathscr{L} = -155\,\mathrm{dBc/Hz}$ at offset frequency $\Delta f = 1\,\mathrm{MHz}$. Using (2.10), this can be scaled to a phase noise of $\mathscr{L} = -136.1\,\mathrm{dBc/Hz}$ at output frequency $f_0 = 3120\,\mathrm{MHz}$. This phase noise is 16 dB lower than the reference signal and will therefore be negligible in comparison. Because of limited time and resources, the phase noise of the phase detector was not measured during this work. It has however been measured previously by designers at RUAG, which verified the values in the data-sheet.

When choosing a frequency divider for this synthesizer, two criteria must be fulfilled. The first one is to cover the synthesizer bandwidth, $2340\,\mathrm{MHz} < f_0 < 4420\,\mathrm{MHz}$, and the second one is to cover the desirable division numbers which in this case are all integers between $9 < N < 17$. It is also desirable to have as constant output power as possible. This simplifies the circuitry between the divider and phase detector if the phase

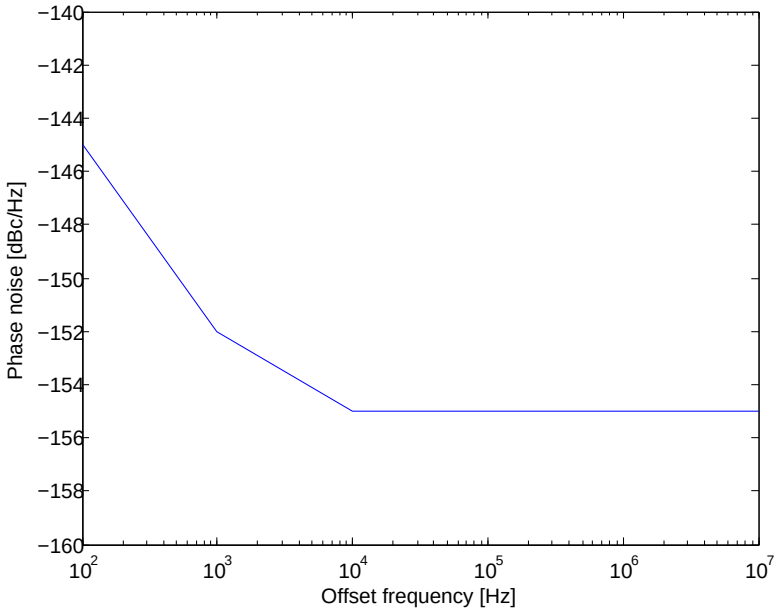


Fig. 3.7: Divider phase noise from data-sheet for $f_{\mathrm{div,out}} = 353\,\mathrm{MHz}$.

detector performance is affected by power level differences. The phase noise performance is generally not very critical since it is often negligible compared to the phase detector and reference signal. The two criteria are clearly fulfilled, and as can be seen in Fig. 3.7 the phase noise is much lower than the phase noise of the reference source. This divider was chosen because it showed a more constant output power compared to alternatives.

3.1.5 Loop filter

As was discussed in Section 2.2.2, OP AMPs and resistors generate voltage noise, which is translated to phase noise by the VCO. This is mostly a problem for VCOs with high sensitivity, since the magnitude of the phase noise scales linearly with K_{vco}. In this design, a wide bandwidth is required which requires a high sensitivity. To reach the higher output frequencies, a high filter output voltage is also required. For the highest operation frequency, $f_0 = 4420\,\mathrm{MHz}$ the voltage at the output of the filter needs to be $v_{out} \approx 16\,\mathrm{V}$. In locked state, the small signal level is very low, which from (2.17) means that the DC offset voltage must be $V_{out} \approx 16\,\mathrm{V}$. Achieving this high filter output voltage can be difficult as will be discussed further below.

Case 1: Original filter topology

A schematic of the complete original loop filter design is shown in Fig. 3.8 and all the passive component values are listed in Tab. 3.3. Note that R_5 is constant but was

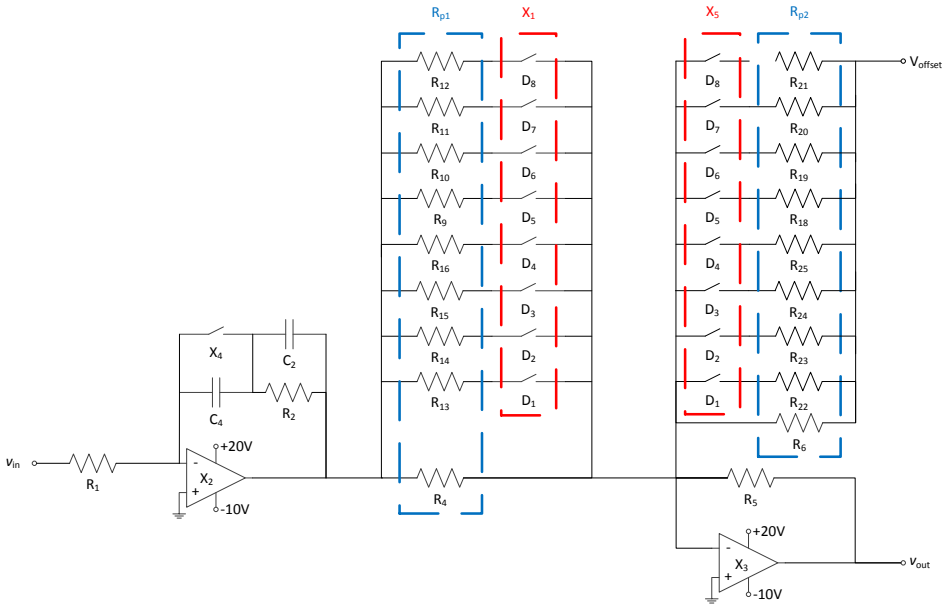


Fig. 3.8: Schematic of the original loop filter topology.

Tab. 3.3: Component values in the original loop filter topology.

$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{C_2}$	$\mathbf{C_4}$	$\mathbf{R_{p1}}$	$\mathbf{R_{p2}}$	$\mathbf{R_5}$
51.3 Ω	51.3 Ω	22 pF	22 nF	Variable	Variable	Constant

varied during the analysis, while R_{p1} and R_{p2} can be digitally adjusted to optimize the performance for every output frequency.

X_1, X_4 and X_5 are active switches from Analog Devices, where X_1 and X_5 are serial pulse-controlled 8-channel switches, ADG1414BRUZ, and X_4 is a single channel switch, ADG741BKS. In order to perform an accurate noise analysis of the loop filter, the synthesizer was re-fabricated without switches. This eliminated parasitics and on-resistances in the switches which allowed for a more accurate filter model. In the measurements performed in this thesis, R_{p1} and R_{p2} were replaced with fixed resistances while the switch X_4 was replaced with a mechanical switch. The OP AMPs, X_2-X_3, are high performance OP AMPs from Texas Instruments, OPA161, with low noise, 1.1 nV $\sqrt{\mathrm{Hz}}^{-1}$ and 1.7 pA $\sqrt{\mathrm{Hz}}^{-1}$ at 1 kHz, and wide bandwidth, 40 MHz. The maximum allowed short-circuit current for this OP AMP is $I_{sc} = 55$ mA at room temperature, which during this work was higher than other OP AMPs with comparable noise performance and bandwidth. However, this design assumes a maximum short-circuit current of $I_{sc} = 25$ mA in order to allow for alternative OP AMPs, since the availability of space qualified OP AMPs is quite limited.

The total equivalent voltage noise of the circuit can be found by using (2.29), where

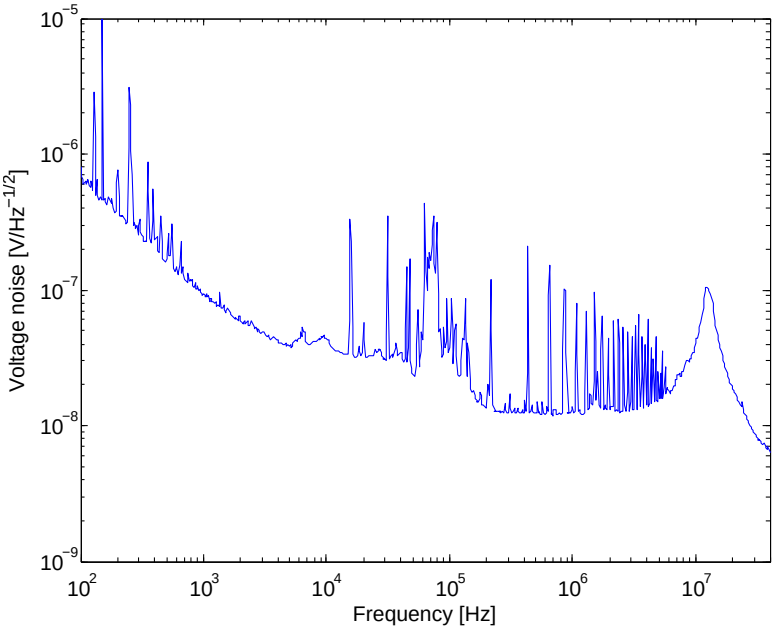


Fig. 3.9: Measurement of original filter design with 50 Ω-termination at the input.

(2.30) is used for the OP AMPs current noise and (2.28) for all resistors. Then the total noise voltage at the output of the filter (and input of the VCO) can be found:

$$\begin{aligned} v^2_{rms,\,tot} = {} & v^2_{rms,\,OP\ AMP1} + \left(\frac{1}{R_1} + \frac{1}{R_2}\right)^{-2} i^2_{rms,\,OP\ AMP1} + \ldots \\ & + v^2_{rms,\,OP\ AMP2} + \left(\frac{1}{R_{p1}} + \frac{1}{R_{p2}} + \frac{1}{R_5}\right)^{-2} i^2_{rms,\,OP\ AMP2} + \ldots. \\ & + 4k_BTR_1 + 4k_BTR_2 + 4k_BTR_{p1} + 4k_BTR_{p2} + 4k_BTR_5\ . \end{aligned} \tag{3.1}$$

The phase noise caused by this voltage noise can be calculated from (2.27).

The component values for the original filter design were $R_{\mathrm{p1}} = 6030\,\Omega$, $R_{\mathrm{p2}} = 4420\,\Omega$ and $R_5 = 2730\,\Omega$ together with the values presented in Tab. 3.3. Inserting these into (3.1) at $T = 298\,\mathrm{K}$ results in a total equivalent voltage noise of

$$v_{\mathrm{rms,\,tot}} = 15.0\,\mathrm{nV}\,\sqrt{\mathrm{Hz}}^{-1}\ .$$

By terminating the input of the filter with 50 Ω and applying the DC feed to the OP AMPs the baseband voltage noise could be measured. The result is shown in Fig. 3.9, measured at temperature $T = 298\,\mathrm{K}$. As can be seen in the figure, the calculated voltage noise agrees well with the measurement around $f = 100\,\mathrm{kHz}$. When this voltage noise is translated to phase noise in the VCO, the voltage noise at $f = 100\,\mathrm{kHz}$ will produce a

phase noise at an offset frequency $\Delta f = 100\,\text{kHz}$. It can also be seen in the graph that the voltage noise is higher at lower frequencies. This is natural because the OP AMPs are noisier at lower frequencies, a feature which have been neglected in this thesis because this noise is heavily suppressed by the PLL at low offset frequencies. Furthermore, there is a peak around $f = 12\,\text{MHz}$ in Fig. 3.9 which have been disregarded in the calculations. It showed up on all baseband measurements, even in measurements on a single resistor, and the reason is most likely interference from other devices in the lab.

Maximum current in the filter

As was mentioned earlier in this section, the higher output frequencies require a higher filter output voltage. This puts a requirement on the loop filter, since this voltage needs to be generated by the second OP AMP and the feedback resistor. The maximum current that the OP AMP need to be able to deliver is

$$I_{\text{max}} = \frac{V_{\text{out, max}} - 0\,\text{V}}{R_5} = \frac{16\,\text{V}}{R_5}\,. \tag{3.2}$$

This means that the limited output current of the OP AMPs limits how small R_5 can be chosen. According to (2.19) and (2.20), R_{p1} and R_{p2} scales linearly with R_5. It is desirable to reduce the size of these resistances which, since the high output voltage is necessary, means that I_{max} needs to be increased. To simplify the nomenclature in this thesis, where simulations and measurements are performed for several different resistances, the parameter k can be introduced to represent the factor with which the resistances are reduced:

$$k = \frac{R_{5,\text{ original value}}}{R_{5,\text{ new value}}} = \frac{R_{\text{p1, original value}}}{R_{\text{p1, new value}}} = \frac{R_{\text{p2, original value}}}{R_{\text{p2, new value}}}\,. \tag{3.3}$$

Case 2: Modified loop filter topology

In order to allow for smaller resistances in the loop filter, a transistor was placed at the output of the second OP AMP, X_3 which makes it possible to drive a higher current. The transistor chosen for this design was a bipolar Si-NPN transistor, 2N2219A, from STMicroelectronics. This transistor can amplify the loop filter current up to 800 mA which means that the resistances can be greatly reduced according to (3.2) and (3.3). To prevent oscillations in the feedback loop a small resistor, R_{b} was placed between the OP AMP output and the transistor base. A circuit diagram of the modified filter is shown in Fig. 3.10 and the component values are listed in Tab. 3.4. Assuming that the transistor does not add voltage noise, the total noise at the input of the VCO is then

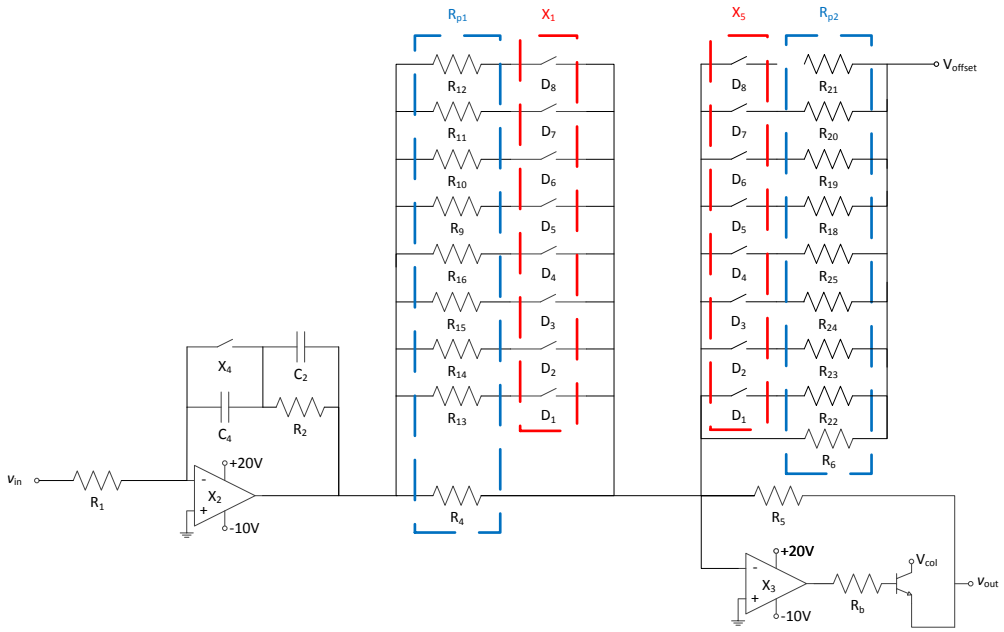


Fig. 3.10: Schematic of loop filter topology with current amplifying transistor.

Tab. 3.4: Component values in the loop filter topology with current amplifying transistor.

$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{C_2}$	$\mathbf{C_4}$	$\mathbf{R_b}$	$\mathbf{R_{p1}}$	$\mathbf{R_{p2}}$	$\mathbf{R_5}$
51.3 Ω	51.3 Ω	22 pF	22 nF	10.5 Ω	Variable	Variable	Constant

found in the same way as in the previous section:

$$\begin{aligned} v^2_{\text{rms, tot}} = v^2_{\text{rms, OP AMP1}} + \left(\frac{1}{R_1} + \frac{1}{R_2}\right)^{-2} i^2_{\text{rms, OP AMP1}} + \dots \\ + v^2_{\text{rms, OP AMP2}} + \left(\frac{1}{R_{\text{p1}}} + \frac{1}{R_{\text{p2}}} + \frac{1}{R_5}\right)^{-2} i^2_{\text{rms, OP AMP2}} + ... \\ + 4k_{\text{B}}TR_1 + 4k_{\text{B}}TR_{\text{p1}} + 4k_{\text{B}}TR_{\text{p2}} + 4k_{\text{B}}TR_5 + 4k_{\text{B}}TR_{\text{b}} \, . \end{aligned} \tag{3.4}$$

The phase noise caused by this voltage noise can be calculated from (2.27).

The power loss in the filter can be approximated by looking at the PLL in locked state, when the current through R_{p1} is close to zero. From (2.16) it can be seen that $V_{\text{offset}}/R_{\text{p2}} \approx V_{\text{out}}/R_5$ for small i_{p1}, which makes the approximated power loss in R_{p2} and R_5:

$$P_{\text{loss, resistors}} = \frac{V^2_{\text{out}}}{R_5} + \frac{V^2_{\text{offset}}}{R_{\text{p2}}} \approx \frac{2V^2_{\text{out}}}{R_5} \, . \tag{3.5}$$

The power consumed in the transistor, in locked state when $v_{\text{out}} \approx V_{\text{out}}$, can be expressed

as

$$P_{\text{loss, transistor}} = (V_{\text{col}} - v_{\text{out}})\frac{v_{\text{out}}}{R_5} \approx (V_{\text{col}} - V_{\text{out}})\frac{V_{\text{out}}}{R_5} = \frac{V_{\text{col}}V_{\text{out}}}{R_5} - \frac{V_{\text{out}}^2}{R_5} \ , \tag{3.6}$$

where V_{col} is the DC voltage at the transistor's collector which needs to be approximately 0.7 V higher than $V_{\text{out,max}}$, because of the voltage drop in the transistor. In this design, the collector voltage was chosen to be $V_{\text{col}} = 20\,\text{V}$ which was convenient since the OP AMPs also uses 20 volt supply voltage.

At locked state, all other currents in the filter are very small and therefore the power loss in other resistors are assumed to be negligible. The total power loss in the filter, excluding the losses in OP AMPs, can then be approximated from sum of (3.6) and (3.5):

$$\begin{aligned} P_{\text{loss, filter}} &= P_{\text{loss, transistor}} + P_{\text{loss, resistors}} \approx \\ &\approx \frac{V_{\text{col}}V_{\text{out}}}{R_5} - \frac{V_{\text{out}}^2}{R_5} + \frac{2V_{\text{out}}^2}{R_5} = \\ &= \frac{V_{\text{col}}V_{\text{out}}}{R_5} + \frac{V_{\text{out}}^2}{R_5} \ . \end{aligned} \tag{3.7}$$

This indicates that the power loss increases with increasing V_{out} and thereby with increasing output frequency.

Loop stability

For the original loop filter topology the different functions $F(s)$, $G_{\text{ol}}(s)$, $G_{\text{lp}}(s)$ and $G_{\text{hp}}(s)$ were plotted versus frequency, the result is shown in Fig. 3.11. In the plot, the functions are plotted for the original loop filter design at $f_0 = 3120\,\text{MHz}$, that is $N = 12$, $R_{\text{p1}} = 6030\,\Omega$, $R_{\text{p2}} = 4420\,\Omega$, $R_5 = 2730\,\Omega$ together with the components listed in Tab. 3.3. A different N would however only make a very small change in the behaviour of the functions and it is therefore not illustrated further.

Since R_1, R_2, C_2, C_4 and the ratio R_5/R_{p1} are equal in both topologies, the filter transfer function (2.18) will also be the same in both topologies. This means, from (2.13), that $G_{\text{ol}}(s)$ and thereby stability will also be approximately equal in both cases. Because the transfer functions have similar behaviour for all f_0, the stability will also be similar for the different output frequencies.

The stability was analyzed using Nyquist stability criterion described in Section 2.2.1, a Nyquist diagram of $G_{\text{ol}}(s)$ is shown in Fig. 3.12. As can be seen in the graph, the Nyquist curve of $G_{\text{ol}}(s)$ does not encircle the critical point -1 which implies that the closed loop system is stable.

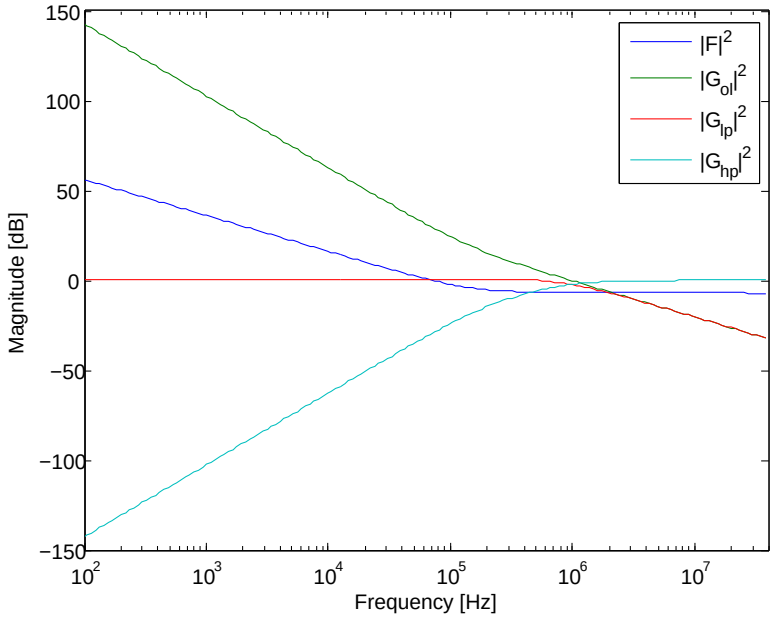


Fig. 3.11: The transfer and gain functions $F(s)$, $G_{\mathrm{ol}}(s)$, $G_{\mathrm{lp}}(s)$ and $G_{\mathrm{hp}}(s)$ of the original filter topology at $f_0 = 3120\,\mathrm{MHz}$.

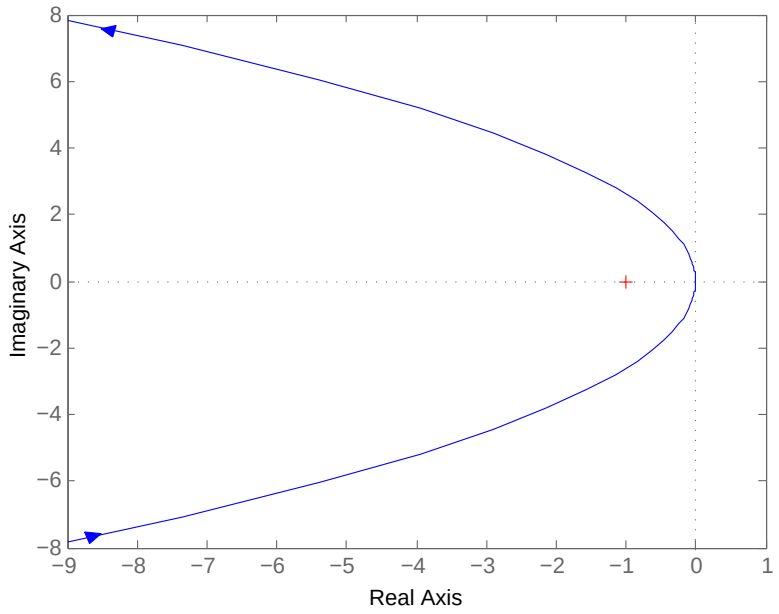


Fig. 3.12: Nyquist plot of $G_{\mathrm{ol}}(s)$.

3.2 Instruments and experimental procedure

All simulations in this project were carried out in MATLAB and the measurements were performed with several different instruments. For general troubleshooting the spectrum analyzer 8596E from Hewlett Packard was used, with a high impedance probe, to be able to look at the spectrum at any exposed pad in the circuit. The power meter E4416A from Agilent was also used throughout the project to keep track of the power level of the signal.

3.2.1 Phase noise measurements

The phase noise of the reference signal and the VCO was measured with the Signal Source Analyzer (SSA) E5052B from Agilent. The same instrument was used to measure the VCO output frequency vs. control voltage in Fig. 3.5.

The PLLs total output phase noise was measured with the older version of the same instrument, E5052A. When this phase noise was measured, the PLL output was split with a 3 dB-divider, where one port was connected to the SSA and the other was connected to the spectrum analyzer. The spectrum analyzer was used to simplify the process of finding a locked state. During these measurements R_{p2} was not tunable but replaced with a fixed resistance and V_{offset} was instead adjusted until the PLL locked in.

3.2.2 Baseband noise measurements

The voltage noise in the loop filter, Fig. 3.9, was measured with the SSA E5052B. During this measurement, the output of the filter was connected to the baseband port of the SSA while the input of the filter was terminated with a 50 Ω load. The DC supply voltages were applied in order to include the full voltage noise from the OP AMPs.

3.2.3 Phase detector characterization

The phase detector constant, Fig. 3.6, was measured using two signal generators SMB100A and one oscilloscope RTO1044, all from Rohde & Schwarz. To simulate the phase detector, which in this design was a mixer, as realistically as possible, the LO- and RF-ports were fed with signals similar to the signals which would appear in the real circuit. A 14 dBm, 260 MHz signal was applied to the LO-port while a −2 dBm signal of different frequency was applied to the RF-port.

Chapter 4

Results & Discussion

In this chapter, the results from the different measurements and simulations will be presented and discussed. In the first half of the chapter, simulations of the filter phase noise model are compared with measurements, verifying the model's accuracy. A suggestion of a final design will be presented in the later half of the chapter which is followed by a general discussion at the end.

4.1 Measurement & simulation of synthesizer with original loop filter design

The original loop filter design, at $f_0 = 3120\,\text{MHz}$, consisted of resistors with values according to Tab. 4.1. In the same table the resistance scale factor k and maximum filter current, calculated from (3.2) and (3.3), are also provided. For circuit diagram and additional component values see Fig. 3.8 and Tab. 3.3 in chapter 3. The phase noise performance of the complete PLL was measured and simulated, the result is shown in 4.1. Two simulations are presented, one with and one without an included filter model. The figure also shows the phase noise of the free running VCO, filter and upconverted reference signal, that is the reference signal multiplied with the division number ($N = 12$) as was explained in (2.10). Note that the peak at $\Delta f = 13.5\,\text{MHz}$ is disregarded since it does not originate from the synthesizer itself, as was mentioned in Section 3.1.

As can be seen in Fig. 4.1, the simulation including the filter model proposed in Section 2.3.1 is much more accurate than the simulation not including the filter model. The most critical point is at offset frequency $\Delta f = 841\,\text{kHz}$, where the measured phase noise is 3.7 dB higher than the maximum allowed phase noise according to the specification presented in Section 3.1. Note that for offset frequencies above $\Delta f = 860\,\text{Hz}$ the filter contributes more noise than the VCO. Since both the VCO and the filter have the same transfer function $G_{\text{hp}}(s)$, (2.15), the filter will dominate the phase noise contribution instead of the VCO for high offset frequencies. This is not desirable since it is generally

Tab. 4.1: Component values of the original loop filter design at $f_0 = 3120\,\text{MHz}$.

k	$\mathbf{R}_{\text{p1}}$	$\mathbf{R}_{\text{p2}}$	$\mathbf{R}_5$	$\mathbf{I}_{\text{max}}$
1	$6030\,\Omega$	$4420\,\Omega$	$2730\,\Omega$	6 mA

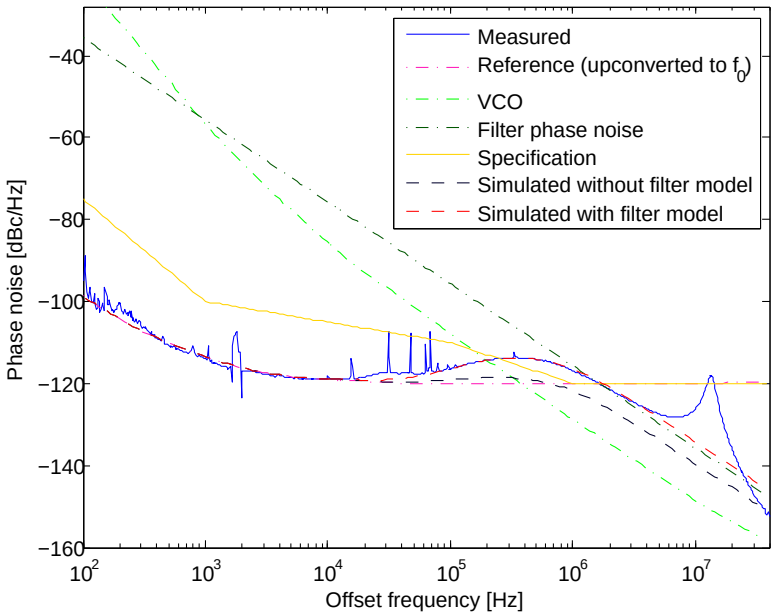


Fig. 4.1: Measured and simulated phase noise of the synthesizer at $f_0 = 3120\,\text{MHz}$ with the original loop filter design.

considered harder to design a low phase noise VCO than a loop filter with low phase noise contribution. To investigate the filter further, an analysis of each filter component's phase noise contribution was performed, the result is shown in Fig. 4.2. As can be seen in the graph, the largest phase noise contributors are the large resistors R_{p1}, R_{p2} and R_5, followed by the current noise from the second OP AMP. The phase noise caused by the current noise in the second OP AMP is related to the size of R_{p1}, R_{p2} and R_5 according to (2.30). Therefore, by reducing these resistances the phase noise contribution from the filter can be substantially reduced.

4.2 Simulation of synthesizer with original filter topology where resistances are reduced by a factor $k = 4.3$

The low noise, wide bandwidth OP AMPs mentioned in Section 3.1.5 are assumed to be able to operate at a short-circuit current of 25 mA. From (3.2) and (3.3) this allows for a reduction of the resistances by a factor $k = 4.3$. Therefore a design with $k = 4.3$ was simulated, the corresponding resistor values are presented in Tab. 4.2 and the

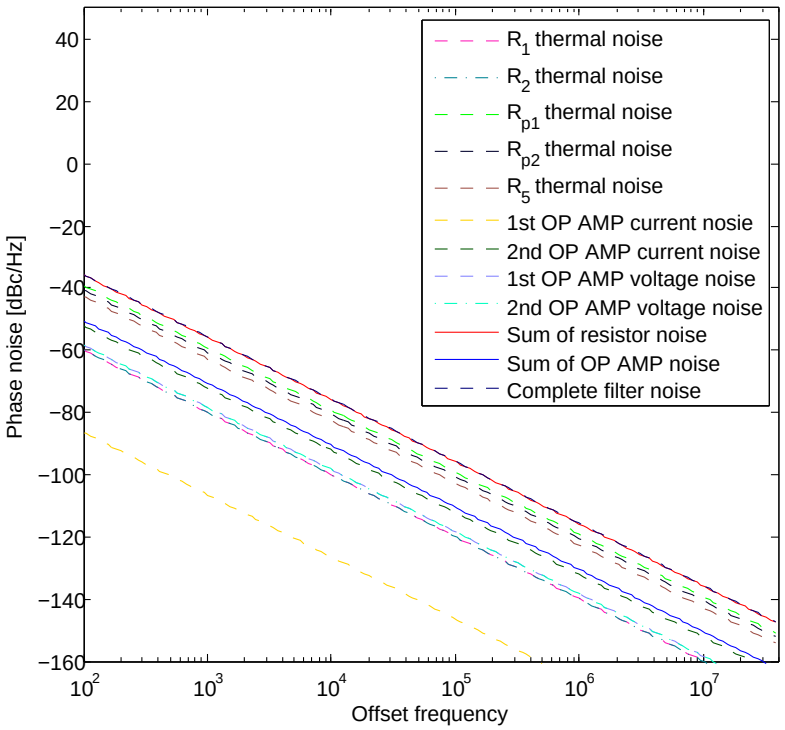


Fig. 4.2: Simulated phase noise contribution from the different components in the original loop filter at $f_0 = 3120\,\text{MHz}$.

Tab. 4.2: Component values of the loop filter with original topology, where $k = 4.3$ and $f_0 = 3120\,\text{MHz}$.

k	$\mathbf{R}_{\text{p1}}$	$\mathbf{R}_{\text{p2}}$	$\mathbf{R}_5$	$\mathbf{I}_{\text{max}}$
4.3	$1414\,\Omega$	$1036\,\Omega$	$640\,\Omega$	$25\,\text{mA}$

simulation result is shown in Fig. 4.3. As can be seen in the graph, the phase noise is greatly improved when the resistances are reduced and is near the specification at this output frequency. However the phase noise contributions will increase with higher output frequencies according to (2.10) and therefore the filter design needs to be improved even further.

4.3 Measurement & simulation of synthesizer with modified loop filter topology where resistances are reduced by a factor $k = 6.8$

To reduce the phase noise from the filter even further, a current amplifying transistor was added as shown in Fig. 3.10. The resistances were this time reduced by a factor

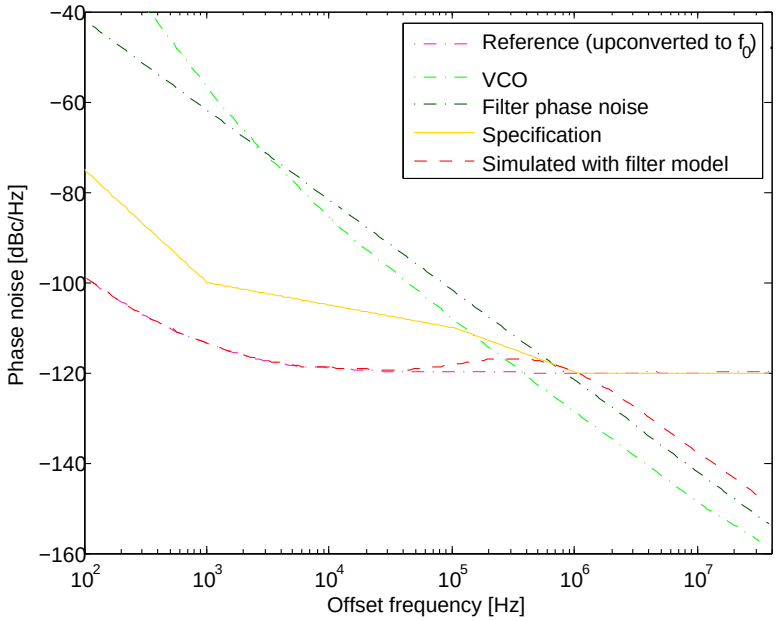


Fig. 4.3: Simulated phase noise of the synthesizer at $f_0 = 3120\,\text{MHz}$, with original filter topology where resistances are reduced by a factor $k = 4.3$.

Tab. 4.3: Component values of the loop filter with modified topology, where $k = 6.8$ and $f_0 = 3120\,\text{MHz}$.

k	$\mathbf{R}_{\text{p1}}$	$\mathbf{R}_{\text{p2}}$	$\mathbf{R}_5$	$\mathbf{I}_{\text{max}}$
6.8	842 Ω	653 Ω	404 Ω	40 mA

$k = 6.8$ compared to the original design, the values that are listed in Tab. 4.3 were chosen. The simulated and measured result is shown in Fig. 4.4, where it can be seen that the phase noise is further improved compared to Fig. 4.3 in Section 4.2. It can also be seen that the simulated model fits the measured phase noise well for this new topology as well, which suggests that the transistor adds very little phase noise, as was assumed. However, the phase noise is still not low enough to meet the specification for higher operation frequencies. At the most critical region, where the phase noise is as high as the specification, around $\Delta f = 1\,\text{MHz}$, the total phase noise level is close to the level of the reference phase noise. This suggests that an improved reference could improve the phase noise even at this high offset frequency. It was mentioned in Section 3.1.1 that the phase noise performance of the QuickSyn reference is not excellent and there is room for improvement by choosing a better reference source for the final design. Therefore a simulation was performed with data from a different reference, the result is shown in Fig. 4.5. As can be seen in the graph, the phase noise can be greatly reduced by improving the reference.

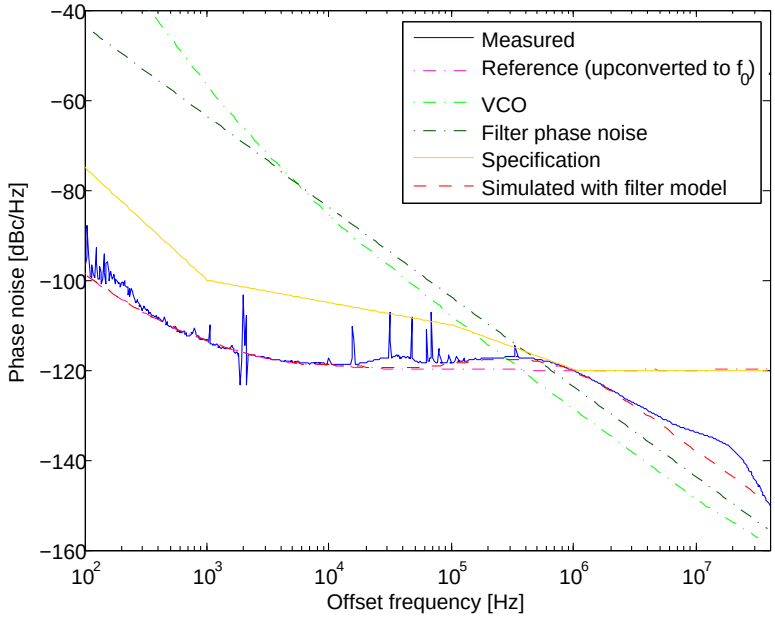


Fig. 4.4: Measured and simulated phase noise of the synthesizer at $f_0 = 3120\,\text{MHz}$, with modified filter topology where resistances are reduced by a factor $k = 6.8$.

4.4 Simulation of synthesizer phase noise for different resistance reduction factor k

To investigate how much the phase noise can be improved using the current amplifying topology, the phase noise was simulated for several different k. The different component values are listed in Tab. 3.4 and 4.4. The simulation result for the original reference source is shown in Fig. 4.6 and for the improved reference source in Fig 4.7. To clarify the impact of increasing the filter current, the phase noise of the synthesizer with improved reference was also plotted within the most critical region, $100\,\text{kHz} < \Delta f < 1\,\text{MHz}$, in Fig. 4.8. As can be seen in the graphs, the phase noise is improved when k is increased. However, the later steps represents a much larger current increase which makes the improvement much less energy efficient at these current levels. For this reason, the value $k = 17.1$ was chosen for further analysis. The higher k were considered unreasonable even if they do improve the phase noise.

4.5 Simulation of synthesizer with modified loop filter topology where resistances are reduced by a factor $k = 17.1$

A simulation was performed of the synthesizer with modified loop filter topology, where $k = 17.1$, and with the improved reference signal from Fig. 3.3. The component values can be found in Tab. 4.4. The total phase noise together with the phase noise contribution from the reference, divider, VCO and filter is shown in Fig. 4.9. The phase

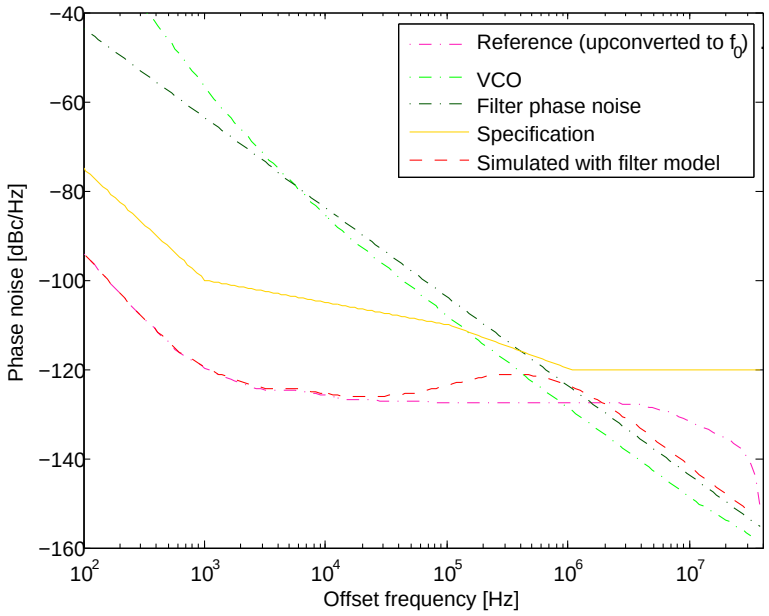


Fig. 4.5: Simulated phase noise of the synthesizer at $f_0 = 3120\,\text{MHz}$ with an improved reference signal and modified filter topology where resistances are reduced by a factor $k = 6.8$.

Tab. 4.4: Component values of the loopfilter with modified topology, for different k at $f_0 = 3120\,\text{MHz}$.

k	$\mathbf{R}_{\text{p1}}$	$\mathbf{R}_{\text{p2}}$	$\mathbf{R}_5$	$\mathbf{I}_{\text{max}}$
1	6030 Ω	4420 Ω	2730 Ω	40 mA
6.8	842 Ω	653 Ω	404 Ω	40 mA
12.0	503 Ω	368 Ω	228 Ω	70 mA
17.1	354 Ω	259 Ω	160 Ω	100 mA
34.1	177 Ω	130 Ω	80 Ω	200 mA
85.3	71 Ω	52 Ω	32 Ω	500 mA

noise contribution from each component in the loop filter is shown in Fig. 4.10. As can be seen in Fig. 4.9, the phase noise for this k is more than 4 dB lower than the specification. In Fig. 4.10 it can be seen that the phase noise contribution from the largest resistances R_{p1}, R_{p2} and R_5 are now comparable with the the OP AMP voltage noise, which explains why the phase noise did not improve at the same rate for higher currents in Section 4.4. To efficiently improve the phase noise further with this method, the noise of the OP AMPs would also need to be reduced.

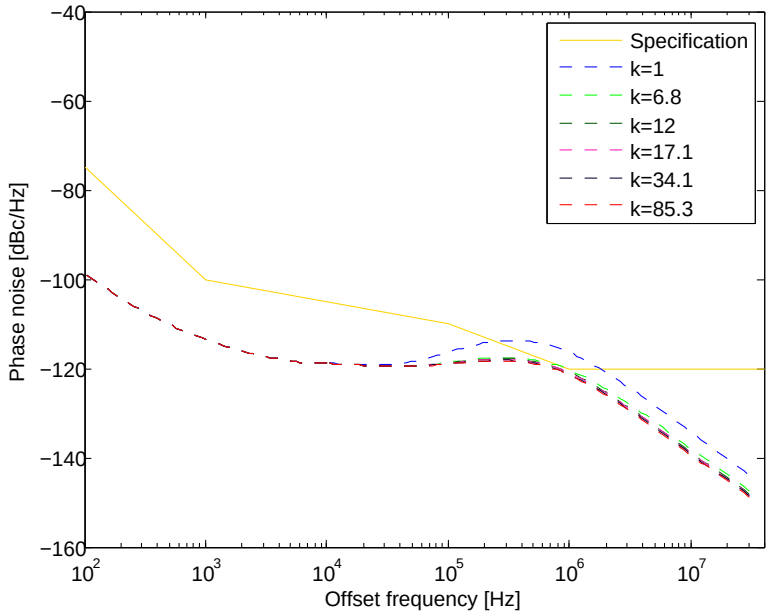


Fig. 4.6: Simulated phase noise of the synthesizer with modified filter topology, for different k at $f_0 = 3120\,\mathrm{MHz}$.

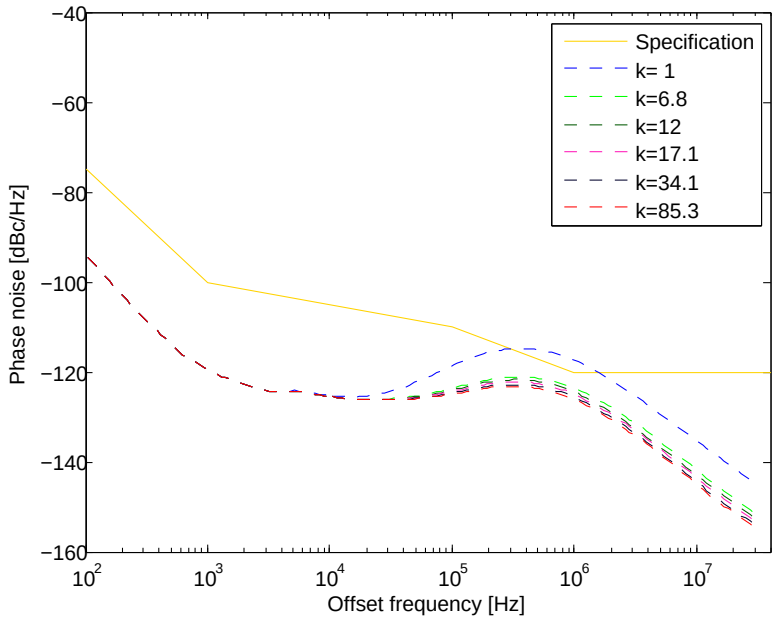


Fig. 4.7: Simulated phase noise of the synthesizer with modified filter topology and improved reference signal, for different k at $f_0 = 3120\,\mathrm{MHz}$.

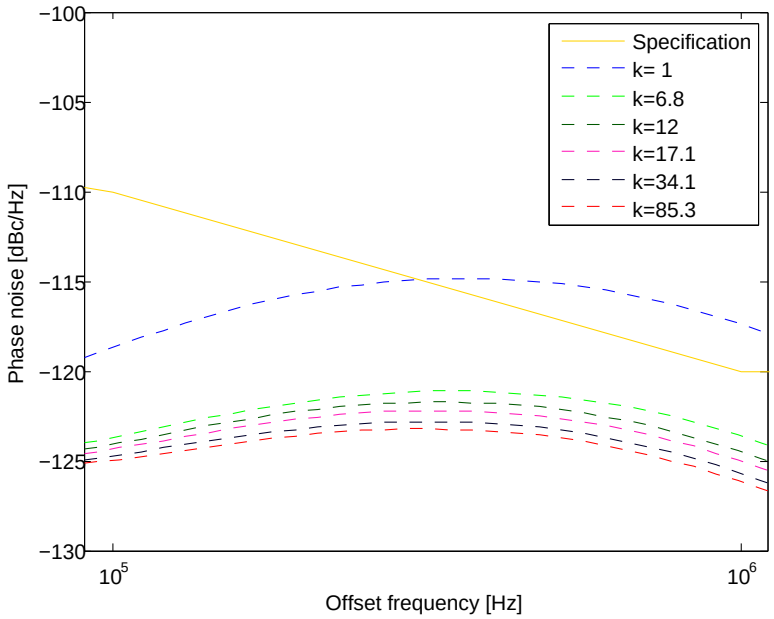


Fig. 4.8: Simulated phase noise of the synthesizer with modified filter topology and improved reference signal, for different k at $f_0 = 3120\,\text{MHz}$ and $100\,\text{kHz} < \Delta f < 1\,\text{MHz}$.

4.6 Simulation of synthesizer with modified loop filter topology and $k = 17.1$ for different output frequencies

To investigate how well the $k = 17.1$ design works over the whole frequency band, $2340\,\text{MHz} < f_0 < 4420\,\text{MHz}$, the output phase noise was simulated for the highest and lowest frequency. The result is shown in Fig. 4.11, where it can be seen that the design meets the specification well for those frequencies. It can also be seen that the phase noise increases with frequency which is expected since the VCO have higher phase noise at high f_0. Larger f_0 means larger N which from (2.14) also increases the phase noise contribution reference, phase detector and divider.

4.7 Discussions and alternative solutions

Looking at the phase noise graphs above, for instance Fig. 4.10, one might be tempted to reduce the cut-off frequency of the loop filter such that the phase noise rolls off at a lower offset frequency. Unfortunately this is not possible because if C_2 is increased $G_{\text{ol}}(s)$ will have a peak within the loop bandwidth which causes instability. C_2 can be increased a little, but not enough to move the breakpoint considerably and these small adjustments only showed degraded phase noise performance in simulations.

The power consumption and efficiency was not the focus of this thesis, but it was considered for instance when choosing to not reduce the resistances further than a factor $k = 17.1$. This k, which is the design where $R_5 = 160\,\Omega$, has a total power

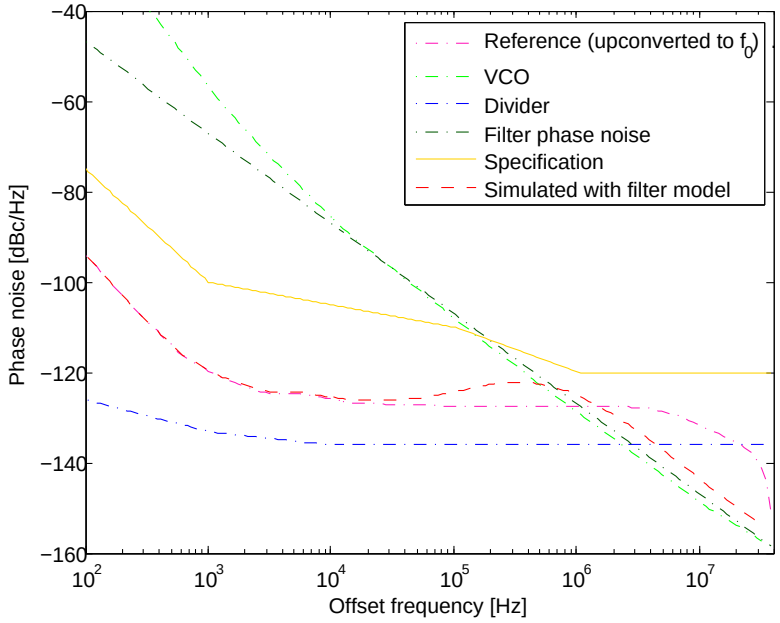


Fig. 4.9: Simulated phase noise of the synthesizer at $f_0 = 3120\,\text{MHz}$, with modified loop filter topology where the resistances are reduced by a factor $k = 17.1$.

loss in the filter of $P_{loss,\,filter} = 3.6\,\text{W}$ according to (3.7) when the collector voltage is $V_{\text{col}} = 20\,\text{V}$ and $V_{\text{out}} = 16\,\text{V}$. This high V_{out} is necessary to achieve the highest output frequency but V_{col} could safely be reduced to 17 V. This would decrease the power loss to $P_{loss,\,filter} = 3.3\,\text{W}$. This is still a large power loss, but as was already stated, power loss was not the focus of this thesis.

During this work, other ways of reducing the resistances were considered. However, to achieve the high output voltage reducing the resistances will require a high current unless the loop filter or the complete PLL is completely re-designed. Therefore, some time was spent on searching for ways of increasing this current. One way of achieving $I_{\text{max}} = 100\,\text{mA}$, other than using a current amplifying transistor, would be to connect four OP AMPs in parallel in the second OP AMP stage. Each OP AMP would add voltage noise and the OP AMPs would need to be stabilized with a small resistance at the output similar to R_{b} in Fig. 3.1.5. This small resistance would also add a little voltage noise. This means that this solution would not be able to achieve as good phase noise performance while it also would be physically larger and more expensive. The benefit of a design like this would be that it could be less power consuming, since a lot of power is lost as heat in the transistor. This design was never tested since the power loss were not considered as high priority as the phase noise performance, size and cost.

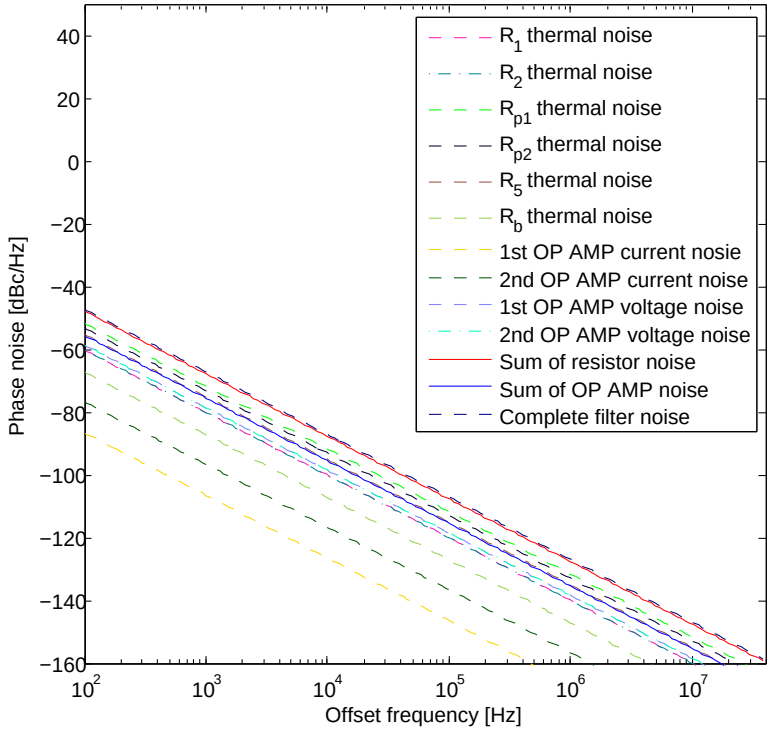


Fig. 4.10: Simulated phase noise contribution from the different components in the modified loop filter with $k = 17.1$ and $f_0 = 3120\,\text{MHz}$.

4.8 Estimation of loop filter phase noise contribution in an early PLL design stage

When designing a PLL there are many different parameters that can be considered which can make it difficult to find a good approach in the beginning of the design process. The theory behind the filter phase noise contribution is relatively extensive and it is not likely that a designer would consider this in an early design stage. It could therefore be useful to have a tool which, with only a few easily measured PLL parameters, can estimate the phase noise contribution from the filter. A suggestion of such an estimation tool will be formulated in this section.

From a phase noise perspective, the general approach in the beginning of a PLL design process is to investigate the VCO, reference source and phase detector. The phase noise curves of these components will provide a rough indication of the performance of the complete PLL. The phase noise of the system will follow the reference or phase detector at low offset frequencies and the VCO at high offset frequencies. The offset frequency where the VCO phase noise intersects the reference or phase detector phase noise also gives a good estimation of the loop bandwidth. With this data, one could also estimate some initial parameters for the loop filter.

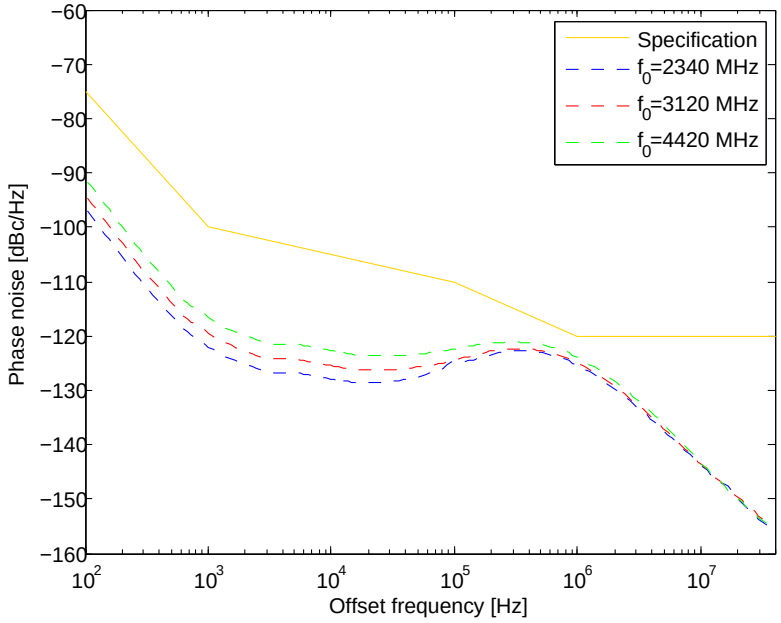


Fig. 4.11: Simulated phase noise of the synthesizer with modified filter topology, improved reference and $k = 17.1$ for three different output frequencies.

Let Δf_{i} represent the offset frequency where the VCO phase noise curve intersects the reference or phase detector phase noise curve. If the phase noise of the reference source is larger than the phase noise of the phase detector this intersection will occur between the VCO and reference source, otherwise it will occur between the VCO and phase detector. Also note that the phase noise of the reference or phase detector needs to be up-converted to the same frequency as the VCO according to (2.10). At Δf_{i}, the VCO phase noise is $\mathscr{L}_{\mathrm{vco}}(\Delta f_{\mathrm{i}})$. It is desirable that the filter's phase noise contribution is less than the VCO's phase noise. A reasonable specification is to require the maximum allowed phase noise of the filter to be less than half the phase noise of the VCO, that is $\mathscr{L}_{\mathrm{filter,\,max}}(\Delta f_{\mathrm{i}}) = \mathscr{L}_{\mathrm{vco}}(\Delta f_{\mathrm{i}})/2$. Inserting this into (2.26) and rewriting provides

$$v_{\mathrm{rms,\,max}} = \frac{K_{\mathrm{vco}}}{\Delta f_{\mathrm{i}}}\sqrt{2\mathscr{L}_{\mathrm{filter,\,max}}(\Delta f_{\mathrm{i}})} = \frac{K_{\mathrm{vco}}}{\Delta f_{\mathrm{i}}}\sqrt{\mathscr{L}_{\mathrm{vco}}(\Delta f_{\mathrm{i}})}\,. \tag{4.1}$$

This means, that if this intersection point and the VCO sensitivity K_{vco} are known, a maximum allowed voltage noise in the filter can easily be estimated. This is a valuable knowledge to have in the process of choosing OP AMPs and resistors for the filter. To develop this further, another rough estimation can be made. If the filter consists of M components such as resistors and OP AMPs, then according to (2.29) the maximum allowed average voltage noise of these components can be found as

$$v_{\mathrm{rms,\,avg}} = \frac{v_{\mathrm{rms,\,max}}}{\sqrt{M}}\,. \tag{4.2}$$

The maximum average resistance which generates a thermal voltage noise of this magnitude is then easily calculated by (2.28):

$$R_{\mathrm{max,avg}} = \frac{v_{\mathrm{rms,\ avg}}^2}{4k_{\mathrm{B}}T} \ . \tag{4.3}$$

With equations (4.1)-(4.3), the voltage noise of the OP AMPs and the size of the resistances in the loop filter can be estimated from a few parameters which are generally known early in the PLL design process. This gives a rough estimation to help in an early design stage and this approach should be valid in filter topologies which are relatively similar to the ones studied in this thesis, e.g. Fig. 2.5.

Chapter 5

Conclusions and future work

Phase noise analysis was performed on an already designed and fabricated synthesizer on which measurements had shown a larger phase noise than predicted. To allow for an accurate phase noise analysis, the circuit was re-fabricated with a simpler loop filter. The pulse-controlled 8-channel switches were removed and the filter was designed for a single state only.

A model for the PLL output phase noise was developed which included the effect of voltage noise generated in the loop filter. This model was then verified through measurements, which indicated that the unpredicted increase of phase noise originated mostly from thermal noise in the loop filter's relatively large resistances. These resistances could not be directly reduced since the VCO requires a high input voltage while the OP AMPs limit the current, which together limits how small the resistances can be. Therefore, the loop filter was modified by adding a current amplifying transistor at the output of the filter. This allowed for the necessary high output voltage while reducing the resistances. The modified loop filter was fabricated and measured which proved that the phase noise increase did, as predicted, originate mostly from thermal noise.

When the model was verified, a new loop filter was designed to meet the specification. For the highest operation frequency, $f_0 = 4420\,\text{GHz}$, and at the most critical offset frequency, $\Delta f = 1\,\text{MHz}$, the new design's simulated phase noise was $\mathscr{L} = -123.6\,\text{dBc/Hz}$ which is a 7.5 dB improvement compared to the original design and low enough to meet the specification with over 3.6 dB margin.

The new design utilizes a high current to achieve the required high output voltage while still keeping the noisy resistors small. A large amount of power is lost as heat in the transistor and resistors, which could be a topic for future work. For a wide bandwidth PLL, the VCO needs to be very sensitive or require a wide range of input voltage. If the VCO is very sensitive the resistances in the filter need to be small, otherwise their thermal noise will generate a large phase noise. This requires high currents which causes power loss in the filter. If a wide range of VCO input voltage is required it normally means that the higher frequencies need a high input voltage. This high input voltage would then cause power loss in the filter. Either way, this filter design is relatively power consuming. One suggestion for future research is to investigate ways of summing a small signal voltage with a variable DC voltage other than a summing OP AMP and a variable voltage divider, as was used in this design. Another suggestion is to investigate a design using a different phase detector, for example one using logic gates to create a pulse width modulated signal. This kind of phase detector could possibly achieve the high voltage without utilizing a summing OP AMP, which would make it possible to design a less noisy loop filter.

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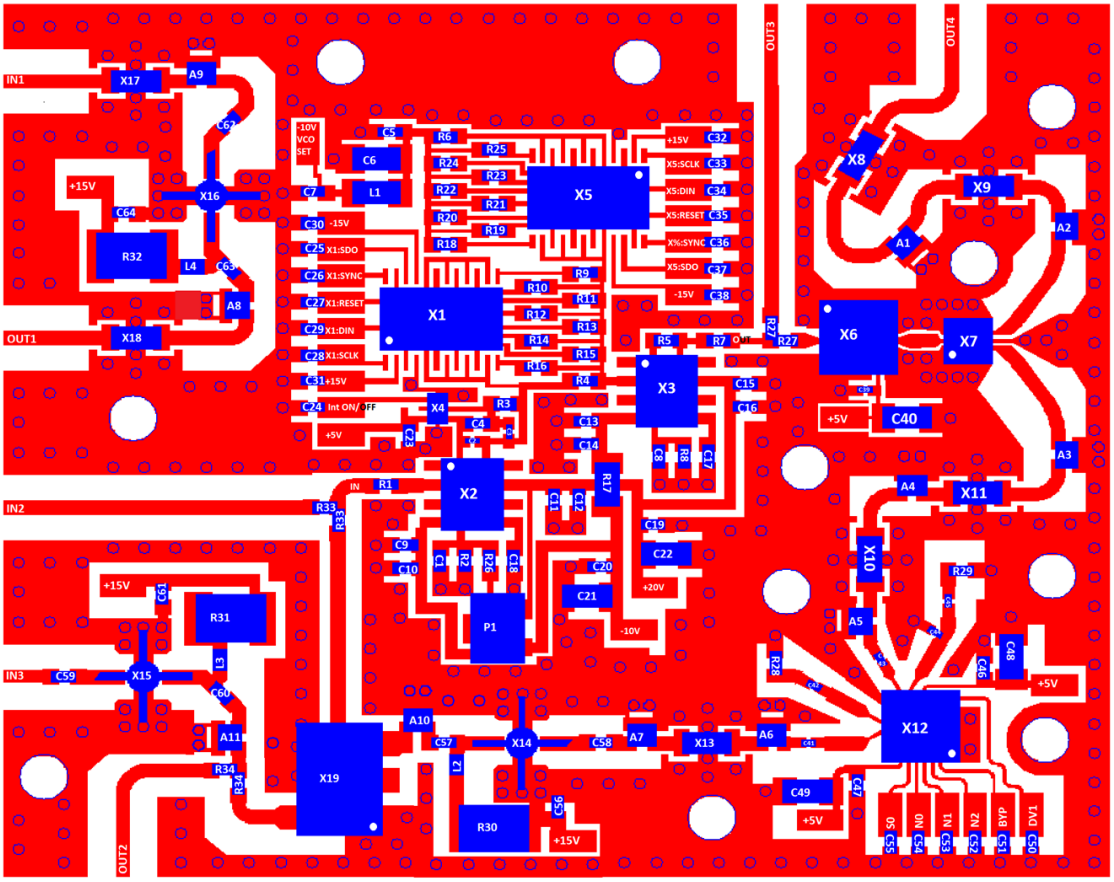
Appendix A

Synthesizer layout



Appendix B

Bill of materials

Label	Component
X_1	8-channel switch ADG1414BURZ
X_2	OP AMP OPA161
X_3	OP AMP OPA161
X_4	Single channel switch ADG741BKS
X_5	8-channel switch ADG1414BURZ
X_6	VCO HMC3589LC4B
X_7	Power divider GP2Y1+
X_8	Low-pass filter LFCN-4400
X_9	High-pass filter HFCN-2000
X_{10}	Low-pass filter LFCN-4400
X_{11}	High-pass filter HFCN-2000
X_{12}	Frequency divider HMC705LP4
X_{13}	Low-pass filter LCFN-320
X_{14}	LNA ERA-5XSM+
X_{15}	LNA ERA-5XSM+
X_{16}	Not used
X_{17}	Not used
X_{18}	Not used

Label	Component
X_{19}	Mixer ADE-1+
R_1	Resistor 51 Ω
R_2	Not used
R_3	Resistor, 51 Ω
R_4	Part of R_{p1}*
R_5	Resistor 2.7 kΩ
R_6	Part of R_{p2}*
R_7	Resistor 0 Ω
R_8	Resistor 1.33 kΩ
R_9	Part of R_{p1}*
R_{10}	Part of R_{p1}*
R_{11}	Part of R_{p1}*
R_{12}	Part of R_{p1}*
R_{13}	Part of R_{p1}*
R_{14}	Part of R_{p1}*
R_{15}	Part of R_{p1}*
R_{16}	Part of R_{p1}*
R_{17}	Resistor 0 Ω

*Included in R_{p1} or R_{p2} which were varied throughout this work.

Label	Component
R_{18}	Part of R_{p2}*
R_{19}	Part of R_{p2}*
R_{20}	Part of R_{p2}*
R_{21}	Part of R_{p2}*
R_{22}	Part of R_{p2}*
R_{23}	Part of R_{p2} *
R_{24}	Part of R_{p2}*
R_{25}	Part of R_{p2}*
R_{26}	Not used
R_{27}	Resistor 0 Ω
R_{28}	Resistor 51 Ω
R_{29}	Resistor 51 Ω
R_{30}	Resistor 36 Ω
R_{31}	Resistor 36 Ω
R_{32}	Not used
R_{33}	Resistor 0 Ω
R_{34}	Resistor 0 Ω
L_1	Inductor 220 nH
L_2	Inductor 330 nH
L_3	Inductor 330 nH
L_4	Not used
C_1	Capacitor 1 µF
C_2	Capacitor 22 pF
C_3	Capacitor 22 pF
C_4	Capacitor 22 nF
C_5	Capacitor 100 nF
C_6	Capacitor 100 µF
C_7	Capacitor 1 µF

Label	Component
C_8	Capacitor 1 µF
C_9	Capacitor 100 nF
C_{10}	Capacitor 1 µF
C_{11}	Capacitor 100 nF
C_{12}	Capacitor 1 µF
C_{13}	Capacitor 100 nF
C_{14}	Capacitor 1 µF
C_{15}	Capacitor 100 nF
C_{16}	Capacitor 1 µF
C_{17}	Not used
C_{18}	Not used
C_{19}	Capacitor 100 nF
C_{20}	Capacitor 100 nF
C_{21}	Capacitor 10 µF
C_{22}	Capacitor 10 µF
C_{23}	Capacitor 100 nF
C_{24}	Capacitor 100 nF
C_{25}	Capacitor 100 nF
C_{26}	Capacitor 100 nF
C_{27}	Capacitor 100 nF
C_{28}	Capacitor 100 nF
C_{29}	Capacitor 100 nF
C_{30}	Capacitor 100 nF
C_{31}	Capacitor 100 nF
C_{32}	Capacitor 100 nF
C_{33}	Capacitor 100 nF
C_{34}	Capacitor 100 nF
C_{35}	Capacitor 100 nF

*Included in R_{p1} or R_{p2} which were varied throughout this work.

Label	Component
C_{36}	Capacitor 100 nF
C_{37}	Capacitor 100 nF
C_{38}	Capacitor 100 nF
C_{39}	Capacitor 1 nF
C_{40}	Capacitor 4.7 µF
C_{41}	Capacitor 1 nF
C_{42}	Capacitor 1 nF
C_{43}	Capacitor 100 pF
C_{44}	Capacitor 100 pF
C_{45}	Capacitor 100 pF
C_{46}	Capacitor 1 nF
C_{47}	Capacitor 1 nF
C_{48}	Capacitor 4.7 µF
C_{49}	Capacitor 4.7 µF
C_{50}	Capacitor 100 nF
C_{51}	Capacitor 100 nF
C_{52}	Capacitor 100 nF
C_{53}	Capacitor 100 nF
C_{54}	Capacitor 100 nF
C_{55}	Capacitor 100 nF

Label	Component
C_{56}	Capacitor 100 nF
C_{57}	Capacitor 100 pF
C_{58}	Capacitor 100 pF
C_{59}	Capacitor 100 pF
C_{60}	Capacitor 100 pF
C_{61}	Capacitor 100 nF
C_{62}	Not used
C_{63}	Not used
C_{64}	Not used
A_1	Attenator 4 dB
A_2	Attenator 4 dB
A_3	Attenator 3 dB
A_4	Attenator 3 dB
A_5	Attenator 2 dB
A_6	Attenator 2 dB
A_7	Attenator 2 dB
A_8	Not used
A_9	Not used
A_{10}	Attenator 10 dB
A_{11}	Attenator 3 dB