CHALMERS

Design of 28 nm FD-SOI CMOS laser drive circuit for energy efficient Datacom applications.

Master's Thesis in Embedded Electronic System Design

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Abstract

The field of power efficient optical communications has seen a large growth in the recent years due to the growing number of data-centers around the globe and the increasing demands for data rate. While the performance of those data links keeps increasing, it drives the power consumption high as well. Research in the field of energy efficient opto-electronic links is picking up speed in order to keep up with the current trends in data-rate demand without exceeding the power budget. At higher speeds, the electronics start to have more crucial role in the power consumption, therefore, the work of optimizing a optical link starts from the transmitter and receiver electronics. This study attempts to explore the design of an existing 65 nm CMOS transmitter circuit and transfer it to the 28 nm FDSOI CMOS process in order to benefit from the intrinsic power efficiency and speed provided by technology scaling. A laser driver circuit is designed using PAM-4 modulation, optimized to drive a VCSEL laser at 25GHz frequency. Additional techniques are implemented to provide control over the output behavior of the chip in real time, allowing for a great range of experimental scenarios to be performed with a single chip and to potentially permit the testing of different VCSEL diodes. The benchmarked values of the original 65 nm design are met and surpassed by the 28 nm simulated values, even though the latter is constructed with several degrees of parametrization available, in order to serve as a testing chip. The simulated results also surpassed in terms of energy efficiency, most the top-tech driver circuits in the literature.

Keywords: VCSEL, CMOS, FD-SOI, 28nm, Laser Driver, Datacom, Energy efficient.

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Stavros Giannakopoulos, Gothenburg, Sweden 31/8/2015

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Introduction

In modern data centers, one major contributor to the expenses is the energy spent on powering the interconnected networks that typically cover an area of a few hundred meters [3]. In the past, copper wires have been the main means of interconnecting. However, as the demand on communication speed rose, the power and cooling demand of the interconnect framework became a major concern. As a result, optical fiber networks are gradually taking over the field, providing improved performance at lower energy demands.

Therefore, a new generation of laser driver circuits based on modern technology nodes is required in order to keep up with the increasing demand in speed while maintaining high power efficiency. The migration on smaller feature size offers reduced power consumption, faster performance and smaller area on the CMOS level which in turn can be utilised to design simpler driver circuits with the same or even better performance.

1.1 Place in the field

As the data-rate scales, so does the power consumption of the network, mainly that of the driver electronics as seen in [4–8]. While VCSELs have been shown to achieve high speeds with low power consumption [9], the transmitter and receiver electronics are still the major contributors to the power consumption.

Furthermore, the current and previous driver designs focus either on BiCMOS technology [10] or CMOS above 65 nm technology nodes [11]. However the 65 nm requires complex methods to keep up with the current demands of performance e.g. inductive peaking [11], feed forward equalization (FFE) [12]. Thus, arises a need for transition into newer technologies in which the smaller feature size can offer intrinsically faster performance, lower energy consumption and smaller area, without increasing the complexity of the design.

The ST Microelectronics' 28 nm *Fully Depleted Silicon on Insulator* [13] (FDSOI) technology node fulfills all of the above criteria including high bandwidth and low power

[14]. Since it is a CMOS compatible process, it provides an advantage in terms of energy efficiency, over BiCMOS, which is more energy consuming.

While technology scaling in terms of gate sizes still follows Moore's law, the energy figures of the smaller nodes do not scale that fast, effectively hitting a "power wall" [15]. Whether the new 28 nm driver design can outperform the 65 nm one in terms of energy efficiency, or not, and to what extent remains to be verified.

1.2 Goal of the project

The goal of this project is to transfer an existing low power 65 nm CMOS driver design [11], into 28 nm, without sacrificing performance or energy efficiency. Laser driver circuits have shown a substantial improvement on their energy efficiency, area and bit-rate on each technology transition but with increased complexity [11,16,16]. Therefore, the main challenge is to maintain or ideally to improve those aspects, but with a simpler design.

Since the 28 nm technology has not yet been utilised to a great extent by the department, expertise must be developed during the project and should also be passed over in the form of documentation.

The final result should be the well documented process of designing a high-end laser driver circuit in the specific feature size, along with a chip design as close to fabrication as possible. The driver design needs to be migrated into the new technology node, while the speed and power efficiency of the final chip should be on par with the demonstrated values on [11] or better. Namely, the circuit should achieve a throughput of at least 50 Gbps while providing a bias current of 1 mA and a maximum modulation current of up to 20 mA. Lastly, the energy efficiency of the driver should be 0.54 pJ/bit or less at that frequency.

1.3 Scope of this work

The system design process should include all the steps of an electronic system design, starting from the system specification, reading up on the technology node specifics, learning and utilizing the development tools in order to design the circuit, performing simulations to verify its functionality against the 65 nm circuit, and performing all the required steps to prepare it for fabrication on a test chip.

The tools for the design are available but have not been used to a great extent, so learning how to use them is important.

The circuit will be benchmarked with simulations and a straightforward on-off keying mode. During the process of the project it will be decided if there is a need for 4-PAM (pulse amplitude modulation) in order to achieve the characteristics demonstrated in [11] in terms of data-rate.

Additionally, if time permits, the effects of the chip parasitics on the signal integrity and power efficiency need to be explored before the chip is sent for fabrication, as shown in previous works [17]. And then the final design should be prepared for fabrication by performing all the necessary steps.

1.4 Document structure

Since this is an interdisciplinary project, the required background on electronics, optoelectronics, and telecommunications, will be set in in Chapter 2. Chapter 3 discusses the methodology that will be used in the design of the driver circuit, as well as the individual steps required for the design to be completed. The design decisions made along with their motivation are discussed in Chapter 4. The preliminary results of the driver in the 65 nm process, which are to be used as benchmarks for the final design, are presented in Chapter 5. Then in Chapter 6 we discuss the implementation of the 28 nm circuit and compare its performance to the benchmarked values. In Chapter 7 we present and assess the final results and reflect on the design process. The report is summed up in Chapter 8.

2

Background

The following chapter includes the background as well as the motivation behind the research on energy efficient laser drivers.

2.1 Optoelectronic links

The global demand for data-rate puts increasing demands on computation and information routing on data centers. Since power dissipated in the electronics is a major contributor to the energy consumption of these data centers, the overall energy efficiency of the communication system needs to be investigated. Furthermore power is directly related to cost, therefore, energy efficiency can be used to assess the cost of the data-rate. The energy efficiency of a system is defined as the energy spent per bit of information transmitted or received. Energy efficiency is measured in pJ per bit (pJ/b) or mW/Gb/s and it is typically annotated with the symbol η [18].

In communication links within a data center, optical interconnects are overtaking their copper counterparts since they are practically loss-less for the short distances in a LAN and they offer better performance vs energy trade-off. According to the ITRS the optical interconnect technology has to reach 1 pJ/b energy efficiencies, for the complete link, by 2020 [19]. With the current technologies achieving efficiencies of about $50 - 15$ pJ/b it is evident that there is a long way to go to meet the predictions of the ITRS.

The energy efficiency of an optical link is a rather complex issue to tackle since it reflects an equally complex system, which can fortunately be broken down in separate sub-problems or subsystems. If we follow the flow of information within an optoelectronic link it is easy to see that complexity. The data initially stored in an digital format are first encoded, then transferred to the light emitter through on-chip interconnects where they are transformed into optical pulses, then travel through optical fiber until they reach the optical receiver only to be transformed again into electrical pulses to be decoded and stored or further forwarded.

The first distinction that can be made, is between the different media where the

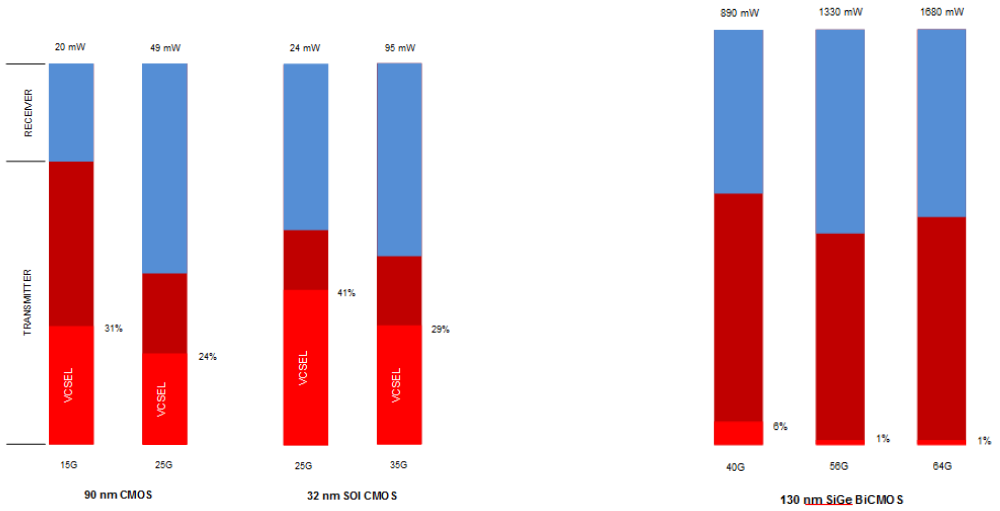
information is traveling through. We have three subsystems (the transmitter, the optical medium and the receiver) that need to be optimized individually as well as collectively to achieve the best energy efficiency.

Furthermore, on both the transmitter and the receiver, there is an optoelectronic conversion; from the encoder, to the driver electronics and then to the light emitter or from the photo-receiver to the electronics and finally to the decoder. The respective efficiencies of those conversions need to be taken into account and optimized for the best trade-off between data-rate and energy consumption.

Even though substantial research is needed on all three fields, i.e. the transmitter circuit, the optical medium and the receiver circuit, this project is focused on the transmitter only.

2.2 Energy efficiency

The energy consumption and efficiency, of the optical link are mostly dependent on the respective electronics as the data-rate increases beyond the 30 Gbps limit (see Fig. 2.1b).



(a) Energy dissipation for Low data-rates.

(b) Energy dissipation for High data-rates.

Figure 2.1: Illustration of energy dissipation for various data-rates based on literature values [20].

In the frequency band of interest ($10 - 30$ Gbps region), the optimizations carried out target the light emitter. Some of the techniques employed target the type of laser, or the fabrication of lasers with higher power efficiency. However, since the laser is given in this study, another way to improve the energy efficiency is required. Using encoding schemes in the driver electronics can allow higher bit rates for the same frequency by transmitting multiple bits of information with each symbol transmitted. The modulation schemes can also improve the BER (bit error rate) of the system, effectively providing a

larger noise margin in the higher frequency of the transmission.

Concerning the light emitter, important parameters that affect link performance in addition to its power efficiency are: the slope efficiency $\Delta P/\Delta I$, the threshold current I_{th}, its external differential quantum efficiency η_d and its power efficiency η_p. Additionally, for high speed modulation, bandwidth, modulation response and turn-on delay, are important [21].

2.3 Driver circuits

As Fig. 2.1a shows, in the data-rate of interest for this design, the driver electronics contribute significantly to the power consumption of the system. That fact is enough to motivate research in optimizing the driver electronics and the encoding schemes used in laser driver circuits. The biggest challenge in such a task, is the fact that the design of the electronics, the key encoding method, the transmission channel, and the light emitter affect each other. For example, altering the encoding scheme in order to transmit more bits per symbol will actually increase the energy efficiency. However, the increased complexity of the electronics on both the transmitter and the receiver might also increase the energy consumption, effectively reducing the energy efficiency. Additionally, the effects of the channel on the transmitted data must be investigated and tested separately.

Therefore, an efficient optoelectronic link needs to be co-designed or at least the functionality of all the distinctive subsystems needs to be co-verified. That process is not trivial, especially since half of the system lies in the optical domain and the other half in the electronic. Thus, in order to be able to draw meaningful conclusions, an electrical modeling or other simulated model of each subsystem must be made.

2.4 Modulation and encoding schemes

Typical modulation schemes used in laser driver circuits are: Pulse Amplitude Modulation (PAM) [22], non-return-to-zero (NRZ) [5] and simple On-off-keying (OOK).

A typical method used for error correction is Forward Error Correction (FEC) [23], however for this study error correction schemes are not considered.

The modulation scheme selected for this project is Pulse Amplitude Modulation (hereby referred as PAM) [24, pp. 345–350].

PAM has been demonstrated to perform exceptionally well in short haul optical links (up to 100 m long) by achieving very high data-rates while being a relatively simple way of encoding [11, 22, 25]. The most important benefit of PAM is that it can transmit multiple bits per symbol. Since the VCSEL assumed for this study, has a bandwidth of ≈ 25 GHz, it is mandatory to transmit at least 2 bits per symbol to achieve the $50 - 56$ Gbps set by the requirements. While NRZ and OOK are relatively more simple to implement, PAM-4 is the only modulation method that can achieve post 50 Gbps rates with the given setup. More motivation about this choice is presented in Section 4.3.

The encoding of the binary data was chosen to be Binary Reflected Gray Coding (BRGC or simply Gray encoding) in order to decrease the Bit Error Rate (BER). The BRGC has been proven to be optimal for use in M-PAM modulations [26] and has been

used in directly modulated laser drivers [11]. Additionally, the outputs of the encoder were thermometer-coded, which meant that no two drivers will switch on and off at the same time. This coding had the benefit of allowing us to use 3 drivers (or driver slices) of equal modulation current, which turn on and off in unison, eliminating glitches and transient effects that could arise if two current drivers were to attempt to switch the output on and off simultaneously.

2.5 The VCSEL

In this report, the light emitter assumed is a Vertical Cavity Surface Emitting Laser (referred as VCSEL from now on) which is one of the most intensively researched lasers for use in optical communications.

2.5.1 Basics

A VCSEL is essentially a p-i-n heterostructure laser, and is enclosed within two distributed Bragg reflectors (DBR) that serve as the mirrors of the laser. Selective oxidation of the outer part of the top layer (typically the p-doped) allows for the light to be confined in a small aperture and escape through that aperture from the surface of the device (see Fig. 2.2). Thus the laser takes the name vertical cavity surface emitting laser.

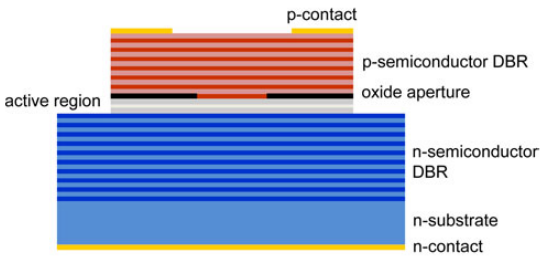


Figure 2.2: Cross-section of a typical VCSEL structure [27].

More details about the VCSEL assumed in this work are presented in Section 4.1 and are derived from [1]. The equivalent electrical model used in the simulations is provided in Appendix C.

2.5.2 Modulation

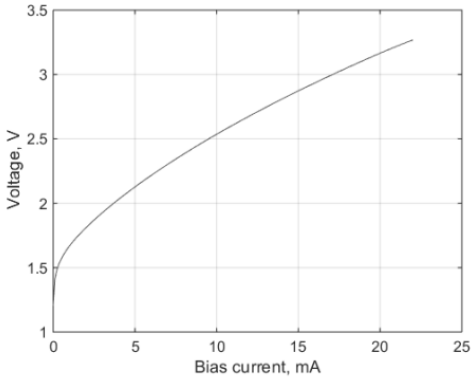
Modulating a laser is typically done by either direct or external modulation. In direct modulation, the signal is encoded via the bias current of the laser, effectively modulating the optical power emitted. In external modulation, the signal is applied over the light pulse while the laser is emitting a constant optical power. The first method is simpler, while the latter is more expensive in terms of the modulating device. For VCSEL devices the direct modulation is more typical since a diode laser is one the few types of lasers that have the required bandwidth for direct high speed modulation [28].

2.5.3 VCSEL parameters

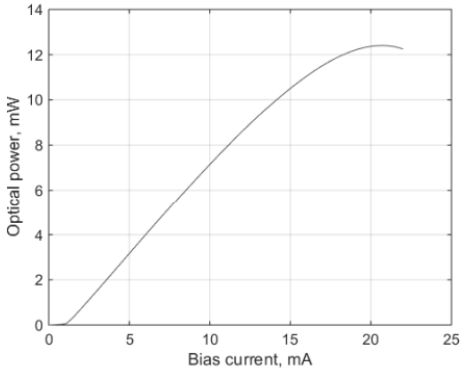
The two critical characteristics in modulating a VCSEL diode are the V-I and the P-I curves.

The first gives a measure of how the differential resistance of the diode changes with the bias current.It is important in this study because a higher current imposes a higher voltage drop across the diode effectively changing the bias point of the driver. A characteristic of the V-I behavior of the VCSEL are shown in Fig. 2.3a.

The second provides information about the efficiency of the VCSEL in converting the current into optical power. This is very important since constant modulation steps are in the requirements of PAM. Therefore, in high currents it requires more current in order to extract the same amount of optical power out of the VCSEL. The P-I curve also gives us the slope efficiency of the laser which is measured by the slope of the characteristic. The P-I curve of the VCSEL to be used in the design is shown in Fig. 2.3b.



(a) V-I characteristic of the VCSEL.



(b) P-I characteristic of the VCSEL.

Figure 2.3: Measured values for the P-I and V-I characteristics of the VCSEL diode [1].

2.6 Technology node

Driver circuits have been demonstrated using 130 nm, 90 nm or 65 nm CMOS technologies. There are also successful implementations of more advanced CMOS technology that further improve power efficiency.

Even though laser driver circuits using IBM's 130 nm Bi-CMOS [29] or STM's 65 nm CMOS [11] and 32 nm CMOS [8] processes have been demonstrated, there has been no attempt to design a laser driver in the FDSOI 28 nm CMOS node to the authors best knowledge. The scaling of gate sizes should provide inherently higher performance and lower energy consumption from the electronic driver circuits. Although reducing the channel length by half (65 nm down to 28 nm) does not necessarily guarantee a doubling in the bandwidth or halving of the power dissipation, it certainly opens the possibility to improve the above parameters without extreme optimizations on the design. The

suitability of the 32 nm node, which is very similar to the 28 nm one, in low power high performance applications has been discussed in [30].

The SOI (Silicon on Insulator) technology in comparison with the bulk Si-CMOS technologies provides a smaller junction capacitance, and allows floating body bias [31]. From a design point of view, the lower junction capacitance in combination with a floating or positively charged body means that the transistors are faster and the current required to charge and discharge the gate of a transistor is less, gaining up to $25 - 35\%$ in performance [32], [33, p. 318–322]. The floating body, on the other hand, poses a severe challenge to the designer, since the charge of the body is not fixed, which allows the threshold voltage of the transistor to change depending on the bias point of the device [32].

This issue can be addressed by using the Fully Depleted SOI or FDSOI technology which minimises the effects of the body bias to the threshold voltage of the transistor [34]. FDSOI gates provide increased current at low V_{ds} voltages, and higher performance due to the decreased threshold voltage. However, a downside of the FD devices is that there is a big fluctuation on the threshold voltage due to the fact that it only depends on the very thin gate oxide used in this process, effectively relying only on fabrication parameters [35]. That thin oxide also makes FDSOI devices harder to manufacture and more prone to reliability issues. Nevertheless, FDSOI have been deemed suitable for both transconductance MOSFET amplifiers and RF applications in mixed-signal systems such as the one to be designed in this project [36].

Lastly, the completely isolated body of the FDSOI process, provides great control of the threshold voltage of the transistors, increasing the speed and decreasing the static leakage [37, 38]. The large voltage margin of the body bias (from -3 to 3 Volts) makes that process an excellent candidate for high performance power efficient systems.

The structural differences between bulk and FDSOI CMOS technologies are shown in Fig. 2.4.

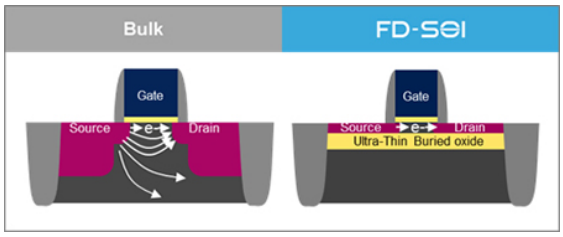


Figure 2.4: Structural differences between bulk and FDSOI 28 nm technologies [39].

2.7 MOSFET basics

The system under design can be described as a digital to analog conversion system or a mixed signal system since it essentially takes 2 digital bit-streams as inputs and outputs an analog value of current to the load (VCSEL).

Therefore, in order to obtain a basic understanding of the system we need to describe the fundamentals of the MOSFET devices.

Typically a MOSFET (in our case an enhancement MOSFET) can operate in three distinct regions of operation: cut-off when the channel is shut off, in the linear of triode region where the channel is established between the source and the drain, and finally the saturation region when the channel starts to pinch off. Since the regions of a N-channel and a P-channel are mirrored we will briefly discuss only the former.

The large signal, long channel current of an N-MOSFET can be roughly described by Eq. 2.1 derived in [40].

$$I_d = \begin{cases} 0 & \text{if } V_{GS} < V_T \\ \mu C_{ox} \frac{W}{L}((V_{GS} - V_T)V_{DS} - \frac{V_{DS}}{2}^2) & \text{if } V_{GS} - V_T > V_{ds} \\ \frac{\mu}{2} C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 & \text{if } V_{GS} - V_T < V_{ds} \end{cases} \tag{2.1}$$

However, in the modern processes the devices are far from the ideal long channel model, mainly due to velocity saturation and channel length modulation effects [33, p. 74–78]. Channel length modulation is especially important to the design of a current source driver because it causes the current during saturation to depend on V_{DS}. This directly contradicts the definition of an ideal current source which requires the current to be completely independent from the voltage in the output. Also this gives rise to more issues if we take into account that multiple drivers are connected to the same output voltage, and therefore will be constantly affecting each others bias voltages.

In current technology nodes the saturation current of the MOSFET is never following the square law mainly due to channel length modulation and body bias effects. Nevertheless, we can use the above equations to extract meaningful information about the circuit to be designed. A more accurate method for estimating the saturation current is presented in [36], and is shown in Eq. 2.2, where n is a factor related to the body bias effect with typical values around $1.05 - 1.1$ in FDSOI MOSFETS.

$$I_{Dsat} \simeq \frac{\mu}{2} C_{ox} \frac{W}{L \times n}(V_{GS} - V_T)^2 \tag{2.2}$$

However, all of the above equations include the electron mobility μ_n and the capacitance per unit area C_{ox}, both of which are not disclosed. Thus, in order to extract the accurate behavior of the circuit, simulations must be run, for which a range of possible values for the different technology and device variables are needed. An analytical approach of the driver circuit needs to be performed to extract rough estimates for the Width (W) and bias conditions before the design can be optimized for typical and assumed values for μ_n and C_{ox}. These calculations and all related design decisions are further discussed in Section 4.4.

2.7.1 Cascode topology

For this project, the cascode topology has been selected as the most appropriate to fulfill the requirement specification both in terms of performance and in current stability. The technique described as cascoding has been used to improve analog circuits since the era of vacuum tube technology and has been documented thoroughly [41].

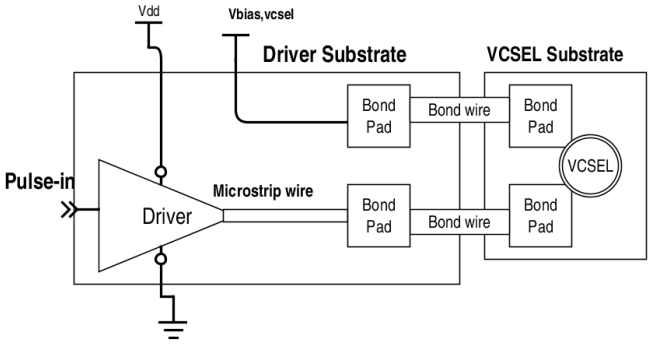


Figure 2.5: Proposed integration topology of the driver-VCSEL system with wire-bonding including the parasitics.

A cascode stage is essentially a two stage amplification stage comprised of two parts, one operating as a transconductance amplifier and the other as a current buffer. In this project the two stages are two MOSFET devices, a common source device to serve as the transconductance amplifier providing the modulation current, and a common gate device that serves as a buffer to isolate the current source from external voltage variations, provide higher output impedance and improve the bandwidth.

In the typical cascode topology the two stages are biased through a bias resistor, commonly called R_D, however, in this design the bias resistor has been replaced by the load which is the complex VCSEL impedance. This has the benefit of reducing the power consumption which would otherwise would dissipate on the bias resistor, but, as it is discussed in Section 6.3.3, introduces issues with the biasing of the driver.

2.8 Design and integration

The problem of integrating the driver and light emitter is a complex one for several reasons. The two dice are made using different fabrication processes and materials. Since they are fabricated separately, they need to be integrated and the electrical connections between them need to be done via additional process steps. A proposed topology for integrating the two devices including the interconnects, presented in [17], is shown in Fig. 2.5.

Additionally, the nature and parameters of those interconnects need to be carefully controlled due to the high frequencies of the system and the strict signal and power integrity requirements.

In the design process of such a system, several steps are needed, including: the schematic design, layout design, the cross-referencing of those two designs, modeling of the interconnect and light emitter behavior, simulating and verifying the complete system's functionality, E/M analysis of the design possibly including the interconnects and the VCSEL and finally preparation for tape-out. All of the above have been shown necessary in the design of high frequency CMOS drivers [42]. The steps are further illustrated in Chapter 3.

3

Method

In this chapter we present the method that is followed in this project. However, design decisions and requirement discussions are presented in Chapter 4.

3.1 Methodologies used

The various methodologies that were followed in this study are presented in this section.

3.1.1 Background study

During the early stages of the project, a literature study was conducted regarding the broader field of optical interconnect systems. This study was meant to set the appropriate background for the smooth flow of work and to allow for better time assessment of the tasks to be performed. It also provided an indication of the proper tools and methods to test the driver and also a framework for comparisons of the 28 nm driver with the 65 nm and with other driver designs found in literature.

3.1.2 Design process

The design process followed the background study and combined further reading of various design architectures, simulating them and proposing new designs. Among the many different laser driver topologies existing, the one that was deemed adequate for this project was a cascode current source driver circuit. As discussed in Chapter 2 this has been used in literature and has some critical advantages for this type of system. The cascode stage is simple enough, while being a decent current source that can provide stable current at high modulation frequencies. Additionally it is innately power efficient, compared to differential driver topologies since it does not waste half of the energy to drive a dummy load. For the same reason, however, it is more sensitive to supply noise so careful characterisation of the parasitic and E/M effects is required.

The main limitation of the design process was to adapt the driver to the load which consists of the VCSEL diode, together with the interconnect parasitics. In previous work we showed that the wire-bond, and wire parasitics between the load and the driver can have detrimental effects on the signal quality, especially at those high frequencies, due to the L-C oscillations that emerge between the inductive wire-bond and the capacitive bond-pads [17]. Therefore, the scattering parameters of the loads need to be simulated for various bonding scenarios and the driver needs to be adapted if necessary.

3.1.3 Results

During the comparisons between the proposed architecture and the ones existing in literature, special care needed to be taken in order for those comparisons to be fair. All results presented in this report were based on simulated values as well as simulated models of the load and packaging. Since most of the previous laser driver designs provide measured results on the fabricated chips, it is expected that our results would be better, since they did not include the fabrication–induced variations. Thus, any conclusions about the behavior of the driver designed should be assessed with moderation when providing minor improvements on the existing results.

3.1.4 Driver Parametrization

The most critical part of the design process were to match the requirements in terms of current, frequency, and power efficiency imposed by the VCSEL. The VCSEL diodes are in fact non-linear devices especially in high modulation currents. They present a dynamic resistance sensitive to the bias current as well as the modulation frequency, so predicting system behavior accurately without performing real tests is difficult.

The best way to alleviate this issue to an extent, together with any variations induced by the fabrication of the chip, were to make the driver chip as parameterizable as possible during testing. This was done by allowing one or more degrees of freedom that exist during the design and verification process to persist to the final chip. The driver that served as a basis for this study, presented in [11], had two degrees of freedom already implemented, by allowing the bias current point and the modulation current to be adjusted by two control voltages. This idea has been utilised in the current design, albeit adapted to the bias and modulation current requirements of our VCSEL diode. Additionally, the FD-SOI process allows for great control of the body bias of the chip, without negatively affecting the behavior of the devices. Thus, by increasing the body bias voltage allowed us to further set the operating point and drawn current of the chip.

With those three variables implemented, the final chip would have a very large range of operating points. Therefore, we must also guarantee the proper functionality of the driver in all those points. Thus, during the course of this project we will provide suggested operating points in terms of current levels, performance and energy efficiency along with the maximum and minimum allowed values of the control voltages where we can guarantee the functionality required.

Ultimately, one can also argue that the current driver circuit can be used to drive different VCSEL loads as well given its versatility.

3.2 Simulation and characterisation

In this section we present the methods that will be used during the simulation and characterisation parts of the project.

3.2.1 Power and Energy

It was required to calculate the energy efficiency of the system in order to be able to compare it with the already existing architectures. In order to do that, we had to extract the energy per symbol or energy per bit values from the simulations. However, energy cannot be calculated directly. Therefore, the instantaneous power was calculated on simulations for a time period and then the energy values were extracted by integrating the power over time, as shown in Eq. 3.1.

$$E_t = \int_0^t P_{inst}(t)dt \tag{3.1}$$

The signal is of periodic nature, so we needed to calculate the energy per symbol transmitted in each period. That can be done in two ways. First, the Eq. 3.1 can be used to calculate the total energy E_t in the simulation of total time t_f. Then, that value can be divided by the total number of periods (symbols) N in the simulation to provide the *energy per symbol* E_s (see Eq. 3.2).

$$E_s = \int_0^{t_f} P_{inst}(t)dt \times \frac{1}{N} = \int_0^{t_f} P_{inst}(t)dt \times \frac{T}{t_f} \tag{3.2}$$

The *Energy per bit* E_b can be estimated by dividing the *Energy per symbol* by two. There is an error involved with this estimation since the different symbols of PAM do not typically carry the same energy. However, that estimation is considered accurate enough, provided that the simulations are run with random input signals that have roughly equal number of all the 4-PAM symbols.

Furthermore, an additional way of calculating the energy per bit will be utilised in order to compare the results obtained by the above method. The second way is presented in the next section.

Averaged pulse power

As mentioned earlier, since we have a periodic signal of period T, we can average the instantaneous power of the whole simulation time t_f in T-long windows in order to estimate the average instantaneous power of a symbol. A graphical representation of how the window is set can be seen in Fig. 3.1.

Then once the averaged instantaneous power has been calculated it can be displayed over the time of one period T. Subsequently Eq. 3.1 can be used from 0 to T in order to extract the energy per symbol. The graphical equivalent of the integral can be seen in Fig. 3.2. This method has the added benefit of not being affected by the different energy values of a symbol since everything is averaged.

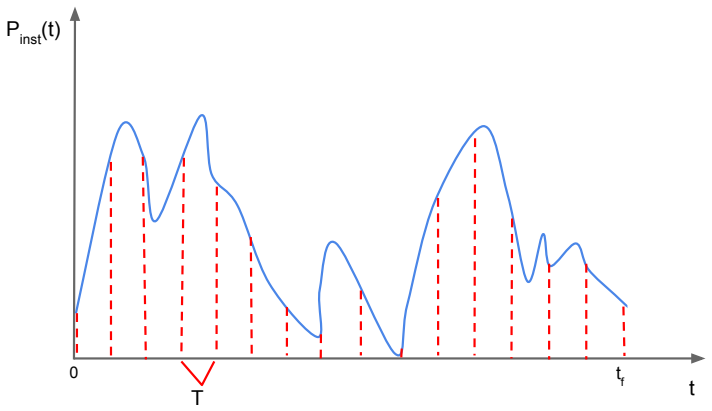


Figure 3.1: Instantaneous power of the total simulation time t_f broken down in periods of time T.

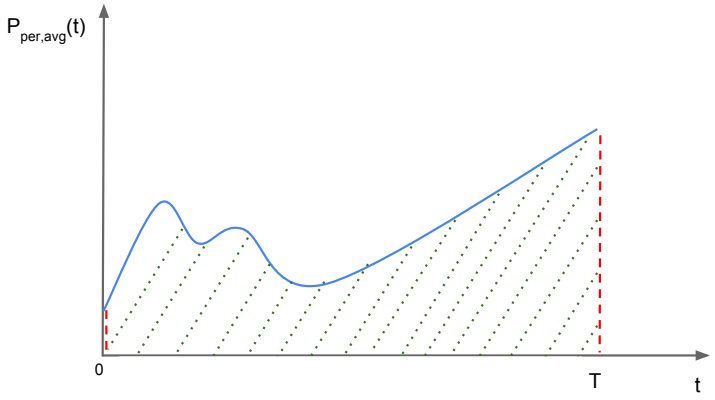


Figure 3.2: Averaged instantaneous power of a symbol. The dotted lines represent the surface given by the integral that represents the energy per symbol.

3.2.2 Extinction ratio

The extinction ratio (r_e) is a dimensionless metric (often expressed in dB) used in telecommunications to indicate the ratio of two power levels of a digital or optical output pulse. It is useful as a figure of the difference between the two possible transmitted levels.

A large extinction ratio means that the receiver will be more easily able to distinguish between the two different transmitted levels and therefore will be less like to make an error while deciding. The extinction ratio can be calculated by Eq. 3.3.

$$r_e = 10log(\frac{P_{max}}{P_{min}}) \tag{3.3}$$

In this project, we have the limitation on the minimum current, which should be above the threshold current of the VCSEL. Subsequently, the minimum power will be non-zero. Additionally, we do not have direct measurements of the *responsivity* (ρ) of the VCSEL diode and we cannot simulate the output optical power accurately from the model provided. Therefore, in order to assess the extinction ratio of the system we will have to suffice with measuring the ratio of currents through the driver, assuming that the responsivity of the VCSEL is linear in the range of modulation. We can relate the bias current with the power through Eq. 3.4.

$$I_0 = \rho \times P_0 \tag{3.4}$$

From Eq. 3.3 and Eq.3.4 we obtain the equation to calculate the extinction ratio from the current:

$$\begin{aligned} r_e &= 10log(\frac{\frac{I_{max}}{\rho}}{\frac{I_{min}}{\rho}}) \Rightarrow \\ r_e &= 10log(\frac{I_{max}}{I_{min}}) \end{aligned} \tag{3.5}$$

3.2.3 Eye patterns

In digital communication systems, one of the most utilised oscilloscope/ simulation displays is the the *Eye pattern*, also referred as *Eye diagram*, which provides a multitude of information about a signal and the transmission channel with a single simulation. Essentially every period of the output of a system is superimposed over each other on the y-axis while the x-axis is typically two to three pulse periods long in order to clearly cover all the pulse transitions. The eye pattern can provide information about the jitter between the pulses, the different rise and fall times between pulse transitions, noise in the channel, the noise margins of the signal as well as to which time is the optimal point to sample the output signal [24, pp. 490]. A graphical representation of a typical 4-PAM modulation eye diagram is shown in Fig. 3.3.

An eye diagram can also provide information about the matching between a transmitter and a receiver. In case of bad matching the reflections will severely affect the pattern as shown Fig. 3.4.

In optoelectronic links the vertical eye opening is also very important since it is what mainly defines the BER by setting the noise margin on the receiver. The horizontal opening is important for the receiver to perform timing recovery and proper decision point placement, which can be detrimental for the system, especially if the decision point placement is faulty.

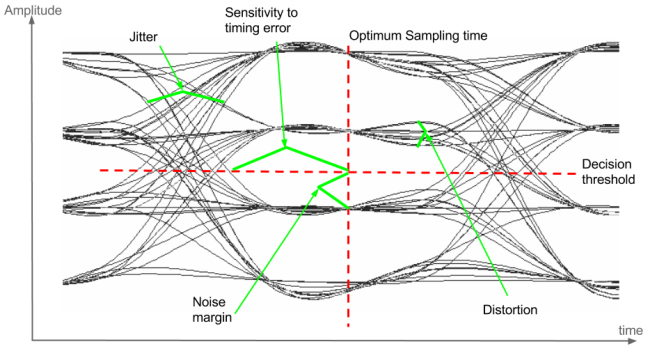
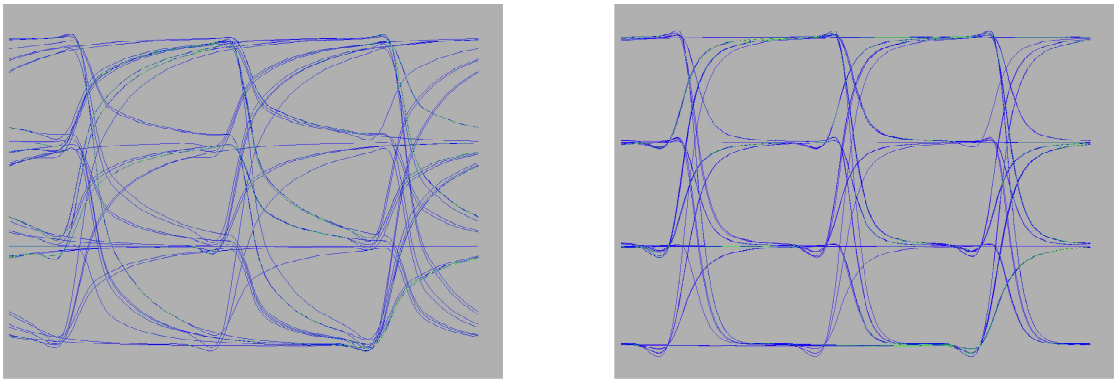


Figure 3.3: Sample eye diagram along with some of the signal figures that can be extracted by it.



(a) With reflections. **(b)** Without reflections.

Figure 3.4: Simulated binary PAM-4 eye diagrams that illustrate the effects of reflections induced by bad matching.

In this project, the most important aspect of the eye diagrams to preserve was be the vertical eye opening, or the current opening. This is because the driver is a transmitter device, therefore the requirements of the light emitter are the most critical. Furthermore, we lack the necessary knowledge about the nature of the receiver or the transfer medium in order to extract information about the channel noise or the sensitivity of the photo-receiver. Therefore, the main goal was to maximize the horizontal eye opening while meeting the vertical eye opening requirements.

3.3 Work model

The thesis project followed a hybrid approach between agile and linear project planning. The main activities of the project, or stories, were organized in a linear way. Each story was broken down in tasks, that were able to be run concurrently and followed a more agile planning.

Only two tasks were active at any given time-slot, which allowed for a certain extent

of multitasking to accommodate for delays from external factors (such as a problem with the software tools).

Re-iteration of certain tasks had been planned such as redesigning of the circuit if the E/M simulation results dictate so. Design tasks were also paired with simulation or evaluation tasks during the same week to further allow re-design if necessary.

As mentioned above, the project was divided in stories which in turn were comprised of individual tasks of work. The description of the planned stories with their respective tasks are presented in this section.

For detailed description of the work flow and organization of the project, see the time plan in Appendix E.

3.3.1 System Specification

This story was aimed at providing a good description of the system to be designed, based on the 65 nm transceiver already described in [11]. This was done by a literature study on the driver circuit and by simulating the circuit to obtain values required to perform comparisons between the 28 nm drive and the 65 nm drive circuits. Additionally, a description of the VCSEL light emitter used in this study in documentation and electrical model was created. The VCSEL model was then to be used when performing simulations to better estimate the performance of the driver with a more accurate representation of the load. Then a documentation of the characteristics, requirements and performance of the 65 nm circuit described in [11] were carried out by performing simulations on the circuit and obtaining values for performance and energy efficiency that were be used as benchmark for the new 28 nm driver circuit.

3.3.2 Driver design

This story included the main design process of the project: the driver circuit design, layout design, and the first set of measurements to characterise it. Additionally, a second design phase were to take place after the electro-magnetic analysis in order to refine the high frequency behavior of the parasitics.

Due to the fact that the 28 nm library has not been utilised extensively in the department, a learning and set-up time was expected and planned. Then, the design of the circuit of the driver in 28 nm library was performed, together with verification and characterisation of each individual submodule. If the design kit allowed it, the layout of the 28 nm driver were to be created and parasitic extraction to be be performed as a first way to predict the circuits real performance characteristics. Finally, energy and performance measurements were done to provide an insight on the quality of the design. Additional iterative steps, were also planned, between redesign of the layout and measurement, until a satisfactory result (compared to the system specification above) was reached.

3.3.3 Optional Tasks

If the time allowed the following steps were also planned to further prepare the driver for fabrication.

E/M simulation

This story included learning the high frequency structural simulator (HFSS) software, making an electromagnetic model of the circuit, and extracting impedance characteristics in order to do impedance matching between the VCSEL and the driver to minimise losses. A prerequisite for this story was to have the driver circuit's layout ready at hand, in order for the 3 dimensional model to be created, upon which the HFSS software would run.

The HFSS software first needed to be properly set up and tested. Then a 3-D model of the physical layout of the driver needed to be created in a way to comply with the requirements of the software. Then the high frequency parasitic values could be extracted in order to design an impedance matching network if it is required.

Tape-out Preparation

In this story, the necessary steps were planned to be performed in order to prepare the circuit for Tape-out. It includes the obtaining of information regarding the requirements of the tape-out as well as material and design rule information. Then, finalization of the design with fixed values for all the components and fine-tuning calibrations would be performed. The last step was the production of the stream file required by the fabrication plant in order to print the circuit board.

4

Design Decisions

4.1 System specification

In order to design the driver circuit for an optoelectronic communication link, there are a multitude of subsystems that need to be taken into account: the encoding of the information, the driver and pre-driver circuits, the light emitter, the optical fiber, the optical receiver, and the receiver electronics.

As mentioned earlier, only the transmitting part will be discussed in this report, and more specifically the stages after the encoding of the information up until the light emitter. That includes the driver and any pre-driver circuit, the VCSEL, and the interconnects between the two.

4.2 System Overview

The circuit topology used, is based on the design where the transceiver circuit is mounted on a 32 mm $\times$ 32 mm circuit board that includes the driver IC, two VCSEL lasers and some additional components such as thermistors for thermal monitoring [43].

In the current study, only the transmitter circuit is considered. The modeled circuit is composed by the driver electronics and a single VCSEL along with their respective power networks and the parasitics included. The two devices are assumed to be connected via wire-bonding, with the exact specifications being assumed based on the typical values for the technology node.

The circuit schematic as seen in Fig. 4.1 shows the driver, the laser, the power network on both devices, the power grid parasitics, and the interconnect parasitic component which includes the parasitics between the output of the driver towards the bond-pad, the wire-bond and the bond-pad parasitics.

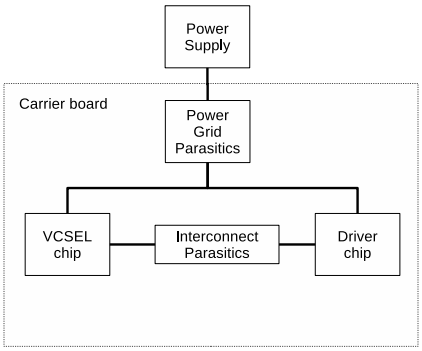


Figure 4.1: Block diagram of the system.

4.2.1 Laser driver circuit

The laser driver circuit is based on the implementation found in [11] of a 65nm CMOS driver circuit. In the current study a few simplifications have been done to the design as seen in Fig. 4.2.

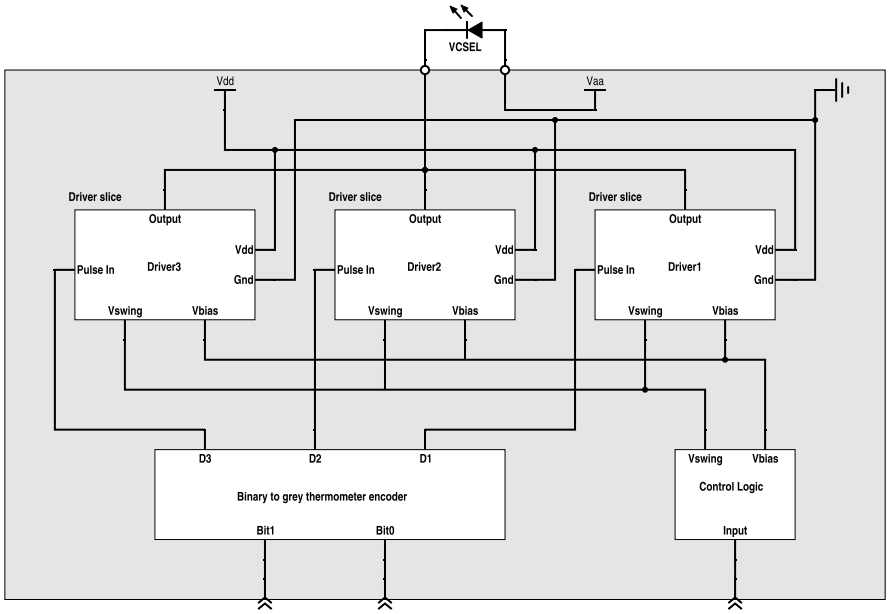


Figure 4.2: Block schematic of the complete driver architecture.

The driver is divided in two distinct parts, the control logic and the driver slices.

The control logic includes the circuit that translates the two 25 GHz bit-streams into thermometer encoding required for the current PAM-4 implementation. It also includes the circuit for controlling the bias and voltage swing levels (V_{bias} and V_{swing}) of the individual driver slices.

The driver slices are the main driver circuits that bias and drive the VCSEL by

pulling current through it. The VCSEL is constantly biased with a bias current (I_{bias}) above its threshold current to avoid the turn-on delay, but as close to the threshold current as possible in order to minimise the DC power consumption. The bias current also corresponds to the 1^{st} PAM-4 symbol, while each driver slice drives an additional current of ΔI_{mod} while its input is high, effectively realizing the thermometer encoding.

PAM-4 Encoder

The thermometer PAM-4 encoding was done via Gray coding in order to minimise the BER. The truth table is shown in Table 4.1, where A and B are the input bit-streams, PAM corresponds to the PAM-4 symbol to be transmitted and X,Y,Z correspond to the driver slices that will be active.

Table 4.1: Truth table of the PAM-4 binary to thermometer encoder.

A	B	PAM	X	Y	Z
0	0	1	0	0	0
0	1	2	1	0	0
1	1	3	1	1	0
1	0	4	1	1	1

As can be extracted from the truth table, each of the outputs can be implemented using boolean logic as follows:

- $X = A\ OR\ B = \bar{A}\ NAND\ \bar{B}$
- $Y = A$
- $Z = A\ AND\ \bar{B} = \bar{A}\ NOR\ B$

In this implementation the NAND and NOR logic will be used since they require less gates. However for the Y output, a pair of inverters will be used in order to properly drive the driver slice and to ensure that the driving signals arrive at the driver slices as concurrently as possible. The Binary-to-thermometer encoding block is shown in Fig. 4.3.

Driver slices

The driver circuit model that corresponds to a single slice of the Driver, and was used for the simulations is shown in Fig. 4.4 and the complete circuit from Cadence in Fig. B.1.

In Fig. 4.4 the first inverter corresponds to the pre-driver circuit in order to minimise the load on the binary-to-thermometer encoder's gates. Since the transistor sizes affect their current-driving capabilities and their respective rise and fall times, it might be necessary to replace that simple inverter driver with a more suitable pre-driver circuit of multiple stages.

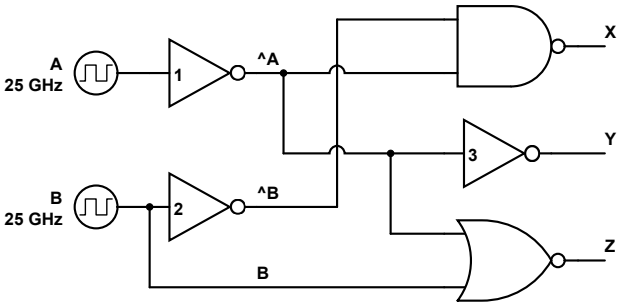


Figure 4.3: Logic diagram of the binary-to-thermometer Gray encoder.

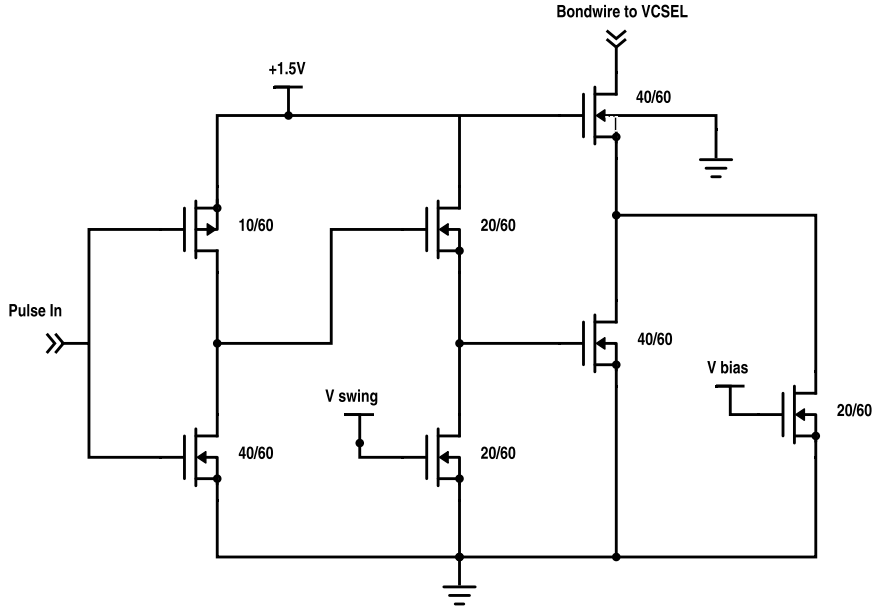


Figure 4.4: Schematic of a driver slice derived from [11] including a buffer inverter. The MOSFET dimensions (channel width/length) are in μm/nm and were used in the first test setup.

4.2.2 VCSEL

Physical characteristics

The VCSEL chip is designed in CTH and it is shown in Fig. C.1a. The die has dimensions of 375 $\mu m \times 325\ \mu m \times 200\ \mu m$. The substrate is Teflon and the bond-pads are Ti/Au 150/5000 Å on BCB.

The VCSEL emits light at 845 nm, it has a threshold current of ≈ 1 mA, an input resistance of 90 Ω, and an input capacitance of 170 fF.

An equivalent circuit of the VCSEL was modeled in order to be used in the simulations with cadence. The model is further described in Appendix C. The original device

that was assumed for this project was presented in [1].

4.3 Requirements

In this section, the requirement specification of the driver design is described.

4.3.1 Performance requirements

The optoelectronic link has a target bit-rate of 50 – 55 Gbps with direct modulating the laser diode. In order for that to be achieved with the current laser with a bandwidth of ≈ 25 GHz, a form of modulation scheme, other than On-off-keying, must be used.

With the use of NRZ (Non Return Zero) modulation scheme, a bit-rate of 55 Gbps has been demonstrated with an equivalent VCSEL. However, the driver circuit was designed on SiGe 130 nm Bi-CMOS technology in order to cope with the high performance required [29, 43].

The most promising modulation mode for 28 nm CMOS driver is 4-PAM (Pulse Amplitude Modulation) which has already been demonstrated to achieve above 55 Gbps bit-rates with a 25 GHz Bandwidth VCSEL [25]. Additionally, a 65 nm CMOS driver has achieved 58 Gbps baud-rate [11]. Thus, in the current technology node (at 28 nm) a PAM-4 driver should theoretically outperform the 65 nm one due to its higher intrinsic performance and power efficiency.

4.3.2 Current requirements

The threshold current of the VCSEL for this study is assumed to be ≈ 1 mA, while the modulation current required in the receiver to be able to distinguish the different PAM levels must be $\approx 5 - 7$ mA per step. Thus, in total the driver circuit must be able to drive $I_{bias} + 3\Delta I_{mod}$ for a total of at least ≈ 16 mA.

Since the VCSEL exhibits a total junction and contact resistance of 90 Ω, that gives us a voltage drop across the diode that will range between $\{90\text{ mV} - 1.44\text{ V}\}$. Therefore, the driver must be able to provide constant current across a range of 1.4 Volts. An ideal current source should provide constant current independent of the voltage at the input, however since this is a real implementation, special measures have to be taken in order for a CMOS driver to be able to function at that diverse voltage range.

Additionally, the real VCSEL diode exhibits an additional dynamic resistance that is dependent on the frequency of modulation as well as the temperature. This resistance will further increase the above voltage drop across the junction. Since this behavior is not captured by the VCSEL electrical equivalent model used as a test load for this study, the design needs to take this into account as well.

The modulation current is derived from the differential power efficiency of the VCSEL and in literature it takes values between a few hundreds of μA up to 2 mA in low power architectures [11] and is set at ≈ 5 mA for this design.

4.3.3 Energy efficiency requirements

The driver architecture is a similar design to the one described in [11] and corresponds to one slice of the PAM-4 driver. That circuit was designed to work up to 55 GHz with PAM-4 with a BER $< 1E-12$ and a power efficiency of 0.56 pJ/b at that frequency.

This energy efficiency however includes: the SPI interface of the designed chip, the logic required for the PAM and the Gray encoding, the 3 individual driver slices, but not the light emitter.

Therefore, a series of energy simulations have to be done in one slice of the 65 nm driver in order to compare its energy efficiency with the 28 nm driver to be designed.

4.4 Design considerations

In this section, considerations that arise during the design process are presented along with any decisions made, backed up by their motivation.

4.4.1 Driver slice functionality

When designing circuits that interact with analog devices such as the VCSEL diode mentioned in the earlier chapters, one of the most important decisions is the sizing of the transistors. Since the technology node is fixed, the channel length of the transistors together with their oxide capacitance per unit width are fixed. Thus, only the width of the devices provides a certain degree of freedom by directly affecting the current that the device can sustain as well as the gate capacitance of that device.

In order to calculate the transistor sizes we need to first analyze the driver schematics. The driver can be broken down in two stages as seen in Fig. 4.5.

An analysis of the circuit can be done separately for each stage with the following assumptions:

- The gate-source current I_{G-S4} is considered to be 0.
- This analysis does not consider dynamic effects under high speed charge and discharge of the gate capacitance C_{g4}.
- V_{in} is either equal to V_{dd} or 0.
- The body effect on *M1* and *M3* which raises their respective threshold voltages is not considered in this preliminary analysis.

First stage

The first stage serves as a level shifter of the input pulse. The shift of the V_x in regards to V_{in} is controlled by the voltage V_{swing}.

The N-MOS *M1* is either in saturation or in the cut-off region since V_{in} is a full swing pulse. The current through *M1* and the stage 1 in general will be set by the transistor *M2*. In order to obtain greater control over that current and subsequently to the voltage V_x, that serves as the output of that stage, we opt to bias *M2* in the linear

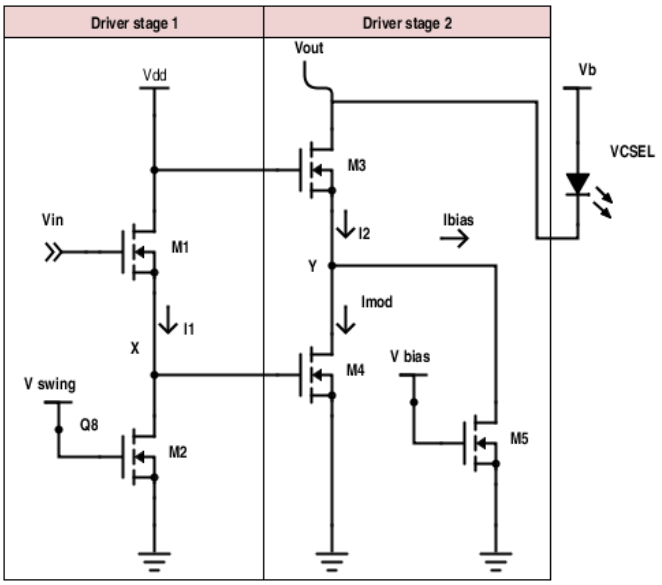


Figure 4.5: Circuit schematic of a single driver slice divided into its two stages. The source follower stage (stage 1) and the Cascode stage (stage 2).

- triode region. That is because a MOS in the linear region behaves approximately as a voltage controlled resistor, effectively setting the current through the node X and therefore setting the voltage on that point.

So the transistor *M2* will set the current I_1 and by definition the current through *M1* will be the same when it is on saturation and virtually 0 when it is in cut-off.

The main constraint in this stage for the static behavior of the driver is to keep *M2* in the linear region, while keeping a high enough V_x that will also keep $M4$ in saturation and with enough current I_{mod}.

Second stage

If the second stage of the driver is considered individually we can see it represents a well documented cascode gain stage as long as we do not consider *M5* and the current I_{bias} important in this analysis [41].

In this stage *M3* sets the (maximum) bias current through the node Y: I_2 which is split in the bias current: I_{bias} and the modulation current I_{mod} which in turn is controlled by $V_{GS4} = V_x$ the input voltage of the second stage.

Since the driver slice is supposed to operate as a current source, it should ideally remain unaffected by voltage fluctuations at the output of the driver (drain terminal of *M3*). However, this cannot be achieved, especially considering the fact that 1 to 3 driver slices will switch on and off at the same time affecting V_{out}. In this case the constraint for V_{out} has to be high enough to keep all MOSFETs of Stage 2 in saturation, in order to maintain as constant current as possible.

4.4.2 Dynamic behavior

We have some additional concerns for the dynamic behavior of the driver, referring to high frequency modulation.

On Stage 1, *M1* must be able to drive enough current to charge the gate capacitance of *M4* while still driving *M2* to keep V_x high (as mentioned above). This also has to happen fast enough to not affect the next pulse. That means that the sizing of *M1* should be substantially bigger than *M2*. Additionally, when a falling edge appears at the input, *M2* needs to be able to discharge the aforementioned gate capacitance in the same speed as *M1* to avoid an asymmetric rise / fall time in the input of *M4* which will distort the signal. However since the node V_x will be at a voltage just above the threshold voltage of *M4*, transistor *M2* will only have to reduce the voltage V_x below the threshold in order to turn *M4* off. Thus, there is a significant slack in the asymmetry of the rise and fall times in this case. Therefore, *M2* needs to be wide enough, and to be biased at a certain point, where it can still drive the same current as *M1*, while not lowering V_x below a certain voltage. An additional matter of concern is that since this is only the first stage of the driver, the current I_1 is effectively an overhead. Therefore, it needs to be as small as possible.

On stage 2 of the driver, the most important requirement related to the dynamic behavior is that the current I_{mod} needs to have a certain value that when transformed to optical power by the VCSEL can be distinguished by the remote receiver without errors as discussed in Section 2.5.3. Therefore, the sizing of the two MOSFETs *M3,M4* needs to be calculated in such a way that *M3* can provide enough current for both *M5* and *M4*.

4.4.3 E/M effects

Since the 25 GHz frequency of the system is high compared to typical CMOS designs, a more detailed analysis of the E/M effects is required. This analysis needs to be performed at the chip level by extracting the E/M parasitics due to the on chip interconnects and also in the output of the chip interconnects, between the driver and the light emitter.

Parasitic models

Ideally, a full 3-D model of the driver, including technology and material properties, will be needed to perform simulations using an E/M simulator software like Ansys HFSS (High Frequency Structural Solver). However, since the exact parameters of the technology and materials used in the driver are not disclosed, this report will consider the typical parasitic and E/M analysis of the Cadence tool-set sufficient.

The most important analysis that needs to be taken into account, concerns the effects of the impedance mismatch between the driver, the wire-bond interconnects and the VCSEL load. The wire-bond impedance depends largely on the length of the wire and the substrate to be used as well as in the technology. Typical wire-bond techniques used in such high frequencies are ball soldered round wires or preferably wedge bonded ribbon wires. The latter have lower impedance and lower inductance and are much less prone to the skin effect [44].

Bandwidth and rise time requirements

As discussed above, the signal frequency of 25 GHz justifies the microwave analysis. However, the highest frequency that is significant in the system is the frequency related to the rising edge of the pulse. An infinitely large bandwidth of harmonics is required to approach a square pulse. Therefore, the higher requirements in the pulse rise times increase the maximum bandwidth of the system accordingly.

If the system uses a Return-to-Zero implementation where a pulse has a 50% duty cycle, the rise time must be between one fifth to, at most, a quarter of the period. Thus, the frequency of 25 GHz gives us a period of 40 ps and, subsequently, a maximum rise time of 8 to 10 ps effectively increasing the required bandwidth of the system to 100 GHz. This bandwidth is derived by the clock frequency of the system while assuming perfectly square pulses. In reality, in order to represent a pulse we do not need all the harmonics included in the 100 GHz bandwidth. Based on the rule of thumb in bandwidth estimation for rise and fall times seen in Eq. 4.1, which only includes first order effects, we obtain a bandwith of 35–43.8 GHz.

$$\begin{aligned} \omega_{bw} &= \frac{2.2}{t_{rise}} \\ f_{bw} &= \frac{2.2}{2\pi t_{rise}} = \frac{0.35}{t_{rise}} \end{aligned} \tag{4.1}$$

Furthermore, in the case of PAM each symbol is represented by a single level and not a pulse, effectively increasing the maximum allowed rise time to 10 to 15 ps and reducing the bandwidth to $\approx$ 25–35 GHz.

Within the chip the rise-fall times are expected to vary with a maximum of 15 ps. Additionally the external inputs A and B are assumed to have equal rise and fall times of 8 ps. Those two input bit-streams are assumed to arrive at exactly the same time since any timing difference between the arrival of the inputs induces timing hazards in the encoding logic. In practice a maximum allowed time differences between the two inputs needs to be provided by simulating the effect.

Time of flight effect

A recurring issue in high frequencies and long wires is the so called time-of-flight effect. This appears when the wire length is comparable with the wavelength of the signal, in which case different parts of the wire experience large differences in the signal phase. When that happens, the wires cannot be treated as lumped loads and detailed impedance analysis needs to be performed, and matching is required in the wire [45, p. 178–186].

A study on the effects of this phenomenon has been presented in detail in previous works [17].

High frequency modeling

The need for the high frequency characterisation of the load, in this case the VCSEL including the wire-bonds, is justified above. The simulations of the complex load of the interconnects together with the laser are presented in Appendix D.2.

5

65nm Design

5.1 Driver prototype in 65 nm

As already discussed in earlier chapters, there is a need for a developed prototype in the 65 nm process in order to be used as a basis to study the behavior of the driver circuit before the 28 nm tools are available for use.

The circuit designed with a modular structure, to ease its characterisation and to allow for easier transfer to the new technology. In analog design, calculations such as: DC/AC analysis, and transistor sizing, are performed before the actual schematic. In this case however, that was not applicable. The main reason being that there is no need for accurate calibration of the 65 nm circuit since it has already been optimized and demonstrated in [11]. Therefore, this circuit was used as a proof of concept and exploratory ground until the 28 nm design kit is ready for use.

5.1.1 Circuit

The modular schematic test bench based on the discussions in Section 4.2 is shown in Appendix B.

The driver's behavior can be controlled by the two voltages V_{bias} and V_{swing}, which in turn control the bias current and driving current swing of each slice respectively. It is important to know that these two voltages do not represent the bias current or the current swing. They only control them within a range of values allowed by the CMOS device that does the actual driving.

5.1.2 Functionality

The correct functionality of the circuit can be verified by conducting several simulations in Cadence.

Firstly, the correct operation of the binary to thermometer encoder is verified and is shown in Fig. 5.1. In the figure, from top to bottom we have : A and B as the input bit

streams at 10 GHz each. X, Y and Z as the outputs of the encoder to the driver slices.

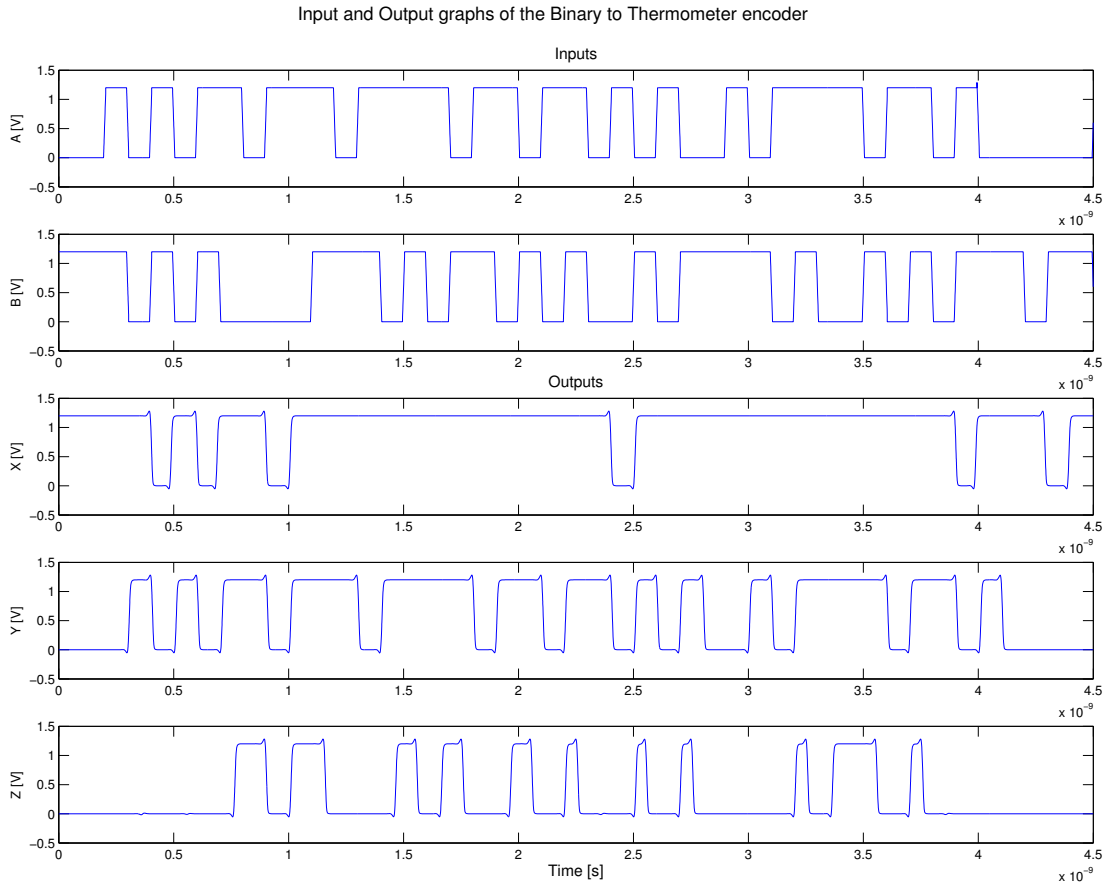


Figure 5.1: Simulation of the binary to thermometer encoder. From top to bottom: A and B are the input bit streams at 10 GHz, X, Y and Z are the outputs of the Thermometer encoder.

In order to verify the complete driver setup, we need to use an electrical VCSEL model discussed in Appendix C as a load for the driver. By connecting the VCSEL model as the load of the driver we get the resulting graphs presented in Fig. 5.2. In the figure, V_{driver} is the voltage at the output of the driver, $I_{optical}$ is the current at the cathode of the laser, and $V_{optical}$ is a voltage that corresponds to the output optical power of the laser.

As we can see in Fig. 5.2, the PAM levels are distinguishable, although a few glitches appear at the output voltage. This is probably due to the stacking behavior of the three driver slices that switch on and off at the same time, but requires further investigation. Additionally, it is evident that in such high frequencies the 65 nm driver exhibits slow rise times, which in turn cause some of the PAM symbols to appear as peaks instead of pulses. The issue becomes more prominent when the output takes two consecutive

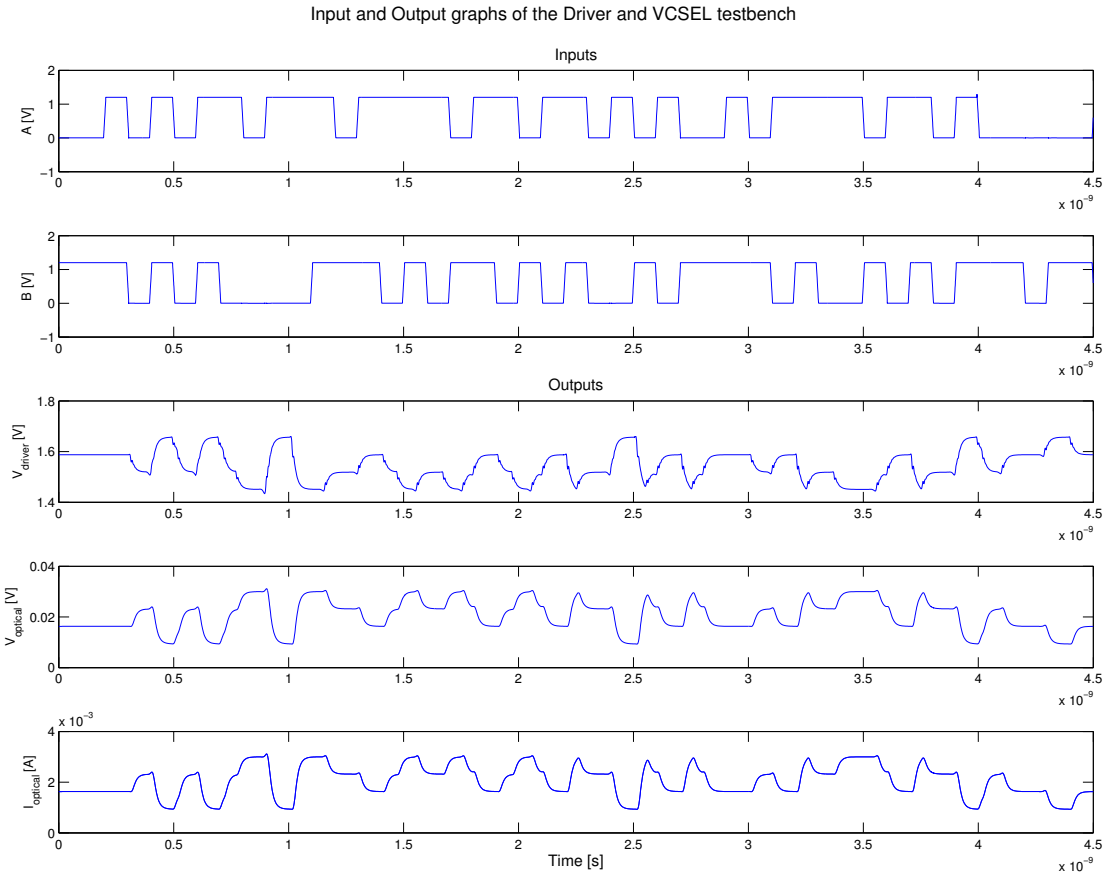


Figure 5.2: Simulation of the complete drive. From top to bottom: A and B are the input bit streams at 10 GHz, V_{driver} is the output voltage of the driver, and V_{driver}, $I_{optical}$ are the outputs of the VCSEL model.

symbols (see Fig. 5.2 V_{driver} at time 1.5 and 2). In such cases there is only a very short window between the rising edge settles until the next one starts rising and it is easier for the receiver to miss that symbol.

In Section 5.1.1 we discussed the two control voltages V_{bias} and V_{swing}. In order to observe the effect that those two voltages have in the behavior of the system, we performed a parametric analysis for various values of both. The results of the analysis are shown in Fig. 5.3.

As is evident from the graph, V_{bias} directly affects the bias current through the VCSEL. At this point, we have to note that in the figure the simulation starts with the PAM key ”1” instead of ”0”, therefore the starting current is not the same for the two values of V_{bias}. The bias current through the VCSEL is set for each device and needs to be higher than its $I_{threshold}$. That is in order to minimise the laser’s turn–on delay since it will be operated in high speed modulation. The V_{bias} voltage will be connected to an

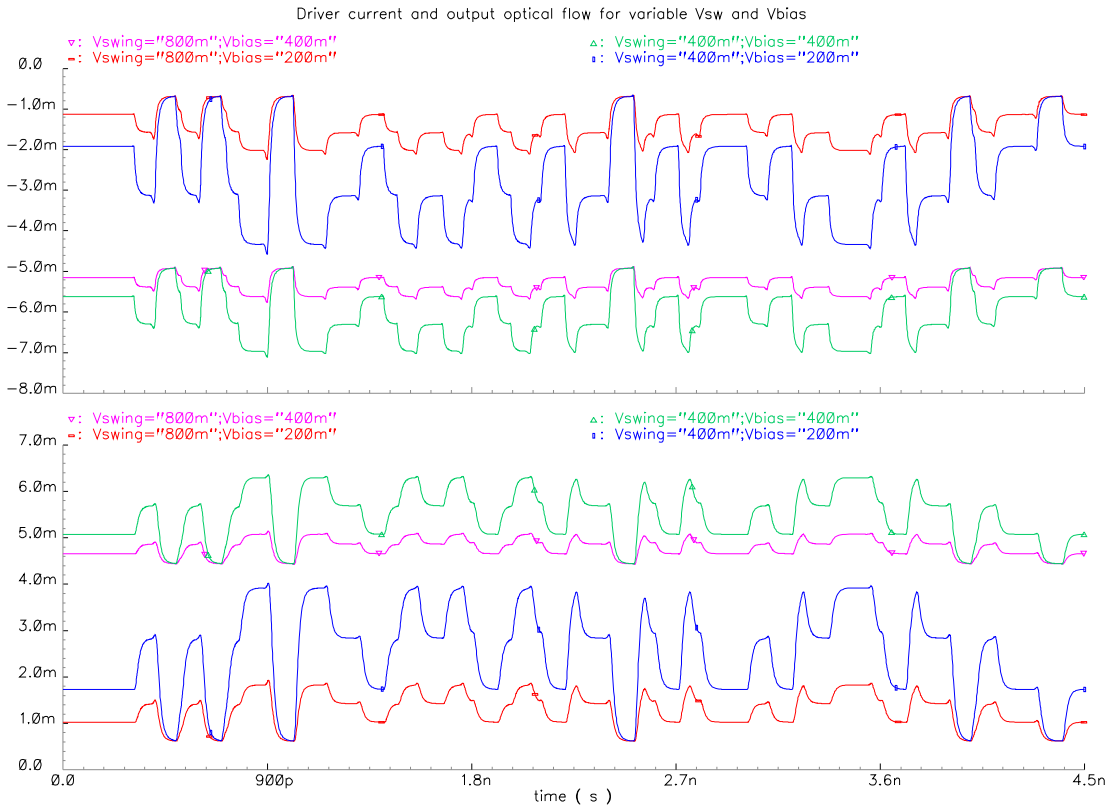


Figure 5.3: Simulation of the 65 nm drive for $V_{bias} = \{200, 400\}\ mV$ and $V_{swing} = \{400, 800\}\ mV$. Top: The current at the output of the driver - cathode of the VCSEL. Bottom: the optical current at the output of the VCSEL.

I/O pin of the final chip to allow the bias current to be adjusted externally for testing purposes. An additional reason is that the VCSEL is very sensitive to temperature variations, and the $I_{threshold}$ might require adjustments to compensate for that [43, 46].

The different values of V_{swing} affect each driver's output swing which translates to a larger current step between two consecutive PAM symbols. It is implicit that for a smaller power consumption, we will need as little current as possible through the driver. A large value of V_{swing} would reduce the output current swing, effectively delivering less power to the laser. That way it would achieve higher energy efficiency. At the same time, it would make the task of receiving and decoding the data more difficult and possibly more error prone. Thus, in order to chose the appropriate value for V_{swing}, we need to have information about the optical channel and the receiver characteristics. The same principle will apply at the 28 nm design and since it's meant for testing purposes, we opt to allow V_{swing} to be set externally to make the calibration process easier on the fabricated chip.

5.1.3 Load Characterization

The high frequency operation of the driver imposes some severe limitations regarding the load and the interconnects between the driver chip and the VCSEL chip. The total interconnect distance is comparable to the wavelength of the highest frequency existing in the system. When the signal is composed of pulses, then the highest frequency to properly represent the signal is the rising/falling edge of the pulse. Therefore, a complete electromagnetic analysis is required up to the frequency defined by the rising/falling times. Additionally, the interconnects together with the VCSEL load must be treated as complex impedance loads if the frequency is high enough.

As shown in previous work, the interconnect parasitics together with the complex load of the VCSEL affect the signal at the frequencies of interest [17]. In order to be able to characterise the performance of the driver in a more realistic scenario, we had to use a model of the channel between the driver and the VCSEL along with the VCSEL electrical model and extract the scattering (S) parameters. The interconnect model included the short interconnects and the bond pad on the driver chip, as well as the wire-bond to the laser chip. The S-parameters of the loads are shown in Fig. 5.4.

As we can see the S-21 parameters of the load drop by -3 dB at a frequency close to 50 GHz so this low-pass filter behavior does not affect the signal. However, it does affect the frequencies close to 45 GHz which are required to represent the rising edge of the pulse. Thus, the longer the interconnect, the more distorted the pulse will become [45, p. 160–167].

The S-11 parameters, which show us the reflected signal off of the load, exhibit good matching at the signal frequency of 25 GHz. In that case, the requirement of good S-11 matching is to have less than -10 dB of reflected signal which is apparent in Fig. 5.4 that does not hold for frequencies above 30 GHz. Thus, we are expecting to have reflections due to the harmonics induced by the square pulse, unless proper matching is done.

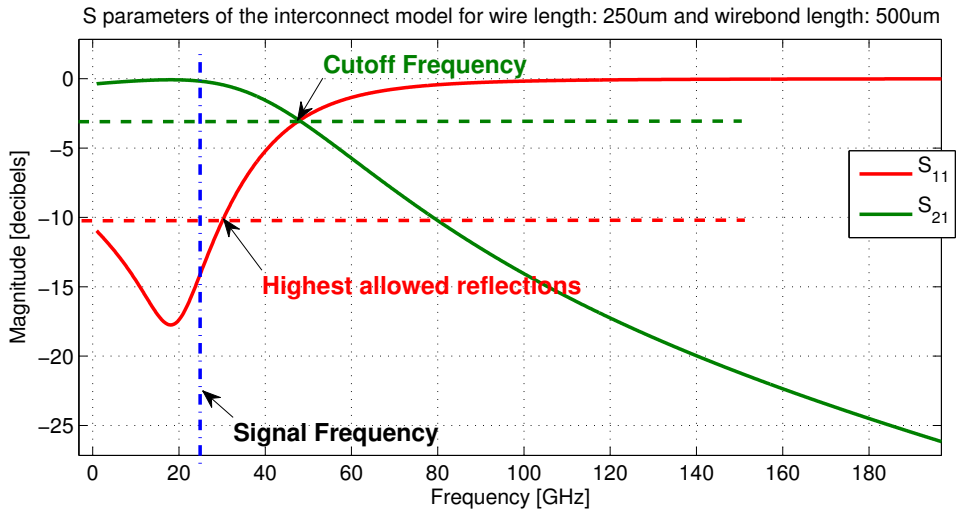


Figure 5.4: Graph of the S-parameters of the driver load including interconnects for wire length $w_l = 250\ \mu m$ and bond wire length $wb_l = 500\ \mu m$.

Additionally, in order to better understand the behavior of the interconnects and the VCSEL as a load, different implementations of the VCSEL equivalent model were used. The performance of each of these models, along with real measured values of the VCSEL diode are presented in Fig. 5.5.

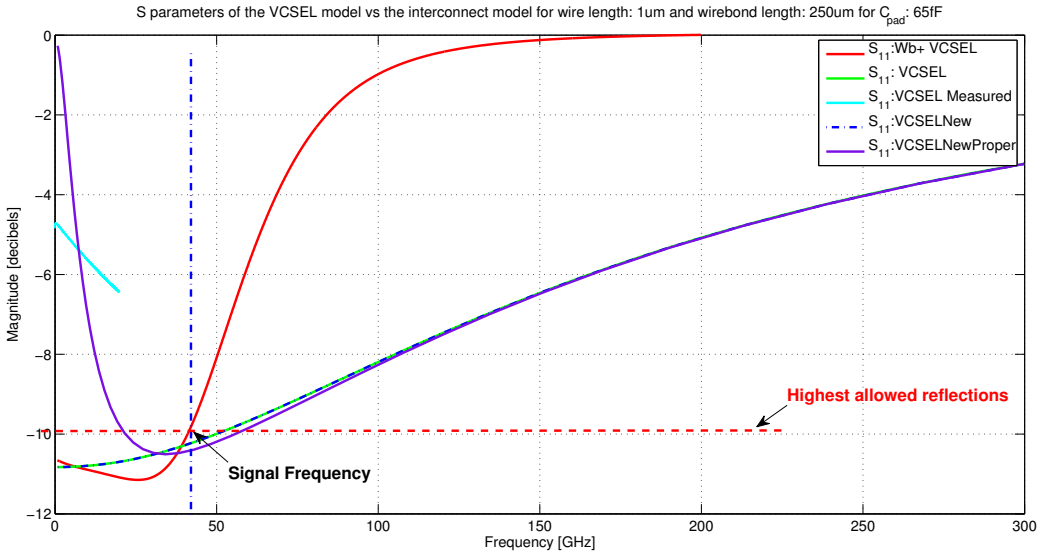


Figure 5.5: Graph of the S-11 parameters of the VCSEL load. *Red*: S-11 of the VCSEL including the wirebonds. *Green*: S-11 of the VCSEL model described in Verilog. *Cyan*: Measured S-11 from the fabricated VCSEL die. *Blue dashed*: Verilog-free VCSEL electrical equivalent model. *Purple*: VCSEL model with dynamic resistance modeling.

In Fig. 5.5, we can see that two implementations of the model agree (seen in green and dotted blue lines). That is because these behaviors are simplified versions of the VCSEL diode behavior and include verilog descriptions of some of the equations. In purple (*VCSEL NewProper*), we can see the complete (and verilog-free) electrical model of the VCSEL while in cyan (*VCSEL Measured*) we have the real measured values of the VCSEL diode. We can immediately see that the latter two experiments agree the most, and any discrepancies are attributed to the fact that the simplified electrical model is not accurate enough as it includes only first order effects.

Additional experiments with different sets of wire and wire-bond length parameters were used to compare their effect on the signal. The results of these experiments are presented in Appendix D.2.

5.1.4 Energy and Power

The power consumption of the current prototype is of great importance since the final design is meant to be energy efficient. Therefore, a parametric analysis on the two voltages, V_{bias} and V_{swing}, was done to better distinguish the bottlenecks of the design in terms of power. The results are shown in Fig. 5.6. As is evident from the figure, the most power is consumed when all three slices of the driver are on, which is expected

since that would draw the maximum current from the VCSEL. This increase in power consumed is occurring in spikes which is caused by the current flowing in CMOS logic when the gates are switching state. That can be further verified since that spikes in power only appear in the total power consumption and not in the VCSEL power consumption.

Additionally, we can see that the bias current varies from ≈ 1.5 to 5 mA, which has a great effect to the power of the VCSEL as well as to the total power. This is expected since most of the power consumed comes from the driving current through the VCSEL. The highest power dissipation appears for high V_{swing} values which in turn produces a high driving current on each of the driver slices.

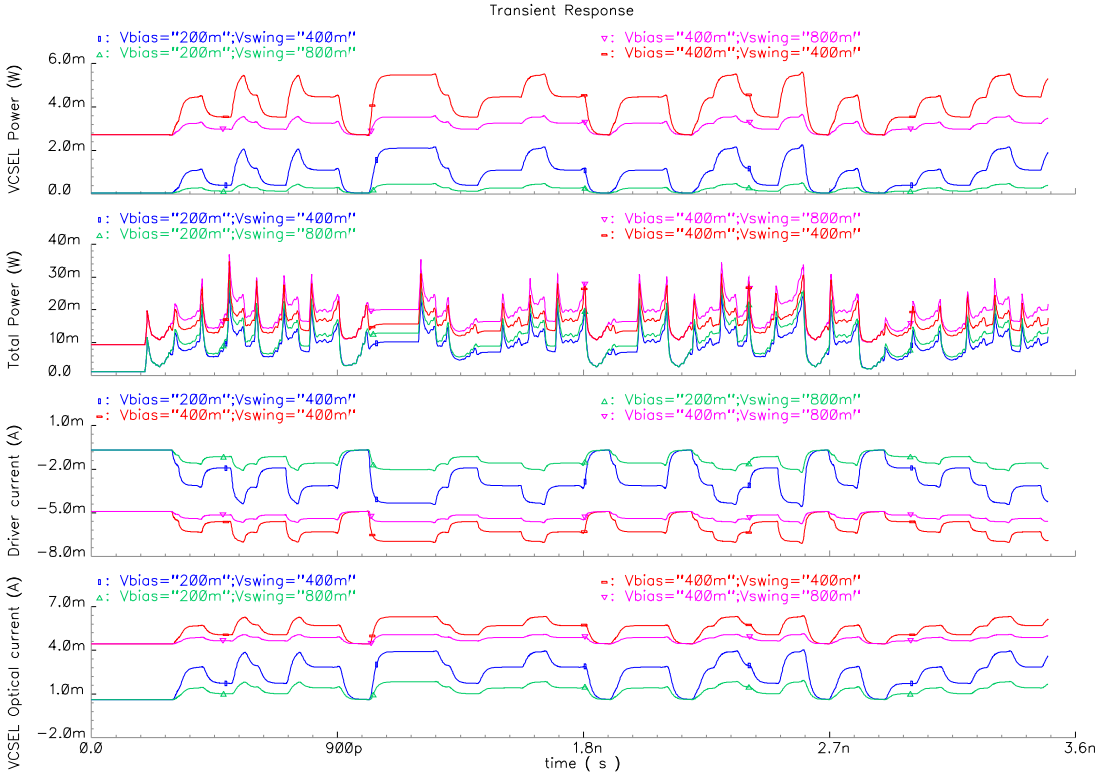


Figure 5.6: Power consumption of the 65 nm driver circuit vs the laser current and optical current. The parametric analysis is for $V_{bias} = \{200, 400\}\ mV$ and $V_{swing} = \{400, 800\}\ mV$.

When we consider the average power consumed by the driver, we can observe energy efficiency values on par with the ones demonstrated in literature [11]. The results of another parametric analysis for $V_{bias} = \{200, 400\}\ mV$ and $V_{swing} = \{400, 800\}\ mV$ are shown in Table 5.1. We must note, however, that this energy efficiency is misleading, since we have less than half of the baud-rate compared to literature. The values in Table 5.1 are obtained with the simple energy calculation method mentioned in Section 3.2.1.

Table 5.1: Average Power and power efficiency values of the 65 nm Driver circuit.

F [GHz]	Vsw [mV]	Vbias [mV]	Average Power [mW]	Power Efficiency [pJ/b]
10	200	800	11.2	0.56
10	200	400	8.8	0.44
10	400	400	15.7	0.79
10	400	800	17.8	0.89

6

28nm Design

In this chapter we will discuss the design of the 28 nm circuit.

6.1 MOS-FET devices

In order to be able to design and subsequently predict the operation of the driver, insight on the functionality of the MOS devices must be attained. This step is crucial to the design since the FDSOI process behaves differently from the long-channel models and idealised square law of saturation current discussed in Chapter 2.

While the encoder logic uses both N-MOS and P-MOS, the driver slices only utilise N-MOS transistors. However, a characterisation of both devices is important in order to be able to decide on the channel width of the final layout. Furthermore, since the operation of the driver is in high frequencies the MOSFET devices need to be characterised at and around those frequencies in order to get an understanding of their dynamic performance.

6.1.1 Device behavior

There are two devices that are suitable for the design of the driver: the typical N and P MOS devices, and their low threshold voltage counterparts. The low threshold voltage or *lvt* MOS have , as the name implies, lower threshold voltage. This allows these transistors to have a higher maximum saturation current, since the lower threshold voltage allows the devices to go into the linear region for smaller over-drive voltages. The downside however, is a higher leakage current due to sub-threshold effects, as well as a significantly lower early voltage V_A, which translates into a higher current slope in the saturation mode of the transistor. The high-Vt devices approximate the square-law MOSFET current model (presented in Section 2.7) better than the low-Vt ones, however they still exhibit a high saturation current slope due to short channel effects. The main cause is that the current becomes increasingly dependent on the drain voltage as the channel becomes shorter.

A graphical representation of the short channel devices compared to long channel ones is shown in Fig. 6.1. As we can see in the figure, the short-channel devices provide higher current (however the graph is in scale). Additionally we can see that the short-channel devices exhibit much steeper saturation slopes which can be mitigated or worsened by the effects of the threshold voltage. A lower threshold voltage will allow the MOS to go in the linear region for lower values of V_{gs} but it will also further decrease the early voltage effectively increasing the slope of the saturation current. A higher threshold voltage will make the device turn on for slightly higher values of V_{gs} but it will allow for a more stable saturation current (Fig. 6.2).

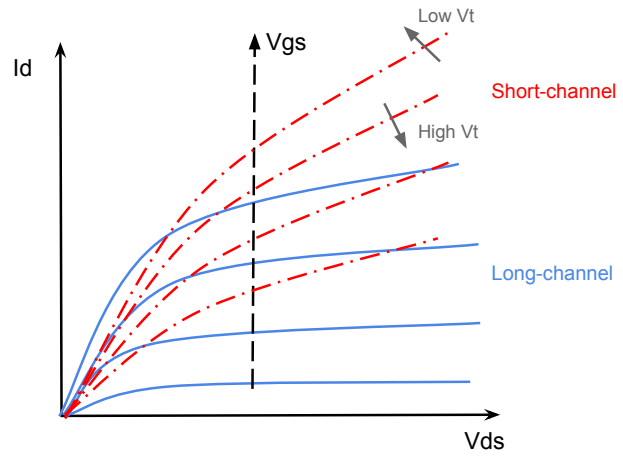


Figure 6.1: Graphic representation of the I-V_{ds} characteristic for short and long channel N-MOS devices for various values of V_{GS}.

6.1.2 Over drive voltage effects

The saturation current of the MOSFET devices depends on both V_{GS} and V_{DS} due to small channel-length modulation effects, as discussed in Chapter 2 and Section 6.1.1. Furthermore, the design kit offers an array of different devices, among them the nominal *N* and *P MOS* and their low voltage counterparts *lvtNmos* and *lvtPmos*.

An extensive analysis of the device performance for various gate and drain voltages was carried out but the device sweeps are protected by the non-disclosure agreement covering the 28 nm design kit.

The results motivated us to design the logic gates using the *lvt* gates. This will increase their leakage current when switching so it will increase the dissipated power. However, the logic gates to be used in the digital parts of the design, such as the encoder, do not need to be wide transistors. Since speed and timing are critical in the digital encoder, the *lvt MOSFETs* will provide higher saturation current which in turn will help minimise the rise and fall times of the logic gates.

On the other hand, the typical N-FETs will be utilised in the main driver stage where

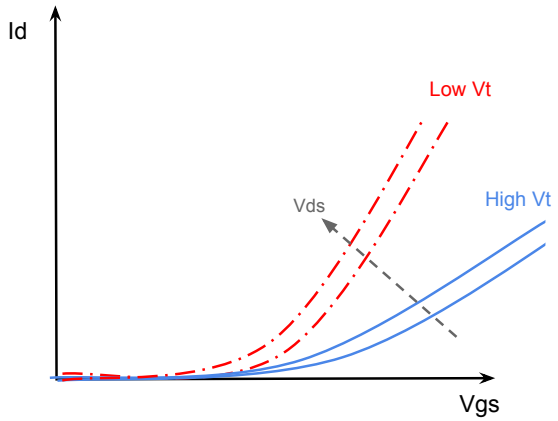


Figure 6.2: Graphic representation of the I-V_{gs} characteristic for low and high threshold N-MOS devices.

the transistors need to be exceptionally wide. Wider transistors have higher leakage current, therefore, by using the lower leakage devices we can minimise the power lost due to leakage. In the pre-driving stage however, the speed of the devices is more critical so *lvt* devices might be selected. Even though the driver by definition demands high currents from the devices, a constant saturation current (or one with a lower sensitivity to changes in the voltage) is much more preferable for a current source design such as this. Especially since 3 identical very wide transistors will be driving a current on the same load, which will lead significant drops in the output voltage of the driver as discussed in Section 4.3.

The driver can also be divided into two stages, the pre-driving stage that works as a level shifter, and the main driving stage. The above arguments apply mostly for the main driving stage but whether or not the pre-driver should be designed with the lvt transistors needs to be investigated. This is performed in Section 6.3.

6.2 Encoding logic

As mentioned in earlier chapters, a Gray encoding is employed in order to minimise the impact of an erroneous symbol to the BER. In Gray encoding, neighboring symbols only differ by a single bit. Thus, a miss-interpretation of a received symbol by the receiver can only be wrong by one bit.

Additionally, the thermometer encoding assigns each PAM-4 symbol to a specific current level comprised by 3 identical parallel driver slices. The slices turn on additively to produce the necessary current for the PAM symbol to be transmitted. When a symbol is sent, some of the driver slices will turn on or off in unison but there will never be two slices making different transitions at the same time. This will minimise the dynamic

effects between the slices even though they are connected to the same load.

However, in order for the system to have a low BER, a wide eye opening needs to be achieved. The fact that all the slices turn on or off at the same time will have an effect on the voltage at the output of the driver. This is problematic since the output voltage is also the bias point of the 3 driver slices. If the voltage in the output of the driver becomes too low, then the NMOSes that comprise each driver slice are in the risk of falling into the linear region of operation which will significantly affect their current driving capabilities.

6.2.1 Gate sizing

The most straightforward way to minimise the delay between the outputs is to size the gates of each path - or branch - accordingly. That, in conjunction with additional buffers-inverters before and after each branch allows a great extent of control over the delay of the paths. The schematic of the binary to thermometer Gray encoder is shown in Fig. 6.3. Since the design kit is protected by the NDA, we cannot disclose the exact sizes of the gates, but we can provide the relations between them. The sizes of each logic gate are in relation to a unit inverter decided for this design with sizes 1/2 for N-MOS / P-MOS respectively. The buffers in the output of each path have a large size in order to account for the driving of the substantially wider driver slice transistors.

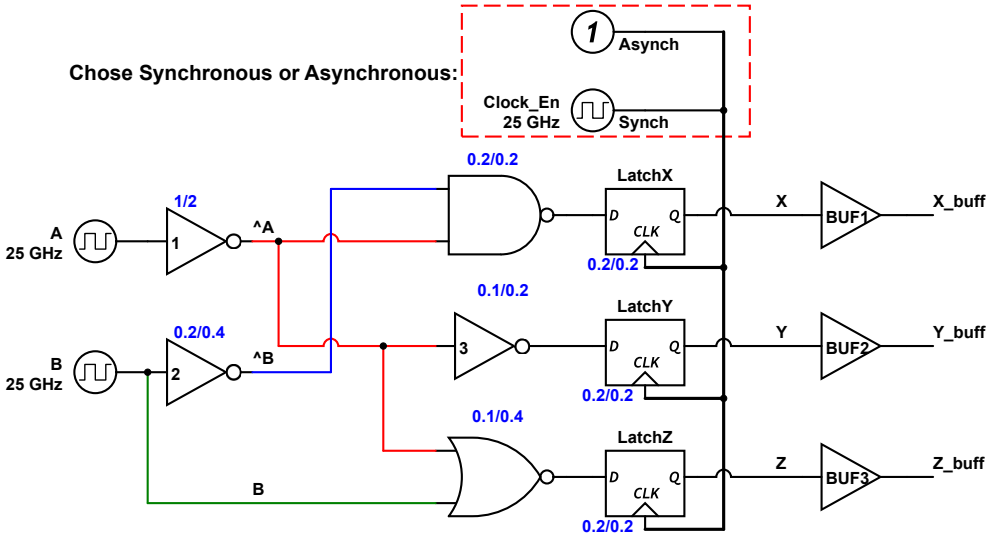


Figure 6.3: Schematic of the binary to thermometer Gray encoder including transistor relative sizes (N-mos/P-mos) and output driving buffers. The widths are in relation to a unit inverter defined in order to protect the sensitive process parameters covered by the NDA.

In Fig. 6.3 the critical branch can be seen in red, the next most critical in blue and finally in green we can see the least critical branch. As one can see, *Inverter 1* is severely loaded with three gates . Even though the traditional scheme for calculating

the Elmore delay [47] indicates that the typical scaling factor is between 3-4, *Inverter 1* is significantly larger. That is to ensure that the gates being driven by that inverter have a time constant similar to that of the green branch. Alternatively, a set of unity buffers can be included in the green branch in order to slow it down on par with the red one. Additionally, a set of NAND logic D-latches have been introduced to the output of each path. The latches are driven by a clock at the same frequency as the two inputs but at a lower duty cycle. When the clock is high, the latches become transparent and the three outputs of the encoder (X, Y, Z) are transmitted in unison to the next stage, the buffers. Further motivation on the use of the latches is presented in Section 6.2.4.

6.2.2 Implementation

The performance of the encoder cell without buffers in the output is shown in Fig. 6.4. The plot shows a parametric analysis of the inputs of the encoder {*A, A', B, B'*} and the outputs {X, Y, Z} together with the total current drawn by the cell for values of gate widths between 0.3 and 1 of the unit inverter size discussed above. That *width multiplier* is applied to all gate sizes shown in Fig. 6.4 and is used to study the effects of the encoder sizing in its performance.

In the figure, we can see that the outputs correspond to the truth table presented earlier (Table 4.1). The only effect that the *width multiplier* appears to have, is the increase in the drawn current which is expected since wider transistors have higher current. Also, it is apparent that the rise and fall times of all the logic gates are significantly smaller compared to the pulse width. Therefore we conclude that the gates at this size can successfully function in the required frequency.

6.2.3 Timing glitches

In order to address the aforementioned effects of timing delay glitches between the encoded values {X, Y, Z}, an analysis of the logic of the encoder in terms of delay is carried out. The encoder has 2 inputs and 3 outputs as seen in Fig. 4.3.

The main factors that define the delay of each output of the encoder are: the number of logic stages between the input and output, and the delay added by each logic stage. Therefore, the critical path must be detected, and the rest of the paths need to be slowed down artificially in order to match the slowest one. Alternatively, if this is not possible due to technology or complexity issues, then latches or some form of memory logic needs to be implemented along with a clock in order to synchronize all three outputs. The later has the downside of extra logic, extra power to constantly keep the latches on as well as additional complexity with the extra clock input. However, an extra advantage is that the latches can also eliminate any delay between the two input bit-streams, which can prove problematic and will be examined in a following section.

After adding the buffers as seen in Fig. 6.3, we repeated the analysis for sizing multiplier of 0.3 and the results are shown in Fig. 6.5. In the figure, we have a similar setup as we did in the previous experiment with the following alterations. The inverted inputs are no longer shown. The output of each path ({X, Y, Z}) is followed by the output

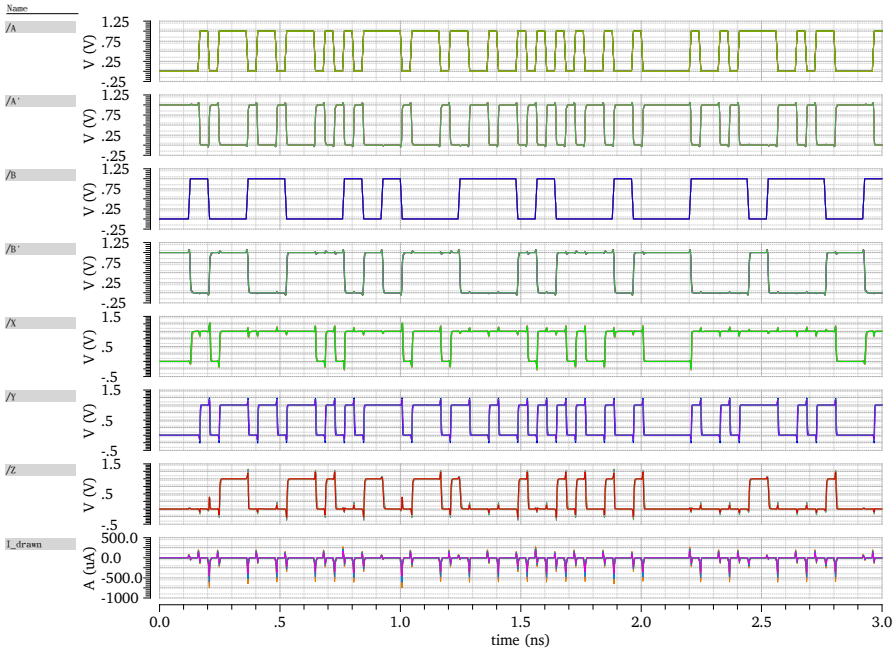


Figure 6.4: Transient plot of the performance of the encoder without latches and output buffers for values of *width multiplier* between 0.3, 1.From top to bottom: the 2 input bit-streams A and B and their inverted counterparts A' and B', the three outputs of the encoder X, Y and Z, and the total instantaneous current drawn by the encoder.

of the buffer following (or loading) that path $\{X\_buff,\ Y\_buff,\ Z\_buff\}$. The current drawn is replaced by the instantaneous power of the encoder cell including the buffers.

In Fig. 6.5, we can see a significant degradation of the rise and fall times of the pulses at the three encoder outputs $\{X,\ Y,\ Z\}$, since they are driving the buffer inverters which are 4 times their size. In order to have proper load in the output of the three buffers, four identical buffers were added to simulate a load 4-times larger effectively giving us the *Fan-out of 4* delay.

In terms of timing delay, we can see from Fig. 6.5 that the three paths are almost concurrent. This can also be verified in Fig. 6.6 where we can observe the timing delay between the paths switching. It is also evident that the spikes in the instantaneous power coincide with the switches of the gate outputs, which is expected since CMOS gates draw the most power when switching.

6.2.4 Synchronous logic

In order to improve the eye opening of the driver, we were required to be able to synchronize the three outputs of the encoder. Therefore, as mentioned earlier in the chapter, D-latches were inserted at the output of the binary to thermometer encoder. The D-latches used in this design are transparent when fed with a high pulse, and maintain their previous value when provided a low pulse in the enable pin. Thus, by timing an externally provided *Clock_enable* signal at the middle of the input pulses, we can guar-

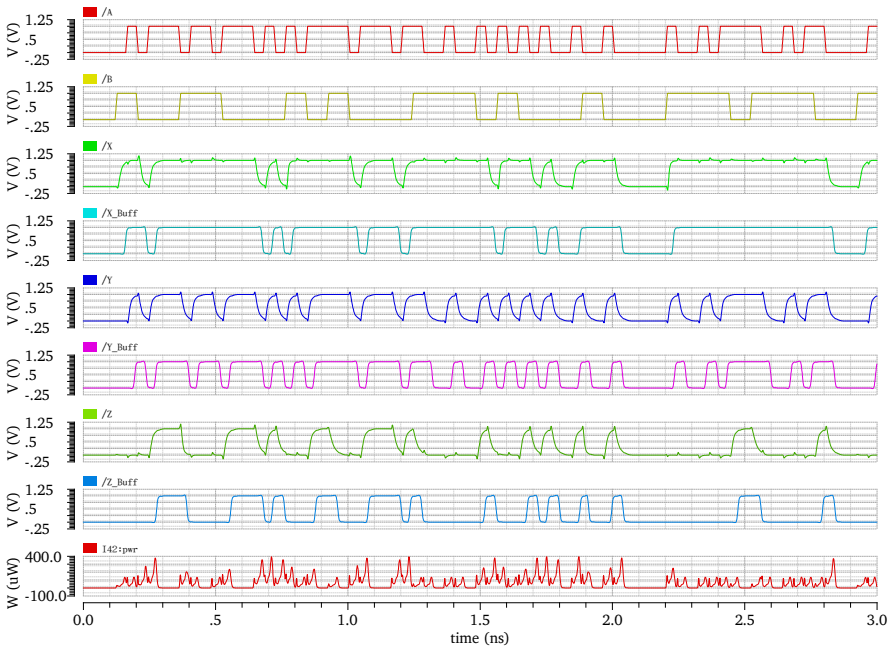


Figure 6.5: Transient plot of the performance of the encoder without including output buffers for *width multiplier* of 0.3. From top to bottom: the 2 input bit-streams A and B, the three outputs of the encoder X, Y and Z along with the respective outputs from the buffers *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous Power drawn by the encoder *I42:pwr* including the buffers.

antee that all 3 outputs of the encoder will have time to settle at the proper value before they are allowed to transition to the buffers. That way, we synchronize the three outputs perfectly, and we can avoid any sort of timing hazards appearing in the gates due to timing mismatch between the inputs A,B as well.

Since this chip is meant as a test setup we have no prior knowledge about whether the final design will be synchronous or asynchronous. Additionally, the clock synchronization with the inputs A,B is very important. In the case where the clock cannot be provided or cannot be accurately timed, the design has the capability of functioning in asynchronous mode as well. This can be done by setting the clock at a logic "1", effectively making the latches transparent. This choice has the side-effect of degrading the eye opening of the driver.

The addition of the latches in the design effectively increased the number of logic gates by $\approx 60\%$. However, the power consumed of the encoder has been shown to be less than 10 fJ/b, thus the power efficiency of the driver has increased only minimally.

6.2.5 Power and Energy measurements

As mentioned in Section 3.2.1, the instantaneous power of the cell does not provide enough information to assess the impact of the encoder in the total *energy efficiency* of the system. The *energy efficiency* is given as the energy spent per unit of information

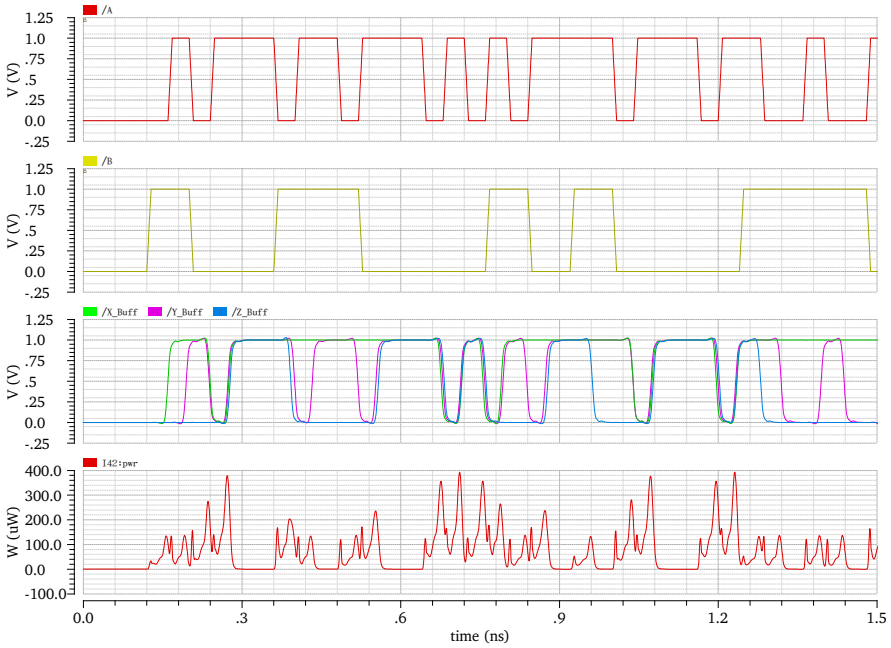


Figure 6.6: Transient plot of the performance of the encoder without including output buffers for *width multiplier* of 0.3. From top to bottom: the 2 input bit-streams *A* and *B*, the three outputs from the buffers *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous Power drawn by the encoder *I42:pwr* including the buffers.

(bit or symbol) while the power given in the figures presented is energy per unit time (second).

In order to calculate the energy of a pulse, two ways were implemented. The first one, was to first take the periodic average of the power per pulse (every 40 ps) and then integrate that power to get the energy per pulse. The second, was the more straightforward way of integrating the instantaneous power of the whole simulation time, and then divide it by the number of pulses existing in that time. The two methods were compared for verification purposes and both produced almost identical results.

Averaged pulse power

Since we have a periodic signal in the input with a period of 40 ps we can average the instantaneous power of the whole simulation time in 40 ps windows in order to estimate the average power of each symbol (see Fig. 6.7).

The resulting average instantaneous power per symbol is shown in Fig. 6.8. We can see in the figure that the average power follows a similar pattern as the one seen in the instantaneous power window in Fig. 6.7. The average power exhibits two peaks around 8 ps and 34 ps. This can be attributed to the fact that CMOS gates consume power while switching and since the input signals have an inherent rise time of ≈ 8 ps the peak power should be around 8 ps and close to 40 ps. The reason that the second peak is shifted towards 34 ps might be the fact that the three different gates have slight timing

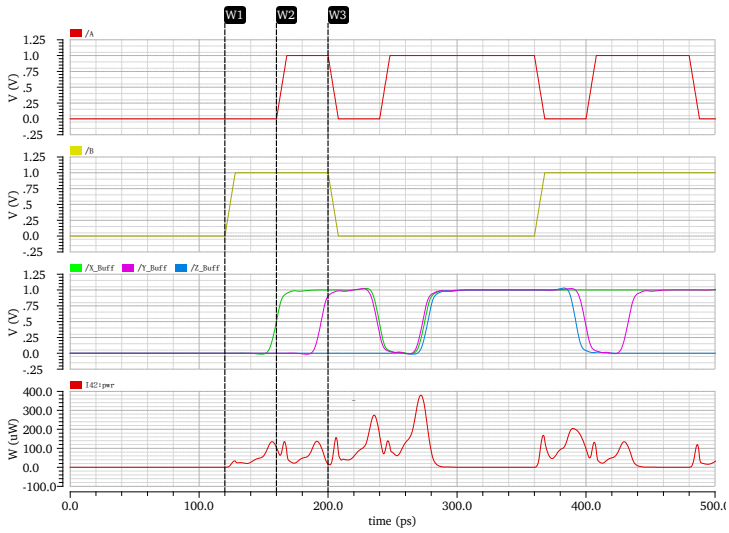


Figure 6.7: Transient plot of the averaging window to calculate the average power per symbol. From top to bottom: the 2 input bit-streams A and B, the three outputs from the buffers *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous power drawn by the encoder *I42:pwr* including the buffers. The three markers represent the the borders between two consecutive windows or symbols.

difference between them which is in the order of a few pico seconds as we saw in Fig. 6.6. Therefore, some of the switching occurs a few ps earlier.

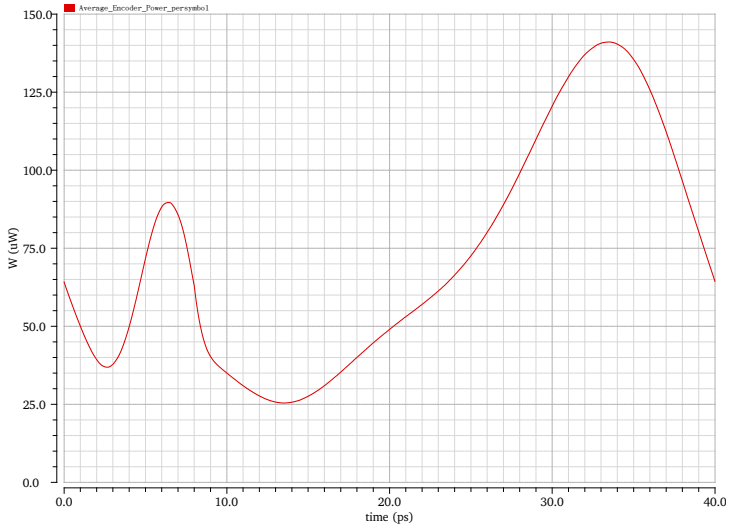


Figure 6.8: Average power per symbol calculated over 3 ns with random input bit streams.

Lastly, when comparing the values of the two methods of energy calculation presented in Section 3.2.1 we obtain almost identical results that verified the measurements.

Sizing effects

The gate sizing has is the major defining factor of the gate current consumption since larger MOS allow more current to go through. Therefore, an analysis of the effects of sizing on power and energy consumption was done. The main incentive is to better quantify the trade-off between energy efficiency (since larger gates are less energy efficient) and the driving potential of the gates (since a wider gate can drive a large load faster).

The transient behavior of the encoder for varying gate sizes is shown in Fig. 6.9. It is evident from the figure that a threefold increase in the gate sizing did not affect the rise and fall times, since all the gates are scaled up equally. However, the gate delay was affected, which again is expected since the gate delay is strongly connected to the capacitances of the gates, which scale up along with the gates.

The most important effect of scaling is that the instantaneous power also increases greatly and at some cases more than 3 times. Since the energy efficiency of the system is a major concern this is an important finding that needs to be taken into account when setting the sizes of the logic.

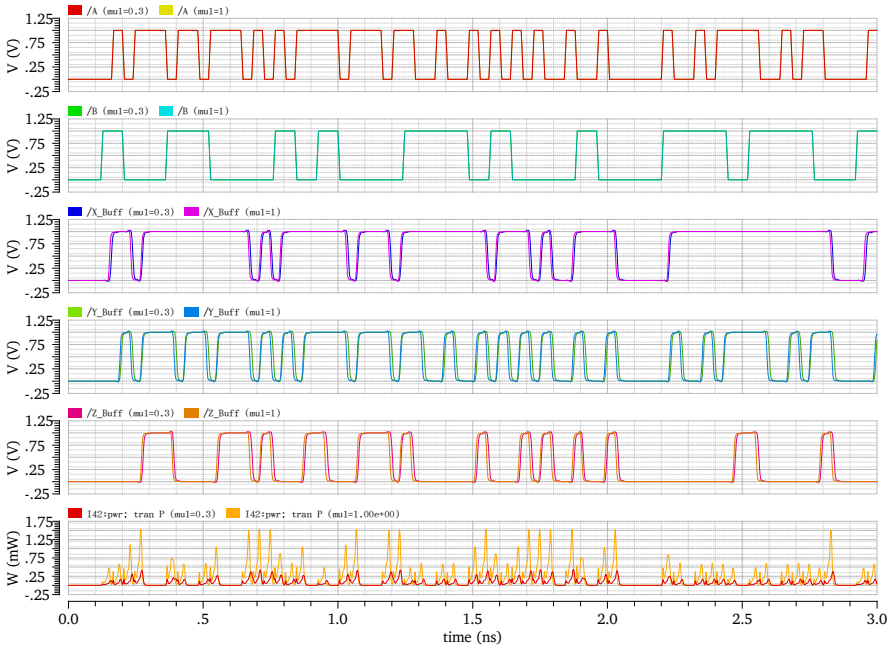
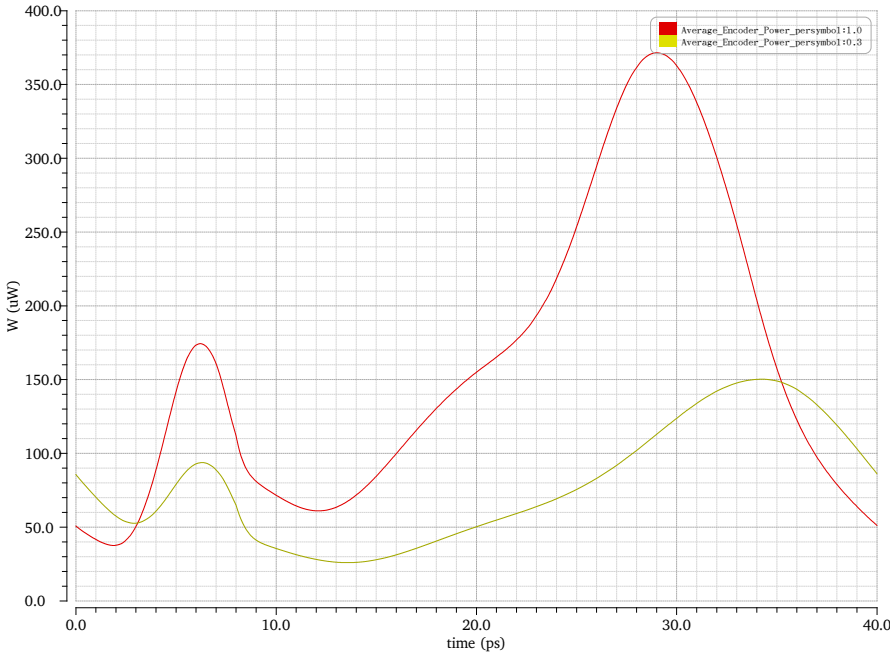
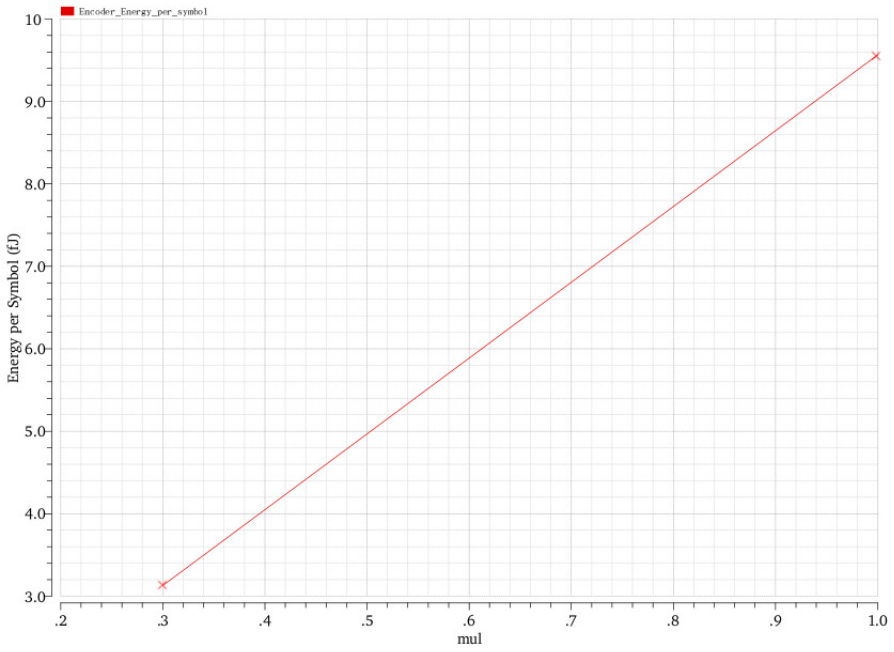


Figure 6.9: Transient plot of the performance of the encoder, including output buffers, for values of *width multiplier* between 0.3, 1. From top to bottom: the 2 input bit-streams A and B , the three outputs of the encoder *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous power of the encoder including the output buffers.

To better assess the effects of size in the energy efficiency, we can look at Fig. 6.10. The average power for width multiplier factor of 1.0 is significantly larger than that for 0.3, which is expected as discussed earlier. Also, we can observe an increased energy per symbol from ≈ 3 fJ per symbol to ≈ 9 fJ per symbol.



(a) [Instantaneous power of a single symbol averaged.] (40 ps) averaged over the total simulation time.



(b) Energy efficiency in fJ per symbol.

Figure 6.10: Average power and energy per symbol of the encoder for values of width multiplier of {0.3, 1.0}

Delay effects

As mentioned earlier, the delay between the two input bit-streams can be detrimental for the driver's performance. The delay gives rise to glitches or timing hazards since the three paths of the encoder do not switch concurrently. Despite the fact that with larger delay between the inputs the instantaneous power might seem to drop, that does not apply to the average power. The transient behavior of the encoder, including the output buffers, is shown in Fig. 6.11. The delay between the two inputs only affects paths X and Z since Y is only dependent on input A. Furthermore, it is evident from the figure that the delay only affects some transitions, namely those that are triggered by both inputs changing at the same time.

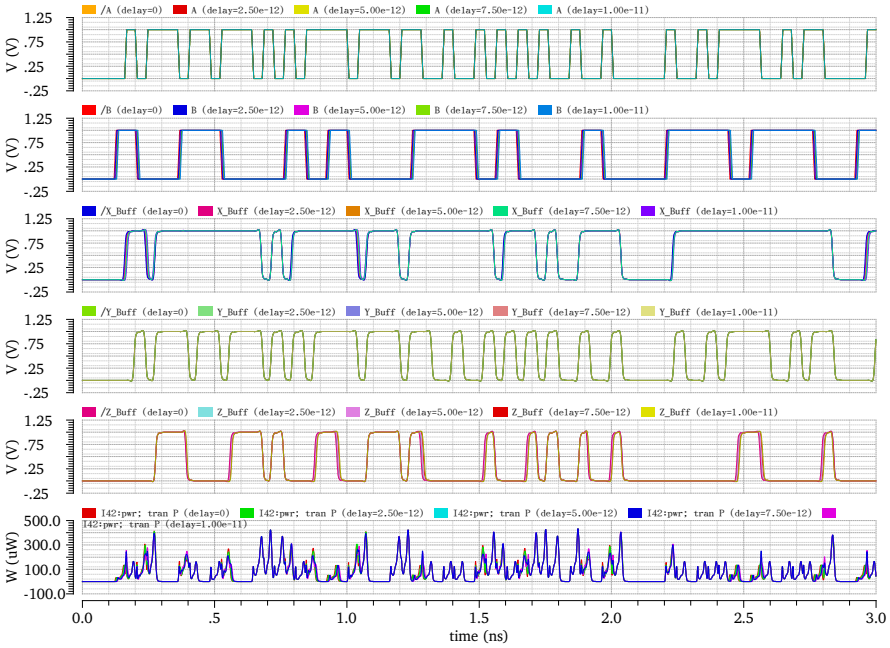
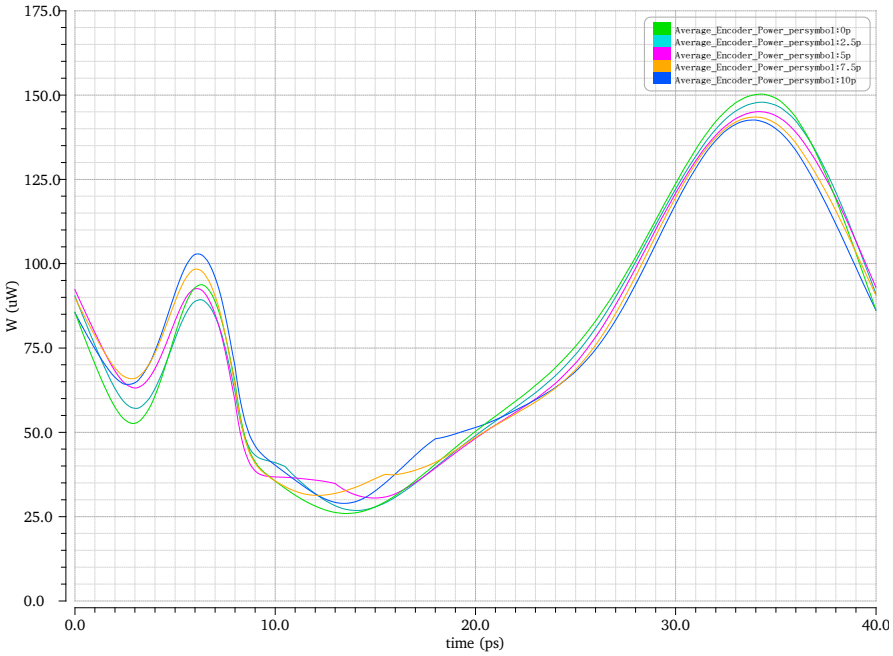


Figure 6.11: Transient plot of the performance of the encoder including output buffers for *width multiplier* of 0.3 and delay between the inputs of 0p - 11p. From top to bottom: the 2 input bit-streams A and B, the three outputs of the encoder X, Y and Z along with the respective outputs from the buffers *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous power drawn by the encoder *I42:pwr* including the buffers.

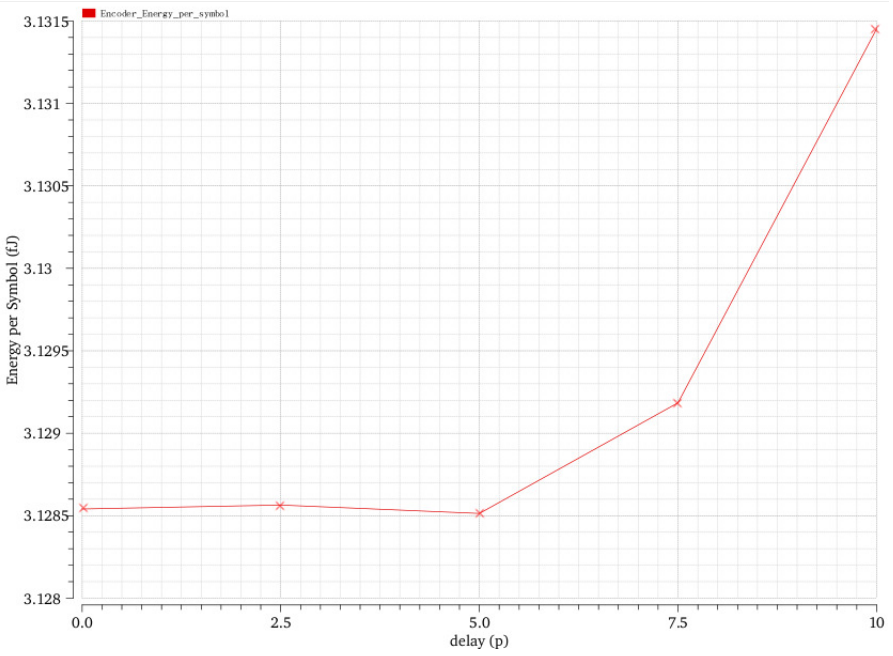
The effects of the delay in the energy and power consumption are shown in Fig. 6.12. We can see that in the case of the averaged power per symbol in Fig. 6.12a, the differences in peak power values for different delays are in the order of a few μW. However, as we can tell from Fig. 6.12b, there seems to be a very slight increase in the energy per symbol of the encoder for higher delay times, but it is in the order of 0.01%.

Even though the delay does not have a big impact in the energy efficiency of the encoder, it is expected to affect the output of the driver slices more and subsequently in the total BER of the system.

The analysis performed above takes into account normal values of delay between the



(a) Instantaneous power of a single symbol (40 ps) averaged over the total simulation time .



(b) Energy efficiency in fJ per symbol.

Figure 6.12: Average power and energy per symbol of the encoder for delay times {0 ps - 10ps} for width multiplier of 0.3.

gates, that is delay that does not exceed a quarter of the pulse time. In order to get a better idea of the system limitations, a similar analysis was also performed for delay times up to 20 ps. The transient plot of the parametric analysis is shown in Fig. 6.13 and the energy per symbol in Fig. 6.14. The scaling factor was also set to 1 in order to allow the encoder to drive the output stage better, effectively minimizing the effects of the gate load on the delay times.

From Fig. 6.13, we can see that the increased delay is affecting X and Z to the point where the output starts to produce errors either by omitting transitions or introducing glitches, where there shouldn't be any. Also, from Fig. 6.14, we can observe that the increased delay is also affecting the energy efficiency. For values of delay ranging from 10 ps up to 20 ps, the energy per symbol has increased by roughly 0.5%. It must be noted, however, that in a real system there should not be such high delay times between the two inputs.

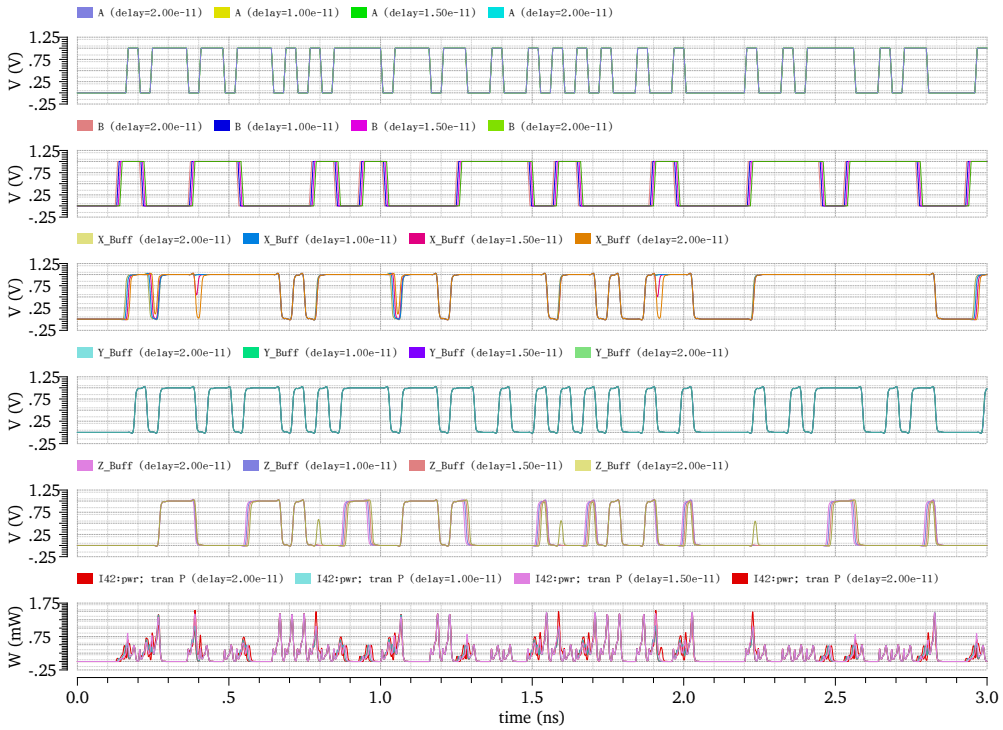


Figure 6.13: Transient plot of the performance of the encoder including output buffers for *width multiplier* of 1.0 and delay between the inputs of 10p - 20p. From top to bottom: the 2 input bit-streams A and B, the three outputs from the buffers *X_buff*, *Y_buff* and *Z_buff*, and the instantaneous Power drawn by the encoder *I42:pwr* including the buffers.

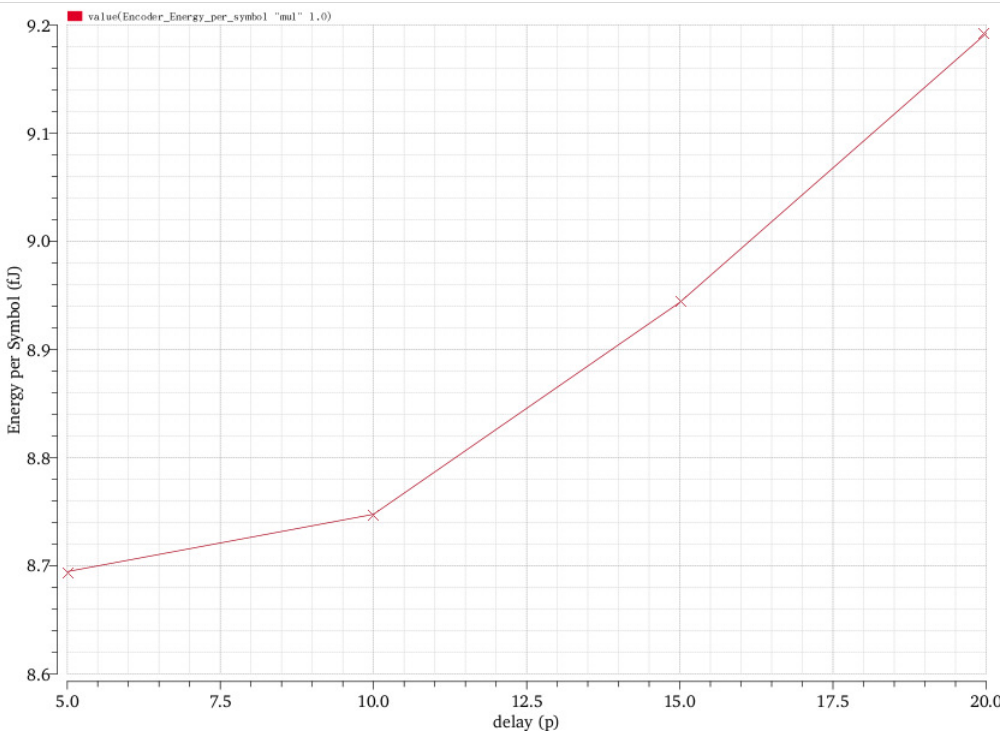


Figure 6.14: Energy efficiency in fJ per symbol for delay times {10 ps - 20ps} for width multiplier of 1.0.

6.3 Driver Slices

As mentioned in Section 6.1.2, the driver slices can be designed by using either the nominal NMOS devices or by using a mix of normal and lvt devices.

In the current implementation, the latter was used in order to focus on the performance of the driver slices. However, if the final device meets the performance requirements by a large margin, then the first choice might be implemented to further enhance the system's energy efficiency.

The test setup of the driver slice is shown in Fig.6.15, where: V_{sw} controls the level shifting from the pre driver stage to the main driver stage, V_b controls the bias current level, V_{in} is the input bit stream at 25 GHz, and V_{out} is the output voltage towards the VCSEL load. For the transistors:

N_{input} : is the input transistor of the pre-drive stage.

N_{swing} : is the transistor that controls the level shift from V_{in} to V_x by changing the current through it, controlled by V_{sw}.

N_{drive} : is the output stage of the driver that is connected to the VCSEL via wire bonds.

N_{mod} : is the transistor that draws the modulation current, based on V_x.

N_{bias} : is the device that controls the bias current, dependent on V_b.

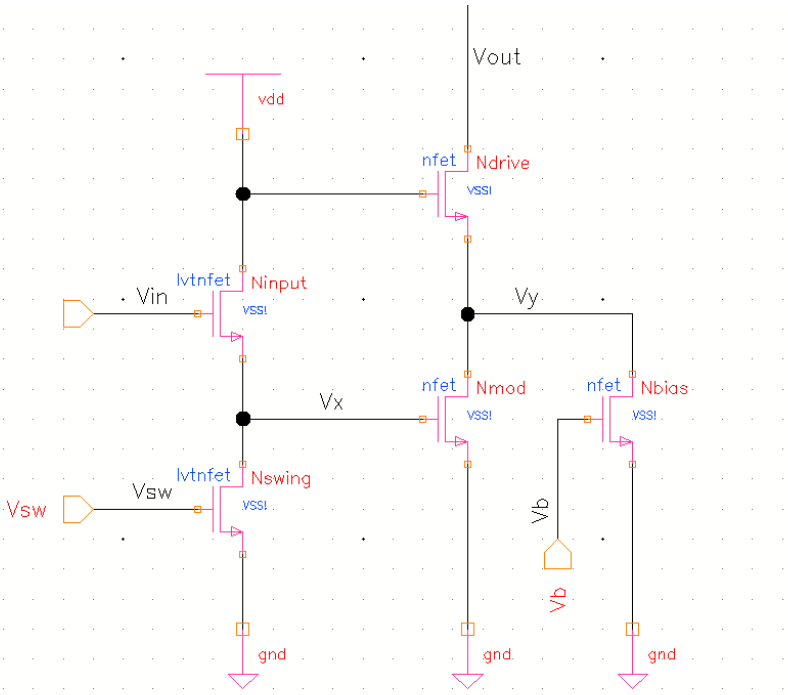


Figure 6.15: Schematic of the test implementation of the driver slice on Cadence ADS.

As is apparent, there is a vast design space to be explored. Therefore, in order to make progress in the design, the sizes of all the transistors are initially set to the nominal size (as discussed in Section 6.1.1 above). Then, we progressively make adjustments to the design until the intended functionality has been achieved. During this process, the following values were considered static:

- V_{dd} was set to 1 V.
- The main driver was biased through the VCSEL load by a voltage V_{bb}: $\approx$ 5 V minus the voltage drop due to the diode junction.
- The input V_{in} has a voltage swing equal to V_{dd} and a frequency of 25 GHz. The rise and fall times were considered equal at 8 ps.

Based on these assumptions, a series of parametric simulations were made in order to quantify the effects of various variables to the performance of the driver. The variables under test included: V_{sw}, V_b, the width of N_{drive} transistor, and the width of the N_{mod} transistor. The simulation results followed a similar method to the one described in Section 6.2.5 for measuring the energy per symbol.

6.3.1 V_b effects

Since the VCSEL requires a constant minimum bias current in order to remain above the threshold, the first benchmark of the driver is to be able to supply that current. The

V_b input is used to set this bias current by controlling the saturation current of N_{bias}. The results of a parametric simulation for values of V_b ={0.4, 0.5, 0.6 } and constant V_{sw} = 0.1 V are shown in Fig. 6.16 and Fig. 6.17. In Fig. 6.16 we can see from top to bottom: V_{in}, I_{swing}, V_x,V_y, V_{out},I_{bias}, $I_{modulation}$ and I_{driver} for variable bias control voltages. We can see that the higher values of V_b affect the bias current I_{bias} as well as the total current of the driver I_{driver}. Additionally the voltage V_y of the node connected to the drains of the bias and modulation transistors also follows a descending course for increasing values of the bias current since the higher current through the node induces a voltage drop on that node in accordance to Kirchhoff law. A similar but less prominent effect appears at the output voltage of the driver slice V_{out}. In Fig. 6.17 we can see the relationship of the energy efficiency of a single drive slice with higher bias currents. It is apparent that for bias current values of 0.25, 1.0 and 1.75 mA the energy per symbol increases by around 20% between each step.

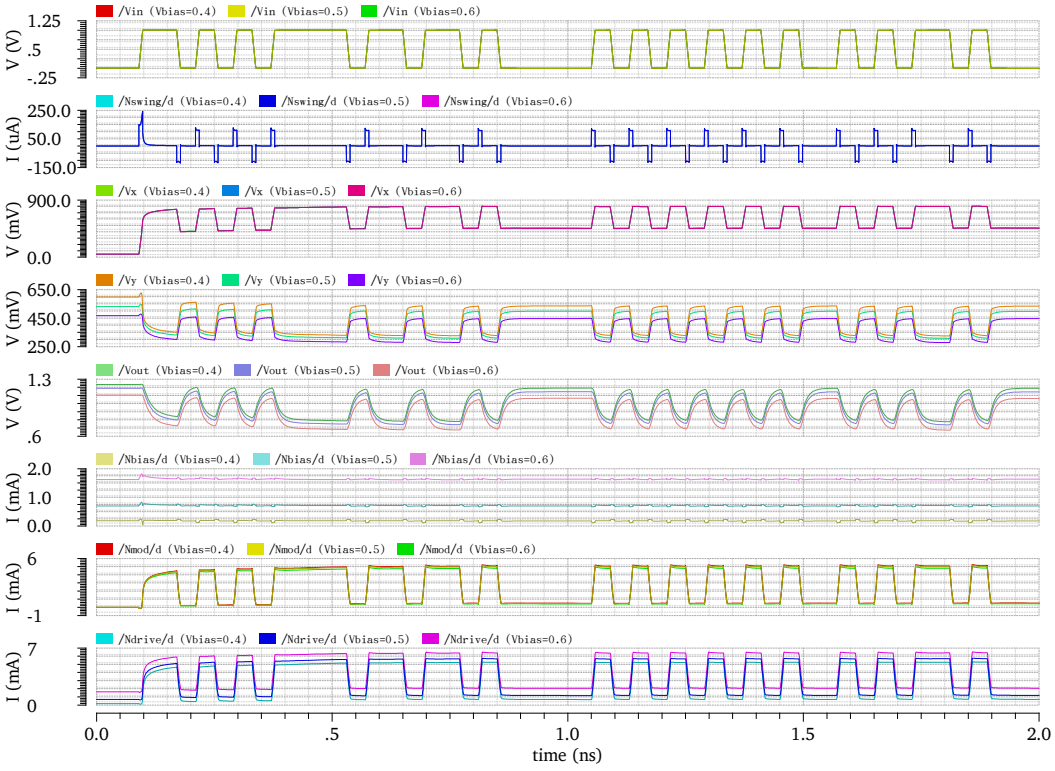


Figure 6.16: Transient performance of the driver slice for various values of V_{bias}. From top to bottom: V_{in}, I_{swing}, V_x, V_y, V_{out}, I_{bias}, $I_{modulation}$, I_{driver}.

6.3.2 V_{sw} effects

In a similar fashion, the effects of the output swing control voltage V_{sw} are investigated and presented in Fig. 6.18 and Fig. 6.19. In Fig. 6.18, we can observe that the increase of V_{sw} causes a decrease in the output current swing at the drain of the driver, shown

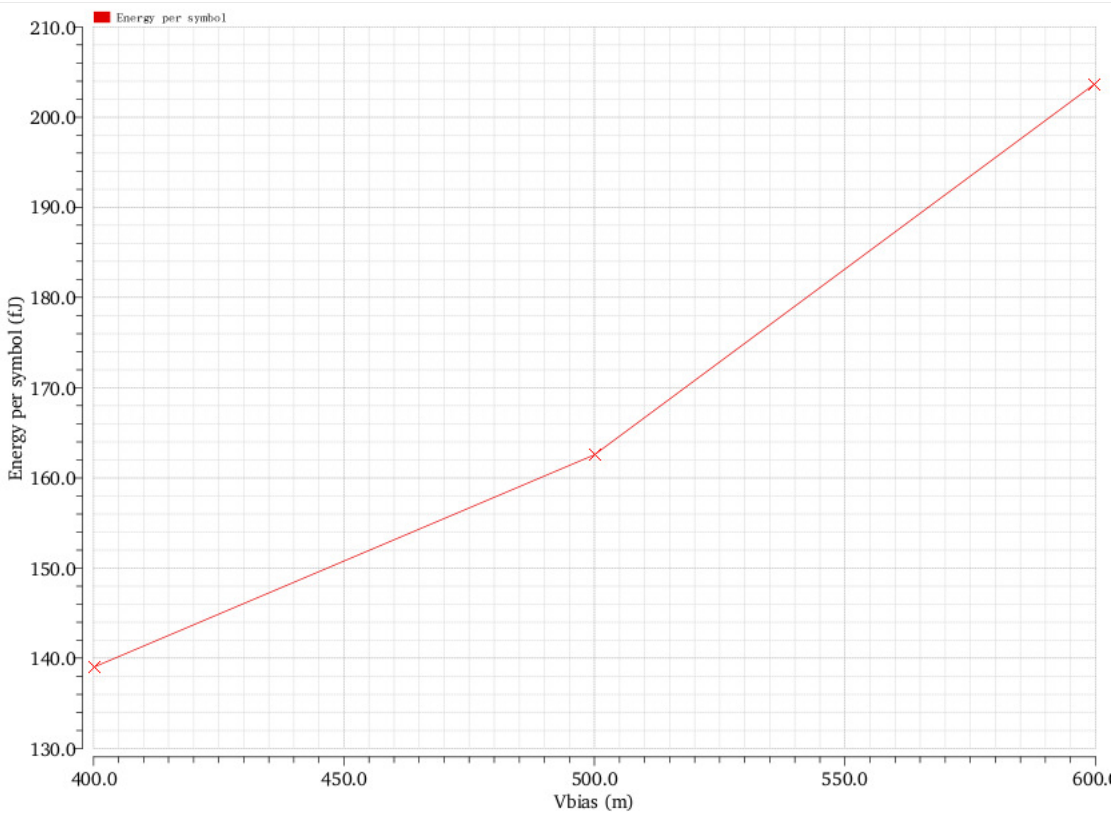


Figure 6.17: Energy efficiency in fJ per symbol of a driver slice for values of V_{bias}={0.4, 0.5, 0.6 }.

as N_{driver}/d. As discussed in the introduction of Section 6.3, this is expected since the increased current through the swing control transistor N_{swing} causes the voltage on its drain, marked as V_x, to drop which limits the current of the modulating transistor N_{mod}. Additionally, we can see that small increase in the values of V_{sw} introduce a large increase in the current through the pre-drive stage. This current is effectively an overhead since it does not directly contribute to the driving of the VCSEL load, and therefore it must be minimised. So a small value of V_{sw} is preferable in order to maintain the energy efficient aspect of the design. Even though this contradicts the earlier insights presented in Section 5.1.2, there is a valid reasoning for that disparity. A larger output swing should in theory account for more power and effectively for less power efficiency. However, an increase of V_{sw}, increases the current I_{sw} more than it increases I_{mod}, so in effect we expend more current in the level-shifter stage of the driver than we are actually gaining in the output. This can be attributed to the behavior of the *lvt* devices which have a large saturation current slope (large dependence on their V_{ds}). Additionally, the increased modulation current should account for larger expense in power if we took the power dissipated on the VCSEL into account in the measurements. However, in this design, as it is customary in literature, we consider them separately.

Despite the relatively large output current swing (N_{driver}/d) variations for values of

V_{sw} between 0.1 and 0.3 we can see that the current that is dissipated on the pre-driving stage is relatively low compared to the 0.4 case. This is because the transistor N_{swing} is approaching its saturation region which increases its current. Therefore, in order to minimise the energy wasted in the pre-driving stage we need to ensure that N_{swing} is biased in its linear region of operation.

The above can also be verified by looking at Fig. 6.19, which depicts the energy per symbol dissipated in total by the driver slice. As we can see, by changing the bias of the gate of transistor N_{swing} from the 0.3 V point up to 0.4 V we have an increase in the energy per symbol of about 15% without any significant increase in the output current swing. This leads to the conclusion that this increase in energy is practically overhead. On the contrary, by selecting a smaller V_{sw} at 0.1, we have a 30% increase in the energy per symbol, however this is accompanied by an almost zero N_{swing}/d current and a 60% increase in the modulation current from 3 mA to 5 mA.

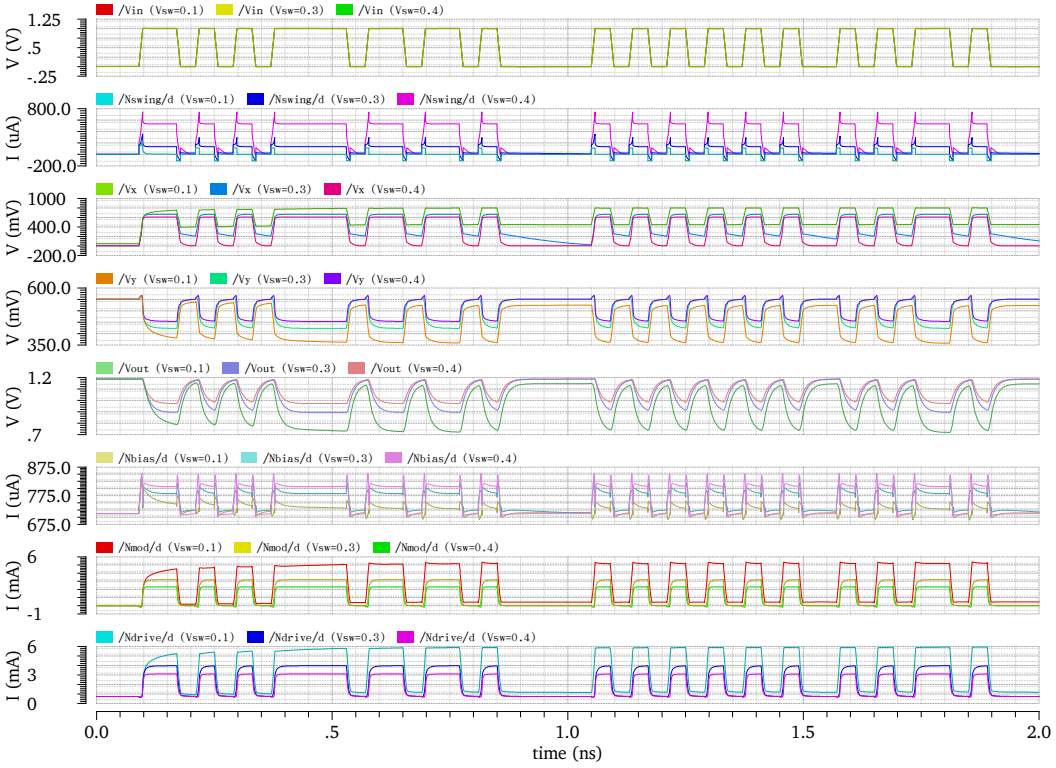


Figure 6.18: Transient performance of the driver slice for various values of V_{sw}. From top to bottom: V_{in}, I_{swing}, V_x, V_y, V_{out}, I_{bias}, $I_{modulation}$, I_{driver}.

6.3.3 Output Voltage swing

In order to properly design the driver we need to take into account the output voltage swing caused by the high currents involved.

The main issues that impose a limitation on the maximum current of the driver are

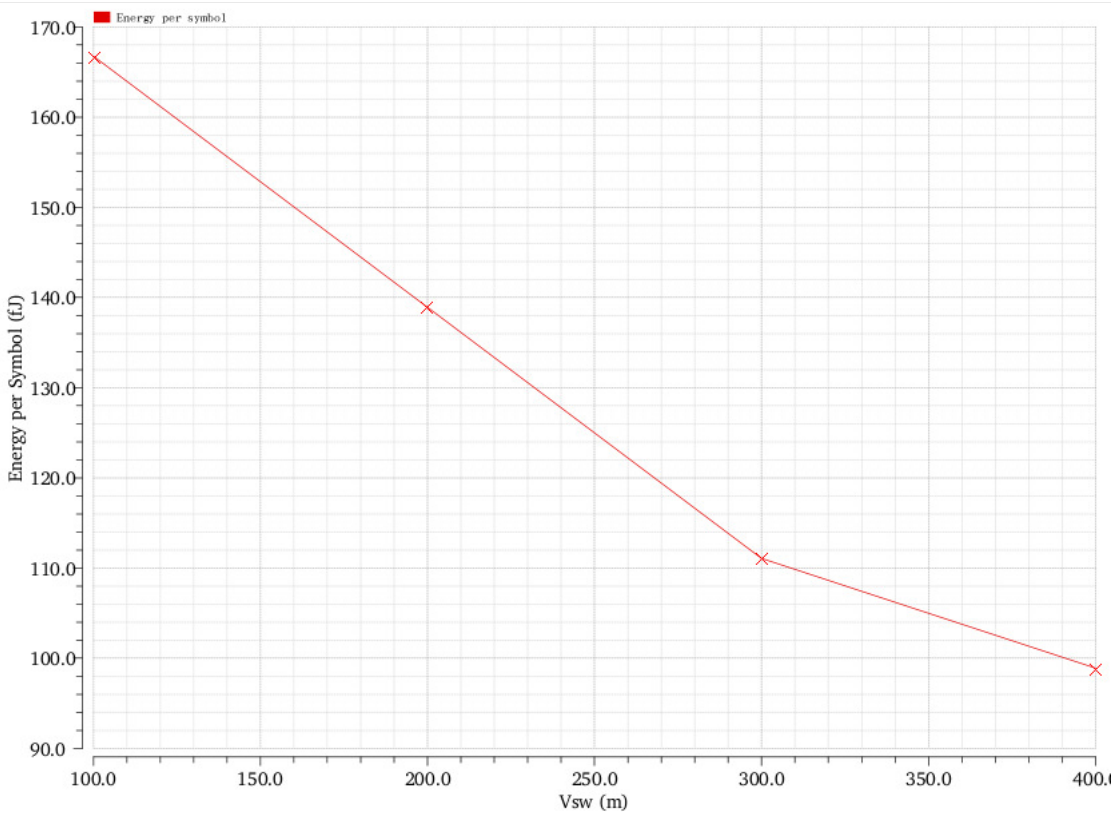


Figure 6.19: Energy efficiency in fJ per symbol for different values of V_{sw}.

two. Firstly, the slope efficiency of the VCSEL that indicates how the optical power relates to the bias current is not linear (as presented in Fig. 2.3b). At high modulation currents (above 15 mA), the optical power per mA drops. Thus, in order for the eye diagram to be translated from the driving current to the optical power accurately, we need to make adjustments so that the highest step of modulation current is higher than the other two. That way we can compensate for the lower optical power. Secondly, the VCSEL's small signal resistance changes both with the frequency of modulation as well as with the bias current. For higher currents, the VCSEL exhibits higher voltage drop across the junction (as seen in Fig. 2.3a). Effectively, when the third driver slice switches on (the other two were already on) it experiences a larger ohmic load, and, consequently, a lower voltage at the output. However, since the main driver stage is biased through the VCSEL, and we have the limitation to maintain both transistors of that stage in saturation, we need to have adequate voltage at the output. That voltage in practice is ≈ 0.6 Volts at minimum.

7

Results and Discussion

In this chapter we present the final results of the project along with their discussion.

7.1 Driver Schematic

The final driver design is shown in Fig. 7.1. It includes the three driver slices with their three control voltages V_{bias},V_{swing} and V_{body} together with the pre-driving buffers. The Binary to thermometer Grey encoder along with three transparent D-latches which are meant to synchronize the three outputs of the encoder to minimise jitter, when their *Enable* is "1". The *Vdd* and *Gnd* pins have been omitted to reduce clutter in the schematic from all the above blocks.

7.1.1 Modes of operation

The driver circuit can operate in two modes, *Asynchronous* by setting the *Clock_Enable* input to logic "1" and *Synchronous* mode by applying a 25 GHz clock signal with $25-50\%$ duty cycle in that input. The main difference is that in *Synchronous* mode the latches only update their values on the rising edge of the clock effectively ignoring any output jitter between the X,Y,Z outputs of the encoder and any jitter introduced by the input bit-streams. The *Asynchronous* mode is intended for applications when the clock cannot be supplied or the x-axis eye opening is not of critical importance.

7.1.2 Operation characteristics

The driver operates at an internal V_{dd} voltage of 1 V with a 10% margin and simulations have shown it can function up to a frequency of 40 GHz without any severe degradation of its performance. The high frequency results are presented in Appendix D.1.

The two inputs A and B are expected to have a rate of 25 Gbps each for a total driver baud-rate of 50 Gbps at 25 GHz 4-PAM. The inputs can have rise and fall times

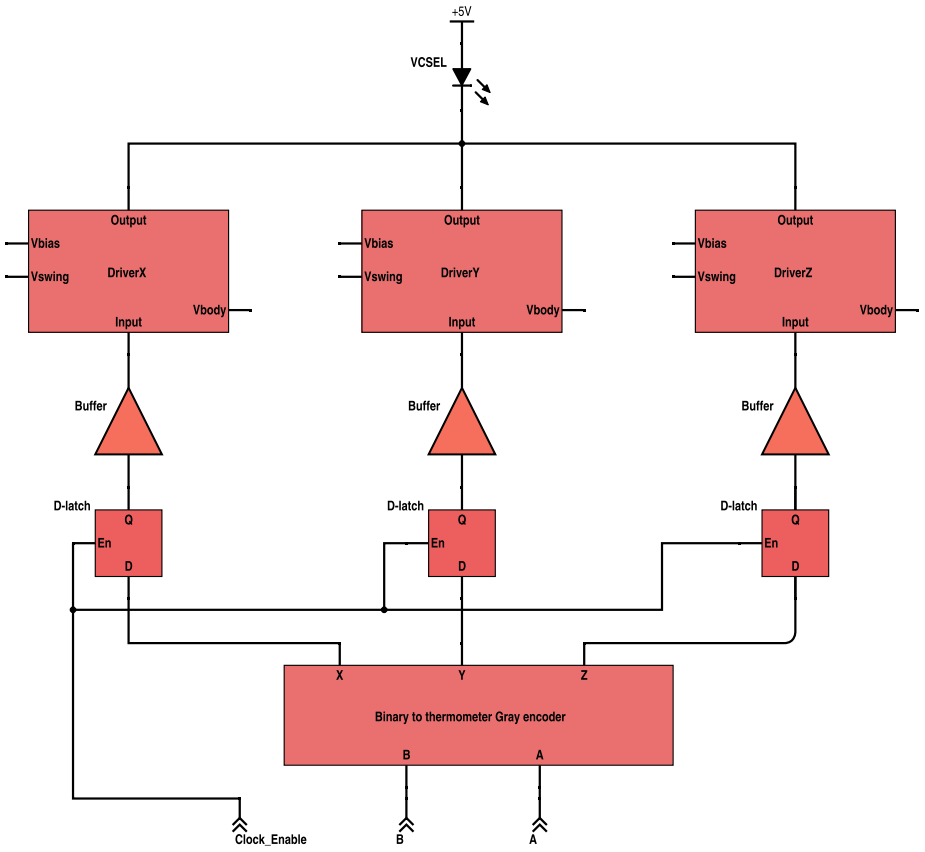


Figure 7.1: Block diagram of the final driver layout. The V_{dd} and Gnd on each block are implied and were left out of the schematic for clarity reasons.

up to $8 - 10$ ps (that accounts for 20%-25% of the pulse) without affecting the system's behavior.

The *Clock_Enable* signal however, that is meant to serve as a clock to allow for the Synchronous mode of the driver, should be kept at a maximum of $4 - 8$ ps rise and fall times in order to not affect the operation of the system.

The V_{body} that controls the body bias can be set to any voltage between 1 to 3 V and it increases the output bias and modulation current of the driver significantly.

7.1.3 Supply voltages

As it is already mentioned, the device requires a multitude of different voltages in order to operate. Typically, in low power designs the existence of multiple voltage domains is seen as a disadvantage. Which is natural since the stages responsible of generating these voltages need to be implemented as well, and they consume additional power. In the current design, the voltages that are strictly required were originally the V_{dd} voltage of 1 V, which could also be applied as forward body bias, and the VCSEL bias voltage

$V_{b,vcsel}$ of 5 V. The two additional voltages that were introduced, V_{bias} and V_{swing}, were added as a means to adapt the design in different test scenarios in order to fulfill its purpose as a test setup. Lastly, the body biasV_{body} of 1 to 3 V was also required in order to improve on the performance of the design.

Even though the driver is designed with energy efficiency in mind, the energy that will be consumed by these voltages (as well as the inputs) is not taken into account in this study. Rather, it is assumed that the supply voltages, the input bit-streams, and the clock will be supplied externally to the circuit.

In a future design when the driver could potentially be optimized for a specific VCSEL, the voltage generation would have to be done on chip, but the control voltages would not be necessary since their purpose is to make the device configurable. However, the body bias would have to be supplied externally or generated on the chip, but it has the benefit of not contributing to any currents, therefore, not consuming any power other than that of the electronics meant to handle or generate it.

7.1.4 Control voltages and Energy efficiency

The control voltage limitations for the two voltages V_{bias} and V_{swing} are shown in Table 7.1 along with the respective energy efficiency values for both modes of operation.

Table 7.1: Energy efficiency and average power values on the control voltage limits for V_{sw} and V_{bias} and for $V_{body} = 3$ V.

Vsw [mV]	*Vbias [mV]*	*Energy Efficiency [pJ/b]*		*Average Power [mW]*	
		Synchronous	*Asynchronous*	*Synchronous*	*Asynchronous*
450	600	0.256	0.257	11.67	11.86
650	450	0.268	0.278	13.11	13.48
450	450	0.236	0.242	12.90	12.89
650	600	0.297	0.301	14.86	15.02

The results in Table 7.1 are taken for Body bias Voltage of 3 V with a VCSEL model as the load and without taking the wire-bond interconnects into account. The power values are exclusively for the driver and do not include the VCSEL power dissipation. The decrease in energy efficiency for higher V_{sw} has to do with the way the level shifter works. A higher V_{sw} control voltage decreases the voltage of the main driving stage of the driver slices by increasing the current in the pre-driving stage which is essentially wasted current. Thus, for higher swing control voltage we obtain less modulation current and more wasted internal current.

The decrease in energy efficiency for higher V_{bias} voltages is mainly attributed to the higher bias current of the VCSEL which drives the average power of the system up.

The Synchronous mode provides only a slight improvement in energy efficiency by decreasing the time the D-Latches are kept on, effectively reducing the static power of the three latches. However this change is not substantial enough, so we can assume that the final device has roughly the same energy efficiency in both modes of operation.

Lastly, the current levels produced for the four control corners and the two extreme body bias limits, are presented in Table 7.2. The table also includes the extinction ratios for those bias and modulation currents. However, the extinction ratio is limited to the current through the VCSEL as mentioned in Section 3.2.2.

Table 7.2: Bias and peak currents and extinction ratio for the four control corners and two body bias limits.

V_{sw} [mV]	V_{bias} [mV]	$V_{body} = 3$ V			$V_{body} = 1$ V		
		I_{bias} [mA]	I_{peak} [mA]	r_e [dB]	I_{bias} [mA]	I_{peak} [mA]	r_e [dB]
450	450	1.5	16.8	10.5	1	8.8	9.4
650	450	1.5	14	9.7	1	5.6	7.5
450	600	5	17.8	5.5	4.4	10.8	3.9
650	600	5	16	5.1	4.4	7.9	2.5

7.2 Result comparisons

The driver design needs to be compared to both the benchmarked values of the 65 nm design presented in Chapter 5 as well as with other Laser driver circuits presented in literature.

7.2.1 Comparison between 28 and 65 nm simulations

When comparing the above results with the ones presented in Chapter 5 we can make the following observations.

The control voltage margins have changed which is attributed to the scaling down of the channel size. More specifically the short channel behavior of the 28 nm devices imposes much more strict limitations on the range of the control voltages as well as a higher threshold voltage which must be surpassed in order for the driver transistors to remain in saturation.

In terms of performance, as expected the 28 nm driver could outperform the 65 nm one without the need of bandwidth extending techniques. In fact the 28 nm driver design could perform equally well up to 40 GHz -a value $\approx 30\%$ higher than the requirements- and the reason it could not go higher is mainly due to the bandwidth limitations of the VCSEL diode and the wire-bond interconnects.

As for the power efficiency, we can clearly see by comparing Tables 5.1 and 7.1 that the 28 nm driver is twice as power efficient at the lowest modulation current and at least 3 times more efficient for high modulation currents.

It should be noted that since the layout has not be done and LVS could not be performed in neither of the designs, the real results might differ slightly from the ones presented above. The accuracy of the simulations were the best that the simulator could provide without the layout extracted parasitics. The measure of how well those

results depict reality only depends on the underlying design of the simulator and the device models. However, even in the case were the simulator has an accuracy of 20% the resulting driver still exhibits double the energy efficiency of the original 65 nm design that served as an inspiration [11], and more than 8 times more energy efficient than [48].

7.2.2 Comparison with literature

For a fair comparison with the other drivers presented in literature we would ideally need to have the layout simulations available. The main reasoning is that only after the layout parasitics have been taken into account we can have a realistic view on the designs performance. Additionally the layout can give us the total area of the driver chip which is accountable for the cost of the fabrication.

A comparison with other PAM drivers presented in the previous years is shown in Table 7.3.

Table 7.3: Comparison of PAM driver circuits found in literature with the proposed device.

Source	*Bitrate [Gbps]*	*Baudrate [GHz]*	*Technology (CMOS)*	*Supply Voltage [V]*	*Power Consumption [mW]*	*Energy Efficiency [pJ/b]*
[49]	25	12.5	90nm	1.0	99.3	3.97
[16]	20	10	180nm	1.8	252	4.5
[11]	56	28	65nm	1.2	32	0.56
[48]	56	28	130nm BI-CMOS	2.3 & 3.0	55.8	2.05
This work	50	25	28nm FDSOI	1.0 & 5.0	13	0.24

In Table 7.3 at the current work row, the voltage describes both the V_{dd} required within the chip as well as the VCSEL bias voltage. Additionally the 3 control voltages discussed in earlier sections are not mentioned here since they do not contribute in the power consumption.

Even though the layout design was not carried out, an assessment of the area of the chip could be made. By using the 65 nm design as a basis we could assume that the 28 nm chip would occupy approximately half as much silicon real estate. Additionally, since we did not implement the SPI interface that was used in [11] we would expect to conserve more area. In addition to that, that driver included very large inductors to improve the bandwidth so more silicon area could be saved since that was not needed in the 28 nm design. However, since we have no accurate knowledge about the layout specifications of the 65 nm, we cannot conclude if the total area was limited by the actual driver or by the pitch of the I/O pins.

7.2.3 Eye diagrams

In order to better assess the performance of the driver we will provide the eye patterns (as discussed in Section 3.2.3) of the 3 control voltages V_{bias}, V_{sw} and V_{body} for Synchronous

(*Clock 0*) and Asynchronous (*Clock 1*) modes. The minimum and maximum values for the body bias V_{body} are set to 1 and 3 V respectively. The resulting eye diagrams for the Asynchronous mode are shown in Fig. 7.2 and for the Synchronous in Fig. 7.2.

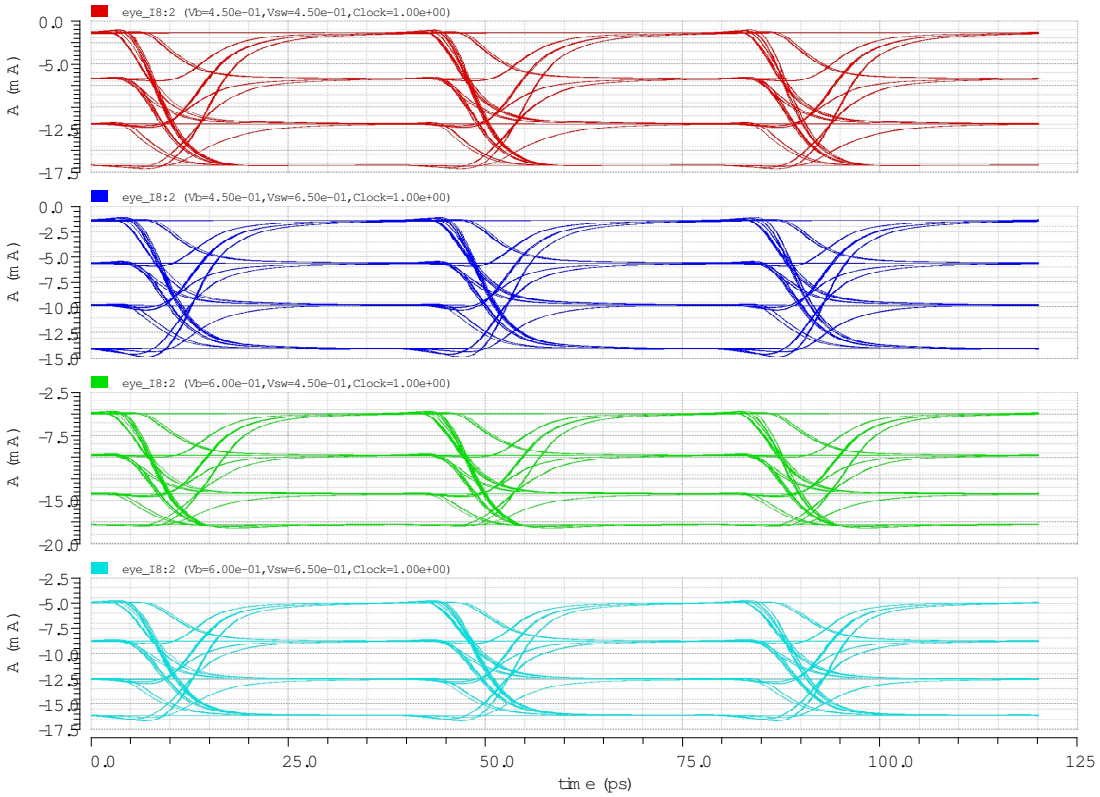


Figure 7.2: Eye diagrams in Asynchronous mode for the extreme corners for the control voltages V_{bias}, V_{sw} and $V_{body} = 3$ V. The graphs are from top to bottom: Red: $V_{bias} = 450\ mV$, $V_{sw} = 450\ mV$, Blue: $V_{bias} = 450\ mV$, $V_{sw} = 650\ mV$, Green: $V_{bias} = 600\ mV$, $V_{sw} = 450\ mV$, Cyan: $V_{bias} = 600\ mV$, $V_{sw} = 650\ mV$

As we can see in Fig. 7.2 for values of the bias control voltage $V_b = \{450\ mV, 600\ mV\}$ allows to set the bias current I_{bias} from ≈ 1.5 mA up to ≈ 5 mA. Similarly, for the values of the modulation control voltage $V_{sw} = \{450\ mV, 600\ mV\}$, we obtain a modulation step I_{mod} between 4 mA and 5 mA.

The slope efficiency of the laser however drops above 15 mA and its dynamic resistance increases. This is shown in Fig. 7.2 as the "closing" of the eye pattern at high modulation currents, which is most prominent in the 3^{rd} case (green).

Given that the slope efficiency of the VCSEL diode starts to drop above 15 mA of bias current we consider that 1 mA of margin in the modulation of a single driver slice is enough to account for that non-linearity. Thus setting the third driver slice to provide more current by adjusting the V_{sw} to a slightly lower value than the other two driver slices can equalize the three eye patterns.

In Fig. 7.3 we can see similar effects as in the previous figure but we can also observe substantially larger eye openings in the time axis. This is gained by the D-latches that

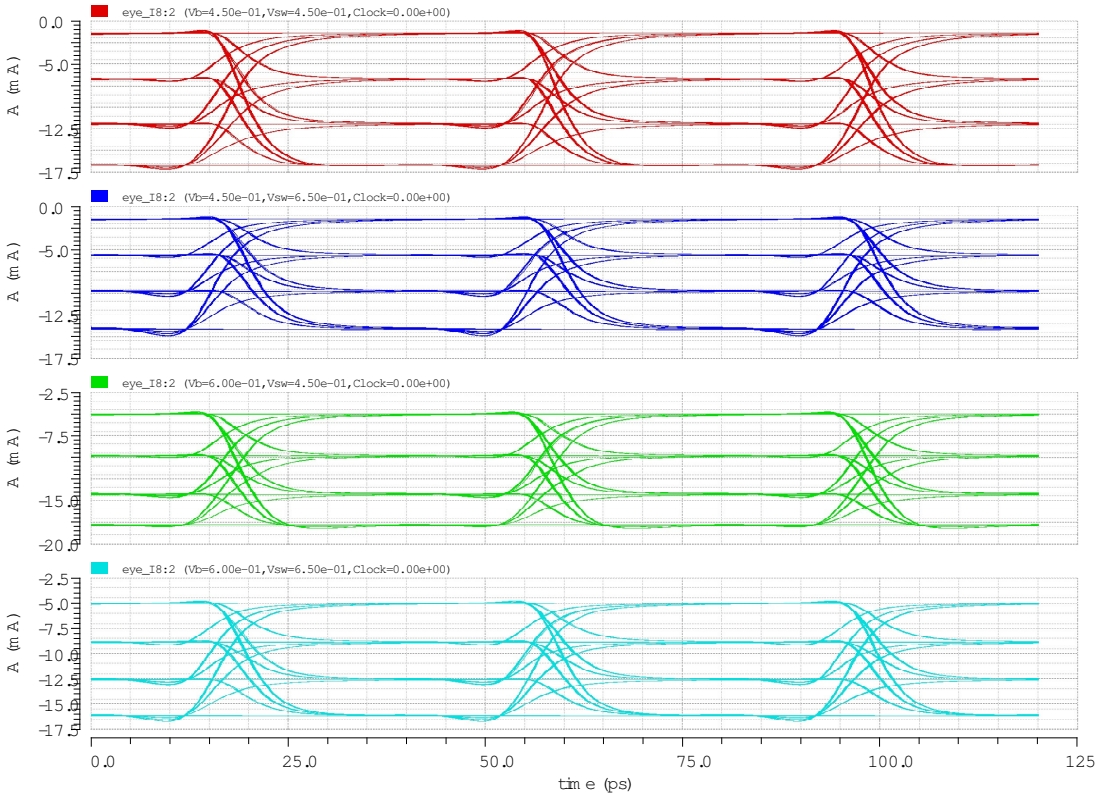


Figure 7.3: Eye diagrams in Synchronous mode for the extreme corners for the control voltages V_{bias}, V_{sw} and $V_{body} = 3$ V. The graphs are from top to bottom: Red: $V_{bias} = 450\ mV$, $V_{sw} = 450\ mV$, Blue: $V_{bias} = 450\ mV$, $V_{sw} = 650\ mV$, Green: $V_{bias} = 600\ mV$, $V_{sw} = 450\ mV$, Cyan: $V_{bias} = 600\ mV$, $V_{sw} = 650\ mV$

synchronize the inputs in the three driver slices, effectively minimizing timing glitches between the three output current driver stages. In the same fashion as in the Asynchronous case the higher bias current limits the allowable modulation current effectively squeezing the third Eye opening.

In order to have a complete view of the system's behavior we also present the eye patterns for the corner values of V_{bias}, V_{sw} and for $V_{body} = 1$ V. The results are shown in Fig. 7.4.

7.2.4 Output voltage swing

As discussed in Section 6.3.3, the driver must be able to provide stable current ideally the same on all 3 PAM steps above the bias current. Even though an ideal current source should provide a constant current independent by any voltage variations in the output, the realistic devices cannot operate in such a wide voltage range unaffected. Especially since the nominal V_{ds} that a 28 nm device can handle is around the 1 V regime due to the thin oxide.

From Ohm's law we can estimate that the voltage drop across the laser diode for

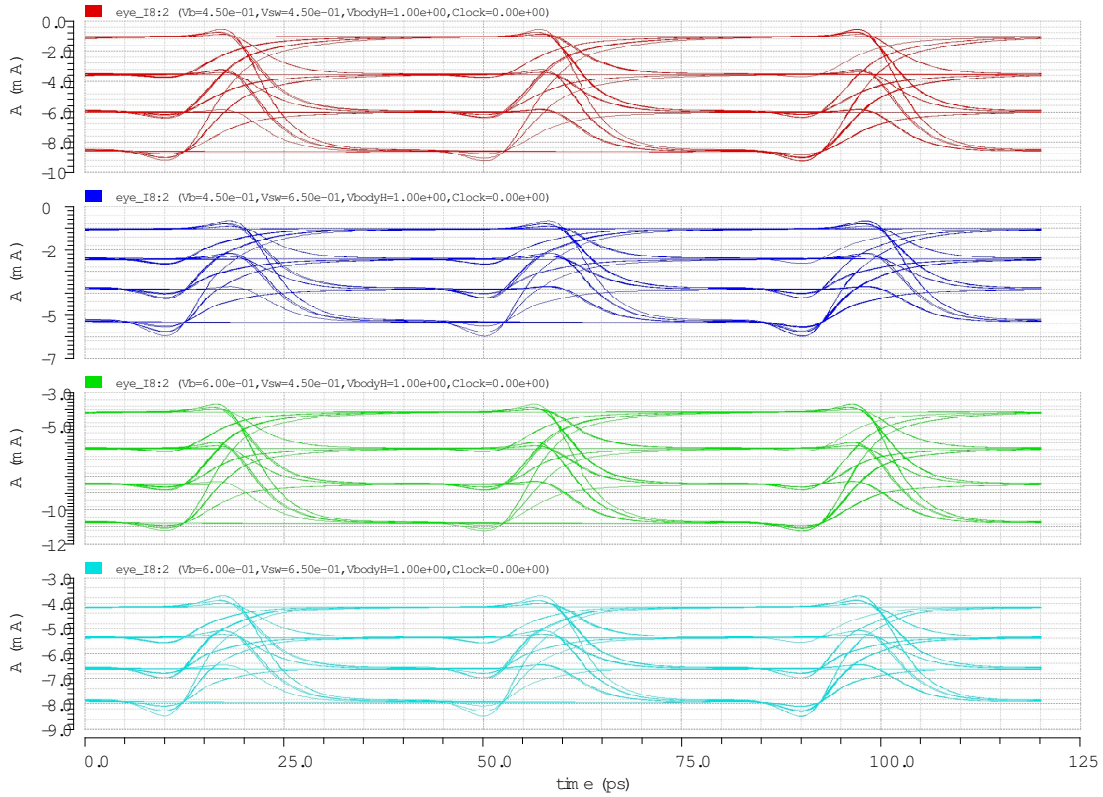


Figure 7.4: Eye diagrams in Synchronous mode for the extreme corners for the control voltages V_{bias}, V_{sw} and $V_{body} = 1$ V. The graphs are from top to bottom: Red: $V_{bias} = 450\ mV$, $V_{sw} = 450\ mV$, Blue: $V_{bias} = 450\ mV$, $V_{sw} = 650\ mV$, Green: $V_{bias} = 600\ mV$, $V_{sw} = 450\ mV$, Cyan: $V_{bias} = 600\ mV$, $V_{sw} = 650\ mV$

$R_{vcsel} \approx 90\ \Omega$ and a current in the range {1.5 mA , 17 mA} gives us a total voltage swing in the output between {0.135 V, 1.530 V}. This can also be verified by looking in Fig 2.3a. In order to maintain a minimum 0.6 Volts in the output of the driver as discussed in Section 6.3.3, one must increase the total bias voltage of the VCSEL. However during low current operation when the minimum voltage drop will occur at the VCSEL the bias voltage will be too high for the driver to handle safely.

So the upper limitation on the current through the VCSEL is two-fold. The inherent slope efficiency of the VCSEL is dropping and the voltage drop across the VCSEL diode itself reduces the bias voltage of the driver too much.

Therefore the modulation current has been limited at a maximum of 5 mA so in total with the bias current the VCSEL will not operate at currents higher than 17 mA.

7.3 Wire-bonds

As discussed in Section 5.1.3 the load is very important to the performance of the driver chip. In order to properly characterise the driver by taking the load into account, equiv-

alent models of both the VCSEL and the wire-bond interconnects were used. The wire-bond load exhibited inductive behavior that was related to its length and it was based on inductance values for typical 1 mil thick, golden wire-bonds used in industry. It also includes a model of the bond pad capacitance, and a small resistance that corresponds to the radiative resistance at the frequencies of interest.

The best way to assess the effect of the interconnects on the performance of the system is to repeat the eye diagram simulations for various lengths of the wires.

7.3.1 Energy efficiency

The energy efficiency simulations with and without wire-bonds are presented in Table 7.4. As we can see in the table the two methods of calculating the energy efficiency presented in Section 3.2.1 give almost identical results. We can also see that the energy per bit of the VCSEL is three times larger than that of the driver, which can be attributed on the fact that the Rms bias current that the VCSEL experiences is quite high for a total modulation current of $17mA$. The energy efficiency is clearly not affected by the wire-bonds, which is expected since the wire-bond resistance is negligible, so there is no ohmic loss over the wires.

Table 7.4: Energy efficiency values for the two modes of operation (synchronous and asynchronous) with and without wire-bonds. The control voltages were $V_{bias} = 0.45$ V, $V_{sw} = 0.45$ V and $V_{body} = 3$ V. The η_{avg} refers to the values calculated with the averaging window discussed in Section 6.2.5.

	Clock mode	η *[pJ/bit]*	η_{avg} *[pJ/bit]*	η_{VCSEL} *[pJ/bit]*
500 μm Wirebond	Synchronous (0)	0.237	0.237	0.700
	Asynchronous (1)	0.241	0.244	0.743
No Wirebond	Synchronous (0)	0.234	0.234	0.700
	Asynchronous (1)	0.237	0.240	0.745

7.3.2 Wire effects in performance

Since the wire-bonds do not affect the energy efficiency we proceed to assess their impact in the performance of the driver. The most straightforward way to examine the multitude of effects that the wires can have we have to look at the eye openings both in the x (time) and the y (current) axes. The results of the eye pattern simulations are shown in Table 7.5.

As we can see in Table 7.5, the existence of a 500μm wire has detrimental effects in the minimum eye opening at the x-axis. That translates into less noise margin, which could lead in higher BER (bit error rates) in the receiver. The RMS current through the VCSEL diode is largely unaffected despite the introduction of a wire-bond however we can also see that the Eye opening in the y-axis becomes smaller. That means that the rise and fall times of the symbols become larger or the jitter between different transitions becomes larger.

Table 7.5: Eye diagram simulations for the two modes of operation (synchronous and asynchronous) with and without wire-bonds. The $I_{mod,min}$ and $I_{mod,avg}$ refer to the minimum and average eye opening in the y-axis of the diagram.

	Clock mode	$I_{bias,rms}$ *[mA]*	*Eye Opening [ps]*	$I_{mod,avg}$ *[mA]*	$I_{mod,min}$ *[mA]*
500 μm Wirebond	Synchronous (0)	10.25	30.4	4.72	3.09
	Asynchronous (1)	10.68	25.9	4.67	3.13
No Wirebond	Synchronous (0)	10.30	33	5.38	5.00
	Asynchronous (1)	10.80	28	5.26	4.93

7.3.3 Effects of wire inductance on eye opening

These issues can be attributed in the L-C behavior that is formed between the capacitive bond pad, the strongly inductive wire and the capacitive load (the VCSEL). Essentially a C-L-C circuit forms which oscillates at a specific frequency close to the frequency of the system. In order to verify this theory, we proceed to make similar simulations for various lengths of the wire-bonds, which will give us different values of inductance, effectively moving the oscillation frequency away from the 25 GHz frequency of the system.

The results of that simulation are shown in Table 7.6. It is evident from the simulation data, that the wire inductance increases linearly with the wire length (as it was set in this model of the wire-bond). As the wire inductance increases, the horizontal eye opening increases, until it starts to drop again somewhere between 500 – 1000 μm. We can also see that the synchronous mode highly suppresses the effect of the wire inductance, so we can assume that the main source of the eye opening reduction is increased jitter since the synchronous mode mainly corrects the misalignment between the outputs.

Table 7.6: Eye opening versus wire-bond lengths between {125 μm – 1000 μm } for the two modes of operation.

WB length [μm]	*WB Inductance [pH]*	*Eye Opening [ps]*	
		Asynchronous	*Synchronous*
125	82.5	20.3	23.5
250	165	24.1	30.4
500	330	25.9	30.5
1000	660	23.3	28.8

In order to better visualize the dependence of the horizontal eye opening on the wire-bond inductance, we have presented the above results in a graph seen in Fig. 7.5.

As we can see in Fig. 7.5, the eye opening does not change dramatically between 300 and 700 μm. This behavior is due to the oscillations caused by the LC circuit. Since there is no resistive component in the wire the oscillation remains at a great extend under-

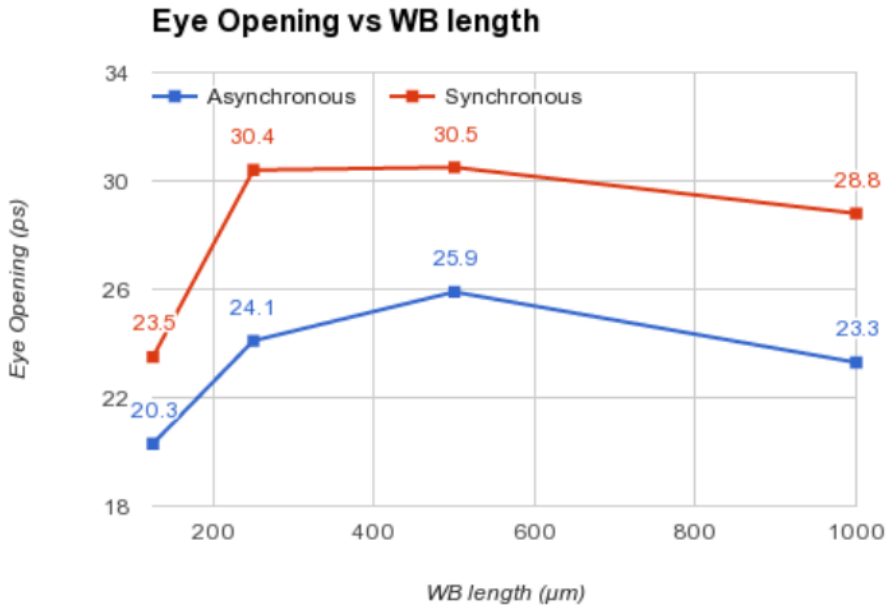


Figure 7.5: Eye opening vs wire-bond inductance for synchronous and asynchronous mode.

dumped. Thus, the leading cause of that, has to do with inter-symbol interference. Some particular transitions of the PAM are more sensitive to those oscillations.

7.3.4 Eye diagram of various wire-bond lengths

Also, the difference that occurs at a specific range of wire lengths, seems to be purely dependent on the frequency of oscillation. In order to verify that, we perform similar eye pattern simulations as before, but this time at several wire-bond lengths. From the resulting simulated data presented in Fig. 7.6 and Fig. 7.7, we can clearly see the difference that the various bond wire lengths make to the output current of the driver.

As is apparent from the figures, the most intact eye diagram occurs for wire length of 500 μm for both modes. Even though the one at 1000 μm is decent in terms of the vertical opening, it has worse x-axis opening due to the rise and fall times becoming drawn out.

In practice, the inductance of the real wire might vary, as well as the driver's output impedance. That is the main reasoning behind having E/M simulations in the time plan, together with the parasitic extraction from the chip layout. However, due to the high load and ambitious nature of the project there was not enough time to perform these steps.

7.4 Method of Work

The methodology in terms of planing and organization that used in this project was a mix between the traditional linear project planning and a more agile approach inspired by

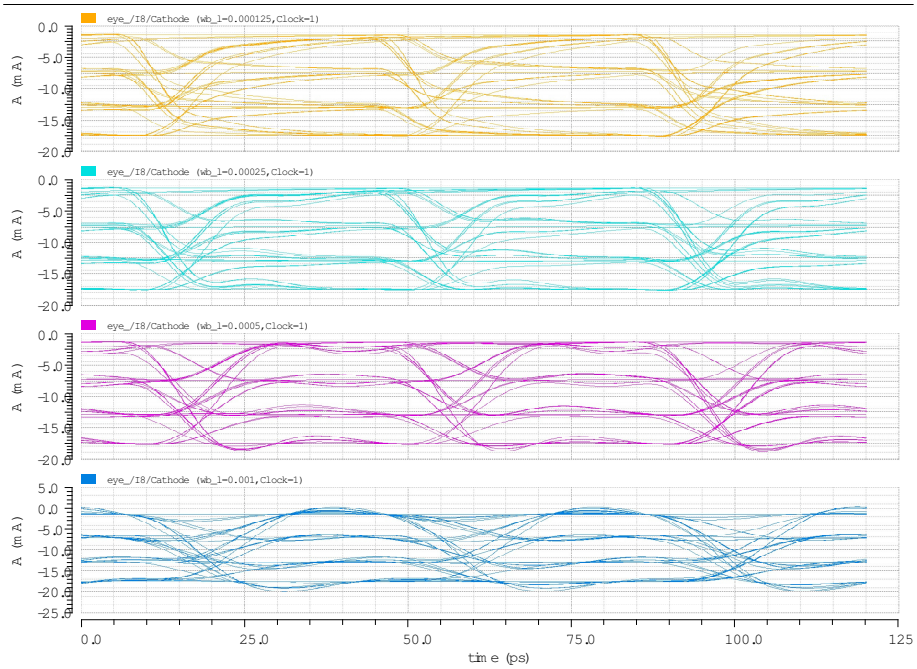


Figure 7.6: Eye diagrams in Asynchronous mode for various lengths of the wire-bonds.

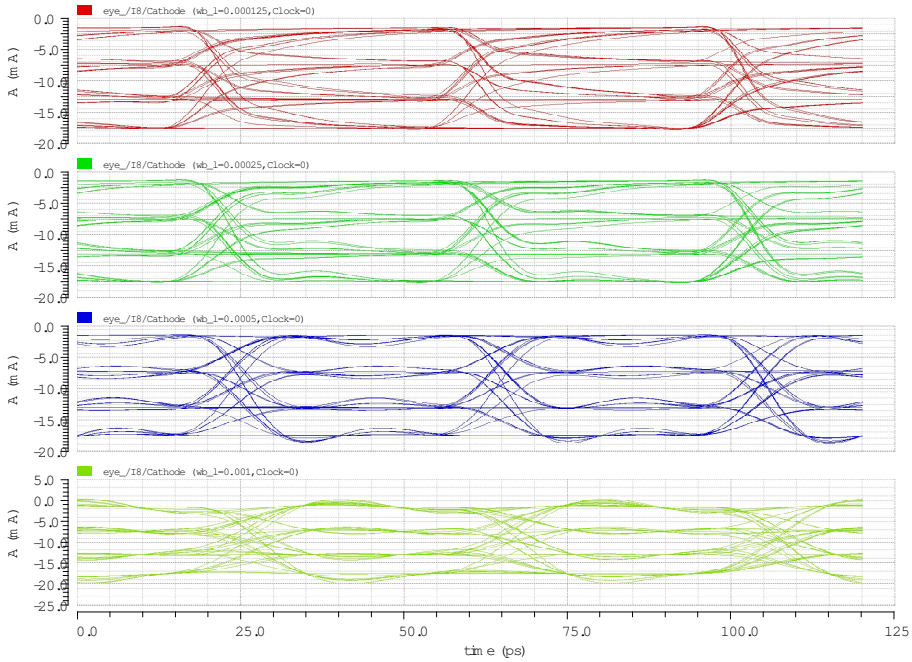


Figure 7.7: Eye diagrams in Synchronous mode for various lengths of the wire-bonds.

the agile methodologies currently in use in industry. The task breakdown was discussed in Section 3.3 and the time-plan is presented in Appendix E.

7.4.1 Plan fulfillment

According to the plan, the layout design, Layout vs Schematic verification, parasitic extraction and E/M characterisation were supposed to be completed.

However, as presented in the risk analysis in the *project planning* document, one of the major risks involving design using the new design kit is to not have access on the software tools.

The access to the 28 nm design kit, and all of it's documentation were not available until after half-way into the project. This setback delayed the whole design process significantly, since in order to perform the layout, the schematic had to be completed, which was dependent on simulations. Even though extended simulations and characterisations of the loads and the driver, as well as preliminary documentation, were carried out in the first part of the project, any real progress in the design was halted.

Additionally, due to the substantial differences of the behavior of the 28 nm devices, the circuit design took significantly longer than it was originally planned.

The energy and performance simulations were carried out, but without taking into account the on-chip parasitics that required the layout to be already in place.

The impedance characterisation of the loads (VCSEL and wire-bonds), was also able to be carried out on model-level while the 28 nm design was on hold. So the driver was completed and characterised and with a good idea of the interconnect limitation thanks to the extended load characterisation and modeling.

7.4.2 Agile methodology

The project was ambitious to begin with, since it had little tolerance to delays in its critical parts, and was tightly planned in terms of time.

In terms of the agile vs linear project methodology, we can argue that in this specific project it was the linear dependencies between the 28 nm tool availability, design, layout and parasitic extraction that actually posed the most important obstacle. Had those steps been independent then the layout could have been completed in the time alloted for this project.

Specifically, the agile execution of the documentation, load characterisation and impedance calculation when we were waiting for the 28 nm design kit to become functional was a major positive factor. If those had not been done ahead of time there would be little or no time to adequately test the resulting driver circuit.

Overall, undertaking such a project with this mix of Agile and Linear planning was an interesting venture which could have been easier if the Linear tasks were not so tightly dependent to each other.

8

Conclusion

In this work, the design of a power efficient laser driver circuit is presented. The completed design process from the literature review to the final driver schematic characterisation is documented. The driver designed in the 28 nm FD SOI technology was compared to a similar implementation in 65 nm. The 28 nm design was expected to outperform the 65 nm one simply due to technology scaling both in terms of power consumption as well as performance.

The final results surpassed the requirements by a good margin exhibiting a doubling in performance as well as half the energy spent per bit. The proposed 28 nm driver achieved almost 0.25 pJ/b energy efficiency at a 50 Gbps bit-rate by using PAM-4. The driver was intended to be used as a test setup for research in optimizing the power efficiency of optical links and therefore was made with versatility in mind. Thus, two modes of operation, Synchronous and Asynchronous, were implemented. Furthermore, means to adjust the bias current and the modulation current were provided as the three control voltages V_{bias}, V_{swing} and V_{body}.

Additional steps were taken to make the integration of the chip with the VCSEL as seamless as possible. That was done by modeling the complex load together with the wire-bond parasitics and using those models to make the driver able to compensate for the effects of the load in the driver performance.

The driver exhibited a significant improvement over the driver circuits presented in literature, however, the energy efficiency and performance simulation results did not include post-layout parasitics, which are expected to negatively affect the performance. This can be mainly attributed to the low power consumption and high performance traits that are inherent in the 28 nm FDSOI process. An additional factor was the power efficient PAM design, that was based on the driver that inspired this project. The above reasons allowed for the creation a driver circuit that could potentially outperform most existing driver chips without the need of extra design measures such as inductive peaking or equalization.

Since this work did not include any models of the transfer medium and the receiver, comprehensive conclusions regarding the power and BER of the complete link could not

be drawn. Additionally, most modern electronic driver chips for laser communications include means of error correction and equalization which are not included in this study. The necessity of those measures might be required in this driver in order to achieve an error free link, however there is no way to verify the BER due to the transmitter system without knowledge of the receiver and the link.

The integration-aware way of design allowed us to compensate for the interconnect effects on the signal integrity during the early steps of the process. However, it also bears the risk of making the driver circuit too specific which could potentially take away some of the versatility of a test setup.

High performance short haul optical data links are the main driving force behind the research of directly modulated VCSELs. However, as power consumption becomes an increasing concern there is a need for novel, high performance and energy efficient data links. Thus, the proposed driver aims to fulfill that niche and help push the research in the field of CMOS laser driver circuits further.

As the design presented is not ready for fabrication, the first future steps would be to proceed with the layout design and verification. Based on the insights we obtained during this study, the on chip parasitics should be important but not be detrimental to the performance of the driver. Additional variability tests will also be necessary, however since the main driver stage of the chip is composed solely by N-MOS transistors the design corners will only affect the encoding logic stage. After the fabrication of the chip is completed, various experimental setups could be devised to test both the potential of the driver as well as the VCSEL. Due to the versatility provided by the chip, by utilizing the control voltages, the driver could be adapted to be used in different link scenarios and even different VCSEL diodes. Furthermore, the driver also demonstrated in the simulations that can perform up to a frequency of 40 GHz which would also allow for a faster VCSEL to be used potentially driving the baud-rate up to 80 Gbps.

In terms of expanding or improving the driver design, the most straightforward steps would be to implement alternative topologies in the driving stages in order to identify the best way to drive the VCSEL diode load. Additionally, on a link perspective, error correction or equalization could be included in order to minimise the BER if the eye opening presented in this report gets degraded by the transfer medium and noise. These stages however, would definitely have a negative impact in the energy efficiency achieved, but will help decrease the bit error rate.

In conclusion, in this report we have demonstrated a PAM-4 laser driver circuit based on an existing architecture, implemented in a the 28 nm FD-SOI process. The models of the interconnects and the VCSEL diode provided insight on the scattering parameters that the signal will experience from the driver to the load and allowed to better assess the complete system performance. Simulated values revealed significant advantages by transferring the driver into the new technology node including a doubling of the energy efficiency while maintaining the bit-rate. The great improvement in energy efficiency motivate the next steps which would be the fabrication and testing of the driver chip.

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A

Calculations

A.1 Source follower stage sizing

In the source follower we have two transistors *M1* and *M2*. The purpose of this stage is to follow the input voltage *Vin* but with a reduced voltage swing *Vx*. Essentially this is a level shifter stage with a voltage gain less than 1. The voltage gain can be controlled by the gate of the second transistor. By increasing the gate voltage, the current *Isw* through node *X* increases as well, effectively reducing the voltage *Vx*. For greater control over that behavior we would want *M2* to be ideally in the linear region of operation, in which case it would behave as a voltage controlled resistor.

A.1.1 Linear

Given that the bias voltage *Vdd* at 1.0 V and the transistor threshold voltages *Vt1, Vt2* at ≈ 0.40 V the equations to be fulfilled for the two transistors *M1* and *M2* to be in saturation and triode regions respectively are as follows: For saturation:

$$\begin{aligned} \text{Transistor 1: } & Vgs_1 - Vt_1 < Vds_1 \Leftrightarrow \\ & Vin - Vx - Vt_1 < Vdd - Vx \Leftrightarrow \\ & 1 - Vx - 0.4 < 1 - Vx \Leftrightarrow \\ & 0.6 - Vx < 1 - Vx \end{aligned} \tag{A.1}$$

Additionally the threshold equation must hold:

$$\begin{aligned} \text{Transistor 1: } & Vgs_1 > Vt_1 \Leftrightarrow \\ & Vin - Vx > Vt_1 \Leftrightarrow \\ & 1 - 0.4 > Vx \Leftrightarrow \\ & 0.6 > Vx \end{aligned} \tag{A.2}$$

Similarly for Transistor 2 in linear region:

$$\begin{aligned} \text{Transistor 2: } & Vgs_2 - Vt_2 > Vds_2 \Leftrightarrow \\ & Vsw - 0 - Vt_2 > Vx - 0 \Leftrightarrow \\ & Vsw - 0.4 > Vx \end{aligned} \tag{A.3}$$

And the threshold equation :

$$\begin{aligned} \text{Transistor 2: } & Vgs_2 > Vt_2 \Leftrightarrow \\ & Vsw - 0 > Vt_2 \Leftrightarrow \\ & Vsw > 0.4 \end{aligned} \tag{A.4}$$

Furthermore since the requirement for the output voltage Vx is to be able to turn on transistor *M4* we have:

From the threshold equation :

$$\begin{aligned} \text{Transistor 4: } & Vgs_4 > Vt_4 \Leftrightarrow \\ & Vx - 0 > Vt_4 \Leftrightarrow \\ & Vx > 0.45 \end{aligned} \tag{A.5}$$

So essentially we have limited the potential output values of Vx in the range $\{0.45 - 0.6\}$ based on Eq. A.1 and Eq. A.5. Thus Eq. A.1 is always fulfilled. However, in order to have Eq.A.3 fulfilled we need to set Vsw at 1 V. Even then, transistor *M4* will marginally be in the linear region since the values of Vt are approximated to 0.4, whereas the real values in the low threshold devices (*lvtNmos*) lie somewhere between $0.41 - 0.43$ based on the simulations run.

Even if the range of values Vx can take is limited at $\{0.45 - 0.55\}$ V that only allows for a very narrow area of freedom for Vsw: $\{0.9 - 1.0\}$ V.

In reality though, the current does not saturate immediately mainly because of the short channel modulation in such small feature sizes. So there is a larger array of values in the margin between the linear and saturation regions. Effectively Vsw could go down to 0.8 or even 0.7 and the transistor *M2* will still be able to push the output voltage of this stage Vx a little higher.

A.1.2 Saturation

Alternatively *M2* can be biased in the saturation region. This will provide greater freedom in the values we can set for Vsw, however it might also increase the power wasted in the source follower stage, since both transistors will have to be larger.

Instead of Eq.A.3, we will have for transistor 2 in Saturation:

$$\begin{aligned} \text{Transistor 2: } & Vgs_2 - Vt_2 < Vds_2 \Leftrightarrow \\ & Vsw - 0 - Vt_2 < Vx - 0 \Leftrightarrow \\ & Vsw - 0.4 < Vx \end{aligned} \tag{A.6}$$

So Eq. A.6 in combination with Eq. A.4 and Eq. A.2 gives us a range for Vsw of $\{0.45 - 0.9\}$ V. In reality a usable range would be up to Vsw of about 0.6 V in order to maintain Vx above 0.45 V.

A.1.3 Sizing

In order to have an idea about the sizing of the two transistors in either of the two cases presented above we need to make an analytical calculation. The preferred result would be an equation of the ratio between the width of the two transistors, in relation to the voltages *Vsw, Vx*.

For the linear calculations:

$$Id1 = \frac{k\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{2L} \tag{A.7}$$

$$Id2 = \frac{k\mathrm{W2}\left(\mathrm{Vx}(\mathrm{Vsw} - \mathrm{Vt2}) - \frac{\mathrm{Vx}^2}{2}\right)}{L} \tag{A.8}$$

We know that: $Id1 = Id2$

$$\frac{k\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{2L} = \frac{k\mathrm{W2}\left(\mathrm{Vx}(\mathrm{Vsw} - \mathrm{Vt2}) - \frac{\mathrm{Vx}^2}{2}\right)}{L} \tag{A.9}$$

$$\frac{Id1}{Id2} = \frac{\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{2\mathrm{W2}\left(\mathrm{Vx}(\mathrm{Vsw} - \mathrm{Vt2}) - \frac{\mathrm{Vx}^2}{2}\right)}$$

$$1 = -\frac{\mathrm{W1}(\mathrm{Va1} - \mathrm{Vdd} + \mathrm{Vx})(-\mathrm{Vin} + \mathrm{Vt1} + \mathrm{Vx})^2}{\mathrm{Va1VxW2}(-2\mathrm{Vsw} + 2\mathrm{Vt2} + \mathrm{Vx})} \tag{A.10}$$

$$\frac{W2}{W1} = -\frac{(\mathrm{Va1} - \mathrm{Vdd} + \mathrm{Vx})(-\mathrm{Vin} + \mathrm{Vt1} + \mathrm{Vx})^2}{\mathrm{Va1Vx}(-2\mathrm{Vsw} + 2\mathrm{Vt2} + \mathrm{Vx})}$$

For the saturation calculations:

$$Id1 = \frac{k\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{2L} \tag{A.11}$$

$$Id2 = \frac{k\mathrm{W2}\left(1 - \frac{\mathrm{Vx}}{\mathrm{Va2}}\right)(\mathrm{Vsw} - \mathrm{Vt2})^2}{2L} \tag{A.12}$$

We know that: $Id1 = Id2$

$$\frac{k\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{2L} = \frac{k\mathrm{W2}\left(1 - \frac{\mathrm{Vx}}{\mathrm{Va2}}\right)(\mathrm{Vsw} - \mathrm{Vt2})^2}{2L} \tag{A.13}$$

$$\frac{Id1}{Id2} = \frac{\mathrm{W1}\left(1 - \frac{\mathrm{Vdd-Vx}}{\mathrm{Va1}}\right)(\mathrm{Vin} - \mathrm{Vt1} - \mathrm{Vx})^2}{\mathrm{W2}\left(1 - \frac{\mathrm{Vx}}{\mathrm{Va2}}\right)(\mathrm{Vsw} - \mathrm{Vt2})^2}$$

$$1 = -\frac{\mathrm{Va2W1}(\mathrm{Va1} - \mathrm{Vdd} + \mathrm{Vx})(-\mathrm{Vin} + \mathrm{Vt1} + \mathrm{Vx})^2}{\mathrm{Va1W2}(\mathrm{Vx} - \mathrm{Va2})(\mathrm{Vsw} - \mathrm{Vt2})^2} \tag{A.14}$$

$$\frac{W2}{W1} = -\frac{\mathrm{Va2}(\mathrm{Va1} - \mathrm{Vdd} + \mathrm{Vx})(-\mathrm{Vin} + \mathrm{Vt1} + \mathrm{Vx})^2}{\mathrm{Va1}(\mathrm{Vx} - \mathrm{Va2})(\mathrm{Vsw} - \mathrm{Vt2})^2}$$

So for:

$$Vt1 = Vt2 = 0.45 \text{ V}$$
$$Vdd = 1.0 \text{ V}$$
$$Vin = 1.0 \text{ V}$$

In Saturation:

$$\frac{\text{W2}}{\text{W1}} = -\frac{1.\text{Va2}(\text{Vx} - 0.55)^2(\text{Va1} + \text{Vx} - 1.)}{\text{Va1}(\text{Vsw} - 0.45)^2(\text{Vx} - 1.\text{Va2})} \tag{A.15}$$

In Linear:

$$\frac{\text{W2}}{\text{W1}} = -\frac{1.(\text{Vx} - 0.55)^2(\text{Va1} + \text{Vx} - 1.)}{\text{Va1}\left(-2.\text{VswVx} + \text{Vx}^2 + 0.9\text{Vx}\right)} \tag{A.16}$$

As we can see, the issues above are rather complex to be solved since the early voltages *Va1, Va2* depend on the overdrive voltages of the two transistors. In turn, the overdrive voltage of transistor 2 depends on the input of the system *Vsw* while the overdrive voltage of transistor 1 depends on the output *Vx* itself. So the exact sizing in combination with the two voltages *Vsw, Vx* of the two transistors *M1,M2* can be only determined by simulating the two devices in Cadence.

B

Schematics

B.1 Preliminary Driver Designs

During the first stages of the design process the circuit schematic presented in Fig. B.1 was used in understanding the functionality of the driver.

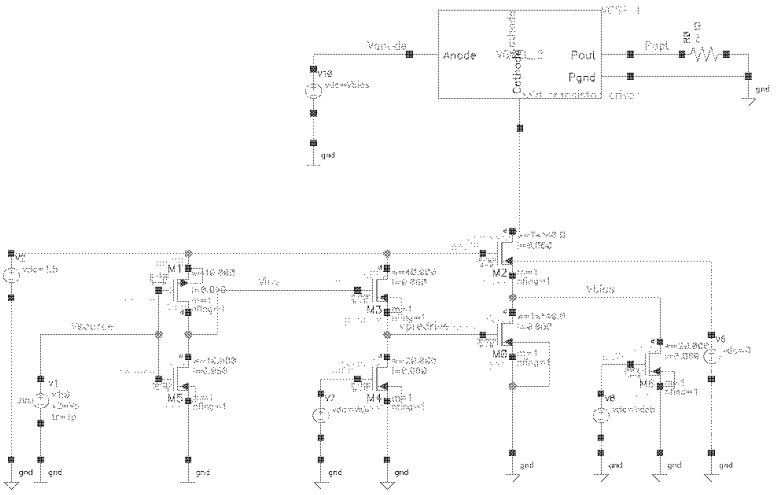


Figure B.1: Cadence circuit model of the 65 nm driver and the VCSEL load.

B.2 PAM-4 driver Test Bench at 65nm node.

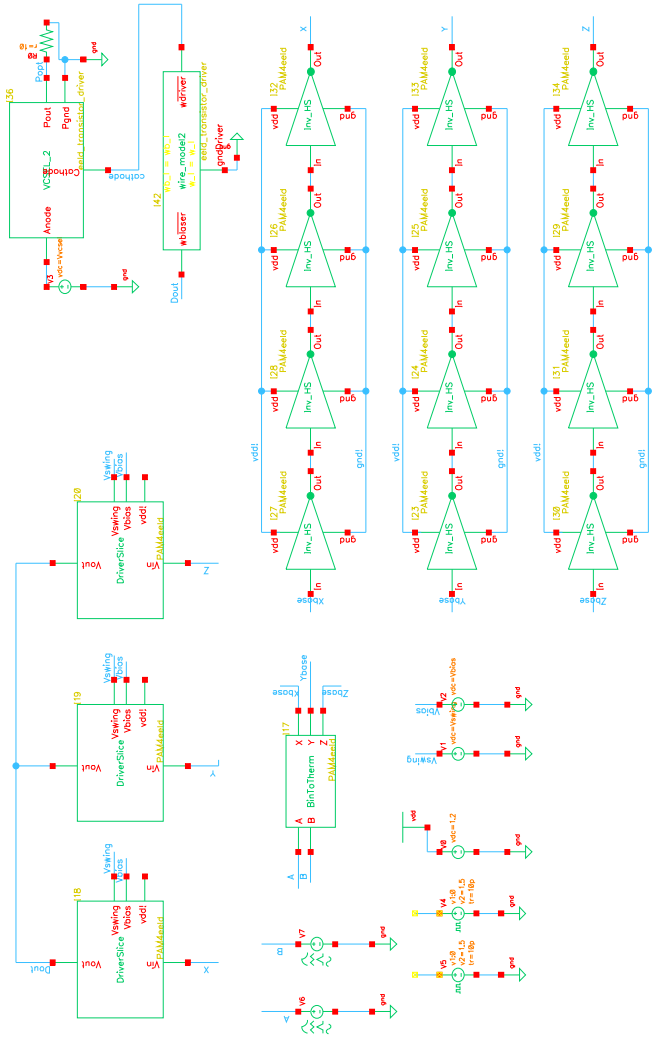


Figure B.2: Schematic printout of the Test Bench used for characterizing the 65nm Driver design.

B.3 PAM-4 Driver in the 28nm node.

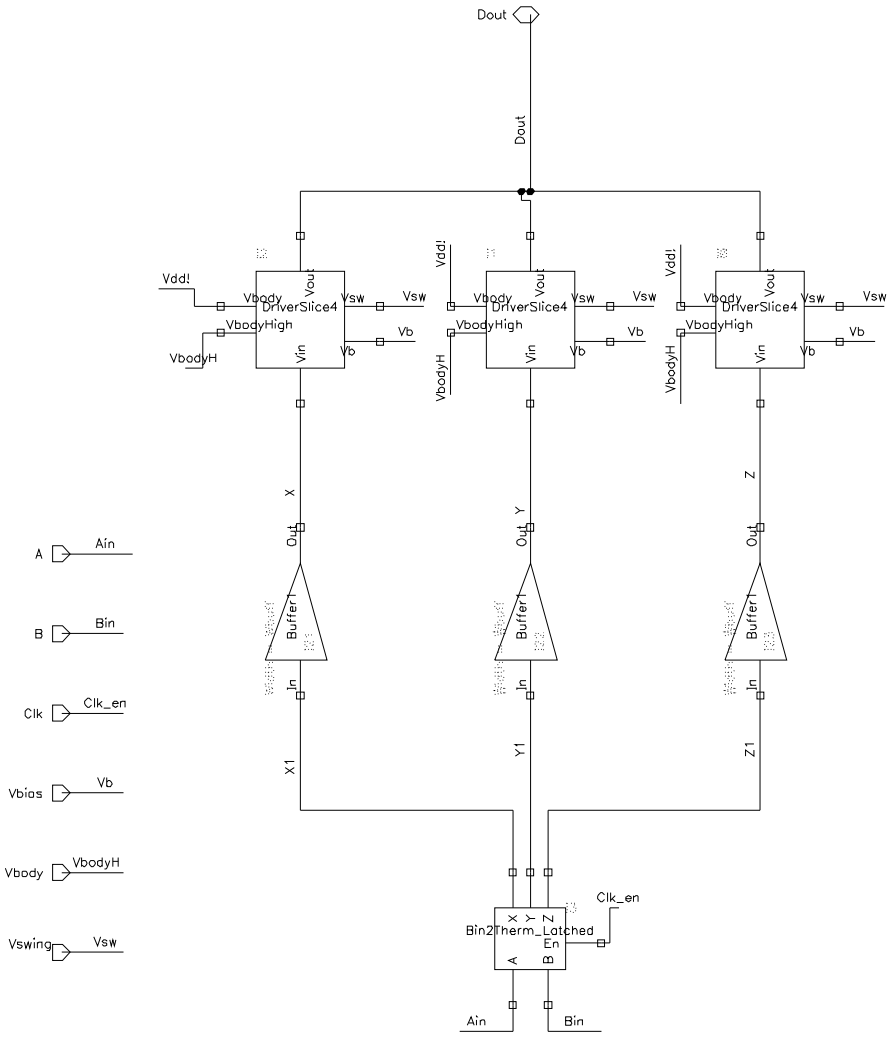


Figure B.3: Schematic printout of the 28nm Drive cell.

C

VCSEL electrical Model

The electrical equivalent VCSEL modeling discussed in Section 4.2.2 can be seen in Fig. C.1b is described by the parameters and equations seen below [2].

$$U_f(U_N) = U_{f0} + \frac{dU_f}{dN}\Big|_0 \cdot \left(\frac{U_N}{10^{-6} \cdot V_\alpha} - N_0\right) \tag{C.1}$$

$$I_{inj} = \eta_i \cdot I_\alpha \tag{C.2}$$

$$C_N = q \cdot 10^6 \tag{C.3}$$

$$r_{sp} = \frac{\tau_n}{q \cdot 10^6} \tag{C.4}$$

$$I_{st}(U_N,U_S) = q \cdot \Gamma \cdot \frac{g_0 \cdot (10^6 \cdot \frac{U_N}{V_\alpha} - N_0)}{1 + \varepsilon \cdot \Gamma \cdot 10^6 \cdot \frac{U_S}{V_\alpha} \cdot 10^6 \cdot U_N} \tag{C.5}$$

$$P_{sp}(U_N) = \frac{\beta \cdot h \cdot c}{\tau_n \cdot \lambda} \cdot U_N \tag{C.6}$$

$$P_{st}(I_{st}) = \frac{h \cdot c}{q \cdot \lambda} \cdot I_{st} \tag{C.7}$$

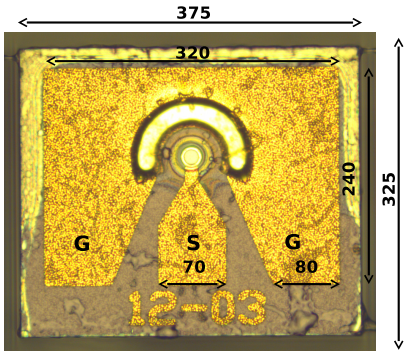
$$c_s = \frac{h \cdot c}{\lambda} \cdot 10^6 \tag{C.8}$$

$$r_{cav} = \frac{\tau_p \cdot \lambda}{10^6 \cdot h \cdot c} \tag{C.9}$$

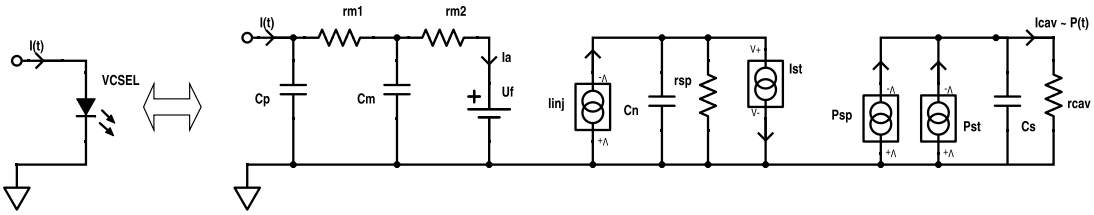
$$P = \eta_e \cdot I_{cav} \tag{C.10}$$

With c: speed of light in vacuum, h: Planck's constant and q: electron charge.

Where the parameters are described as:
c_p = pad capacitance $(20 \cdot 10^{-15})[F]$
r_{m1} = DBR + contact resistance $(45)[\Omega]$
r_{m2} = oxide aperture resistance $(45)[\Omega]$
c_m = oxide + depletion capacitance $(150 \cdot 10^{-15})[F]$
U_{f0} = Fermi separation at transparency $(1.75)[V]$
$\left.\frac{dU_f}{dN}\right|_0$ = differential Fermi separation at transparency $(2.94 \cdot 10^{-26})[Vm^3]$
V_a = effective active volume $(7.7 \cdot 10^{-19})[m^{-3}]$
N_0 = transparency carrier density $(3.38 \cdot 10^{24})[m^{-3}]$
η_i = internal quantum efficiency $(0.86)[-]$
τ_n = carrier lifetime $(1.5 \cdot 10^{-9})[s]$
Γ = optical confinement factor $(0.029)[-]$
g_0 = differential gain $(1.01 \cdot 10^{-11})[m^3 s^{-1}]$
ε = gain suppression factor $(1.37 \cdot 10^{-23})[m^3]$
β = spontaneous emission factor $(1.7 \cdot 10^{-4})[-]$
λ = wavelength $(845 \cdot 10^{-9})[m]$
τ_p = photon lifetime $(3.3 \cdot 10^{-12})[s]$
η_e = photon extraction efficiency $(0.716)[-]$



(a) The structure of the VCSEL chip.



(b) The electrical equivalent circuit of the VCSEL chip.

Figure C.1: Physical layout and electrical equivalent of the VCSEL [1, 2].

D

Additional plots

D.1 40 GHz simulations

In this section we present the resulting eye diagram of the driver current at a frequency of 40 GHz. The control voltages selected for this run are: $V_b = 0.45$ V,$V_{sw} = 0.5$ V and $V_{body} = 3$ V. The resulting eye patterns are presented in Fig. D.1.

The Synchronous mode of operation provides decent eye opening, while the Asynchronous has a multitude of errors. Even if it is not immediately apparent from the eye diagram, the Asynchronous mode skips bits at various transitions. This is due to the inherent gate delay of the encoder, in conjunction with the rise and fall times of the pulse produce delay times that are comparable to half the pulse width, or 25 ps. Thus, the pulse does not have enough time to rise to the peak value before it starts falling again. That produces the reduced amplitude pulses that can be seen in the lower diagram of Fig. D.1. So even though the eye diagram appears relatively clean, in reality it has significant bit errors.

The results presented in Fig. D.1 are an indication of the capabilities of the driver circuit and its performance. However, since the VCSEL model, as the VCSEL diode itself, have a bandwidth of $\approx$ 25 GHz we cannot use it to evaluate the driver-load performance. Consequently, the driver will be assumed to perform up to 25 GHz until it can be thoroughly tested with a faster VCSEL model or a real device.

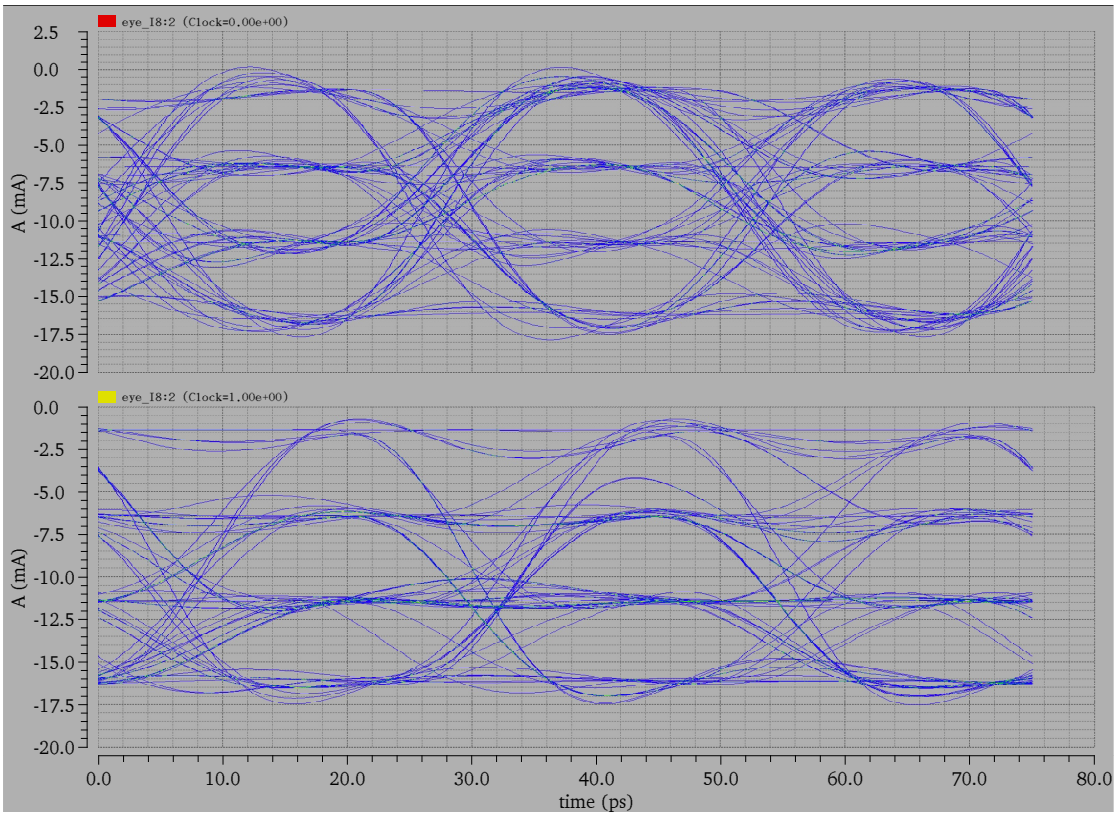


Figure D.1: Eye diagrams for Synchronous (top) and Asynchronous (bottom) mode operation at 40 GHz for control voltage values: $V_b = 0.45$ V,$V_{sw} = 0.5$ V and $V_{body} = 3$ V, and bond wire length $wb_l = 700\mu m$.

D.2 Load S-parameters

In this section we present the characterisation of the interconnect channel and the VCSEL load in terms of their S-parameters at frequencies above 1 GHz.

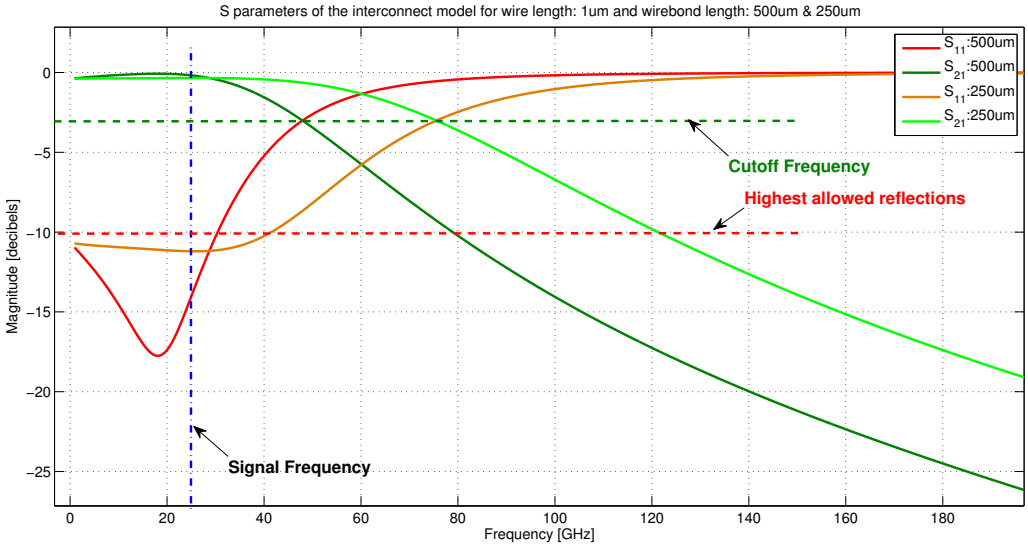


Figure D.2: Graph of the S-parameters of the driver load including interconnects for wire length $w_l = 1\ \mu m$ and bond wire length $wb_l = \{250, 500\}\ \mu m$.

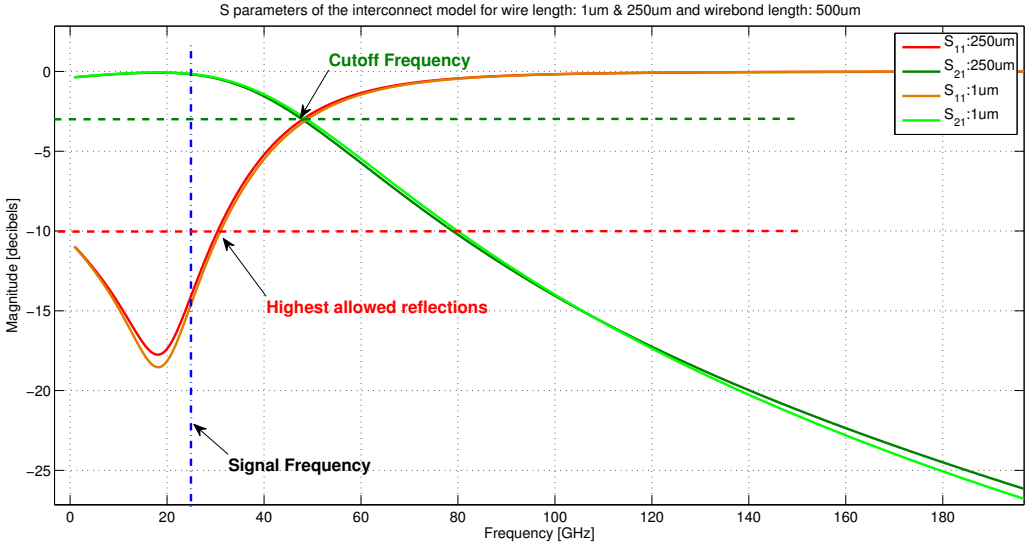


Figure D.3: Graph of the S-parameters of the driver load including interconnects for wire length $w_l = \{1, 250\}\ \mu m$ and bond wire length $wb_l = 250\ \mu m$.

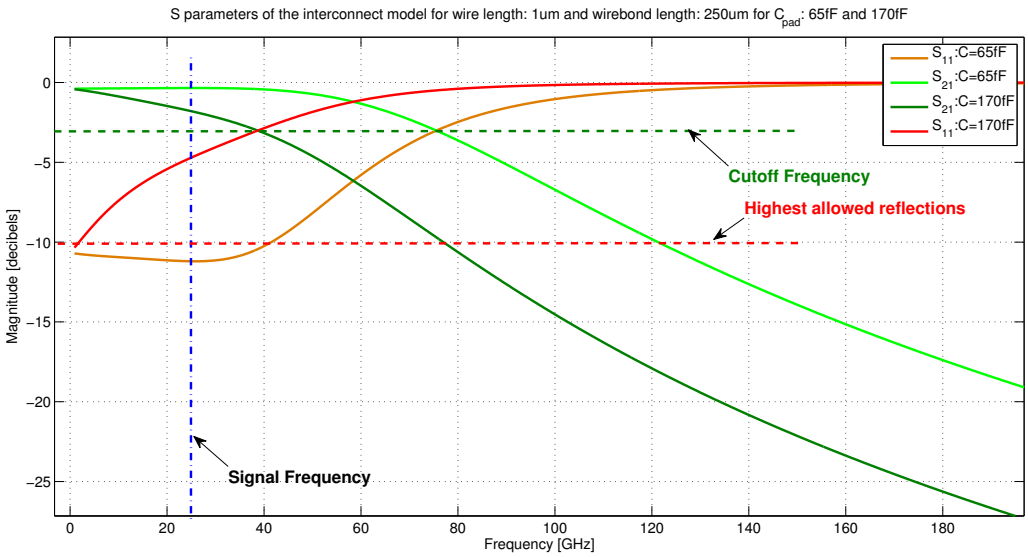
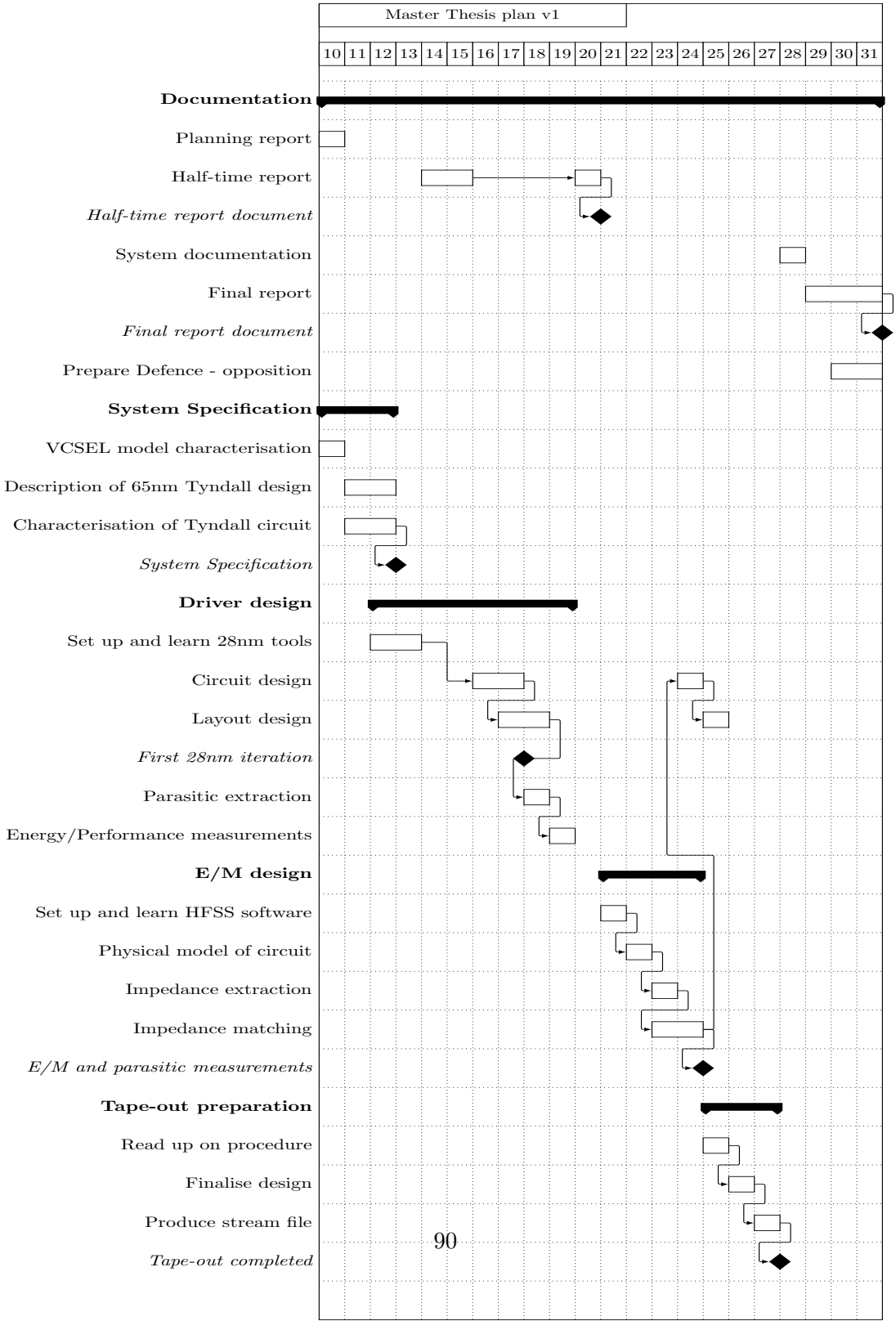


Figure D.4: Graph of the S-parameters of the driver load including interconnects for wire length $w_l = 1\ \mu m$ and bond wire length $wb_l = 250\ \mu m$ and variable bond-pad capacitance values.

E

Timeplan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Documentation
Planning report
Half-time report
Half-time report document
System documentation
Final report
Final report document
Prepare Defence - opposition
System Specification
VCSEL model characterisation
Description of 65nm Tyndall design
Characterisation of Tyndall circuit
System Specification
Driver design
Set up and learn 28nm tools
Circuit design
Layout design
First 28nm iteration
Parasitic extraction
Energy/Performance measurements
E/M design
Set up and learn HFSS software
Physical model of circuit
Impedance extraction
Impedance matching
E/M and parasitic measurements
Tape-out preparation
Read up on procedure
Finalise design
Produce stream file
Tape-out completed