

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Millimeter and Sub-Millimeter Wave Integrated Active Frequency Down-Converters

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Abstract

In recent years, the increasing amount of data transmission, the need for automotive radars, and standoff imaging for security applications are the main factors that accelerate research in the millimeter and sub-millimeter wave frequency ranges. The semiconductor industries have continuously developed their processes, which have opened up opportunities for manufacturing monolithically integrated circuits up to a few hundred GHz, based on transistor technologies. In this thesis, a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology, which show a typical f_t / f_{\max} of 200/300 GHz, 375/650 GHz, and 250/400 GHz, respectively, are verified for analog circuit design. In the above mentioned applications, the frequency mixer is one of the most important components. Consequently, a study of millimeter/sub-millimeter wave mixers is important for the choice of technology and topology.

Aiming for either the next generation of high-speed communication or standoff imaging applications, different mixer topologies are studied, designed and fabricated as candidates for further integration in receivers. The presented mixer topologies include the self-oscillating mixer, the resistive FET mixer, the Gilbert mixer, and the transconductance mixer. All these topologies have been realized in given technologies, and cover the frequencies around ~145 GHz, ~220 GHz, and ~340 GHz. The designed 340 GHz Gilbert mixer with IF buffer amplifier and on-chip patch array antenna demonstrated the first fully integrated receiver in HBT technology at such high frequencies as well as a reasonable noise figure of 17 dB. A novel 110~170 GHz transconductance mixer is characterized in $\times 1$, $\times 2$, $\times 3$, and $\times 4$ harmonic mixing modes, which allows for flexibility in the overall system design.

Apart from the mixer designs, a transceiver, which operates as an amplifier for transmitting and simultaneously as a down-converting mixer for receiving, is designed for the frequency range of 110~170 GHz, aiming for sub-cm resolution in multipixel standoff imaging systems. It is successfully demonstrated in a FMCW radar setup for distance measurements.

Keywords: millimeter wave, sub-millimeter wave, THz, 145 GHz, 220 GHz, 340 GHz, GaAs, mHEMT, InP, DHBT, SiGe, BiCMOS, monolithic, mixer, self-oscillating mixer, resistive mixer, Gilbert mixer, transconductance mixer, harmonic, conversion gain, noise figure, transceiver, FMCW, radar.

List of Publications

Appended publications

This thesis is based on the following papers.

- [A] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, and H. Zirath, “24 GHz balanced self-oscillating mixer with integrated patch antenna array,” in *European Microw. Conf. (EuMC)*, Oct. 2011, pp. 404-407.

- [B] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, B. M. Motlagh, S. Cherednichenko, I. Kallfass, A. Leuther, and H. Zirath, “Monolithically integrated 200-GHz double-slot antenna and resistive mixers in a GaAs-mHEMT MMIC process,” *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2494-2503, Oct. 2011.

- [C] Y. Yan, Y. B. Karandikar, S. E. Gunnarsson, M. Urteaga, R. Pierson, and H. Zirath, “340 GHz integrated receiver in 250 nm InP DHBT technology,” *IEEE Trans. THz Sci. Technol.*, vol. 2, no. 3, pp. 306-314, May 2012.

- [D] Y. Yan, M. Bao, S. E. Gunnarsson, V. Vassilev, and H. Zirath, “A 110-170-GHz multi-mode transconductance mixer in 250-nm InP DHBT technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 9, pp. 2897-2904, Sep. 2015.

- [E] Y. Yan, T. Bryllert, S. E. Gunnarsson, and H. Zirath, “A 110-170 GHz transceiver in 130 nm SiGe BiCMOS technology for FMCW applications,” manuscript to be submitted to *IEEE Trans. Microw. Theory Tech.*.

Other publications

- [a] Y. B. Karandikar, H. Zirath, Y. Yan, and V. Vassilev, “Compact integration of subharmonic resistive mixer with differential double slot antenna in G-band using 50nm InP-HEMT MMIC process,” in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE*, Oct. 2012.

- [b] Y. B. Karandikar, H. Zirath, Y. Yan, and V. Vassilev, “A compact 340 GHz 2×4 patch array with integrated subharmonic Gilbert core mixer as a building block for multi-pixel imaging frontends,” in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2014 IEEE*, Oct. 2014.

Notations and Abbreviations

Notations

B	Bandwidth
β	dc current gain of bipolar transistor in common emitter configuration
BV_{CEO}	Common-emitter breakdown voltage
c	Speed of light
ϵ_r	Relative permittivity
F	Noise factor
f	Frequency
f_{max}	Power gain cutoff frequency
f_t	Current gain cutoff frequency
G	Gain
g_m	Transconductance
I_C	Collector current
I_D	Drain current
k	Boltzmann's constant
L	Loss
P	Power
T	Temperature
V_{CE}	Collector to emitter voltage
V_t	Threshold voltage

Abbreviations

AM	Amplitude modulation
Au	Gold
BCB	Benzocyclobutene
CMOS	Complementary metal-oxide-semiconductor
Cu	Copper
CW	Continuous wave
dc	Direct Current
DDS	Direct digital synthesizer
DHBT	Double-heterojunction bipolar transistor
DSB-NF	Double-sideband noise figure
DUT	Device under test
EM	Electromagnetic
FET	Field effect transistor
FFT	Fast Fourier transform
FMCW	Frequency modulated continuous wave
GaAs	Gallium Arsenide
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IF	Intermediate frequency
ILD	Interlayer dielectric
IM2	Second-order intermodulation
InP	Indium phosphide
LED	Light-emitting diode
LNA	Low noise amplifier
LO	Local oscillator
mHEMT	Metamorphic high electron mobility transistor
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MOS	Metal-oxide-semiconductor
NF	Noise figure
PCB	Printed circuit board
RF	Radio frequency
Rx	Receiver
SHM	Sub-harmonic mixer
Si	Silicon
SiC	Silicon carbide
SiGe	Silicon germanium
SNR	Signal-to-noise ratio
SOM	Self-oscillating mixer
TEM	Transmission electron microscopy
TFR	Thin film resistor
Tx	Transmitter

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Chapter 1

Introduction and Motivation

The millimeter wave portion of the electromagnetic spectrum is defined as frequencies from 30 GHz to 300 GHz, corresponding to a range of wavelengths from 10 millimeters to 1 millimeter in vacuum. The sub-millimeter wave or terahertz (THz) is commonly defined from 300 GHz to 3 THz, with correspondent wavelengths from 1 millimeter to 0.1 millimeter in vacuum. So far, the frequencies below 100 GHz have been relatively well explored, and the research interest at higher frequencies has been boosted by many applications, in which the high-speed data transmission and THz imaging are the two main accelerators.

In data transmission fields, 1.8 zettabytes (1 zettabytes= 10^{21} bytes) of data was created in the year 2011 alone. According to the International Data Corp (IDC) Digital Universe study [1], the amount of data created globally will reach 40 zettabytes by 2020, in which the unstructured information (e.g. files, emails and videos) will account for 90%. As the amount of information to be transferred increases drastically, the millimeter wave becomes very attractive as a medium for data transfer.

In imaging application fields, different ranges of the electromagnetic spectrum from acoustic waves to gamma-rays have been employed for a variety of applications. In recent years, growing terror threats have required more effective security scanning. Ever since a number of experiments showed that the THz signal has the ability to detect certain hidden substances (e.g. plastic explosives, chemical threats and biological threats) from their characteristic spectra with very low levels of non-ionizing radiation [2], increasing research activities have been and will continuously be carried out on THz imaging technologies.

For either high-speed data transmission or standoff imaging, the receiver is an essential component. Fig. 1.1 shows the block diagram of a traditional receiver front-end. The noise figure (NF) is one of the most important figure-of-merits for receivers, and the noise factor of a cascaded network can be calculated by the Friis formula [3]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}} \quad (1.1)$$

where the noise factor F , and the power gain G are in linear scale.

As can be seen from the Friis formula, the noise figure and power gain of the first stage

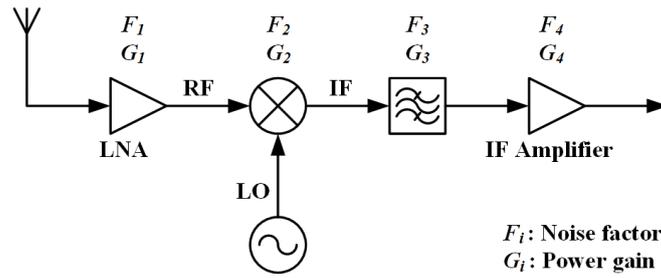


Fig. 1.1. Block diagram of a traditional receiver front-end.

play a dominant role. Therefore, a low noise amplifier (LNA), which is featured by low noise and high gain, is often preferred at the first stage.

In the Friis formula, if only the noise contribution from the first two stages are taken into account, Fig. 1.2 shows the noise figure of the overall receiver chain dependence on the NF_{LNA} (noise figure of the LNA), the G_{LNA} (power gain of the LNA), and the NF_{Mixer} (noise figure of the mixer). Take the $NF_{tot}=10$ dB surface as an example, only if the G_{LNA} is greater than ~ 10 dB, the NF_{LNA} is dominant. On the other hand, when the NF_{LNA} is comparable to the NF_{Mixer} , the LNA becomes less important.

At millimeter wave range, commercial LNAs are available up to ~ 130 GHz with a

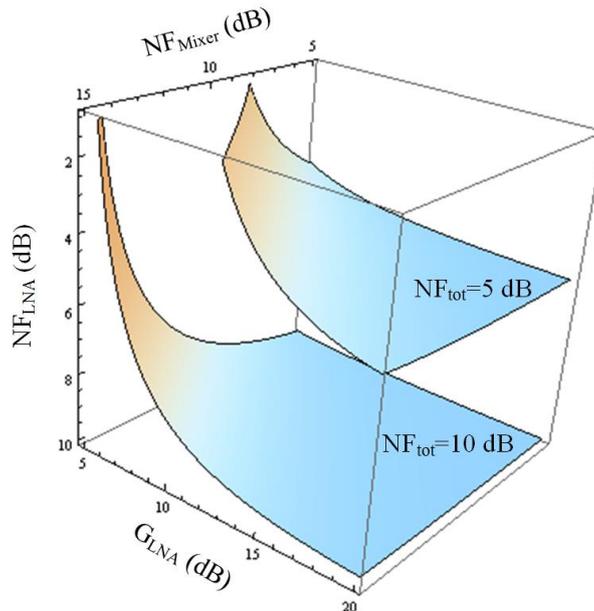


Fig. 1.2. Total noise figure of a receiver as a function of the LNA's noise figure, LNA's gain and the mixer's noise figure.

typical gain of 10 dB and a typical noise figure of 8 dB [4]. At frequencies above 100 GHz, research activities on LNAs have been carried out for years and continuous development is still ongoing at different semiconductor technologies. Fig. 1.3 shows the state-of-the-art small signal gain and the room temperature noise performance of integrated LNAs at frequencies above 100 GHz in recent years. In Fig. 1.3 (a), the trend of reported gain is not clear, because different topologies and amplifier stages were chosen in different works.

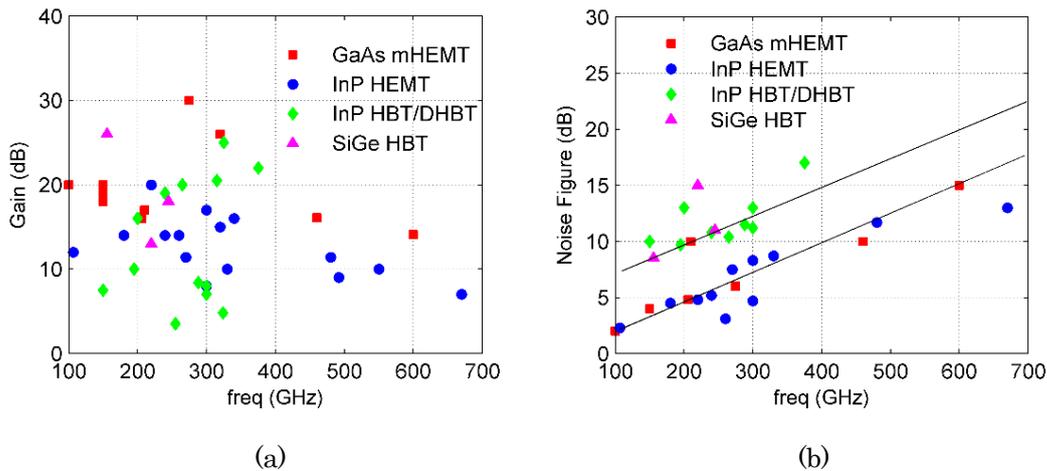


Fig. 1.3. State-of-the-art (a) small signal gain and (b) room temperature noise performance of integrated LNAs in open literature [5]-[37].

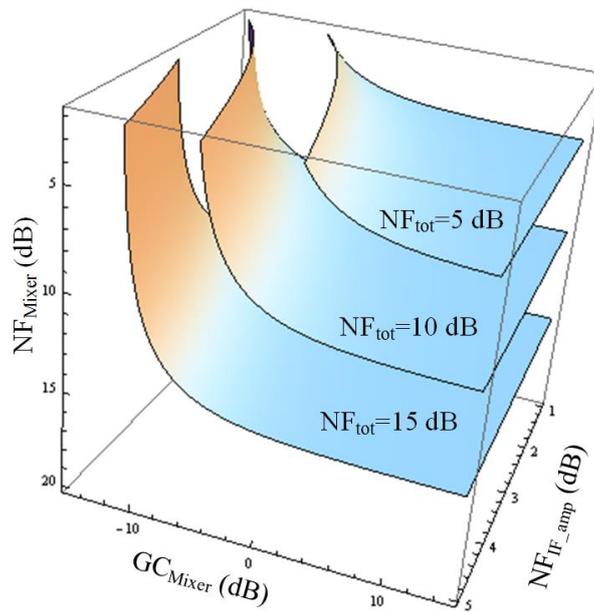


Fig. 1.4. Total noise figure of a receiver as a function of the mixer's noise figure, mixer's conversion gain and the IF amplifier's noise figure.

But from Fig. 1.3 (b), it can be seen that the best noise figures reported from heterojunction bipolar transistor (HBT) technologies are around 5 dB higher than the ones from high electron mobility transistor (HEMT) technologies, and the noise figure increases proportionally with the working frequency in general.

For a receiver, it is definitely preferable to have an LNA at the first stage. However, at the time when the work presented in this thesis was done, most of them are pioneer research in given technologies and frequencies. Considering the relative high noise figure (especially for the LNAs in HBT technologies) and the design risk, such as center frequency shift, the LNA and the mixer are developed separately in the first phase. For this reason, my research is mainly millimeter and sub-millimeter wave active mixers, either stand-alone or integrated with antennas.

For situations where the LNA is omitted in a receiver front-end, Fig. 1.4 shows the noise figure dependence on the NF_{Mixer} (noise figure of the mixer), the G_{Mixer} (conversion gain of the mixer), and the $NF_{\text{IF_amp}}$ (noise figure of the IF amplifier). The $NF_{\text{IF_amp}}$ is normally better than 5 dB. Hence, for a moderate NF_{tot} of 10 ~ 15 dB, as long as the G_{Mixer} is better than ~ -10 dB, the noise contribution from the mixer is dominant.

Aiming for monolithically integrated mixers at millimeter and sub-millimeter wave range, different semiconductor technologies are employed in this thesis. In Chapter 2, a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology are presented and compared. In Chapter 3, dominant topologies of active mixers are described and corresponding designs, aiming for millimeter/sub-millimeter wave frequencies, are presented. Chapter 4 presents a 110-170 GHz frequency modulated continuous wave (FMCW) transceiver, in which the transistor operates as both an amplifier for transmitting and a fundamental mixer for receiving, intended for standoff imaging applications. Finally, the thesis is concluded in Chapter 5.

Chapter 2

Technologies

Semiconductors brought a revolutionary change to the world. The first semiconductor effect was recorded in 1833 by Michael Faraday, who observed that the electrical conduction increased with temperature in silver sulfide crystals, which was opposite to the other metals [38]. In 1874, Karl Ferdinand Braun discovered the semiconductor point-contact rectifier effect, and described the semiconductor diode for the first time [39]. In 1926, Julius Lilienfeld patented the concept of the field effect semiconductor device [40], which is called a field-effect transistor (FET) today. However, no functioning devices were constructed at that time. In 1940, Russel Ohl discovered the p-n junction in silicon [41]. Derived from Ohl's discovery, William Shockley conceived an improved transistor, which is the junction transistor, in 1948 [42]. Due to the lack of sufficiently pure, uniform semiconductor materials, it took three more years until the first grown-junction transistor was fabricated by Gordon Teal in 1951 [43].

In 1958, Jack S. Kilby demonstrated the first all-semiconductor solid state circuit, on which both active and passive components were fabricated from semiconductor materials, and the separate elements were connected through gold wires [44]. Aiming for a more efficient way to make electronic circuits, Jean Hoerni invented the “planar” manufacturing process in 1959, thereby solving reliability problems and revolutionizing semiconductor manufacturing [45]. In the same year, Robert Noyce patented a monolithic integrated circuit concept that can be manufactured in high volume [46]. Based on Hoerni's planar process and Noyce's approach, Jay Last led the development of the first commercial planar integrated circuit in 1960 [47]. From then on, monolithic integrated circuits together with the semiconductor technologies began to be developed rapidly and research has drastically changed the world.

In the past half century, researchers have explored many semiconductor materials, in which silicon (Si) is the most widely used material because of its low raw material cost, high yield, and relatively high thermal conductivity. By alloying other materials with the silicon, several compound semiconductor materials emerged with different features. Silicon germanium (SiGe) is a relative new material, and it is now commonly used for high-speed heterojunction bipolar transistors. Silicon carbide (SiC) is found to be applied for light-emitting diodes (LEDs) and detectors. Investigations also show that the SiC can withstand very high temperatures and high voltages. In III-V technologies, gallium arsenide (GaAs) and indium phosphide (InP) are the two most popular materials for very

high speed devices. By far, both the GaAs-based metamorphic high electron mobility transistor (mHEMT) [13] and the InP-based high electron mobility transistors (HEMT)/heterojunction bipolar transistors (HBT) have reported state-of-the-art performance, with current gain cutoff frequency (f_i) and power gain cutoff frequency (f_{\max}) approaching or exceeding 1 THz [48]-[50].

In this thesis, the presented work covers three semiconductor technologies, namely 100 nm GaAs mHEMT technology, 250 nm InP double-heterojunction bipolar transistor (DHBT) technology, and 130 nm SiGe BiCMOS technology.

2.1 100 nm GaAs mHEMT Technology

The HEMT based on InGaAs/InAlAs heterostructures is a well-proven device for high-frequency and low-noise applications [51]-[52]. The 100 nm GaAs mHEMT technology presented in this work is developed by the Fraunhofer Institute of Applied Solid-State Physics (FHG-IAF), Freiburg, Germany [53]. Fig. 2.1 shows a transmission electron microscopy (TEM) cross section of the metamorphic buffer with the active device on top. The high dislocation density confined to the metamorphic buffer is clearly visible, and the heterostructure is grown on a metamorphic buffer to adapt the lattice constant on GaAs wafers.

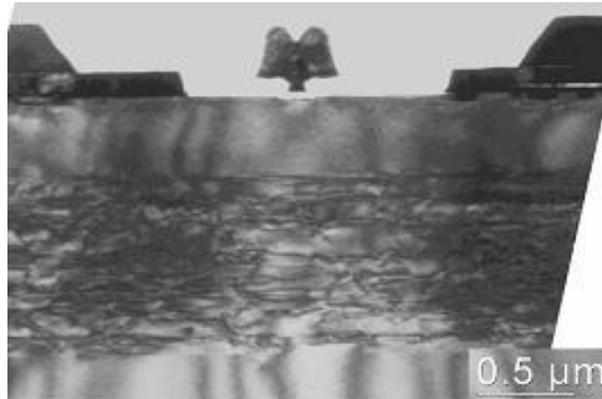


Fig. 2.1. TEM cross section of a mHEMT. (from Fraunhofer Institute)

In this process, passive elements are metal-insulator-metal (MIM) capacitors, thin film resistors (TFR), an electron beam evaporated Au-based interconnection layer and a 2.7 μm thick plated Au layer for air bridges and transmission lines. The GaAs substrate is thinned to a final thickness of 50 μm in order to suppress substrate modes for circuits operating in the G- and H- band. Fabricated transistors exhibit a maximum transconductance ($g_{m,\max}$) of 140 mS/mm and a maximum drain current ($I_{D,\max}$) of 900 mA/mm. A $2 \times 30 \mu\text{m}$ gate width 100 nm mHEMT demonstrates an f_i of 200 GHz and an f_{\max} of 300 GHz.

2.2 250 nm InP DHBT Technology

InP HBTs are competitive for millimeter wave power amplification [50], because they

offer a high cutoff frequency with high voltage handling capacity due to the use of a wide bandgap InP collector. Furthermore, at frequencies approaching a significant fraction of the cutoff frequency, input shot noise no longer dominates over Johnson noise from the base resistance, and InP HBTs operated at 10–20% of their peak current density should have comparable noise figures to HEMTs of similar bandwidth [54].

Fig. 2.2 shows a representative cross-section of the back-end of the 250 nm InP DHBT MMIC-process, which is developed by Teledyne Technologies, Inc., Thousand Oaks, California, USA [55]. This process includes thin-film resistors (TFR), MIM capacitors, and 4-levels of interconnect (MET1–MET4). A benzocyclobutene (BCB) spin-on-dielectric ($\epsilon_r \sim 2.7$) is used as the interlayer dielectric (ILD) with 1 μm ILD spacing between each metal layer. Electroplated Au-based interconnects are used for the metallization layers, where MET1–MET3 have a thickness of 1 μm and MET4 has a thickness of 3 μm . Fabricated transistors exhibit a typical dc current gain (β) of around 25 and a common-emitter breakdown voltage (BV_{CEO}) of >4 V. A typical 4×0.25 μm^2 HBT demonstrates an f_t of 375 GHz and an f_{max} of >650 GHz, at $I_C=9$ mA and $V_{\text{CE}}=1.8$ V.

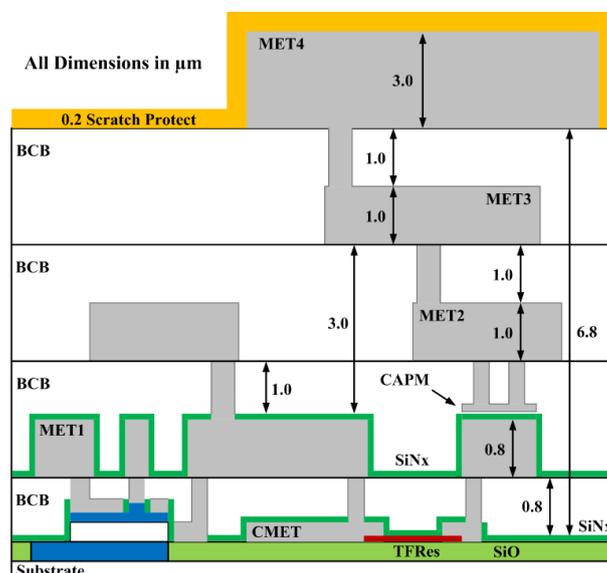


Fig. 2.2. Cross-section of the 250 nm InP DHBT process. (from Teledyne Technologies)

2.3 130 nm SiGe BiCMOS Technology

SiGe BiCMOS technology combines the strengths of two different transistor technologies, namely the bipolar transistor and the CMOS transistor, into a single integrated chip. The HBTs offer high speed and high gain, which are critical for high frequency analog components, whereas CMOS technology allows for low-power logic gates. This unique combination opens up the opportunity for Si-based RF system-on-a-chip solutions [56].

The 130 nm SiGe BiCMOS technology presented here is developed by Infineon Technologies [57]. The cross section of this SiGe BiCMOS process back-end is shown in Fig. 2.3. It includes *npn* transistors, metal-oxide-semiconductor (MOS) transistors, metal

film resistor, MIM capacitor, junction capacitor, pin diode, and 6-levels of interconnect (M1-M6). Cu-based interconnects are used for the metallization layers, with 4 thin lower layers (M1-M4) and 2 thick upper layers (M5-M6).

For RF designs, 3 types of *npn* transistors are available in this process. These are high speed transistors, medium speed transistors, and high voltage transistors. All types of transistors show a typical dc current gain (β) of around 1500. A single base high speed *npn* transistor with an emitter mask size of $0.22 \times 2.8 \mu\text{m}^2$ exhibits a common-emitter breakdown voltage (BV_{CEO}) of 1.4 V and demonstrates typical f_i / f_{max} of 250/400 GHz. A medium speed *npn* transistor exhibits a BV_{CEO} of 2.2 V and demonstrates a typical f_i of 100 GHz. A high voltage *npn* transistor exhibits a BV_{CEO} of 3 V and demonstrates a typical f_i of 55 GHz.

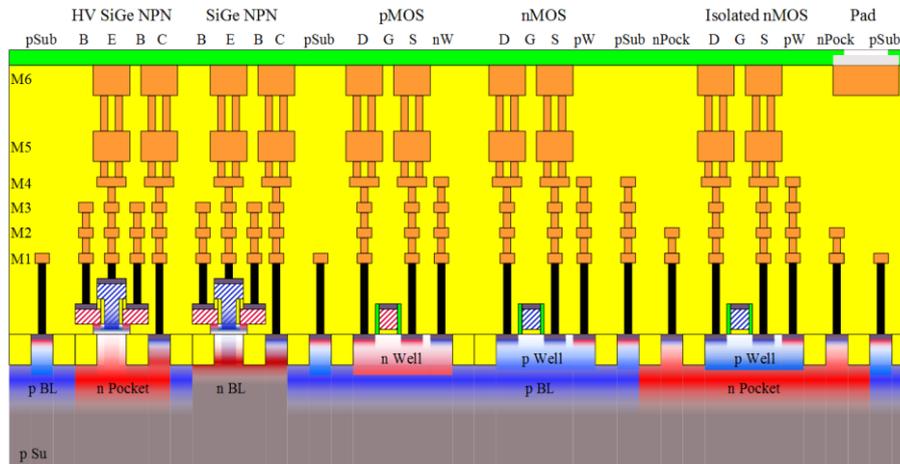


Fig. 2.3. Cross-section of the 130 nm SiGe BiCMOS B11HFC process. (from Infineon Technologies)

Chapter 3

Mixer Topologies

In general, a mixer is a nonlinear electrical component that multiplies the two input signals (f_1 and f_2) and generates a number of new frequencies (f_{out}):

$$f_{out} = mf_1 + nf_2 \quad (3.1)$$

where m and n are integers or zero ($0, \pm 1, \pm 2, \pm 3, \dots$).

For a down-converter mixer, normally the IF frequency, $f_{IF}=|f_1 - f_2|$, is the desired one, while for an up-converter mixer, $f_{RF}=f_1 + f_2$ is most often used.

A frequency mixer can be realized on any device with a non-linear current-voltage (I-V) characteristic. Depending on the device property, mixers are widely classified as passive mixers and active mixers. Passive mixers often use one or more diodes, e.g. point-contact diodes, PN-junction diodes, or Schottky-barrier diodes, as the non-linear device [58]-[59]. Since a passive mixer consumes no dc power, only conversion loss can be obtained. Nowadays, active mixers using transistors as the dominant devices may achieve conversion gain instead of conversion loss, and normally require lower local oscillator (LO) power levels than would be required for passive mixers [60]. In the millimeter wave and THz regimes, Schottky diodes based on waveguide technologies used to be the only solution for mixers [61]-[63]. As the semiconductor manufacturing technologies are continuously developing, active mixers based on transistors have already reached the THz range [64]-[65].

Based on transistor technologies, a self-oscillating mixer (SOM), which avoids a bulky LO chain, may be a cost-effective solution especially at millimeter and sub-millimeter wave frequencies. The topology is studied in this thesis and a 24 GHz SOM is designed and evaluated. In FET technologies, resistive mixers have various advantages such as no dc consumption, no shot noise, high linearity, low $1/f$ noise [60], and possibility to operate at or even above the transistor's f_t/f_{max} [66]. Therefore, in the 100 nm GaAs mHEMT technology with f_t/f_{max} of 200/300 GHz, two resistive mixers are designed at ~ 200 GHz. In bipolar junction transistor (BJT) technologies, both Gilbert mixers and transconductance mixers have been experimentally well-proved at frequencies below 100 GHz. In a 250 nm InP DHBT technology with f_t/f_{max} of 375/650 GHz, both topologies are studied and designed at frequencies above 100 GHz. Pros and cons of each topologies are discussed at the end of this chapter.

3.1 Self-Oscillating Mixer (SOM)

3.1.1 Principle of SOM

The SOM operates as both a frequency mixer and an oscillator, in which the self-oscillation signal applies as the LO for the mixer. It can be a convenient solution at high frequencies where a typical bulky LO multiplication chain may be omitted [67]. Fig. 3.1 shows the schematic of one type of single-ended SOM. It is a combination of a gate mixer and a common source oscillator.

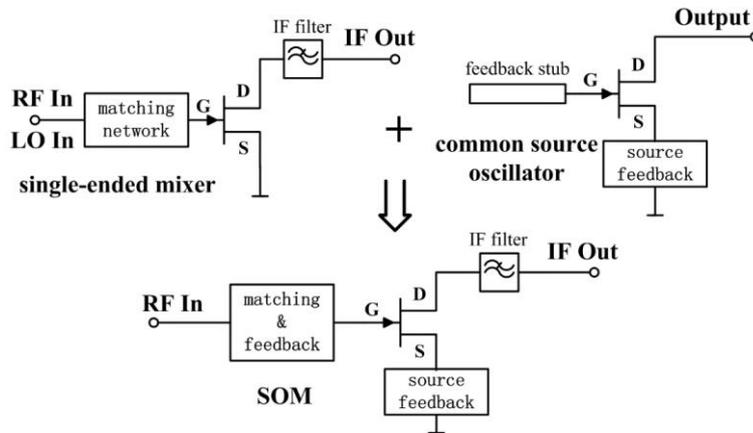


Fig. 3.1. Schematic of a single-ended SOM.

Since an oscillator is an autonomous component, to make the SOM oscillate at the desired frequency with acceptable power is of higher priority than optimizing the mixer performance. Therefore, the design priority is to have the source feedback and gate feedback optimized and make the SOM fulfill oscillation conditions at the desired frequency [68]. Then, all parts including the dc biases are tuned for optimized performance. In addition, the matching network at the gate should be designed such that the oscillation is not sensitive to the input RF signal.

3.1.2 Design and Evaluation of a 24 GHz Balanced SOM with Integrated Patch Array

The purpose of designing the 24 GHz SOM was to evaluate the circuit for later use as an up-scaled key-element for millimeter-wave standoff imaging applications. Considering the target frequency of 340 GHz, the SOM may be a convenient solution even though a deteriorated conversion gain and noise performance might be foreseen compared to a traditional mixer.

In order to gain more experimental knowledge on a SOM, the 24 GHz design is fabricated as a hybrid integrated circuit, which enables on-board trimming. Fig. 3.2 shows the schematic of the designed 24 GHz SOM. A balanced topology is chosen in order to reduce the required oscillation frequency by a factor of 2. This can be of benefit for the planned 340 GHz SOM, because the maximum oscillation frequency is limited by the f_{\max}

of the transistor in use. In Fig. 3.2, a quarter wavelength short-circuited stub (at 24 GHz) is connected at the source to enable a dc ground path for the transistor. The resonant circuit which mainly determines the oscillating frequency incorporates the gate transmission line as an inductive element and the capacitors “ C_1 ”. Values of these components are tuned in simulations to achieve the fundamental oscillating frequency at 12 GHz. The RF port, which is inserted at the center point, does not affect the oscillation condition due to the virtual ground property at this node. Furthermore, the anti-phase condition offered by the topology will cancel the fundamental frequency (12 GHz) and all the odd harmonics at both RF and IF ports, while the even harmonics are in phase and will thus be added constructively.

The designed 24 GHz SOM is integrated with a 4×4 patch array antenna with uniform amplitude and phase feeding network. The SOM and the antenna are matched to 50Ω and connected to each other. Fig. 3.3 shows the photo of the integrated 24 GHz down-converter. It is fabricated on standard Rogers 3003 substrate with $\epsilon_r=3$, and occupies a board size of $75 \times 45 \text{ mm}^2$.

The integrated SOM with the patch array is characterized as a receiver in a complete transmitter/receiver (Tx/Rx) link. A standard rectangular horn acts as the Tx antenna and is

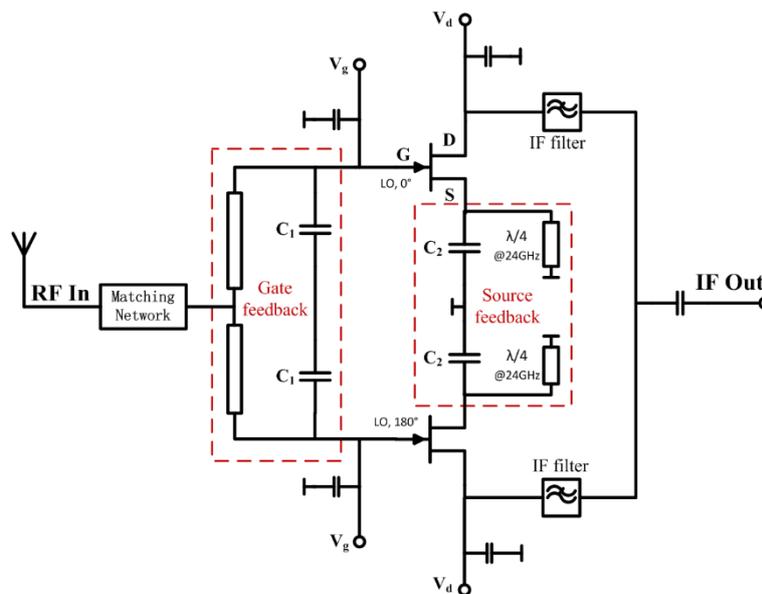


Fig. 3.2. Schematic of the balanced SOM.

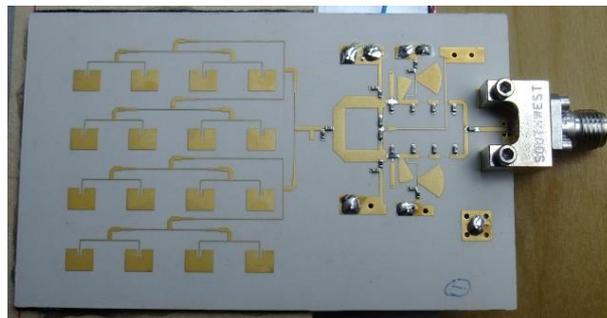


Fig. 3.3. Photo of the 24 GHz SOM with integrated 4×4 patch array antenna.

aligned on axis with the R_x patch array. A distance of 4 meters between the two antennas guarantees the far-field condition. In the link budget, the T_x antenna gain is from electromagnetic (EM) simulation while the patch array antenna gain is from the measurement results on the breakout antenna alone. Fig. 3.4 shows both the simulated and measured isotropic receiver gain, which incorporates the SOM's conversion gain and the antenna's isotropic gain. The integrated receiver (SOM+patch array) achieves a peak isotropic gain of 5.9 dB and a 3-dB-bandwidth of 800 MHz.

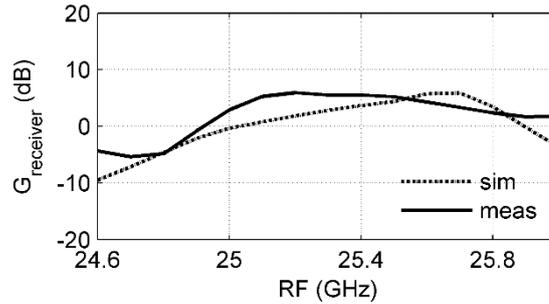


Fig. 3.4. Simulated and measured isotropic gain of the receiver.

3.2 Resistive FET Mixer

3.2.1 Principle of Resistive FET Mixer

The resistive FET mixer was first proposed by Stephen A. Maas in 1987 [69]. The topology is shown in Fig. 3.5. The LO signal along with a dc bias are applied at the gate while the RF signal is applied to the drain. The IF frequency is then filtered from the drain.

Fig. 3.6 shows the typical I-V characteristics of a FET. In the linear region, the drain-to-source channel can be approximated by a variable resistor, and channel resistances can be denoted by the IV-slopes which depend on the gate voltage. Resistive FET mixers utilize exactly this property, so it can be modeled as a variable resistance which is controlled by the LO signal. For a typical resistive mixer, the gate is biased at the transistor's threshold voltage (V_t) while no dc bias is applied to the drain [70]. In one LO cycle, the channel resistance increases to virtually infinity (R_{off}) when the gate voltage drops below V_t , and it decreases to a very low value (R_{on}) when the gate voltage reaches its maximum.

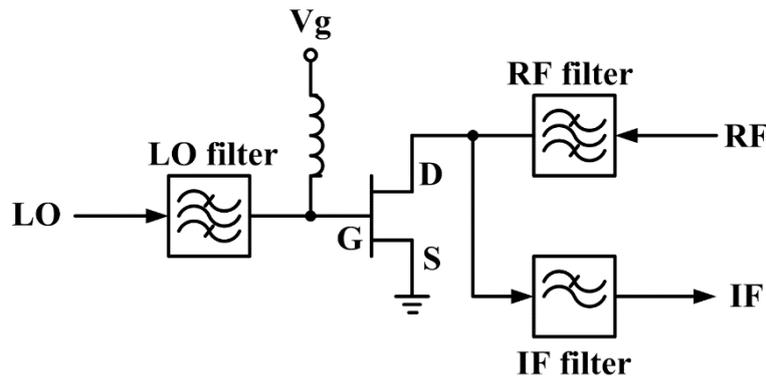


Fig. 3.5. Topology of the resistive FET mixer.

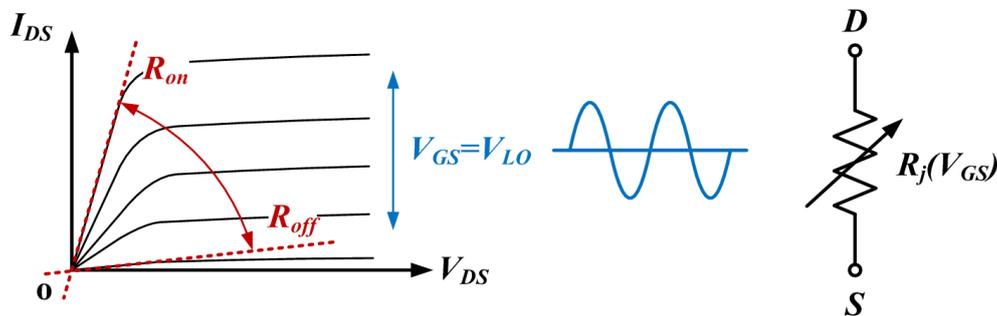


Fig. 3.6. Simplified model of the resistive mixer.

3.2.2 Design and Evaluation of Two 200 GHz Resistive Mixers with Integrated Double-Slot Antenna

The frequency band around 220 GHz, as one of the atmosphere windows, is potentially interesting for both high-speed wireless communication and high-resolution imaging applications. In the past decade, continuous development of semiconductor manufacturing technologies has opened up opportunities for monolithic integrated circuits at such high frequencies.

The 100-nm mHEMT technology, which has been described in section 2.1, shows typical f_t / f_{\max} of 200/300 GHz. Therefore, circuits at around 220 GHz are theoretically realizable. Based on such a technology, a single-ended resistive mixer and a single-balanced resistive mixer with integrated double-slot antenna are designed at ~ 200 GHz. Fig. 3.7 shows the schematics of the two mixers. In both topologies, the LO is connected to the gate in order to vary the channel resistance, and a single-section coupled line filter is inserted at the RF port to suppress LO-to-RF leakage. In the single-balanced topology, the LO signals at the two gates show a 180° phase difference due to the half wavelength stub. Therefore, the LO leakage at the combined RF port can be cancelled.

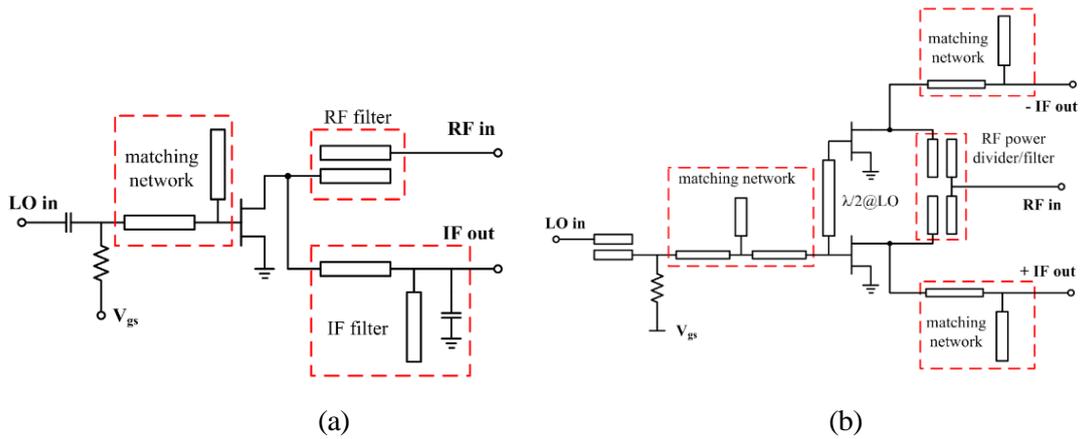


Fig. 3.7. Schematic of (a) the single-ended resistive mixer and (b) the single-balanced resistive mixer.

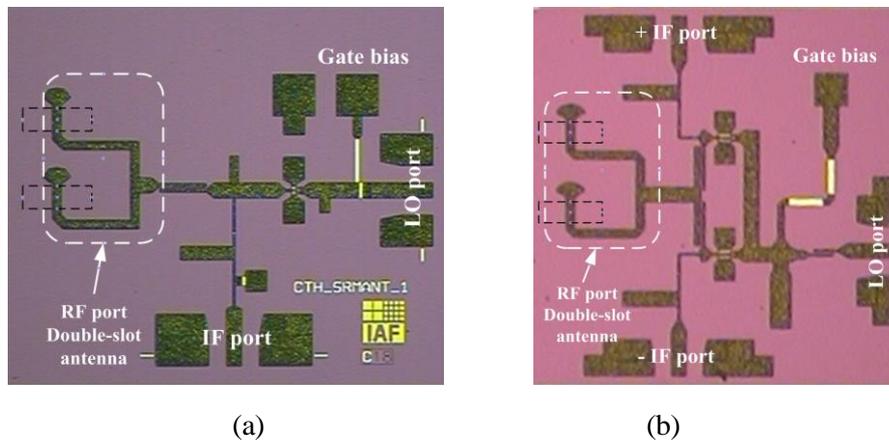


Fig. 3.8. Chip photos of (a) double-slot antenna integrated with single-ended resistive mixer and (b) double-slot antenna integrated with single-balanced resistive mixer.

In the given process with two metal layers (including the ground layer at the backside), the double-slot antenna is chosen to be integrated on-chip, because at millimeter-wave frequencies, its radiation can be coupled to a focusing ellipsoidal lens [71]-[72]. With the help of the focusing lens, a narrow beam with a directivity of ~ 24.5 dBi is obtained in simulation.

Fig. 3.8 shows the chip photos of both integrated receivers. Two slots are etched out on the backside metal layer (marked by the black dashed rectangles) while the microstrip feed network is located on the top metal layer for integration with resistive mixers. The RF ports of both mixers and the antenna ports are matched to 50Ω to be able to connect directly. The two integrated receivers occupy chip areas of $1100 \times 700 \mu\text{m}^2$ and $900 \times 950 \mu\text{m}^2$, respectively.

An attempt was initially made to measure the two integrated receivers by using the Y-factor method, where a big piece of absorbing foam at room temperature (295 K) is seen by the receiver antenna as the hot load, and a box of absorbing foam at liquid nitrogen (77 K) serves as the cold load. A similar measurement setup is presented in [73]. Theoretically, both conversion gain and noise figure can be obtained from the Y-factor method. However, the measured Y-factors of the two designed receivers are too small to be read accurately.

As can be seen from Fig. 3.9, the Y-factor tends to be lower than 0.5 dB when the noise figure is higher than 7.5 dB.

In order to evaluate the two integrated receivers in a more reliable way, a complete T_x/R_x link at G-band (140-220 GHz) has been built. Fig. 3.10 shows a photo of the measurement setup. In a wafer-probe measurement, the pads on the chip can only be probed from the top direction, so the beam from the on-chip double-slot antenna radiates downwards. A 30 cm high metallic table is specially designed and fabricated for this measurement to offer the possibility to mount probe manipulators from three directions. The receiver to be tested is glued onto a Si lens, which is mounted at the center opening on top of the metallic table, and a G-band corrugated horn antenna together with an in-house manufactured $\times 6$ frequency multiplier source module (output frequency band: 163-202 GHz) are located 200 mm beneath it. The T_x/R_x antennas should be aligned in axis with the same polarization.

With +5 dBm LO power applied, the measured receiver gain (G_{RX}) and conversion loss of the mixers (L_c) are shown in Fig. 3.11 and Fig. 3.12, respectively. Here the receiver

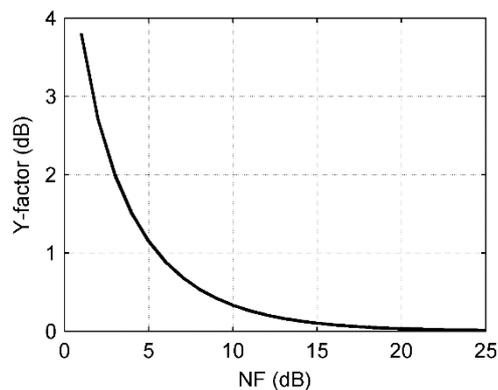


Fig. 3.9. The Y-factor as a function of the noise figure when $T_{\text{hot}} = 290$ K and $T_{\text{cold}} = 77$ K.

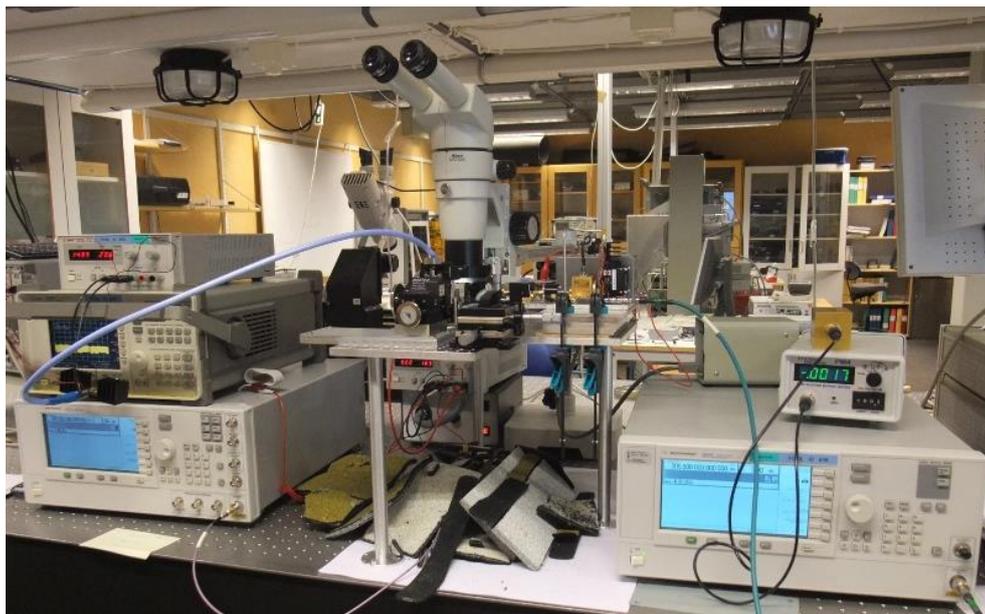


Fig. 3.10. Photo of the measurement setup.

gain incorporates the antenna gain referred to an isotropic antenna and the conversion loss of the mixer. Therefore, in the RF frequency range of 185~202 GHz or the IF frequency range of 1~18 GHz, a typical L_c of 8.0 dB and G_{RX} of 15.4 dB are measured for the single-ended topology, while a typical L_c of 12.2 dB and G_{RX} of 11.2 dB are obtained from one of the two IF outputs for the single-balanced one.

In this work, the noise figures of the two integrated receivers are estimated by a proposed novel method, which is called the signal generator N-times power method. The working principle of the proposed method is presented in the Appendix. The measured noise figure of the two receivers is around 1 dB higher than the conversion loss of mixers alone.

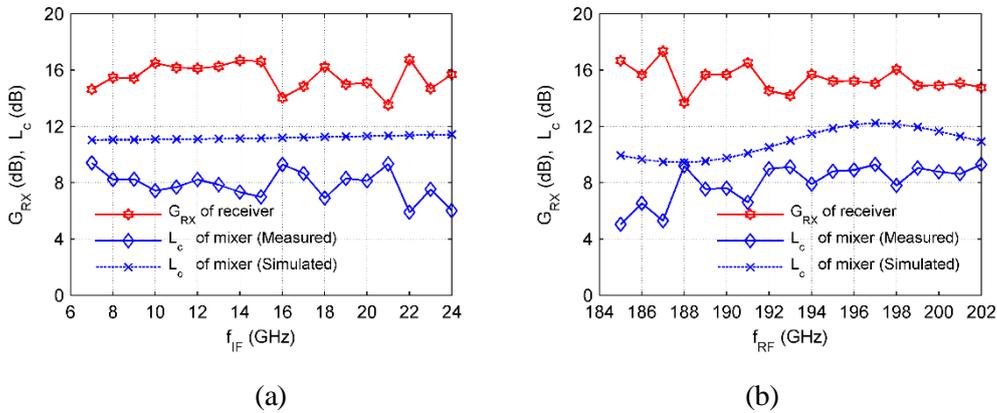


Fig. 3.11. Conversion loss of the single-ended resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 209 GHz (b) fixed IF at 1 GHz.

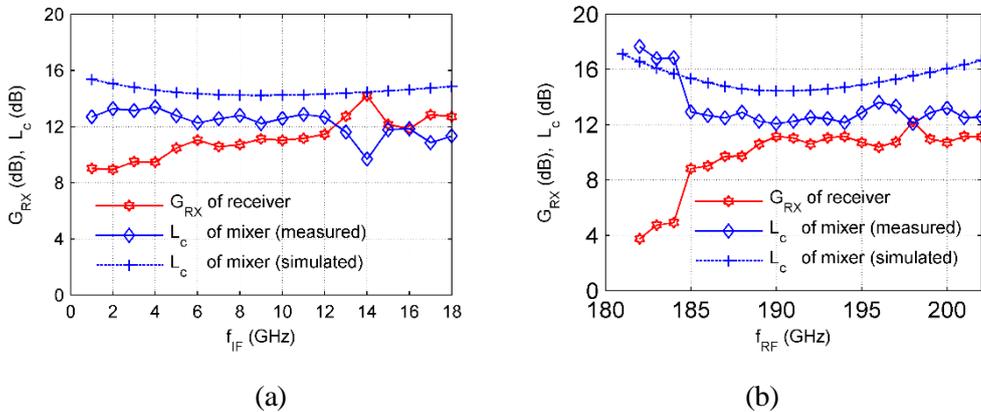


Fig. 3.12. Conversion loss of the single-balanced resistive mixer and estimated gain of the integrated receiver (a) fixed LO at 184 GHz (b) fixed IF at 1 GHz.

3.3 Gilbert Mixer

3.3.1 Principle of Gilbert Mixer

In bipolar transistor technologies, the Gilbert-cell mixer is popular for its excellent properties, such as relative high conversion gain, broad operating bandwidth, relative low LO driving power, and good port-to-port isolation [74]. Fig. 3.13 shows the topology of a basic bipolar Gilbert-cell mixer. It is double-balanced and has all the properties of a double-balanced mixer. The upper four LO transistors are driven by a strong LO signal and operate as switches which are turned alternately on and off over the LO cycle. The lower two RF transistors are biased at the forward active region and operate like a differential amplifier. Ideally, the emitters of the LO transistors are virtual ground for the LO, so there will be no LO voltage on the collectors of the RF transistors. Similarly, the collectors of the LO transistors are also virtual ground for the LO, so the LO-to-IF isolation is usually good (e.g. can be around 50~60 dB at frequencies below 1 GHz [74]).

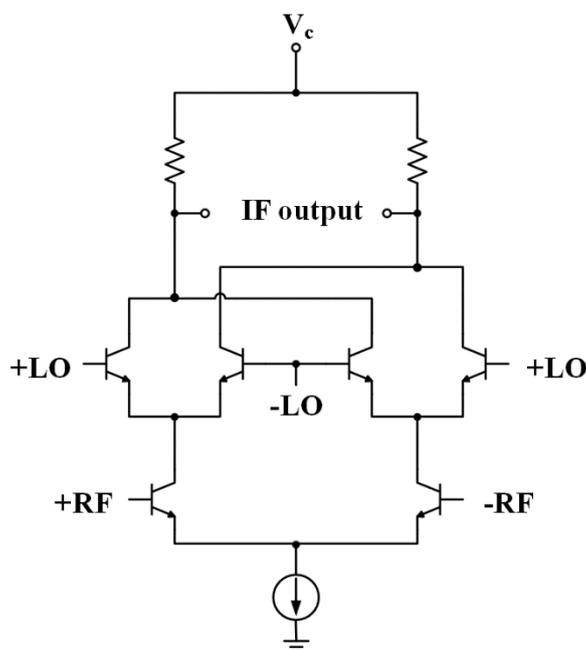


Fig. 3.13. Basic bipolar Gilbert-cell mixer.

3.3.2 Topologies of Sub-Harmonic Gilbert Mixer

As the operating frequency increases into millimeter/sub-millimeter wave frequency ranges, generation of sufficient high LO power is a challenging task. Therefore, the sub-harmonic mixer (SHM) is especially interesting because the LO frequency is only half of the frequency needed for a fundamentally pumped type.

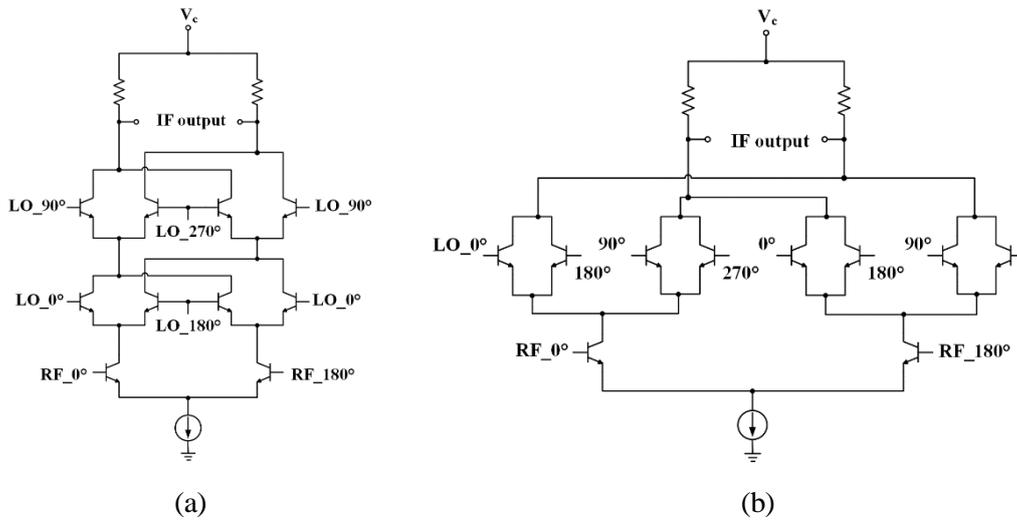


Fig. 3.14. Topology of (a) the stacked-LO sub-harmonic Gilbert mixer and (b) the leveled-LO sub-harmonic Gilbert mixer.

The most popular topologies for sub-harmonic Gilbert mixers are the stacked-LO configuration and the leveled-LO configuration. Fig. 3.14 (a) shows the simplified topology of the stacked-LO sub-harmonic Gilbert mixer. It is composed of two upper LO stages of a double-balanced switching cell and a lower RF stage of a differential pair. When the switching phases are offset by 90° , the two stages of double-balanced switching cell will double the LO frequency effectively [75]. Fig. 3.14 (b) shows the simplified topology of the leveled-LO sub-harmonic Gilbert mixer. It consists of four cross-connected transistor pairs at the upper LO level and one transistor pair at the lower RF level. The LO is applied in quadrature at around half of the RF frequency. By feeding the LO signals with a large enough amplitude, the upper transistors work as a mixer by commutating the RF current at twice the LO input frequency [76].

Both topologies have been investigated and compared in [77]. The stacked-LO configuration requires a smaller LO pumping power at the expense of a greater supply voltage and degraded noise performance. Since the upper LO level transistors are stacked in a cascode type, the $2f_{LO}$ to the RF port leakage is suppressed. Therefore, the stacked-LO structure is claimed to be the best topology to achieve the highest $2LO$ -to-RF isolation. In a leveled-LO sub-harmonic Gilbert mixer, the mixing operation is based on the transistor's nonlinearity, so it can potentially operate at higher frequency but requires larger LO pumping power.

3.3.3 Design and Evaluation of a 340 GHz Receiver Front-End with Integrated 2×2 Patch Array

As is mentioned in Chapter 1, THz frequencies are especially interesting for standoff imaging applications due to their unique properties. However, a combined effect from absorptions, distortions, attenuation and the relative weakness of spectral features in the reflection makes the THz spectra difficult to use in practical applications [78]. At the expense of reduced spatial resolution or increased optical system size, the lower end of the

THz frequency range (e.g. frequency band at ~340 GHz) seems more promising for standoff imaging applications [78]-[79].

In Teledyne’s 250 nm InP DHBT process, which shows an f_i of 375 GHz and an f_{max} of >650 GHz, circuits and even integrated system (e.g. fully integrated transmitters and receivers) at ~340 GHz frequency band can be realized. Therefore, a 340 GHz integrated receiver, which consists of a sub-harmonic Gilbert mixer, an IF differential amplifier, and a 2×2 patch array, is designed and fabricated in this technology.

Fig. 3.15 shows the schematic of the integrated 340 GHz Gilbert mixer and differential IF buffer amplifier. The leveled-LO sub-harmonic Gilbert mixer topology is adopted due to its higher operating frequency, as is discussed in the previous section. The smallest available transistor ($0.25 \times 3 \mu\text{m}^2$) is chosen for both the upper LO level and lower RF level. The quadrature-phase LO is generated by a simple combination of a Marchand balun [80] followed by two branch-line hybrids [81]. The differential IF buffer amplifier consists of three transistor stages, in which the second stage is the core for power amplification and the first and third stages improve the matching.

In order to achieve a compact integration, a differential patch antenna is designed to

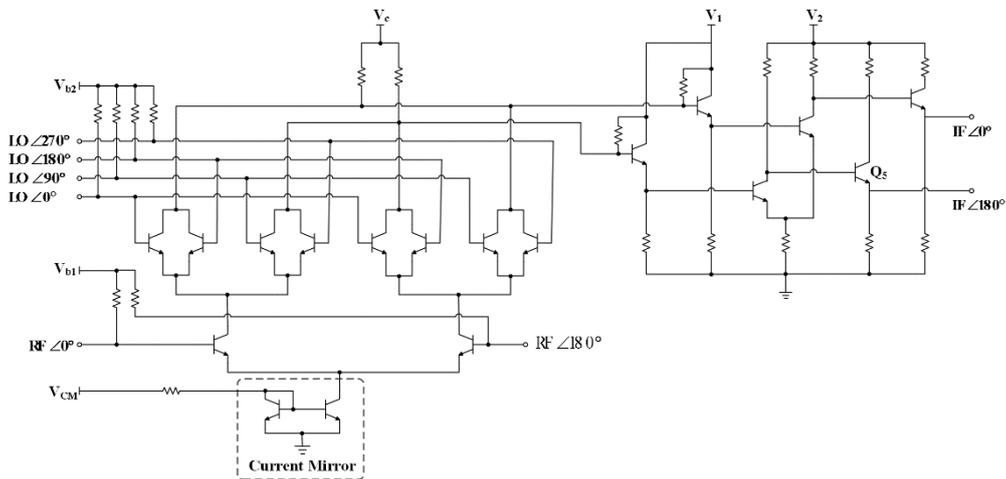


Fig. 3.15. Schematic of the integrated 340 GHz subharmonic Gilbert and differential IF buffer amplifier.

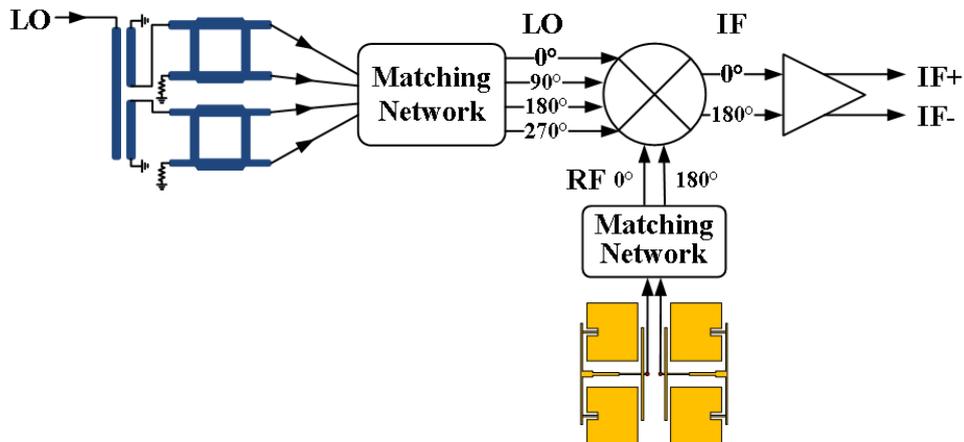


Fig. 3.16. Block diagram of the integrated receiver.

feed out-of-phase RF signals into the mixer. Therefore, no additional RF balun is needed. Fig. 3.16 shows the block diagram of the 340 GHz integrated receiver, and the chip photo is shown in Fig. 3.17. The single-ended LO port, differential IF ports, and dc bias ports are designed with on-wafer pads. The whole chip occupies an area of $1680 \times 1840 \mu\text{m}^2$ and consumes 472 mW dc power out of which 55 mW is consumed by the mixer.

Similar to before, a complete Tx/Rx link is set up to characterize the designed receiver front-end. Fig. 3.18 shows the photo of the measurement setup. The receiver chip is glued onto a small piece of brass block and further mounted at the opening of a big piece of aluminum board, which has been attached on an optical table. Probe manipulators with a magnet underneath are mounted on the same optical table to enable the on-wafer probing. A WR-03 conical horn is connected with the built transmitter chain to illuminate the on-chip antenna with RF signals. The alignment of the two antennas is obtained by the fine-tuning x-y scanner which is mounted on the top plate.

In this work, G_{RX} is defined as the receiver gain, which incorporates the conversion

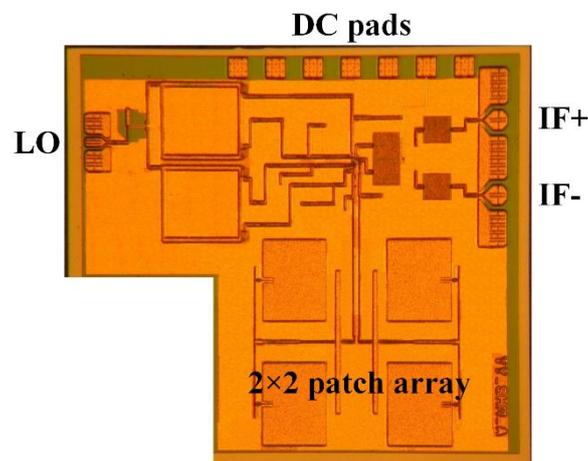


Fig. 3.17. Chip photo of the integrated receiver (Size: $1680 \times 1840 \mu\text{m}^2$)

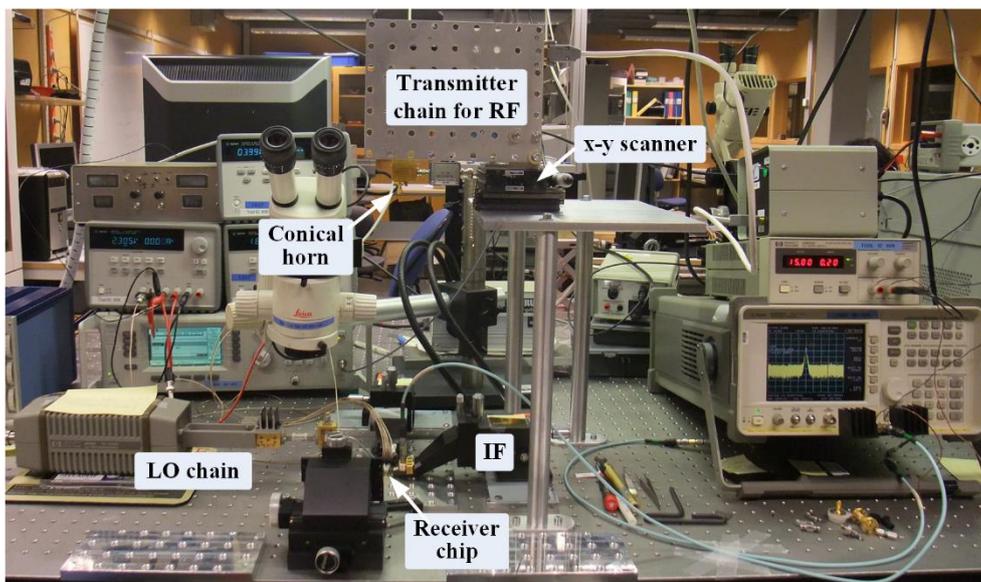


Fig. 3.18. Photo of the measurement setup.

gain of the mixer, the gain from IF buffer amplifier and the antenna gain referred to an isotropic antenna, and $G_{c,circuit}$ is defined as the conversion gain of the down-converter circuit, where the on-chip antenna gain (G_t) is excluded from G_{RX} . Limited by the measurement setup, the RF signal can only sweep up to 338 GHz. Therefore, double sideband performance at 160 GHz LO and the lower sideband performance at 170 GHz LO, with a maximum available LO power of ~ 4 dBm on-chip applied, are characterized by measuring the output power from one of the IF ports. Fig. 3.19 shows the measured results. A peak G_{RX} of ~ 12 dB and a peak $G_{c,circuit}$ of ~ 14 dB are obtained at 170 GHz LO and 338 GHz RF. The gain slope is mainly due to the limited bandwidth of the IF buffer amplifier.

The double-sideband noise figure (DSB-NF) of the receiver is calculated from the direct noise measurement method [82]. A typical noise figure of 17 dB is obtained.

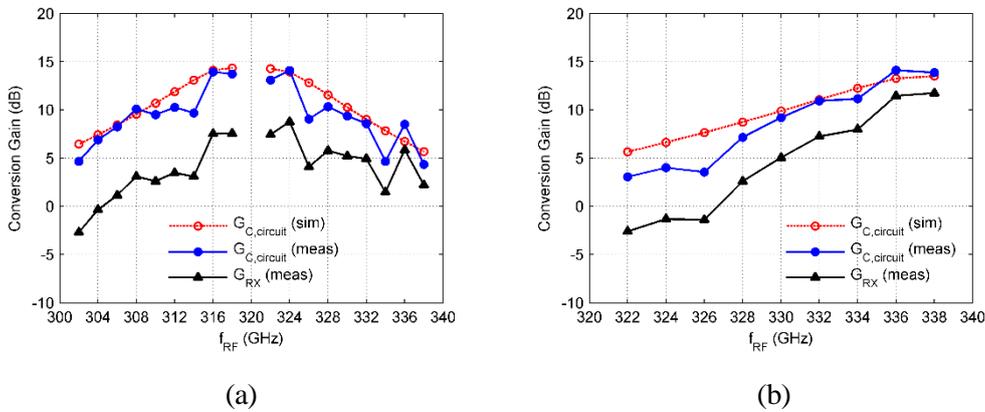


Fig. 3.19. Measured conversion gain (from single IF output port) of the down-converter circuit and the conversion gain of the receiver at (a) $f_{LO} = 160$ GHz, and (b) $f_{LO} = 170$ GHz.

3.4 Transconductance Mixer

3.4.1 Principle of Transconductance Mixer

In a transconductance mixer, the transistor is biased to provide transconductance, and possibly amplification for the RF and LO signals applied to the input base or gate terminal of the transistor [83]. Fig. 3.20 shows a simplified schematic of a single-ended transconductance mixer. The transistor is biased around the turn-on voltage, similar to that of a class-B amplifier, with the transfer characteristic shown in Fig. 3.21. As the LO input drives the base, the transistor switches on along the load line during the positive voltage swings. Thus the transconductance waveform will have the same frequency as the LO. Therefore, $g_m(t)$ can be written as

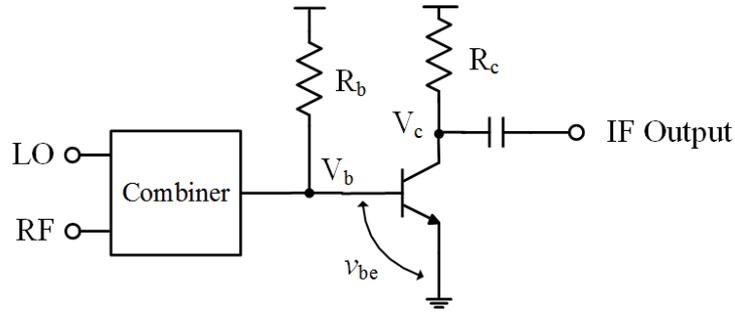


Fig. 3.20. Schematic of a single-ended transconductance mixer.

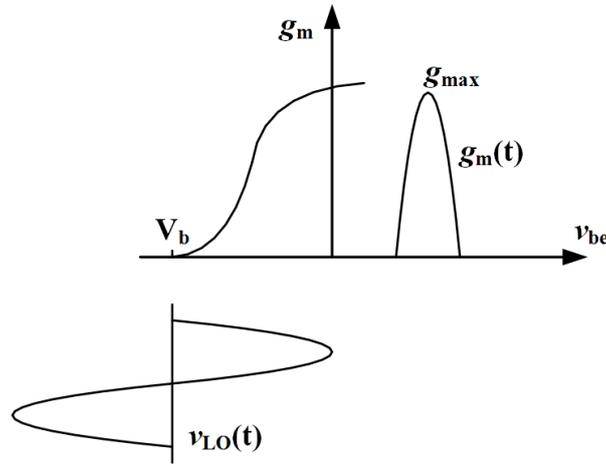


Fig. 3.21. Transfer characteristic of a transconductance mixer.

$$g_m(t) = g_0 + g_1 \cos(\omega_{LO}t) + g_2 \cos(2\omega_{LO}t) + g_3 \cos(3\omega_{LO}t) + \dots \quad (3.2)$$

As the small-signal RF voltage is applied to the base, the collector current will be

$$\begin{aligned} i(t) &= g_m(t) \cdot v_{RF}(t) \\ &= g_0 V_{RF} \cos(\omega_{LO}t) \\ &\quad + \frac{g_1}{2} V_{RF} [\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t] \\ &\quad + \dots \end{aligned} \quad (3.3)$$

Then the IF signal, which is represented by $\frac{g_1}{2} V_{RF} \cos(\omega_{RF} - \omega_{LO})t$, can be selected by an output IF filter.

For optimal conversion gain, the base-emitter junction of a fundamentally pumped

transconductance mixer is biased around the turn-on voltage, where a 50% duty-cycle of the transconductance waveform is obtained. For an arbitrary harmonic mixer, the optimal duty-cycle of the transconductance waveform is $1/2n$, where the integer number n is equal to the order of harmonic that is used for mixing. In reality, the duty-cycle of the transconductance waveform can be controlled by varying dc bias at the base-emitter junction. More details of this design rule can be found in paper [D].

3.4.2 Design and Evaluation of a 110-170 GHz Multi-Mode Transconductance Mixer

At the atmospheric window around 145 GHz, a relatively broad frequency band (141~148.5 GHz) has recently been allocated for fixed and mobile communication [84]. As several semiconductor manufacturing technologies have achieved over 500 GHz or even 1 THz f_t/f_{\max} , it is feasible to design circuits in the ~145 GHz frequency band. In the Teledyne 250 nm InP DHBT technology, a typical $4 \times 0.25 \mu\text{m}^2$ HBT demonstrates an f_t of 375 GHz and an f_{\max} of >650 GHz. From the receiver point of view, key components (LNAs and mixers) with relative high performance should be realizable in such a technology. In many wireless communication systems, dc power consumption is also important. For a traditional receiver architecture, the LO chain often consumes a large portion of the dc power. As the operation frequency increases into the millimeter wave range, the LO chain becomes more bulky. By using a harmonic ($\times 2$, $\times 3$, $\times 4 \dots$) mixer, the LO-generation is simplified at the expense of mixer performance. In the given 250 nm InP DHBT technology, a 145 GHz well-performed LNA can be expected to compensate the mixer noise, and the conversion gain of the mixer can be easily increased by adding an IF amplifier. Therefore, a transconductance mixer, which can be pumped at multiple LO harmonic mixing modes, is designed and characterized for the next generation of high-speed communication.

The schematic is shown in Fig. 3.22. A single-balanced topology is used in order to suppress the second-order intermodulation (IM2). The two identical branches are fed with in-phase LO and differential RF signals. The two IF outputs are out-of-phase and can be combined by an off-chip balun. Looking into either one of the two identical branches, transistors Q_1 and Q_2 are biased in class-A condition and work together as a broadband active power combiner for RF and LO signals. The transistor Q_3 is the transconductance mixer transistor. Its base-emitter junction is biased depending on the order of harmonic mixing mode. A large transistor ($0.25 \mu\text{m} \times 10 \mu\text{m} \times 2$ finger) is chosen for Q_4 while it is biased under class-A condition, to make sure that the linearity of the overall mixer will not be deteriorated. The chip photo is shown in Fig. 3.23, and it occupies an area of $1100 \times 750 \mu\text{m}^2$.

Table 3.1 lists the base bias of the mixer transistor (V_{b2} in Fig. 3.22) at different harmonic mixing modes. With the $\times 1$, and $\times 2$ mixing modes, instability was observed in the measurement. To stabilize the circuit, the base bias V_{b2} at the mixing transistor is decreased compared to the ones in the simulation.

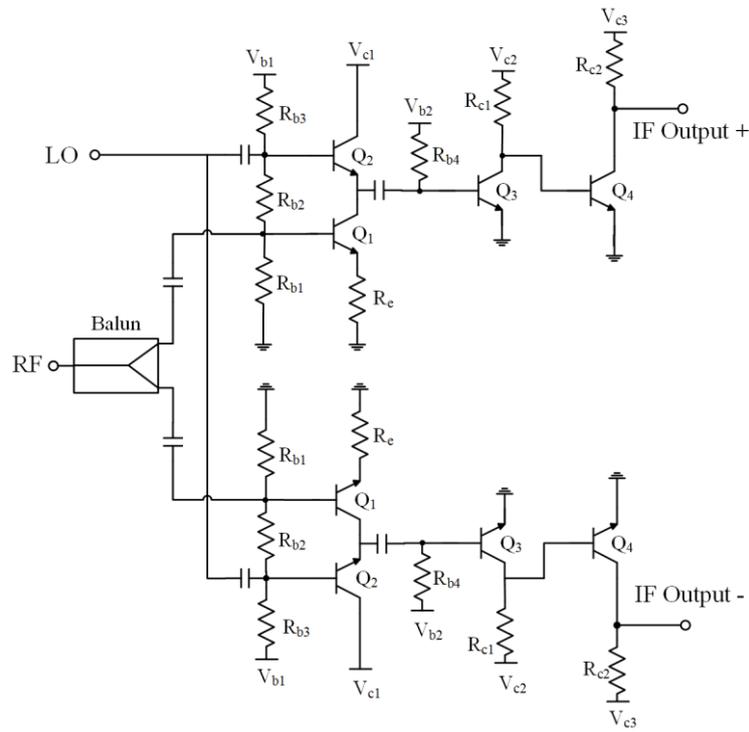


Fig. 3.22. Schematic of the single-balanced D-band mixer.

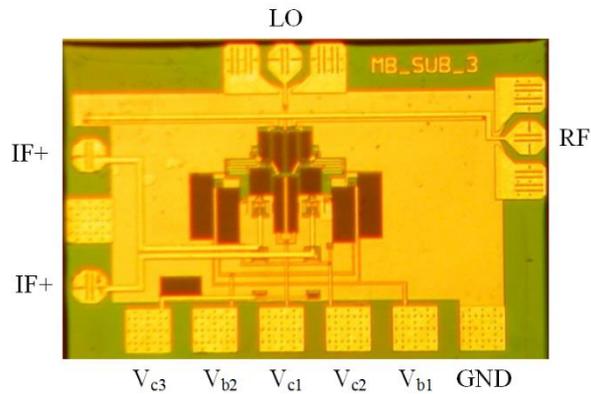


Fig. 3.23. Chip photo of the transconductance mixer. (Size: 1100×750 μm²)

Table 3.1.

BASE BIAS OF THE MIXER CORE

	×1	×2	×3	×4
V_{b2_sim} (V)	0.7	0.6	0.32	0.32
V_{b2_meas} (V)	0.5	0.45	0.32	0.32

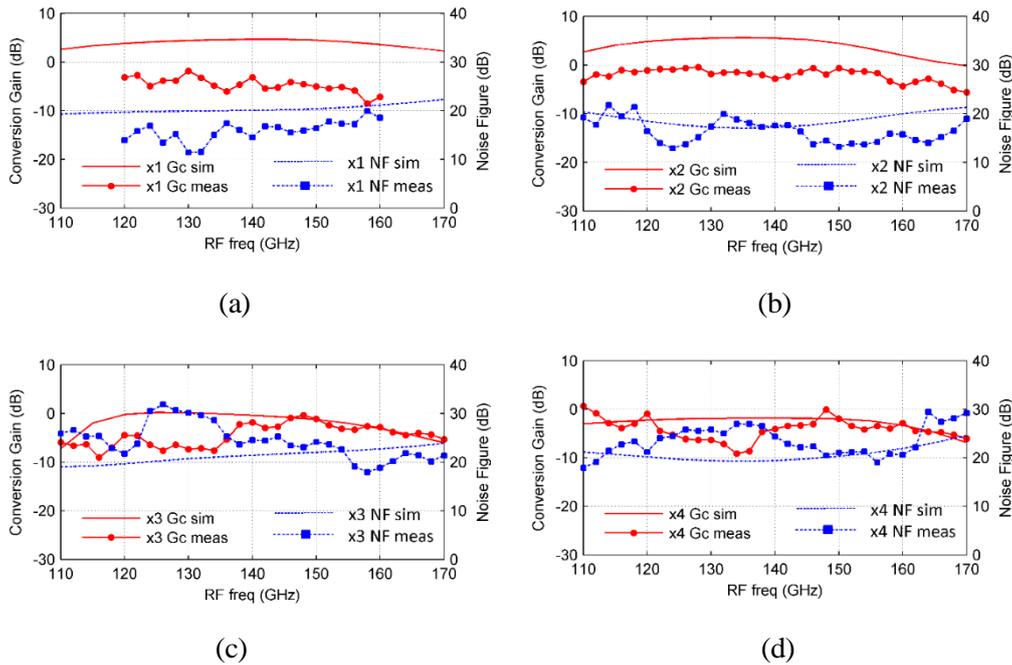


Fig. 3.24. Simulated and measured conversion gain and noise figure as a function of RF frequency at $\times 1$, $\times 2$, $\times 3$, and $\times 4$ LO mixing modes, with the LO power of around 0 dBm, -1 dBm, 5 dBm, and 6 dBm respectively. ($f_{IF}=2$ GHz)

At an IF frequency of 2 GHz, the conversion gain and noise figure are measured versus RF frequencies, as is shown in Fig. 3.24. For $\times 1$ and $\times 2$ mixing modes, the discrepancy between the simulation and measurement is due to the base bias reduction (as is shown in Table 3.1) and the collector current deviation through the Q_4 in Fig. 3.22.

3.5 Discussion

In this chapter, four frequency converter topologies are described. Aiming for either high-speed communication or standoff imaging applications, all four topologies are designed and characterized.

Based on the presented works and literature study, the electrical performances of the four mixer topologies are compared in Table 3.2. In general, a self-oscillating mixer is cost effective in terms of compact size (considering the LO is applied by itself) and relative low dc power consumption [85]-[87]. However, since the dc bias is compromised between an optimized oscillator and an optimized mixer, the other electrical performances (e.g. conversion gain and noise figure) cannot compete with the other traditional mixer topologies.

Resistive mixers use the channel-resistance of FETs to achieve frequency conversion and typically show better linearity than an active mixer. Since the drain is not biased, a resistive mixer consumes virtually zero dc power. However, it normally requires a high LO power to work efficiently. For a single-ended resistive mixer, the LO-to-RF isolation is poor (e.g. 9.3 dB isolation was obtained from the single-ended mixer [88]). However, this can be solved by using a balanced topology in which the LO leakage can be suppressed

Table 3.2.
COMPARISON OF MIXER TOPOLOGIES

	SOM	Resistive mixer	Gilbert mixer	Transconductance mixer
dc power consumption	Low	0	High	Moderate
Conversion gain	Low	Low	Moderate~High	Moderate~High
Noise figure	Poor	Moderate	Moderate	Moderate~Good
Bandwidth	Poor	Good	Moderate~Good	Moderate~Good
Linearity	Poor	Good	Moderate	Moderate
LO power	0	High	Low~Moderate	Low~Moderate
Port isolation	Poor~Moderate	Poor (single-ended) Good (balanced)	Good	Poor (single-ended) Good (balanced)
Design complexity	Moderate	Low	High	Low~Moderate

intrinsically because the LO signals at the two gates are 180° out-of-phase. By comparing the presented resistive mixers, the LO-to-RF isolation from the single-balanced topology is improved by 30 dB compared to the single-ended one. However, since two transistors are working for frequency conversion in a single-balanced mixer, higher LO power would be needed.

Gilbert mixers have been very successful since they were invented, and are more suitable in BJT technologies than in FET technologies. Since the Gilbert mixer is doubly balanced, it has delightful properties such as isolation between all three ports, LO AM noise suppression, and rejection of all spurious responses with odd LO harmonics (for sub-harmonic mixer). Typically, Gilbert mixers can achieve a moderate to high conversion gain but relatively poor linearity. As the working frequency increases, a Gilbert cell can be modified, e.g. the stacked-LO configuration and the leveled-LO configuration, to operate as a sub-harmonically pumped mixer.

Transconductance mixers, which utilize the time varying transconductance of BJTs, feature a simple topology compared to a Gilbert mixer. It is feasible to be pumped in an arbitrary harmonic mixing mode without changing the topology. Since the noise of a mixer consists of the internal noise generated by the mixer device itself and the noise converted from all the harmonics' ports, by increasing the order of the harmonic mixing mode, the local oscillator (LO) frequency can be decreased at the expense of the higher noise figure.

Chapter 4

A 110-170 GHz Transceiver for FMCW Applications

The frequency modulated continuous wave (FMCW) radar is widely used in applications such as automotive anti-collision, maritime navigation, aircraft navigation, etc. In this chapter, the principle of a basic FMCW radar is introduced. Aiming at a standoff imaging array with a sub-cm range resolution, a 110-170 GHz transceiver is presented for FMCW applications.

4.1 Principle of FMCW Radar for Range Measurement

The FMCW radar is a special type of continuous wave (CW) radar [89]. Aiming for measuring range and velocity, the transmitted signal is modulated in frequency, and the modulation can be different, e.g. triangle wave, sawtooth wave, sine wave, and square wave. The most common method is to modulate the frequency of a continuous wave in a linear manner. As is shown in Fig. 4.1 (a), the transmitted signal is shown by the solid triangular waveform, with a modulation rate of f_m and a frequency sweeping bandwidth of B_{sweep} . The dashed waveform represents the received echo signal from a stationary target. When the transmitted signal is taken as a reference, the time when the echo signal arrives back at the radar can be represented by:

$$t_b = \frac{2R}{c} \quad (4.1)$$

where

- R represents the range to the target;
- c is the speed of light.

When the received echo signal is mixed with the transmitted one, a beat frequency f_b is generated, as is shown in Fig. 4.1 (b). From the geometry of Fig. 4.1 (a), f_b can be expressed as:

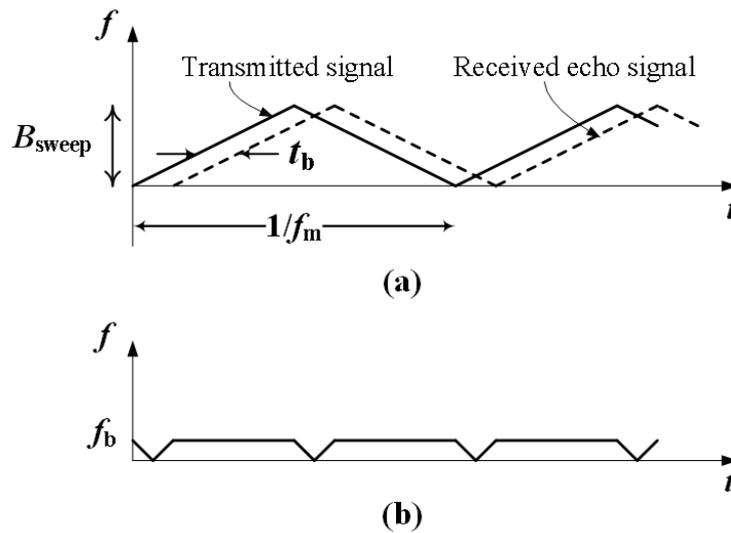


Fig. 4.1. (a) Frequency vs. time in a FMCW radar with linear triangular frequency modulation. (b) Beat frequency vs. time.

$$f_b = 2f_m \times B_{sweep} \times t_b = \frac{4Rf_m B_{sweep}}{c} \quad (4.2)$$

4.2 Design of a 110-170 GHz Transceiver for FMCW Applications

In a conventional FMCW radar front-end, the receiver path and transmitter path are separated all the way through the antenna [90]-[95], or share one antenna by introducing either a circulator [96]-[97] or a hybrid [98]-[99]. For reasons of simplicity and low dc power consumption, an FMCW radar transceiver, which operates as both transmitter and receiver, was demonstrated in [100]. Then, in the microstrip technology, a single-ended transceiver, which uses only one transistor and several passive components, is published for ~10 GHz FMCW radar applications [101], and followed by a balanced version with improved AM noise suppression [102].

For standoff imaging applications, Jet Propulsion Laboratory (JPL) has developed three generations of FMCW imaging radars at frequencies above 500 GHz [93]-[95]. In order to separate the transmitted and received signal in their radars, a beam splitter is used, however, this introduces a round-trip loss of at least 6 dB. In order to overcome the 6 dB additional loss from the beam splitter and again simplify the Tx/Rx chains, an integrated FMCW radar transceiver module, which uses GaAs Schottky diode technology and has the transmitter and receiver as a single unit, is demonstrated at 200-240 GHz [103]. In reality, a single transceiver is not enough to provide the necessary frame rate for real-time standoff imaging, so an array of transceivers is needed. Therefore, making an array in monolithically integrated circuit technologies is more efficient in terms of space and cost

compared to stacked single transceivers in waveguide technologies.

To allow future production in high volume, a balanced 110-170 GHz transceiver is designed, utilizing a SiGe BiCMOS technology. Fig. 4.2 shows the schematic of the transceiver. The transistors are biased under class-AB condition. Therefore, they operate as amplifiers for transmitting and simultaneously as fundamentally pumped down-converter mixers for receiving. When the circuit works as a receiver, the input signal serves as the LO and the returned signal back into the output port serves as the RF. The two branches are fed through a 90° hybrid and further combined by a second 90° hybrid. Thus the transmitted signals from the two branches are in-phase at the output. At the differential IF ports, a commercial transformer is connected to obtain a single-ended output, and its center tap is used to apply collector dc bias. The chip photo of the transceiver is shown in Fig. 4.3, with a size of $980 \times 560 \mu\text{m}^2$.

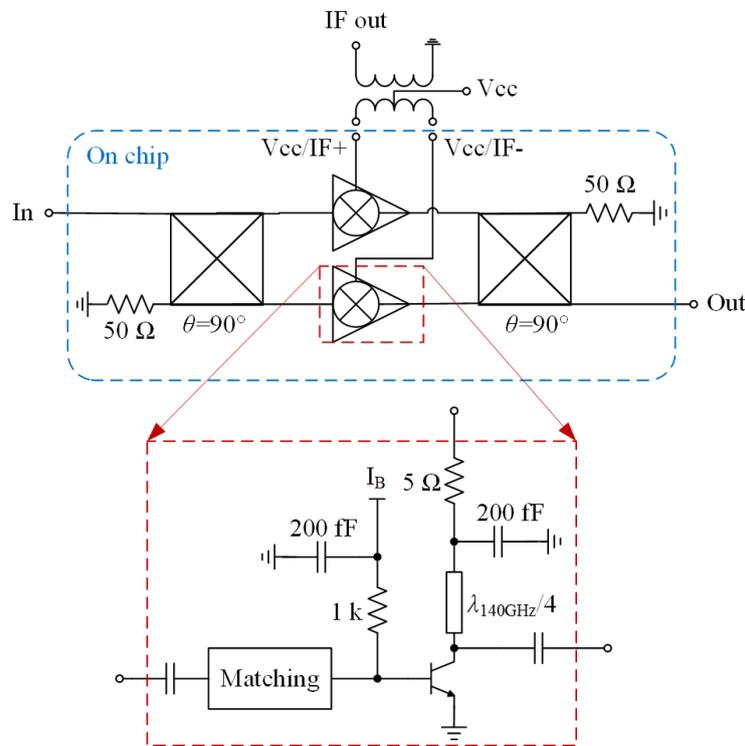


Fig. 4.2. Schematic of the balanced transceiver.

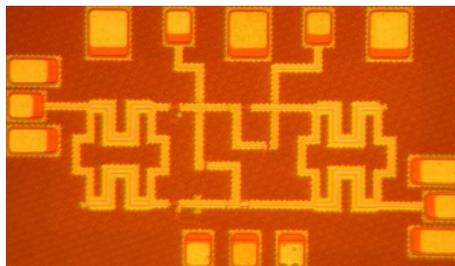


Fig. 4.3. Chip photo of the transceiver (chip size: $980 \times 560 \mu\text{m}^2$).

4.3 Experimental Results

The designed transceiver is characterized by on-wafer probed measurements on circuit level, and in addition also demonstrated as a FMCW radar for distance measurement.

4.3.1 Circuit Measurement

The transceiver is characterized as an amplifier and as a down-converter mixer. After terminating the IF port by a $50\ \Omega$ matched load, the two-port small signal S-parameter is measured, as shown in Fig. 4.4 (a). Since the transistors are not biased for an optimal amplifier, very little power gain is achieved from simulation while a ~ 4 dB lower value is obtained in the measurement. However, in our applications, the maximum output power is more crucial for a transmitter. It is observed from measurements that more than 0 dBm output power can be obtained when an input power of +3 dBm is applied. Under the same bias condition as a transmitter, the circuit is also measured as a receiving down-converting mixer. With an LO power of approximately 3 dBm, the measured conversion gain is shown in Fig. 4.4 (b). The IF frequency is limited to 300 MHz by the off-chip transformer. With an LO frequency of 130 GHz, a typical conversion gain of -9 dB is obtained. The noise performance of the mixer is evaluated by measuring the IF noise power. A noise figure of 19 dB is achieved with an LO frequency of 130 GHz.

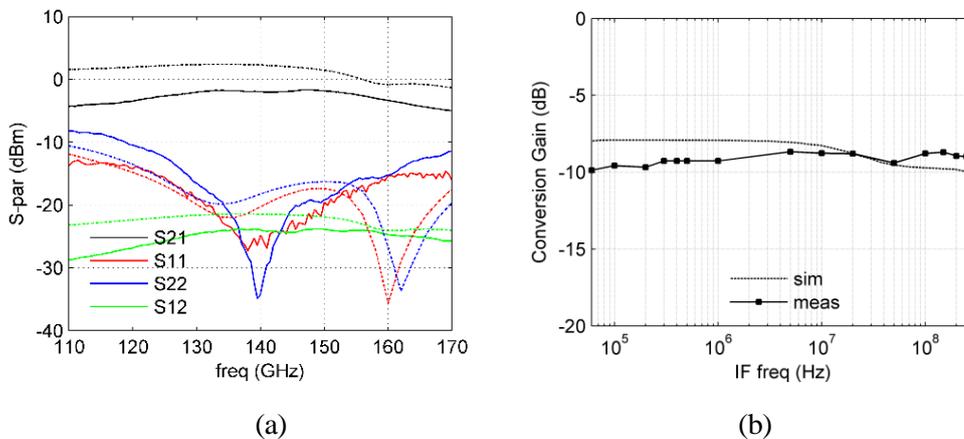


Fig. 4.4. (a) The measured (solid line) and the simulated (dashed line) two-port small signal S-parameter for transmitter. (b) Simulated and measured conversion gain as a function of the IF frequency ($f_{LO}=130$ GHz).

4.3.2 FMCW Radar Measurement

The transceiver is also demonstrated for distance measurement. The FMCW radar measurement setup is shown in Fig. 4.5.

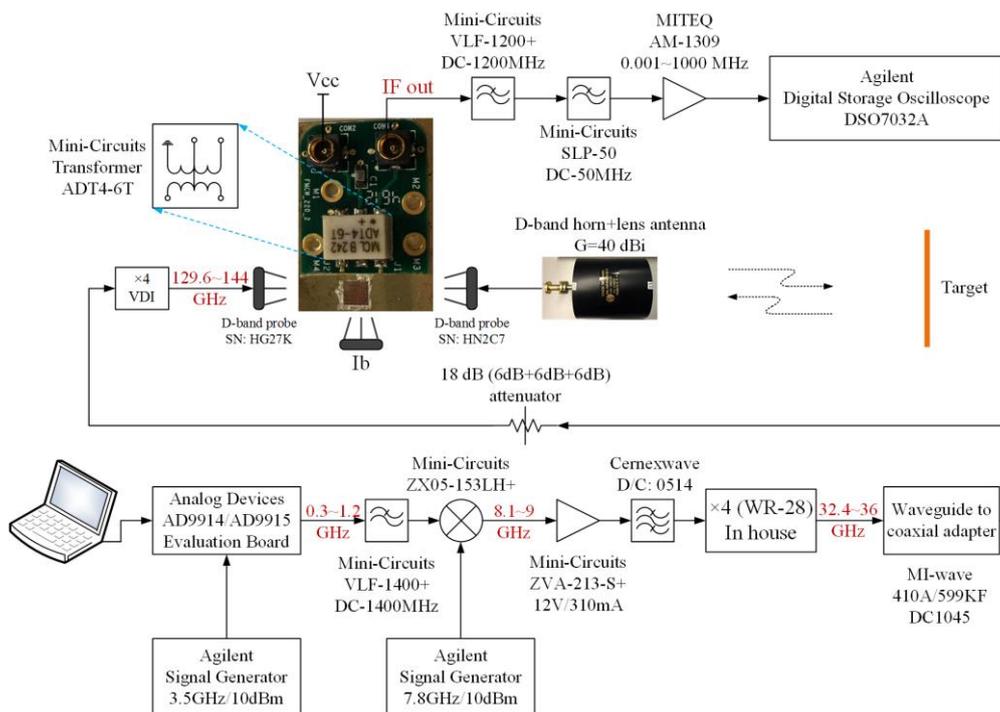
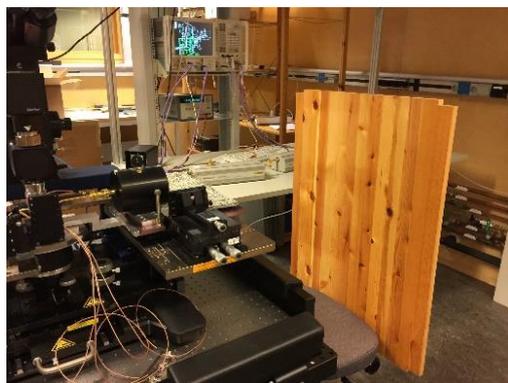
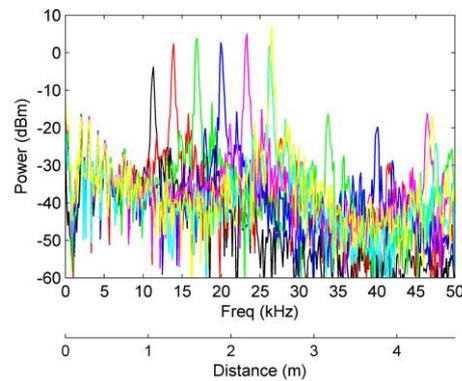


Fig. 4.5. FMCW radar measurement setup.



(a)



(b)

Fig. 4.6. (a) Measurement photo when the target is a big piece of wood; (b) The measured IF spectra when the target is located at different distances from the transceiver.

To demonstrate the capability of measuring distance, a piece of wood is placed in front of the antenna, as is shown in Fig. 4.6 (a). Fig. 4.6 (b) shows the IF spectrum when placing the target at different distances from the radar transceiver, and the second x-axis shows the corresponding distance according to the IF frequency.

With the aim of demonstrating the range resolution, cardboard boxes with different thicknesses are chosen as the targets. Therefore, the two cardboard layers from one box should be recognized as two targets in the wave propagation direction. Fig. 4.7 shows the IF spectra with different layer distances. It can be seen that the two targets (cardboard layers) can be well distinguished between each other when the distance is more than 10

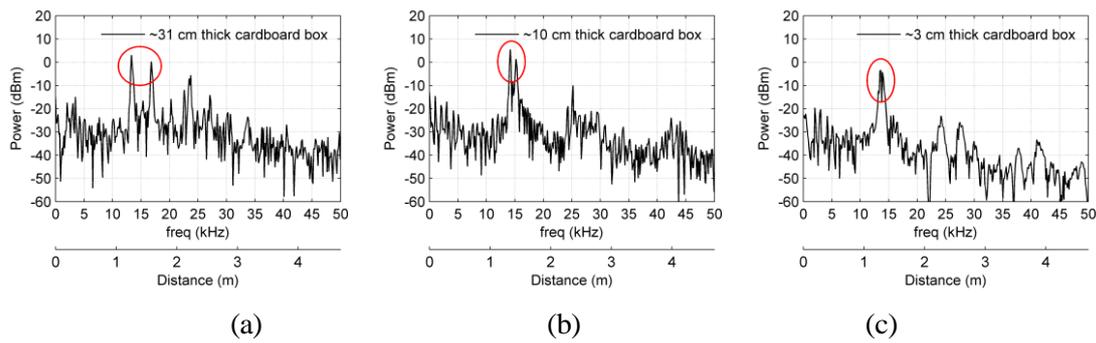


Fig. 4.7. The IF spectra when the target is (a) 31 cm thick cardboard box; (b) 10 cm thick cardboard box; (c) 3 cm cardboard box.

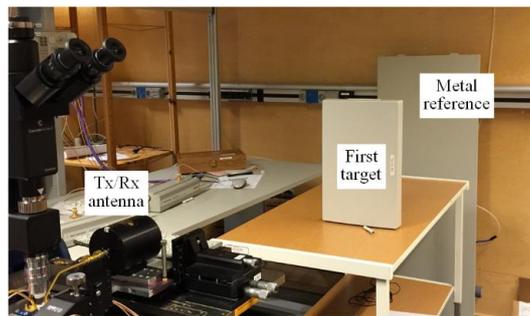


Fig. 4.8. Photo of penetration test.

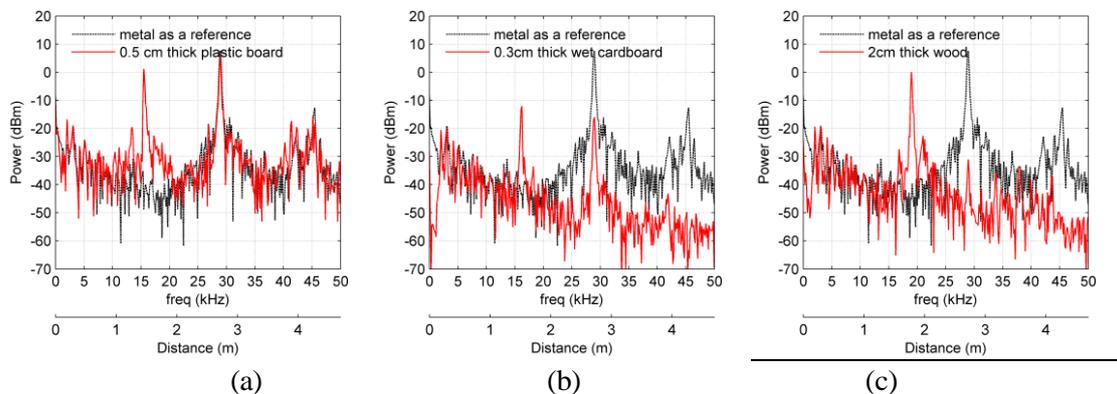


Fig. 4.9. Measured IF spectra of just metal target as a reference and when the first target is (a) a 0.5 cm thick plastic board, (b) a 0.3 cm thick wet cardboard, and (c) a 2 cm thick wood.

cm. With a range difference of 3 cm, two peaks can still be recognized from the IF spectra, as is shown in Fig. 4.7 (c), but are very close to each other. So the range resolution of such a radar setup is better than 3 cm.

A penetration test is also carried out on different materials while a piece of metal is placed on the backside as a reference, as is shown in Fig. 4.8. A plastic board, a piece of wet cardboard and a piece of wood have been alternatively placed as the first target in front of the Tx/Rx antenna. Fig. 4.9 shows the measured IF spectra of the three cases. It can be seen that the ~140 GHz signal penetrates through a 0.5 cm thick plastic board with barely any loss, while a 0.3 cm thick piece of wet cardboard and a 2 cm thick piece of wood show around 20 dB loss and 40 dB loss in a return path, respectively.

Chapter 5

Conclusions

In this thesis, millimeter and sub-millimeter wave frequency converters are studied as possible candidates for the next generation of high-speed communication and standoff imaging applications. State-of-the-art semiconductor manufacturing technologies, which include a 100 nm GaAs mHEMT technology, a 250 nm InP DHBT technology, and a 130 nm SiGe BiCMOS technology, are employed for circuit designs. In chapter 3, the self-oscillating mixer, the resistive mixer, the Gilbert mixer, and the transconductance mixer are described. Circuits based on those mixer topologies are designed and characterized at, or aiming at, the ~ 145 GHz frequency range, ~ 220 GHz frequency range, or ~ 340 GHz frequency range. From the measurement results, these mixers are suitable candidates in given technologies to be further integrated with other components.

In chapter 4, a 110~170 GHz novel transceiver is designed and manufactured for standoff imaging applications. It is successfully demonstrated in a FMCW radar setup for distance measurement. This circuit is planned to be packaged into a waveguide module and employed in an imaging scanning system. Furthermore, the design is planned to be scaled to 220 GHz and 340 GHz.

Appendix

Noise Figure Measurements

The noise figure is an important factor from a system perspective. It measures the amount of noise added by a component, and is defined by the ratio of the input signal-to-noise ratio (SNR) to the output SNR, or more often by the ratio of the total available noise power at the output to the output available noise power due to thermal noise originating from the input resistor at standard room temperature [104]. The noise can be quantified by either the equivalent noise temperature (T_e) or the noise factor (F), and they can be interconverted by:

$$T_e = T_0(F - 1) \quad (\text{A.1})$$

In communication fields, the noise figure (NF) in dB, which is $10\log F$, is often preferred.

A.1 Traditional Noise Figure Measurement Methods

Traditional noise figure measurement methods include the direct noise measurement method, the Y-factor method and the signal generator twice-power method [82]. Representing the device under test (DUT) in Fig. A.1, where

- G is the power gain in linear scale.
- T_e is the equivalent noise temperature, which is to be measured.
- B is the equivalent noise bandwidth.

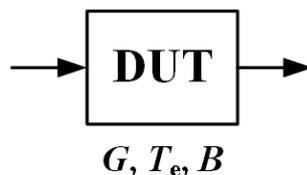


Fig. A.1. Block diagram of a DUT represented by its power gain (G), equivalent noise temperature (T_e), and equivalent noise bandwidth (B).

Table. A. 1.

TRADITIONAL NOISE FIGURE MEASUREMENT METHODS

	Noise temperature	Noise factor (linear scale)	Parameters should be known	Limitations at mm/sub-mm wave
Direct noise power method	$T_e = \frac{P_N}{kBG} - T_0$	$F_{DUT} = \frac{P_N}{kT_0BG}$	* P_N, G, B	Active DUT with moderate to high NF
Y-factor method	$T_e = \frac{T_{hot} - YT_{cold}}{Y - 1}$	$F_{DUT} = \frac{T_{hot} - YT_{cold}}{(Y - 1)T_0} + 1$	# $T_{hot}, \$T_{cold},$ * Y	Low to moderate (<10 dB) NF
Twice- power method	$T_e = \frac{P_{gen}}{kB} - T_0$	$F_{DUT} = \frac{P_{gen}}{kT_0B}$	* P_{gen}, B	Active DUT with high NF

$k=1.38 \times 10^{-23}$ J/K is the Boltzmann constant.

$T_0=295$ K is the standard room temperature in Kelvin.

* P_N is the measured output noise power.

$T_{hot}=295$ K (standard room temperature) is the hot temperature in Kelvin.

\$ $T_{cold}=77$ K (temperature of liquid nitrogen) is the cold temperature in Kelvin.

* Y is the ratio of the measured output noise power when the input is terminated by a matched load at T_{hot} and T_{cold} .

* P_{gen} is the power of the input continuous wave signal when the total measured output power is twice as the output noise power only.

Table. A. 1 lists the properties of the traditional methods. As can be seen from the limitations at the millimeter/sub-millimeter wave range, none of the traditional methods would work nicely for a relative high noise figure component, which has no gain and nearly passive, e.g. resistive mixers. Therefore, based on the signal generator twice-power method, the signal generator N-times power method is proposed.

A.2 Signal Generator N-Times Power Method

Fig. A.2 shows the working principle of the signal generator N-times power method. The output noise power is first measured when the input port is terminated by a matched load at the standard room temperature, and represented by P_1 :

$$P_1 = k(T_0 + T_e)BG \quad (\text{A.2})$$

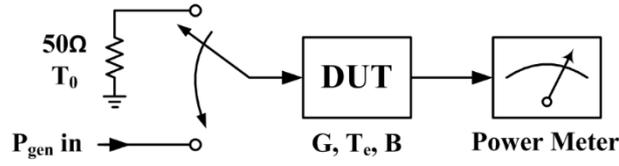


Fig. A.2. The signal generator N-times power method.

Then the input is fed with a continuous wave signal, which is within the bandwidth of the DUT. With a certain input power of P_{gen} , the output power can be measured and represented by

$$P_2 = k(T_0 + T_e)BG + P_{gen}G \quad (A.3)$$

The N factor is defined as

$$N = \frac{P_2}{P_1} \quad (A.4)$$

Substituting eq. (A.2) and eq. (A.3) into eq. (A.4), the equivalent noise temperature can be expressed by

$$T_e = \frac{P_{gen}}{kB(N-1)} - T_0 \quad (A.5)$$

And the noise factor is:

$$F_{DUT} = \frac{P_{gen}}{kT_0B(N-1)} \quad (A.6)$$

So far, the dynamic range of a power meter is very much limited at frequencies above 100 GHz, e.g. $\sim 1 \mu\text{W}$ from an Erickson power meter [105]. Therefore, the proposed signal generator N-times power method is especially beneficial, because the input P_{gen} can be an arbitrary amount of power.

Summary of Appended Papers

Paper A

24 GHz Balanced Self-Oscillating Mixer with Integrated Patch Antenna Array

This paper presents the design and characterization of a 24-GHz self-oscillating mixer integrated with a 16 element quadratic microstrip patch array. It has been demonstrated as a receiver front-end without any additional local oscillator supply. I contributed with the design, simulation and measurement of the SOM circuit part while the patch array antenna was designed by Y. B. Karandikar, radar measurement together with Y. B. Karandikar, and writing of the paper.

Paper B

Monolithically Integrated 200-GHz Double-Slot Antenna and Resistive Mixers in a GaAs-mHEMT MMIC Process

This paper presents the design and characterization of a single-ended and a balanced 200-GHz integrated resistive mixer with double-slot antenna in a 100 nm GaAs-mHEMT technology. A novel method is also proposed and proved to evaluate a moderate to high noise figure device in millimeter/sub-millimeter frequency band. The mixers were originally designed by Sten E. Gunnarsson and Bahar M. Motlagh, and the antenna was originally designed by Bahar M. Motlagh under supervision from Sergey Cherednichenko. I contributed with circuit re-simulation, characterization together with Y. B. Karandikar, idea and experimental validation of the novel noise figure measurement method with Y. B. Karandikar, and writing of the paper.

Paper C

340 GHz Integrated Receiver in 250 nm InP DHBT Technology

This paper presents a 340 GHz integrated receiver, which consists of a sub-harmonically pumped Gilbert mixer, a differential IF buffer amplifier, and a 2×2 differential patch array antenna, in a 250 nm InP DHBT technology. This work demonstrated the first integrated receiver above 300 GHz in such technology. The antenna was designed by Y. B. Karandikar. I contributed with the design and simulation of the Gilbert mixer and IF amplifier, measurements together with Y. B. Karandikar, and writing of the paper.

Paper D

A 110-170-GHz Multi-Mode Transconductance Mixer in 250-nm InP DHBT Technology

This paper presents a 110-170 GHz multi-mode transconductance mixer in a 250 nm InP DHBT technology. It is successfully demonstrated as a $\times 1$, $\times 2$, $\times 3$, and $\times 4$ harmonic mixer. In order to understand how the mixer should be biased at different harmonic mixing modes, an arbitrary harmonically pumped transconductance mixer is described. The circuit was originally designed by Mingquan Bao. I contributed with the circuit re-simulation, characterisation, theoretical mechanism analysis, and writing of the paper.

Paper E

A 110-170 GHz Transceiver in 130 nm SiGe BiCMOS Technology for FMCW Applications

This paper presents a balanced 110-170 GHz transceiver in a 130 nm SiGe BiCMOS technology for FMCW applications. The designed transceiver operates as an amplifier for transmitting and simultaneously as a down-converter for receiving. The transceiver is successfully demonstrated as an FMCW radar for distance measurement. I contributed with the design and simulation of the circuits, measurements together with T. Bryllert, and writing of the paper.

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The journey towards my PhD has been full of challenges, happiness, and occasional confusions. All those experiences shaped who I am today, and I would like to express my gratitude to the people who have helped me during my PhD study.

I would like to express my deepest gratitude to my supervisor Prof. Herbert Zirath. Looking back over the past six years, I feel so lucky to be one of his PhD students. As a supervisor, he offered me the opportunity to explore the world of monolithic microwave integrated circuit design freely, and supported me with continuous inspiration, encouragement, and guidance. As an employer, he expressed the kindest understanding especially when I was pregnant and on parental leave. Also, I would like to thank my co-supervisor Sten E. Gunnarsson for his valuable suggestions and discussions whenever I had new ideas or got confused in my research. He helped me to make detailed study plans towards my PhD, and always supported me with prompt proofreading.

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