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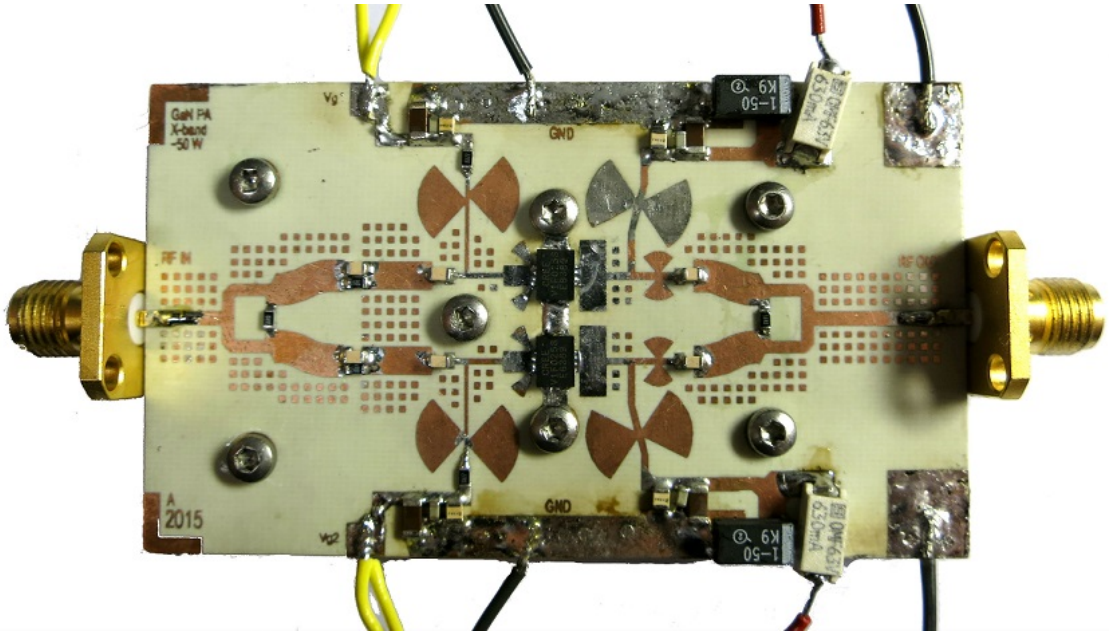

Design of X-band GaN combined power amplifier for radar applications

Master's thesis in Wireless, Photonics and Space Engineering

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Gothenburg, Sweden 2015

Master's thesis 2015

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Cover: Fabricated 50 W X-band power amplifier produced during the project.

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Abstract

Most wireless systems must be able to output a high enough output power to serve their purpose. A power amplifier is often needed in order to amplify the outgoing signal to a decent power level. Power amplifiers can be constructed using a variety of materials and techniques. Most modern amplifiers are constructed using semiconductor materials. Gallium nitride or GaN is a relatively recent semiconductor material used to manufacture high speed transistors that can handle high power levels and withstand high temperature. Smaller and more efficient amplifiers can be constructed if using GaN as compared to using other semiconductor materials.
A surface mount 25 W GaN transistor have been used to construct a prototype of a combined power amplifier. The amplifier was supposed to use two of these transistors in a combined configuration and be able to output 50 W of power at X-band. The design was realized by simulations using a computer based design tool together with a non-linear transistor model. A prototype was then constructed to be able to perform measurements and analyze its performance.
The prototype was able to output up to 50 W of power, but bandwidth and efficiency did not reach the same levels compared to when performing the simulations. Maximum performance was reached at a frequency 350 MHz lower than expected.

Keywords: gallium nitride, power amplifier, power combining

Acknowledgements

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Robert Robinsson, Gothenburg 2015-06-05

Contents

1
Introduction

The need for more efficient electronic circuitry is always evolving [1]. Electronic systems typically consists of several blocks performing different tasks. Some blocks consume more power than others. The efficiency of the entire circuit can be increased if the power consumption of these circuit elements can be decreased.
Microwave circuits are used to generate and amplify RF power for use in a wireless system, i.e. a communication or radar system. A majority of the energy will typically be used by the power amplifier in these systems. It is thus very important to keep the efficiency of the power amplifier high to lower the power consumption of the entire system [2]. The wasted energy will otherwise turn into heat that will have to be conducted away from the circuit using cooling solutions.
A typical radar system operates with high output power in order to increase the range and detection probability of targets [3]. Semiconductor based amplifiers have in the past not been used to achieve very high power levels at high frequency. Vacuum electron devices have instead been used to make amplifiers that can operate at high power levels [4]. One such device is the travelling wave tube (TWT), a big and bulky device that require high voltage to run. They also have a lot of mechanical parts in them that could fail.
Semiconductor devices on the other hand can be small in size and reliable. Research and development in the field of semiconductor devices have enabled fabrication of transistors that could compete with some of the vacuum devices in terms of output power. These breakthroughs in semiconductor research have enabled fabrication of gallium nitride (GaN) based transistors that can be operated at higher power levels [5].
Gallium nitride transistors can operate at high power levels due to their high power density and at high frequency due to the high electron mobility transistor (HEMT) transistor architecture [4]. The development of GaN HEMTs have been rapid and the output power level of a device can be high even at microwave frequencies. This is why GaN devices can outperform other popular semiconductor materials as gallium arsenide (GaAs) and silicon (Si) in terms of power and efficiency [6].
The power level can further be increased by combining multiple transistors in parallel. This requires combining networks to be used that can feed all transistors with the input signal and then sum the signal at the output. GaAs transistors have been used during a longer period, but it is becoming difficult to achieve high power levels with this technique. Multiple transistors have to be combined at once, but losses in the combining network itself will also be higher when the number of devices grow. There is no advantage in combining too many transistors due to this effect, since more and more power will be lost [6]. The combining network must therefore be

optimized to have as small loss as possible to ensure maximum output power.
The transistor must also be matched with using a matching network and supplied with power through a bias network. These three circuit elements together with the transistor itself will form the major parts of the combined microwave amplifier.
There are pre-matched 50 Ω GaN amplifiers blocks available on the market for use as power amplifiers, but their cost is rather high. A more cost effective solution could be to use ordinary unmatched GaN transistors along with a custom combining, matching and bias network designed for them. Output power and efficiency are the most important performance figures if considering requirements for radar applications.

1.1 Purpose

The purpose of the project is to investigate if unmatched GaN transistors can be used to fabricate an X-band power amplifier with output power up to 50 W. The final prototype will be characterized by measurements to see how well it could perform.

1.2 Research questions

A number of questions have been looked into to reach the goal and fulfil the purpose of the project:

- What type of combining network should be used to combine multiple transistors in parallel?
- How can losses in the combining network be minimized?
- What type of matching network should be used?
- How should the transistor be biased?
- How should the bias network be designed?
- What will happen during failure of one or more transistor?
- On what substrate material should the circuit be built on?
- How should oscillations be prevented?
- How small in size can the circuit be?

1.3 Methods

A literature review of the subject was first performed to gain knowledge on how to design the amplifier and its combining networks. Books and research papers have mainly been used to gather information about the topic. The information obtained during this study have been used to decide how the following design project should evolve.
The next step in the project was to perform simulations using a computer based design tool called Microwave Office, a program especially suited for microwave design work. A non-linear model of the transistor have been available for use with the simulation software. Different variants of combining networks have been evaluated in order to find a suitable design for combination of multiple transistors. Individual

components of the amplifier have been simulated as independent modular blocks to a large extent to make the design process less complex. Circuit blocks have then been fitted together to form a complete power amplifier.
A 50 W X-band power amplifier was then constructed using the unmatched transistor. Each transistor is capable of delivering 25 W. The prototype is therefore using two transistors connected in parallel, since usage of more transistors would make the project too complex for practical construction. The prototype has been manufactured as a surface mount board with lumped components and distributed elements on a printed copper circuit board. Measurements on the prototype were performed to investigate how well the performance compared with that of the simulated circuit. The findings of the project have been documented in this report during the entire length of the project to capture the entire process as complete as possible.

1.4 Limitations

The main tool used for the circuit design have been Microwave Office and the supplied transistor model for it. The project has been limited by the capabilities of the software and the model as they are based on assumptions that approximate the real world behaviour of the device.
The project has also been limited by the fabrication techniques available for prototyping. Commercial processes can offer higher quality boards, but the fabrication time needed would have delayed the project. Multiple test boards have been possible to fabricate during the project because of the short manufacturing time.

2
Theory

This chapter will discuss the theory behind the design and construction process of the project. The reader of this section is assumed to have some knowledge regarding basic microwave engineering to be able to follow the concepts presented.

2.1 Semiconductor devices

Semiconductor devices are today very popular for use in electronic devices of all categories. Transistors and diodes are the most common semiconductor based electrical components. They are widely used in digital electronics, but also very frequently used in analog circuits [7]. Microwave circuits require special transistors to be used that can operate at high frequency with reasonable performance.
The transistor is a non-linear three terminal device, i.e. Ohm's law can not be used to analyze the electrical properties of the device. There exists two main types of transistors, the bipolar junction transistor (BJT) and the field effect transistor (FET) [7]. The BJT has a collector, base and emitter terminal. The collector current is controlled by an input current at the base. The FET has a drain, gate and source terminal, but the drain current is instead controlled by a voltage applied to the gate.
The BJT and FET devices can both be found in modern circuits. They are different and there are uses for both of them depending on the application. Modern semiconductor materials like GaN are used to create FET devices, with no bipolar equivalent.
The FET family of devices is itself divided into different categories. The high electron mobility transistor (HEMT) is the semiconductor architecture used when fabricating GaN transistors [4].
The most common use for transistors in analog microwave circuits is as an amplifier. The transistor is typically used as a variable resistor when it is used in analog circuitry [4]. An applied input signal on the gate will control the amount of current flowing through the transistor. A signal with a small amplitude applied to the gate can in this way generate a larger amplitude output signal at the drain side of the transistor [8]. This is the basic principle when using transistors to amplify signals.

2.2 GaN transistors

Gallium nitride (GaN) transistors are becoming more and more used in microwave applications because of their high performance figures compared to other semicon-

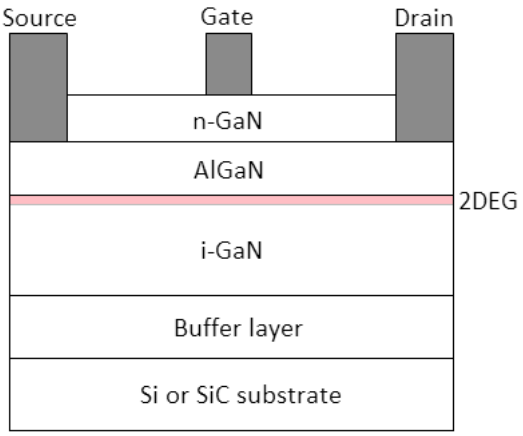


Figure 2.1: Basic layer structure of a GaN HEMT.

ductor materials used earlier [4]. Research about the semiconductor material accelerated during the 1990's along with development of new methods to grow the material on other substrates [5]. GaAs transistors have been and are still very popular for use in microwave circuits, but GaN transistors will and have replaced the GaAs transistor in many circuits.
The GaN technology is still relatively young and development of device fabrication methods are still moving ahead. A new technology is often expensive to implement in the beginning, but the performance increase can make it worth in long term. Reliability is always a concern when selecting devices for use in a circuit. GaN devices have still not been tested in the field for long time periods [9]. This fact may exclude GaN transistors to be used within some application areas.
GaN is a semiconductor material with very high power density, hence it can be used to produce transistors with high output power. The material can also withstand high electric fields before breaking down [5]. The efficiency can be very high since the resistance during the on state is low. The drain-source voltage can be high since the device can tolerate high electric fields. The drain current can thus be lowered and losses can be decreased since they are heavily dependent on the current. The parasitic capacitance at the input and output is low, making matching the device to another impedance more easy [5].

2.2.1 HEMT

The high-electron-mobility transistor or HEMT is the type of transistor manufactured based on GaN. The GaN HEMT device is a hetrostructure of two semiconductors, GaN and AlGaN, see figure 2.1. A two dimensional electron gas is formed in the intrinsic region between the two sandwiched semiconductors. The electrons are trapped in this region and they can only move freely in this plane while the transistors is active [4]. The active channel where the electrons are moving is undoped or intrinsic. This enables the electrons to move fast through the transistor since no collisions involving dopants occur. This will also make the channel resistance very low during the active state. Less power will therefore be dissipated over the transistor [4]. This power could instead be delivered to the load.

GaN devices are today typically grown on either silicon carbide (SiC) or silicon (Si) substrates. GaN grown on SiC is superior when considering parameters such as thermal and power performance. SiC have a very high thermal conductivity and can act as a heat sink to conduct heat away from the active channel of the transistor. GaN on Si on the other hand is a cost effective solution since the fabrication process is well developed and Si wafers can be bought for a low price [5].

2.3 Power amplifiers

Power amplifiers are used to amplify an input signal and output a signal with higher power. The gain of the device is not always very high, but the amplifier must be able to source enough of power to the load without going into saturation. A microwave amplifier design have to be executed with special care to the effects occurring at the higher frequency. The design must take reflections into consideration when the wavelength of the signal approaches the circuit size [10].
Power amplifiers have to be able to output a high output power, while still maintaining high efficiency. Special design considerations have to be introduced, not used when designing a more general amplifier. These should help maximize the output power and efficiency of the amplifier. These methods mostly concern the configuration of the components used on the drain side of the transistor [10].

2.3.1 SSPA and TWTA

Semiconductor devices are not the only device historically used to construct power amplifiers for microwave applications. The travelling wave tube amplifier (TWTA) can output a high power at very high frequencies. The solid state power amplifier (SSPA) have historically only been used at relatively low frequencies and low power levels [11]. The GaN technology have during recent years made the SSPA technology more interesting and the competition between the SSPA and TWTA have become more equal.
Replacing vacuum tubes with solid state devices have been a goal for many researches and circuit designers. The main disadvantage using the TWTA is its reliability. Mechanical parts inside the TWTA are sensitive and prone to failure. The tube itself will wear out after a certain time and a replacement must be installed [11]. A high voltage power supply must be used to operate the TWTA. This is both unsafe and the complexity of the power supply can be high.
Solid state devices have proven more and more useful in applications that before only relied on vacuum tubes. SSPA can be made smaller to shrink the entire size of the device using it. This is important in modern wireless applications where the power amplifier often is mounted in an antenna array. Overall efficiency can also increase to eliminate heat problems when mounting the circuitry in a dense environment.

2.3.2 Bias point

A DC voltage is applied to the gate and source of the transistor to set the bias point of the device. The bias voltage will enable the transistor to operate with a small

RF input signal. The RF signal would otherwise not be able to set the transistor to operate in the active region, this would result in a very distorted signal or in worst case no output signal at all. The DC operating point is a very important parameter that will determine the RF performance of the amplifier to a large extent [2].

Table 2.1: Summary of amplifier classes.

Class	**Conduction angle**
A	360°
AB	180°-360°
B	180°
C	$< 180°$

The chosen bias point can be adjusted to change the performance of the amplifier drastically. Different classes have been used to name these operating modes. The class is determined by how long during a full cycle the transistor will conduct when an RF signal is applied at the input. Table 2.1 shows a summary of some amplifier classes. There are other classes, but they are switched amplifiers [12].
The bias point and class will determine how efficient the amplifier can be. A class A type of amplifier will be most inefficient, while a class C amplifier will be the most efficient. Distortion will be the disadvantage when increasing the efficiency by this method.

2.3.3 Stability

The amplifier will oscillate if it is unstable. This could cause the device to self destruct or damage surrounding components [10]. Stability of the transistor is dependent on the amount of power reflected back from the active device. The transistor is unstable if more power is reflected back than is fed towards the transistor. This can happen if the impedance on the input or output port have a negative real part. This would result in reflection coefficients $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$ [2]. This is the general condition for instability.
Stability is classified into two categories, unconditionally stable and conditionally stable devices.
An unconditionally stable transistor will be stable independently of what terminations are applied to the input or output ports. A conditionally stable transistor is only stable for a limited range of terminations.
A few tools and methods are available to analyze the stability of a circuit. The most common are based on calculations using scattering parameters of the transistor.
Rollet's condition is one of these, defined as

$$K = \frac{1 - |S_{11}|^2 + |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

where Δ is

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

These two conditions indicate if the transistor is stable or unstable [2].

Another stability condition involves just a single parameter [13]. It is defined as

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11} * | + |S_{12}S_{21}|} > 1$$

There are several methods of making an unstable transistor stable [14]. A feedback network can be constructed to make the transistor stable. A resistor can also be placed at the gate or drain either in series or parallel. This will load the transistor and make the amplifier stable. It is a bad idea to place a resistor on the drain side when developing a power amplifier since it would dissipate much of the output power.

2.3.3.1 Stability at non-linear conditions

It is not enough to just examine the stability of the circuit when no input signal is applied. The circuit could be stable when performing an analysis based on small-signal s-parameters, but become unstable when driven with a large input signal [15]. The input signal will change the characteristics of the non-linear device. A harmonic balance simulation is often performed to investigate the performance of a non-linear circuit, but this method can only be used to find oscillations harmonically related to the input signal [15].
A method to find such an unwanted oscillation must be utilized to examine if the circuit will be stable with different levels of input power applied. A method called the auxiliary generator technique is one way to perform such a simulation [15]. This method is based on a local stability analysis of a circuit, where nodes in the circuit are examined to check for unwanted oscillations. This technique is convenient to use on circuits as power amplifiers, since they often are driven hard into non-linear operation.
The auxiliary generator method is simple to implement using standard tools in Microwave Office. A sinusoidal voltage source is connected to a node in the circuit to be examined. The voltage amplitude and phase of the signal source is set to be constant, while the frequency f_{ag} can be swept. The current is measured with a current probe at the same point. The admittance at the test point can be calculated simply as

$$Y_{test\ point} = \frac{I_{test\ point}}{V_{test\ point}}$$

The value of the admittance can be used to find a point where it approaches zero. This happens if the current flowing through the test probe approaches zero. The condition to look for is

$$Y_{test\ point} = \frac{I_{test\ point}}{V_{test\ point}} = 0 + j0$$

Potential unstable frequencies can be found by performing a sweep of the generator frequency f_{ag} while looking for the above condition to become true.

2.3.4 Output power

Output power can be maximized by following a few principles when designing the amplifier circuit. These methods will define how the matching networks later have to be designed. The input of the transistor should be terminated to allow for maximum gain [14]. This will occur when

$$\Gamma_{in} = \Gamma_S^*$$

The output could also be terminated in the same way, according to

$$\Gamma_{out} = \Gamma_L^*$$

if the amplifier was to be designed for the maximum amount of gain.
A power amplifier should not have maximum gain as the main requirement, but output power should instead be the main concern. The input could be designed following the method above, but the output termination should be constructed in a different way. Maximum output power will be reached when the voltage and current swing at the output of the transistor is maximized. The output of the transistor needs to see a specific load impedance in order for this to occur. This type of load is referred to as a Cripps load. A Cripps load will place the load line of the transistor in a way that maximizes the output power [12].
This method will ideally produce an amplifier that can deliver the maximum amount of power to the load. Losses are not taken into account, but they will also affect the power performance.

2.3.5 Efficiency

The efficiency of the amplifier is a measure of how much of the input RF power and DC supply power that is converted into usable RF output power [12]. Less wasted power in the device will make it more efficient. The efficiency is determined by measuring both the consumed DC power and the RF output power. The drain efficiency η is defined as

$$\eta = \frac{P_{RF}}{P_{DC}}$$

Another popular measure takes the added input RF power into consideration. It is referred to as the power added efficiency (PAE), given by

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}}$$

2.3.6 Matching network

Matching networks are needed at the input and output of the transistor to transform the impedance of the source and load to the impedance required on the input and output of the transistor. This is performed in order to eliminate or at least minimize the reflections present otherwise [6].
The matching network can be realized in many different ways. Lumped components such as capacitors and inductors can be used for lossless matching networks in the

ideal case. Resistors can be used in some cases, but they will introduce losses in the matching network. Distributed components are the alternative to lumped components. Lumped components are more complex to use at higher frequencies since parasitic effects become a problem [2]. Distributed elements on the other hand become very large in size if the frequency is low. The right strategy have to be used depending on the operation frequency of the circuit.
The bandwidth over which the matching network can operate properly should be as wide as possible. This can be hard to realize in reality. Wide bandwidth matching networks will typically increase in size, a compromise must therefore be made [6].

2.3.7 Bias network

The bias network should supply the DC power needed to run the transistor. The bias network should also isolate the DC power supply from RF energy [2]. The bias supply must remain stable even if the current drawn by the amplifier can vary. This is especially important at the gate, where the bias point could be altered otherwise. The bias network will if constructed correctly stabilize the the amplifier. Relatively long wires are often used to connect the circuit to the power supply. These wires are inductive and could potentially form a LC-tank together with the capacitors in the power supply. The LC-tank could introduce oscillations at its resonance frequency [8]. A battery of capacitors could be placed near the DC fed point of the bias network to counter act this process. Different values of capacitors are used to ensure capacitive properties over a wide bandwidth.
The bias network should supply the transistor with current even when the power supply can not keep up. The peak current is taken from the capacitors and the power supply will deliver the average current drawn [6].
Large currents will sometimes be sourced from the drain supply. The microstrip trace must be able to handle this current passing through the network without heating up to much. The microstrip trace could otherwise be destroyed by excessive temperatures.
Some active circuitry could also be added to protect the transistor from being destroyed beyond recovery. This protection function should limit the current drawn by both the gate and drain within safe operating limits.

2.3.8 Substrate

The surface mount amplifier circuit is built on a circuit board. The circuit board is made using a dielectric substrate material covered with a thin layer of metal on the top and bottom. The backside metal layer is usually left untouched to form a ground plane for the circuit. The top metal layer is etched according to the design layout. Surface mount components and other packages could then be soldered to the top of the board [16].
The substrate can be made using different dielectric materials. The substrate material must be selected according to the application considered. The top metal layer is made of copper, sometimes with a thin layer of some other metal to protect it. The thickness of the substrate and metal layer can also be chosen by the designer. The

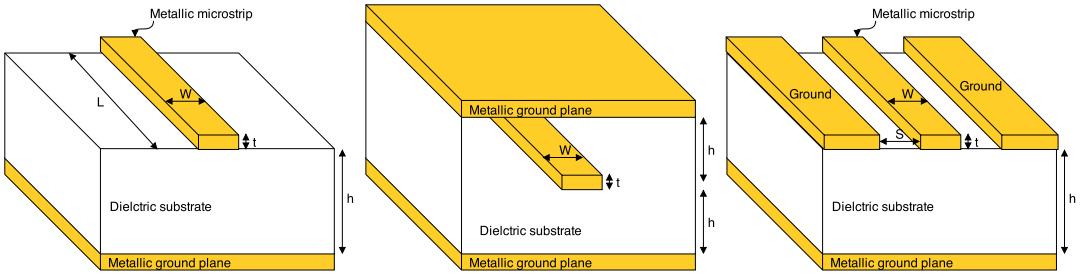


Figure 2.2: Three common types of transmission lines, microstrip, stripline and coplanar waveguide.

size of the circuit and the losses will be affected by the type of substrate material chosen [2].

2.3.9 Transmission lines

Transmission lines must be used to guide the electromagnetic energy to a desired location on the circuit board. Different alternatives exists, but three major ones are common for printed circuit board construction. These are illustrated in figure 2.2. Losses will always be present in a non ideal transmission line, independent on how good the design is. Losses can be controlled and reduced by careful selection of the physical structure of the transmission line as well as what materials that are used to fabricate it. Losses occur because of different reasons [6]. Losses can be present in the dielectric material or in the metal layer. Radiation losses can also occur, but they depend a lot on the layout used. Antennas could for example be manufactured as transmission lines on a circuit board. These should have very high radiation losses.

2.3.9.1 Microstrip

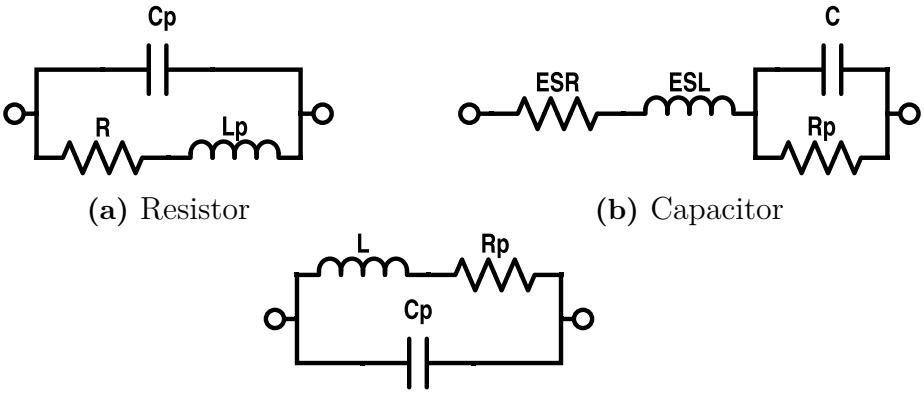
The microstrip line is placed on a substrate of dielectric material with a ground plane on the bottom. The characteristic impedance of the line is determined by the width of the line. The thickness of the metal layer and the substrate will also be factors affecting the electrical performance of the microstrip line [2].

2.3.9.2 Stripline

A stripline transmission line is similar in structure to a microstrip, but a substrate and ground layer is also place on top of the center conductor to fully confine the field between two layers of dielectric materials and ground planes.

2.3.9.3 Coplanar waveguide

The coplanar waveguide transmission line is similar to the microstrip structure, but a top ground plane have been added in the same plane as the top conductor. The top ground plane is placed close to the top transmission line with some spacing to confine the fields as much as possible.



(a) Resistor **(b)** Capacitor

(c) Inductor

Figure 2.3: Basic equivalent circuits of a resistor, capacitor and inductor.

2.3.10 Lumped components

Passive components such as resistors, capacitors and inductors have to be used where distributed elements can not be implemented. These components should in theory be ideal, but they are in practice more complex. Parasitic circuit elements will be present in all physical components. The equivalent circuit of a typical non-ideal component will contain other parasitic components [8]. Basic equivalent circuits representing these parasitics are shown in figure 2.3.

These parasitic effects can cause problems since self oscillations may occur at a specific frequency. It is therefore important to take the parasitic effects into consideration when designing circuits. The passive will not oscillate by itself, but improper design of the circuit can excite the component and cause an unwanted oscillation to start [6].

Most lumped components are available as surface mounted chips to be soldered directly to the circuit board. The size may differ depending on the component value, but standard sizes are available.

The size of the lumped component should be small compared to the wavelength of the signal applied to it. The component must otherwise be considered as a distributed element [6].

2.3.10.1 Capacitors

Capacitors are important components in a microwave circuit. They can be used to decouple and smooth out DC voltages. They can also be used to block DC and couple the RF signal between sections of a circuit [6].

Capacitors have a serial and a parallel resonance frequency. The capacitor will have no reactive part at the series resonance frequency, hence it will have its lowest impedance at this frequency [17]. The insertion loss of the capacitor will thus be at its lowest. This is useful when capacitors are are placed in series with an RF transmission line, i.e. as a coupling capacitor to couple power from one part of the circuit to another.

2.3.10.2 Inductors

Inductors can be used to block RF signals and conduct DC signals, they can also be used for matching. It is difficult to utilized surface mount inductors operating at high frequency, due to the large stray capacitance [17]. This capacitance will cause the inductor to have a self-resonant frequency. The inductor will be seen as a capacitor and not work as expected above this frequency. It is not practical to use inductors when designing circuits for high frequency operation because of this property [17].

2.3.10.3 Resistors

Resistors have a wide variety of uses in microwave circuits. They can by introducing loss dissipate unwanted power in circuits or used to stabilize an unstable circuit [6]. Resistors are in practice always associated with some stray capacitance and inductance. This may cause the resistor to act very differently at higher frequencies [17].

2.3.11 RF drive signal

The input drive signal will supply the amplifier with input power. The power level of the input signal must be sufficiently large since the power gain of a typical power amplifier can be relatively low.
The input signal can be a continuous wave (CW) or a pulsed type of signal. A pulsed input signal will be switched on for a limited time during a period, called the duty cycle. The duty cycle is often expressed in terms of percent.
A pulsed input signal will lower the overall average power dissipated in the amplifier. This will lower the thermal stress on the amplifier compared to when feeding the amplifier with a CW input signal [6].
The bias supply for the amplifier can also be switched on and off together with the input RF power. The bias supply must be turned on slightly before the input signal is applied, since the bias network must have some time to charge up. The overall efficiency of the amplifier will be improved when switching the bias supply, since no power is dissipated when the input RF signal is turned off.
A power amplifier for use in a radar system is often operated with a pulsed input signal [6].

2.3.12 Device failure

Catastrophic failure of a transistor used in a power combined amplifier will degrade the performance in some way, but the amplifier could in theory continue to operate at some level. The faulty transistor will change its electrical properties and be seen as a short circuit or in most cases an open circuit. This will change the impedance seen by external networks connected to the transistor [6]. This may cause severe power reflection to occur that may destroy external components along the way. The circuit must therefore be constructed with robust components that can handle the extra stress applied in such a case.

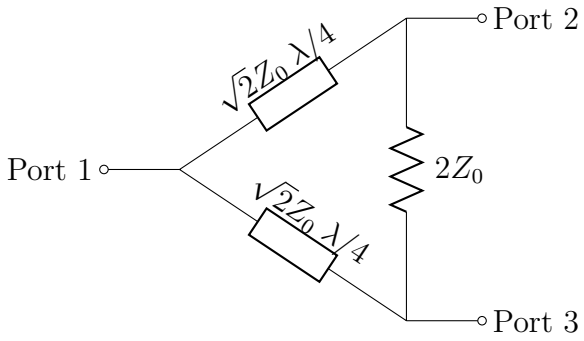


Figure 2.4: Circuit topology of a two-way Wilkinson power divider.

The amplifier developed in this work will not be designed to withstand a failure. This is not needed in all cases, since the entire amplifier could be replaced instead if a failure was to occur.

2.4 Combining network

A combining network should enable N number of transistors to be connected to a single source and load. This passive device will split or combine the power of a single device and distribute it to two or more outputs at a lower power level. The amount of power can be equal at all outputs or unequal with some other division ratio. The phase of the output signals can also vary. The phase can be equal or in phase, but it could also be out of phase with some amount, typically 90° or 180°.
There are multiple alternatives available when choosing what type of combiner should be used. The combiner must have small losses, since losses will add up when multiple transistors are connected [6]. Both the input and output ports should be matched and also isolated from each other. It is not possible to satisfy all these conditions with all types of combining networks at once.
Amplitude and phase imbalance between the outputs of the divider must also be controlled. Imbalance in amplitude and phase can cause problems if one active device is overloaded due to unequal power division of the input signal. Phase imbalance can be a problem if the signal coming from the active devices are combined out of phase, since it can result in power loss [6].

2.4.1 Wilkinson divider

The Wilkinson power divider is frequently used in microwave designs to divide or combine a signal. It is simple and easy to fabricate the component, often realized using microstrip transmission line. The most common Wilkinson divider is a three port device matched on all ports and isolated from each other. Losses will ideally only occur if the load on the outputs are mismatched. A shunt resistor is utilized to absorb the reflected power if that was to occur [2].
The outputs of the Wilkinson divider typically have the same phase. The amplitude on both ports can be equal, but it can also be unequal if needed.

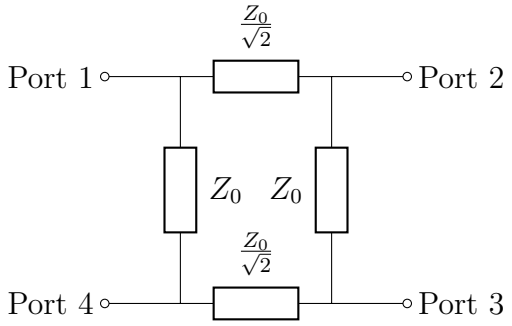


Figure 2.5: Circuit topology of a two-way quadrature hybrid. All the transmission lines are $\lambda/4$ in length.

The Wilkinson power divider will transform the input impedance to $2Z_0$ with a quarter-wave transformer. Both the outputs are combined in parallel, with a resistor of $2Z_0$ place between them. Figure 2.4 show a typical two-way Wilkinson divider design.
The standard Wilkinson divider is matched to 50 Ω on all parts, but it is possible to choose an arbitrary impedance to match to [18]. This could be advantageous as the divider could be incorporated with the matching network. Lower losses could be achieved if an impedance transforming divider is used. The output impedance can not be entirely chosen freely. The layout of the circuit must be practical and possible to fabricate. The divider will in this case be terminated with resistive loads R_2 and R_3 on ports 2 and 3 and a different input termination of R_1 on port 1. The characteristic impedance $Z_{\lambda/4}$ of the quarter wave line should then be

$$Z_{\lambda/4} = \sqrt{(R_2 + R_3)R_1}$$

The shunt resistor should have a resistance R_{shunt} of

$$R_{shunt} = R_2 + R_3$$

2.4.2 90 ° hybrid

A 90 ° hybrid also known as a quadrature hybrid will divide the incoming signal towards two output ports. Figure 2.5 illustrates a two-way quadrature hybrid. A 90 ° phase shift will occur between the two outputs since the signals have travelled different distances. A fourth port called the isolated port will ideally not receive any power and should be terminated. The output ports are isolated relative to each other. Reflections caused by mismatch on the output ports are terminated at the isolated port and not present at the input port. The quadrature hybrid can also transform the impedance from input to output [19].
The quadrature hybrid can also be realized using another topology called the Lange coupler[2]. The Lange coupler is constructed of closely spaced transmission lines arranged as fingers. This topology can offer good performance, but physical fabrication can be more complex. The transmission lines can be difficult to produce with a clean result. Bridges between transmission lines also have to be produced, often using bond wires.

2.4.3 180 ° hybrid

The 180 ° hybrid is also a four-port network, but with 180 ° of phase shift between the two output ports. It will otherwise operate in the same manner as the 90 ° hybrid. Different topologies are available to construct a 180 ° hybrid. The ring hybrid or rat-race is the most common topology used. The 180 ° hybrid is typically larger in size compared to other dividers since the phase shift often is realized using a length of transmission line.

2.4.4 Bus bar combiner

Multiple transistors can be combined using a very small area if a bus bar combiner is used. The bus bar is made as a single transmission line or bus bar where transistors are connected to. This type of combining network is commonly used for amplifiers designed for use in a MMIC design[20]. The distance between individual transistors must be much smaller than the wavelength for the used frequency. Most individual discrete transistors in packages are too large in size to be successfully combined together using this type of combining network topology [6].

2.4.5 Parallel matching network

One way to design an amplifier with several transistors is to begin with an individual stage using only one transistor. This amplifier should be matched at a higher system impedance of 100 Ω when combining two transistors. Two of these stages could then be connected together in parallel. The system impedance of both stages in parallel will be 50 Ω. The matching networks could then be simplified since multiple components will be symmetric and can be combined into one component [6].

2.4.6 Distributed amplifier

A distributed amplifier is using a combining topology where several transistors are placed in parallel with all the gates of the transistors connected to the same line. The drains of the transistors are also connected to a common line at the output [21]. Figure 2.6 shows two different topologies used to design a distributed amplifier.

The distributed amplifier can be single- or dual-fed at the input and output [21]. A single-fed design will be fed with power from a single line as opposed to a dual-fed design where a balun or a hybrid coupler is used to feed the amplifier from two different directions. The same technique is used at the output to combine the signal in to a single output line.

A dual-fed design can take advantage of both the forward and backwards travelling wave [21]. The output power can therefore be higher with a dual-fed design.

This type of design is only advantageous to use if more than two transistors are to be combined. There is no point in using this topology when combining two transistors since other methods then are better to use.

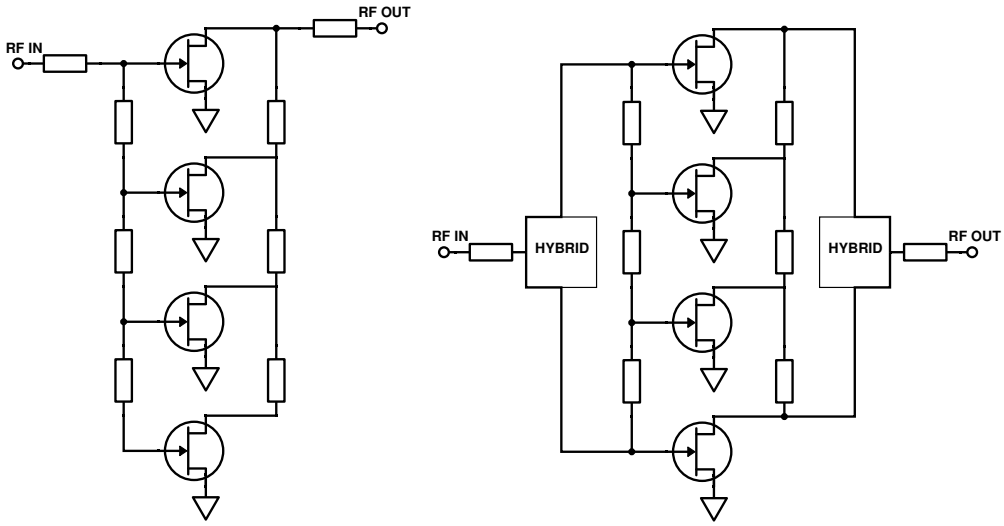


Figure 2.6: Circuit topology of a distributed amplifier. Single fed topology to the left and a dual fed topology to the right.

2.5 Simulation and models

A proper microwave circuit must be designed with great care if the performance of the circuit should be as planned. Computer aided design is therefore a vital part when working with microwave circuit design [2]. The computer software will simulate the circuit and present the designer with results reflecting its performance. This is a very fast method to determine the performance without actually building a real life circuit [6]. A number of different variations and iterations can be analyzed during a short time period.

The circuit simulation uses mathematical formulas and models to calculate the performance of the simulated circuit. This type of simulation can be run in a short time period and is in most cases very accurate. This enables the circuit designer to tune and optimize component values of the circuit to maximize its performance.

Components used for simulation must be based on a model. It could be a simple model for just a straight piece of microstrip line or a complex model of a transistor. It is important to have a model of the transistor that represent the physical device as close as possible. Different transistor models exists, some are simple and some are more complex [22]. It could be based on measurements performed on a physical device, such as s-parameters. This model is only valid at the same bias point as when the measurements were performed.

Other models are more general and can be used at arbitrary bias points. A non-linear model can model the behaviour of a non-linear device, a diode or a transistor are examples of such devices. This type of model should be able to work properly during a large-signal simulation independent on the bias point chosen at the time [22].

The circuit simulation is not able to handle all characteristics of the circuit. Coupling between elements is often not taken into account during regular circuit simulations [6]. Electromagnetic simulations can be used instead to more precisely capture the

performance of the simulated circuit element.
Most EM simulation algorithms are based on Maxwell's equations governing the properties of electromagnetic waves [23]. The EM simulation algorithm can ignore certain important facts about the circuit and simplify it to limit the simulation time needed. It is very important to not fully trust the circuit simulation at all times because of this property.

3
Methods

The following chapter will discuss the methods used during the project to reach the before stated purpose. The process from design idea to the final design and prototype circuit will be described in detail.

3.1 Performance requirements

The power amplifier should operate according to a couple of given requirements. The goal was to have the amplifier operate with acceptable performance within a frequency band between 8.5 GHz and 9 GHz, with an output power reaching 50 W or 47 dBm. The efficiency had to be high, but output power was the main concern. The size of the circuit had to be as small as possible.
The transistors to be used to construct the amplifier were already chosen. A 25 W GaN HEMT with model number CGHV1F025 manufactured by the company Cree had to be used. The transistor is packaged in a plastic dual-flat-no-lead (DFN) package, with size 3 mm x 4 mm. Operating frequency range is between DC and 15 GHz.

3.2 Analysis of reference amplifier

An already existing amplifier circuit supplied by the company Cree was characterised in order to investigate what performance a single transistor could deliver. This circuit used the proposed transistor to be used in the later designed power combined amplifier. See figure 3.1 for an image showing the reference amplifier.

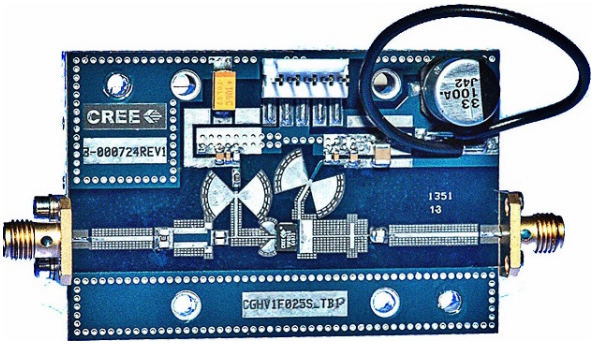


Figure 3.1: Reference amplifier designed and manufactured by Cree. This amplifier is based around a single CGHV1F025 transistor.

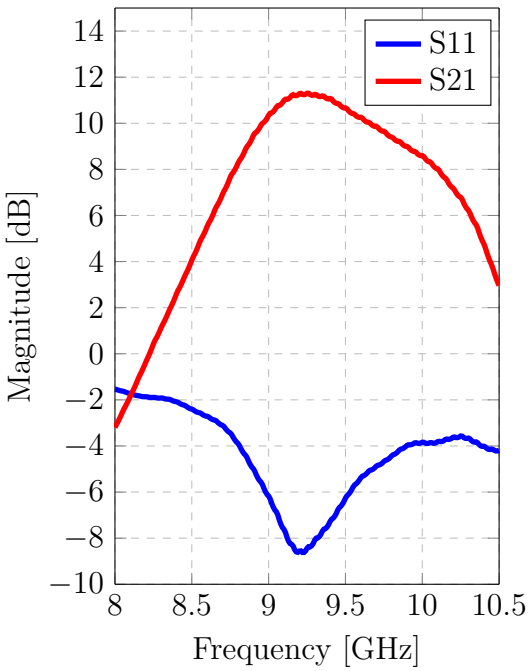


Figure 3.2: Measured magnitude of S_{21} and S_{11} versus frequency at $P_{in} = 0\ dBm$

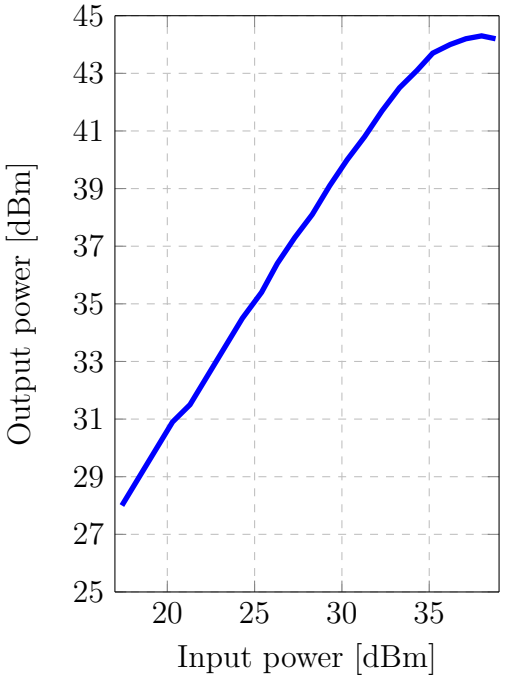


Figure 3.3: Measured output power of the reference power amplifier at frequency $f_{in} = 9.2\,\text{GHz}$.

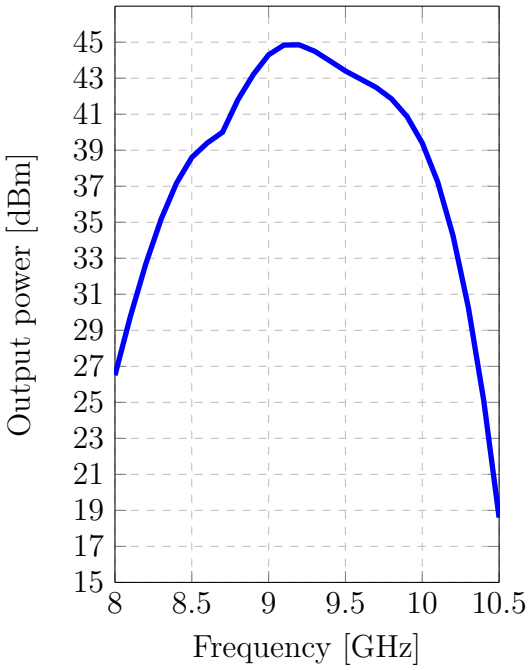


Figure 3.4: Measured output power of the reference power amplifier versus frequency at input power $P_{in} = 37\,\text{dBm}$.

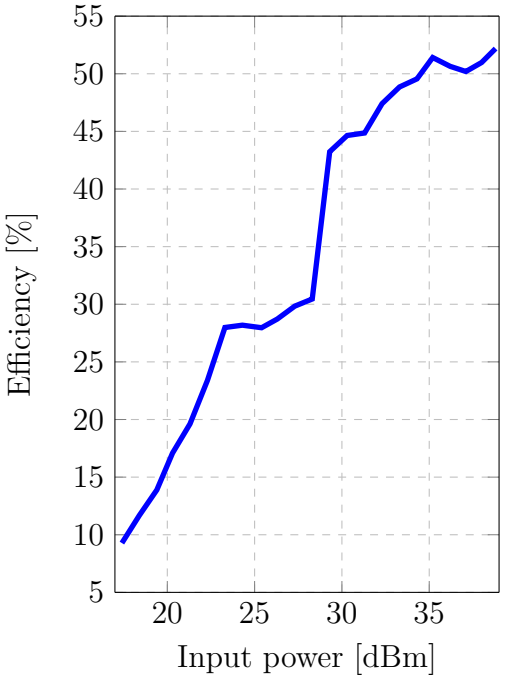


Figure 3.5: Measured drain efficiency versus input power at frequency $f_{in} = 9.2\,\text{GHz}$.

Some information was available in the data sheet for the transistor, but measurements could give some further knowledge about the properties of the physical device before simulations with the model commenced.
The measurement procedure is described further in section 3.5.
Figure 3.2 shows measured S_{11} and S_{21} of the reference amplifier. Output power related to frequency is shown in figure 3.4 and related to input power in figure 3.3. The measured efficiency is plotted in figure 3.5.
The measured performance of the reference amplifier was approximately as stated in the data sheet for the device.

3.3 Design of prototype

A prototype of an combined amplifier using two of these transistors were designed using mainly simulations and some additional measurements.

3.3.1 Substrate material

The substrate used to build the circuit had to be chosen early in the design phase. The following simulation will use parameters based on the chosen substrate. Microstrip technology was used to make transmission lines with minimum loss at shorter distances, they can also be easily fabricated. Simulations of the characteristic impedance and line width were performed to find a suitable substrate material to use. Rogers 4350B was chosen as the laminate material to use. This laminate is based on a ceramic substrate material with dielectric constant ϵ_r of 3.66 and a loss tangent δ of 0.0036. A compromise was done regarding the substrate thickness to get a low loss microstrip line with a relatively small circuit size. A 20 mil substrate thickness was chosen. The metal thickness had to be much larger than the penetration depth at the lowest frequency in the band of interest. 17 μm of metal thickness was considered more than enough.

3.3.2 DC characteristics and bias point

The first step in the design of the power amplifier was to find a suitable bias point for the transistor to operate at. A class AB type of biasing was chosen to achieve good efficiency while still maintaining a high output power.
The data sheet for the transistor states what the maximum tolerances are. The gate and drain voltage as well as the drain current can not exceed the absolute maximum limits stated in the data sheet. The bias point was chosen to allow maximum swing of drain voltage and drain current at operation with an input signal applied to the gate.
The DC characteristics of the GaN HEMT was then found by simulations with swept DC supply levels of gate and drain. An IV plot could then be generated in order to locate the approximate bias point that could support a load line optimal for a power amplifier operating at the desired class. The simulated DC characteristic is illustrated in figure 3.6.

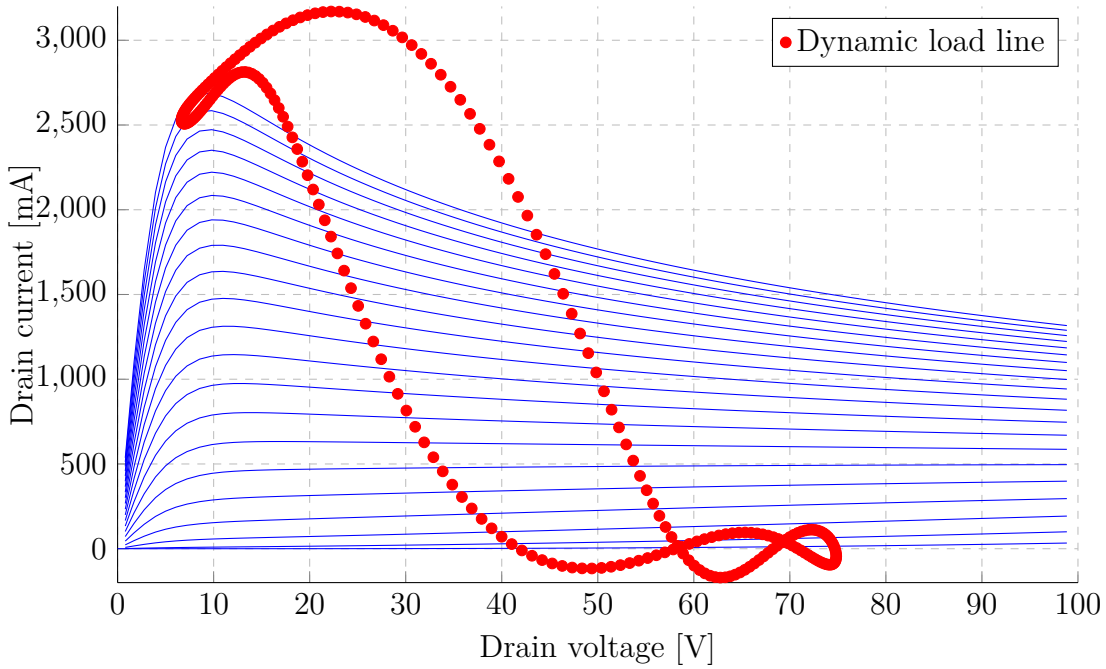


Figure 3.6: DC characteristics generated using the model in Microwave Office. The gate voltage V_g is swept between -3 V to 0 V. Dynamic load line of the final amplifier to be designed is plotted on top.

3.3.3 Stability

The stability of the transistor could then be analyzed to see if any instabilities were present. K and μ parameters were generated and plotted from DC up to 15 GHz. The amplifier was unstable at lower frequencies, a series resistor was placed on the input of the amplifier to make it stable. This would in turn lower the gain, a capacitor was therefore placed in parallel with the resistor to lower the insertion loss for frequencies at the band of interest. This solution would still allow the amplifier to be stable at low frequencies, but allow the gain at higher frequencies to be less affected by the stability network.

3.3.4 Source and load reflection coefficient

The reflection coefficients of the transistor could be determined after the bias point was chosen. Ideal bias networks were used to set the right bias point for the transistor at both input and output. An ideal input matching network was developed by generation of the input reflection coefficient of the transistor based on simulations. The gate was terminated using a conjugate match to achieve maximum gain. A tuner that can present an arbitrary reflection coefficient to the gate of the transistor was used to simulate an ideal matching network.
With the input terminated properly attention was given to the output of the transistor. A load pull simulation was performed to find an area on the Smith chart where output power and efficiency would be at its maximum. An ideal matching network was generated also for the output. An ideal amplifier model had now been

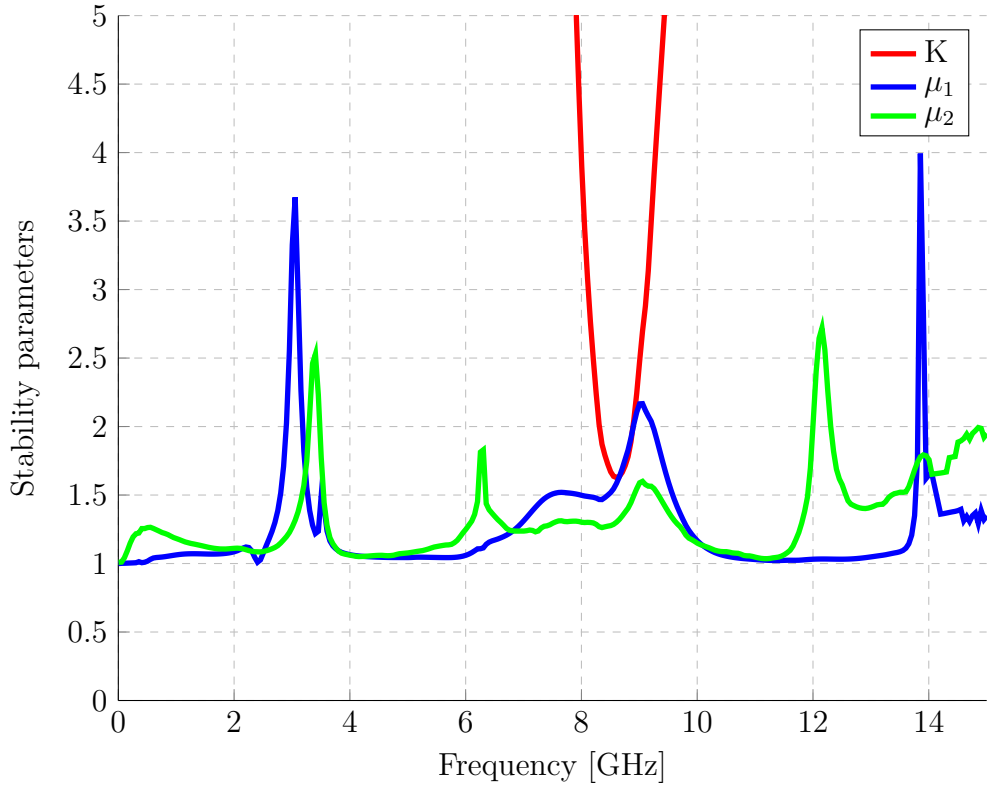


Figure 3.7: Stability parameters K and μ plotted from DC to 15 GHz.

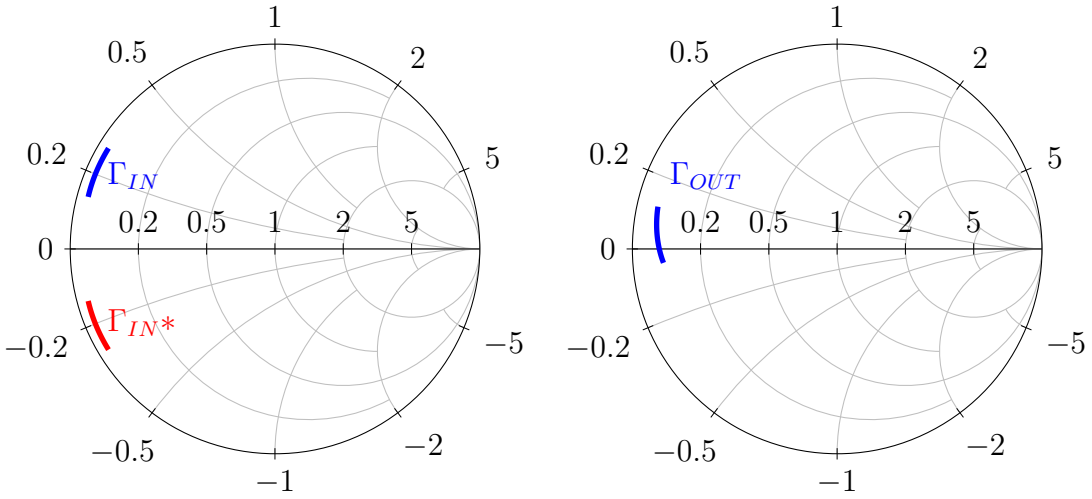


Figure 3.8: Input and output reflection coefficients generated from transistor model in Microwave Office. The frequency is swept from 7 GHz to 10.5 GHz at the bias point $V_d = 40\,V$, $V_g = -2.6\,V$.

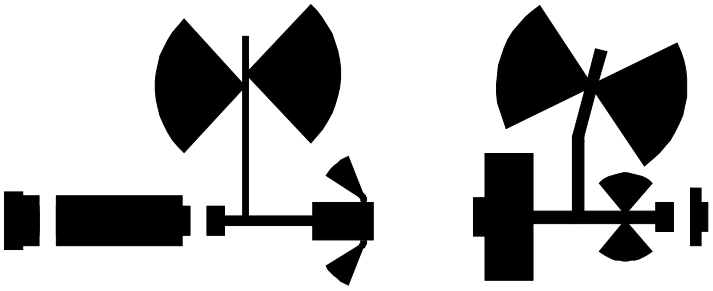


Figure 3.9: Final copper layout of the matching networks with integrated bias networks for input and output of the transistor.

constructed, but with no physical parts. The next step was to develop a physical circuit with the results generated during this simulation.

3.3.5 Matching network

The ideal matching network could only be used for simulation, a physical circuit had to be developed to make a realizable matching network. The matching network was designed with the desired reflection coefficients already known from the previous simulation. The most difficult part of this design stage was to find a matching network that could present the transistor with the right reflection coefficient over a wide enough bandwidth.
A design tool named iFilter in Microwave Office was the main tool used to design the matching network. This tool was used to compare and realize a number of different matching networks. The goal was to find a matching network with a bandpass response. Distributed elements made with microstrip line were preferred since lumped components suffer from parasitic effects at this high frequency. Short circuited stubs were also avoided since via holes would be needed. The size of the matching network was also a design criteria. A too wide network would make it hard to position two transistors in parallel, as stubs would come to close to each other.
The most simple input matching network consisting of a stub and a transmission line would have poor bandwidth with high insertion loss within the band of interest. A more complex design of the input matching network had to be implemented to reach the desired bandwidth performance of the amplifier. The copper layout of the matching networks used for the final prototype are shown in figure 3.9.

3.3.6 Bias network

A standalone bias network was first developed. This design could then be integrated with the matching network to save board space. Good isolation and wide bandwidth were the main design goals when constructing the bias network. A design with a quarter wave transmission line and two radial stubs was chosen as the topology for the bias network, see figure 3.10. Two radial stubs were used, placed at different distances from the RF transmission line to achieve a higher bandwidth. The first radial stub closes to the RF line was optimized for the highest frequency in the

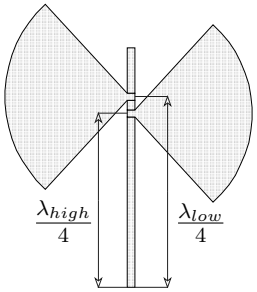


Figure 3.10: Layout of the input bias network. Notice that the radial stubs are placed at different distances from the RF line.

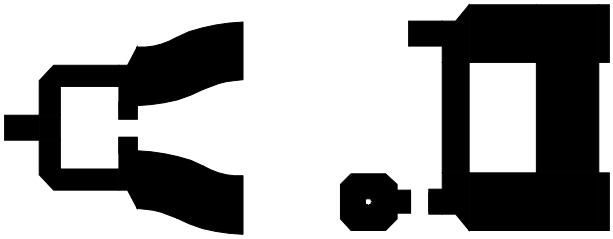


Figure 3.11: Layout of the combining networks designed to be used as candidates for the final amplifier design. The Wilkinson divider to the left and the quadrature hybrid to the right.

band, the other radial stub for the lowest frequency. A regular topology was used at the drain side because of lack of space. The width of the line use to feed DC power to the drain was dimensioned to handle more current.

3.3.7 Combining network

Different topologies of combining networks were evaluated to find the most suitable for use when designing a combined amplifier. A number of combining networks were implemented in Microwave Office, then tuned to their best possible performance for the frequency band of interest. The combining networks could then be compared with each other. Insertion loss, bandwidth, isolation and amplitude imbalance were the performance figures used when performing the comparison.
A number of different ways of performing power combination with multiple transistors were examined. A selection of the most interesting methods were further analyzed.
The topologies chosen for simulation have been described and treated in the theory section 2.4.
Some of these networks were found not to be suitable for use with discrete surface mount transistors. These networks were only suitable to use when designing MMIC circuits with a much smaller feature size.
There were methods to combine two or more transistors. Some of the techniques were more general and could be scaled up to incorporate arbitrarily many transistors connected in parallel. Some topologies were most useful to utilize if four or more transistors had to be combined.

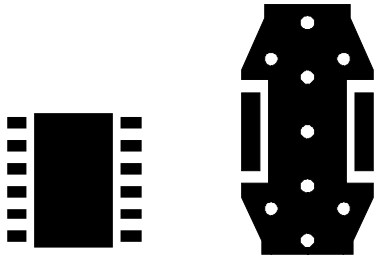


Figure 3.12: Standard footprint for a 12 pin DFN package to the left. Modified footprint used for the circuit to the right.

The prototype design should only use two transistors in parallel. A combining network suitable for use within this setting was therefore used for the amplifier.
A Wilkinson and a quadrature hybrid were chosen as candidates for use along with the combined amplifier. These combining techniques seemed most promising to further analyze. The combining networks were designed to also transform the impedance from 50 Ω to around 28 Ω on both outputs. A lower output impedance would require very wide conductors to be used. They would be unpractical or impossible to fabricate.
Figure 3.11 illustrates the two candidates for use as dividers in the final amplifier design. The Wilkinson divider has a 56 Ω shunt resistor and the quadrature hybrid is terminated with a 50 Ω resistor at the isolated port.

3.3.8 Coupling capacitors

Coupling capacitors were placed at the input and output of the amplifier to act as DC blocks for the bias voltages. The capacitors were chosen to have minimum insertion loss at the operating frequency band. The specific capacitors used were made especially for use with circuits operating at high frequency.

3.3.9 Transistor footprint

The footprint for the DFN encapsulate transistor must be traced out on the PCB to allow for soldering of the component. The suggested standard footprint is illustrated in figure 3.12. Most pins on the chip are shared which allows the input and output RF transmission lines to be connected to the transistor package with a single copper structure. The ground connections are placed on each corner of the package and on the large pad in the middle of the package. The pad in the middle will as well act as a heat sink, but via holes to the backside of the board must be placed on the pad to ensure a good ground for the transistor and a path for heat to be conducted away through. The modified version of the footprint used for the amplifier layout can also be studied in figure 3.12.

3.3.10 Electromagnetic simulation

Electromagnetic simulations were performed once the ordinary circuit simulation showed promising performance of the amplifier. This was done to check and verify if

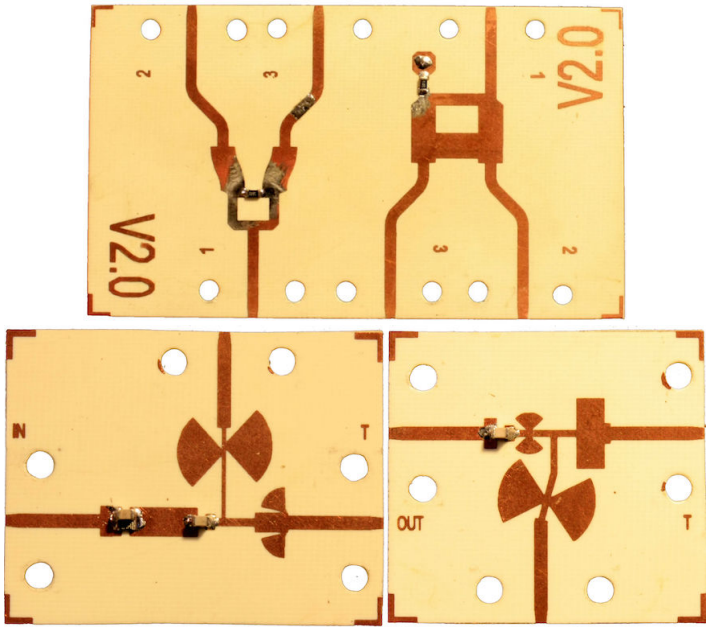


Figure 3.13: Above are the fabricated test boards of the dividers. Below are the test boards for the input and output matching and bias networks.

the performance still was the same when performing a more realistic EM simulation. Tuning and optimization had to be performed on the circuit elements since the results generated by the EM simulation were slightly different. Two different designs using the same amplifier branches but with different combining networks were generated. These could then be further analyzed by constructing physical test boards.

3.3.11 Test boards

A number of test boards were made to test the real performance of different sub circuits of the power amplifier. This was done to verify and compare the performance of the simulated circuit against the manufactured equivalent. This would make it possible to detect potential problems and errors on an early stage, before testing the complete amplifier circuit all at once. The matching networks for both input and output were placed on individual boards to allow for measurement of the reflection coefficient directly where the transistor is supposed to be placed later. A Wilkinson divider and a quadrature hybrid were also placed on test boards.
The layout of the fabricated test boards on the substrate are pictured in figure 3.13. The measurements on these test boards have been executed using a standard two-port 50 Ω network analyzer, even if some of the ports required some other termination impedance. This has been dealt with during the post processing of the measurement data, where Microwave Office have been used to recalculate the s-parameters for the correct termination impedance. All unconnected ports on the device under test have been terminated with a 50 Ω load. Three measurement have been performed on every three-port, these measurements have then been combined into a single three-port s-parameter data file.
A TRL calibration was performed to calibrate out the transition from coaxial to

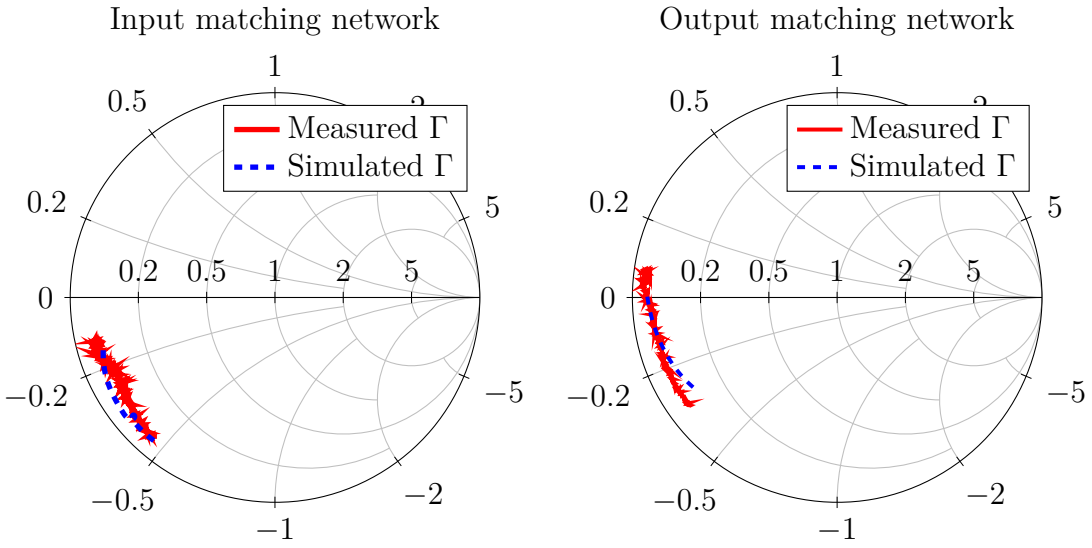


Figure 3.14: Measured reflection coefficients of the matching networks fabricated on the test boards. Frequency is swept between 7 and 10.5 GHz.

microstrip transmission line. A calibration kit consisting of a thru, reflect and line standard was made on the same substrate, see figure A.1 in appendix A for an image showing the used calibration kit. This calibration method placed the reference plane on well defined position allowing for easy comparison with the simulated data.
The electrical connections to the boards were made using screw on end-launch SMA-connectors from the company Southwest. These connectors could be installed quickly and no soldering was required when mounting them to the board.
The measurements performed on the input and output matching networks are summarized in figure 3.14. The measured reflection coefficients corresponds very closely with the simulated ones. These networks could perform well if used in the final amplifier according to this test. The capability of the bias network to isolate DC and RF could also be evaluated. This isolation was determined to be sufficient over a wide enough bandwidth, always under -30 dB.
The measured performance of the physical dividers compared to the simulated ones can be seen in figure 3.15 and 3.16
The results generated by measurements of the test boards allowed for comparison of the simulated circuit model with the physical test circuit. The most suitable divider and combiner for use with the amplifier was chosen based on the measured results. The Wilkinson divider had better amplitude imbalance and bandwidth. Both alternatives could offer a good match on all ports. The Wilkinson divider was chosen as the alternative to used in the combined amplifier based on the measurements on the test boards.

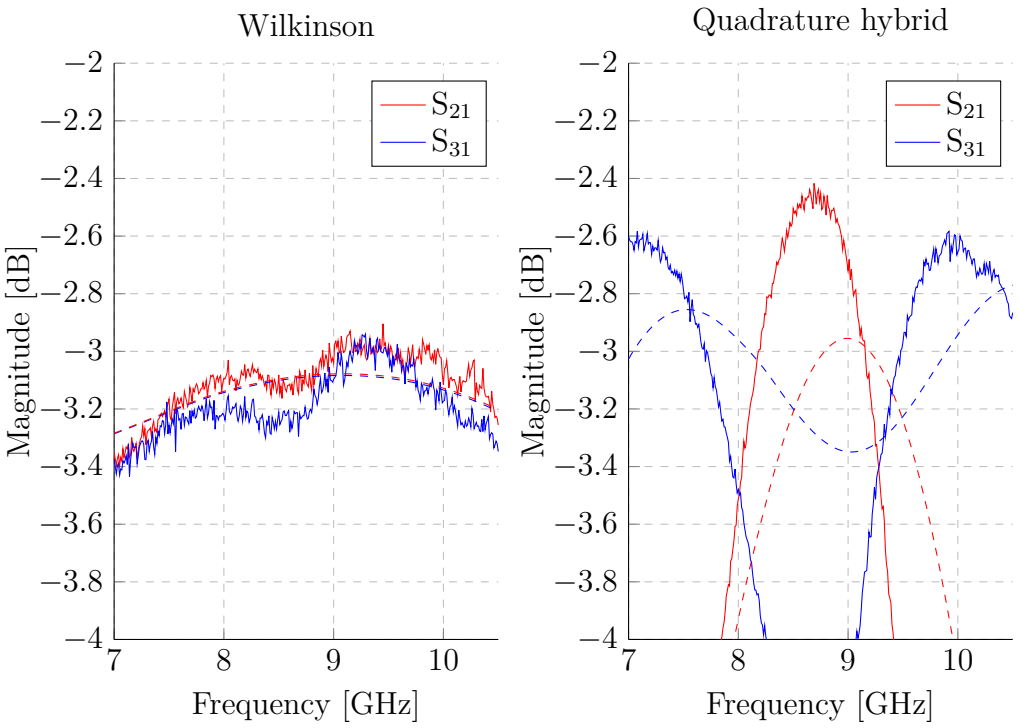


Figure 3.15: Performance of the fabricated divider test boards, illustrated using measured magnitude of S_{21} adn S_{31}. Solid traces represent measured values and dashed traces are results from EM simulations.

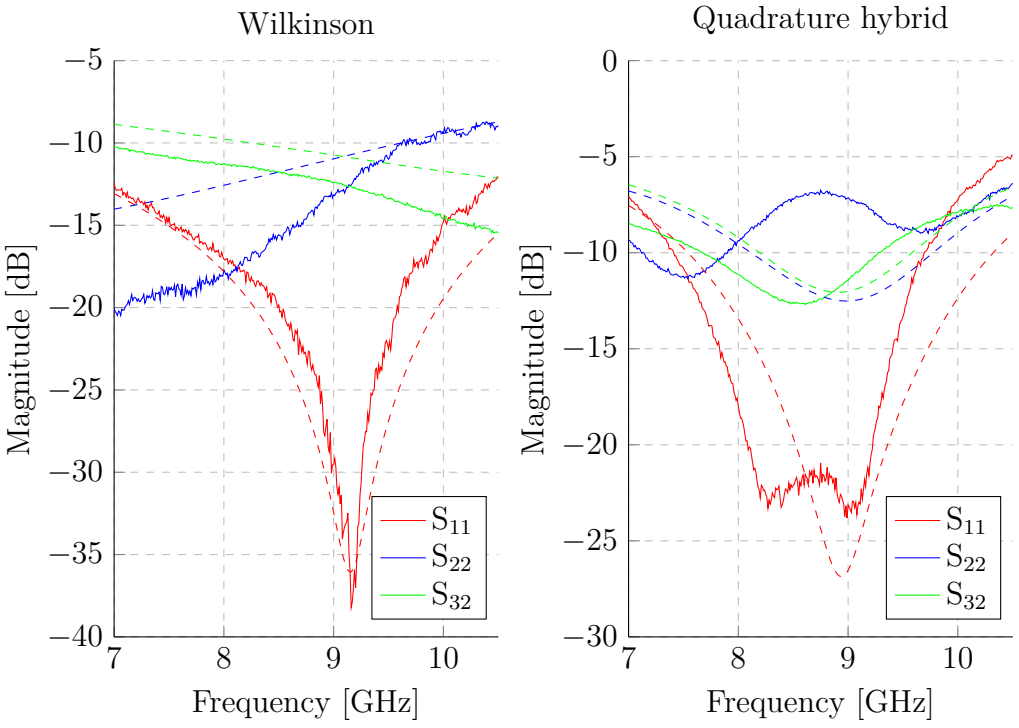


Figure 3.16: Performance of the fabricated divider test boards showing measured magnitude of S_{11}, S_{22} and S_{32}. Solid traces represent measured values and dashed traces are results from EM simulations.

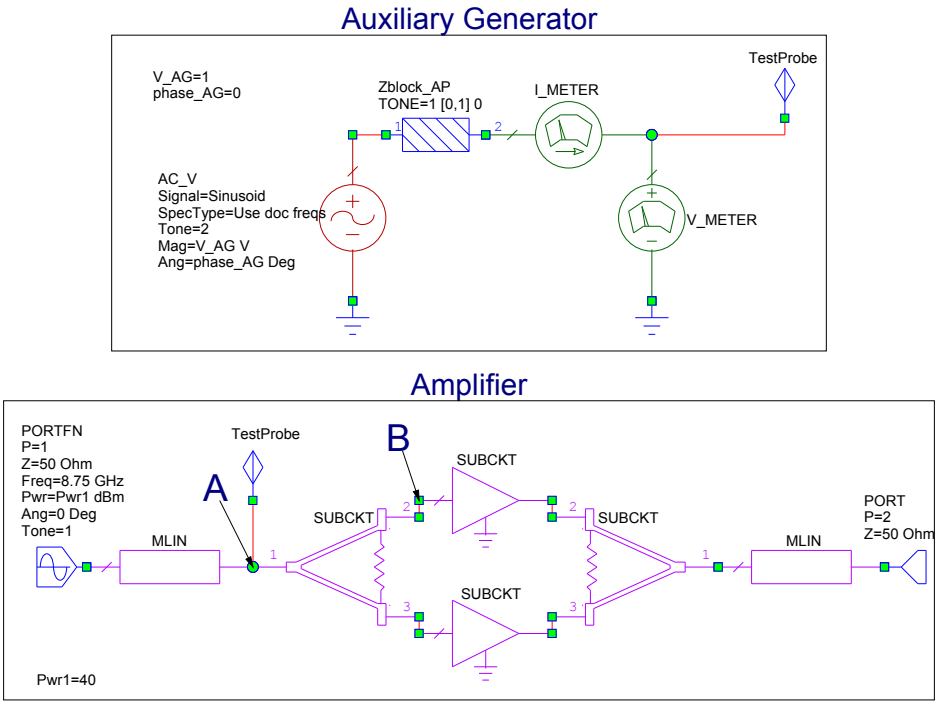


Figure 3.17: Simulation setup used to perform the stability analysis following the auxiliary generator method.

3.3.12 Stability with applied input power

The auxiliary generator method was used to investigate if the power amplifier was stable even with an input signal applied. The simulation setup used to perform the simulation is illustrated in figure 3.17. The result can be seen in figure 3.18. A real part near zero together with an imaginary part near zero would indicate potential instabilities. The analysis was performed for frequencies between DC and 15 GHz using five different power levels for the input between 0 dBm and 40 dBm. The simulation test probe was also place at two points of the circuit, point A and B as indicated in figure 3.17.
The same simulation was also performed on a reference circuit already known to be able to oscillate. The actual results could then be compared with the results generated using the reference to be able to decide how stable the circuit really is. A simple LC circuit consisting of a capacitor and inductor was used as a reference circuit. The real part of the admittance had values in the range of 10^{-12} when oscillations occurred.
There are small variation of the admittance for different power levels and positions in the circuit, but no evidence of oscillations could be found using this method. It should indicate that the circuit is stable even if an input signal is applied.

3.3.13 Final optimization and adjustments

The power amplifier circuit was then prepared for final assembly. Electromagnetic based simulations were performed on all circuit elements together. This was done to make sure that performance still was as desired.

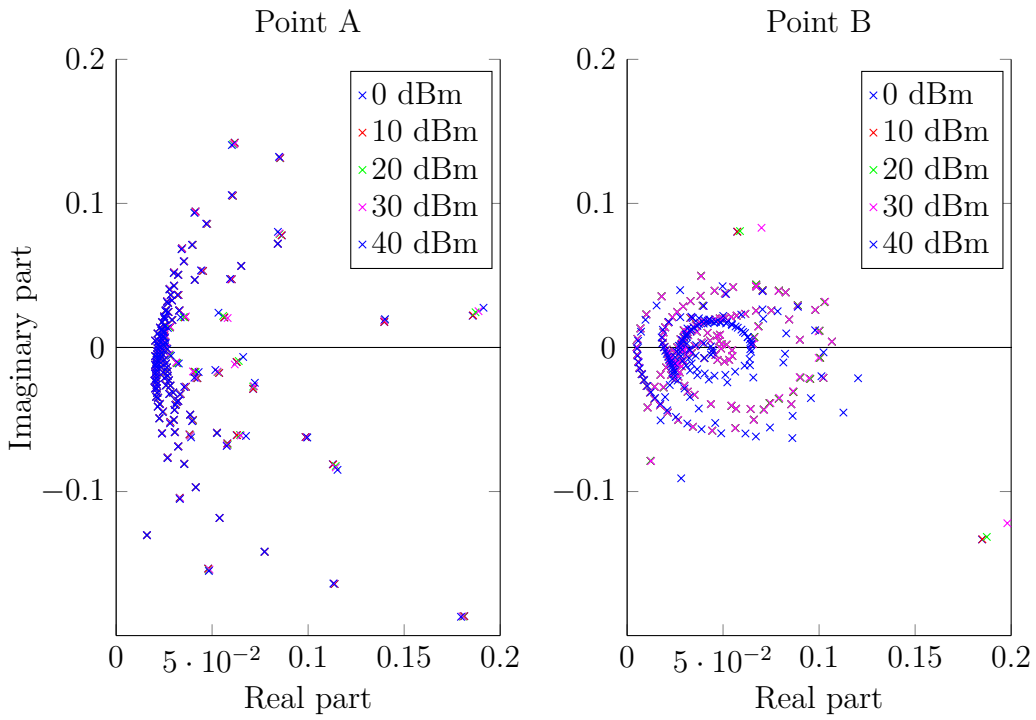


Figure 3.18: Impedance measured with the auxiliary generator method at point A and B in the amplifier circuit. Every point represents the admittance at a frequency from DC to 15 GHz. A point with real part near zero together with the imaginary part at zero would indicate an instability.

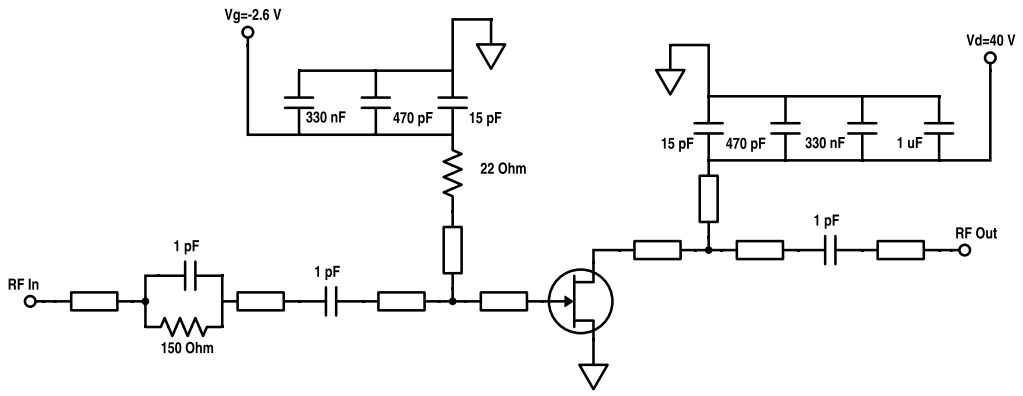


Figure 3.19: Circuit level schematic of one amplifier branch illustrating the lumped components used in the circuit. A 150 Ω series resistor in parallel with a 1 pF capacitor is stabilizing the amplifier at the input. A 22 Ω resistor is also placed before the input bias network for the same reason.

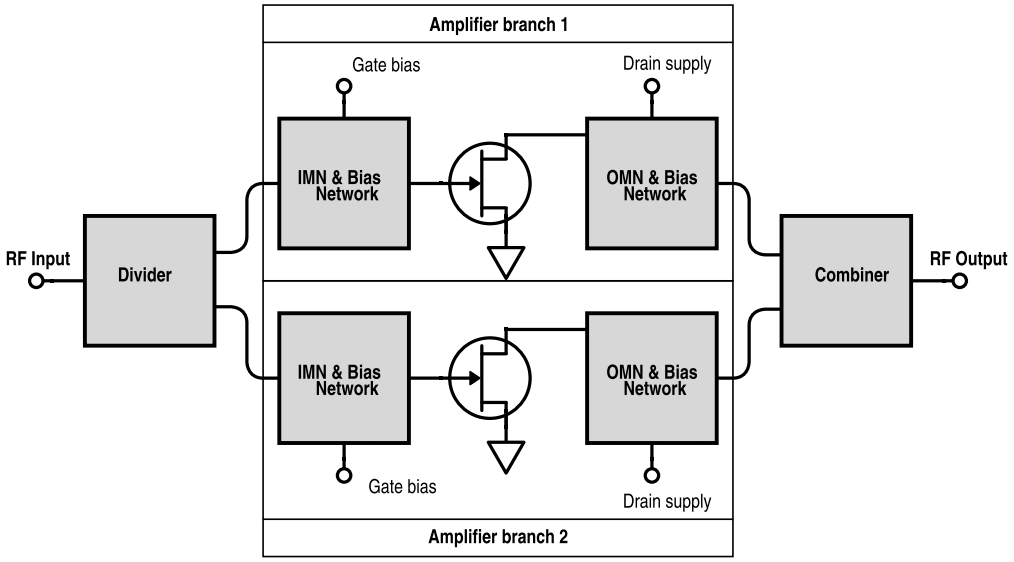


Figure 3.20: System level overview of the power amplifier. The incoming RF signal is divided equally towards the two amplifier branches. Identical input and output matching networks with incorporated bias networks feed the two transistors. The two output signals are then fed to a combiner feeding the RF output. Bias voltages are independently applied to the amplifier branches.

An overview of the final component values used for the two individual amplifier branches of the combined amplifier can be seen in figure 3.19. A system overview of the entire power amplifier can be seen in figure 3.20. This overview shows all the sub circuits used to form the complete amplifier.
The final design layout was then exported in a suitable format for manufacturing. The areas of the circuit consisting of copper were exported as a PDF to enable further processing of the layout during the fabrication, see figure 3.21 for an image of the output.
Figures 3.22, 3.23, 3.24, 3.25, 3.26, 3.27 show the EM simulated performance of the final amplifier ready for prototype fabrication.

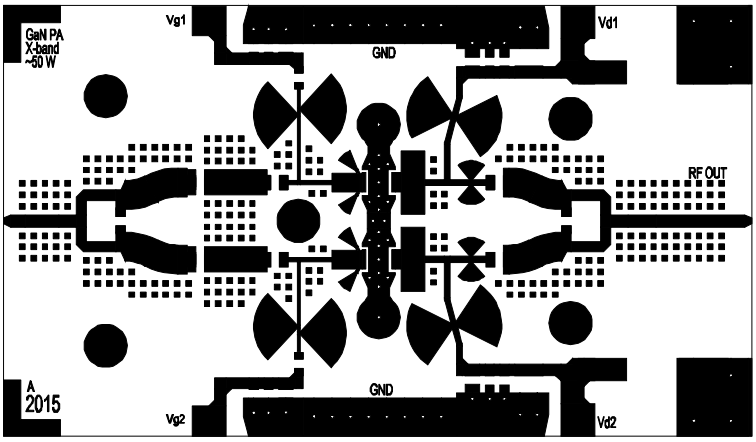


Figure 3.21: Final layout of the design used for fabrication. Total layout size is 66 mm x 38 mm. All black colored areas represent copper, white is bare substrate.

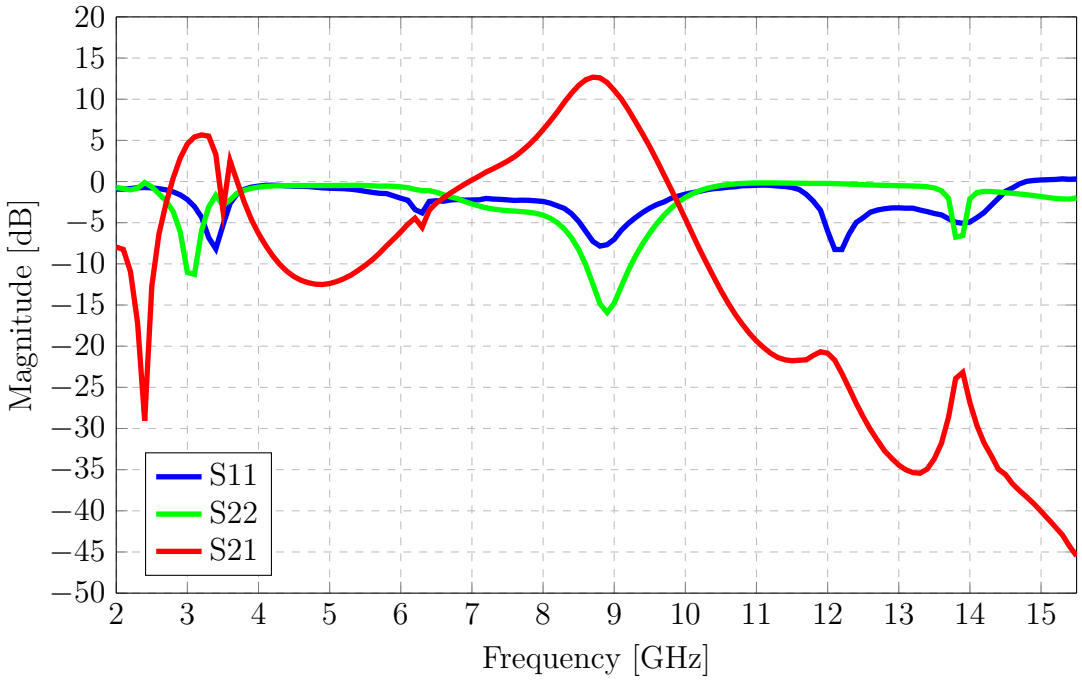


Figure 3.22: Simulated magnitude of s-parameters over wide frequency range.

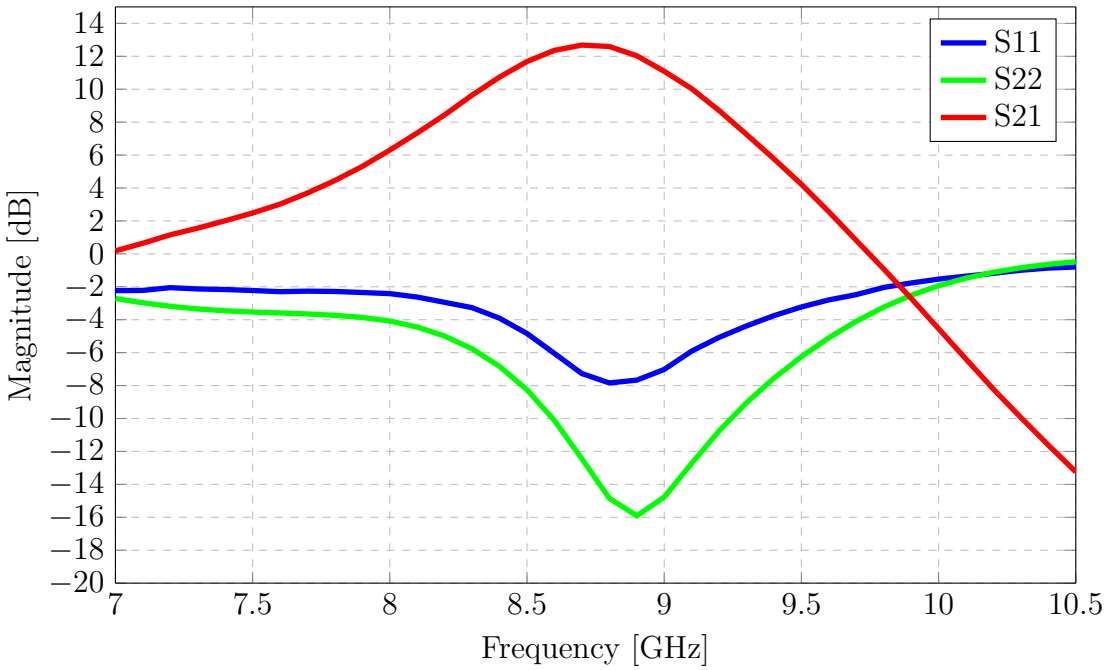


Figure 3.23: Simulated magnitude of s-parameters over narrow frequency range.

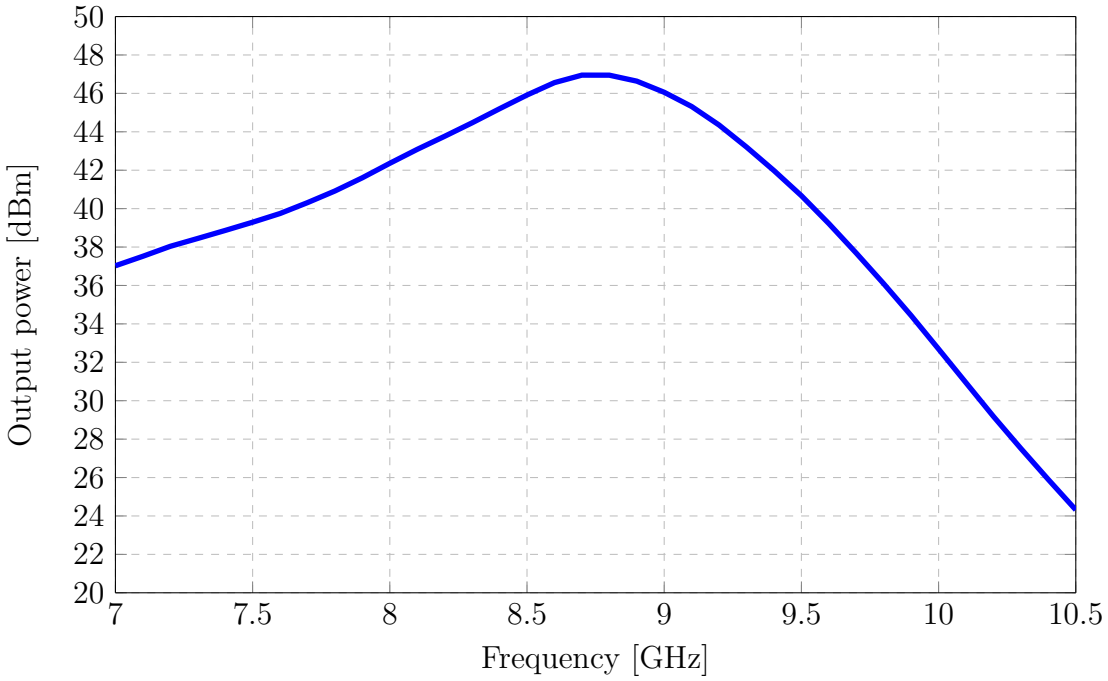


Figure 3.24: Simulated output power as a function of frequency at $P_{in} = 40\ dBm$.

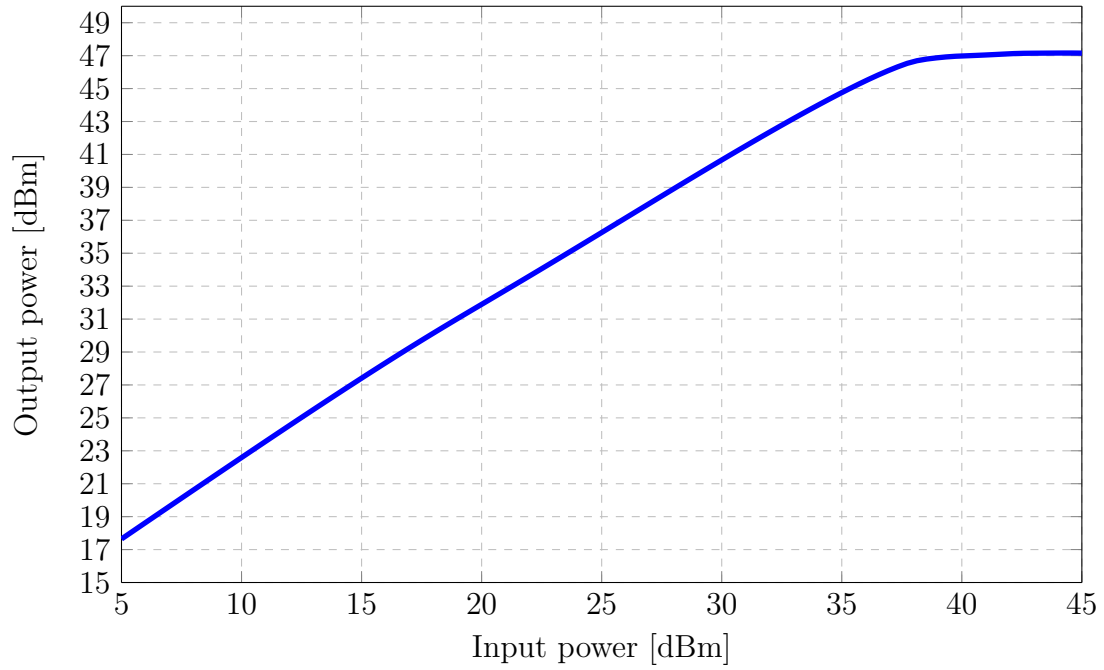


Figure 3.25: Simulated output power as a function of input power at 8.75 GHz.

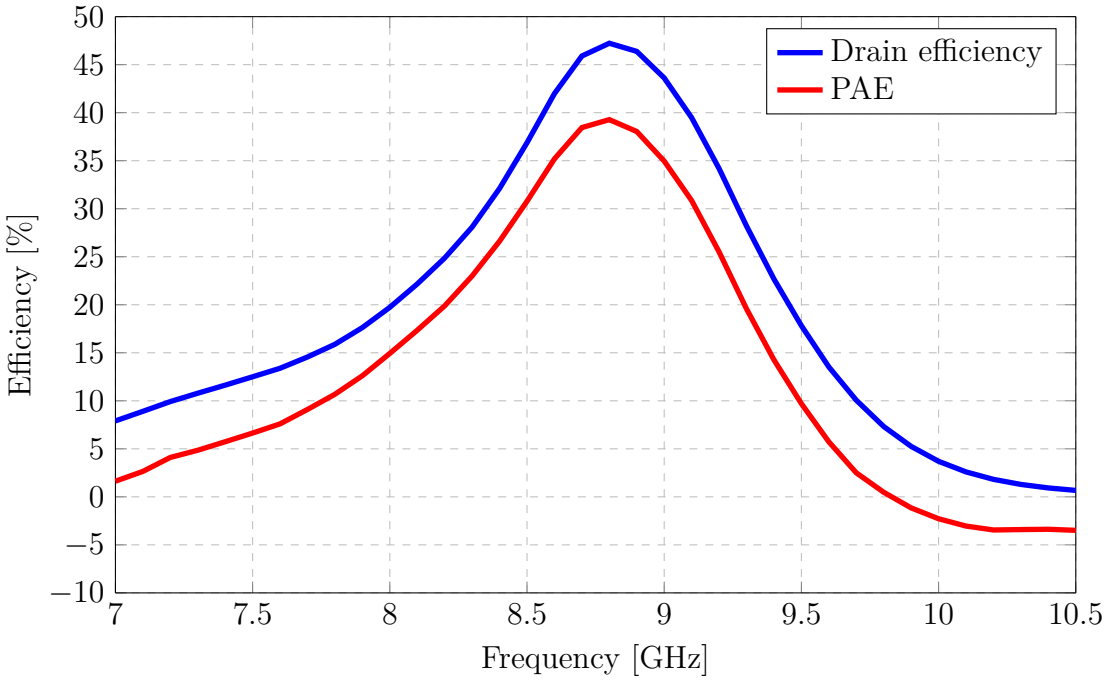


Figure 3.26: Simulated drain efficiency and power added efficiency against frequency at $P_{in} = 40\ dBm$.

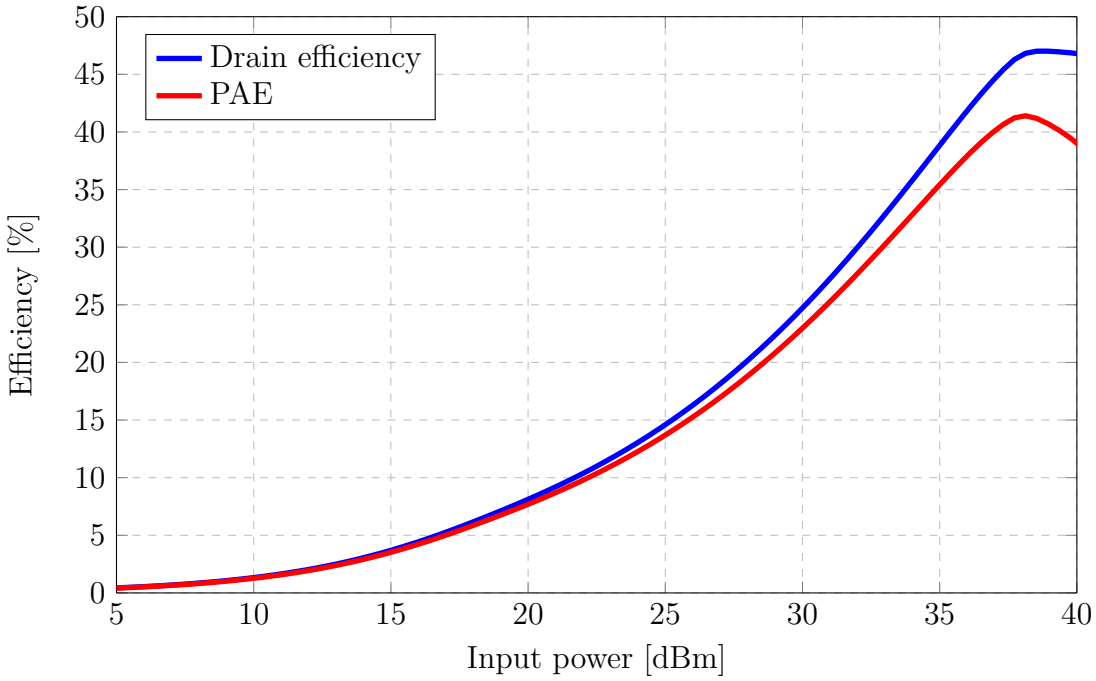


Figure 3.27: Simulated drain efficiency and power added efficiency against input power at 8.75 GHz.

3.4 Fabrication of prototype

A physical prototype was then manufactured to investigate how close the performance of the circuit would be compared to the simulated circuit. A printed circuit board was manufactured according to the design developed during the design phase of the project. The printed circuit board was then populated with all the lumped components needed, including the transistors. Connectors were then soldered on the board for RF and DC connections to external devices.

3.4.1 Printed circuit board

The printed circuit board (PCB) was manufactured using a chemical etching technique. The final layout of the copper layer was printed mirrored on a transparent plastic sheet. A mirrored print out will cover the copper clad more tightly and produce a sharper exposure. The plastic mask was then placed on top of a copper clad board covered with etch resist. The copper board was then exposed to UV light to activate the resist. The copper clad board was then placed in a bath of 7-8 % sodium hydroxide solution to remove the etch resist from areas to be etch away later. The copper board was then immersed in a solution of hydrochloric acid and hydrogen peroxide to etch away the unwanted areas of copper while the resist covered traces are left intact.

The etched board was examined under a microscope with 40x magnification to inspect the copper areas on the substrate. The copper traces were checked to not include any unwanted open or short circuits. The overall quality of the etching process was also evaluated to be able to decide which printed circuit board that could be used for the final circuit. Several samples had to be manufactured to find a decent quality board. Some imperfections found on the copper areas could be repaired by applying a small amount of solder over the area.

Via holes are essential to connect the top copper layer with the bottom copper layer through the substrate. Via holes are typically drilled and then plated through using an electroplating process to make the walls of the drilled hole conductive. This process is complex and requires expensive equipment to be performed with good result. This process is most often performed by the foundry responsible for the printed board manufacturing because of this reason.

Via holes could not be made the traditional way since the printed circuit board used for this project was manufactured manually. An alternative method was instead used to make the via holes. Holes were drilled as normal but copper wires were then instead inserted into the holes and then cut off nearly flush with the copper surface on the board. A hammer and anvil was then used to flatten the top of these rivets. The resulting via will bulge a little, but this excess material could be filed away to make the surface as smooth as possible. It was especially important to have a flat ground pad for the transistor package to mount against. Figure 3.28 illustrates this process with a before and after picture of the via holes placed under the transistor. These solid via holes have more mass compared to ordinary plated vias. This property would improve the heat conduction capability of each via.

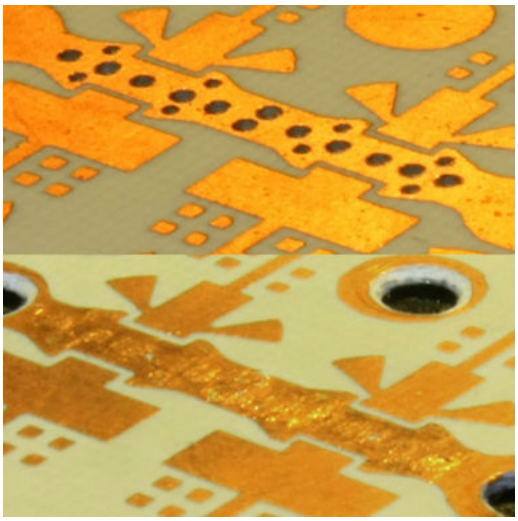


Figure 3.28: Process of fabricating copper filled via holes in the printed circuit board to create a good heat sink and ground.

3.4.2 Connectors

RF and DC signals must fed to the amplifier through good connections to eliminate coupling problems. SMA to board connectors from the company Rosenberger (32K441-600L5) were used at the input and output RF terminals of the amplifier circuit. These connectors are screwed on to the mounting fixture and a tab from the center pin is soldered directly to the trace on the PCB. These connectors are specified to work in the frequency range from DC to 12.4 GHz, having an insertion loss of 0.07 dB at 9 GHz.
DC power is fed to the circuit by a simple copper pad on the PCB itself. The connectors are individual for both transistors to allow for independent adjustment of the quiescent drain current.

3.4.3 Soldering and assembly

The transistors were mounted on the printed circuit board first of all, since they were expected to be the most difficult components to solder. The transistors could not be soldered using any traditional method since the package is of DFN type with no leads to apply solder to. Solder must be applied to the underside of the component and then must the board together with the component be heated using some method to fully make the component bond with the copper on the board. These types of packages are usually soldered to the board by applying solder paste to the copper pads on the board. The solder paste is a mixture of small solder balls and flux. The component to be soldered can then be placed on top of the pads and solder paste. The board is then inserted into an oven, were the temperature is raised in a controlled way until all the solder paste has melted and secured the component to the board. Another method was used to solder the transistors in this project, since this was a prototype that only required two DFN packages to be soldered. The soldering area was first cleaned with alcohol to remove dirt and residues left from

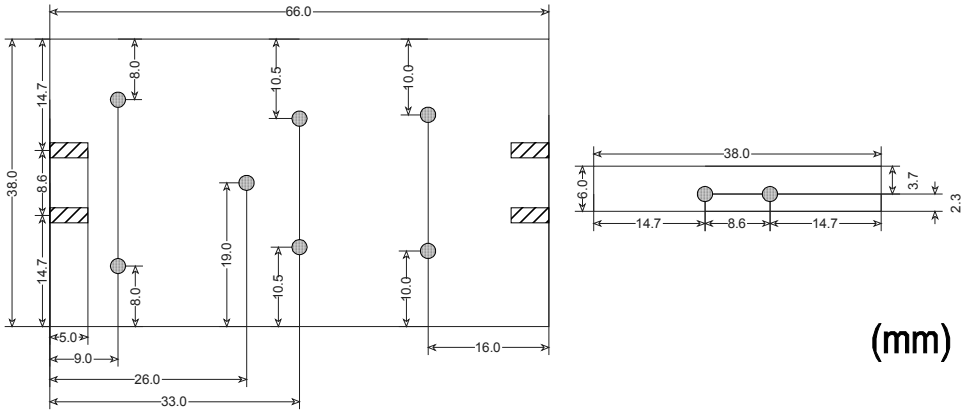


Figure 3.29: Drawing of the mounting fixture used to secure the printed circuit board.

the fabrication. A small amount of solder paste was applied to the copper pads of the transistor footprint. The solder paste was distributed as evenly as possible over the board area to ensure a good solder joint for all pins on the transistor package. The transistor package was then placed on the board as precise as possible. The underside ground plane was then heated with a soldering iron fitted with a flat-headed tip. The heat will travel through the vias to the area to be soldered. The soldering iron was held to the board long enough to fully melt all the solder on all pads under the package. Final adjustments on the position of the package could be done before the soldering iron was removed and the solder was left to cool.
Resistors and capacitors were then mounted to the board followed by connectors for RF and the bias supply circuitry.

3.4.4 Mounting fixture

A mounting fixture for the amplifier circuit board was manufactured using 6 mm thick aluminium, see figure 3.29 for more details. The fixture should hold the circuit board and connectors securely in place and most importantly it should conduct heat away from the board. The heat sinking properties of the mounting fixture should allow the circuit to operate within safe temperature levels. A small amount of thermal grease was applied to the area directly under the transistors to further increase the thermal conductivity. The circuit board was secured to the mounting fixture using a number of screws. The SMA connectors for the RF signal were also screwed directly to this mounting fixture.

3.4.5 Verification and troubleshooting

The assembled board had to be tested beforehand to ensure safe operation during the first power up. The circuit board was checked for short or open circuits by eye and by using a continuity tester. The transistors were tested by measuring the resistance with an ohm meter between drain and ground with the gate turned on and off. This test procedure would ensure that a good connection between the board and

transistor package had been made. The resistance to ground on all copper surfaces connected to ground with via holes was also checked with the ohm meter.
One of the RF connectors going from SMA to the circuit board had some strange coupling issue that attenuated the signal very strongly. This could be solved by just applying more solder to the area bonding the center pin to the copper trace on the board.

3.4.6 Tuning and setup

Tuning arrays were placed around and alongside all distributed components of the circuit to enable easy tuning if needed. These tuning arrays consists of simple copper pads placed with constant intervals around transmission lines of the layout. The tuning array should not affect the performance of the original circuit layout, thus putting requirements on the spacing between the layout and tuning array to be sufficient.
Some efforts were made to improve the performance by tuning of the layout. Small pieces of copper on top of a wooden stick were placed around the layout while the circuit still was connected to a network analyzer. This was in reality very difficult to succeed with since very small adjustments had to be made.
Already available bias circuits were connected to the gate, drain and ground terminals of both amplifier branches individually. These bias circuits could be set up to deliver an adjustable gate voltage while the drain voltage was held constant at 40 V. This enabled the idle drain current to be set to a desired value for the two transistors independently.
The input of the amplifier was terminated with a 50 Ω load and the output was connected to a spectrum analyzer through an attenuator. The spectrum analyzer set at displaying a full span from low to high frequencies was used to find possible oscillations occurring when increasing the bias voltage. These oscillations could otherwise potentially destroy components on the circuit.
The gate voltage of both amplifier branches was set so the measured idle drain current was around 160 mA, the value given by the simulations performed earlier. This procedure was executed with the bias circuit set to run in constant CW mode without a pulsed gate bias and drain supply.
Figure 3.30 shows the final fabricated board mounted on the fixture and also on an external heat sink.

3.5 Measurements on prototype

The prototype was tested using available measurement instrumentation in a microwave laboratory at SAAB. Instruments used have been listed in table A.1 in appendix A. S-parameters were first measured to confirm the performance of the amplifier compared to the results generated during the simulation phase. It was important to verify and analyze the performance at lower power levels, before increasing the power during the following power measurements.

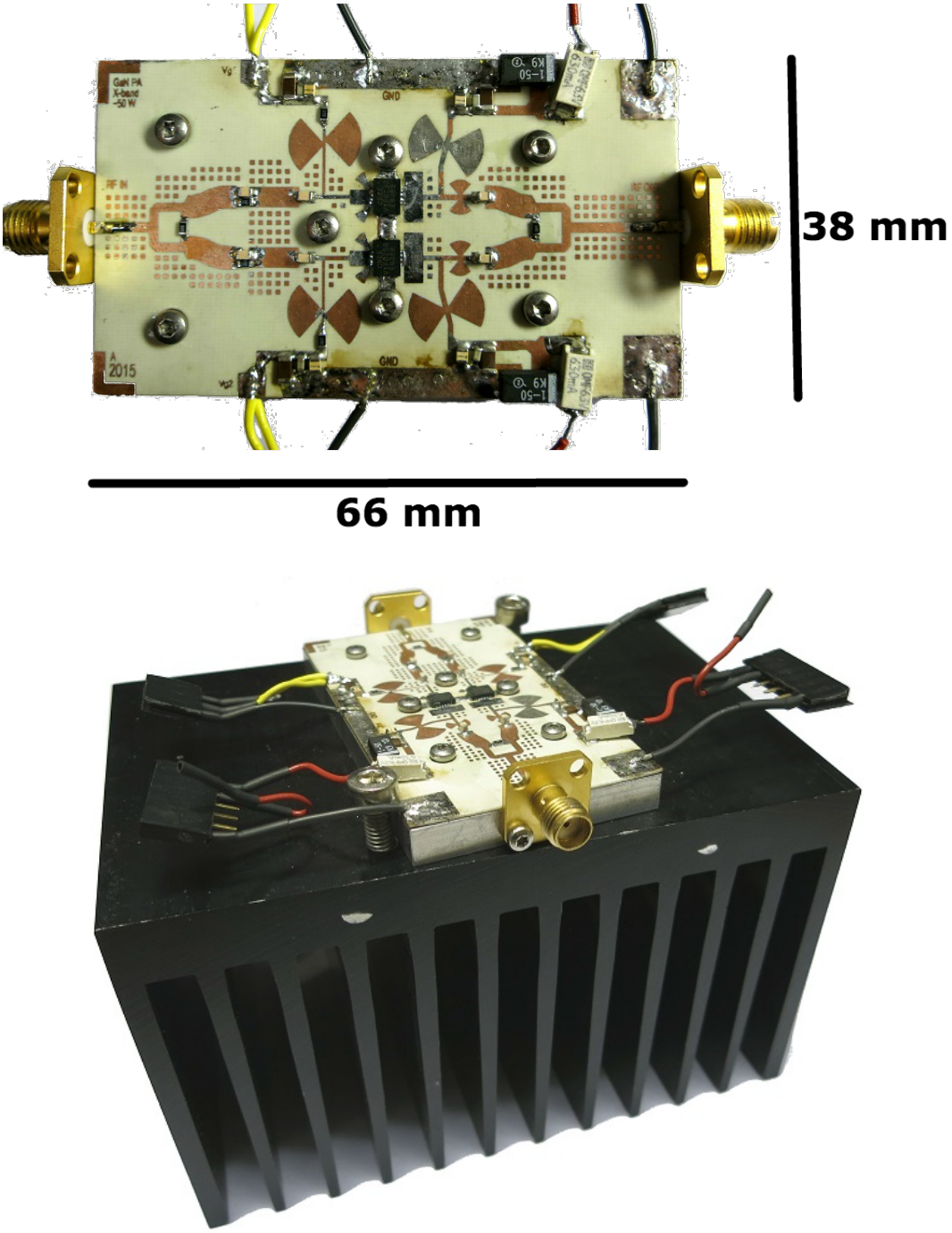


Figure 3.30: The fabricated prototype board above and below the same board mounted to a heat sink.

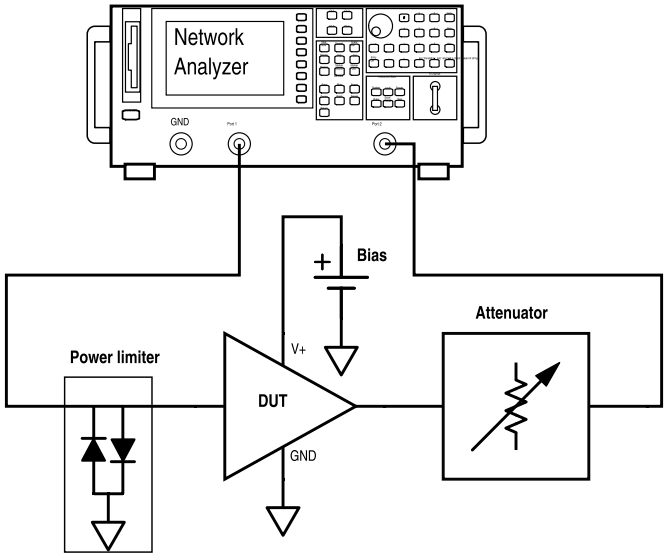


Figure 3.31: Overview of the setup used to measure the s-parameters of the amplifier. A 10 dBm power limiter and a 30 dB attenuator was used.

3.5.1 S-parameter measurements

S-parameters of the power amplifier were measured using a two-port network analyzer including some needed protection hardware to protect the ports of the network analyzer. An overview of the test setup used to measure the s-parameters can be seen in figure 3.31. The output power of the network analyzer was set to 0 dBm during all s-parameter measurements. Measurements were performed twice, once over a wide frequency range between 2 GHz and 15.5 GHz and then over a more narrow range around the center frequency between 7.4 GHz and 9.4 GHz. The network analyzer was calibrated both times using a short, open, load and thru calibration standard.

The measurements were taken with the amplifier biased for normal operation based on results from previous simulations. A power limiter was connected between the first port of the network analyzer and the input of the amplifier under test. The power limiter would protect the instrument from any reflections caused by the amplifier. An attenuator was also connected between the amplifier output and the second port of the network analyzer to limit the output power reaching the instrument. The attenuator consisted of two attenuators connected in series, first a 20 dB attenuator followed by a 10 dB attenuator. The attenuator was characterized by individually measure the s-parameters of it, these could then be used to correct the measurements taken.

The calibration was performed with the power limiter included, but not the attenuator since it would attenuate the signal to much for the receiver inside the instrument. The S_{22} s-parameter could not be measured since the attenuator would interfere with the measurement.

Measurements of S_{11}, S_{12}, S_{21} were saved for further analysis. Data for S_{12} and S_{21} had to be corrected using the data previously gained from measurements of the attenuator used. This was done by importing s-parameter data from both mea-

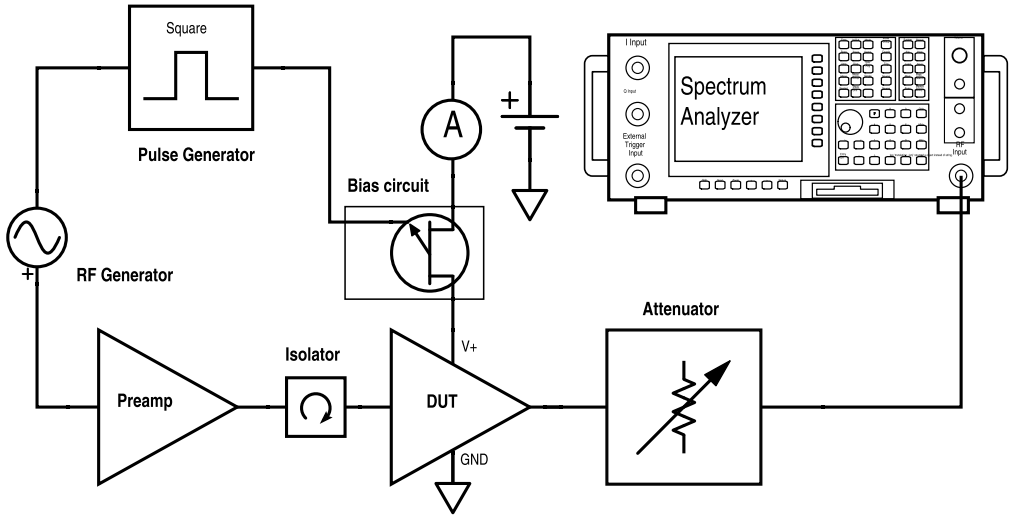


Figure 3.32: Overview of the setup for measuring the output power of the amplifier.

surements into Microwave Office and then subtract the attenuator data using a de-embedding operation.

3.5.2 Power measurements

The output power of the amplifier was measured with another setup, since the network analyzer could not generate enough power for the input of the amplifier. The power measurements were performed with a pulsed input signal to keep the average power low and to reduce the thermal stress on the transistors.
An overview of the test setup used during the power measurements can be viewed in figure 3.32. A bias circuit with capability to turn the gate on and off with a control signal was used to switch the bias supply to the amplifier during the measurements. An RF generator created the high frequency input signal, also this source was pulsed with a control signal. A pulse generator set to generate an output pulse with a 100 μs period and 10 % duty cycle was used as the control signal for the RF generator and bias circuit.
The RF generator could not generate an output signal with high enough power. An X-band drive amplifier had to be used to boost the input signal before it reached the amplifier under test. An X-band isolator was connected before the input to the amplifier under test to terminate back reflections.
The same attenuator used during the s-parameter measurement was reused to limit the output power of the amplifier under test and protect the following instrument from too high power levels. A spectrum analyzer was used to measure the output power. The spectrum analyzer was set to measure with zero span at the frequency of the input signal. This would cause the instrument to display the envelope of the pulsed signal and enable a measurement marker to be placed at the top of the pulse. An average of 100 samples were taken to smooth out the displayed power level. The entire setup was switched on during a time period before the actual measurements were performed to enable all components to warm up and stabilize.

The drive amplifier had to be characterized in terms of output power before the actual power measurement on the test circuit. The input power at the input of the test amplifier had to be known in order to get accurate results. This measurement was performed with all hardware connected, except the amplifier to be tested. The output level of the signal from the RF generator was stepped with 1 dB intervals and the output level displayed by the spectrum analyzer was noted.
The actual power measurement on the test amplifier could then commence. The amplifier was connected and the pulsed bias was activated. The pulse used had a period of 100 μs with 10 % duty cycle. The output of the RF generator was then enabled with the drive amplifier already running.
The output power was measured at the maximum gain peak measured during the s-parameter measurement. The generator and spectrum analyzer were therefore set to work at 8.4 GHz. The input signal was then swept from low to high power with the output power noted as before. The supplied DC current to the test amplifier was measured with a multimeter set to measure the DC current. This value was also noted along with the output power.
The efficiency was calculated from these measurements by methods described earlier in the theory section. The current during the pulse had to be used in these calculations, but the average DC current was measured. The average value was converted to a peak value using the formula

$$I_{peak} = I_{average} \frac{100}{\text{Duty cycle (\%)}}$$

The next measurement was taken with the input power level fixed at 40 dBm. The frequency was instead swept around the center frequency of 8.4 GHz. The same measurement method was applied as before.
The thermal performance was also evaluated with a 40 dBm input power level at frequency 8.4 GHz. A thermal imaging device was used to measure the temperature gradient around the transistors.

3.5.3 Error sources

Errors can be present in most stages of the measurements. These errors could affect the final result in several ways, they can be both significant or insignificant in nature. Human errors are the most probable error source when performing complex measurements. Not just the measurement itself can cause errors, there could also be errors made during the post processing of the measurement data.
Calibration errors are another main error source. Used instrumentation have been calibrated frequently, but there could be deviations.
Measurements are always affected by measurement uncertainties. These could be affected by external factors, as temperature or humidity.

4
Results

Results generated through measurements on the prototype will be presented in this chapter. All measured values are presented using solid thick traces and all simulated values are displayed using dashed traces. Simulated values are based on EM simulations performed during the simulation phase.

4.1 S-parameters

S-parameters S_{11} and S_{21} measured over the wide frequency range are shown in figure 4.1 and over the more narrow range in figure 4.2. The measured device reach peak performance at a frequency around 350 MHz lower compared to simulated results.

4.2 Output power

Figure 4.3 shows the output power measured over the frequency band and figure 4.4 shows efficiency over the same band. The same frequency shift can also be observed in these measurements.
Figure 4.5 shows the results generated when measuring the output power as a function of input power. Measurements of drain efficiency and power added efficiency are illustrated in figure 4.6.

4.3 Device temperature

Figure 4.7 displays an image showing the temperature gradient of both transistor packages.

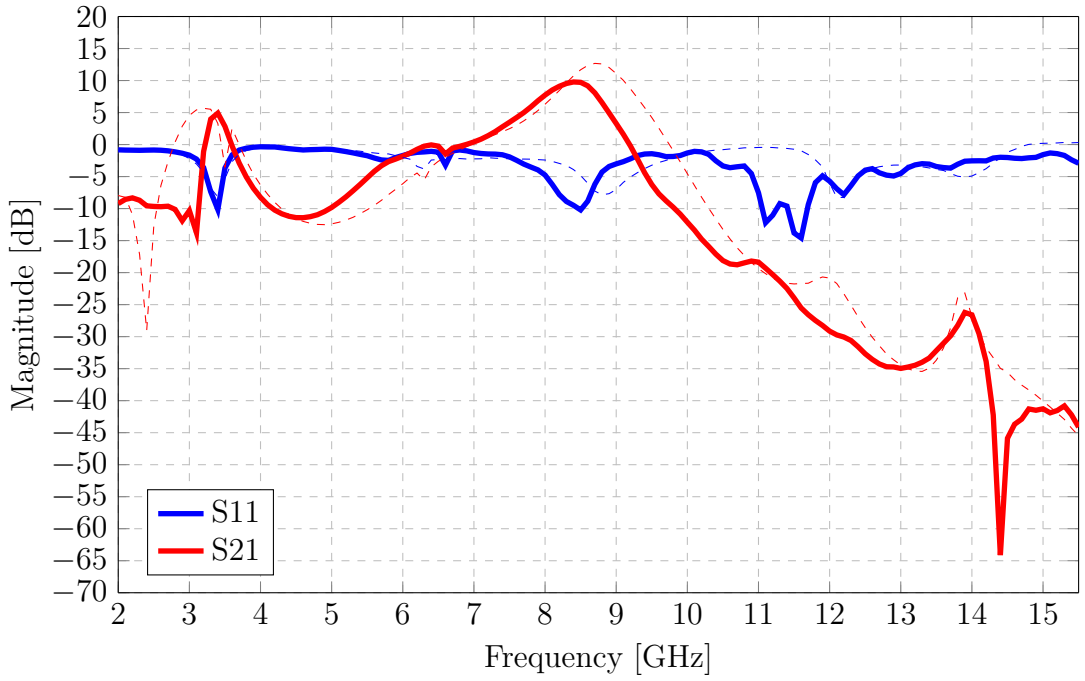


Figure 4.1: Measured S11 and S21 versus frequency between 2 GHz and 15.5 GHz. Measured at $P_{in} = 0\,\text{dBm}$. Solid traces represent measured values and dashed traces are results from EM simulations.

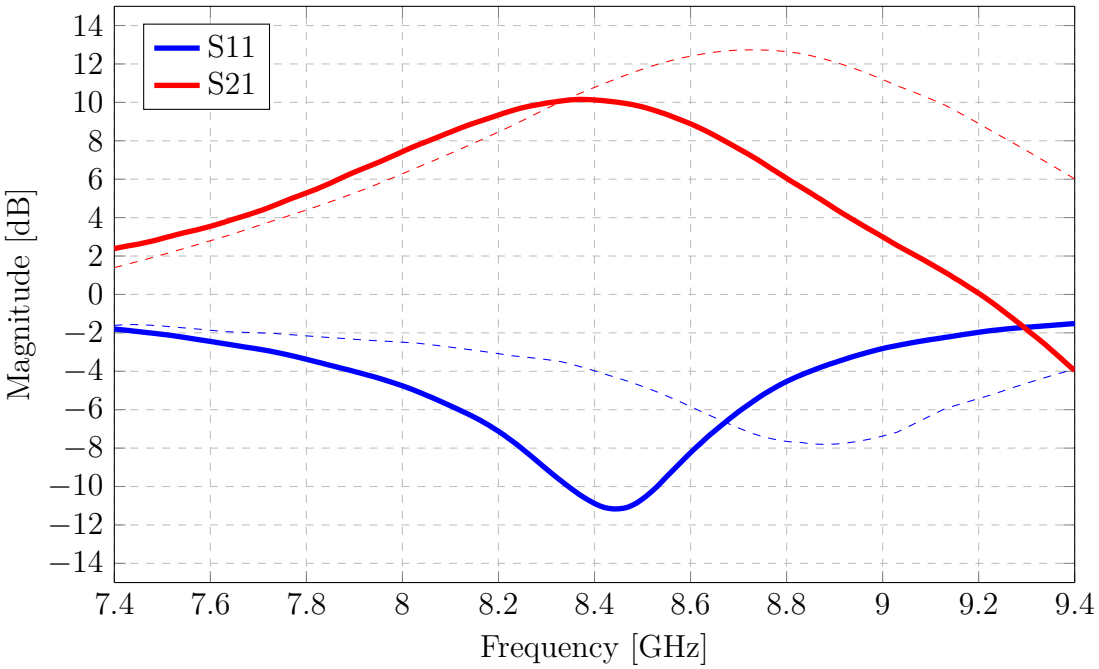


Figure 4.2: Measured S11 and S21 versus frequency between 7.4 GHz and 9.4 GHz. Measured at $P_{in} = 0\,\text{dBm}$. Solid traces represent measured values and dashed traces are results from EM simulations.

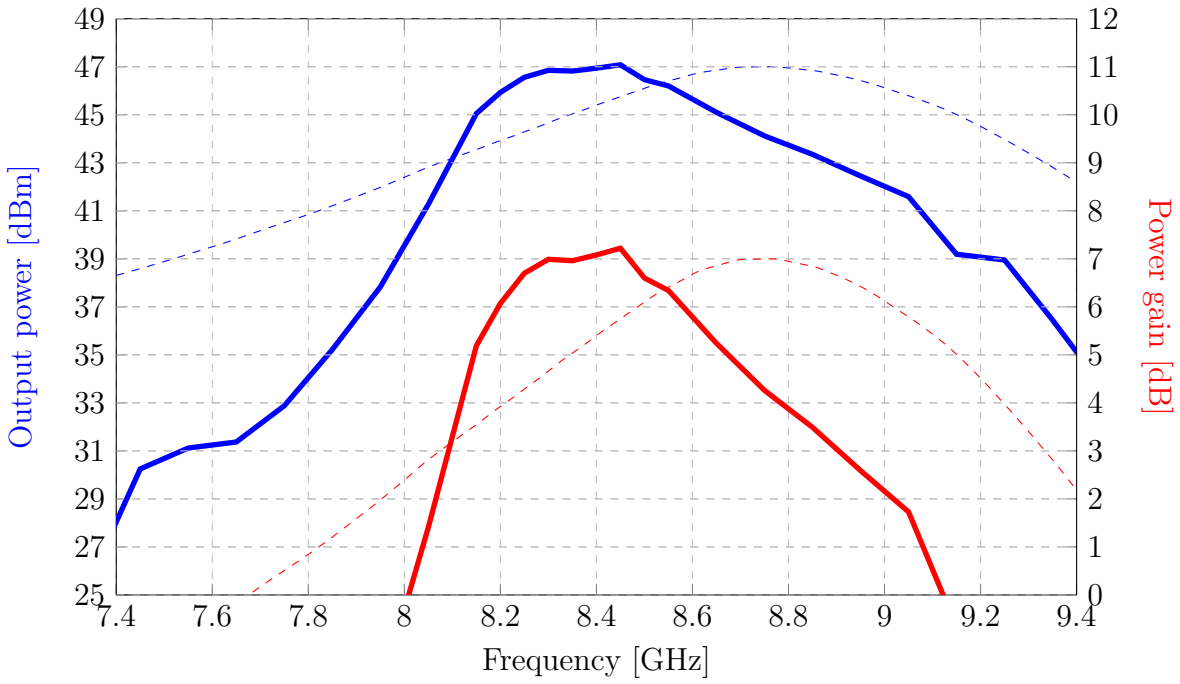


Figure 4.3: Measured output power versus frequency. Measured at $P_{in} = 40\,\text{dBm}$. Solid traces represent measured values and dashed traces are results from EM simulations.

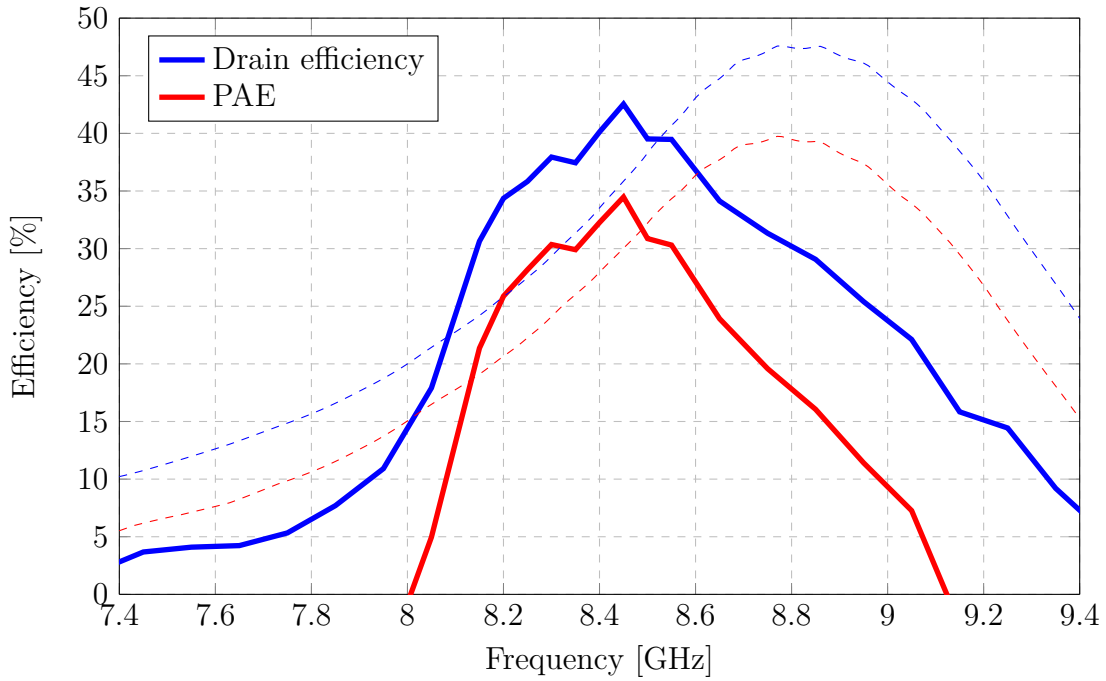


Figure 4.4: Measured drain efficiency and PAE versus frequency. Measured at $P_{in} = 40\,\text{dBm}$. Solid traces represent measured values and dashed traces are results from EM simulations.

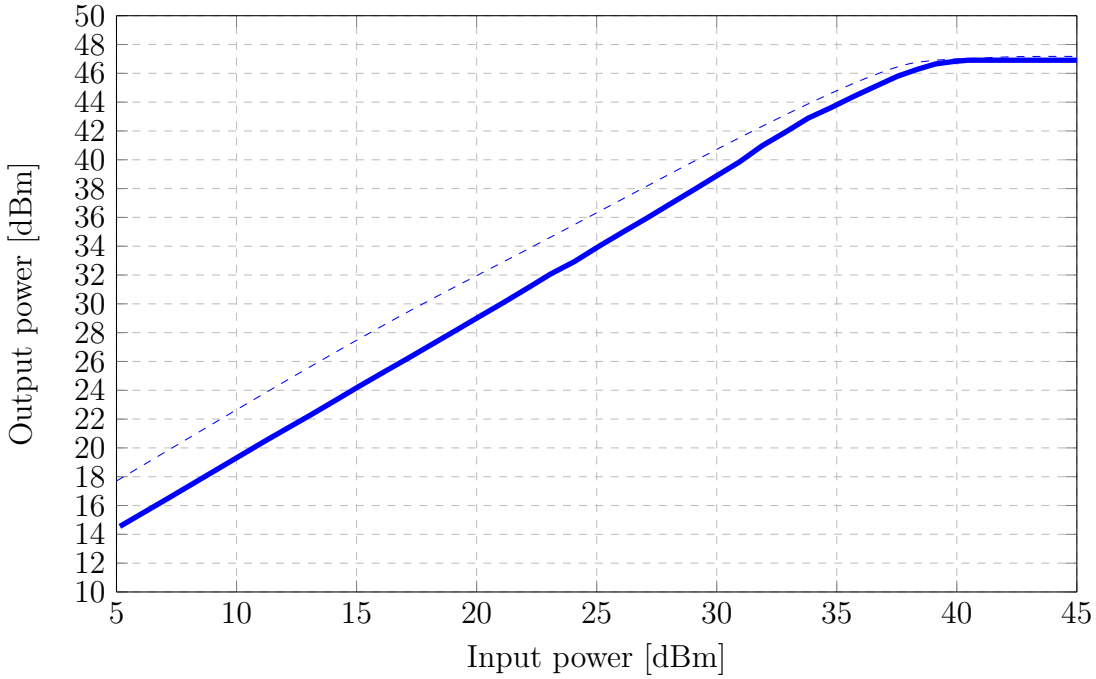


Figure 4.5: Measured output power versus input power. Measured at 8.4 GHz. Solid traces represent measured values and dashed traces are results from EM simulations.

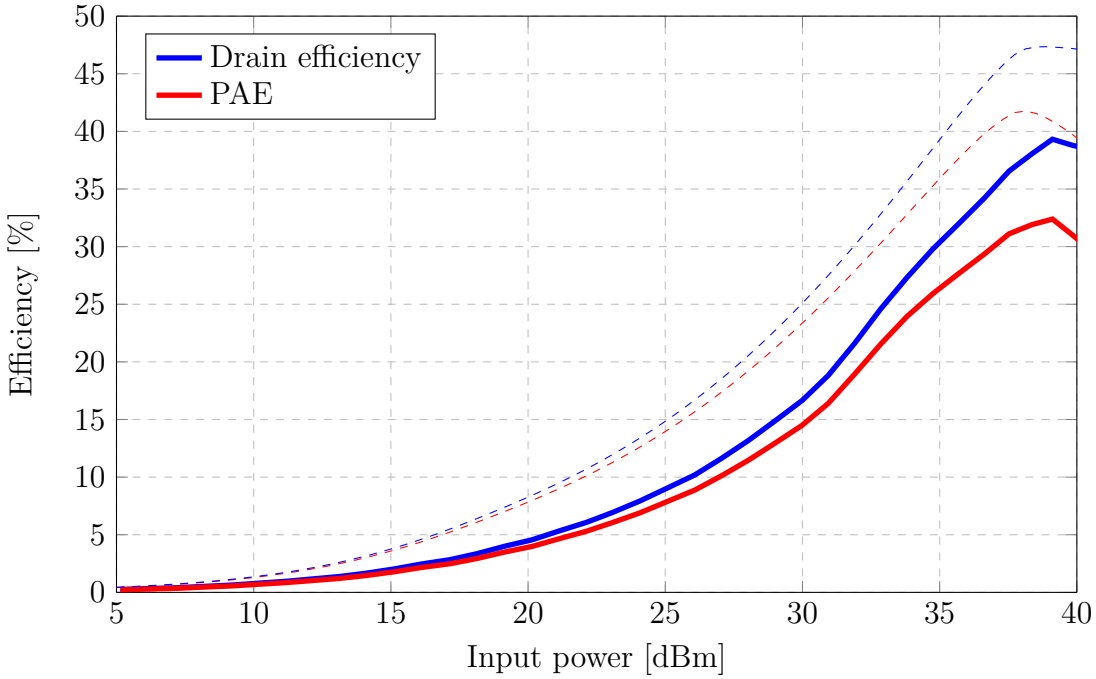


Figure 4.6: Measured drain efficiency and PAE versus input power. Measured at 8.4 GHz. Solid traces represent measured values and dashed traces are results from EM simulations.

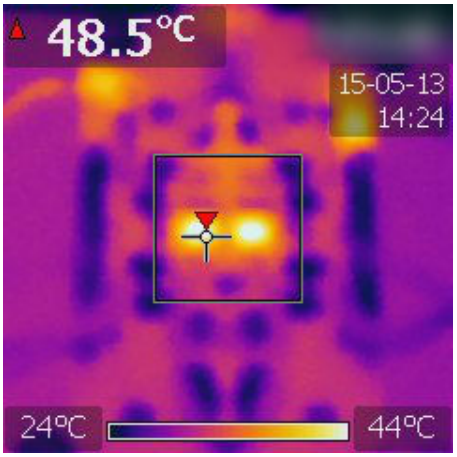


Figure 4.7: Image captured using an infrared camera showing the temperature gradient of the transistors mounted on the circuit board. Measured at 8.4 GHz and $P_{in} = 40$ dBm.

5
Discussion

There are many crucial steps involved when designing a power amplifier for a prototype build. The simulation of the circuit itself relies on many input parameters. These parameters must be chosen properly to make the simulation reliable. It can sometimes be difficult to know if the results generated by the simulation software can be trusted.
The final measurements performed showed slightly different results compared to the results generated during the simulations. The goal set for saturated output power was reached, but at a lower frequency. Some changes should always be expected, but consistent variations can indicate some error caused by some global parameter. It is very difficult to capture all the characteristics of a physical circuit within the simulation software. The circuit model can be very ideal even if care have been taken to supply the model with many input parameters.
A fabricated circuit will always be different due to manufacturing tolerances and imperfections generated during the build. It is therefore important to make the circuit robust to small changes in order to still get the wanted performance out of the circuit.
The exact placement of the transistor package on the footprint could affect the performance. The placement will decide where on the microstrip the pins on the package will connect. The impedance seen by the transistor could potentially change due to this fact.
A difficult task during the simulation phase was to know how to set up the simulation to correctly simulate the copper footprint together with the transistor model. The model is supposed to have its reference plane directly at the pins of the package, excluding any footprint. The performance changed when the transistor footprint was included in the EM simulation compared to when not. The distance between the transmission lines of the matching networks and the center ground pad is very short, only 0.2 mm. The coupling between these areas can be assumed to be significant. Solder will also be present in this area when the transistor has been soldered. This may change the spacing and potentially also the performance.
The via holes under the transistor will introduce inductance between the ground pad of the transistor and the bottom ground plane. This inductance may also affect the measured performance. The via holes were included during the simulation phase, but the model may not have been able to correctly model these special via holes.
The relatively rough surface under the transistor due to placement of via holes is another factor not included when performing the simulations.
The Wilkinson dividers used could potentially have limited the bandwidth of the amplifier, but the measurements performed on only the Wilkinson divider showed

acceptable performance. The amplifier branch itself should probably be the main uncertainty, since no measurement was performed on only a single amplifier branch without the divider.
Lumped components could not be EM simulated, but were simulated using models supplied by the manufacturer. These models are based on certain assumptions regarding placement and orientation on the circuit board. These conditions may not have been true during this simulation. The lumped component model used could in this way have been responsible for some of the performance shift observed.
The circuit board could be made reasonable small in size. The designed input matching network occupied more board space than the network at the output. The input network could perhaps been made smaller to shrink the total size. RF connectors could also been placed closer to the circuit itself to save some more board space.

6
Conclusion

The saturated output power of the amplifier reached 50 W, but only within a narrow frequency band. The performance peak was positioned lower in frequency than when simulated.
Efficiency peaked slightly above 40 %, around 6-8 percentages worse than expected. The overall bandwidth was narrower when performing power measurements. S-parameter measurements showed better bandwidth performance.
The fabrication of the prototype could be performed as planned. Only small modifications had to be done to make the design work.
The performance of the designed amplifier compared to the commercial reference amplifier offered twice the output power, but within a slightly narrower bandwidth. The size of the prototype amplifier was rather large if compared to a pre-matched amplifier block instead, but the cost can be cut in nearly half.

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A

Measurement equipment

Table A.1: Instruments used to perform measurements.

Instrument	Manufacturer	Model	Info
Network analyzer	Rohde & Schwarz	ZVM 1127.8500.60	10 MHz-20 GHz
Spectrum analyzer	Agilent	E4440A	
RF generator	Rohde & Schwarz	SMR20	10 MHz-20 GHz
Pulse generator	Agilent	81104A	
Drive amplifier	CTT	ASN/096-4242-14	40 dBm
Power limiter	Agilent	N9355B	0.001-18 GHz, 10 dB limit
Attenuator 1	Narda	776B-20	50 W CW, 20 dB
Attenuator 1	Weinschel associates	WA3	10 dB
Isolator	Teledyne	-	X-band
Multimeter	Fluke	79III	True RMS multimeter
Power supply 1	Powerbox	PB3100	
Power supply 2	Switchbox	SB15-20	

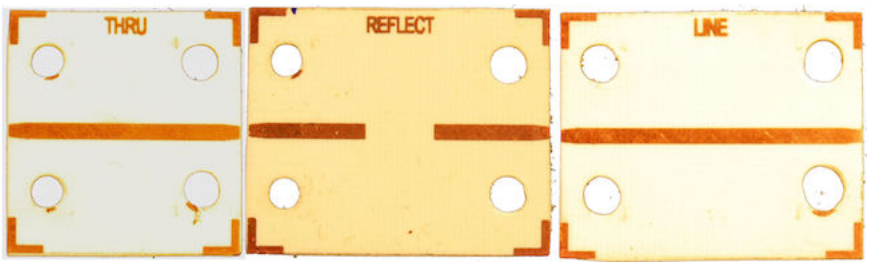

Figure A.1: The custom made TRL calibration kit used to calibrate the network analyzer.