# Direct Measurement of Superconducting Tunnel Junction Capacitance

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*Abstract*—**Superconductor-Insulator-Superconductor (SIS) is the key component for millimeter and submillimeter mixers for radio astronomy and environmental science. The capacitance of the SIS mixer determines both the RF and IF performances. Previously, the measurements of this capacitance have been followed with high uncertainty levels. Herein, we present the characterization of the SIS junction capacitance at cryogenic temperature (~4 K) by direct measurement of the SIS junction impedance at microwave frequencies allowing accurate characterization of the SIS junction capacitance. The proposed calibration method uses only one short-circuit reference. The SIS junction capacitance measurement is realized by biasing the junction at the different parts of its current-voltage characteristic, thus eliminating a separate measurement of short-circuit standard. In order to verify the acquired measurement results, thin-film capacitors with known capacitance were also characterized. The capacitances of four SIS junctions with various areas were measured. The absolute uncertainty of the proposed measurement method was found to vary from 5 to 6.8 % amongst different junction areas.**

*Index Terms*—**Capacitance measurement, Microwave measurement, Superconducting microwave devices, Tunnel junctions, Submillimeter wave devices**

## I. INTRODUCTION

Superconductor-Insulator-Superconductor (SIS) mixers have been a workhorse in radio astronomy receivers for the last few decades. SIS mixers with Nb/Al-$AlO_x$/Nb trilayer are commonly recognized for their lowest-noise performance at operating frequencies up to 1 THz [1]–[3].

The performance of the SIS mixer is largely dependent and limited by its intrinsic (geometrical) capacitance. The SIS junction is produced by means of thin film technology and topologically resembling a parallel-plate capacitor. The impedance of the SIS junction is represented as a parallel connection of the SIS junction quantum impedance (here only the real part $R$ is considered) and the intrinsic capacitance ($C$). In the context of this paper, the differential resistance at areas denoted as A, B, and C (Fig. 1) are designated as sub-gap resistance ($R_{sg}$), gap resistance ($R_g$), and normal resistance ($R_n$), respectively. The $R_nA$ product, where $A$ is the SIS junction area, defines the SIS junction Q-factor value and limits the junction operation band [4]. Additionally, the $R_nA$ value is a measure of the tunnel barrier transparency; the lower the $R_nA$ value, the higher the critical current density of the junction [5]. The $R_nA$ can be measured from the DC current-voltage characteristic (IVC) of the junction and using prior knowledge of the junction area. The specific capacitance ($C/A$) is estimated to be inversely proportional to $ln(R_nA)$ [4]. In order to achieve broadband operation of SIS mixers, low Q-factor (low $R_nA$) SIS junctions should be used [6].

At very low barrier thicknesses the junction quality degrades, which manifests itself in a decrease of the sub-gap resistance and consequently additional shot noise [7]. Also, experiments have shown that at very low barrier thicknesses, the specific capacitance deviates from estimated values [8]. Furthermore, depending on the trilayer deposition techniques, inconsistent values of specific capacitance for the same $R_nA$ value have been reported [8]. There is, therefore, a clear demand for an unambiguous direct method to accurately measure the capacitance.

To date, the most commonly used methods to obtain the specific capacitance have been based on analysis of Fiske steps [9], SQUID structures [10] or the McCumber parameter [11]. In these methods, the capacitance is calculated from a model based on indirect measurement of its effects, e.g., resonance or dispersion of the resonant frequencies. Thus, the estimated value is accompanied with noticeable uncertainty, depending on the accuracy of the aforementioned measurements themselves. The uncertainty also includes assumptions made in the employed models and those related to the material parameters, e.g., London penetration depth in Nb films, the relative permittivity of the sputtered dielectric film and its thickness.

In another method, the escape rate from the tilted washboard potential is studied while a microwave signal is applied to the junction [12]. In this method, also known as time-resolved measurement, specific capacitance of Josephson junction ($R_nA$ ~1200 $\Omega.\mu m^2$) was measured at microwave frequencies with high accuracy. However, for the SIS junctions with $R_nA$ in the range of practical interest ($< 45\ \Omega.\mu m^2$), this method would require cryogenic measurements at 100 GHz and above. Such measurements become technically challenging and less accurate, which diminishes the advantage of the method.

In this paper, we present a technique for characterization of the SIS junction capacitance, which uses direct reflection coefficient measurement of the circuitry where the junction is placed at the end of a transmission line. In practice, when the

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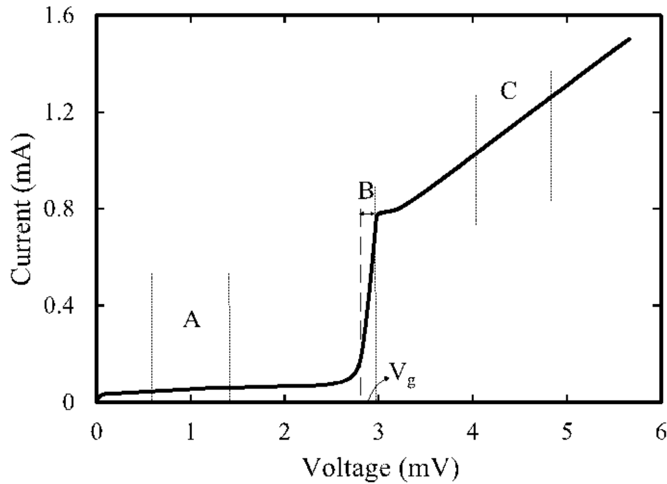


Fig. 1. Schematically shown IV characteristics of an SIS junction when the Josephson current is suppressed. The differential resistances at areas A, B, and C are designated as sub-gap resistance ($R_{sg}$), gap resistance ($R_g$), and normal resistance ($R_n$), respectively. Gap voltage ($V_g$) is defined as the mid-point of the current onset.

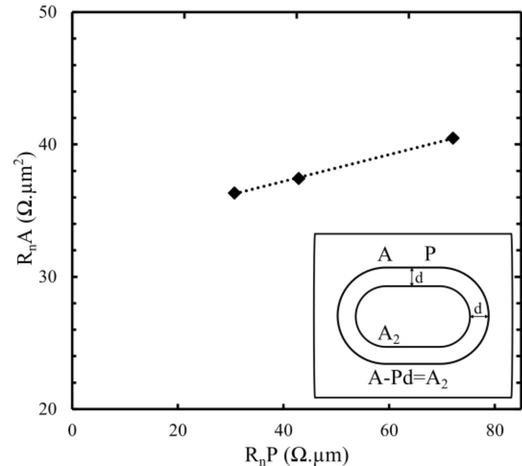


Fig. 2. The plot of $\boldsymbol{R_nA}$ ***versus*** $\boldsymbol{R_nP}$ and the trend line. The inset depicts uniform junction shrinkage of $d$ and its calculation procedure.

junction is biased at the normal-state range (area C at Fig. 1), the impedance of the junction is often very small compared to the 50 Ω impedance of a standard microwave measurement system. Consequently, the effect of the intrinsic junction capacitance on the reflection coefficient is rather masked by a very large mismatch. A rather more pronounced masking effect is seen when the junction is biased at the gap (area B). However, since the differential resistance at the subgap (area A) is high, the effect of capacitance would not be masked. Such distinctive characteristics of the junction at different bias points can be used as calibration standards [13], where the points in areas, A, B, and C on the IVC (cf. Fig. 1.) are employed as open, short and load, respectively.

We present results of direct measurements of SIS junction capacitance at 4 K and the applied calibration method, which allows extracting of the junction capacitance with high accuracy. In the calibration approach, only one point on the area B (a short-circuit reference) is used. The measurement is performed at the subgap (area A) where the effect of the capacitance is less masked by SIS junction differential resistance as discussed above. In order to implement such measurements and evaluate the accuracy of the suggested technique, we fabricated SIS junctions and thin-film parallel-plate capacitors followed by placing them into the test fixtures and performing the measurements as discussed in the following sections.

## II. Fabrication and DC Characterization

The Nb/Al-$AlO_x$/Nb SIS junctions were fabricated in-house following the procedure described in [14]. The SIS junction at the end of a 50 Ω superconducting microstripline is fabricated on a high resistivity Si substrate. This substrate is mounted into a fixture (copper piece), which connects the junction to the SMA connector (with sliding pin). The junctions were fabricated with various dimensions, from which the resulting $R_nA$ value and the actual junction area were estimated. The $R_nA$ value estimation procedure is illustrated in the Fig. 2 insert. In practice, the actual junction area is smaller than the nominal size on the photomask due to the employed fabrication processes, e.g., lithography or photoresist development. We calculate the junction area by $A_2 = A\text{-}Pd,$ where $A$, $P$ and $d$ are the nominal junction area, nominal junction perimeter, and the dimension shrinkage due to the fabrication process, respectively. This assumes $d$ to be substantially smaller than the junction linear dimensions and homogeneous for all dimensions. By multiplying the above calculated area ($A_2$) and $R_n$ obtained from the DC measured junction IVC, and applying linear fitting for the $R_nA$ versus $R_nP$, we obtained $R_nA_2$ value (33.1 Ω.µm²) and the junction linear dimension shrinkage (0.1 µm) as compared to the nominal size. The DC measurements of the junction IVC have been performed in a dipstick using data-acquisition system, controlling DC bias with current stabilization.

In order to verify the proposed SIS junction capacitance measurement technique and the setup, we needed to measure a DUT with known capacitance value. Therefore, planar parallel-plate capacitors using thin-film technology were designed and fabricated. The corresponding capacitance values were chosen within the range of the tested SIS junction capacitances. The capacitor was fabricated with dimensions of 110 µm × 96 µm with two Nb electrodes and 300 nm thickness of sputtered $SiO_2$ ($\varepsilon_r$=3.74 [15],[16]) having the estimated capacitance value of 1.16 pF. For the thin-film capacitor, the same layout of the circuitry as for the SIS junction was used. As will be discussed below, a short-circuit reference is used for calibration. This reference sample was fabricated with the exact abovementioned dimensions but without the dielectric $SiO_2$ layer, thereby having two electrodes in contact.

## III. Measurement Setup

Normal operation of Nb/Al-$AlO_x$/Nb SIS junctions requires cryogenic temperatures, approximately 4 K. Consequently, the SIS junction, mounted at a 4 K temperature stage, is connected to the measurement equipment at room temperature via relatively long stainless steel cryogenic coaxial cables (see Fig. 3) having noticeable losses. The temperature gradient

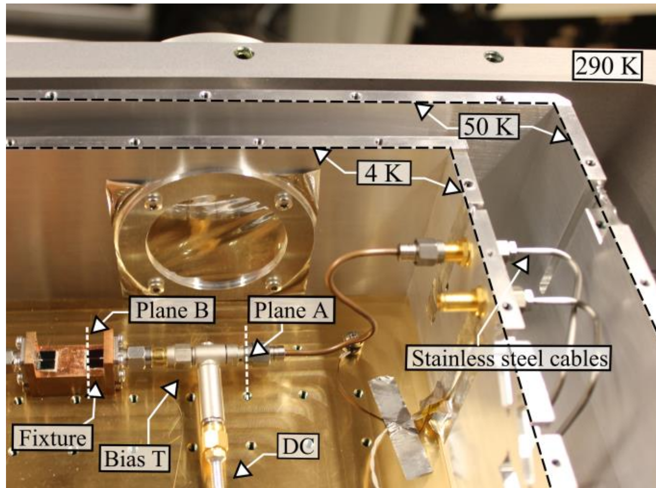


Fig. 3. Cryogenic measurement setup: interior of the cryostat illustrating the 50 K and 4 K stage. The long stainless steel and copper coaxial cables plus the bias T connect the fixture (containing the DUT at plane B) to the PNA. The room temperature calibration is done at the plane A.

through the long stainless steel cryo-cables and corresponding thermal contraction of all materials constituting the cable alters the electrical length and propagation characteristics of the cables. Therefore, room temperature calibration alone would not be adequate for an accurate measurement. Either an *in situ* calibration method or a de-embedding method in addition to the ambient temperature calibration can be utilized to exclude the aforementioned effects. At cryogenic temperatures, the losses are substantially less than at room temperature. The measurements were done using Agilent Parametric Network Analyzer (PNA) E8364B. The PNA still uses the room temperature calibration coefficients, which results in observation of "gain" instead of loss in the measurement due to overcompensation, when performing the measurements at 4 K.

## IV. Calibration

The commonly used Thru-Reflect-Line (TRL) calibration method can accurately determine the error terms and move the reference plane of the measurements to the DUT plane. However, this technique is very sensitive to the quality of the standards and also requires three cooling cycles in addition to the DUT measurement. That makes the measurements sensitive to drift in the PNA performance as a cooling cycle takes approximately 8 - 12 hours.

In our proposed approach, at the first step of the calibration, the measurement setup is calibrated at room-temperature at the A-plane, as shown in Fig. 3. The calibration is performed using the Agilent E-cal module N4691 [17]. Then, cryogenic one-port S-parameter measurements of a short-circuit reference (explained in section II) and the DUT are performed employing time-domain feature in the PNA. Later, these two measurements are used to build equivalent circuit model of both the short-circuit reference and the DUT, from which the impedance of the DUT is extracted.

Since the response of the DUT can be masked by mismatches and unwanted effects from discontinuities, the short-circuit reference is chosen to pinpoint the response of the DUT in time domain.

Once the position of the DUT's response in time is known, we can benefit from the time-domain processing techniques in the PNA [17]. Afterwards, the time gating procedure [18] is used to isolate the reflected signal at the DUT plane from other parasitic reflections both for the short-circuit reference and the SIS junction in a similar fashion as was performed in [19],[20].

Because of the gating span (1 ns), the result still contains response from the circuitry beyond calibration plane A in Fig. 3. De-embedding of all the aforementioned components could be done through modelling them as a 2-port 50 Ω transmission line in. e.g., our case by employing Advanced Design System (ADS), Agilent [17].

The described procedure was applied for thin-film capacitor, however, was modified for SIS junction calibration procedure. The junction could be biased at different voltages on the IVC (cf. Fig. 1) and consequently exhibit different differential resistances. Permanent magnets were utilized to suppress the Josephson current and slight changes in differential resistances of the SIS junction IVC were observed depending on the position of the magnets relative to the junctions.

Once the junction is biased at the gap-voltage, the very small differential resistance ($R_g$~1 Ω) shunts the junction capacitance. Therefore, the gap voltage biased junction can be considered as the short-circuit reference. This modification has the advantage of obtaining both the short-circuit reference and capacitance measurement responses by physically the same device and in the same cooling cycle.

The choice of implementing the short-circuit by biasing the SIS junction at the gap voltage, might raise some argument regarding the quantum susceptance, since the quantum susceptance has its peak value at $V_g$ [1], [21]. Specifically, the quanta size, hν, where h is Planck's constant and ν the RF frequency, is negligibly small at frequencies of interest (2-6 GHz). At this frequency range, VNA output power of -60 dBm at a junction biased at $V_g$ results in a quantum susceptance $B_Q$=0.05 $\Omega^{-1}$ , calculated by the models in [22]. Additionally, junction's intrinsic (geometrical) capacitance results in susceptance value $B_C$=0.033 $\Omega^{-1}$ (for the biggest area junction). The total susceptance value (0.083 $\Omega^{-1}$) is insignificant as it is in parallel with the much larger quantum conductance $G_Q$=1.54 $\Omega^{-1}$ value at the gap.

## V. Modeling

As mentioned above, we used Agilent ADS for the modeling where the ADS model has two parts. The model parameters have been adjusted based on the calibration and were used for the SIS junction capacitance extraction. The model for the SIS junction (with values of the biggest area junction) is depicted in Fig. 4. First, as explained in Section IV, a 50 ohm transmission line with unknown delay time is terminated with $R_g$, representing the response of the short-circuit reference cf. Fig. 4a. Subsequently, the delay time is tuned to replicate the gated S11 response of the short-circuit reference. The reflection amplitude for this delay line in the model is 0 dB because of the assumed lossless transmission line. However, in reality, the transmission lines have frequency dependent loss, which in the measurements, as described before, are

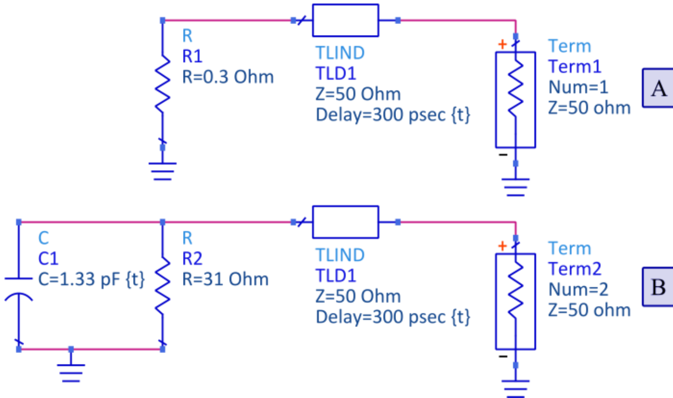


Fig. 4. The SIS junction capacitance extraction model is illustrated in two parts; A) The short-circuit reference is represented by a delay line terminated with the $R_g$. B) The SIS junction measurement is modeled with the delay line extracted from part a and the parallel $R_{sg}$ and C.

overcompensated by the PNA, yielding slightly higher amplitude (~0.5 dB at 6 GHz).

At the second stage of the model adjustment, the extracted delay time of the lossless transmission line is fixed, cf. Fig. 4b. In this stage, the model represents a lossless transmission line terminated with the junction biased at the subgap. Therefore, the lumped circuit that is equivalent to the junction ($R_{sg}$ in parallel with C) terminates the transmission line. $R_{sg}$ value can be readily inserted in the model as it is extracted from the DC IVC measurements. The lumped capacitor value is increased until the S11 response of the circuit B (cf. Fig. 4b) fits closely to the gated S11 response of the biased junction at the subgap bias. The capacitance of the junction is extracted once the best fit is achieved.

The same modelling procedure is done for the thin film capacitor. However, in the second stage of the modeling the resistance is absent. The results of the modeling are presented in the next section.

## VI. Results & Measurement Accuracy

The measurements were performed across the 2-6 GHz band. First, in order to verify the measurement setup and the calibration procedure, the thin-film parallel-plate capacitor with known estimated capacitance value was measured. The corresponding estimation value of the capacitance was calculated to be 1.16 pF using the relation for the parallel-plate capacitor with parameters given in section II. Additional to the parallel-plate capacitance, the fringing field capacitance should also be considered. Calculating this effect using the 2D Palmer formula [23], resulted in an 1.6 % increase from the parallel-plate capacitance value, bringing the estimated value to ~1.18 pF. It should be noted that the used thickness of the $SiO_2$ and the relative dielectric constant may deviate from the actual values which could result in an error in the calculated capacitance compared to the real one.

After conducting the measurements and the modeling, we obtained the capacitance value of 1.21 pF resulting in nearly perfect fit across the frequency band 3.25-4.25 GHz, cf. Fig. 5. The applied gating was chosen to be 1 ns to minimize the errors related to small gate width and power loss. This choice

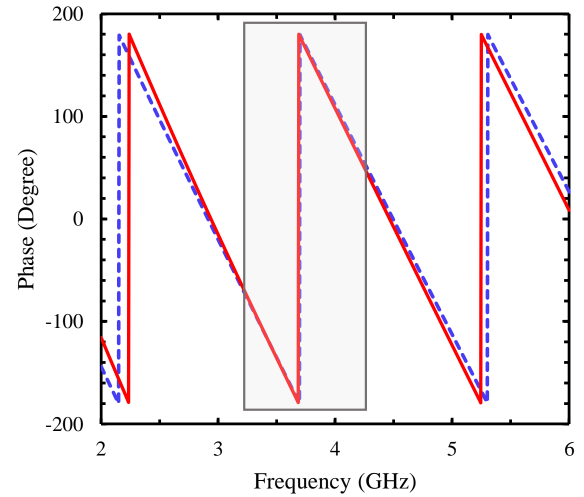


Fig. 5. The phase characteristics of the model (blue dashed line) and the measurement (red solid line) of a thin film capacitor. The grey region indicates the best-fit from 3.25 to 4.25 GHz.

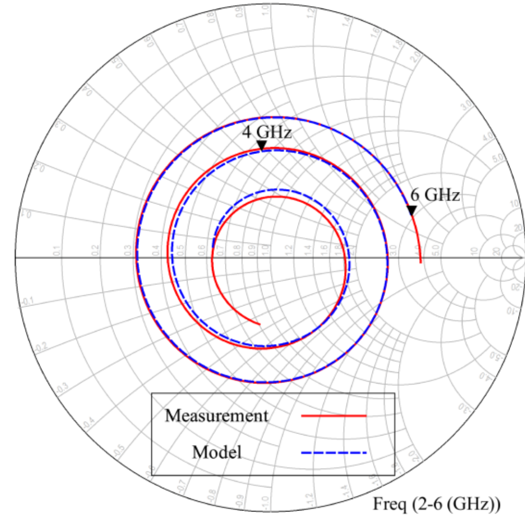


Fig. 6. Smith chart plot of the measured and modeled S11 parameter of the SIS junction with the extracted capacitance of 0.7 pF.

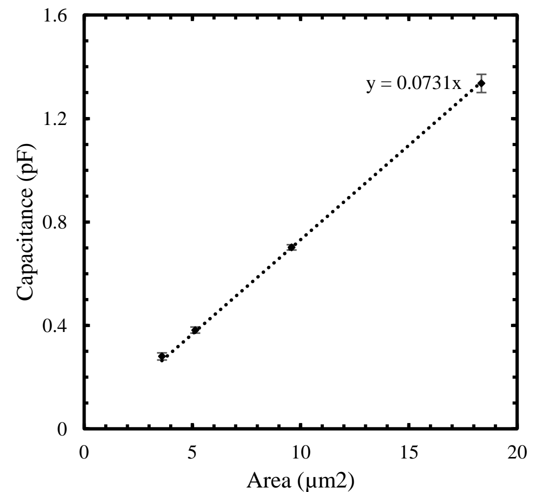


Fig. 7. The resulted capacitance values for SIS junction with four different areas are plotted. A statistical analysis was also done by extracting the capacitances of each junction for multi frequency points over the best-fit band. This analysis led to scattering of the resulted capacitances around the mean value for each junction, shown as error bars (standard deviation). The linear trendline shows the specific capacitance of 73.1 fF/µm$^2$

doesn't allow us to exclude the bias-T response. The non-idealities of the bias tee in the lower frequencies, and the variations in SMA properties at higher end of the band (under cryogenic cooling) could be the reasons for lower quality of the data-model fit at measurement frequency band edges.

This small difference of 2.5 % between the deduced capacitance value and the calculated one proves the method accuracy. This difference could stem from packaging effects, such as different mounting parasitics between the short-circuit fixture and the capacitor's, connector repeatability, and cable bending under mounting DUT.

The measurement and model fit process has been conducted for four SIS junctions with designed areas ranging from 4 to 20 μm$^2$. As an example, a Smith chart plot of both the measurement and modelling results of the fabricated SIS junction with $R_n$ of 3.45 Ω and extracted capacitance of 0.7 pF is presented in Fig. 6.

In the case of SIS junction, combining the measurements of the short-circuit reference and the DUT, undoubtedly reduces the uncertainty of the measurement results through excluding effects such as PNA's gain drift from one cooling to another. However, the measurement uncertainty of the SIS junction capacitance consists of three contributing factors: the performed measurements of the SIS junction biased at the sub-gap and the gap-voltage, and the estimation of the $R_{sg}$ from the DC IVC.

The uncertainty information for the given PNA model, E-Cal module, and the used coaxial cables are provided by Agilent [17]. From this information, two reflection uncertainty curves give the absolute ambiguity in the amplitude and phase measurements depending on the measured reflection coefficient amplitude of DUT. In addition, a variation of the measured magnitude and phase caused by the 4°C temperature change in the laboratory is also considered.

The correct reading of the resistance values at the sub-gap bias point is essential in obtaining the correct capacitance value. As a result, the noise of the read-out circuit adds extra error in the measurement. Depending on the magnets position with respect to the junction, the IV curve exhibits slightly different slopes. Some of the IV curves were noisier and reading the resistance by a linear regression line would add uncertainty depending on analyzed interval of data. Therefore, the standard deviation from the linear regression at the vicinity of 1 mV bias point is included in the estimation of the uncertainty.

As shown in Fig. 6, the capacitance was extracted with the best fit between the model and the measurement in the frequency band 3.5 GHz to 5.5 GHz. The error from the measurements of the DUT and the short-circuit reference and the standard deviation for estimation of $R_{sg}$ of this SIS junction (Fig. 6.), yields in ± 2.98° and ± 0.27 dB uncertainty at 3.5 GHz in S11's phase and amplitude, respectively. Consequently, the uncertainty in S11 (2.98° and 0.27 dB) results in approximately 5 % variation in the capacitance determination. In the same fashion, the absolute error values, 5 - 6.8 %, were calculated for the capacitance of the four junctions at 4 GHz. For the thin film capacitor, the same uncertainty treatment, gives 4.95% error across 3.25-4.25 GHz.

In order to calculate the specific capacitance of the junctions, the measured capacitances were plotted versus corresponding areas estimated by the method discussed in the Section II. The resulting specific capacitance of the fabricated SIS junctions with $R_nA$ of ~33.1 Ω.μm$^2$ was calculated to be 73.1 fF/μm$^2$, by the linear regression line cf. Fig. 7.

## VII. Conclusion

In this paper, we have proposed and experimentally verified a new microwave measurement method for the capacitance of SIS junction. This method can also be used for extracting capacitance of other one-terminal devices such as Schottky diodes at cryogenic temperatures for mixer and multiplier applications. In contrast with previously used methods involving extraction of the SIS junction capacitance from model of a complex superconducting resonant structure, the suggested technique employs direct and accurate VNA measurements. We presented measurement data for one thin-film parallel-plate capacitor and four junctions with various areas. The resulted specific capacitance of the SIS junctions with $R_nA$ of ~33.1 Ω.μm$^2$ was measured to be 73.1 fF/μm$^2$ with 5 - 6.8 % absolute uncertainty at 4 GHz.

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