Organic Thin Film Transistors for Circuitry on Flexible Substrates

by

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Diploma work No 146/2014

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Master of Science Thesis Advanced Engineering Materials

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Cover photo: TFT fabricated on flexible substrate

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Abstract

In recent years organic thin-film transistors (OTFTs) have shown great improvements. Solution processed organic semiconductors (OSC) can be spin-coated or inkjet-printed on TFT (Thin Film Transistor) substrates; the OTFT performance depends on the charge transport properties, the orientation and the morphology of the OSC. The latter can be influenced by several parameters such as surface modifications (e.g. self-assembled monolayers) of the transistor substrates, ink composition and processing strategy. The purpose of this project is to study how the processing of a state-of-the-art polymer p-type semiconductor is related to the device performance and the morphology of the active material. Actually, it can be translated as finding the best way of applying polymer as a semiconductor in order to obtain the best performance of transistor.

The process methods will typically be spin-coating and inkjet-printing. First of all, the focus is on the processability of the OSC inks with spin-coating, and especially the surface treatments of the dielectric interface. The optimization of the process will be correlated to the device performance of bottom-contact bottom-gate, and top-gate TFTs and the OSC film morphology. Next, the study was focused towards the jettability of the OSC polymer for the inkjet-printing technique. The optimization of the inks was to be strongly correlated to device performance of bottom-contact bottom-gate TFTs. In this part of the project, the emphasis lays on the stability of the TFT performance measured as variation in current, mobility, threshold voltage, etc.

Fundamentally, the survey highlights the influence of the morphology on the device performance; therefore the TFT performance can be evaluated statistically on large area devices. Finally, the gained fundamental understanding of the morphology-device performance from the optimized ink and processing conditions will be important for circuitry applications (as uni-polar circuits and/or CMOS (Complementary metal oxide semiconductor)).

Keywords: flexible electronic, organic electronics, thin film transistor (TFT), ink jet printing (IJP), P-type organic semiconductor.

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Thanks God, the merciful and the passionate, for providing me the opportunity to step in the excellent world of science.

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Finally, I appreciate my parents (Mohsen & Afsaneh) for their endless love, supporting and understanding.

List of Abbreviations

ALD	Atomic layer deposition
Al_2O_3	Aluminum oxide
Au	Gold
CF_4	Tetrafluoromethane
CVD	CVD chemical vapor deposition
C8	Octylcylphosphonic acid
C12	Dodecylphosphonic acid
CMOS	Complementary metal oxide semiconductor
DECYL	Dodecyltriethoxysilane
HOMO	HOMO highest occupied molecular orbital
IJP	Ink jet printing
I-V	Current-voltage
LUMO	Lowest unoccupied molecular orbital
OSC	Organic semiconductor
OTFT	Organic thin film transistor
ODTS	Octadecyltrichlorosilane
PA	Phosphonic acid
PET	Poly (ethylene terephthalate)
PFBT	Pentafluorobenzenthio
PVD	Physical vapor deposition
SAM	Self-assembly monolayer
Si	Silicon
SiO_2	Silicon oxide
TFT	Thin film transistor
TCPS	Tricresyl phosphate silane

Table of Contents

1. Introduction and aim

In 1962, the world's first thin film transistor (TFT) was successfully fabricated by P. K. Weimer et al. [1]. Different from the traditional bulk Si-based transistors; TFTs are made from microcrystalline thin material films, which could reduce the vertical dimension of the devices. As a result, this kind of devices, because of its tolerance towards different extents of bending, is compatible with flexible plastic substrates [2, 3]. Hydrogenated amorphous silicon (a-Si:H) is most commonly used as the semiconductor (SC) these days in the inorganic TFTs, especially in active-matrix liquid crystal displays (AMLCDs) [4]. Besides Si-based materials, metal oxide is also attracting a lot of interest as the n-type semiconductor. In 1996, Prins et al. reported that transistors with zinc oxide (ZnO)-based semiconductor materials were achieved with carrier mobility as high as 100 $cm^2\ V^{-1}\ s^{-1}$ [5]. Twenty-four years after the invention of TFTs, the first organic thin film transistor (OTFT) was fabricated by Mitsubishi Electric Corporation in 1986 [6]. An OTFT is a TFT with organic semiconductor, which could be deposited at room temperature without high vacuum equipment, therefore more attractive for the flexible substrates. Moreover, the van der Waals forces between two organic molecules are much weaker than the chemical bond between two inorganic atoms [7]; therefore mechanical failures like cracks or delaminations are less likely to happen when the substrate is bent. During last decades, the OTFT technologies have been carried forward significantly in the domains of materials, fabrication methods and their applications. For example, some organic semiconductors are used in the OTFTs, attempting to achieve high device performance [6, 8]. Although the charge carrier mobility of the organic semiconductors at the beginning was about one thousand times lower than for inorganic materials such as Si and Ge [9], advanced materials was developed to increase the mobility from $10^{-5}\ cm^2\ V^{-1}\ s^{-1}$ [6] to 2.7 $cm^2\ V^{-1}\ s^{-1}$ [8]. Besides, the substrate materials also vary from rigid ones to flexible ones [10]. Another issue to consider is that different methods could be used to pattern and fabricate the OTFTs. Photolithography [11], imprint lithography [12] inkjet-printing (IJP) [13] and laser printing [14] could be employed to pattern the devices. The organic semiconductors can be applied by vacuum deposition [11], solution spin coating [15] and inkjet printing [16]. Taking into account the OTFT processing compatibility with flexible substrates and thanks to these technologies, OTFTs nowadays are attracting more and more attention in applications like large area flexible displays [17], sensor arrays [18], solar cells [19] and radio frequency identification (RFID) tags [20].

This thesis is based on the master degree project "Organic Thin Film Transistors for circuitry on flexible substrate" carried out at the Holst Centre (Eindhoven, the Netherlands) within the collaboration between IMEC (Interuniversity Microelectronics Centre) and Netherlands Organization for Applied Scientific Research (TNO (Toegepast Natuurwetenschappelijk Onderzoek)).

Aim of the project

The aim of this project is to study how the processing of a state-of-the-art polymer p-type semiconductor is related to the device performance and the morphology of the active material. The project employs different methods for understanding the charge transfer characteristics of polymer semiconductors (p-type) as well as presents opportunities for inkjet-printing of organic semiconductors. Here, the effect of the morphology of different appropriate self-assembly-monolayers (SAMs) applied on polymer dielectrics was studied. Finally, the ink morphology and the process that is correlated to the optimized TFT performance are discussed.

In this thesis, theoretical studies and specifications, presented in Chapter 2, constitute a major part and also the starting point. Based on the theoretical design, experiments are carried out to verify and optimize the processes. The experimental set-up is described in Chapter 3 and Chapter 4 describes the results of these experiments. Finally, Chapter 5 gives the conclusions of this project and thesis; suggestions for the future work are given as well.

2. Theory

2.1 Thin film transistor

A transistor is a miniature electronic component that can do two different jobs. It can work either as an amplifier or as a switch [23]. The transistor is based on semiconducting materials, which means that it is neither really a conductor (something like a metal that lets electricity flow) nor an insulator (something like a plastic that stops electricity flowing). Nowadays silicon based transistors are used widely. A transistor can be laid out in different ways. In this project, thin film transistors will be considered.

A thin-film transistor (TFT) is a kind of field-effect transistor made by depositing thin films of semiconducting materials. An organic field-effect transistor (OFET) is a field-effect transistor using an organic semiconductor in its channel [24]. It is based on solution-processable polymers and also small molecular semiconductors. The layout of one TFT is show below, figure 1.

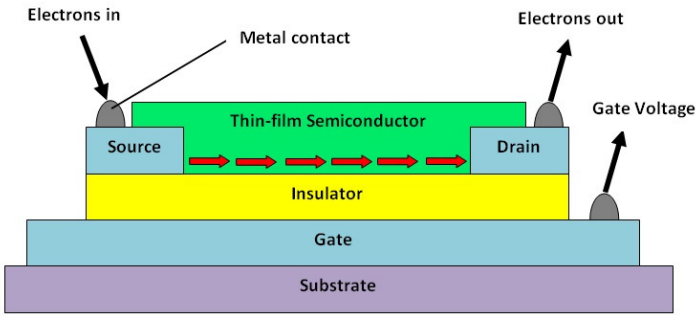


Figure 1.- Cross-sectional layout of a TFT

A common layout of the source and drain contacts is the so-called 'finger' transistor. A graphic of this layout is shown in figure 2.

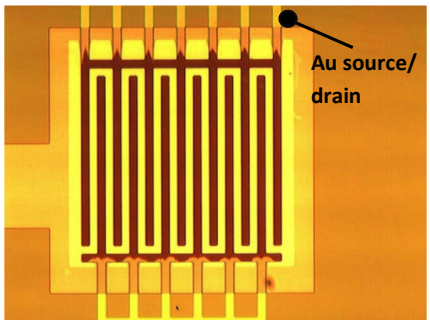


Figure 2.- Pattern of 'finger' transistor as a source or drain

Important parameters of a transistor are its channel length *L* (the distance between source and drain contacts) and channel width *W* (extension of the transistor, the lateral dimension). The width to length ratio (*W/L*) is linearly related to the drain current capability of the transistor. A wider transistor will let more current pass.

A thin film transistor comprises a semiconducting layer, a gate insulating layer and a gate electrode, figure 3. Since the source electrode is earthed, the applied voltage to the gate is the main factor which controls the electron flow between source and drain. When the gate voltage is positive, the electrons are attracted to the bottom surface layer of the semiconductor, and therefore, a conduction channel is formed. A voltage difference between source and drain means an input of electrons to the source and output from the drain which lead to a current through the conduction path [23, 24].

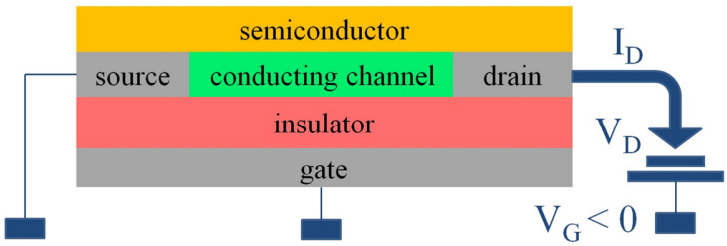


Figure 3.- Schematic of a TFT (p-type) operation

The dielectric (insulator)/organic semiconductor interface is important (see 2.7.1), because at this interface the transport of the current takes place. The electron or hole current is sensitive to morphology effects from the organic semiconductor. The electrical response of the dielectric material (insulator) can influence the current transport, for example due to hysteresis effects. A more detailed operating principle of OFETs and hysteresis effects will be described later in section 2.4.

Thin film layouts: TFTs and OFETs have been fabricated with various device geometries: bottom gate, top gate, dual gate and so on. The most commonly used device geometry is the bottom gate with top contact, since this geometry is similar to that of the thin-film silicon transistor. Since a Si/SiO_2 substrate has the highest quality in this field, it has been largely utilized. Organic polymers, such as poly (methyl methacrylate) (PMMA), can be used as the dielectric. With this layout the electron charge are injected directly from the electrode (source and drain) to the transistor channel (figure 4).

Figure 4.- Schematic of a bottom gate TFT

Use of the organic dielectric for the top-gate structured OFET does not destroy the underlying organic semiconductors. The top-gate bottom contact structure devices allow patterning the bottom source-drain electrodes on top of any flexible or rigid substrate first before building the rest of the device. The top gate top contact structure devices enable growing organic semiconductor films on top of any flexible or rigid substrate (figure 5).

Figure 5.- Schematic of a top gate TFT

A dual-gate TFT, figure 6, is fabricated by a combination of bottom gate and top gate TFTs in one device. This device has the benefit that it is possible to measure bottom gate and top gate characteristics of a semiconductor layer and its two interfaces with the dielectric in one device. The major problem with this device is the possibility of dissolving the semiconductor when applying the dielectric on top of the semiconductor. Therefore, by preparing this device a solvent that does not dissolve the semiconductor should be used.

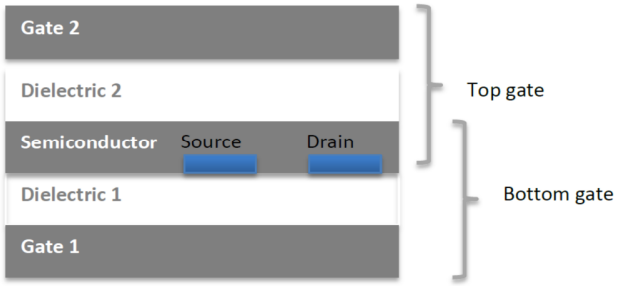


Figure 6.- Schematic of a dual-gate TFT

2.2 Organic semiconductors

The organic semiconducting materials are grouped as polymers, monomers, and small molecules. Their current revival of interest in electronic applications is reflected by a considerable increase in the number of investigations dealing with the measurement of electrical conductivity. They are of great interest in electronic devices and provide multiple advantages because of the variety of structures. Their electrical transport properties are of current interest and they present different aspects of the conduction mechanism, nature of charge carriers and their properties. They contain an extended л- electron system and this system can be changed from a semiconducting state to a conducting state. Conjugated polymers and small molecules are two classes of organic semiconductors used in OTFTs [26].

2.3 Electron transport in organic material

For two reasons organic materials are intrinsically insulating; a) their highest occupied molecular orbitals (HOMO) of all molecules are occupied, b) the energy difference to lowest unoccupied molecular orbital (LUMO) is quite substantial. The electronic structure of conductors simply consists of states that, at 0 K, are filled up to the Fermi energy E_f. At higher temperatures electrons are excited to higher states and they become free conducting electrons. The HOMO–LUMO gap must be reduced, then the conductivity will increase. The reduced band gap allows electrons to more easily jump between the conduction and the valence bands and then gives the semi-conductive properties (figure 7) [25].

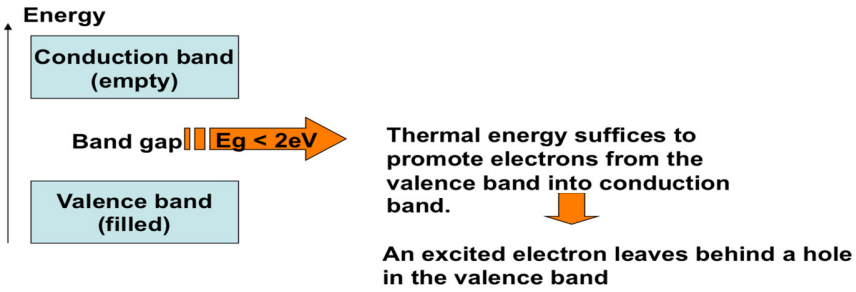


Figure 7.- Schematic of (semi) conduction [23]

In this project, organic compound pentacene is used as p-type semiconductors. By applying p-type semiconductors, the majority carrier will be holes. The Fermi level of the contact metal is close to the HOMO of the semiconductor and far away from the LUMO (figure 8).

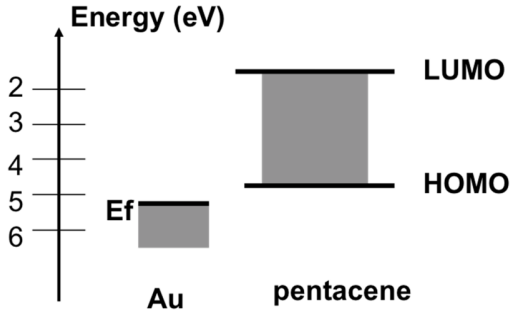


Figure 8.- HOMO and LUMO of p-type (pentacene) with Au contact [23]

An electric field is created in the dielectric by applying a negative gate voltage (V_g). This can lead to attraction of holes at interface of the dielectric/ semiconductor. A current flows toward this accumulation layer by applying a voltage between source and drain contacts. No charges are injected when V_g = 0; When a negative voltage is applied to the gate, negative charges are induced at the dielectric side of the interface and positive charges are induced at the organic semiconductor side of the interface (at the channel).

In n-type OTFT the LUMO level is close to the metal Fermi level. Then a positive gate voltage causes negative mobile charge carriers for conduction and consequently electrons can be injected from the source/drain metal to the LUMO of the semiconductor and an n-type OFET is realized [23].

2.4 Operating principle of OFETs

In field effect transistors (FETs), the current flows via a conducting channel that connects the source to the drain. The voltage applied between the gate and source controls the current between the drain and source. As the gate–source voltage (V_{gs}) increases, the drain–source current (I_{ds}) increases for V_{gs} above a threshold voltage (V_T). The relation between I_{ds}, V_{gs} and V_T is indicated in equation (1) below where V_T is the threshold voltage at which the drain current begins:

$$I_{ds} \propto \left(V_{gs} - V_T\right)^2 \qquad (1)$$

Applying a gate voltage will cause charge carriers to accumulate above the gate dielectric. The density of charge carriers depends on the sign and magnitude of the voltage. The energy diagrams of an ideal p-type metal oxide semiconductor (MOS) can be found on literature [23].

Applying a negative gate voltage (V_{gs}) leads to accumulation of holes at the semiconductor-insulator interface and the device is in an accumulation mode. The current in a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), however, is made up of minority charge carriers.

When a small positive gate voltage (V_{gs}) is applied to a p-type substrate, some electrons are attracted to the semiconductor-insulator interface and the holes are repelled. The device is in a depletion mode, as the majority charges are depleted in the semiconductor-insulator region. The low voltage only results in a low density of electrons at the interface and no conductive channel is formed between the source and drain contacts. The device is off. Applying a higher positive V_{gs} will induce a transition in the device from the depletion mode into the inversion mode. The gate voltage at which the transition between depletion and inversion modes occurs is called the threshold voltage (V_T). The gate voltage controls the charge density in the channel. For a current to flow in the device, however, a drain-source (V_{ds}) voltage must be applied. Applying a positive voltage to the drain will result in a channel current (I_{ds}), as well as a decrease in the charge density in the region around the drain contact. The current-voltage is calculated according to the gradual channel, or Shockley approximation, for a field independent mobility. The Shockley approximation is based on the assumption that the variation in the electric field due to V_{ds} is much smaller than the variation in the field due to V_{gs}. This assumption is justified as the thickness of the gate insulator is in the order of nanometers while the channel length is in the order of micrometers. For lower V_{ds}, the I_{ds} follows an ohmic behavior, which can be described by:

$$I_{ds} = \frac{W}{L}\mu FEC_i\left(V_{gs} - V_T\right)V_{ds} \tag{2}$$

where W is the width of the channel, L is the length of the channel, μFE is the field effect mobility, C_i is the capacitance of the insulating layer and V_T is the threshold voltage. Eventually, at higher V_{ds}, the charge density becomes very low in the region around the drain contact. Increasing the gate voltage still results in increased current, as the gate voltage controls the density in the conductive channel, but the current is no longer dependent on V_{ds} and saturates. This V_{ds} value is known as the pinch-off voltage. The saturation current can be described by:

$$I_{ds} = \frac{W}{2L}\mu FEC_i\left(V_{gs} - V_T\right)^2 \tag{3}$$

For evaluating the TFT performance two charactersitics should be given; the transfer characteristics and the output charachteristics. In the output characteristics, the drain current I_{ds} is plotted as a function of the drain voltage V_{ds}. This is done for a number of gate voltages V_{gs}. A typical example of an output characteristic can be found in figure 9. From this output characteristics it can be easily seen that the TFT operates in a linear current regime at low drain voltages (if $V_{ds} << V_{gs}$) and for high drain voltages ($V_{ds} \geq V_{gs}$) in a current saturation regime with a gradual transition in between.

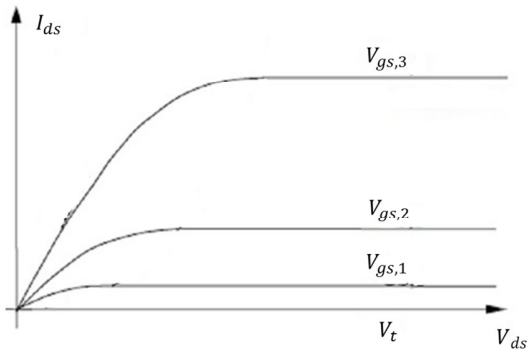


Figure 9.-Example of output characteristics of an ideal TFT. V_{gs}: gate–source voltage , I_{ds}: drain–source current , V_{ds} : drain–source voltage, V_t: threshold voltage. $V_{gs,1} < V_{gs,2} < V_{gs,3}$ [23].

The transfer characteristics are obtained when the drain current I_{ds} is measured as function of the gate voltage V_{gs}. Different regimes could then be detected. In the linear regime ($V_{ds} << V_{gs}$) and in the saturation regime ($V_{ds} > V_{gs}$). A transfer charactersitic of a p-type TFT without much hysteresis can be seen in figure 10. V_{gs} is swept forward and backwards in order to find out if hysteresis is present. If hysteresis is present, this indicates that the transisator's behaviour is not ideal.

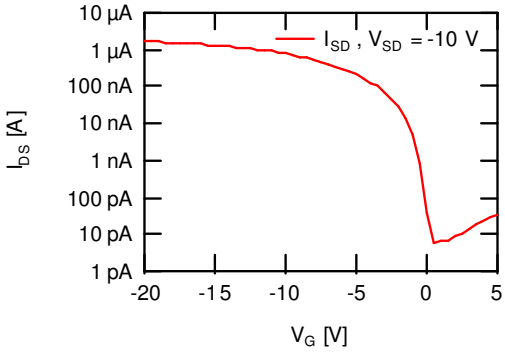


Figure 10.-Example of transfer characteristics of a p-type TFT, V_{ds}: source-drain voltage , I_{sd}: source-drain current , I_{ds} : drain–source current, V_{gs}: gate voltage.

Hysteresis

Hysteresis, caused by a shift of V_{on} (V_{on} is defined as the gate-source voltage at which I_{ds} increases abruptly), might be observed in both the transfer curves and the output curves of an organic field-effect transistor. I_{ds} increases or decreases during a back and forth sweep, depending on the direction of the shift of V_{on} . It leads to an error in the extracted parameters and

is a sign of instability of the transistor. Most often the hysteresis is described in the transfer characteristics, where values for V_{on} can be directly determined. Here in this project the hystersis is due to two reasons:

1. The trapping of holes and electrons from the semiconductor side of the gate dielectric results in a decreasing current during the sweep which results in V_{on} shifts towards the applied V_{gs} in IV (current-voltage) diagrams.

2. The trapping of holes and electrons from the gate side of the gate dielectric results in an increasing current during the sweep which results to V_{on} shifts away from the applied V_{gs} in IV (current-voltage) diagrams.

2.5 Processability

Thin films are thin layers ranging from fractions of a nanometer to several micrometers in thickness. A uniform thin film can be applied by different techniques like gas-phase based techniques (for example, Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD)). Other techniques are solvent-based techniques (for example, spin-coating and inkjet-printing). In this project, spin-coating (for semiconductor depositon and/or monolayer depositon on dielectric layer) and inkjet-printing (for semiconductor depositon on dielectric layer) were mainly used.

2.5.1 Spin-coating

For spin-coating the substrate is placed in the middle of a chuck and is covered with a solution (contains a polymer and a solvent). Upon revolving the chuck, the centrifugal forces spread out the solution and a uniform film is formed. Since the solvent is volatile, a thin layer of polymer will be left on the substrate. The spin-coating process steps are (figure 11):

- Deposition of the coating fluid onto the substrate.
- The substrate is accelerated to its target rotation speed.
- The substrate is spinning at constant rate. (In this step, the viscous forces and the solvent evaporation of the fluid dominate the thinning behaviour.)

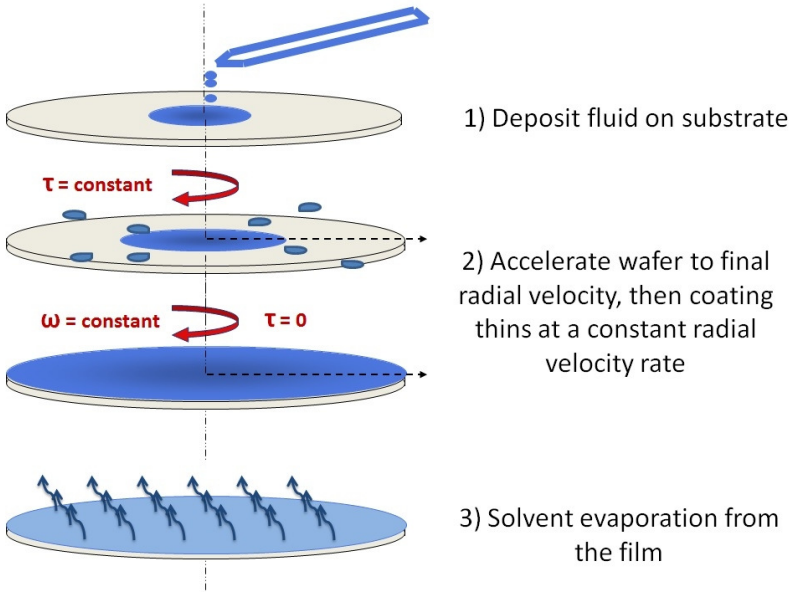


Figure 11.-The steps in the spin-coating process

Several factors influence the spin-coating process. The major parameters of the spin-coating process are:

- Fluid; Solvent, density, polymer, surface tension and viscosity.
- Spin process; Rotation speed and acceleration.
- Air surrouding; Temperature and humudity.
- Substrate; Roughness, temperature and surface energy.

Fluid

The two main components of the fluid are the solvent and the polymer. The solvent evaporates during the process, this will result in a thin layer of polymer. The viscosity of the solution affects the film thickness This is described in the paragraph on the spin process. The fluid will dry (evaporation of the solvent) from the moment of application on the substrate. The volatility of the solvents in the fluid and the air that surrounds the substrate both affect the drying rate of the fluid.

Spin process

The spin speed is one of the most important parameters in the spin-coating process. The speed of the substrate (in rpm) determines the centrifugal force that spreads the fluid.

The film thickness is the result of a balance between the spin speed and the viscosity of the solution. As the solvent of the fluid evaporates, the viscosity increases (which reduces the flow) until the spreading of the fluid ceases. The final film thickness is normally defined by the spin speed.

Air surrounding

The fluid will start to dry (evaporation of the solvent) at the moment of application on the substrate. The volatility of the solvents and the air that surrounds the substrate affect the drying rate of the fluid. A higher temperature and a lower humidity will cause faster evaporation of the solvent. A change of only a few percent in relative humidity can result in large variations of the film thickness. The turbulence of the air directly above the substrate is affected by the spin speed. It is important that the air flow is minimized or at least kept constant. A turbulent air flow can result in an increased evaporation rate which causes a incorrect flow from inner to outer side of the substrate.

2.5.2 Inkjet-printing

Inkjet-printing (IJP) is one of the most promising methods for controlled deposition of small amounts of materials such as metal inks, photoresists, organic semiconductors (OSC) and other functional materials. By means of inkjet-printing, a very small droplet of a solution is pressed out of the nozzle of a print head onto a substrate. The formation and size of the droplets are controlled by a piezoelectric element. The substrate can be heated to optimize the drying of the droplet.

Basic physics of inkjet printing

There are two important types of print heads: piezoceramic and thermal. In a piezoelectric inkjet printer, there is a a piezo crystal behind the ink reservoir (of the nozzle). A small current to crystal induces vibrations, and hence a small amount of ink is dispensed out from the nozzle. Once the vibration stops, ink will flow into the empty nozzle. In contrast, in a thermal inkjet printer, a resistive heater pad is heated and produces vapour bubbles which eject the ink droplets. The thermal method is not widely used in inkjet-printing of organic semiconductor materials because the high temperature can degradade the materials.

The nozzle can deposit single droplets of different volumes depending on nozzle size and voltage applied. The ultimate size of droplets is limited by evaporation of the droplet during flight and other factors. The droplet generation in a piezoceramic print head occurs in several steps. The piezoceramic is at its idle voltage. This is increased rapidly to the jetting voltage to deflect the piezoceramic membrane outwards and cause the chamber to shrink and expel a volume of liquid through the nozzle over a period of a few microseconds.

The rate of deflection of the membrane is governed by the the change in voltage over time. The liquid volume then necks to give one or more liquid droplets over the next tens of microseconds. Here there is possibility for formation of satellite droplets which is not undesirable. In some cases, the satellite droplet catches up with the primary droplet during flight giving a single droplet on the substrate; in other cases, the satellite droplets can land separately.

The size of the ejected droplet depends on the size of the nozzle and the physico-chemical properties of the liquid, such as surface tension, viscosity and density. The ejection velocity of this droplet is determined by the jetting voltage and the liquid physico-chemical properties. The landed formation of the droplet depends in addition to the ejection volume also on its contact angle and the impact velocity on the substrate.

After the necking of the ejected liquid volume, the voltage on the piezoceramic can be decreased over a period of tens of microseconds, or in steps to recover the original position of the piezoceramic membrane. This causes the chamber to expand and back-fill with the liquid from the reservoir. By a proper optimisation of the drive voltage waveform at each nozzle, it is possible for piezoelectric printers to achieve good control over precise volume and velocity of every droplet deposited. A schematic of single nozzle jetting and the steps of drop formation is show below in figure 12.

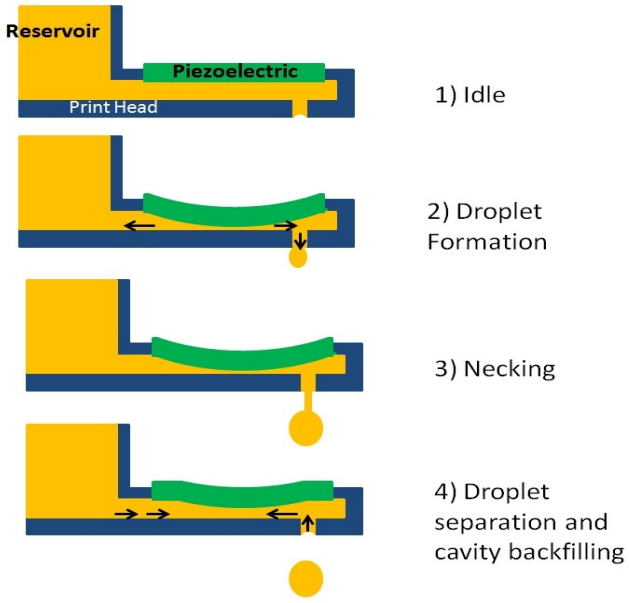


Figure 12.-The steps of the inkjet-printing process

2.6 Thickness measurements

The measurement method used to measure the thickness was contact profilometry. A Dektak measurement device or Dektak profilometery is one the recently invented equipments which are

employed to measure height and depth steps of surfaces. The general purpose of Dektak is to quantify the surface roughness at the sub-micron scale. The device has a stylus with a spherical tip which contacts the surface, and then gently moves along the surface of the substrate in order to get the surface profile; 12.5 μm is the minimum value of the radius of the stylus and 2 mm is the maximum value of the vertical range of the stylus, so traces narrower and deeper than these values are not recordable.

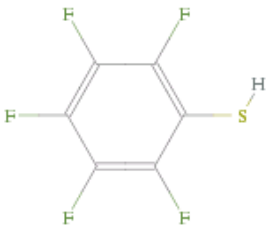
2.7 Surface treatments

For modifiying the surface properties of the dielectric and the gold contacts, self-assembling monolayers (SAMs) are applied. These SAMs change the enthalpy of the surfaces and then their wettability change. They may also influence the interaction of the surface with the deposited semiconductor and thus affect the transistor performance.

Electrode surface modification with SAMs

Efficient charge injection is important for transistors to work properly**.** This requires the work function of the electrode to match well with the energy level of the organic semiconductor giving a low energy barrier for charge injection. For organic transistors, typically high work function electrodes (Au, Pd, or indium tin oxide) have been used for p-channel organic semiconductors, in which holes are injected and transported through the organic material. It has been found that an electrode surface modification with a self-assembled monolayer can be used to improve the charge injection into the organic semiconductor. For example, when Au electrodes are used, they can be functionalized with various thiol SAMs to modifiy their work functions. Moreover, the morphology of organic semiconductors is significantly different when deposited on SAM modified Au compared to bare Au. This observation has been used to tune the morphology of the organic semiconductor at the Au/organic interface to improve the charge injection [28].

Pentafluorobenzenthiol (PFBT) on a gold surface is an example of this treatment. The gold contacts are treated by thiol SAMs. PFBT can be applied by immersion, spinning or vapour treatment. The reaction is schematically shown below (figure 13).



Formula	C_6F_5SH
Name	pentafluorobenzenethiol
IUPAC name	2,3,4,5,6-pentafluorobenzenethiol

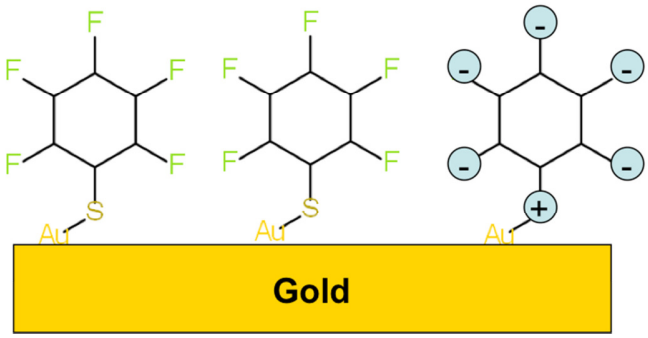


Figure 13.-Modification of a gold electrode with PFBT

Dielectric surface modification

Since most of the charge carriers induced in the semiconductor layers are confined to the first 5 nm of organic semiconductor from the semiconductor/dielectric interface, the surface chemical and physical characteristics of the dielectric play a significant role for the charge carrier transport. For example, Si-OH groups on SiO_2 surfaces (a typical dielectric material) are known to trap electrons. Capping SiO_2 surfaces with octadecyltrichlorosilane (ODTS) "CH3(CH2)17SiCl3" molecules can significantly reduce the electron trapping and improve the mobility in semiconductors (electrons are the major charge carriers). Additionally, surface treatment of the dielectric with SAMs also affects the nucleation and growth of organic semiconductors [27].

2.7.1 (De)Wetting

Wettability is of great importance in solution processing of organic semiconductors. When the surface of substrate is not covered with solution, the semiconductor will not be present there; this is what is called a dewetting surface. In order to characterize the wettability of the substrate, contact angle measurements were used.

2.7.2 Contact angle measurements

Each liquid drop makes an angle when it contacts with a solid surface. Drop shape analysis at the liquid-solid interface (figure 14) is a common way to measure contact angles and then perform a subsequent calculation of the surface energy of the substrate.

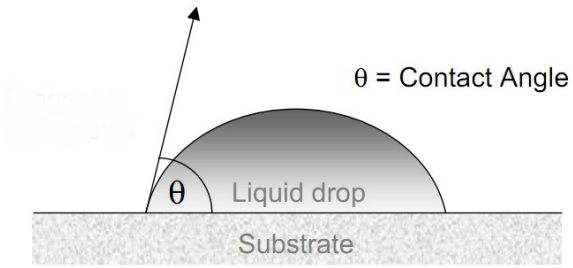


Figure 14.-Schematic droplet and contact angle with the substrate

The principle of the device that calculates the contact angle is based on recognition and estimation of the droplet shape. A certain volume of the liquid is ejected from a syringe onto the surface of the substrate, see figures 15-17. When the droplet has come to rest on the surface, its shape and contact angle towards the substrate can be evaluated by a dedicated software.

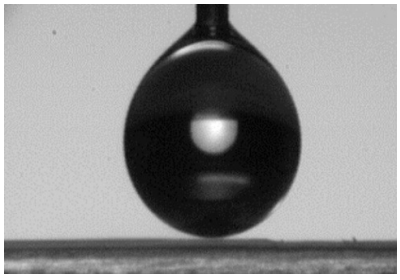


Figure 15. Drop loaded above surface

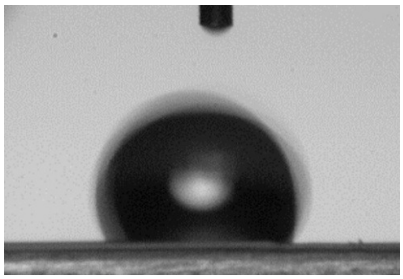


Figure 16. Drop just caught by surface

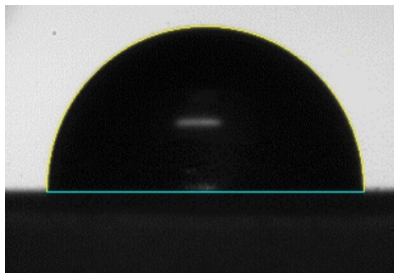


Figure 17. Estimation of angle via software

3. Experimental setup

All process steps are performed in a clean room atmosphere. The entire process is designed for a bottom-gate transistor layout.

3.1 Preparation of the semiconductor solution

- Dissolve the organic polymer in toluene (water free, 99,9%) to obtain a 0.75 wt% solution
- To facilitate the process, the material should be dissolved at 80°C for 30 min, then the solution is cooled down to room temperature before further processing.
- Filter the cold solution using a syringe equipped with a 0.45 μm PTFE filter. The filtered solution should be standing for 15 min to ensure that no air bubbles remain.

Fresh solutions were prepared for the experiments and were stored in the dark.

3.2 Preparation of TFTs on flexible substrates

Two cleaning methods for the preparation of TFTs on flexible substrate were tested:
1: Cloth wiping

- Rinse the substrate with acetone and ethanol
- Dry the substrate using a clean cloth

2: Solution rinsing

- Rinse the substrate repetitively for 5 seconds with acetone and ethanol.
- Dry the substrate immediately with a stream of clean nitrogen; afterwards expose it to 60°C for 30 s on a hot plate.
- UV/O_3 (ultraviolet-ozone) treatment of the surface for 10 minutes (for some processes). This method provides a special way to clean the surface without any damaging risk of the circuit board or the surface of products.

Now, two substrates obtained with different cleaning methods were ready for measuring the TFT performance in a N_2 environment. On the substrate that was cleaned with cloth, no TFT measurements were however performed. This method easily destroyed the Au-contacts and the micrograph, figure 18, showed that this method damaged the surface of the substrate as well.

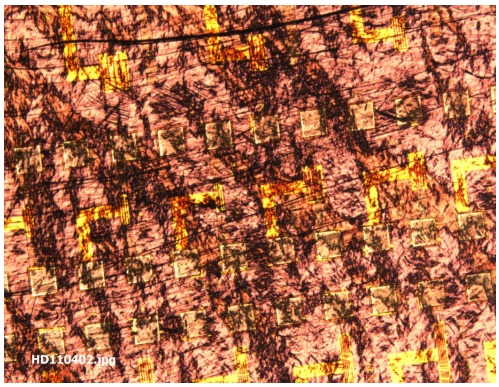


Figure 18.-Wipe cleaning of substrate damaged the surface of the surface

Solution cleaning on the other hand appeared not to damage the surface of the substrate as indicated by figure 19.

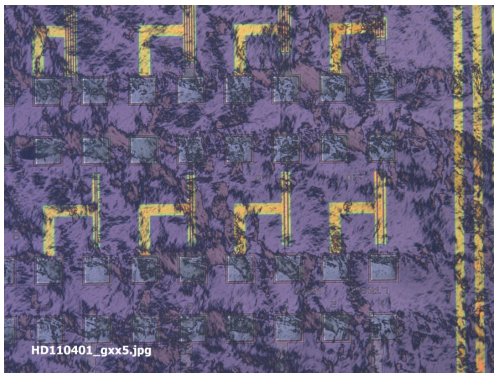


Figure 19.-Micrograph of solution-cleaned substrate

For the further experiments solution cleaning was used for preparing the substrates. Cleaned substrates were kept no longer than 4h before further processing; otherwise they needed to be cleaned again.

3.3 Spin-coating of the semiconductor

Below the way for applying a semiconductor on the substrate is outlined:

- A glass pipette was used to apply the semiconductor solution onto the substrate. The whole substrate area should be covered taking care that air bubbles were not created.
- Starting the spin-coater and adjusting spin-coating parameters to achieve a smooth film with a thickness of 45 nm (1300 rpm for 15 s at acceleration of 10000 rpm/s).
- The substrate was immediately transferred onto a hot plate at 90°C for 30 sec.
- Cooling of the substrate to room temperature.

3.4 Ink jet printing of the semiconductor

Jettability of the OSC inks by using a single nozzle ink jet printer was studied. The processability of the ink has to be controlled in order to print a defined amount of OSC on small and constrained areas. For drying of the droplets and better formation, the substrates were placed on a hot plate at 70°C.

In this study, the following parameters were used for ejecting the drops:

- Droplet velocity (droplet speed) fixed at ≈1.9 m/s
- Droplet volume fixed at ≈ 42 – 54 pL
- Latency distance fixed at ≈ 944-978 µm
  Here we had the continuous formation of droplet on a moving plate where the substrate was located. So, the latency distance indicated the particular distance that the droplet travelled.
- Frequency: ≈ 100 Hz
- Back pressure: ≈ 4 mbar
- Precaution should be taken so that the ejected drops were directed to the exact desired location on the TFTs transistors.

The above parameters are crucial in order to fill the TFTs fingers in a controlled manner and in this case almost constant values were used. These parameters correspond to a fixed unipolar (pressure) pulse for ejecting the droplets schematically shown in figure 20. Such a pulse is characterized by a maximum amplitude *A* and a dwell time *(t_d)*.

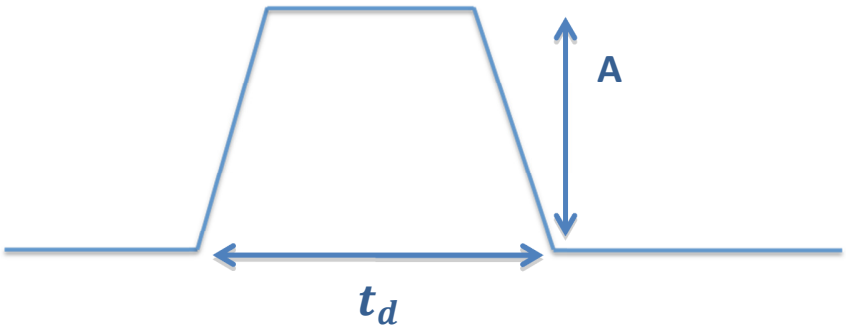


Figure 20.-Unipolar pulse shape used for the ink jet printing study

4. Results and discussion

In this chapter the effects of several parameters, such as surface modifications (e.g. self-assembled monolayers) of the transistor substrates and the processing strategy, on the OTFT performance were studied.

The purpose of this project was to study how the processing of a polymer p-type semiconductor (e.g. pentacene) can be related to the device performance and the morphology of the active material. Actually, it can be translated as finding the best way of applying polymer as a semiconductor in order to obtain the best performance of transistor. First, the effect of OSC annealing on the TFT performance was investigated. Then, the way of applying different SAMs were discussed and the influence of different SAM treatments (silane treatments and phosphonic acid treatments) on different dielectrics were explored and the optimized SAMs which gave best TFT performance were selected. The main dielectric substrates for OSC in this project were SiO_2 dielectrics, but also Al_2O_3 dielectrics and PVP dielectrics were studied for comparison. Moreover, some attempts (treating the gold electrodes with PFBT) in order to improve the charge injection from source to the drain were done.

The process methods used were spin-coating and inkjet-printing. First, the focus was on the processability of the OSC inks with spin-coating, and especially on the effects of the surface treatments of the dielectric interface (surface). The optimization of the process was correlated to the device performance of bottom-contact bottom-gate and the OSC film morphology. Next, the study was focused towards the jettability (inkjet printing ability) of the OSC polymer for the inkjet-printing technique. Then, the optimization of the processing and OSC morphology was correlated to the device performance of bottom-contact bottom-gate TFTs. In this project, the emphasis laid on the stability of the TFT performance measured as the variations in current, mobility, threshold voltage, etc.

The input and output characteristics are explained earlier in the introduction section 2.4.

4.1 The effect of OSC annealing on the TFT performance

The annealing experiments were performed with a hot plate in nitrogen environment for 20 min at respective temperatures of 100°C, 135°C and 150°C. The morphology (the shape, size, texture and phase distribution of OSC) of the polymer semiconductor showed no changes after annealing (Figure 21). In general the TFT performance (mobility, hysteresis) remained relatively constant for the annealed devices. The only significant change induced by the annealing was a threshold

voltage shift. The V_t increased with increasing annealing temperatures. It was found that the annealing steps did not significantly affect the performance of the polymer semiconductor.

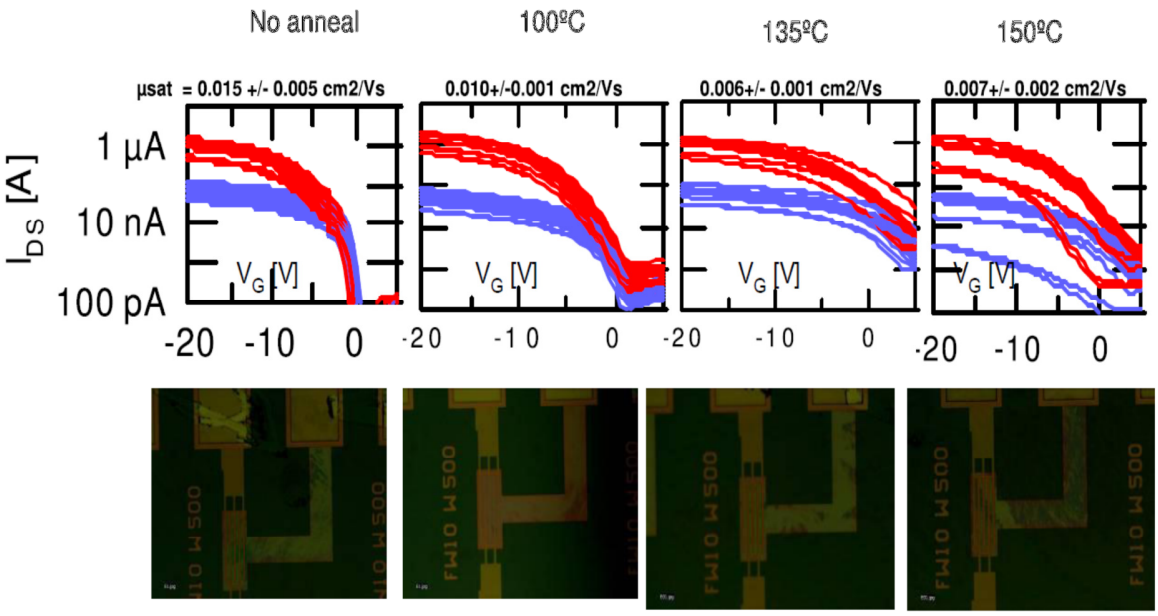


Figure 21. -The influence of OSC annealing on the TFT performance (input characteristics). The substrate was a dielectric (SiO_2) without any treatments of gold electrodes or any SAM-treatment of the dielectric. First row shows transfer characteristics of TFTs. The blue curves represent the forward current and the voltages are extremely small when TFT starts to work and the current increases rapidly for a very small increase in voltage producing a non-linear curve. The reverse response which is greater than forward current is shown in red. The pictures in second row show their related microscopy pictures (OSC morphology).

4.2 Surface treatments

For modifiying the properties of the dielectric/polymer semiconductor interface, the SAMs were applied. These SAMs influence the interaction between the dielectric surface and the deposited semiconductor, make a change in molecular order and cap (covering the electron) the trapped electrons to improve transistor performance. Also, in order to investigate the effects of the charge injection from the Au electrodes to OSC, the Au contacts were modified with PFBT SAMs as it was explained in section 2.7.

To find the best procedure for applying the SAMs on the polymer dielectrics, and improving the charge transfer of polymer semiconductor, different types of SAMs were examined. The experiments were carried out on different dielectrics; polymer dielectrics (SiO_2) , Al_2O_3

dielectrics and PVP dielectrics. The table below shows a list of all surface treatment agents on the different dielectric substrates that have been used during this project and in which sections of the thesis they are discussed.

Dielectric substrates	**SAMs treatment**	**discussed in section**
Polymer dielectric ($\boldsymbol{SiO_2}$)	Silane (ODTS, DECYL and PETs)	4.3.1
Polymer dielectric ($\boldsymbol{SiO_2}$)	Phosphonic acid (C_8 , C_{18} , C_{12})	4.3.2
ALD Al_2O_3 dielectric	Silane (ODTS, OTS)	4.4.1
ALD Al_2O_3 dielectric	Phosphonic acid (C_8 , C_{18})	4.4.2
PVP dielectric	Silane (ODTS,OTS,TCPS,CF_4)	4.6

4.2.1 Silanes and surface modification

The surface modification of dielectrics is described in section 2.7. One way to change the density of electrons at the interface with the gate dielectric is by surface treating the dielectric. No free electrons can be accumulated on a bare SiO_2 surface, due to the immediate trapping of electrons at the interface, from the moment they leave the source electrodes. The trapping site is suggested to be the OH-groups present on the SiO_2 surface. Treating the SiO_2 with a silane like OTS, partly removes these electron traps, resulting in an improved electron accumulation. Covering the SiO_2 with a polymer without OH-groups results in even higher electron currents in the device.

Silanes are silicon-based chemicals that can react with (in)organic dielectrics forming stable covalent bonds (Figure 22). In figure 23, the silane linker which was used in this project is shown.

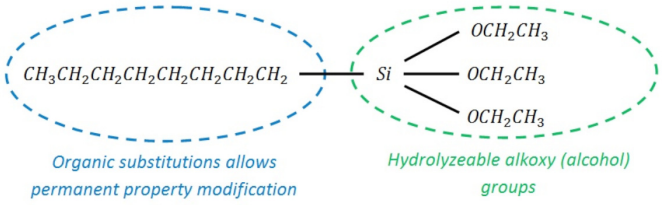


Figure 22. Silanes and surface modification [26]

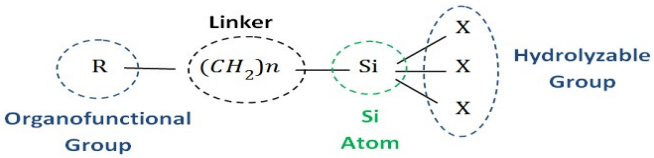


Figure 23- Silane linker length [26]

In order to hydrolyze the alkoxy groups of the trialkoxysilanes giving silanol-containing substrates, a surface treatment is used. The reaction starts by hydrolysis of the three labile groups. Then it continues with bonding of H to OH-groups of the substrate. Eventually, curing leads to formation of covalent bonds to the substrate in conjunction with water loss. Typically the remaining silanol groups are in two forms, in condensed state or free state. Covalent or physical interactions with other phases are possible due to the presence of the remaining R-group (Figure 24). The coverage of the silane SAM of the dielectric can be estimated by contact angle measurements (with water), see section 2.7.

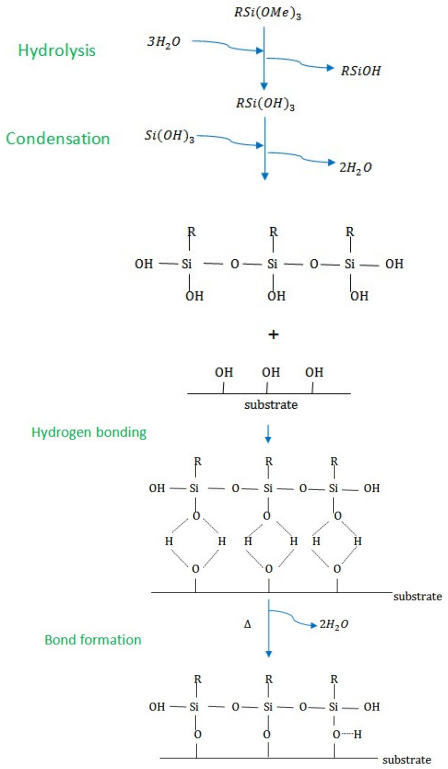


Figure 24.-Hydrolytic deposition of silanes onto a substrate with OH-groups [26].

4.2.2 Applying silane on dielectric substrates

Self-assembled monolayers are commonly deposited through either liquid or vapor based methods. In this project vapor phase deposition and spin-coated deposition of silane-based SAMs

were applied. At following the effect of illumination on devices with a different treatment of interface were discussed.

Vapor Phase Deposition: Silanes can be applied to substrates under dry aprotic conditions using chemical vapor deposition (monolayer deposition). The commercial optimum condition for the deposition is vapor pressures > 5 torr at 100°C. In closed chamber, 5 mm vapor pressure is achieved by heating up the silane reservoir to a certain temperature and applying vacuum until silane evaporation starts. In another approach, the silane can be prepared as a toluene solution. When the toluene comes to reflux, this enables adequate amounts of silane entering the vapor phase. In order facilitate a reaction of the above types, the substrate temperature should be kept between 50°C and 120°C. The quickest deposition is obtained by using cyclic assailants which takes less than 5 minutes. The deposition of the amine-functional silanes takes about 30 minutes, whereas deposition of other silanes will take longer times, 4-24 hours.

Vapor phase deposition of silanes is an effective for the covalent attachment of these reagents to surfaces. In general, this method can be made more reproducible and robust than silane deposition from solution because it is often difficult to control the degree of hydrolysis and oligomer formation of silanes in solution. In general, gas phase deposition of silanes is also much cleaner than the liquid phase approach because the surface is not exposed to impurities that may be in the solvent, and no surface rinsing or cleaning is required after adsorption.

Silane solution deposition: The ease of preparation and the low costs of silane solution deposition are important reasons for the popularity of SAMs. Provided that the substrate has been properly cleaned, in principle, it simply has to be dipped into the corresponding solution for a certain period of time, and the monolayer will assemble. Of course, it is very important to carefully control the cleanliness of the solution, which can be difficult. In the case of silane-based systems, the water content turned out to be crucial for the proper preparation of the SAM. Proper outgassing of the solution is another important issue. Moreover, after completion of the SAM an appropriate rinsing procedure has to be followed.

4.2.2.1 Silane vapor phase deposition

Silanes can be applied to substrates under dry aprotic conditions using chemical vapor deposition as mentioned and described above. In this project, the salinization temperature was 60°C.

4.2.2.2 Silane solution deposition (spin-coating)

Silane, aiming for a final concentration of 2%, was added to a 95% ethanol and 5 % water mixture, pH-adjusted with acetic acid (pH 4.5-5.5). The silane formation takes about 5 minutes. Spin-coating can be performed in either hydrolytic or dry conditions. The hydrolytic condition will promote a multilayer deposition, whereas the dry condition favors a monolayer deposition. The spin speed is typically 500 rpm and rinsing of the solvent should be performed 15 minutes

after the coating.. Monolayer deposition can be obtained under nitrogen atmosphere using low spin speed and the substrate should be heated up to 50°.

The silane SAMs solutions were applied in a nitrogen environment. The preheating temperature was 110°C (80°C for PFBT treated substrates) for 15 min; the spin speed was low, 500 rpm for 15 sec. Following the spin-deposition, a holding period of 1 minute was required before applying the rinsing solvent. Next, the solvent (toluene) was spin-coated with same speed drying of the specimens after the spin-coating took place at the same temperature as the preheating (110°C or 80°C) for 10min. Note that preheat and the post heat treatments can improve the molecular orientation of SAM surface on dielectric and results to have a strict monolayer deposition which was desirable. As shown in figure 24, during drying or curing, a covalent bonding is formed with the substrate accompanied by a loss of water.

4.2.3 Phosphonic acid and surface modification

The polymer dielectric surfaces were modified with organic phosphonic acid (PA)-based molecules. These PA molecules are moisture stable and do not exhibit homocondensation. PA-SAMs molecules efficiently covalently bind to aluminum oxides following an acid-base condensation and a coordination mechanism where acidic PA head groups (pKa ≈ 2) readily react with the more basic metal hydroxyl (M–OH) groups (pKa ≈ 6–9 for many metal oxides) resulting in stable P–O–M phosphonates (≈30–70 kcal mol^{-1} adsorption energy). The coverage of phosphonic acid SAM of the dielectric can be determined by water contact angle measurements, see section 2.7.

4.2.4 Applying phoshonic acid

PA-SAMs were deposited by immersion in an acid solution for different times (15min, 4h). After the deposition, the substrate was rinsed for 5 sec with isopropanol and then blow-drying with N_2. The substrate was thereafter dried on a hotplate in air at 90°C for 30 sec. In this work the effects of three different lengths of the alkyl chains using phosphonic acids as the reactive group; octylcylphosphonic acid (C8), dodecylphosphonic acid (C12) and octadecylphosphonic acid (C18), were here studied (see section 4.3.2). The optimal concentration of phosphonic acid was 0.050 mM phosphonic acid in tetrahydrofuran (THF).

4.3 Applying SAMs on the polymer dielectrics

4.3.1 Silane SAMs treatments of polymer dielectrics

The effect of SAMs modification of the polymer dielectrics was studied using different lengths of the active chain applied with the vapor deposition: dodecyltriethoxysilane (C12-silane), octadecyltrichlorosilane (C18-silane), and poly(ethylene terephthalate) silane (PETS). For

estimating the silane coverage, the water contact angle was measured and the results are shown in figure 25. The vertical axis shows the values of measured contact angle. The horizontal axis on the graph indicates the different SAM treatments of the polymer dielectrics. The notion UVO_3 indicates that the sample was cleaned by UVO_3 without any further treatments, if sample was cleaned by both UVO_3 and H_2O it was denoted ($UVO_3 + H_2O$). The effects of ODTS (octadecyltrichlorosilane) treatment, ODTS + H_2O treatment, DECYL (dodecyltriethoxysilane) treatment, DECYL + H_2O treatment, PETS (poly (ethylene terephthalate)) treatment and PETS + H_2O treatment of polymer dielectric on the contact angle are included in the graph.

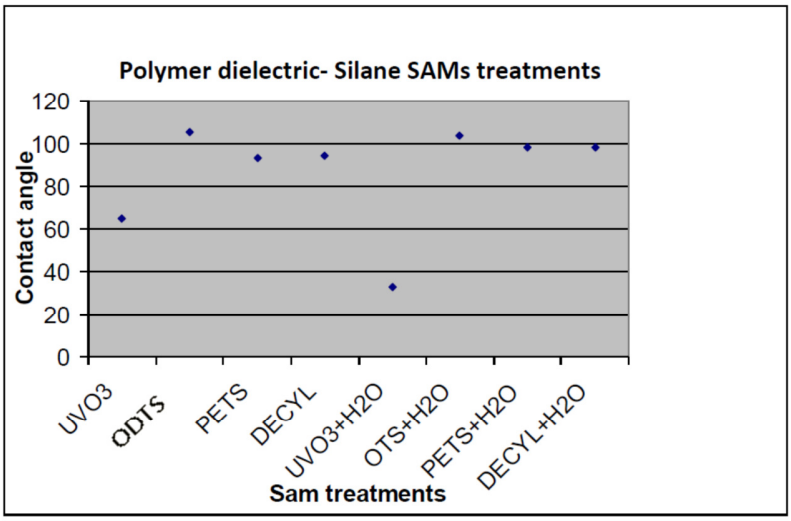


Figure 25- Contact angle measurements vs. different silane SAMs treatments of the polymer dielectric

As an outcome, the contact angles due to the different silane SAMs treatments were in the same range (99^o for C12 (DECYL) to 103^o for C18 (ODTS)), so we expect the same TFT performance of them. These values are quite high for contact angles, which indicate that the coverage of the silanes of the dielectric was good. These results could be compared with that for the "UVO_3" sample. The contact angle (CA) for the UVO_3-treated sample was 60^o whereas it was 35^o after water rinsing of the substrate following the UVO_3 treatment. Water rinsing of the SAMs (ODTS, DECYL and PETS)-treated substrates had no influence on the contact angle. Note that here the purpose was to understand if water rinsing (cleaning) can improve the SAM coverage. Thus, water rinsing is not needed before the silane SAMs deposition. The transfer and output characteristics of TFT performance of the SAMs-treated specimens are shown in figure 26.

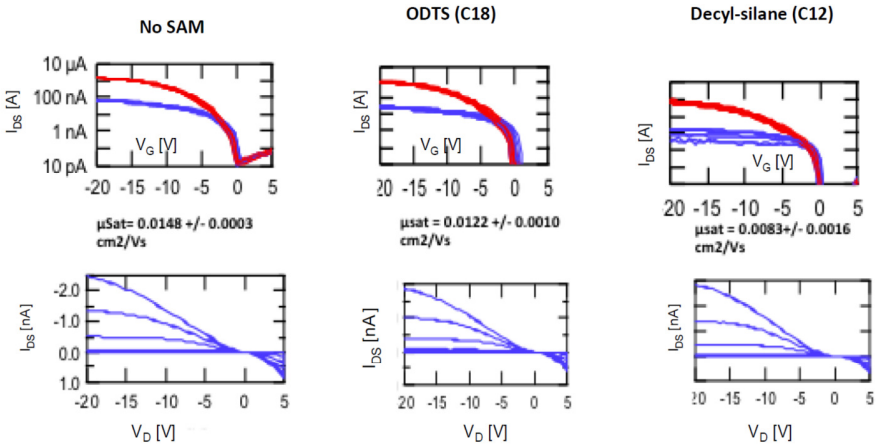


Figure 26 - First and second rows IV (current-voltage) curves show input and output TFTs characteristics, respectively. 'No SAM' sample is a reference sample. The silane SAM was vapor deposited (at 60°C) and ODTS and DECYL were spin-coated on the polymer dielectrics.

As expected from the contact angle measurements (figure 25), the C12 (ODTS) and the C18 (DECYL) silane SAMs treatments gave same TFT performance (figure 26). The silane treatment had no significant effect on the TFT performance. It can be compared with reference sample which is here denoted "no SAM". Good reproducibility and no hysteresis were observed. The threshold voltage V_t was close to zero and no leakage current was detected. The saturation mobility for the untreated sample was 0.014 cm^2/Vs, which slightly decreased after the silane treatment (0.012 cm^2/Vs for C18 - 0.008 cm^2/Vs for C12).

The effects of a PFBT treatment of the gold contacts for reducing the contact resistance and improving the charge injection from Au to the polymer semiconductor were studied (figure 27). The output curves of the PFBT-treated samples showed improvements with regard to the current saturation (compare output curves of figure 26 with figure 27). The I_{ds} increased and become more stable. The transfer characteristics were not appreciably affected by the PFBT treatment; a small decrease in mobility of C18-silane dielectric SAM was observed.

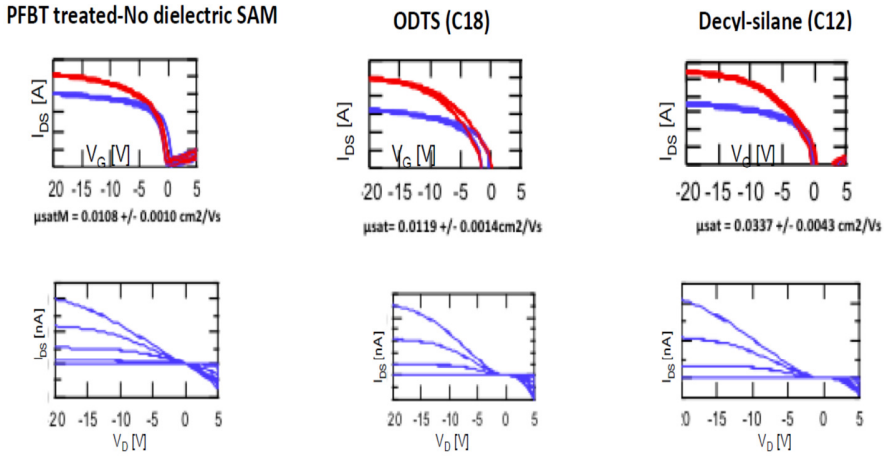


Figure 27– First and second rows IV curves show input and output TFTs characteristics, respectively. The contacts were treated with PFBT. The silane SAM was vapor deposited (at 60°C) and OSC spin-coated on the polymer dielectrics. 'No SAM+PFBT' sample is a reference sample.

4.3.2 Phosphonic acid SAM treatments on polymer dielectrics devices

The charge transport using linear alkyl terminated SAMs on the polymer dielectrics was examined. The effects of three different lengths of the alkyl chains using phosphonic acids as the reactive group; octylcylphosphonic acid (C8), dodecylphosphonic acid (C12) and octadecylphosphonic acid (C18), were here studied. Figure 28 shows the results of water contact angle measurements of the phosphonic acid-treated polymer dielectrics. Effects of a water treatment of the substrates prior to any SAMs deposition are shown in the same graph. It was found that the contact angles for all SAMs treatments were in the same range (51^{o} to 56^{o}). This CA value indicates poor coverage of the phosphonic acid on the polymer dielectric. Water rinsing had no effect on the wettability of the phosphonic acid treated polymer dielectrics.

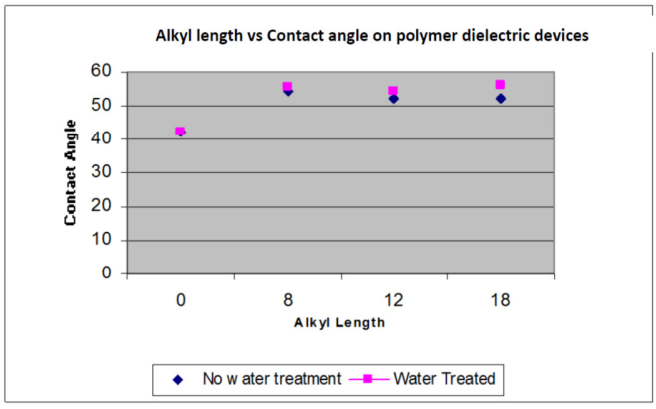


Figure 28- The contact angle on the polymer dielectrics (after phosphonic acid treatment) vs the length of the alkyl chains, with and without water cleaning.

4.3.3 Effects of C18 SAMs silane vs. phosphonic acid SAM treatments on polymer dielectrics

In case of the PA-SAMs treatment prior to the spin-coating of OSC, the gold electrodes of devices were treated with PFBT (15min in ethanol). And modification of dielectrics followed by 15min incubation time in the phosphonic acid. Figure 29 shows the effect of the silane treatments on polymer dielectrics on the TFTs input characteristics for two samples; ODTS treated and one treated with ODTS and PFBT. The gold protection of electrodes with PFBT of the substrates which were silane-treated must performed before applying the SAMs using vapor deposition.

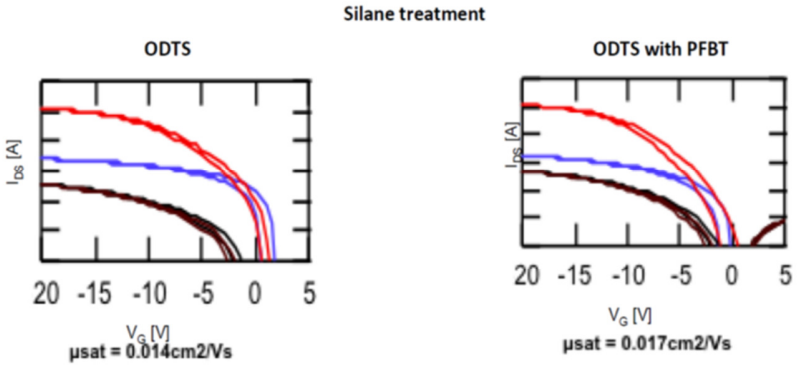


Figure 29- TFTs input characteristics for ODTS and ODTS with PFBT on the polymer dielectric. The silane SAMs were vapor deposited (at 60°C), with and without PFBT-gold treated contacts and OSC spin-coated on the polymer dielectrics. The mobility of both TFTs exhibited almost the same value. The threshold voltage was at zero for both TFTs. No marked differences with regard to the current injection

Figure 30 shows the effect of the phosphonic acid treatment on polymer dielectrics on the TFTs input characteristics for two samples; ODTS (C_{18}) acid treated and ODTS (C_{18}) acid treated with PFBT treatment (of the gold electrodes). The mobility for C_{18} PA was 0.022 cm^2/Vs which is higher than for the silane ODTS (0.014 cm^2/Vs). The results were quite reproducible without any hysteresis. When comparing results in figures 31 and 32, it can be noted that the V_t started at zero for the silane ODTS but for PA-treated samples it shifted to 1 V for C_{18}PA and for C_{18}PA with PFBT it varied between -4 V and 4 V. Thus a small leakage current was at hand for the phosphonic acid treated samples. (Figure 30).

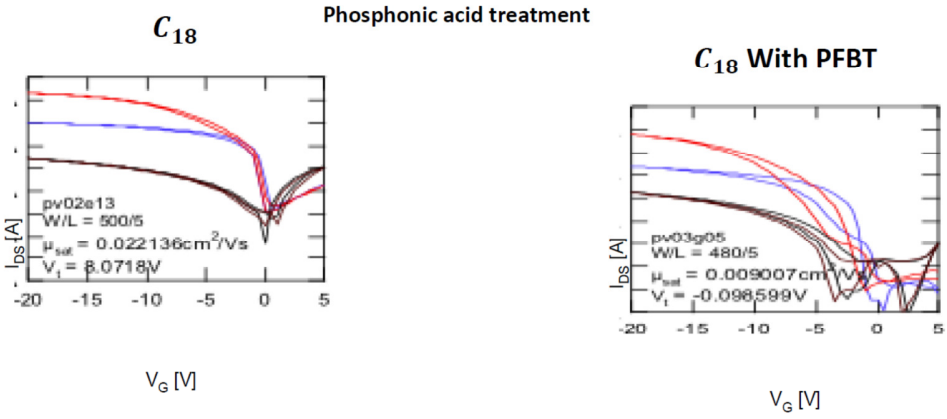


Figure 30 – TFTs input characteristics for ODTS (C_{18}) phosphonic acid treated samples and ODTS (C_{18}) phosphonic acid treated samples with PFBT. The OSC was spin-coated on the polymer dielectrics.

4.3.4 Effects of C12 SAMs silane vs. phosphonic acid SAMs treatments on polymer dielectrics

For preparing substrates with silane treatments, silane SAM was deposited from a vapor gas phase at 60°C and the substrates were PFBT-treated (on gold electrodes) before the SAM deposition on the dielectric. The polymer-dielectrics devices were treated with PFBT (15 min in ethanol), followed by different incubation times (15 min, 4h, 17h) in the phosphonic acid. The results were compared with the TFT performance of samples for which the gold electrodes were not treated with PFBT. OSC was spin-coated on the substrates

The transfer characteristics of the TFTs treated with C_{12}-phosphonic acid on the polymer dielectrics are shown in figure 31. After 15 min the mobility was 0.003 cm^2/Vs which increased when extending the incubation time to 4h to 0.011 cm^2/Vs. This value decreased after 17 h incubation to 0.004 cm^2/Vs. There was no leakage current detected and the threshold voltage started at -1 V. No significant hysteresis was detected. The current injection from the output curves after 4h incubation time exhibited a maximum of -800 nA, but there was also contact resistance. In summary, by increasing the incubation time to 4h, the TFT performance of the PA-treated device improved, but after 17h the TFT performance was poorer.

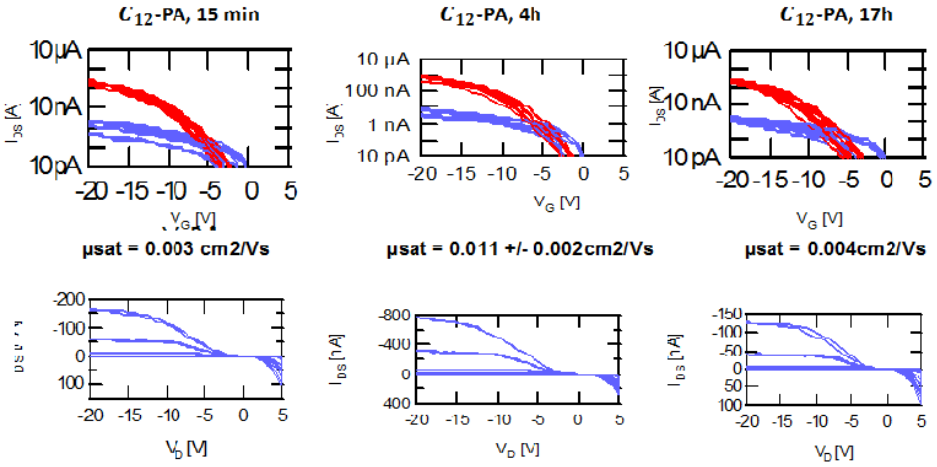


Figure 31 – The first and second rows IV curves shows the input and the output TFTs characteristics, respectively. The samples were treated with C_{12} phoshponic acid for 15min, 4h and 17h (in PA). The contacts were treated with PFBT for 15 min before the SAM deposition.

Next, the transfer characteristics of TFTs treated with C_{12}-silane on the polymer dielectrics with and without PFBT were studied (figure 32). The incubation time in this case was 30 minutes.

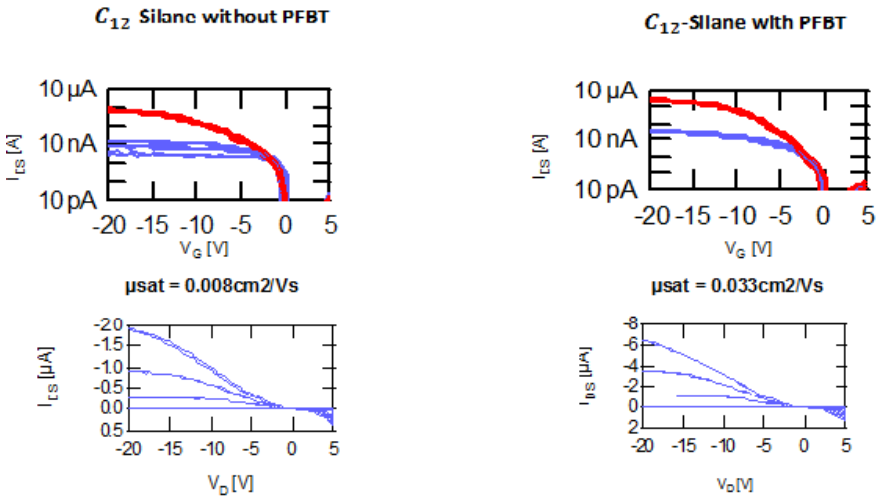


Figure 32 – The first and second rows IV curves shows the input and the output TFTs characteristics, respectively. The samples (polymer dielectric) were treated with C_{12} silane and phoshponic acid with and without PFBT treatment of the contacts. The SAMs were spin-coated on the polymer dielectrics and the PFBT treatment time was 15min.

By applying PFBT, the TFT transfer characteristics of C_{12} –silane treated polymer dielectric showed improvements. A threshold voltage became zero (which was -1 V without PFBT treatment) with no leakage current. Also the mobility increased after applying PFBT. The gold protection also provided a better current injection of -7 μA than with no electrode treatment (-2 μA), see output curves from figure 32. So, by applying PFBT, the contact resistance was reduced.

Now, one can compare C_{12} –PA with PFBT and C_{12} –silane with PFBT SAMs treatments of the polymer dielectrics. The TFT performance from silane deposition from gas phase, which is fast process, showed a mobility of 0.033 cm^2/V_s with V_t at zero volt (figure 32). The corresponding mobility for PA-treated samples was 0.011cm^2/Vs after 4h incubation. Note that the threshold voltage was around -1V for PA-SAM treated devices. These results are in correspondence with the water contact angle indicating a low SAM coverage. The contact angle (CA) of silane-treated surfaces was around 101^o whereas it was 55^o for phosphonic acid coverage. (Compare figure 25, and figure 28).

4.3.5 Overall comparison of SAMs deposition on the polymer dielectric

Comparing results from silane and phosphonic acid SAMs deposition on the polymer dielectric showed that silane deposition with CA of 103^o gave better coverage in comparison with PA deposition with CA of 56^o which resulted in a poorly covered surface. Consequently, the TFT performance from the silane SAMs deposition showed no hysteresis with V_t starting at zero whereas for the PA-treated substrates a shifting of V_t (-4V to 4V) was detected and leakage current also deteriorated the TFT performance. By knowing that silane (from vapor phase) was more reactive than the PA solution and because they easily react with the dielectric surface thus modifying that, these results become understandable.

On the other hand, the obtained transfer characteristics with different alkyl lengths C12 and C18 which were previously discussed (section 4.3.3 and 4.3.4) indicates that by increasing the alkyl length the TFT performance will be improved.

4.4 SAMs on ALD (Atomic Layer Deposition) Al_2O_3 substrate

Atomic layer deposition (ALD) is an ideal technique for depositing ultrathin films with high conformity and precise thickness control. Here Al_2O_3 was deposited with this technique on a flexible substrate which then worked as a dielectric.

4.4.1 Silane spin-coated on ALD Al_2O_3

ODTS (C18) silane and OTS (C8) silane were spin-coated on the unpatterned ALD Al_2O_3 dielectric in order to obtain their water contact angles which are given in figure 33. The

wettability of the C18-treated dielectric corresponded to a CA of 104°. On the other hand, the C8–silane treatment of Al_2O_3 gave a CA of 80°. The ODTS coverage of the polymer dielectric with a CA-value of 103° would then be almost the same as the coverage on Al_2O_3 with CA of 104°.

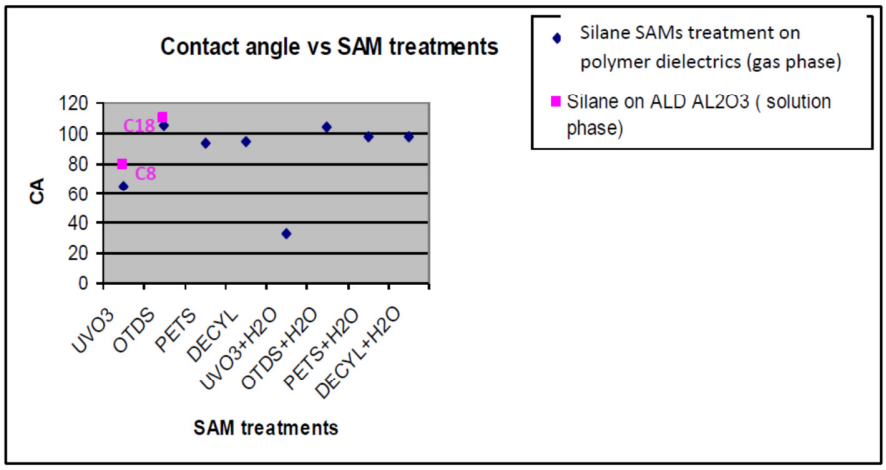


Figure 33- Contact angle measurements (CA) vs. SAMs treatments (silane and phosphonic acid) on Al_2O_3 and polymer dielectrics. The notion UVO_3 indicates that the sample was cleaned by UVO_3 without any further treatments, if sample was cleaned by both UVO_3 and H_2O it was denoted ($UVO_3 + H_2O$). The effects of ODTS (octadecyltrichlorosilane) treatment, ODTS + H_2O treatment, DECYL (dodecyltriethoxysilane) treatment, DECYL + H_2O treatment, PETS (poly (ethylene terephthalate)) treatment and PETS + H_2O treatment of polymer dielectric on the contact angle are included in the graph.

4.4.2 Phosphonic acid SAM treatment of ALD Al_2O_3

The attention was then directed towards C_{18} phosphonic acid as the reactive group and the coverage of SAMs on the Al_2O_3 dielectric, see figure 34. The water contact angle on bare ALD Al_2O_3 was very low, almost 10°. After the SAMs deposition, the contact angle increased to almost 105°, which was not affected by annealing at 100°C or 140°C for 10 min, but the PFBT treatment reduced the CA to 85°. In figure 34 the corresponding mobilities for each device are shown as well. The mobility of the C_{18} –PA treated dielectric was 0.07 cm^2/Vs. If the device first was treated with PFBT for 15 min or 4 h and then deposited with SAM, the mobility increased to 0.1 cm^2/Vs.

The TFT performance of the Al_2O_3 devices was then evaluated. Prior to the spin-coating of the organic polymer, the polymer-dielectric devices were treated with PFBT (15 minutes in ethanol), followed by 15 minutes incubation time in the phosphonic acid. The surface of the substrate treated with octadecylphosphonic acid was dewetting, which resulted in a poor OSC polymer

coverage during spin-coating. Therefore, many devices were not functional with this treatment. Annealing and/or encapsulation of the devices did slightly decrease the hysteresis.

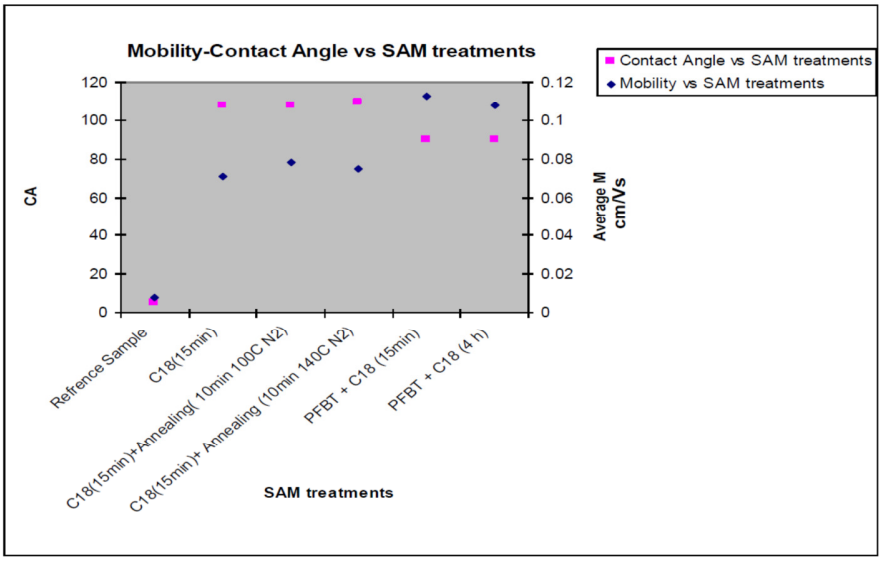


Figure 34- Water contact angle and TFTs mobility resulting from different SAMs treatments of the ALD Al_2O_3 dielectrics. The different SAM treatments were: C_{18} phosphonic acid, C_{18} phosphonic acid with annealing at 100℃ for 10 minutes, C_{18} phosphonic acid with annealing at 140℃ for 10 minutes, PFBT treatment of gold electrodes with C_{18} phosphonic acid for 15 minutes, PFBT treatment of gold electrodes with C_{18} phosphonic acid for 4 hours. The reference sample was bare ALD Al_2O_3 without any SAM treatment.

The possibility of applying the OSC on Al_2O_3 by the inkjet method at a temperature of 70°C was here investigated to some extent. The TFTs characteristics (input) with the Al_2O_3 dielectrics without using any silane or phoshonic acid SAMs is shown in figure 35. This result is regarded as a reference for the TFT performance of inkjet-printed OSC on Al_2O_3 dielectrics for further studies after applying different SAMs.

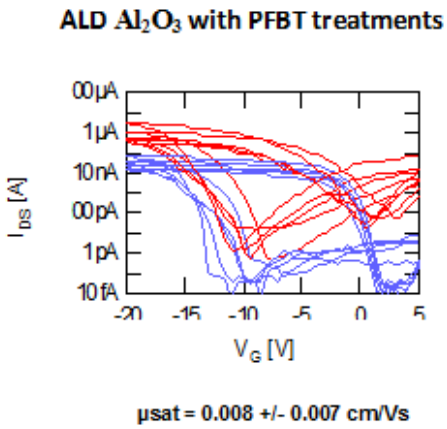


Figure 35-The TFT performances (input) of the ink-jet printed polymer semiconductor on ALD Al_2O_3 with PFBT-treated gold electrodes.

The effects of different silane SAMs treatments and phosphonic acid SAMs treatments (with or without a PFBT treatment of the gold electrodes) on TFT performance of the polymer semiconductor inkjet-printed at 70°C on TFTs with Al2O3 dielectrics are shown in figure 36.

The morphology of the organic semiconductor was not significantly changed by the trichlorosilane and phosphonic acid treatments, see figure 36. The current injections were in the same range, about 10 µA for both treatments. The highest currents and mobilities were noted for C18-PA with PFBT. Large hysteresis (Δ~5 V) was detected for all devices, and large contact resistances were visible in the output curves. For 'no SAM' a larger hysteresis (Δ >10 V) was observed. Annealing and encapsulation of the devices did not decrease the hysteresis.

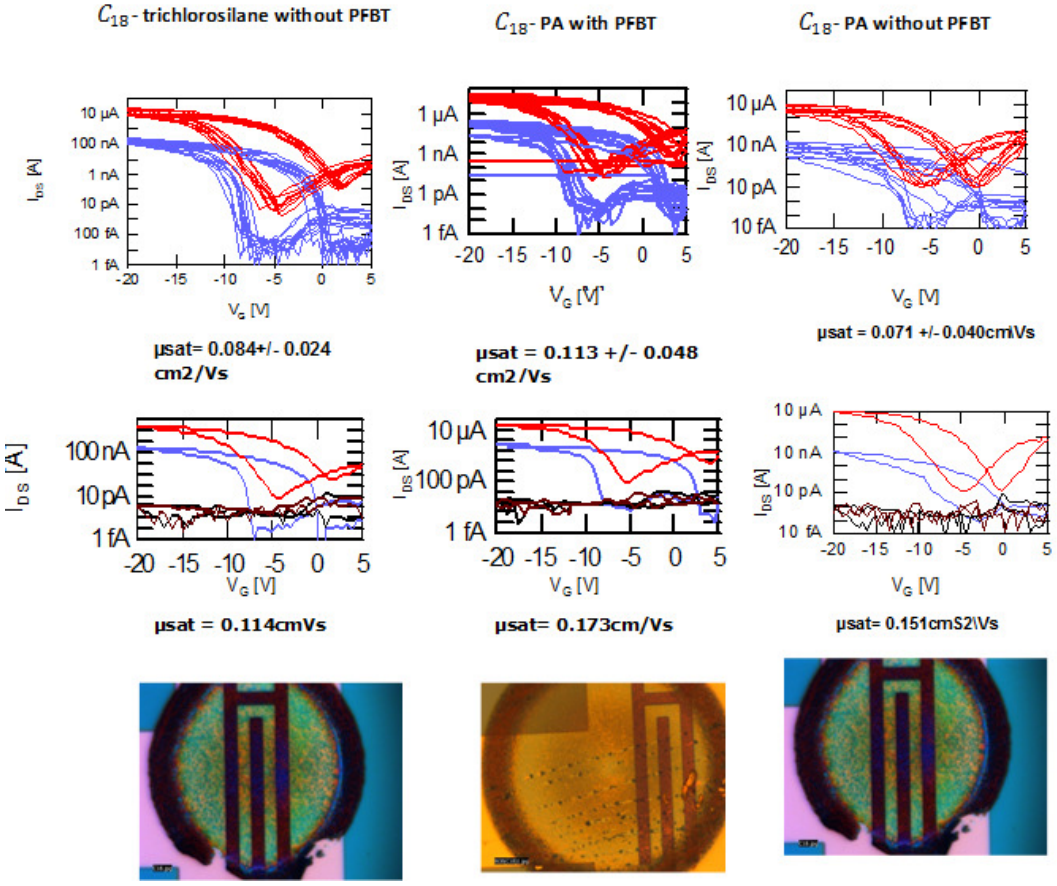


Figure 36- The first row shows all TFTs transfer characteristics with ALD Al_2O_3 dielectrics and inkjet-printed OSC polymer. From the left, the first IV curve shows the TFTs transfer characteristics of a sample treated with C_{18}-silane without PFBT The two rights IV curves show the TFTs performances of PA-treated samples, with and without PFBT-treatment, respectively. The second IV curves row shows the transfer characteristics of single TFT device with relevant dielectric and electrode treatments. The appearances of the inkjet-printed OSC on these single TFT devices are shown in third row.

4.5 Summery of SAMs (polymer dielectrics and ALD Al_2O_3 dielectrics) effects on the TFT performance

SAMs on polymer dielectrics

- The highest contact angles were obtained with C18-silane deposition (ODTS), indicating that the coverage with this SAM of polymer dielectric must be the best one in this case.

- Low mobility, even with good ODTS SAM coverage, was noted for all the polymer dielectrics (silane treatments or phosphonic acid treatment)

- Despite the weak TFTs performance with the polymer dielectrics, the transfer characteristics of these transistors showed hysteresis-free curves. (No shifting in the threshold voltages was detected.)

- V_t ~ 0 V in all cases, except for samples with 'no SAM' which showed V_t > 5 V.

- Very good reproducibility for samples with ODTS SAM was obtained. The threshold voltage exhibited an experimental scatter of < 3%.

- The TFT performance of samples with the polymer dielectric was hardly influenced by any of the SAMs treatments.

SAMs on ALD Al_2O_3 dielectrics

- Large hysteresis (Δ~5 V)) was detected for all devices, and large contact resistances were visible from the output curves.

- For samples with 'no SAM' treatment, a substantial hysteresis (Δ >10 V) was observed.

- Annealing and encapsulation of the devices did not decrease the hysteresis.

- Hydrolyzing (cleaning with water) the Al_2O_3 surface prior to the SAM deposition is required for good SAM coverage.

4.6 SAMs on PVP dielectrics

As mentioned before, the emphasis laid on the stability of the TFT performance measured as variation in current, mobility, threshold voltage, etc. But the results regarding the TFTs performances with polymer dielectrics and ALD Al_2O_3 dielectrics did not achieve the goal of project (e.g. stability of high mobility and current), see 4.5. Thus, there was a need for trying other dielectrics, in this case PVP (poly-4-vinyl phenol) dielectrics (sometimes used as an organic substitute for silicon dioxide). A thin film of PVP was deposited on the insulator (as a surface treatment) by spin-coating. The prepared PVP dielectrics were evaluated with regard to their water contact angle with different SAMs on this substrate and also with respect to their TFT performance.

The coverage of SAM on the PVP dielectrics was indicated by measuring the water contact angle for different silane SAMs treatments. ODTS (C18), OTS (C8) and TCPS SAMs were spin-

coated on substrates. The CA-value corresponding to each SAM treatment can be compared with the reference (No SAM) sample in figure 37.

This study indicated a similar coverage of ODTS on the polymer dielectric and on the PVP dielectric (CA 103°). By decreasing the alkyl length to C8, the contact angle decreased to 65°. The corresponding TFT performances of the ODTS-treated devices are shown in figure 38.

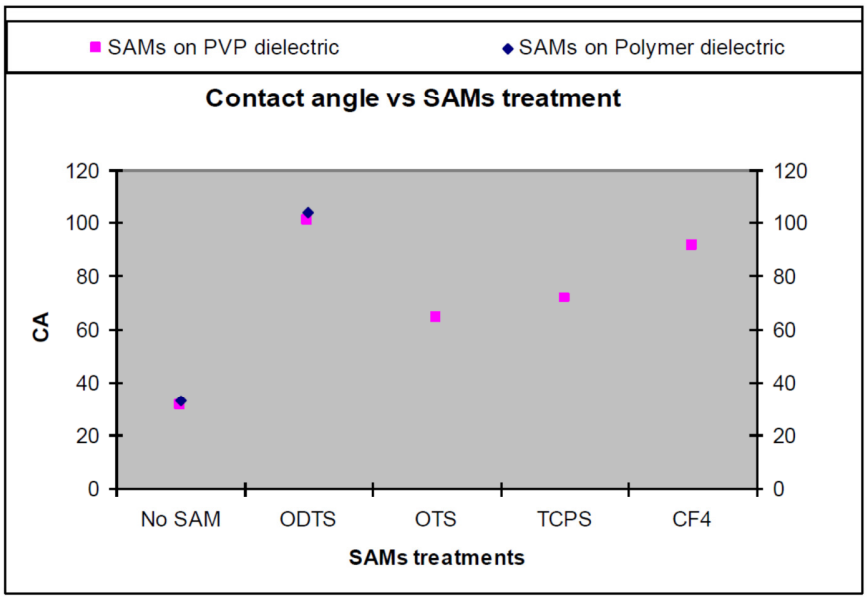


Figure 37- The contact angle vs. SAMs treatments on polymer dielectrics and PVP dielectrics. No SAM: reference sample without any SAM treatment. ODTS: octadecyltrichlorosilane SAM. OTS: octyltrichlorosilane SAM, TCPS: tricresylphosphatesilane. CF_4 : tetrafluoromethane.

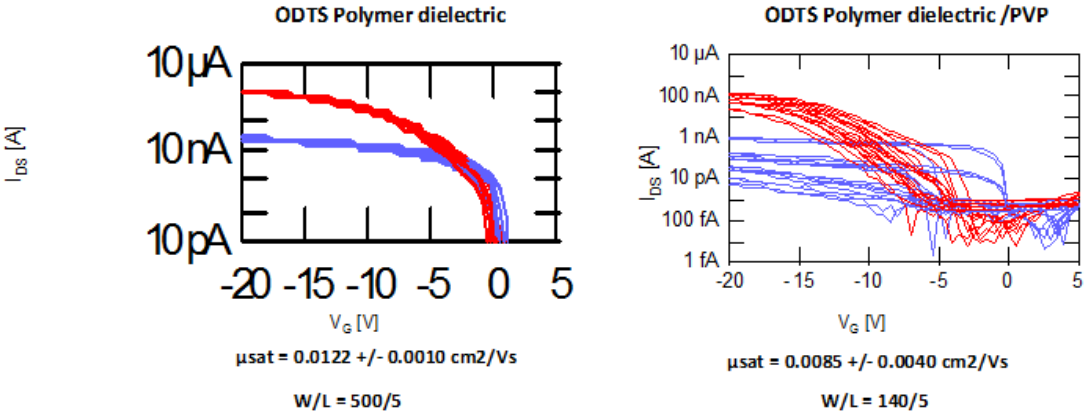


Figure 38- The TFT transfer performances of ODTS-treated TFT devices for polymer dielectric and PVP dielectric semiconductors. The organic semiconductor was applied with spin-coating. The threshold voltages of the PVP dielectrics spread within a quite large range ($-5\ V < V_t < 7V$.)

Unexpectedly poor results were obtained for the TFT performance of the PVP dielectrics. The polymer dielectrics and PVP dielectrics had the same SAMs coverage (CA 103^{o}), see figure 37, but the TFT performance of the devices showed:

- Low mobility with PVP- and polymer dielectrics
- Hysteresis and large spread in V_t (see figure 38) were detected for the PVP dielectrics.

It was noticed that during the TFT measurements, the pins of the measuring device could easily destroy the surface of PVP layer (200 nm is the layer thickness of PVP) and creating shortcuts, thus deteriorating the performance of the transistor. In order to avoid the problem of dielectric pinning and shortcuts, an oxide layer between the gate (n-doped Si) and the PVP dielectric was inserted.

By inserting n-doped Si (Si^{++}) as a middle layer and measuring the TFT characteristics of new dielectrics, the problems were solved. The mobility and current were lower for the SiO2/PVP dielectrics than for the PVP dielectrics. This is the result of using two layers of dielectrics instead of one. In order to clarify why the mobility and the current decreased when using double dielectric, it can be assumed that instead of one capacitor (dielectric) there are now two capacitors are connected in series. Then a lower total capacitance is obtained and consequently a reduction in the current and mobility. The motivation for this can be found by considering the reasoning below with the final result given by equation (8).

It is assumed that SiO_2/PVP substrate as a dielectric was applied. The capacitance of PVP is 10 nF and that of SiO_2 is 17 nF so the capacitance of SiO_2/PVP is 6.3 nF. This comes from the rule for capacitors in series:

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{Cn} \qquad (4)$$

By using equations 5, 6 and 7 below, equation 8 can be obtained:

$$V_b = E_b\, d \qquad (5)$$

$$C = \frac{q}{V} \qquad (6)$$

$$\oint E\,ds = \frac{q}{\varepsilon} \tag{7}$$

$$\frac{E_{PVP/SiO2}}{E_{SiO2}} = \frac{\frac{\varepsilon_{PVP/SiO2}}{C_{PVP/Si=2}}}{\frac{\varepsilon_{SiO2}}{C_{SiO2}}} = \frac{\frac{dV_G}{dt}}{\frac{dV_G}{dt}} = 1 \tag{8}$$

Due to the difference in capacitance between SiO_2 and SiO_2/PVP layers (17 and 6,3 nF, respectively), it follows that in to apply comparable electrical fields/bias over the two types of active materials, V_{on} has to be increased three (exact value is 2.6) times over the double dielectric layer (SiO_2/PVP). It means that the previous gate voltage of -20 V should be changed to -60 V. For the TFT measurements, the drain voltage also should be changed to obtain the adequate V_g value. The gate voltage was decreased to -60 V and the transfer characteristics were determined. But below V_g = -30V shortcuts can happen. Besides, the leakage current increased with increasing gate voltage (V_g), showed by arrowed line in figure 39. The mobility and current at V_g = -30 V were slightly increased compared to V_g = -20 V. Also, the leakage current at -30V was very low (figure 39). So in conclusion the V_g for SiO_2/PVP substrate was fixed at -30 V and subsequently V_d was fixed at -30 V for further measurements.

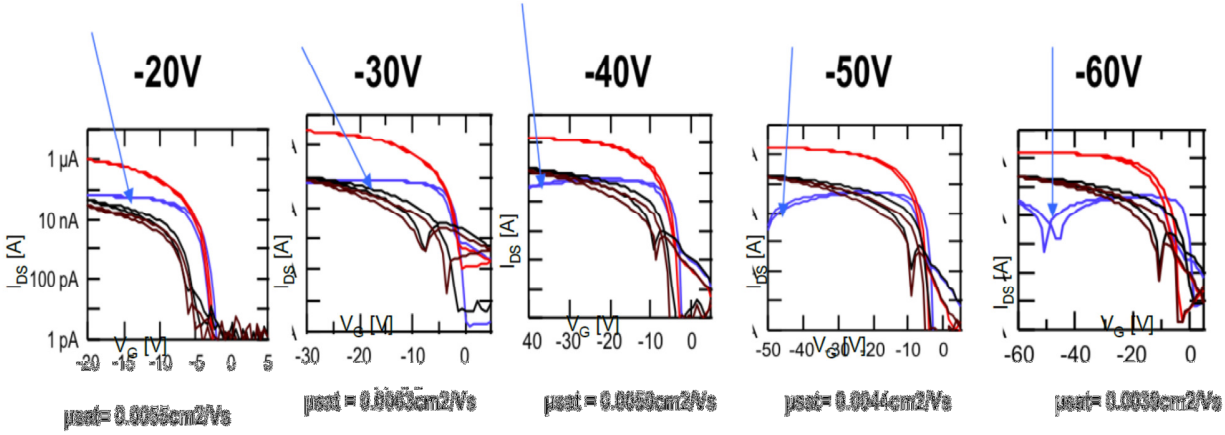


Figure 39- The TFT transfer characteristics for SiO_2/PVP substrates treated with ODTS. The gate voltage V_g was decreased from -20V to -60V in order to find the maximumI_{ds}. At $V_g > -30V$, shortcuts appeared (see the arrows which indicate the drop in current).

4.7 Protection of the gold electrodes during ODTS deposition

It was noted that the ODTS transistors often suffered from a noticeable contact resistance (figure 40). The TFT performance was irregular and an unstable current charge was detectable, both in the transfer and the output characteristics.

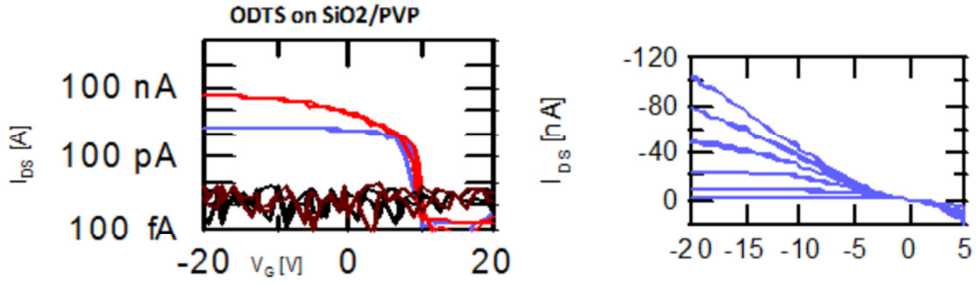


Figure 40- TFT performance of a *W/L* = 140/5 device. SiO2/PVP dielectrics were used with spin-coated ODTS and OSC SAMs. Left, IV-curves showing input characteristics (transfer characteristics). Right, IV-curves showing output characteristics and unstable currents in the output curve are detectable.

In order to improve current injection and to have stable current, the Au electrodes were protected during the ODTS deposition by a PFBT coverage. First, ODTS were deposited on PVP unpatterned substrates at a temperature of 80^{o}C. Then, PFBT was applied on the electrodes. Since PFBT dissolves at high temperatures, it is important to perform the SAMs treatment at high temperature prior to applying PFBT. Figure 41 shows the water contact angles values for different SAMs treatment on bare PVP and gold.

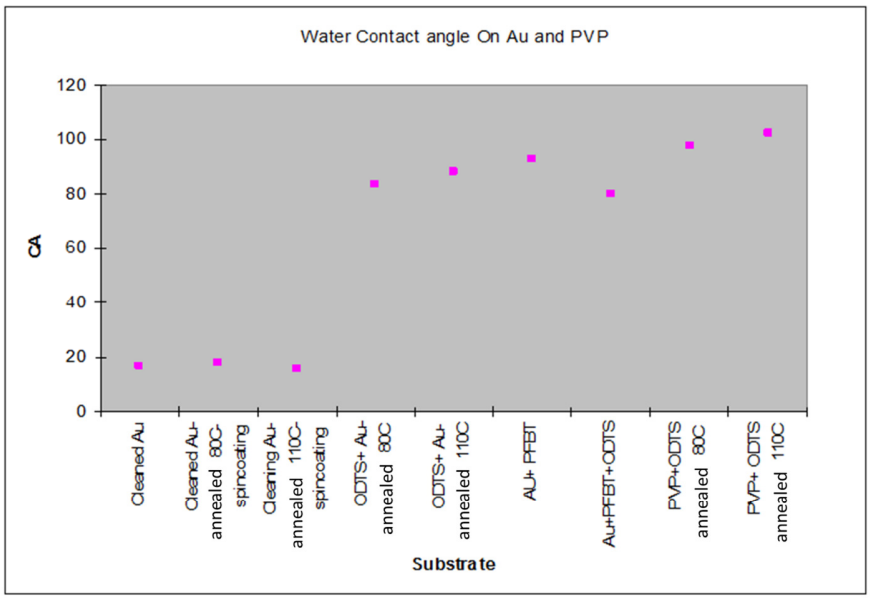


Figure 41- The effect of SAMs treatment of gold and PVP substrates on the contact angle. Notations: Cleaned Au (just cleaned with UVO_3), Cleaned Au and annealed at 80℃, Cleaned Au and annealed at 110℃, Spin-coated ODTS on gold and annealed at 80℃, Spin-coated ODTS on gold and annealed at 110℃, Gold treated with PFBT, Gold treated with PFBT and ODTS, PVP substrate treated with ODTS and annealed at 80℃ and PVP substrate treated with ODTS and annealed at 110℃.

The obtained results (figure 41) are summarized below:

- The CA-values for cleaned Au and annealed at 80°C/110°C were in the same range, thus annealing had no effect on the surface coverage for bare and clean Au.

- The CA-values for ODTS SAM deposited surfaces annealed at 80°C or 110°C were in the same range (84^o and 88^o, respectively), thus indicating the same surface coverage.

- The CA of the PFBT treated Au surface was 92^o. But after annealing and applying ODTS SAM, it decreased to 80^o.

- Deposition of ODTS SAM on PVP and annealing at 80^{o}C or 110^{o}C gave the same coverage. (CA 98^o and 102^o, respectively).

Finally, one can conclude that annealing of the substrates (PVP and gold) had no significant effect on the coverage of SAMs and consequently on the TFTs performances. But, as noted earlier, PFBT can improve the current injection from source and drain (gold contact of transistors) to the semiconductor/dielectric interface. Thus, the charge transfer characteristics of the TFTs with SiO_2/PVP dielectrics when treated with PFBT and ODTS were evaluated (figure 42).

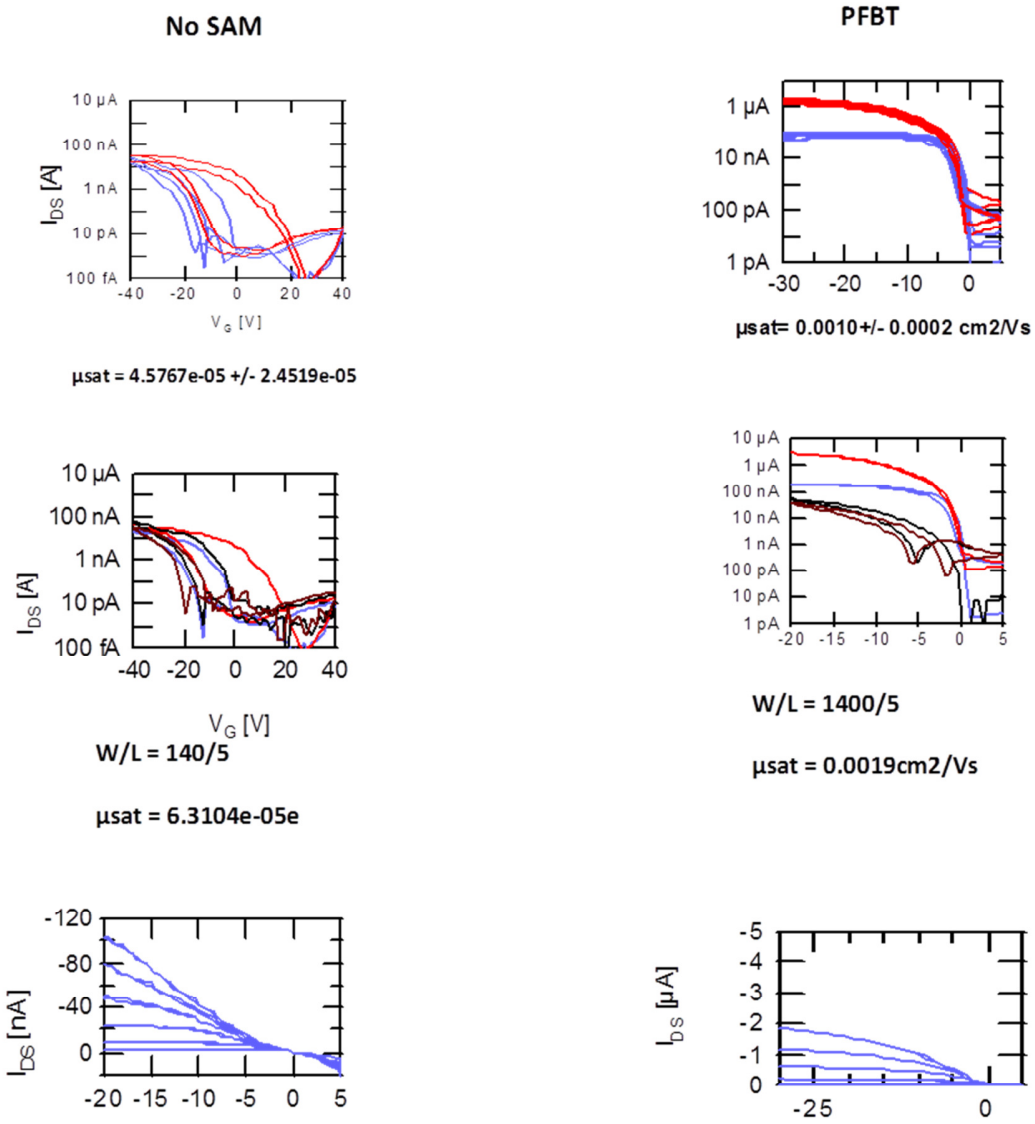


Figure 42- The TFT performances of devices with SiO_2/PVP dielectrics for two samples. The No SAM is the reference without any dielectric treatment and the other sample was treated with PFBT (gold electrodes) (15min) and ODTS was spin-coated on the dielectric. The first row shows the transfer characteristics of all TFTs, the second shows just one sample of TFT device input performance and the third row shows the output characteristics of the TFTs.

The charge transfer of devices with OSC spin-coated on SiO_2/PVP dielectrics without any SAMs was taken as a reference. For these devices, a large leakage current (I_g) was detected. Insulation led to a lower leakage current and increased the mobility, but the source-drain current (I_{ds}) of device was still low and in the same range as the leakage current. Protection of the Au-electrodes with PFBT was then tried in order to improve the charge injection and lower the contact resistance.

Figure 42 shows the TFT performance after PFBT protection (15 min), which resulted in an increased charge injection and mobility. The contact resistance decreased and V_{on} started sharply at zero voltage and decreased the hysteresis compared to the case without PFBT treatment. Lower leakage current compared to the reference devices was obtained and there was no need to insulate the transistors. Improving the charge injection by using PFBT protection prior to the ODTS silane spin-coating was a further aim. The effect of having PFBT SAMs on the electrodes before and after the ODTS deposition was compared with PFBT treatment just after the ODTS spin-coating, figure 43.

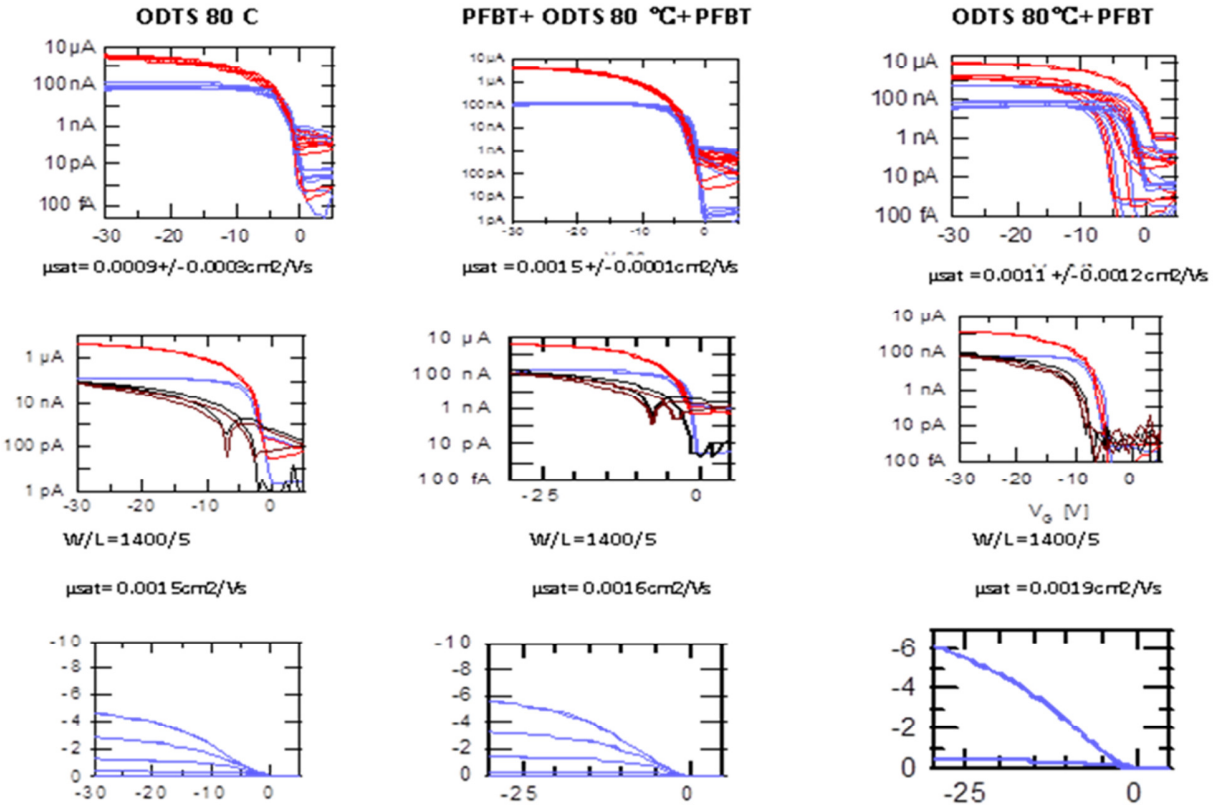


Figure 43- The TFT performances of devices with SiO_2/PVP dielectrics for three samples with spin-coated OSC. The first row shows transfer characteristics, the second single device input performance and the third output characteristics of the TFTs. The first sample is SiO_2/PVP dielectrics with silane-C18 spin-coated at 80℃. The second one is with a PFBT gold treatment (15min) and ODTS spin-coated on the dielectric followed by spin-coating of toluene, and a further PFBT treatment (15min). The third one is sample with spin-coated ODTS on the dielectric followed by spin-coating of toluene, and a final PFBT treatment (15min).

Comparing the TFT performance of the reference sample (cleaned TFTs devices with SiO_2/PVP dielectrics without any SAM treatment, figure 42) with SiO_2/PVP substrates treated with ODTS (figure 43) revealed that the charge current improved (5 μA) at a gate voltage of (-30 V) (compare the output characteristics (I_{ds} vs V_D) for devices shown in figures 42 and 43). A charge current of 1 μA was obtained for the devices which were treated with PFBT (without any silane treatment), figure 42, whereas this value was improved to 10 μA for silane-treated devices (figure 43). On the other hand, for devices without any silane treatment (but with PFBT treated gold electrodes) still a high contact resistance and a high leakage current was detected. For both TFTs devices (silane treated substrates and PFBT treated electrodes) V_{on} started at zero.

By applying PFBT for (15min) before and after the ODTS deposition, the charge injection increased to 5.8 μA, and the mobility increased to 0.0015 cm^2/Vs. Also, the contact resistance decreased slightly and V_{on} started sharply at zero voltage (figure 43, PFBT+ODTS 80℃+PFBT). The output curves of the dielectric with gold treatment after the ODTS deposition (figure 43), showed that the charge injection had increased to 6.3 μA and that the mobility stayed constant at 0.0011 cm^2/Vs. The scatter in V_t was quite large, from -5 V to 5 V (shown in figure 43, the input curves for ODTS 80℃+PFBT devices). This threshold voltage shifting (V_t varied from -5 V to 5 V) can be due to ODTC covering of the gold electrodes during deposition.

To conclude; the optimized SAMs layer for modifying the dielectric and OSC interface is obtained by immersing the substrate in PFBT (15 min), then ODTS spin-coating and then again a PFBT treatment (15 min).

Finally this optimized process was used for preparing devices for ink-jet printing of OSC.

4.8 Jettability of the OSC polymer on optimized SAMs applied on SiO_2/PVP dielectrics

Here jettability means the ability of OSC to be placed on substrates by using ink-jet printing. As mentioned earlier, ink-jet printing is an important direct patterning process for OSC on a field effect transistor (FET) in the form of a thin film. For a successful patterning, the drop jettability is important and depends on the frequency, drop volume, drop velocity and etc, see section 3.4. Characterizing and analyzing the OSC jetting and patterning on substrates with a SAMs treatment and then evaluating the relevant TFTs performance was the next challenge.

First, the charge transfer characteristics of OSC on SiO_2/PVP dielectrics when it had been SAMs-treated with ODTS (silane spin-coated) and PFBT treated before and after the silane treatment was studied.

After ink-jet printing (IJP) of OSC, the process was correlated to the device performance. For recognizing the influence of IJP on the charge transfer, the corresponding devices with spin-

coated OSC were prepared. Thus, two processes (IJP, spin-coating) were evaluated, figure 44. It was found that the current injection and mobility improved six times using IJP. For the spin-coated sample V_{on} started sharply at zero volts but V_{on} for the IJP sample did not start exactly at zero volts; there were some shifts, lower and higher than zero volts, figure 44.

Figure 44- The TFT performance (transfer characteristics) of devices with SiO_2/PVP dielectrics. The electrodes were first treated with PFBT (15 min) and silane-C18 (spin-coated) followed by spin-coating of toluene and finally PFBT treated (15 min). The organic semiconductor was inkjet-printed (IJP), left graph and spin-coated in the right graph.

Typical IV-curves for IJP and spin-coated devices are compared in figure 45.

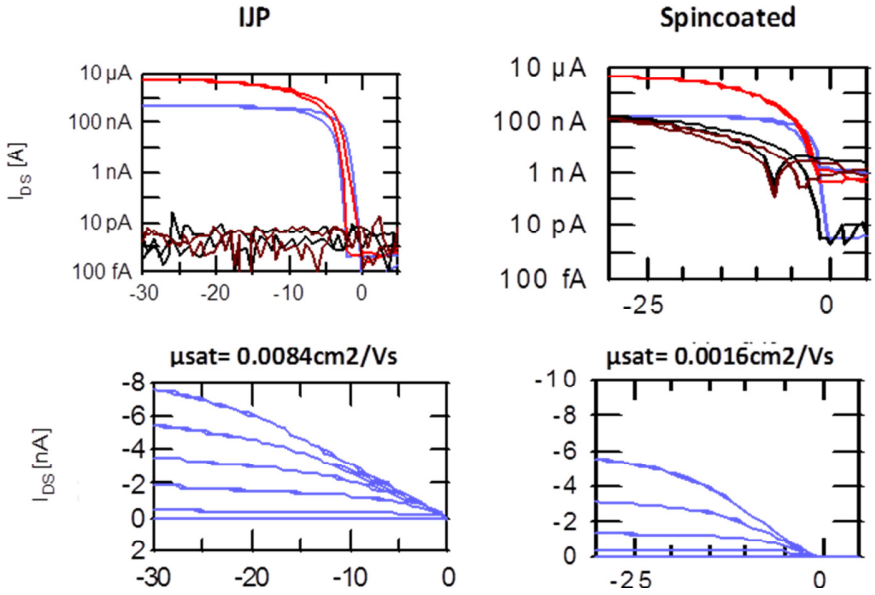


Figure 45- TFT performances (first row: input and second row: output characteristics) of SiO_2/PVP dielectric devices (W/L = 1400/5). First, the gold electrodes were treated with PFBT (15 min), second, silane-C18 applied by spin-coating, followed by spin-coating of toluene and finally a post-treatment with PFBT (15 min). The organic semiconductor was inkjet-printed (IJP) on left graph and spin-coated on the right graph.

The IJP devices exhibited a current injection promotion to -8 µA (spin-coated 5.8 µA) and the IJP mobility obtained was μ_{sat}= 0.0084 cm^2/Vs, which is higher than the spin-coated mobility (μ_{sat}= 0.0016cm^2/Vs). No leakage current was detected for the IJP sample, but a low leakage current was noted for the spin-coated sample, figure 45.

The morphology of the OSC film when it was spin-coated or ink-jet printed on the SiO_2/PVP dielectric (SAMs treatment: PFBT treated (15 min) before and after ODTS silane treatment) was subsequently examined.

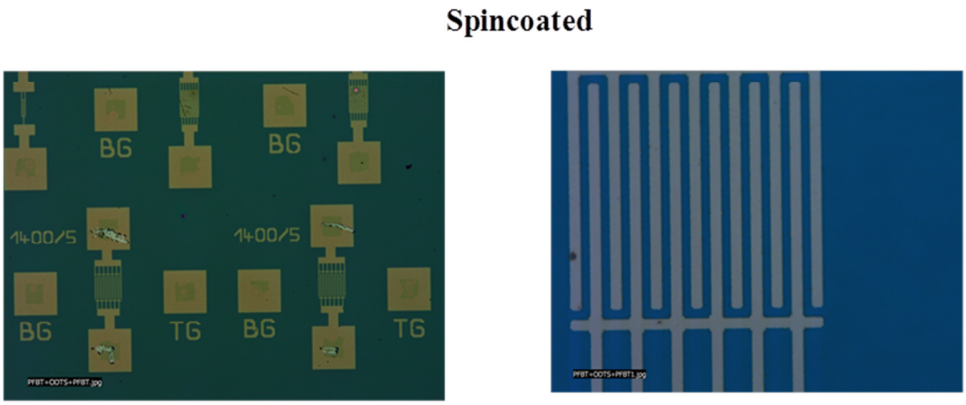


Figure 46- Morphology of a thin layer of OSC spin-coated on SiO_2/PVP dielectric devices (SAMs treatment: PFBT treated (15 min) before and after ODTS silane treatment). The left photo shows a number of TFTs and the right one shows single TFT fingers. Here the presence of a uniform layer of OSC can be established by scratching on the gold pads (left photo).

Figure 46 shows a very thin but uniform layer of spin-coated organic semiconductor covering the silane-treated dielectric surface. The presence of polymer can be detected by make a scratch on the gold pads (source and drains of TFT), left photo. This indicates that OSC completely covers TFTs layout, source and drains. Besides, the area between the TFTs is covered with OSC as well.

Microscopy examination of the ink-jet printed OSC revealed that the droplets on many devices were not positioned exactly on the fingers of the transistors (figure 47). There was a thought that this problem can be solved by using TFTs with an appropriate finger width. Therefore, in order to find the appropriate TFT channel width, the TFTs performances obtained with different finger widths were determined. Note that length of device was kept constant. The charge transfers after the width correction for a number of devices are shown in figure 47.

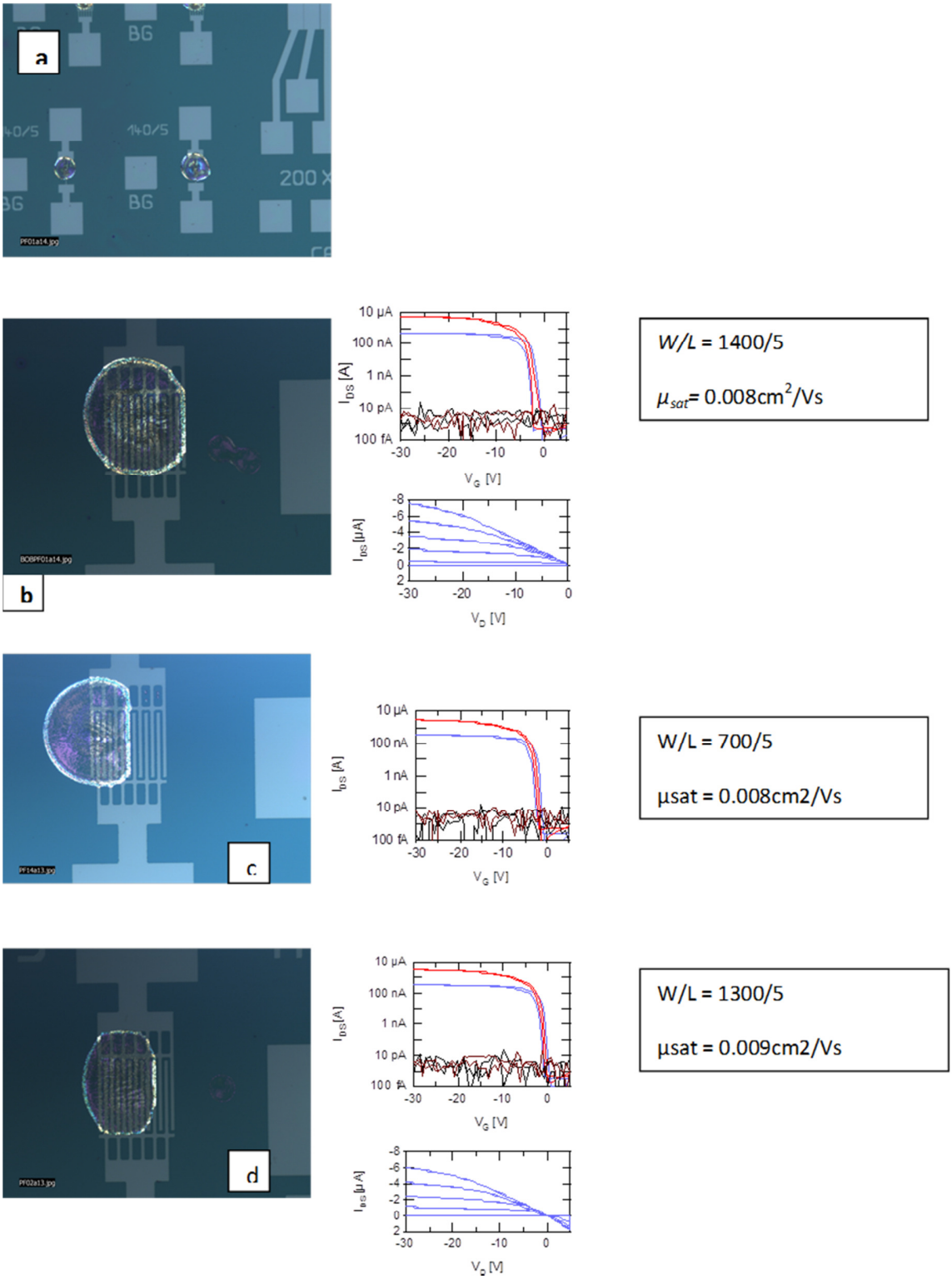


Figure 47- The substrates used were SiO_2/PVP dielectrics (SAMs treated, PFBT (15 min) before and after the ODTS silane treatment). With ink-jet printed OSC. The micrographs (a,b,c,d) show the morphology of OSC on single TFTs with different widths. The corresponding TFT performances (input and output) are included in the figure.

To conclude this section, it may be fair to state that if the OSC droplets from ink-jet printing cover the TFT finger properly, a reasonably good TFT performance can be obtained. Stability of the current in the output curves and a high current injection and high mobility (transfer characteristics) were noted. Thus, in the present study, ink-jet-printing would be preferred over spin-coating for applying OSC on the TFTs.

4.9 Top gate vs bottom gate performance

The aim was to compare the bottom-gate and the top-gate performance of OSC. The silver (Ag) top-gate was ink-jet printed. Figure 48 shows these top-gates.

First, the TFT performance of the bottom gate was measured. The OSC was spin-coated on the polymer dielectric without any SAMs treatment of the dielectric. The transfer characteristics for a typical bottom-gate device are shown in figure 49. Next, a silver top gate was ink-jet printed on the same TFT and once again the transfer characteristics using the bottom gate were measured. Next, the silver top-gate was used as a gate electrode and input characteristics ($I_{ds} - V_g$) performances were recorded (figure 49).

All top-gate devices used worked. In both the bottom-gate (BG) devices and the top-gate (TG) devices, the threshold voltages started at zero volts. Only a low leakage current was detected, which probably can be eliminated by applying a thicker dielectric layer. The top-gate provided the higher mobility $\left(0.1 cm^2 V^{-1} s^{-1}\right)$ than the bottom gates. The charge injections in both TFTs were similar; $10 \mu A$ (figure 49).

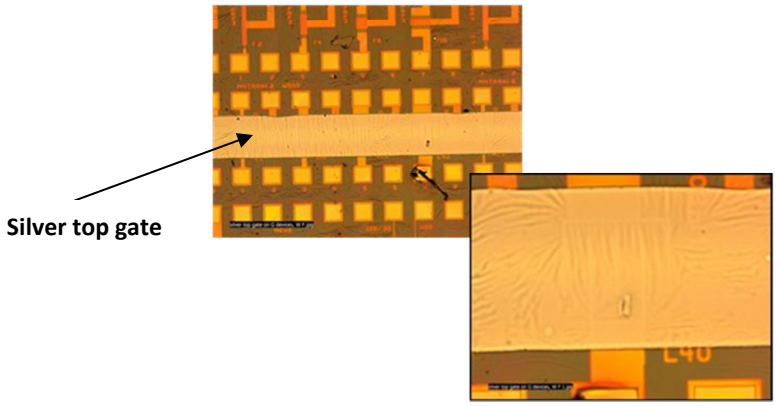


Figure 48-Ink-jet printing of the silver top-gate on the polymer dielectric substrate.

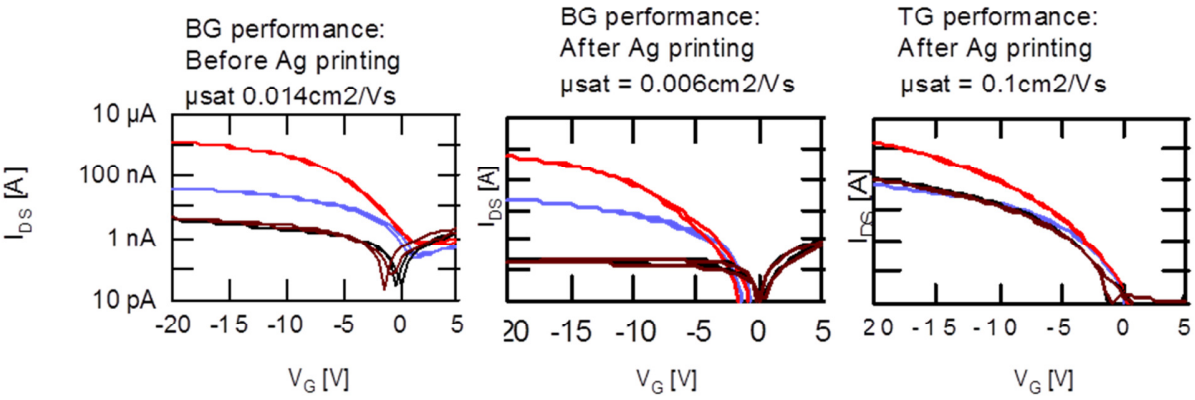


Figure 49- The transfer characteristics of single devices with *W/L* = 500/5. No SAMs treatment of the polymer dielectric. The left IV-curve shows the TFT performance in case of the bottom-gate polymer dielectric. The middle figure shows the input characteristic of this bottom-gate device after ink-jet printing of the top silver gate. The right IV-curve shows the TFT performance of the device using the silver gate as a top-gate.

5. Conclusion and future prospects

When studying the influence of a surface treatment of the dielectric on the performance of the organic semiconductor, we found that SAMs have an important effect on the threshold voltage of organic thin-film transistors. The dependence of V_t on the surface treatment was attributed to trapping of electrons by water and surface hydroxyl groups on the surface. Application of a surface treatment on the dielectrics has been suggested in the literature to lead to passivation and block trapping resulting in a V_t shift and even unstable I_{ds} currents which can be due to electron conducting from field-effect behavior in organic semiconductors.

We noted an excellent reproducibility of the charge transport properties after improving the injection properties using PFBT on Au-electrodes prior to a SAM treatment of dielectrics. Further, we showed that a treatment of the dielectrics by SAM can decrease the electron trapping in p-type devices. An increased current detected from the TFT performance is a sign of this effect. As a result, an optimized surface treatment for applying the polymer semiconductor is to treat the polymer dielectric with ODTS SAMs and apply gold protection (PFBT treatment) before and after the dielectric treatment. Finally, very low off (leakage) current by patterning the polymer semiconductor with IJP is obtained which makes the ink-jet printing the optimal process for applying OSC. Thus, IJP is due to good reproducibility and low off current suitable for circuitry applications (as uni-polar circuits and/or CMOS).

Clearly, further research should include an investigation of the reproducibility on large (6 inches) areas. The TFT performance can be evaluated for a large area (150 mm wafers), where the emphasis lays on the stability of the TFT performance measured as the spread in current, mobility, threshold voltage, etc. Optimizations of the printing technique and the post treatments (e.g. annealing, passivation layer deposition) can be studied. Other concepts, like improved control of drop placement during IJP are also of interest. An improved coverage of transistors by IJP droplet leads to reliable performance of the TFT.

6. References

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