Thesis for the Degree of Doctor of Philosophy

Silicon Integrated HBV Frequency Multipliers for THz Applications

Aleksandra Małko

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
Göteborg, Sweden 2015

Silicon Integrated HBV Frequency Multipliers for THz Applications
Aleksandra Małko

ISBN 978-91-7597-145-2

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie nr 3826
ISSN 0346-718X

Technical Report MC2-297
ISSN 1652-0769

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience – MC2
Chalmers University of Technology SE–412 96 Göteborg, Sweden
Phone: +46 (0)31–772 1000
URL: http://chalmers.se/mc2/EN

Cover: *Bottom:* SEM image of silicon integrated Heterostructure Barrier Varactor (HBV) diode in a 474 GHz frequency quintupler circuit. *Top/left:* Close up of the diode's mesa. *Top/right:* TEM composite image of the transferred HBV material on silicon substrate. Insets show: *Top:* magnified $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/AlAs$ area, and *bottom:* $In_{0.53}Ga_{0.47}As$ and silicon with 5 nm thick amorphous oxide layer in between.

Printed by Kompendiet
Göteborg, Sweden, February 2015

Abstract

This thesis deals with integrated varactor diode circuits for terahertz (THz) applications. In particular hybrid, monolithic microwave integrated circuits (MMICs), and heterogeneous integration are explored for frequency multiplier applications. Each of these techniques addresses different requirements for high power and high frequency electronic circuits. Namely: high thermal conductivity (κ) of substrates for enhanced power capabilities, process reproducibility of small diode and circuit component dimensions, and finally machining properties for enhanced robustness and functionality.

A fixed tuned 175 GHz frequency quintupler with a flip-chip assembled Heterostructure Barrier Varactor (HBV) diode was demonstrated. The microstrip circuit was fabricated on AlN substrate - a material with high thermal conductivity. The device delivers 60 mW of output power corresponding to 6.3 % conversion efficiency.

The heteregeneous integration of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HBV material structure onto silicon and silicon-on-insulator (SOI) substrate was done in a process employing low temperature plasma assisted wafer bonding. Using this technology a frequency tripler ($\times 3$) for W-band (75–110 GHz) and frequency quintupler ($\times 5$) for 474 GHz were fabricated. The performance of the W-band frequency tripler delivering more than 180 mW of output power is comparable to the identical design in InP MMIC technology. The 474 GHz frequency quintupler circuit was fabricated on SOI substrate, hence robust and unform 20 μm thick circuits were achieved. This multiplier delivers 2.8 mW of output power, and it represents the highest frequency of operation for HBV-based frequency multipliers.

By enabling the integration of compound semiconductors onto a silicon substrate, an increase in the performance and functionality of the device is achieved. Moreover, due to good thermal and mechanical properties of silicon, as well as established process technology for this material, a new generation of THz monolithic integrated circuits is possible.

Keywords: Compound semiconductors, epitaxial transfer, frequency multipliers, heterogeneous integration, Heterostructure Barrier Varactors (HBVs), integrated circuits, MICs, silicon, THz sources, wafer bonding.

List of publications

Appended papers

This thesis is based on the following publications:

[A] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "A 474 GHz HBV Frequency Quintupler Integrated on a 20 μm Thick Silicon Substrate," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 1, pp. 85–91, January 2015.

[B] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "Silicon Integrated InGaAs/InAlAs/AlAs HBV Frequency Tripler," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 843–845, July 2013.

[C] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "High Efficiency and Broad-Band Operation of Monolithically Integrated W-Band HBV Frequency Tripler," *24^{th} International Conference on Indium Phosphide and Related Materials*, pp. 92–94, Santa Barbara, USA, 2012.

[D] A. Malko, A.-Y. Tang, T. Bryllert, J. Vukusic, H. Zhao, and J. Stake, "Thermal Analysis of III-V HBV Diode Structures on InP, GaAs, Silicon and Diamond Substrates," *38^{th} International Conference on Infrared, Millimeter and Terahertz Waves*, Mainz, Germany, 2013.

[E] T. Bryllert, A. Malko, J. Vukusic, and J. Stake, "A 175 GHz HBV Frequency Quintupler With 60 mW Output Power," *IEEE Microwave and Wireless Components Letters*, vol. 22 no. 2, pp. 76–78, February 2012.

Other papers and publications

The following publications are not included in this thesis due to an overlap in the content or the content being beyond the scope of this thesis.

[a] V. Drakinskiy, P. Sobis, H. Zhao, A. Malko, T. Bryllert, and J. Stake, "Status and Progress of Schottky Technology Development for SWI and ISMAR," *submitted to International Symposium on Space Terahertz Technology*, Harvard, USA, 2015

[b] A. Malko, T. Bryllert, J. Vukusic, J. Stake, "Silicon Integrated HBV Frequency Multipliers," *Micor- and Millimetre Wave Technology and Techniques Workshop 2014*, ESA/ESTEC, Noordwijk, Netherlands, 2014.

[c] H. Zhao, A. Malko, Z. Lai, "Effect of Bismuth on InAs Films Grown on GaAs Substrates by MBE," *18th International Conference on Molecular Beam Epitaxy*, Flagstaff, USA, 2014.

[d] A. Malko, T. Bryllert, J. Vukusic, H. Zhao, and J. Stake, "Heterogeneous Integrated HBV-based Frequency Quintupler for 500 GHz," *38th Workshops on Compound Semiconductors Devices and Integrated Circuits*, pp. 11–12, Delphi, Greece, 2014.

[e] A. Malko, T. Bryllert, J. Vukusic, H. Zhao and J. Stake, "Wafer Bonding for Integrated III-V Frequency Multipliers on Silicon," *Conference on Wafer Bonding for Microsystems and Wafer Level Integration*, Stockholm, Sweden, 2013.

[f] J. Stake, H. Zhao, V. Drakinskiy, T. Bryllert, A. Malko, J. Hanning, A.-Y. Tang, P. Sobis, R. Dahlbäck, J. Vukusic, "Integrated Diode Technology for THz Applications", *SPIE Optics+Photonics Conference on Terahertz Emitters, Receivers, and Applications IV*, San Diego, USA, 2013.

[g] A. Malko, T. Bryllert, J. Vukusic, and J. Stake, "Integrated III-V Heterostructure Varactor Frequency Tripler on a Silicon Substrate," *7th European Microwave Integrated Circuits Conference*, pp. 516–519, Amsterdam, Netherlands, 2012.

[h] J. Stake, T. Bryllert, R. Dahlbäck, V. Drakinskiy, J. Hanning, A. Malko, A. Y. Tang, J. Vukusic, H. Zhao, and P. Sobis, "Integrated Terahertz Electronics for Imaging and Sensing," *19th International Conference on Microwaves, Radar and Wireless Communications*, pp. 122–123, Warsaw, Poland, 2012.

[i] A. Malko, J. Liljedahl, T. Bryllert, J. Vukusic, and J. Stake, "Investigation of Passivation Methods for HBV Diodes," *GigaHertz Symposium*, Lund, Sweden, 2010.

[j] J. Stake, T. Bryllert, P. Sobis, A. Y. Tang, H. Zhao, J. Vukusic, A. Malko, V. Drakinskiy, A. Ø. Olsen, and A. Emrich, "Development of Integrated Submillimeter Wave Diodes for Sources and Detectors," *5th European Microwave Integrated Circuits Conference*, pp. 226–229, Paris, France, 2010.

List of abbreviations

AFM	Atomic Force Microscope
AG	Amorphous Glass
AlN	Aluminium Nitride
Au	Gold
BHF	Buffered Hydrofluoric Acid
CH_4	Methane
CMOS	Complementary Metal Oxide Semiconductor
CS	Compliant Substrate
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DC	Direct Current
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GHz	Gigahertz (10^9 Hz)
HBV	Heterostructure Barrier Varactor
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IMPATT	IMPact-ionization Avalanche Transit Time
InP	Indium Phosphide
IF	Intermediate Frequency
IR	Infrared
LO	Local Oscillator
LT	Low Temperature
MBE	Molecular Beam Epitaxy
MEMS	Micro-Electro-Mechanical System
MESFET	Metal Semiconductor Field Effect Transistor
MIC	Monolithic Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal-Organic Chemical Vapour Deposition
Ni	Nickel
Pd	Palladium
PMGI	Polydimethylglutarimide
RF	Radio Frequency

RCA	Standard silicon wet chemical clean
RT	Room Temperature
RTA	Rapid Thermal Annealing
SD	Schottky Diode
SI	Semi-insulating
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
SI	Semi-Insulating
SEM	Scanning Electron Microscope
SOI	Silicon-On-Insulator
STO	Strontium Titanate
TEM	Transmission Electron Microscope
Ti	Titanium
TMIC	Terahertz Monolithic Integrated Circuit
THz	Terahertz (10^{12} Hz)
UV	Ultraviolet
XRD	X-Ray Diffraction

List of notations

A	Device area
b	Barrier width
C_j	Junction capacitance
d	Lattice constant
d_{Si}	Thickness of device layer in silicon-on-insulator
ΔS	Elastance swing
E_d	Electric field in modulation layer
E_g	Energy gap
ϵ_0	Permittivity in vacuum
ϵ_b	Permittivity of the barrier material
ϵ_d	Permittivity of the modulation material
ϵ_r	Permittivity
η	Conversion efficiency
f	Frequency
F	Image force
F_{FS}	Image force in free surface
G	Shear module
$G_{epilayer}$	Shear module in epilayer
G_{oxide}	Shear module in oxide
f_c	Dynamic cut-off frequency
f_p	Pump frequency
k_B	Boltzman constant
κ	Thermal conductivity
L_D	Debye length
L_n	Conversion loss
n	Multiplication factor
N	Number of barriers
N_D	Donor impurity concentration
ω	Angular frequency
P_{AVA}	Available input power
P_{AVA}	Source available power
P_{OUT}	Available output power
P_{RL}	Power reflected
q	Elementary charge

R_s	Series resistance
s	Spacer thickness
S	Differential elastance
T	Temperature
$tan\ \delta$	Loss tangent
w	Depletion width
V_{br}	Breakdown voltage
V_d	Voltage across depleted region

Contents

Chapter 1

Introduction

There is a growing interest in systems operating at terahertz (THz) frequencies (0.3–3 THz) [1]. Extensive work is conducted in the following areas: radio astronomy [2], climate change and atmosphere studies, security [3], short range wireless communication [4], and medicine [5]. Many of these applications rely on signal sources, e.g. Local Oscillators (LOs), that can generate sufficient power to drive high frequency components. Conventional electronic, two terminal LOs are based on: impact-ionization avalanche transit-time (IMPATT) [6], and transferred-electron devices (TEDs) also known as Gunn diodes [7]. In the optical domain Quantum Cascade Lasers (QCLs) [8], optical pumped gas lasers and difference frequency generator sources can be distinguished. In order to deliver sufficient LO power at high frequencies one can use power amplifiers or frequency multipliers, or combination of both. The performance of power amplifiers in GaN transistor technology is particularly worth noticing. These can produce Watts of output power at W-band [9]. A more detailed review of the technology and power amplifier performance can be found in [10]. Frequency multipliers are devices, which generate harmonics of an input signal ($n \times f_p$). These are based on nonlinear components, such as transistors [11,12], Schottky Diodes (SDs) [13] and Heterostructure Barrier Varactors (HBVs) [14]. SD frequency doublers ($2 \times f_p$), triplers ($3 \times f_p$) and quadruplers ($4 \times f_p$) are presented in [15–22]. Fig. 1.1 shows performance of state-of-the-art THz sources. One can notice that, as the frequency of operation reaches THz range, the available power greatly reduces. This part of the electromagnetic spectrum is called the "THz gap".

An alternative method to SD is HBV technology. Invented in 1989, HBV is a semiconductor device, which exhibits symmetric voltage-dependent capacitance [14]. The capacitance modulation in HBV is achieved by placing semiconductor material with high bandgap energy within another semiconductor material with lower bandgap energy. This configuration is referred to as a "barrier". Due to its nonlinear capacitance and anti-symmetric current-voltage, HBV generates only odd harmonics of the input signal (n=3,5,7,...). In addition, unlike SD, HBV does not require external biasing. In summary, a relatively simple device structure, compact and simplified circuit design of higher order frequency multipliers are the main advantages of HBV technology. Recently published works on HBV show that high power and high frequency sources in this technology are possible [Paper E], [33],[Paper A]. It also can be used to drive further high frequency multipliers.

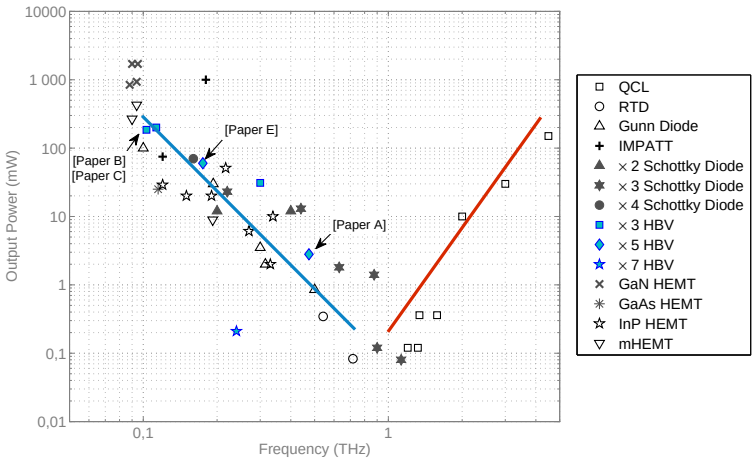


Fig. 1.1: Conventional solid-state THz sources: QCLs [23–25], RTDs [26, 27] Gunn diodes [7, 28], IMPATT diodes [6, 29], Schottky diodes [15–17, 19–22, 30], HBVs [31–33], GaN HEMTs [9, 34, 35], GaAs HEMT [36], metamorphic HEMT [37] and InP HEMT [38–43] power amplifiers.

At THz frequencies, in order to meet the device-circuit matching requirements, the diode and passive components dimensions must be scaled down. Therefore, process technology plays an important role in THz frequency electronics, and relies on high resolution lithographic techniques. It is not only the circuit dimensions that must be scaled with frequency, but also the substrate thickness, which for optimal circuit performance must be thinned to micrometre dimensions.

Common methods for HBV diode-circuit integration include hybrid and monolithic integration circuit (MIC) [44]. The hybrid integration refers to a method in which a discrete diode is flip-chip soldered or wire bonded in a circuit. On the other hand, MIC refers to technology in which diode and circuit are fabricated from the same initial semiconductor material. The MIC approach is preferable over hybrid technology because of high process reproducibility from batch to batch, and reduced parasitics which cause device performance degradation. However, many of the substrates on which MIC approach can be realised have poor thermal conductivity (κ), which limits high power performance of the diode. In addition, GaAs and especially InP are fragile materials, which when thinned to a few micrometres can easily bend or break. Considering the electrical, thermal and mechanical requirements of substrates for microwave circuitry, as well as specific fabrication requirements, a heterogeneous integration is suggested. In this approach combination of III-V compound semiconductors on foreign substrates by epitaxial growth or transfer methods [45] is possible. Using transfer techniques, integrated frequency mixers and multipliers on copper [46], glass [47, 48], AlN [49], diamond [50, 51] were demonstrated. Other possible scenario of heterogeneous integration is combining different active device technologies onto a silicon platform. This can be achieved by epitaxial growth or transfer methods. In contrast to silicon, certain com-

pound semiconductors offer direct bandgap and higher carrier mobility. Advances in III-V epitaxial growth enables growth of complex layer structures (heterostructures) for high performance electronic and photonic components. On the other hand, silicon has high thermal conductivity and it is a robust material with excellent mechanical properties. These properties allow for fabrication of complex waveguide structures, integrated antennas, thin membranes [52–56]. Combining compound semiconductors and silicon allows for new generation of THz electronics.

This thesis focuses on circuit integration methods for high power and high frequency sources based on HBV diodes. The technology development begins with hybrid [Paper E], monolithic microwave integration [Paper C], and novel epitaxial transfer technique onto silicon [Paper B] and silicon-on-insulator [Paper A].

The following structure was used for this thesis: Chapter 2 provides a general description of varactor based frequency multipliers. The basic principle of HBV diode operation is then described. This is followed by a review of to-date presented HBV frequency multipliers, and diode-circuit integration methods.

Chapter 3 contains transmission line theory followed by the description of common substrates for high frequency circuitry. This is continued with an introduction to methods of III-V semiconductor integration onto silicon substrate. The description of low-temperature plasma assisted wafer bonding process and characterisation of epitaxial transferred $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HBV material structure on silicon closes Chapter 3.

Chapter 4 describes fabrication methods for silicon and silicon-on-insulator (SOI) integrated frequency multipliers in HBV technology. This is followed by diode and frequency multiplier characterisation methods. This chapter summaries work on integrated frequency multipliers and places it in the research context. Chapter 5 provides discussion on the conducted research and lists possible future directions.

Chapter 2

Basic principles of HBV frequency multipliers

This chapter begins with basic theory of varactor frequency multipliers. Then, physical and electrical properties of a heterostructure barrier varactor (HBV) are described. This is followed by a review of to-date presented HBV-based frequency multipliers, and discussion on diode-circuit integration approaches.

2.1 Varactor frequency multipliers

A common method to deliver power for devices operating at THz frequencies is to use a frequency multiplier. A frequency multiplier circuit consists of a nonlinear device which transforms an input signal at pump frequency (f_p) into a signal with higher harmonics of f_p ($n \times f_p$) where n is an integer multiplication factor. Traditionally, nonlinear devices, such as transistors or microwave diodes are used for wave distortion.

A microwave diode in a frequency multiplier can operate either in a resistive (varistor) or reactive (varactor) mode [57]. A diode operating in a resistive mode shows a nonlinear resistance, while operational principle of a varactor is based on nonlinear capacitance or inductance. In particular, a forward-biased Schottky diode (SD) shows a strong nonlinear resistance, and a nonlinear capacitance when biased in the backward direction. The shape of the nonlinear capacitance depends on the diode physical properties. These can be either asymmetrical (Fig. 2.1(a)) or symmetrical (Fig. 2.1(b)) with respect to a certain bias point. To the group of varactors with asymmetrical capacitance-voltage characteristic the following belong: p^+-n junction, step-recovery diodes and reverse-biased SDs [58]. Schottky/2-DEG diode [59], back-to-back barrier-n layer-n^+ diode [60], anti-parallel Schottky diode pair with inhomogeneous doping [61] and heterostructure barrier varactor (HBV) [14] are examples of varactors exhibiting symmetrical capacitance-voltage characteristic.

An equivalent circuit of a pure varactor model is shown in Fig. 2.2 [62]. It consists of a variable capacitor connected in series with a resistance (R_s), which summarises resistive losses within the device.

A figure of merit of a frequency multiplier is its dynamic cut-off frequency (f_c), and

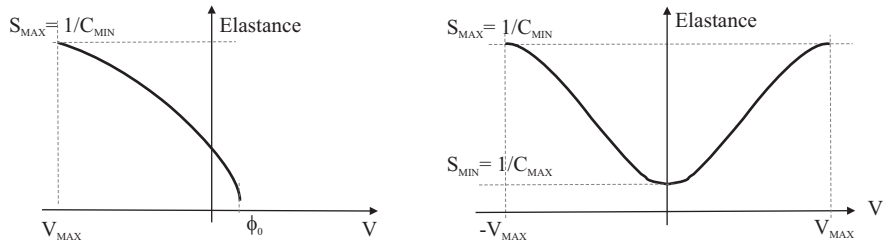


Fig. 2.1: (a) Asymmetrical and (b) symmetrical differential elastance characteristics of varactor.

Fig. 2.2: Equivalent circuit model for a varactor.

it is calculated as

$$f_c = \frac{(S_{max} - S_{min})}{2\pi\ R_s} = \frac{1}{2\pi\ R_s}\left(\frac{1}{C_{min}} - \frac{1}{C_{max}}\right)\ [Hz] \tag{2.1}$$

where S_{min} and S_{max} are minimum and maximum differential elastance respectively, see Fig. 2.1.

The conversion efficiency (η) of a frequency multiplier is a ratio between the output power (P_{OUT}) from the device and the available input power (P_{AVA}) delivered to the device, and is given by

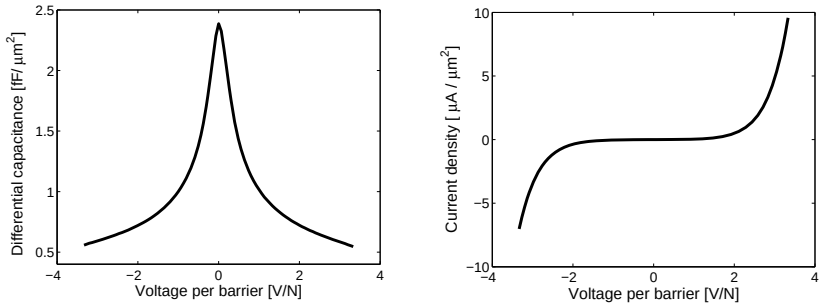
$$\eta = \frac{P_{OUT}}{P_{AVA}}\ [\%] \tag{2.2}$$

In an ideal varactor frequency multiplier the maximum conversion efficiency can reach *100%* [63]. However, in practice this is limited by the device' series resistance (R_s). In contrary the best achievable η in a varistor frequency multipliers is $1/n^2$ [63].

The conversion loss (L_n) is related to a conversion efficiency, expressed in *dB* and is calculated as

$$L_n = P_{AVA} - P_{OUT}\ [dB] \tag{2.3}$$

Improving the performance of a frequency multiplier requires impedance matching, that is presenting optimal embedding impedances for the varactor at different harmonics. This includes harmonics which are not a part of either input or output signal, but are essential for the frequency multiplier performance [57]. These are known as idler harmonics.



(a) (b)

Fig. 2.3: Typical (a) capacitance-voltage and (b) current-voltage characteristics for a HBV diode. The measurements are normalised by unit area and number of barriers (N).

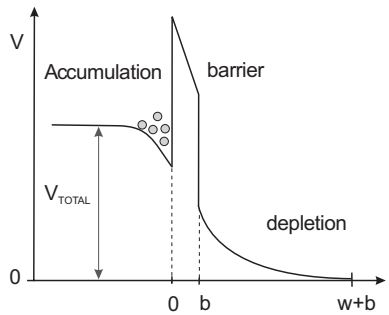


Fig. 2.4: Conduction band of HBV under applied voltage.

2.2 Heterostructure barrier varactors

2.2.1 Basic principle of operation

A heterostructure barrier varactor (HBV) is a semiconductor device. A HBV diode exhibits a nonlinear, symmetrical capacitance-voltage relationship with its maximum at 0 V (Fig. 2.3(a)), and an anti-symmetrical current-voltage (Fig. 2.3(b)). The capacitance modulation in HBV is possible by stacking a material with high bandgap energy within another material with smaller bandgap energy. Under applied voltage the high bandgap acts as a barrier for electrons. This is shown schematically in Fig. 2.4. Increasing the voltage results in increase of the depletion width (w), thereby decreasing the device capacitance respectively. The differential elastance of a HBV diode can be described with following equation:

$$S = \frac{1}{C} = \frac{N}{A}\left(\frac{b}{\epsilon_b} + \frac{s}{\epsilon_d} + \frac{w}{\epsilon_d}\right) \ [1/F] \tag{2.4}$$

where S is elastance, A is the device area, N is the number of barriers, b is the barrier thickness and s is the spacer thickness. ϵ_b and ϵ_d are the dielectric constants of the

barrier and modulation material respectively. The voltage dependent depletion layer width is calculated as

$$w = \sqrt{\frac{2\epsilon_d |V_d|}{qN_D}} \ [m] \tag{2.5}$$

where V_d is the voltage across the depleted region in each of the modulation layers, N_D is the doping concentration in modulation layer, and q is the elementary charge. Equation 2.5 is valid when $V_{br} > V_d > 0$ V. For V_d=0 V condition the minimum elastance is expressed by

$$S_{min} = \frac{1}{C_{max}} = \frac{N}{A}\left(\frac{b}{\epsilon_b} + \frac{2s}{\epsilon_d} + \frac{2L_D}{\epsilon_d}\right) \ [1/F] \tag{2.6}$$

where L_D is the Debye length given by

$$L_D = \sqrt{\frac{\epsilon_d k_B T}{q^2 N_D}} \ [m] \tag{2.7}$$

where k_B is the Boltzmann constant and T is temperature. The maximum elastance S_{max} is limited by

$$S_{max} = \frac{1}{C_{min}} = \frac{N}{A}\left(\frac{b}{\epsilon_b} + \frac{s}{\epsilon_d} + \frac{w_{max}}{\epsilon_d}\right) \ [1/F] \tag{2.8}$$

where w_{max} is the maximum extension of depletion width. The maximum depletion width is determined by one of the following conditions:

- modulation layer punch-through, when w_{max} equals to the modulation layer thickness m;
- large conduction current across the barrier due to the thermionic emission at high electric fields;
- large conduction current due to the impact ionisation at high electric field, calculated as

$$w_{max} = \frac{\epsilon_d E_{d,max}}{qN_D} = \sqrt{\frac{2\epsilon_d V_{br}}{qN_D}} \ [m] \tag{2.9}$$

where $E_{d,max}$ is the maximum electric field, and V_{br} is the breakdown voltage in the modulation layer. V_{br} for an abrupt pn-junction is given by [64]

$$V_{br} = 60\left(\frac{E_g}{1.1eV}\right)^{3/2}\left(\frac{N_D}{10^{16}cm^{-3}}\right)^{-3/4} \ [V] \tag{2.10}$$

where E_g is the barrier height of the semiconductor in modulation layer at 300 K.

- or, due to current saturation [65, 66], and is then estimated as [67]

$$w_{max} = \frac{\nu_{max}}{8f_p} \ [m] \tag{2.11}$$

where ν_{max} is saturated electron velocity and f_p is the pump frequency.

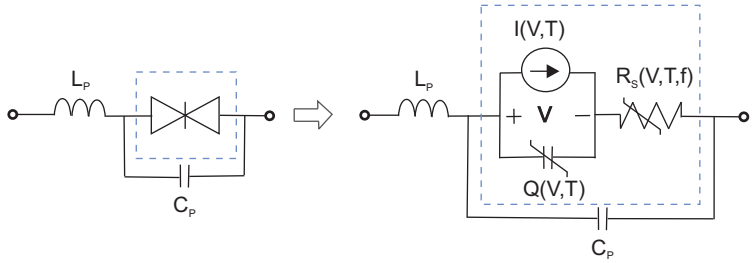


Fig. 2.5: Quasi-static equivalent circuit model of HBV.

2.2.2 HBV model

An extended quasi-static equivalent circuit of HBV is shown in Fig. 2.5. It consists of a current source, which models the device leakage current that is dependent on temperature and frequency [68].

As already mentioned, R_s is a sum of resistive losses within a device. In a HBV diode the main impact on R_S comes from resistance of the ohmic contact area R_c, resistance in the active layer R_{active}, resistance of the contact layer $R_{contact}$, and the spreading resistance in the buffer layer R_{spread}. R_S is given by

$$R_s(V,T,f) = R_c + R_{active}(V,T) + R_{contact}(V,T) + R_{spread}(T,f)\ [\Omega] \tag{2.12}$$

In frequency multipliers R_S affects η, as it dissipates power at every frequency for which current may flow through the diode [57, 69]. Moreover, the R_S will increase with frequency due to the skin effect [70, 71].

With only a temperature dependence of R_{active}, $R_{contact}$, and R_{spread}, as a rule of thumb R_S can be approximated as [72]

$$R_s(T) = R_{s,T_0}\left(\frac{1}{4} + \frac{3}{4}\frac{T}{T_0}\right)\ (\Omega) \tag{2.13}$$

where R_{s,T_0} is the parasitic series resistance at T_0, and T is the elevated junction temperature at dissipated power (P_{DISS}), and assuming P_{DISS} is equal to P_{IN}, the junction temperature can be estimated as [Paper A]

$$T = T_0 + P_{IN}R_{th}\ (K) \tag{2.14}$$

where R_{th} is thermal resistance. For a planar HBV the main contribution to R_{th} is in the mesa region and substrate-buffer contact region [72, 73],[Paper D].

L_P models parasitic connections to the diode (i.e. wire bonding, air-bridges), while C_P represents parasitic capacitance due to packaging.

2.2.3 III-V material systems

The HBV material structure is grown with molecular beam epitaxy (MBE) on semi-insulating (SI) or highly doped substrates. A typical layer structure of a HBV diode is shown in Table 2.1. The highly doped buffer (*layer 1*) and contact materials (*layer*

7) are optimised for low resistive losses. Moderately doped *layer 2* and *layer 6* allow for capacitance modulation. These regions are also optimised for minimum resistivity and maximum breakdown voltage. The undoped region *layer 4* creates a barrier for electrons, and prevents their transport from *layer 6* to *layer 2*. A material with high bandgap energy is preferable, since it minimises the thermionic emission and carrier tunneling through the barrier [74]. *Layer 3* and *layer 5* act as spacers, preventing diffusion of dopants to the barrier.

Because of material symmetry, by repeated growth of *layer 3–layer 6* several barriers can be stacked on top of each other. This is done to increase the device power handling capability. However, the number of barriers (N) is limited by the semiconductor's thermal conductivity [72, 75]. Various material systems have been presented to improve the device electrical and power performance.

Table 2.1: Typical HBV material layer structure.

Layer No.	Comment	Type
7	Contact	n^{++}
6	Modulation (m)	n
5	Spacer (s)	i
4	Barrier (b)	i
3	Spacer (s)	i
2	Modulation (m)	n
1	Buffer (*buff*)	n^{++}
0	Substrate	SI or n^{++}

• **GaAs/AlGaAs**

The very first HBV structure was grown on GaAs substrates [14, 76], with undoped GaAs/ $Al_{0.7}Ga_{0.3}As$/ GaAs barrier region. A small potential barrier height in the modulation layer results in high leakage current, thus degrading the device performance.

• **$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$**

Today, most of the HBV strucutres are grown with $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ on InP substrates. The barrier consists of an undoped $In_{0.52}Al_{0.48}As/AlAs/In_{0.52}Al_{0.48}As$ region [77]. The material stack for $In_{0.53}Ga_{0.47}As$ HBV devices is shown in Fig. 2.6. The interest in $In_{0.53}Ga_{0.47}As$ for HBV diodes is motivated by higher than in GaAs electron mobility. However, because of poor thermal conductivity of $In_{0.53}Ga_{0.47}As$ (κ=4.8 $Wm^{-1}K^{-1}$) HBV diodes suffer from poor heat dissipation, which limits the allowed number of barriers per mesa, and overall device performance at high input power levels [73]. Nevertheless, state-of-the art HBV frequency multipliers have been presented with this material structure [33, 78, 79], [Paper C].

Metamorphic growth of $In_{1-x}Ga_xAs$ on GaAs could substitute HBV devices on InP substrates, which are costly and available in small wafer sizes.

• **$Al_{1-x}Ga_xN/GaN$**

Studies with GaN materials for HBV devices have been proposed and carried out [80,81]. The GaN is characterised by a large energy bandgap (E_g=3.2 eV) and high electron sat-

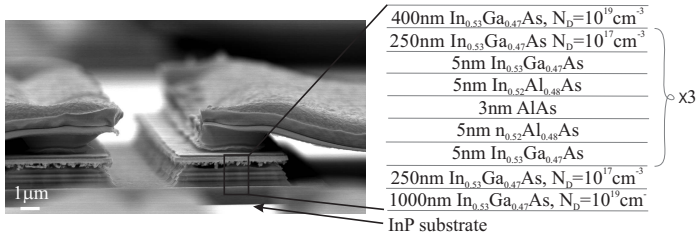


Fig. 2.6: SEM image of an InP-based HBV diode with depicted material strucutre.

uration velocity (25×10^6 cm/s). However, due to spontaneous polarization and stress induced piezoelectric field in AlGaN and GaN, an asymmetrical capacitance-voltage characteristic was obtained [80].

• **InAs/AlSb**

Besides the common III-V semiconductors, AlSb grown on InAs buffer layer has also been proposed for HBV diodes [82, 83]. Although InAs has a narrow bandgap, its main advantage is electron mobility which is almost 33,000 $\mathrm{cm^2V^{-1}s^{-1}}$. However, the alloys containing Sb are sensitive to water and air, making the device fabrication challenging. In addition to that, InAs substrates are rather expensive, thus a common method is growth on substrates like i.e. GaAs. Large lattice mismatch between AlSb and GaAs of almost 8% limits growth of high quality and dislocation free material.

2.3 HBV frequency multipliers

Unlike a Schottky diode the HBV frequency multipliers generate only odd-harmonics of the input signal. Hence, the number of required idler circuits that need to be considered for design of high order harmonics frequency multiplier is reduced. For example, no idler circuits are required to design a HBV frequency tripler ($3\times f_p$), and only one idler circuit at $3\times f_p$ for a frequency quintupler ($5\times f_p$) must be taken into account. The number of required idler circuits is in contrast with an abrupt-junction diode, a frequency tripler and quadrupler will require one idler at $2\times f_p$, while a quintupler will require two idler circuits at $2\times f_p$ and $4\times f_p$ [57].

Due to anti-symmetrical current-voltage of HBV, the frequency multipliers circuits do not require an external bias. This greatly simplifies the circuit design and makes it more compact.

Table 2.2 summarises HBV frequency multipliers reported so far in various technologies and their performance. We distinguish two types of diode-circuit integration methods, i.e. hybrid and integrated circuits.

• **Hybrid**

The hybrid technology refers to the process in which a discrete diode and circuit are fabricated in separate processes and on different substrates. A diode is flip chip soldered or wire-bonded into the circuit [20, 85, 92], [Paper E]. The main advantage of this process is its low cost. However, reduced component dimensions at THz frequencies reduce

Table 2.2: Performance of HBV based frequency multipliers.

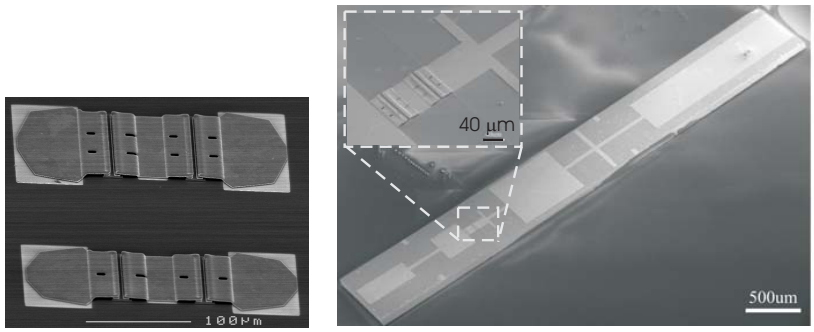
f_{out} [GHz]	P_{OUT} [mW]	η [%]	3-dB BW [%]	Factor	Technology	Ref.
97	85	20		×3	MMIC InP	[84]
100	1	4.9	1.4	×5	hybrid, Quartz	[85]
102	32	21		×3	hybrid, quartz	[86]
107	185	23	15	×3	MMIC InP	[Paper C]
107	185	23	15	×3	heterogeneous, Si	[Paper B]
112	15	5	17	×3	hybrid AlN	[87]
113	195	15	1.5	×3	hybrid, AlN	[32]
175	60	6.3	4.5	×5	hybrid, AlN	[Paper E]
221	7.1	7.9		×3	heterogeneous, Cu	[46]
240	0.21	0.25		×7	MMIC, InP,	[31]
248	8	0.95		×3	quasi-optical, InP	[88]
282	31	7		×3	MMIC, InP	[33]
288	6	6	15	×3	heterogeneous, Quartz	[89]
290	9.5	8	8.6	×3	hybrid, AlN	[90]
450	1	1.45		×3	hybrid, GaAs	[91]
474	2.8	0.75	4	×5	heterogeneous, Si	[Paper A]

the assembly tolerances and repeatability in the device performance [44]. In addition, soldering introduces additional parasitics which must be taken into account during the design.

• **Integrated**

To eliminate the uncertainity associated with wire bonding and soldering techniques, a more convenient method is to integrate the active components within the circuit [44]. Since all passive and active components are fabricated on one substrate, this technology is more reliable and repeatable than hybrid, and is favourable for high frequency applications [11, 33, 37, 38, 93, 94],[Paper C]. Two types of integrated circuit approaches can be distinguished: monolithic integrated circuits (MICs) (i.e. monolithic microwave integrated circuit (MMIC) [44]) and heterogeneous integration. The MMICs are usually realised on high permittivity substrates (e.g. semi-insulating GaAs) with transmission line components for impedance matching. A special case of MMIC is membrane technology [95]. In this method a few micrometres thick and GaAs membrane grown in between thin etch-stop AlGaAs layers on GaAs substrate [95]. The fabrication of diode and passive circuit elements is followed by the substrate removal by standard lapping and etching techniques. The etch selectivity towards GaAs assures that the etch process will stop when AlGaAs layer is reached. This method is dominant for Schottky diode high frequency multipliers and frequency mixers [95–99].

In the heterogenous integration approach an epitaxial layer for active device is grown or transferred onto a non-native substrate which usually has beneficial properties [22, 61, 100], [Paper B], [Paper A]. It gives an additional degree of freedom in device and circuit design, and choice of fabrication techniques, where the overall aim is improved performance, increased functionality and/or reduced cost. A detailed description of het-



(a) (b)

Fig. 2.7: Example of (a) discrete HBV diodes and (b) monolithic integrated circuit [Paper C].

erogeneous integration methods of compound semiconductors onto silicon substrate are given in Chapter 3.

Chapter 3

Heterogeneous integration - III-Vs on silicon

Millimetre- and submillimetre wave circuits can be fabricated either as hybrid circuits, where individual devices are assembled on a host substrate, or as monolithic integrated circuits (MICs). Because of the short wavelength (λ) at high frequencies, the component dimensions must be scaled down. Therefore, the most convenient way is to monolithically integrate a diode and circuit. MIC technology is restricted to substrate materials on which high quality compound semiconductors can be grown. These substrates are often characterised by high dielectric constant and low thermal conductivity, i.e. InP and GaAs. And some of these substrate materials are also fragile, and when thinned to a few micrometres these can bend or break easily. Therefore other materials with superior mechanical and thermal properties must be considered, e.g. silicon.

A method which enables integration of compound semiconductors onto foreign substrates is known as heterogeneous integration [45]. To-date, the heterogeneous integration is mainly associated with photonic devices on a silicon platform, however this method is applicable for silicon integrated high frequency electronic components as well.

This chapter begins with a short introduction to transmission line concept, followed by a review of substrate materials for high frequency applications. It is followed by the description of heterogeneous integration methods of compound semiconductors onto silicon. Then a description of low temperature plasma assisted wafer bonding, which was specifically employed to transfer $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HBV material onto silicon carrier is given. The transferred material was studied with methods like: atomic force microscopy (AFM), transmission electron microscopy (TEM) and X-ray diffraction (XRD). The results are presented in section 3.3.1.

3.1 Transmission lines and substrates for mm-wave and THz applications

The transmission lines are used to guide electromagnetic waves in the circuit [101]. Example of transmission lines used in high frequency circuit design are: microstrip (MS), coplanar waveguide (CPW), and suspended-substrate stripline (SSSL). Schematic

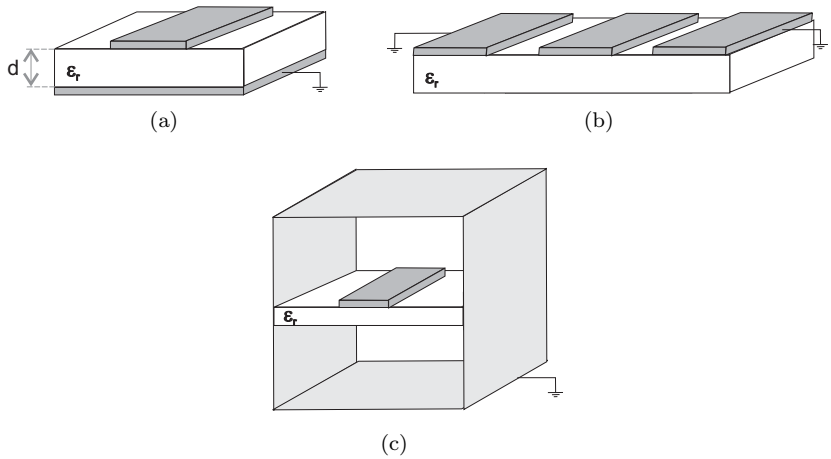


Fig. 3.1: Transmission line structures: (a) microstrip, (b) coplanar waveguide, and (c) suspended-substrate stripline.

drawings of these line concepts are shown in Fig. 3.1.

Microstrip (MS), which propagates quasi-TEM modes, is suitable for both hybrid and monolithically integrated circuits [102]. In the MS configuration a microstrip line is separated from the ground plane with a dielectric material, see Fig. 3.1(a). In traditional microstrip technology the ground connections are realised in the via-hole technology. At high frequencies the moding effect must be considered. The surface waves in microstrip are excited above certain cut-off frequency [103]

$$f_c = \frac{75}{d\sqrt{\epsilon_r - 1}} \; [GHz] \tag{3.1}$$

From eq. 3.1 one can notice that, a high dielectric substrate must be thinned down to micrometre levels if designed at high frequencies to avoid multiple modes in the waveguide. However, losses in thin substrates are higher. Additionally, very thin substrate are not easy to handle.

Unlike in microstrip, the ground connections for CPW are made on the substrate surface [102], which can shorten the electrical length of the ground connections. Thus CPW performance is less dependent on the substrate thickness. The main concern of CPW technology are dispersion and radiation losses, as well as losses on rough conductor edges.

The suspended-substrate stripline (SSSL), which also refers to circuit on a membrane, is a common choice for design of high impedance lines. The main advantages of SSSL topology are its TEM nature and effective permittivity which is close to 1.0 [102]. However, these lines require small feature dimensions, which are not easily obtained with standard photolithography techniques. In addition, unlike in microstrip, the heat-sinking is not located under the substrate, therefore thermal management for SSSL circuit must be carefully considered.

Taking all of these requirements into account, a preferable substrate for high frequency transmission lines should have: low loss tangent (tan δ), low and isotropic

Table 3.1: Parameters of commonly used substrate materials [101, 102, 104–109] at 300 K.

	ϵ_r	tan δ 10^{-4}	κ [Wcm^{-1}K^{-1}]	CTE[1] 10^{-6} [°C^{-1}]
C [2]	5.7	0.6	600	0.8
Si	11.7	40 [3]	156	2.6
SiC	9.66	80 [4]	360	–
AlN	8.5	6	175	4.15
GaAs	12.9	60	55	5.7
InP	12.6	10	68	4.6
SiO_2 [5]	3.78	1	10	0.55
Al_2O_3 [6]	9.0	3	30	–
Al_2O_3 [7]	8.6–10.5	0.4	33	5.6

permittivity (ϵ_r), high resistivity (ρ), and preferably high thermal conductivity (κ). Table 3.1 provides a summary of electrical and physical attributes of some commonly used substrate materials and is followed by a short description of these materials.

• **Diamond**

Commercially available diamond substrates are prepared by chemical vapour deposition (CVD). Main advantage of CVD diamond is its low loss tangent and high thermal conductivity, which makes it a great candidate for high frequency and high power applications [51, 107, 110]. However, substrates of CVD diamond are only available in small die sizes, are expensive and difficult to machine.

• **Silicon**

Silicon has thermal conductivity twice as high as that of InP and GaAs, which is beneficial for high power diode operation [Paper D]. The mechanical properties of silicon, and technology advancement for this material, allows for fabrication of thin membranes, waveguide integrated antennas and complex waveguide shapes for high frequency applications [22, 52, 55, 111–114]. However, bulk silicon has high loss tangent, therefor it is more convenient as substrate for low frequency devices. For high frequency applications a high resistivity (HR) silicon is used. Electrical properties of HR silicon are closer to semi-insulating InP and GaAs. However, charge accumulation at the Si/SiO_2 interface causes enhanced surface conductivity which contributes to an increased microwave loss in HR silicon [115]. In order to reduce this loss methods like surface passivation [116] and surface damage by high dose implantation [117] have been suggested.

[1] Coefficient of Thermal Expansion (CTE).
[2] Data are given for CVD diamond.
[3] At 10 GHz.
[4] At 80 GHz.
[5] Refers to fused silica.
[6] Refers to alumina, ceramic form of sapphire.
[7] Sapphire.

• Aluminium Nitride and Silicon Carbide

Aluminium nitride (AlN) and silicon carbide (SiC) are wide-bandgap and robust materials. Due to their excellent thermal properties, they serve as host substrates for high power GaN HEMTs [118, 119] and other millimetre-wave applications [87], [Paper E]. Because of the high loss tangent of SiC, it is more attractive for applications operating at low frequencies.

• Indium Phosphide and Gallium Arsenide

Semi-insulating (SI) InP and GaAs substrates are broadly used in the mm-wave and THz applications. These are characterised by low loss tangent and high electrical resistivity. Moreover, the epitaxial growth methods allow for growth of high quality structures on these substrates. However, these materials have poor thermal conductivity which limits device performance at high input power levels [72].

• Fused silica

Low loss tangent and low permittivity of fused silica makes this material very attractive for high frequency circuits [92, 120]. Unfortunately, fused silica has very low thermal conductivity, and it is also a brittle material what makes fabrication processes difficult.

• Alumina and sapphire

Alumina and crystalline sapphire have very similar electrical parameters. Both are also robust, temperature stable and are characterised by good thermal conductivity. Unlike sapphire, alumina is less expensive, hence more common for microwave circuits.

Among all of the presented substrates, silicon is the most studied and most established material in the microelectronic industry, which has seen continued and steady growth over the past 50 years [121]. Additionally, electronic and mechanical properties of silicon represent a compromise among the above listed materials.

3.2 Heterogeneous integration methods

In this work the heterogeneous integration refers to growth and epitaxial transfer methods of compound semiconductors onto silicon substrate. Both of these approaches have their advantages and limitations, which are addressed below.

3.2.1 Epitaxial growth

Main limitations of the direct growth of compound semiconductors on silicon substrate are lattice mismatch, difference in the Coefficient of Thermal Expansion (CTE), and material polarity.

The lattice mismatch between the substrate and epitaxial layer will define the critical thickness of the epilayer. For material systems in which the lattice mismatch is below 2%, this critical thickness is relatively high, consequently, the defect density in these films is approximately 10^5 cm^{-2}. For material systems like GaAs—Si and InP—Si in which the lattice mismatch is of 3.3% and 8% respectively, the critical thickness is much lower, making density of dislocations in thick films higher, which will result in degrada-

tion of electrical and optical properties.

Additionally, GaAs and InP are polar semiconductors, while Si is a non-polar material. The difference in the polarity will lead to creation of antiphase boundaries, and consequently the final epilayer may behave like a highly compensated semiconductor. A detailed discussion of antiphase domain and techniques of their suppression can be found in [122].

Typical MBE and MOCVD growth temperatures of compound semiconductors are in the range of 400–600 °C and 800–1000 °C respectively. At these temperature levels the substrate and epilayer maintain their own lattice constants. However, when the wafer is cooled down to room temperature (RT), both materials will follow their lattice constants, which will introduce additional strain in the film. This results in wafer bending or epilayer cracking.

Because of these limitations, a number of growth techniques has been developed and presented in order to reduce the density of misfit and treading dislocations, and to overcome the CTE mismatch. These methods are described below.

• Compliant substrate

When a substrate thickness is in the range of tens or few hundreds of *nm*, the strain relaxation caused by misfit or treading dislocations will be accommodated in a thin substrate rather than in a thick film. This is why the critical thickness of the epitaxial layer can be significantly increased [123]. Handling of very thin substrates is difficult, therefore, it is convenient to prepare a compliant substrate (CS) on a mechanical host substrate. CS can be in a form of a thin membrane or a suspended disk on a narrow pillar [123, 124]. The dimensions of a membrane or disk are limited, therefore a more convenient solution is to use silicon-on-insulator (SOI) substrate with a thin device layer as a CS. It was shown that the generated dislocations will migrate to the underlying Si/oxide interface, further relaxing the misfit strain [125].

Epitaxially grown amorphous oxides can also serve as buffer layers. This method was first presented in [126], where $SrTiO_3$ (STO) and $BaTiO_3$ (BTO) were used. It was shown that amorphous buffer reduces mechanical strain and thermal mismatch in the epilayer. Using this method GaAs MESFETs on Si were presented [127].

• Metamorphic buffer

Nucleation and propagation of antiphase boundaries and treading dislocations can be minimised by introducing a metamorphic buffer layer. Over the years various metamorphic growth approaches on silicon have been suggested. One of them is to grow a buffer layer with sequenced growth temperatures (low/high) [128]. Under such growth conditions the dislocations can be greatly suppressed, and good quality active device layer can be obtained.

Other applications that have been presented on metamorphic buffer are InSb transistors for low power applications accommodated on a GaAs/InAlSb buffer layer [129], and on GaSb/GaP buffer [130]. A disadvantage of this method is a thick buffer layer, which contributes in poor heat dissipation and degrades the device performance.

Another possible method is to use germanium (Ge) as a buffer for GaAs-based devices. Ge and GaAs are lattice matched materials. An example of Ge as a buffer can be found in [131]. In this work a $Si_{1-x}Ge_x$ was grown on silicon substrate, with gradually graded Ge composition, which enables growth of dislocation free GaAs film.

• Pattern substrate growth

The quality of heterogeneous grown III-Vs on silicon can be improved if the growth area is reduced to a few μm^2 or a couple of *nm*. This type of growth is known as a pattern substrate or selective area epitaxy. The reduction of the growth area is obtained by creating a pattern (either trenches or openings) in SiO_2 or SiN [132, 133]. An extensive discussion on the zero deposition on SiO_2 mask can be found in [134]. Alternatively III-V material structure can be grown on Ge template masked with SiO_2 trenches [135].

3.2.2 Epitaxial transfer

An alternative method to epitaxial growth is epitaxial transfer, which is based on wafer bonding technology. In contrast to epitaxial growth, wafer bonding is not limited by materials lattice parameters, CTE or crystal structures. The epitaxial transfer enables combination of almost all materials. To obtain good quality bonding the surfaces of the joined wafers must have micro roughness (rms) below 1 nm [136] and be free of contaminations. Any surface contamination, i.e. dust, hydrocarbons or metal ions, may cause creation of voids (an area where the bonding process did not occur). For example, a particle of a 1 μm diameter on a $4''$ substrate will lead to a void with a diameter of 1 cm [137], which is why proper wafers cleaning is essential.

The process of wafer bonding is of great interest for micromechanics, microelectronics and optoelectronics. Depending on application and properties of the combined materials different bonding techniques can be utilised. Generally speaking, the wafer bonding can be split into direct and indirect techniques. Table 3.2 summarises commonly used methods for semiconductor wafer bonding technology, which are briefly described below.

Table 3.2: Commonly used wafer bonding techniques in semiconductor technology [45, 136, 138–140]

Technique		**Remarks**
Direct	Anodic	Ionic bonding; high electric fields
	Direct	Surface roughness <1 nm; thermal anneling
	Plasma assisted	Low temperature; Oxygen or fluorine plasma. Suitable for thermally mismatched materials.
Indirect	Adhesive	Thin (μm) adhesive layer (polymer, spin-on glass).
	Eutectic	Metal alloys for soldering.

• Indirect wafer bonding

In the indirect method a thin layer of adhesive or metal (eutectic bonding) is used as a bonding agent [141]. In the adhesive approach one or both surfaces are coated with a polymer before bringing wafers into contact. Depending on the adhesive, to solidify the structure it must be treated with temperature or ultraviolet light. In the eutectic bonding one of the wafers is usually covered with a thin layer of metal i.e. gold,

aluminium or chromium. The system is then heated beyond the metal's eutectic point causing diffusion of silicon into the metal.

The indirect wafer bonding technology has been successfully applied to silicon integrated SDs [22, 48, 142], HBVs [46, 47], transistors [143–145], lasers and solar cells [146, 147].

• **Direct wafer bonding**

In contrast to the indirect wafer bonding, the direct wafer bonding technique does not require an intermediate material between the joined wafers, hence good thermal conductivity between materials can be obtained compared with polymer bonding. Clean and contamination free wafers bond spontaneously, however the bonding energy will have to be further increased in order to obtain stable bond. Bonding energy is improved by applying external force or by annealing the bonded pair at high temperatures. However, if the thermal expansion coefficient mismatch is taken into consideration or if high temperatures can change the material or structure properties, then a low temperature (LT) procedure is preferable [148]. A low temperature wafer bonding refers to bonding at temperatures below 400 °C. Prior to the bonding the joined surfaces are treated with oxygen plasma. Oxygen plasma effectively removes hydrocarbon and water related species [138]. Plasma activation allows for spontaneous wafer bonding, and it was shown that the strength of the bonding is comparable to thermally treated wafers, and it is strongly dependent on the plasma discharge energies [138]. If wafers with large areas are bonded, then silicon wafer can be patterned with outgassing channels, which will effectively remove trapped air, reducing probability of voids [149]. In the applications which require oxide free interfaces fluorine or argon plasma can be used [150]. The direct wafer technology was applied to silicon integration of photonic and electronic devices [151].

The direct wafer bonding can also be obtained due to the ion migration under high electric field (anodic bonding) applied to the bonded pair. However, this method is restrained to bonding of sodium containing glass with semiconductor materials of similar thermal expansion.

• **Epitaxial lift-off**

After the wafer bonding in order to expose the transferred material the donor wafer is removed by lapping and/or etching. Removal of the donor wafer adds to the total cost of epitaxial transfer technology, making this process costly. In order to save on the donor wafer methods such as mechanical splitting [152], ion-cuting [153–156] (SmartCut^{TM}), and undercutting by selective chemical etching also known as epitaxial lift-off (ELO) [157] have been proposed.

Prior to the ELO process, the epitaxial structure is grown on a sacrificial buffer layer. This buffer layer is then selectively wet etched releasing the epitaxial film from the donor substrate [157, 158]. A thick photoresist or wax is used to protect the front side of the film. When the sacrificial buffer is completely removed and epilayer is released from the donor substrate, the epitaxial film is placed on a desired substrate. The created hydrogen bonds hold the two pieces together [159, 160]. Because the epitaxial film is lifted-off, the donor substrate stays intact and can be reused for another epitaxial growth, making the process less expensive [161]. Transistors [162, 163], photodiodes [164] and solar cells [165] on different substrates have been demonstrated using ELO method.

3.3 Experimental procedure

For the purpose of this work the HBV material structure is transferred on silicon substrate in a process of low temperature plasma assisted wafer bonding.

Prior to the wafer bonding the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ based HBV material structure is grown by molecular beam epitaxy (MBE) on a lattice matched InP substrate in reverse order to the one shown in Fig. 2.6 and as described in section 2.2.3. By doing so, after the epitaxial transfer the 400 nm thick $In_{0.53}Ga_{0.47}As$ contact layer will be on top of the transferred material, enabling further diode fabrication.

The wafer bonding process steps are depicted in Fig. 3.2. The epitaxial transfer procedure begins with silicon wafer cleaning in the standard cleaning solution (RCA) for removal of organic contaminates. Subsequently, silicon native oxide is etched in HF solution. The native oxide removal step is usually performed just before silicon wafer treatment with plasma. Unless visible surface contamination, InP wafer is not cleaned.

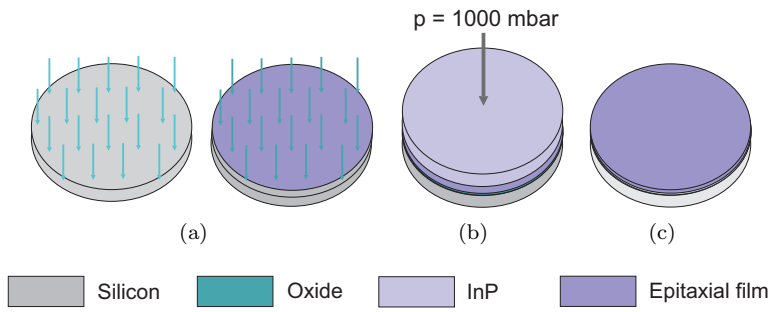


Fig. 3.2: Process flow for epitaxial transfer: (a) O_2 plasma surface treatment, (b) wafer bonding and storage at room temperature and under applied pressure, (c) wet etch removal of InP substrate revealing transferred material.

In the next process step, InP substrate with the epitaxial material and silicon wafer are oxidised. Bombardment with oxygen ions causes breaking of surface bonds, which results in cleaning of the surface from hydrocarbon and water related species. The oxygen plasma treatment also creates free bonds (dangling bonds) which are essential to obtain direct wafer bonding. Prior to the wafer plasma treatment, the chamber is cleaned for 20 min in oxygen atmosphere. Since the available plasma system is not equipped with an in-situ wafer bonding extension, the wafers are oxidised separately and pre-bonded in the ambient air. Before pre-bonding, silicon wafer is dipped in DI water and subsequently blow dried with N_2. Then the wafers are joined with the oxidised surfaces, and the bonded pair is transferred to the wafer bonder. The storage in the wafer bonder under an applied pressure and at specific temperature gradually increases the bonding strength and eventually covalent bonds are created [136].

In the last step of the process the InP substrate is wet etched in $HCl:H_2O$. The selectivity of the etching solution assures that the etching will stop when $In_{0.53}Ga_{0.47}As$ layer is reached.

3.3.1 Material characterisation

Methods like infrared (IR) inspection, transmission electron microscopy (TEM), atomic force microscopy (AFM) and X-ray diffraction (XRD) were introduced to characterise the quality of the epitaxially transferred material. The results of these characterisations are presented below.

• Infrared inspection

The very first procedure after completing the process of wafer bonding is verification of the bond quality. If one of the wafers is transparent to the visible light, i.e. glass, quartz or GaN, then the voids can be easily detected. However, for the bonded pair with wafers that are not transparent to the visible light i.e.: Si/Si, Si/InP or Si/GaAs, an optical transmission method has to be applied. In this method a light source, usually infrared lamp, is placed under the structure, and an IR camera is employed to detect the transmitted wavelength. The voids, areas where the bonding did not occure, will be visible as darker regions. An example of Si/InP structure is shown in Fig. 3.3. The diameter of InP is 3 ″. The revealed void area is 15 mm in diameter.

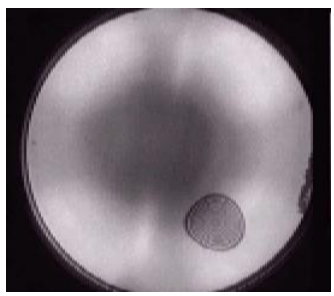


Fig. 3.3: Infrared inspection image of the wafer pair obtained after bonding. InP wafer is 3 ″ size. The dark area indicates unbonded area (void) with the diameter of 15 mm.

• Transmission electron microscopy

In the transmission electron microscopy (TEM) forward scattered electrons are used to study the material grain boundaries and to observe its lattice defects. We have applied this method to study the bonding interface, and to inspect the quality of the $In_{0.53}Ga_{0.47}As$ surface after wet etch removal of InP substrate. The cross-section of HBV material on silicon substrate is shown in Fig. 3.4. The insets show studied areas of (*top*) $In_{0.52}Ga_{0.48}As$/ InAlAs/ AlAs structure and (*bottom*) $In_{0.53}Ga_{0.47}As$/Si interface with 5 nm thick oxide layer.

• Atomic force microscopy

The surface morphology after wet-etch removal of InP substrate was studied with atomic force microscopy (AFM). An example of AFM scan after completed epitaxial transfer is shown in Fig. 3.5. The roughness of epitaxially grown material on lattice matched substrate is usually below 1 nm, while the obtained roughness on this sample is 18 Å. The increased surface roughness might be related to $HCl{:}H_2O$ etching solution, which also etches $In_{0.53}Ga_{0.47}As$ but with much smaller etch rate compared to etch rate of InP.

• X-ray diffraction

X-ray diffraction (XRD) is a non-destructive characterisation method which allows to study structural chemical composition, crystal structure, crystallite size, strain, preferred orientation and layer thickness. Although this method is mainly used for epitaxially grown materials, we have applied it to verify the presence of transferred $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ film on silicon substrate. To do that a ω rocking curve and ω-2Θ 2D scans were taken. All scans were taken with (004) silicon peak as a reference peak. The 2D scan was taken in the range of 8.5°and 4°for 2Θ and ω respectively. A SOI wafer with 300 μm thick silicon handle and 20 μm thick device layer was measured for a reference.

The results of ω rocking curve scan are shown in Fig. 3.6, where blue line corresponds to SOI substrate while red line is for the SOI substrate with epitaxial material. Besides two peaks corresponding to SOI substrate, a clear peak for $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ film was detected. The results for 2D scan are presented in Fig. 3.7.

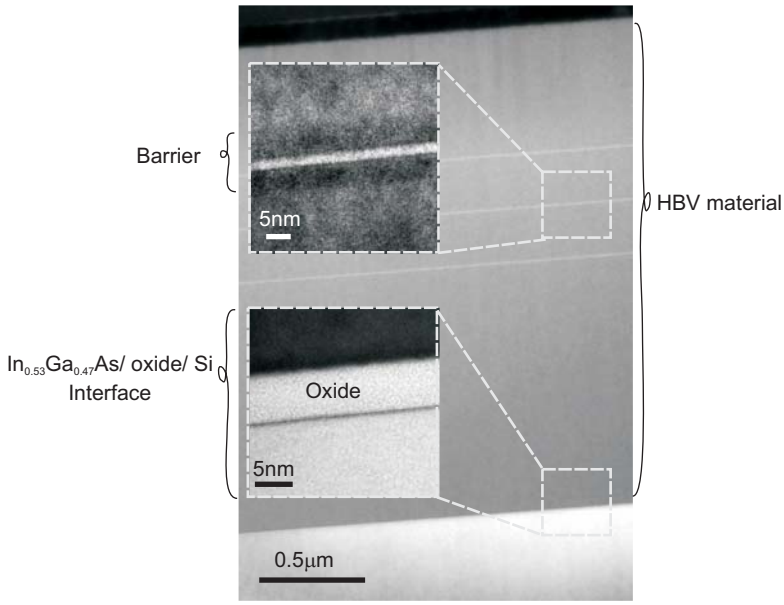


Fig. 3.4: Transmission electron microscopy image of epitaxally transferred HBV material structure onto silicon substrate. The insets show (*top*) $In_{0.52}Ga_{0.48}As$/ InAlAs/ AlAs structure, and (*bottom*) bonding interface with 5 nm thick oxide layer.

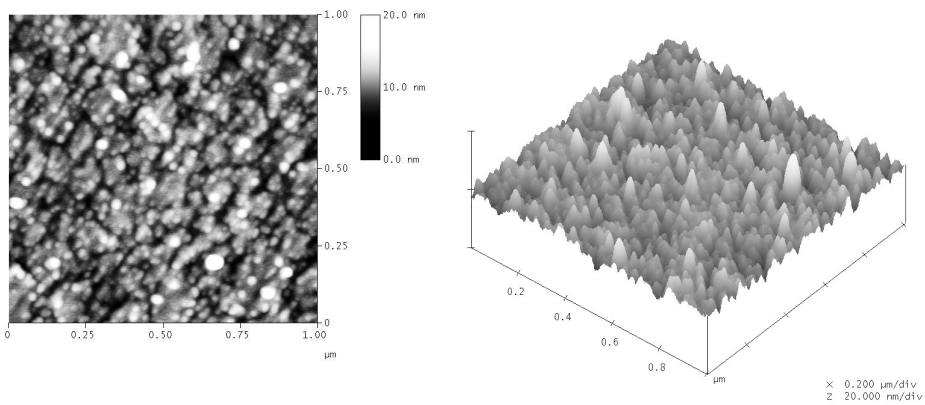


Fig. 3.5: AFM scan of $In_{0.53}Ga_{0.47}As$ after wet etch removal of the InP substrate. The roughness of $In_{0.53}Ga_{0.47}As$ is 18 Å.

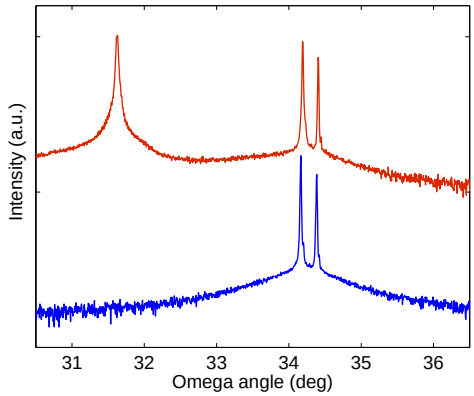


Fig. 3.6: XRD rocking-curve measurements of $In_{0.53}Ga_{0.47}As$ epitaxial transferred on SOI substrate (top), and a reference SOI substrate (bottom). Scans were taken with (004) silicon peak as a reference. (NB! Intensity is not in scale.)

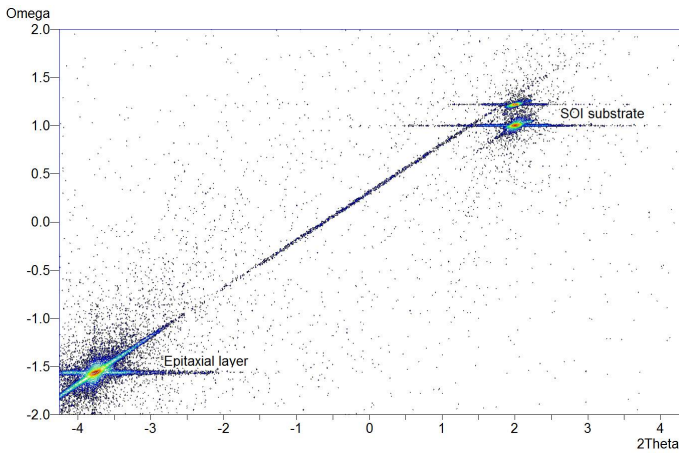


Fig. 3.7: 2D X-ray diffraction scan showing $In_{0.53}Ga_{0.47}As$ epitaxial layer and two peaks corresponding to SOI substrate. Scan was taken with (004) silicon peak as a reference.

Chapter 4

Integrated HBV frequency multipliers

In this chapter, a silicon and silicon-on-insulator (SOI) integrated frequency multipliers in HBV technology are presented. The chapter begins with a detailed description of fabrication procedure for these devices. It is divided into two parts: front- and back-side technologies. The back-side process, which is described in here, was developed specifically for circuits on SOI substrate. The chapter continues with design methodology for HBV diode and frequency multiplier circuits. Then characterisation methods such as DC characterisation, vector network analysis and RF measurements are described. This is followed by the main results for both silicon and SOI technology.

4.1 Technology

Fabrication of integrated frequency multipliers is divided into front and back-side processing. The front-side process is dedicated to HBV device and circuit fabrication, while the back-side process is dedicated to wafer thinning, back-side metallisation, and device separation. The processing steps are described in the following subsections.

4.1.1 Front-side technology

The front-side technology is divided into HBV device formation, air-bridge and microstrip circuit electroplating. The HBV diode is formed using standard III-V fabrication methods. The fabrication steps are illustrated in Fig. 4.1. In the first process step, a UV negative photoresist is applied and the ohmic contact areas are patterned. The pattern exposure and photoresist development is followed by a 30 s long wet etch in HCl:H_2O_2 (1:100) solution, which removes native oxide from $In_{0.53}Ga_{0.47}As$ surface. Native oxide is removed prior to ohmic contact metallisation evaporation.

Two types of metallisation stacks to form ohmic contact to $In_{0.53}Ga_{0.47}As$ have been studied, i.e. Ni/Ge/Au (10 nm/50 nm/150 nm) and Ti/Pd/Au (20 nm/40 nm/200 nm). The Ni/Ge/Au contact requires a thermal annealing step in order to allow germanium diffusion into the epilayer, contributing to increased doping concentration [166]. The

Ni/Ge/Au ohmic contact after annealing at 280 °C for 60 s in N_2 atmosphere shows contact resistance of approximately 2 $\times 10^{-4}$ Ωmm. However, even short annealing time at elevated temperatures will produce voids due to hydrogen outgassing, which originates from the molecular water at the bonding interface [167, 168]. This is resolved by performing annealing after isolation wet etch or use of metallisation that results in an ohmic contact without annealing. Ti/Pd/Au forms ohmic contact as-deposited, and the contact resistance is approximately 2.5 $\times 10^{-4}$ Ωmm. Rapid thermal annealing tests at temperatures below 300 °C did not show significant improvement in the contact resistance value [169].

In addition to ohmic contact metallisation, a 200 nm thick Ti layer is evaporated. This layer is later used as a mask for mesa dry etching.

Following the metallisation lift-off, mesas are first dry etched in CH_4 atmosphere, and subsequently wet etched in H_2O_2:H_2SO_4:H_2O solution. The wet etch results in reduced damage to the mesa side walls, but also reduces the cross sectional mesa dimensions.

Diode formation is followed by electrical mesa isolation. Mesas are first protected with a positive photoresist and then the remaining buffer layer is wet etched in H_2O_2:H_3PO_4:H_2O solution.

Prior to the air-bridge connections and microstrip circuit electroplating, the silicon substrate is passivated with SiO_2. The process steps are shown in Fig. 4.1(d) and 4.1(e). First, diodes are patterned with photoresist, and then SiO_2 is deposited by reactive sputtering. Subsequently, photolithography is repeated and the dielectric is wet etched from diode areas in diluted solution of buffered hydrofluoric acid (BHF). Hydrophobic surface indicates that SiO_2 was completely removed.

Prior to gold electroplating, a layer consisting of PMGI DUV resist is applied on the chip. Subsequently, a seed layer comprised of Ti/Au (10 nm/100 nm) is DC sputtered on the chip surface. In the following photolithography step, the electroplated area that defines air-bridge connections and microstrip components is patterned with a 3.6 μm thick photoresist. Then, 2 μm of gold is deposited by electroplating. After gold deposition the resist is stripped and the seed layer is removed by ion beam sputtering, and the PMGI layer is dissolved in warm photoresist remover.

4.1.2 SOI back-side technology

There is a significant difference in the back-side technology between a W-band frequency tripler [Paper B] and a 500 GHz frequency quintupler [Paper A]. The circuit presented in [Paper B] was fabricated on a bulk silicon substrate, while the circuit from [Paper A] makes use of silicon-on-insulator (SOI) substrate with predefined device thickness. In [Paper A], after completing the process of integrated circuits fabrication, the chip is diced into individual components, and then the substrate is thinned to the desired thickness. For the circuit on SOI, a new approach was developed, and the process flow is illustrated in Fig. 4.2.

Prior to thinning, front side of SOI wafer is coated with thick photoresist (approximately 6 μm), which protects devices from mechanical damage. Then, the silicon chip is mounted upside down on a carrier wafer with a UV curable adhesive. This simplifies silicon handling after the thinning process. Sapphire wafer is used as a carrier. Choice of sapphire is motivated by its excellent thermal properties, hence it provides effective heat reduction during the dry etching process.

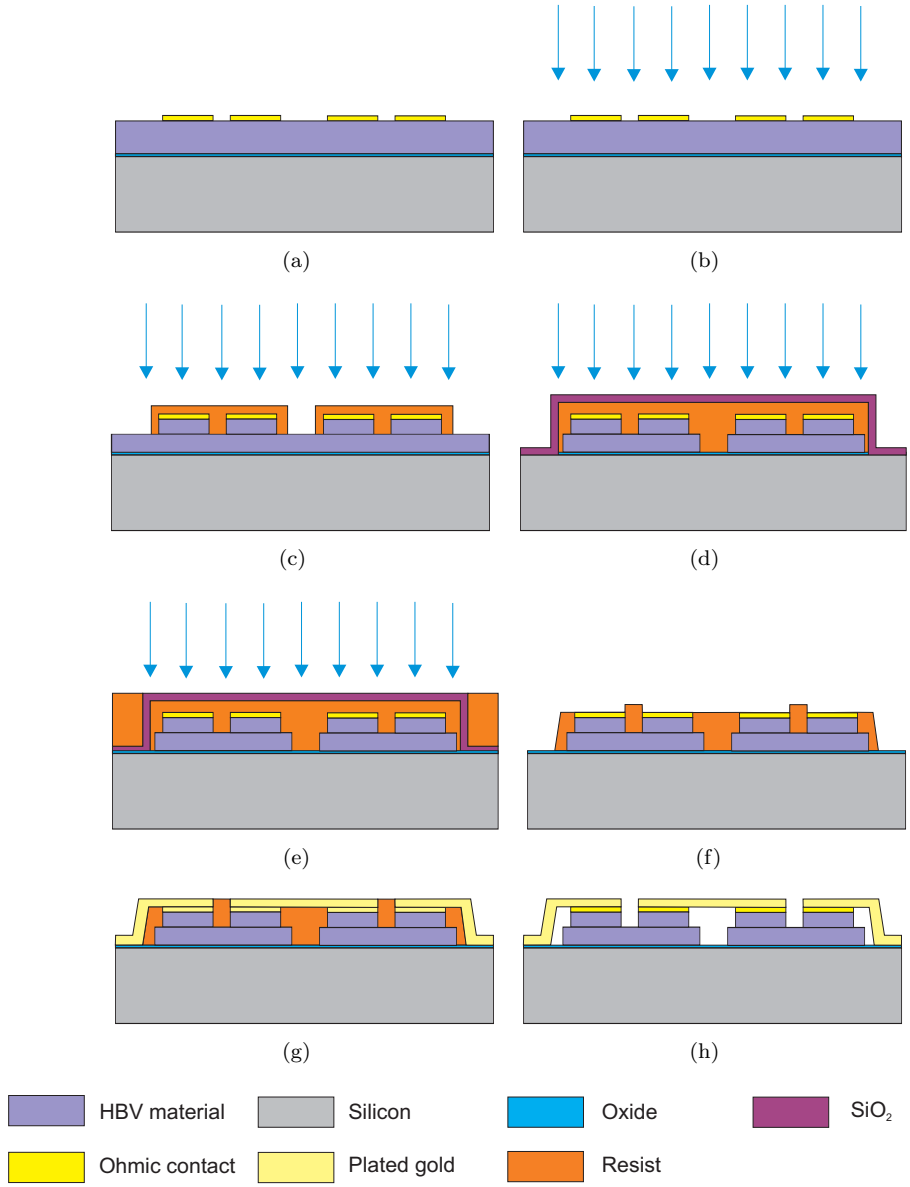


Fig. 4.1: Front-side process flow for integrated HBV frequency multipliers. (a) Ohmic contact formation. (b) Mesas dry and wet etch. (c) Diode isolation by wet etch removal of $In_{0.53}Ga_{0.47}As$ buffer. (d) SiO_2 deposition. Mesas are protected with a photoresist. (e) Wet etch of remaining dielectric layer from mesa area. Photoresist mask is dissolved in resist remover. (f) Photolithography and Au seed layer sputtering. (g) Photolithography and Au electroplating of air bridges and microstrip circuits. (h) Ion beam etching of seed layer and dissolution of PMGI e-beam resists. (NB! Drawings are not in scale.)

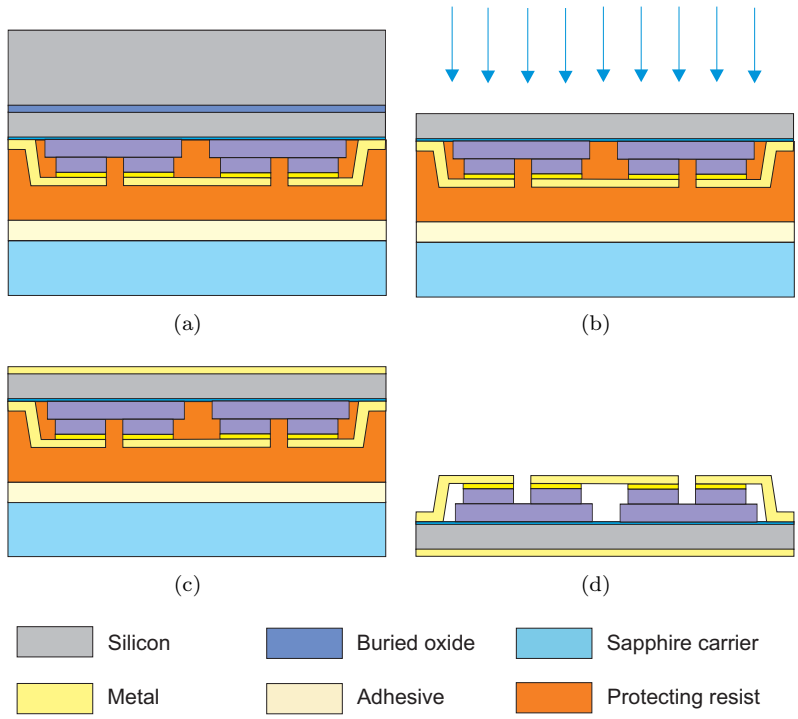


Fig. 4.2: Process flow for circuits on SOI. (a) Upside-down assembly on a sapphire carrier wafer. (b) Dry etch of the bulk silicon handle, followed by wet etch removal of buried oxide. (c) IR back-side photolithography followed by evaporation of metallisation and lift-off. Subsequently, trenches are patterned on the back-side of silicon, and etched in the Bosch process. (d) Removal of the protecting photoresist and circuits release from the carrier wafer. (NB! Drawings are not in scale.)

Next, the silicon handle is dry etched in SF_6 atmosphere. The high selectivity towards SF_6 dry etching between silicon and silicon dioxide ensures that the etching process will stop when the buried oxide is reached. The dry etch technique was prioritized over wet etch technique i.e. KOH and TMAH. It is mainly because of the high temperature etch solutions (80 °C) and slow etch rate, i.e. for KOH it is 65 $\mu m/h$, and for TMAH the etch rate is 20 $\mu m/h$.

Subsequently, the buried oxide is wet etched in buffer oxide etch solution, and the silicon device layer is exposed. In the next step, the back-side of the chip is patterned with IR back-side alignment, and then Ti/Au (5 nm/200 nm) is evaporated. Afterwards, the chip is patterned with thick photoresist which masks the back-side circuit area. The patterned trenches are etched by deep reactive ion etching (Bosch process), and the individual circuits are released from the carrier wafer by dissolving the protecting resist in warm acetone.

4.2 Circuit design and characterisation

4.2.1 Design

The process of circuit design has an iterative nature, in which different circuit components are first optimised separately, and then combined into one item for the final optimisation. The design is divided into several steps that involve optimisation of the diode material structure for low leakage current and high breakdown voltage, followed by optimisation of individual microstrip circuit components for input and output matching, and waveguide probes design. The diode and circuit design methodology and the aims of the optimisation are shortly described below.

• Diode optimisation

Design of a HBV based frequency multiplier begins with optimisation of material structure. The aim is to obtain low conduction current and to maximise the breakdown voltage of the diode [75]. An important parameter that must be considered is the thermal conductivity (κ) of the materials, which will influence the device thermal resistance (R_{th}). In power devices, a high R_{th} value is the main limiting factor for their high power operation. For example, a HBV diode in $In_{0.53}Ga_{0.47}As$ (κ=4.82 W/mK at RT) on InP substrate will have 21 % higher R_{TH} than if the same diode was realised in GaAs (κ=51 W/mK at RT) on GaAs substrate [Paper D]. The R_{th} value can be reduced by 21 % if InP substrate is replaced with silicon, and 50 % in case when silicon is used instead of GaAs substrate [Paper D].

The number of mesas and diode dimensions are optimised using a HBV self-consistent electro-thermal model [68] and harmonic balance simulations. Ideally, the diode dimensions should be smaller than $\lambda/10$. The optimum embedding impedances of the diode should result in the highest possible conversion efficiency. With the optimum diode impedances at desired harmonics the frequency multiplier circuit can be designed.

• Circuit design

Fig. 4.3 show models for frequency multipliers with possible varactor diode mounting configurations. A common method is to realise circuit with microstrip elements. The input signal at fundamental frequency (f_p) is introduced to the varactor with an input

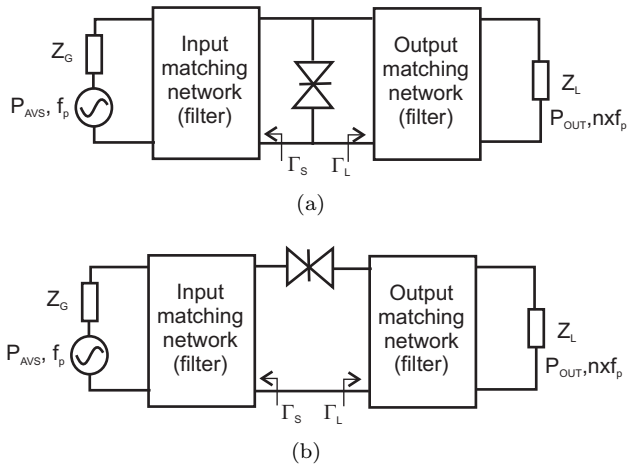


Fig. 4.3: Model for for n-order frequency multiplier with (a) shunt and (b) series mounted HBV diode with respect to input and output network.

matching circuit. The input matching must provide a good match for the fundamental frequency and should include a band-stop filter for higher order harmonics. Since HBV diodes generate only odd harmonics of the input signal ($3\times f_p$, $5\times f_p$, ...), an idler circuit must be included only if a frequency quintupler or higher is to be designed. The output matching network must provide an impedance matching at the output frequency, as well as an RF ground at f_p. Input and output waveguide probes are included in the design, if the frequency multiplier is to be assembled in a waveguide configuration. The input probe couples the input signal at f_p to the circuit, while the output probe couples the generated signal at $n\times f_p$ to the output waveguide. Part of the design is circuit channel optimisation, and it aims to effectively cut-off higher order electromagnetic modes, so that only desired microstrip mode is present. An example of a frequency tripler in HBV technology for W-band is shown in Fig. 4.4. The drawing depicts individual circuit elements.

4.2.2 DC characterisation

The purpose of DC characterisation is to validate the quality of the diode in terms of carrier density and junction capacitance (C_j). To do that a current-voltage (I-V) and capacitance-voltage (C-V) measurements are taken at RT and in dark conditions. The dark measurement conditions eliminate light influence onto device performance. Prior to C-V measurement an open/short compensation is performed in order to extract parasitics from the test set-up components such as probes and cable connections. The C-V curve is taken at AC voltage frequency 1 MHz.

From the I-V measurements a leakage current and breakdown voltage of the diode can be estimated. Performing I-V at different temperatures (T) and plotting I/T^2 versus $1/T$ at constant bias the barrier height (ϕ_B) can be estimated [170]. The doping concentration can be extracted from the slope $1/C^2$-V.

A typical DC characteristic of an integrated four mesas (twelve barriers) HBV diode

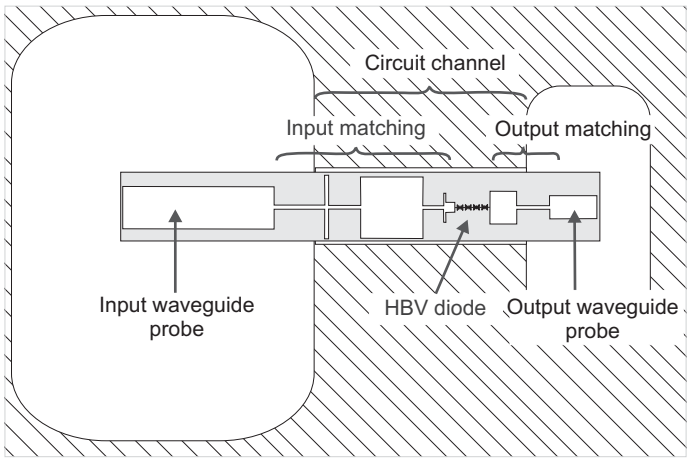


Fig. 4.4: Scheme of a frequency tripler in HBV technology, showing circuit elements.

is shown in Fig. 4.5. The measurement was taken from -10 V to 10 V. The maximum capacitance for this diode is 130 fF, which gives a maximum barrier capacitance of 2.2 fF/μm^2.

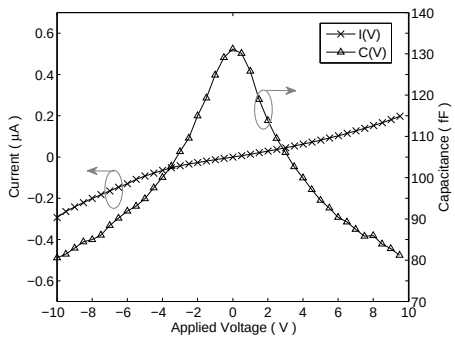
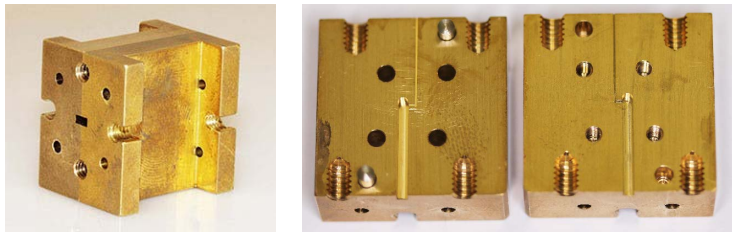


Fig. 4.5: Measured current-voltage and capacitance-voltage for four-mesas HBV diode with 700 μm^2 contact area.

4.2.3 S-parameter characterisation

Although, the C-V characterisation with LRC method is capable of measuring impedance in broad range, this method is limited to hundreds of megahertz. Thus, for devices with high leakage current (parallel conductance, G_p) accurate extraction of C_j is difficult. An alternative method to LRC are scattering parameters (S-parameters) measurements. In this method the device impedance is characterised by measuring incident, reflected and transmitted waves with vector network analyser, usually over a broad frequency range. Performed at high frequencies S-parameter characterisation allows for accurate extrac-



(a) (b)

Fig. 4.6: Photograph of a split waveguide block for 500 GHz a frequency quintupler. Block dimensions are 18 mm×22 mm×22 mm (width×height×length).

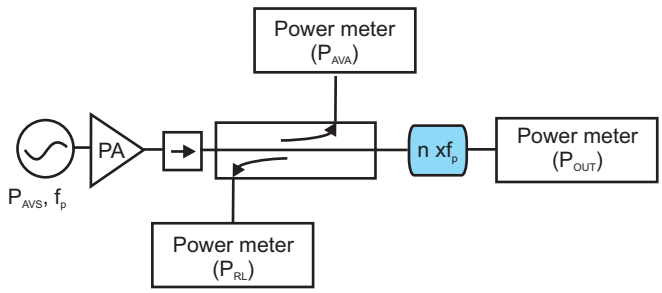


Fig. 4.7: Schematic of RF characterisation setup.

tion of bias dependent diode small-signal equivalent circuit parameters, i.e. R_S, C_j and G_p [171].

4.2.4 RF characterisation

Prior to the RF characterisation the frequency multiplier circuit is assembled in the waveguide channel with a nonconducting glue, wax or solder paste. An example of a waveguide block, which consists of two split and mirrored parts is shown in Fig 4.6. The waveguide block is machined in a brass which is gold electroplated later. The brass-machined waveguides are not the only option for high frequency circuits assembly. Waveguides formed in SU-8 [172, 173] and in silicon [52, 55] were also demonstrated.

The RF characterisation scheme is shown in Fig. 4.7. The input signal is provided by an Agilent E8257D signal generator. If the input signal is in the W-band range (75–110 GHz), then a frequency extender from Agilent/OML is placed after the signal generator. The signal level (P_{AVS}) from the signal generator is 18 dBm, and from the W-band frequency extender it is 5 dBm. This power is usually amplified with a single power amplifier or a chain of power amplifiers. For frequency range between 30 GHz and 40 GHz a Spacek Labs Ka-band power amplifier is used [Paper B], [Paper C], while a GaN power amplifier is used at W-band frequency range [Paper A].

To avoid unwanted effects of standing wave, an isolator is placed after the power amplifier. A 10 dB coupler, which follows the isolator, allows for accurate monitoring of the available power (P_{AVA}) delivered to the frequency multiplier, and the reflected

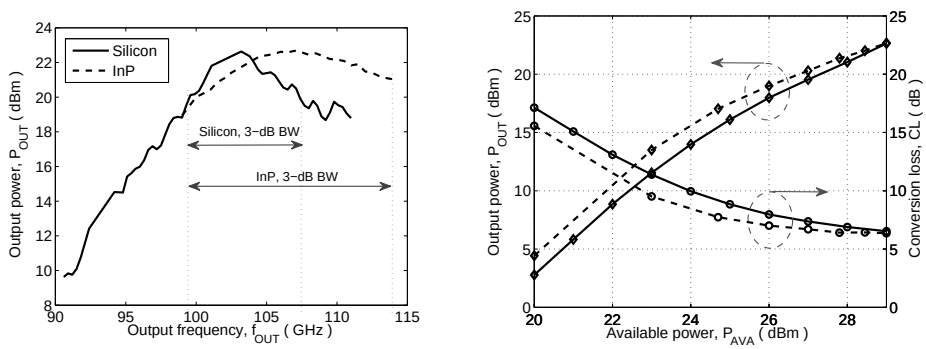
power (P_{RL}). In our case P_{AVA} and P_{RL} are measured with an Agilent power meter E4418B and with an Erickson power meter PM4, respectively. The output power from the frequency multiplier at the desired harmonic is measured with an Erickson PM4 power meter.

4.3 Silicon integrated frequency multipliers

A monolithic integrated frequency tripler for W-band (75–110 GHz) has been designed and demonstrated with InP technology [84],[Paper C]. Because of small difference in the permittivity between InP and silicon material, the same circuit concept was realised on a silicon substrate with epitaxially transferred $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ [Paper B].

The device performance was compared in terms of an output power (P_{OUT}) at 29 dBm power available (P_{AVA}), 3-dB bandwidth, and conversion loss (CL). In Fig. 4.8(a) the measured P_{OUT} versus output frequency (f_{OUT}) for both devices when driven with 29 dBm P_{AVA} is shown. Both devices deliver almost 23 dBm of P_{OUT} at 103 GHz and at 107 GHz f_{peak} for circuits on silicon and InP substrate respectively. The shift in the f_{peak} for these devices can be caused by one of the following factors. First, the diode fabrication processes were not identical, e.g. non-alloyed ohmic contacts were used for diodes formed in epitaxially transferred material. Second, is related to the chip assembly precision in the waveguide block. The monolithically integrated frequency tripler shows broader 3-dB bandwidth if compared with heterogeneously integrated device, marked in Fig. 4.8(a). However, if one considers the device's CL then the silicon integrated frequency multiplier is better than the other device, see Fig. 4.8(b).

To conclude, the insignificant differences in the RF performance between demonstrated frequency triplers with monolithic and heterogeneous integration technology show that the latter has potential for use in high frequency electronics applications.



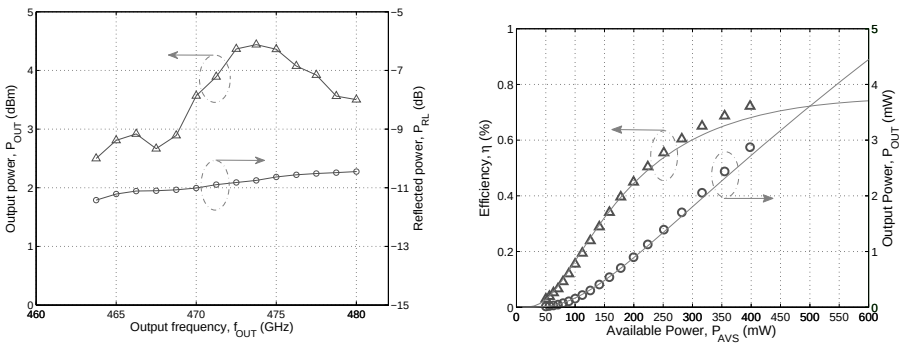
(a) (b)

Fig. 4.8: (a) Output power characteristics at 29 dBm P_{AVA} and 3-dB bandwidth for devices on InP (dashed) and silicon (solid) substrate. (b) Output power and conversion loss at centre frequency for InP (dashed) and silicon (solid) integrated frequency tripler.

4.4 Frequency multipliers in SOI technology

At THz frequencies, for an optimum circuit performance, the substrate must be thinned to a few micrometres. However the thinning process, which is usually done by etching or mechanical lapping, does not assure a uniform and accurate thickness of the final chip. Therefore other methods must be considered. Use of silicon-on-insulator (SOI) is one of possible solutions. By replacing bulk silicon with a SOI wafer thin and uniform devices can be fabricated [174]. The SOI technology was implemented for Schottky diode frequency quadrupler up to 160 GHz [22] and for a 474 GHz frequency quintupler in HBV technology [Paper A]. The latter represents the highest frequency of operation for to-date demonstrated HBV frequency multipliers. It is worth mentioning that the HBV frequency quintupler from [Paper A] was designed in InP technology. However, neither DC nor RF characterisation of 20 μm thick InP MMICs was possible due to circuits bending and breaking. This is not an issue for devices processed on SOI substrate. Excellent mechanical properties of silicon allow for fabrication of planar, uniform in thickness, and robust circuits.

The RF characterisation results for the SOI integrated frequency quintupler are shown in Fig. 4.9(a). The maximum P_{OUT} for this devices is 2.8 mW for 26 dBm P_{AVA}, and the reflected power (P_{RL}) is better than -10 dB. In Fig. 4.9(b) P_{OUT} as a function of P_{AVA} and corresponding conversion efficiency (η) at f_{peak} for this device are presented. Its maximum conversion efficiency is 0.75% [Paper A].



(a) (b)

Fig. 4.9: (a) Measured output and return power for 26 dBm power available. (b) Output power and corresponding conversion efficiency versus power available measured at centre frequency. The measurement results are given with symbols, while the solid line corresponds to the simulation results [Paper A].

Chapter 5

Conclusions and future outlook

In this thesis diode-circuit integration approaches for THz applications were studied. Great part of this work was devoted to technology development for heterogeneously integrated Heterostructure Barrier Varactor (HBV) frequency multipliers on silicon and silicon-on-insulator (SOI) substrates. This is motivated by the fact that the optimal substrate material in terms of electronic, thermal and mechanical properties is often different from the native substrate that the epitaxial material was grown on. By enabling the integration of high performance epitaxy with a suitable substrate, an increase in the performance and functionality of the final device is achieved.

Common methods for diode integration in a high frequency circuit are hybrid and monolithic integration (MIC). The hybrid refers to a method in which a discrete diode is flip-chip assembled or wire bonded to a circuit. For high power electronics most convenient substrate materials are those which provide an efficient heat-dissipation from the active device. This is addressed in [Paper E] in which microstrip circuit was fabricated on AlN substrate - a material which has good thermal conductivity. Presented in [Paper E] frequency quintupler at center frequency of 175 GHz delivers 60 mW of power corresponding to 6.3 % efficiency.

However, with an increase of operational frequency the circuit and diode dimensions must be scaled respectively. These consequently reduce the assembly tolerances for hybrid technology. Therefore, a MIC technology represents a more convenient approach to the issue that allows high circuit reproducibility. An example of MIC integrated frequency tripler on InP substrate is presented in [Paper C]. The device delivers more than 180 mW of output power at 107 GHz, over 15 % broad 3-dB band. However, InP is a fragile material in a way that when thinned to few micrometres it becomes difficult to handle and waveguide assemble. In addition, high power operation of devices on InP substrates is limited by low thermal conductivity of the material. Therefore, use of substrate materials with significantly better mechanical and thermal properties is essential.

An integration of compound semiconductors onto foreign substrate is one of the possible scenarios in heterogeneous integration. This method is common for silicon integrated photonic devices, however it shows a great potential for THz electronic applications also. An example of silicon integrated frequency tripler is given in [Paper B]. It employs the same circuit design as in [Paper C]. The $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HBV material structure was transferred onto silicon using a process of low temperature plasma as-

sisted wafer bonding. Measured output power of 180 mW at 103 GHz, and 9 % broad 3-dB bandwidth for this device is comparable with the results in [Paper C]. The thermal analysis presented in [Paper D] showed that the material transfer to substrates with higher thermal conductivity reduces thermal resistance of the diode, consequently enhancing its thermal performance.

Considering specific requirements for final substrate thickness at THz frequencies, a technology for heterogeneous integrated devices on SOI substrate was developed. Use of SOI wafer with predefined device layer thickness allowed to achieve robust 20 μm frequency multiplier circuits [Paper A]. With measured output power of 2.8 mW at 474 GHz, this device showed great potential of integrated HBV technology as future power sources.

Use of unique mechanical properties of silicon allows for further advancement of membrane, via-holes and filters micromachining. In addition, complex waveguide structures with integrated antennas can be obtained in one process, which reduces misalignments that are in due time detrimental for performance of THz applications. This gives possibility for 3D integration of new generation THz circuits and systems.

Summary of appended papers

Paper A

A 474 GHz HBV Frequency Quintupler Integrated on a 20-μm Thick Silicon Substrate

This paper presents the first silicon integrated HBV frequency quintupler for 474 GHz. The $In_{0.53}Ga_{0.47}As$ based material structure was epitaxial transferred on silicon-on-insulator (SOI) substrate in order to obtain an accurate and uniform final circuit thickness (20μm). In addition to that the steady-state thermal simulations were implemented to study the thermal performance of this diode.

Contribution: I developed the process for SOI substrate, transferred epitaxial material onto SOI, fabricated devices and circuits, performed DC and RF characterisation, analysed measurements data, and wrote the paper.

Paper B

Silicon Integrated InGaAs/ InAlAs/ AlAs HBV Frequency Tripler

The results present the first silicon integrated $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HBV frequency tripler operating at W-band frequency range. The maximum output power measured for this device is better than 180 mW, which corresponds to 23 % efficiency. The performance of this device is comparable with the state-of-the-art monolithic integrated HBV $\times$ 3 frequency multiplier described in [Paper C].

Contribution: I personally contributed to the epitaxial transfer of InP-based HBV material structure onto silicon substrate, device fabrication, DC and RF characterisation, data analysis, and writing the paper.

Paper C

High Efficiency and Broad-Band Operation of Monolithically Integrated W-Band HBV Frequency Tripler

This conference publication presents a monolithically integrated HBV frequency tripler on InP substrate. The circuit delivers 185 mW output power at 107 GHz, corresponding to 23 % efficiency, and 15 % of 3-dB bandwidth.

Contribution: I personally contributed to the device fabrication, DC and RF char-

acterisation, data analysis and writing the paper.

Paper D

Thermal Analysis of III-V HBV Diode Structures on InP, GaAs, Silicon and Diamond Substrates

This paper presents steady-state thermal simulations of $In_{0.53}Ga_{0.47}As$ and GaAs HBV diodes on InP, GaAs, silicon and diamond substrates. The physical dimensions of the studied diode correspond to the dimensions of high power integrated HBV frequency multipliers for W-band. It is shown that material transfer onto substrates with better thermal conductivity than the donor substrate reduces the thermal resistance, thus allowing for enhanced thermal handling capability.

Contribution: I have prepared the steady-state thermal simulations, data analysed and wrote the paper.

Paper E

A 175 GHz HBV Frequency Quintupler With 60 mW Output Power

This publication describes a fixed tuned frequency quintupler at 175 GHz. The discrete HBV diode is flip-chip soldered into a microstrip matching circuitry. The circuit is fabricated from AlN substrate, a material that has a excellent thermal properties which ensure enhanced heat-dissipation from the active component. The presented device delivers 60 mW output power corresponding to 6.3 % efficiency.

Contribution: I personally contributed to the fabrication and DC characterisation of the discrete devices and writing the paper.

Acknowledgment

For the last five years I had possibility to work with many people. Most of them were source of inspiration, motivation and advice. The list is long, and it begins with *Prof. Jan Stake* my examiner and main supervisor. Thank you for the PhD study opportunity at Terahertz and Millimeter Wave Laboratory.

The list continues with my co-supervisors, which number over the past two years tripled suddenly. First, *Dr. Josip Vukusic* who introduced me to the HBV technology. Without designs from *Dr. Tomas Bryllert* I would not have much to work on. And finally *Dr. Huan Zhao* thanks to whom I started to work on molecular beam epitaxy and development of InGaAs Schottky diodes.

Others that should not be forgotten are *Prof. Erik Kollberg* for the feedback on the publications. *Anke Sanz-Velasco* who introduced me to the technology of low temperature plasma assisted wafer bonding. Special thanks go to *Zonghe Lai* for all of these masks that he prepared for my projects, and TEM images which appear in this thesis. *Göran Petersson* who shared with me his knowledge on silicon fabrication. *Mahdad Sadeghi* for the epitaxial material growth. *Arne Øistein Olsen* for RF characterisation assistance, and squash games which kept me in shape.

I shall not forget the current and former staff from the *Nanofabrication Laboratory, Chalmers University of Technology*, in particular: *Johan Andersson*, *Henrik Frederiksen*, *John Halonen*, *Mats Hagberg*, *Karin Hedsten*, *Piotr Jedrasik*, *Kaija Matikainen*, *Emmy Nilsson* and *Ulf Södervall* for their assistance in the cleanroom whenever needed.

I wish to acknowledge all of my colleagues form Terahertz and Millimetre Wave Laboratory, Group of Advanced Receiver Development, Microwave Electronics Laboratory, Physical Chemistry, from the process laboratory and my former neighbors. Thanks to you Chalmers and Göteborg was not only place of labour. I wish not to forget colleagues from my study time in Wroclaw, from whom I am always happy to hear and whom I visit whenever I travel to Poland.

Last but not least, to my *parents* and *family* for their love and support during these years.

This PhD work was in part funded by the *European Space Agency (ESA)*, the *Swedish Research Council (VR)* and the *Swedish National Space Board*.

Bibliography

[1] P. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 910–927, 2002.

[2] T. Phillips and J. Keene, "Submillimeter astronomy," *Proceedings of IEEE*, vol. 80, pp. 1662–1678, 1992.

[3] H. B. Liu, H. Zhong, N. Karpowicz, Y. Chen, and X. C. Zhang, "Terahertz spectroscopy and imaging for defense and security applications," *Proceedings of IEEE*, vol. 95, pp. 1514–1527, 2007.

[4] J. Federici and L. Moeller, "Review of terahertz and subterahertz wireless communications," *Journal of Applied Physics*, vol. 107, p. 111101, 2010.

[5] P. H. Siegel, "Terahertz technology in biology and medicine," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2438–2447, 2004.

[6] M. Tschernitz, J. Freyer, and H. Grothe, "GaAs Read-type IMPATT diode for D-band," *Electronics Letters*, vol. 30, pp. 1070–1071, 1994.

[7] H. Eisele, "State of the art and future of electronic sources at terahertz frequencies," *Electronic Letters*, vol. 46, pp. 8–11, 2010.

[8] B. S. Williams, "Terahertz quantum-cascade lasers," *Nature Photonics*, vol. 1, pp. 517–525, 2007.

[9] A. Brown, K. Brown, J. Chen, K. Hwang, N. Kolias, and R. Scott, "W-band GaN power amplifier MMICs," in *IEEE MTT-S International Microwave Symposium*, 2011, pp. 167–168.

[10] L. A. Samoska, "An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, pp. 9–22, 2011.

[11] M. Abbasi, R. Kozhuharov, C. Karnfelt, I. Angelov, I. Kallfass, A. Leuther, and H. Zirath, "Single-chip frequency multiplier chains for millimeter-wave signal generation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 3134–3142, 2009.

[12] W. Deal, X. B. Mei, K. Leong, V. Radisic, S. Sarkozy, and R. Lai, "THz monolithic integrated circuits using InP high electron mobility transistors," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, pp. 25–32, 2011.

[13] T. W. Crowe, W. L. Bishop, D. W. Porterfield, J. L. Hesler, and R. M. Weikle, "Opening the terahertz window with integrated diode circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2104–2110, 2005.

[14] E. L. Kollberg and A. Rydberg, "Quantum-barrier-varactor diodes for high-efficiency millimetre-wave multipliers," *Electronic Letters*, vol. 25, pp. 1696–1698, 1989.

[15] N. Erickson, "High efficiency submillimeter frequency multipliers," in *IEEE MTT-S International Microwave Symposium*, vol. 3, 1990, pp. 1301–1304.

[16] M. Krach, J. Freyer, and M. Claassen, "Schottky tripler for 210 GHz," *Electronics Letters*, vol. 36, pp. 858–859, 2000.

[17] E. Schlecht, G. Chattopadhyay, A. Maestrini, A. Fung, S. Martin, D. Pukala, J. Bruston, and I. Mehdi, "200, 400 and 800 GHz Schottky diode "substrateless" multipliers: design and results," in *IEEE MTT-S International Microwave Symposium*, vol. 3, 2001, pp. 1649–1652.

[18] G. Chattopadhyay, E. Schlecht, J. Ward, J. Gill, H. Javadi, F. Maiwald, and I. Mehdi, "An all-solid-state broad-band frequency multiplier chain at 1500 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 1538–1547, 2004.

[19] A. Maestrini, J. S. Ward, J. J. Gill, H. S. Javadi, E. Schlecht, C. Tripon-Canseliet, G. Chattopadhyay, and I. Medhi, "A 540–640 GHz high-efficiency four-anode frequency tripler," *IEEE Transactions on Microwave Thoery and Techniques*, vol. 53, pp. 2835–2843, 2005.

[20] D. W. Porterfield, "High-efficiency terahertz frequency triplers," in *IEEE MTT-S International Microwave Symposium*, 2007, pp. 337–340.

[21] M. Hrobak, M. Strens, M. Schramm, W. Stein, and L. P. Schmidt, "Design and fabrication of broadband hybrid GaAs Schottky diode frequency multiplier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, pp. 4442–4460, 2013.

[22] N. Alijabbari, M. F. Bauwens, and R. M. Weikle, "Design and characterisation of integrated submillimeter-wave quasi-vertical Schottky diodes," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, pp. 1–8, 2014.

[23] S. Kumar, B. S. Williams, Q. Hu, and J. L. Reno, "1.9 THz quantum-cascade lasers with one-well injector," *Applied Physics Letters*, vol. 88, p. 121123, 2006.

[24] C. Walther, M. Fischer, G. Scalari, and R. Terazzi, "Quantum cascade lasers operating from 1.2 THz to 1.6 THz," *Applied Physics Letters*, vol. 91, p. 131122, 2007.

[25] M. Ravaro, M. Locatelli, L. Viti, D. Ercolani, L. Consolino, S. Bartalini, L. Sorba, M. S. Vitiello, and P. D. Natale, "Detection of a 2.8 THz quantum cascade laser with a semiconductor nanowire field-effect transistor coupled to a bow-tie antenna," *Applied Physics Letters*, vol. 104, p. 083116, 2014.

[26] K. Ishigaki, K. Karashima, M. Shiraishi, H. Shibayama, S. Suzuki, and M. Asada, "Direct modulation of THz-oscillating resonant tunneling diodes," in *International Conference on Infrared, Millimeter and Terahertz Waves*, 2011.

[27] M. Feiginov, H. Kanaya, S. Suzuki, and M. Asada, "1.46 THz RTD oscillators with strong back injection from collector," in *International Conference on Infrared, Millimeter and Terahertz Waves*, 2014.

[28] H. Eisele and R. Kamouna, "Submillimeter-wave InP Gunn devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2371–2378, 2004.

[29] C. Benz and J. Freyer, "200 GHz pulsed GaAs-IMPATT diodes," *Electronics Letters*, vol. 34, pp. 2351–2353, 1998.

[30] A. Maestrini, J. S. Ward, J. Gill, C. Lee, B. Thomas, R. Lin, G. Chattopadhyay, and I. Mehdi, "A frequency-multiplied source with more than 1 mW of power across the 840–900 GHz band," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, pp. 1925–1932, 2010.

[31] Q. Xiao, J. L. Hesler, Y. Duan, T. W. Crowe, and R. M. Weikle, "A 300-GHz heterostrucutre barrier varactor (HBV) frequency septupler," in *International Conference on Infrared, Millimeter, and Terahertz Waves*, 2005, pp. 80–81.

[32] J. Vukusic, T. Bryllert, T. Emadi, M. Sadeghi, and J. Stake, "A 0.2 W heterostructure barrier varactor frequency tripler at 113 GHz," *IEEE Electron Device Letters*, vol. 28, pp. 340–342, 2007.

[33] J. Vukusic, T. Bryllert, A. O. Olsen, J. Hanning, and J. Stake, "Monolithic HBV-based 282 GHz tripler with 31 mW output power," *IEEE Electron Device Letters*, vol. 33, pp. 800–802, 2012.

[34] M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, M. Hu, A. Corrion, W. Wong, A. Schmitz, P. Hashimoto, P. Willadsen, and D. Chow, "W-band GaN MMIC amplifiers," in *IEEE Lester Eastman Conference*, 2010.

[35] M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, M. Hu, A. Corrion, A. Fung, R. Lin, L. Samoska, P. Kangaslahti, B. Lambrigsten, P. Goldsmith, W. Wong, A. Schmitz, P. Hashimoto, P. Willadsen, and D. H. Chow, "W-band GaN MMIC with 842 mW output power at 88 GHz," in *IEEE MTT-S International Microwave Symposium*, 2010, pp. 237–240.

[36] A. Tessmann, A. Leuther, V. Hurm, H. Messler, and M. Zink, "A 300 GHz mHEMT amplifier module," in *International Conference on Indium Phosphide and Related Materials*, 2009, pp. 1–4.

[37] I. Kallfass, P. Phal, H. Massier, A. Tessmann, S. Koch, and T. Zwick, "A 200 GHz monolithic integrated power amplifier in metamorphic HEMT technology," *IEEE Microwave and Wireless Component Letters*, vol. 19, pp. 410–412, 2009.

[38] L. Samoska, A. Peralta, M. Hu, M. Micovic, and A. Schmitz, "A 20 mW 150 GHz InP HEMT MMIC power amplifier module," *IEEE Microwave and Wirless Component Letters*, vol. 14, pp. 56–58, 2004.

[39] L. Samoska, E. Bryerton, M. Morgan, D. Thacker, K. Saini, T. Boyd, D. Pukala, A. Peralta, M. Hu, and A. Schmitz, "Medium power amplifiers covering 90–130 GHz for the ALMA telescope local oscillators," in *IEEE MTT-S International Microwave Symposium*, 2005, pp. 1583–1586.

[40] P. Huang, R. Lai, R. Grundbacher, and B. Gorospe, "A 20 mW G-band monolithic driver amplifier using 0.07 μm InP HEMT," in *IEEE MTT-S International Microwave Symposium*, 2006, pp. 806–809.

[41] W. Deal, X. Mei, V. Radisic, M. Lange, W. Yoshida, P. Liu, J. Uyeda, M. Barsky, A. Fung, T. Gaier, and R. La, "Development of sub-millimeter-wave power amplifiers," *IEEE Transcations on Microwave Theory and Techniques*, vol. 55, pp. 2719–2726, 20107.

[42] V. Radisic, W. R. Deal, K. Leong, W. Yoshida, P. H. Liu, J. Uyeda, A. Fung, L. Samoska, T. Gaier, and R. Lai, "A 10 mW submillimeter wave solid state power amplifier module," *IEEE Transcations on Microwave Theory and Techniques*, vol. 58, pp. 1903–1909, 2010.

[43] V. Radisic, K. Leong, X. Mei, S. Sarkozy, W. Yoshida, P. Liu, J. Uyeda, R. Lai, and W. R. Deal, "A 50 mW 220 GHz power amplifier module," in *IEEE MTT-S International Microwave Symposium*, vol. 58, 2010, pp. 45–48.

[44] R. A. Pucel, "Design considerations for monolithic microwave circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 6, pp. 513–534, 1981.

[45] O. Moutanabbir and U. Gösele, "Heterogenous integration of compound semiconductors," *Annaul Review of Materials Research*, vol. 40, pp. 469–500, 2010.

[46] L. Dillner, W. Strupinski, S. Hollung, C. Mann, J. Stake, M. Beardsley, and E. Kollberg, "Frequency multiplier measurements on heterostrucutre barrier varactor on a copper substrate," *IEEE Electron Device Letters*, vol. 21, pp. 206–208, 2000.

[47] S. Arscott, P. Mounaix, and D. Lippens, "Substrate transfer process for InP-based heterostrucutre barrier varactor devices," *Journal of Vacuum Science andTechnology B*, vol. 18, pp. 150–155, 2000.

[48] S. M. Marazita, W. L. Bishop, J. L. Hesler, K. Hui, W. E. Bowen, and T. W. Crowe, "Integrated GaAs Schottky mixers by spin-on-glass dielectric wafer bonding," *IEEE Transactions on Electron Devices*, vol. 47, pp. 1152–1157, 2000.

[49] M. Henry, B. Alderman, H. Sanghera, P. Maagt, and D. Matheson, "High-efficiency transferred substrate GaAs varactor multipliers for the terahertz spectrum," in *Terahertz Physics, Devices and Systems*, 2010, p. 76710.

[50] C. Lee, J. Ward, R. Lin, E. Schlecht, G. Chattopadhyay, J. Gill, B. Thomas, A. Maestrini, I. Mehdi, and P. Siegel, "A wafer-level diamond bonding process to improve power handling capability of submillimeter-wave Schottky diode frequency multipliers," in *IEEE MTT-S International Microwave Symposium*, 2009, pp. 957–960.

[51] B. Alderman, M. Henry, A. Maestrini, J. Grajal, R. Zimmermann, H. Sanghera, H. Wang, P. Wilkinson, and D. Matheson, "High power frequency multipliers to 330 GHz," in *European Microwave Integrated Circuits Conference*, 2010, pp. 232–233.

[52] V. M. Lubecke, K. Mizuno, and G. F. Rebeiz, "Micromachining for therahertz applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 1821–1831, 1998.

[53] J. L. Hesler, K. Hui, R. K. Dahlstrom, R. M. Weikle, and T. W. Crowe, "Analysis of an octagonal micromachined horn antenna for submillimeter-wave applications," *IEEE Transactions on Antennas and Propagation*, vol. 49, pp. 997–1001, 2001.

[54] P. L. Kirby, Y. Li, Q. Xiao, J. L. Hesler, and J. Papapolymerou, "Silicon micromachined multiplier utilizing heterostructure barrier varactor diode," in *IEEE MTT-S International Microwave Symposium*, 2007, pp. 1141–1144.

[55] C. Jung, C. Lee, B. Thomas, G. Chattopadhayay, A. Peralta, R. Lin, J. Gill, and I. Mehdi, "Silicon micromachining technology for THz applications," in *International Conference on Infrared, Millimeter, and Terahertz Waves*, 2011.

[56] Y. Li, I. Mehdi, A. Maestrini, R. H. Lin, and J. Papapolymerou, "A broadband 900 GHz silicon micromachined two-anode frequency tripler," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, pp. 1673–1681, 2001.

[57] P. Penfield and R. P. Refuse, *Varactor applications.* Cambridge, Massachusetts, M.I.T. Press, 1962.

[58] D. W. Porterfield, T. W. Crowe, R. F. Bradley, and N. R. Erickson, "A high-power fixed-tuned millimeter-wave balanced frequency doubler," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, pp. 419–425, 1999.

[59] W. C. B. Peatman, T. W. Crowe, and M. Shur, "A novel Schottky/2-DEG diode for millimeter- and submillimeter-wave multiplier applications," *IEEE Electron Device Letters*, vol. 13, pp. 11–13, 1992.

[60] U. Lienweg, B. R. Hancock, and J. Maserjian, "Barrier-intrinsic n^2 (BIN) diode for near-millimeter wave generation," in *Inthernational Conference on Millimeter Waves*, 1987, pp. 6–7.

[61] M. Krach, J. Freyer, and M. Claassen, "Schottky diode tripler for 210 GHz," *Electronics Letters*, vol. 36, pp. 858–859, 2000.

[62] A. Uhlir, "The potential of semiconductor diodes in high-frequency communications," in *Proceedings of the Institute of Radio Engineers*, vol. 46, 1958, pp. 1099–1115.

[63] J. M. Manley and H. E. Rowe, "Some general properties of nonlinear elements - part i. General energy relations," *Proceedings of the Institute of Radio Engineers*, vol. 4, pp. 904–913, 1956.

[64] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. John Wiley & Sons, Inc., 2007.

[65] E. L. Kollberg, T. J. Tolmunen, M. A. Freking, and J. R. East, "Current saturation in submillimeter-wave varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, pp. 831–838, 1992.

[66] T. W. Crowe, T. C. Grein, R. Zimmermann, and P. Zimmermann, "Progress towards solid-state local oscillators at 1 THz," *IEEE Microwave and Guided Wave Letters*, vol. 6, pp. 207–208, 1996.

[67] M. Ingvarson, "Modelling and design of high-power HBV multipliers," Ph.D. dissertation, Chalmers University of Technology, 2004.

[68] M. Ingvarson, J. Vukusic, A. O. Olsen, T. A. Emadi, and J. Stake, "An electrothermal HBV model," in *IEEE MTT-S International Microwave Symposium*, 2005, pp. 1151–1153.

[69] L. Dillner, J. Stake, and E. L. Kollberg, "Analysis of symmetric varactor frequency multipliers," *Microwave and Optical Technology Letters*, vol. 15, pp. 26–29, 1997.

[70] L. E. Dickens, "Spreading resistance as a function of frequency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 15, pp. 101–109, 1967.

[71] A. Y. Tang and J. Stake, "Impact of eddy currents and crowding effects on high frequency losses in planar Schottky diodes," *IEEE Transactions on Electron Devices*, vol. 58, pp. 3260–3269, 2011.

[72] J. Stake, L. Dillner, S. H. Jones, C. M. Mann, J. Thornton, J. R. Jones, W. L. Bishop, and E. L. Kollberg, "Effects of self-heating on planar heterostructure barrier varactor diodes," *IEEE Transactions on Electron Devices*, vol. 45, pp. 2298–2303, 1998.

[73] M. Ingvarson, B. Alderman, A. O. Olsen, J. Vukusic, and J. Stake, "Thermal constrains of heterostructure barrier varactor," *IEEE Electron Device Letters*, vol. 25, pp. 713–715, 2004.

[74] J. Stake, "Planar heterostructure barrier varactor diode for millimetre-wave applications," Ph.D. dissertation, Chalmers University of Technology, 1999.

[75] T. A. Emadi, T. Bryllert, M. Sadeghi, J. Vukusic, and J. Stake, "Optimum barrier thickness study for the InGaAs/InAlAs/AlAs heterostrucutre barrier varactor," *Applied Physics Letters*, vol. 90, p. 012108, 2007.

[76] D. Choudhary, M. A. Frerking, and P. D. Batelaan, "A 200 GHz tripler using a single barrier varactor," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, pp. 595–599, 1993.

[77] V. K. Reddy and D. P. Neikirk, "High breakdown voltage AlAs/InGaAs quantum barrier varactor diodes," *Electronics Letters*, vol. 29, pp. 464–466, 1993.

[78] X. Melique, A. Maestrini, E. Lheurette, P. Mounaix, M. Favreau, O. Vanbesien, J. M. Goutoule, G. Beaudin, T. Nahri, and D. Lippens, "12 % efficiency and 9.5 dBm output power from InP-based heterostructure barrier varactor triplers at 250 ghz," in *IEEE MTT-S International Microwave Symposium*, vol. 1, 1999, pp. 123–126.

[79] T. Bryllert, A. Malko, J. Vukusic, and J. Stake, "A 175 GHz HBV frequency quintupler with 60 mW output power," *IEEE Microwave and Wireless Components Letters*, vol. 22, pp. 76–78, 2012.

[80] M. Saglam, K. Mutamba, A. Megej, C. Sydlo, H. L. Hartnagel, and I. Daumiller, "Influence of polarization charges in $Al_{0.4}Ga_{0.6}N$/GaN heterostrucutre varactors," *Applied Physics Letters*, vol. 82, pp. 227–229, 2003.

[81] B. Nicolae, D. R. Chowdhury, and H. L. Hartnagel, "Experimental studies of $Al_{0.12}Ga_{0.88}N$/GaN heterostructure varactors in view of frequency increases," in *German Microwave Conference*, 2008, pp. 260–262.

[82] J. Stake, L. Dillner, and E. L. Kollberg, "Investigation of an InAs based heterostrucutre barrier varactor," in *GigaHertz Symposium*, 1995, p. 33.

[83] J. G. Champlain, R. Magno, M. Ancona, H. S. newman, and J. B. Boos, "InAs-based heterostructure barrier varactor devices with $In_{0.3}Al_{0.7}As_{0.4}Sb_{0.6}$ as the barrier material," *Solid-State Electornics*, vol. 52, pp. 1829–1832, 2008.

[84] J. Vukusic, T. Bryllert, A. O. Olsen, and J. Stake, "High-power W-band monolithically integrated tripler," in *International Conference on Infrared, Millimeter, and Terahertz Waves*, 2009.

[85] A. O. Olsen, M. Ingvarson, B. Alderman, and J. Stake, "A 100 GHz HBV frequency quintupler using microstrip elements," *IEEE Microwave and Wireless Components Letters*, vol. 14, pp. 493–495, 2004.

[86] J. Vukusic, B. Alderman, T. Emadi, M. Sadeghi, A. Olsen, T. Bryllert, and J. Stake, "HBV tripler with 21 % efficiency at 102 GHz," *Electronic Letters*, vol. 42, pp. 355–356, 2006.

[87] T. Bryllert, J. Vukusic, A. Olsen, and J. Stake, "A broadband heterostructure barrier varactor tripler source," in *IEEE MTT-S International Microwave Symposium*, 2010, pp. 344–347.

[88] R. Dahlbäck, J. Vukusic, R. M. Weikle, and J. Stake, "A weveguide embedded 250 GHz quasi-optical frequency tripler array," in *European Microwave Integrated Circuits Conference*, 2014, pp. 802–805.

[89] T. David, S. Arscott, J. M. Munier, T. Akalin, G. Beaudin, and D. Lippens, "Monolithic integrated circuits incorporating InP-based heterostructure barrier varactors," *IEEE Microwave and Wireless Components Letters*, vol. 12, pp. 281–283, 2002.

[90] Q. Xiao, J. L. Hesler, T. W. Crowe, R. M. Weilke, Y. Duan, and B. S. Deaver, "High-efficiency heterostructure- barrier-varactor frequency triplers using AlN substrates," in *IEEE MTT-S International Microwave Symposium*, 2005, pp. 443–446.

[91] M. Schumann, K. Duwe, C. Domoto, A. Megej, M. Rodriguez-Girones, J. Muller, R. Judaschke, and H. Hartnagel, "High-performance 450 GHz GaAs-based heterostructure barrier varactor tripler," *IEEE Electron Device Letters*, vol. 24, pp. 138–140, 2003.

[92] P. J. Sobis, A. Emrich, and J. Stake, "A low VSWR 2SB Schottky receiver," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, pp. 403–411, 2011.

[93] A. Tessmann, A. Leuther, V. Hurm, H. Messler, and M. Zink, "High-gain submillimeter-wave mHEMT amplifier MMICs," in *IEEE MTT-S Interational Microwave Symposium*, 2010, pp. 53–56.

[94] I. Kallfass, J. Antes, T. Schneider, F. Kurz, D. Lopez-Diaz, S. Diebold, H. Massler, A. Leuther, and A. Tessmann, "All active MMIC-based wireless communication at 220 GHz," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, pp. 477–487, 2011.

[95] P. Siegel, P. Smith, M. C. Gaidis, and S. C. Martin, "2.5 THz monolithic membrane-diode mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, pp. 596–604, 1999.

[96] F. Maiwald, S. Martin, J. Bruston, A. Maestrini, T. Crawford, and P. Siegel, "2.7 THz waveguide tripler using monolithic membrane diodes," in *IEEE MTT-S International Microwave Symposium*, 2001, pp. 1637–1640.

[97] E. Schlecht, J. Gill, R. Dengler, R. Lin, R. Tsang, and I. Mehdi, "A unique 520–590 GHz biased subharmonically-pumped Schottky mixer," *IEEE Microwave and Wireless Components Letters*, vol. 17, pp. 879–881, 2007.

[98] H. Zhao, V. Drakinskiy, P. Sobis, J. Hanning, T. Bryllert, A. Y. Tang, and J. Stake, "Development of a 557 GHz GaAs monolithic membrane diode," in *International Conference on Indium Phosphide and Related Materials*, 2012, pp. 102–105.

[99] V. Drakinskiy, P. Sobis, H. Zhao, T. Bryllert, and J. Stake, "Therahertz GaAs Schottky diode mixer and multiplier MIC's based on e-beam technology," in *International Conference on Indium Phosphide and Related Materials*, 2013.

[100] T. David, A. S. Arscot, J. M. Munier, T. Decoopman, T. Akalin, P. Mounaix, X. Melique, O. Vanbesien, G. Beaudin, and D. Lippens, "High performance HBV multipliers monolithically integrated onto a host quartz substrate," in *International Conference on Terahertz Electronics*, 2002, pp. 113–116.

[101] D. M. Pozar, *Microwave engineering.* John Wiley & Sons, Inc., 2005.

[102] S. A. Maas, *The RF and Microwave Circuit Design Cookbook.*

[103] G. D. Vendelin, "Limitations on stripline Q," *Microwave Journal*, vol. 13, pp. 63–69, 1970.

[104] S. Strite and H. Morkoç, "GaN, AlN and InN: A review," *Journal of Vacuum Science and Technology B*, vol. 10, pp. 1237–1266, 1992.

[105] M. Afsar and H. Chi, "Millimeter wave complex refractive index, complex dielectric permitivity and loss tangent of extra high purity and compensated silicon," *International Journal on Infrared and Millimeterwaves*, vol. 15, pp. 1181–1188, 1994.

[106] http://www.ioffe.ru/SVA/NSM/Semicond/.

[107] H. Espinosa, B. Peng, N. Moldovan, T. Friedmann, X. Xiao, D. Mancini, O. Auciello, J. Carlisle, and C. A. Zorman, "A comparison of mechanical properties of three MEMS materials - silicon carbide, ultrananocrystalline diamond, and hydrogen-free tetrahedral amorphous carbon (Ta-C)," in *International Conference on Fracture*, 2005.

[108] S. Chen, M. Afsar, and D. Sakdatorn, "Dielectric-parameter measusrements of SiC at millimeter and submillimeter wavelengths," *IEEE Transactions on Instrumentation and measurements*, vol. 57, pp. 706–715, 2008.

[109] http://www.cvd diamond.com/.

[110] C. Borgentun, C. Hessenius, J. Bengtsson, M. Fallahi, and A. Larsson, "Widely tunable high-power semiconductor disk laser with nonresonant AR-assisted gain element on diamond heat spreader," *IEEE Photonics Journal*, vol. 3, pp. 946–953, 2011.

[111] W. McGrath, C. Walker, M. Yap, and Y.-C. Tai, "Silicon microachined waveguides for millimeter-wave and submillimeter-wave frequencies," *IEEE Microwave and Guided Wave Letters*, vol. 3, pp. 61–63, 1993.

[112] D. Dochev, V. Desmaris, D. Meledin, A. Pavlotsky, and V. Belitsky, "A technology demonstrator for 1.6-2.0 THz waveguide HEB receiver with a novel mixer layout," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 32, pp. 451–465, 2011.

[113] T. Reck, L. Chen, C. Zhang, A. Arsenovic, C. Groppi, A. Lichtenberger, R. Weikle, and N. Barker, "Micromachined probes for submillimeter-wave on-wafer measurements," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, pp. 349–356, 2011.

[114] K. Leong, K. Henning, C. Zhang, R. Elmadjian, Z. Zhou, B. S. Gorospe, P. Chang-Chien, V. Radisic, and W. R. Deal, "WR1.5 silicon michromachined waveguide components and active circuit integration methodology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, pp. 998–1005, 2012.

[115] D. Lederer and J. P. Raskin, "Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers," *Solid State Electronics*, vol. 47, pp. 1927–1936, 2003.

[116] B. Rong, J. N. Burghartz, L. K. Nanver, B. Rejaei, and M. van der Zwan, "Surface passivated high resistivity silicon substrates for RFICs," *IEEE Electron Device Letters*, vol. 25, pp. 176–178, 2004.

[117] A. Jansman, J. van Beek, M. van Delden, A. Kemmeren, A. den Dekker, and F. Widdershoven, "Elimination of accumulation charge effects for high resistivity silicon substrate," in *Conference on European Solid State Device Research*, 2003, pp. 3–6.

[118] M. Kao, C. Lee, R. Hajji, P. Saunier, and H.-Q. Tserng, "AlGaN/GaN HEMTs with PAE of 53% at 35 GHz for HPA and multi-function MMIC applications," in *IEEE MTT-S International Microwave Symposium*, 2007, pp. 627–629.

[119] M. Südow, M. Fagerlind, M. Thorsell, K. Andersson, N. Billstrom, P.-A. Nilsson, and N. Rorsman, "An AlGaN/GaN HEMT-based microstrip MMIC process for advanced transceiver design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, pp. 1827–1833, 2008.

[120] J. L. Hesler, H. Xu, T. Reck, and T. W. Crowe, "Development and testing of a 2.5 THz Schottky mixer," in *International Conference on Infrared, Millimeter and Terahertz Waves*, 2011, pp. 1–2.

[121] J. W. Gardner, V. K. Varadan, and O. O. Awadelkarim, *Microsensors MEMS and smart devices*. John Wiley & Sons, Inc., 2007.

[122] S. F. Fang, K. Adomi, S. Iyer, H. Morkoc, H. Zabel, C. Choi, and N. Otsuka, "Gallium arsenide and other compound semiconductors on silicon," *Journal of Applied Physics*, vol. 68, pp. 31–58.

[123] Y. Lo, "New approach to grow pseudomorphic substrates over the critical thickness," *Applied Physics Letters*, vol. 59, pp. 2311–2313, 1991.

[124] A. M. Jones, J. L. Jewell, J. C. Mabon, E. E. Reuter, S. G. Bishop, S. D. Roh, and J. J. Coleman, "Long-wavelength InGaAs quantum wells grown without strain-induced warping on InGaAs compliant membranes above a GaAs substrate," *Applied Physics Letters*, vol. 74, pp. 1000–1002, 1999.

[125] C. Pei, J. Heroux, J. Sweet, W. Wang, J. Chen, and M. Chang, "High quality GaAs grown on Si-on-insulator compliant substrates," *Journal of Vacuum Science and Technology B*, vol. 20, pp. 1196–1199, 2002.

[126] Z. Yu, J. Ramdani, J. A. Curless, C. D. Overgaard, J. M. Finder, R. Droopad, K. W. Eisenbeiser, J. A. Hallmark, W. J. Ooms, and V. S. Kaushik, "Epitaxial oxide thin films on Si(001)," *Journal of Vacuum Sicience and Technology B*, vol. 18, pp. 2139–2145, 2000.

[127] K. Eisenbeiser, R. Emrick, R. Droopad, Z. Yu, J. Finder, S. Rockwell, J. Holmes, C. Overgaard, and W. Ooms, "GaAs MESFETs fabricated on Si substrate using a $SrTiO_3$ buffer layer," *IEEE Electron Device Letters*, vol. 23, pp. 300–302, 2002.

[128] M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, M. Radosavljevic, T. Rakish, and R. Chau, "Heterogeneus integration of enhancement mode $In_{0.7}Ga_{0.3}As$ quantum well transistor on silicon substrate using thin (2 μm) composite buffer architecture for high-speed and low-voltage (0.5 v) logic applications," in *IEEE International Electron Device Meeting*, 2007, pp. 625–628.

[129] T. Ashley, L. Bruckle, S. Datta, M. T. Emeny, D. G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. J. Wallis, P. J. Wilding, and R. Chau, "Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications," *Electronics Letters*, vol. 43, 2007.

[130] L. Desplanque, S. E. Kazzi, C. Coinon, S. Ziegler, B. Kunert, A. Beyer, K. Volz, W. Stolz, Y. Wang, P. Ruterana, and X. Wallart, "Monolithic integartion of high electron mobility InAs-based heterostructure on exact (001) silicon using GaSb/GaP accomodation layer," *Applied Physics Letters*, vol. 101, p. 142111, 2012.

[131] H. J. Oh, K. J. Choi, W. Y. Loh, T. Htoo, S. J. Chua, and B. J. Cho, "Integration of GaAs epitaxial layer to Si-based susbtrate using Ge condenstation and low-temperature migration enhanced epitaxy techniques," *Journal of Applied Physics*, vol. 102, p. 054306, 2007.

[132] C. Junesund, W. Metaferia, F. Olsson, M. Avella, J. Jimenez, G. Pozina, L. Hultman, and S. Lourdudoss, "Heteroepitaxial growth of indium phosphide from nano-openings made by masking on a Si (001) wafer," in *International Conference on Indium Phosphide and Relatad Materials*, 2010.

[133] C. W. Hsu, Y. F. Chen, and Y. K. Su, "Heteroepitaxy for GaAs on nanopatterned Si (001)," *IEEE Photonics technology letters*, vol. 24, pp. 1009–10 011, 2012.

[134] S. C. Lee, L. R. Dawson, and S. R. J. Brueck, "Heteroepitaxial selective growth of $In_xGa_{1-x}As$ on SiO_2-patterned GaAs(001) by molecular beam epitaxy," *Journal of Applied Physics*, vol. 96, pp. 4856–4865, 2004.

[135] T. Kazior, J. R. Laroche, D. Lubyshev, J. M. Fastenau, W. K. Liu, M. Urteaga, W. Ha, J. Bergman, M. J. C. M. T. Bulsara, E. A. Fitzgerald, D. Smith, D. Clark, R. Thompson, C. Drazek, N. Daval, L. Benaissa, and E. Augendre, "A high performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates," in *IEEE MTT-S International Microwave Symposium*, 2009, pp. 1113–1116.

[136] A. Sanz-Velasco, "The RDGT - integration of micromechanics and electronics by plasma assisted wafer bonding," Ph.D. dissertation, Chalmers University of Technology, 2002.

[137] A. Plössl and G. Kräuter, "Wafer direct bonding: tailoring adhesion between brittle materials," *Material Science and Engineering*, vol. 25, pp. 1–88, 1999.

[138] D. Pasquarielo and K. Hjort, "Plasma-assisted InP-to-Si temperature wafer bonding," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 8, pp. 118–131, 2002.

[139] K. Hjort, "Transfer of InP epilayers by wafer bonding," *Journal of Crystal Growth*, vol. 268, pp. 346–358, 2004.

[140] A. Sanz-Velasco, C. Rusu, I. Ferain, C. Colinge, and M. Goorsky, *Lattice engineering: technology and applications*. Pan Stanford Publishing, 2013, ch. Low-temperature direct wafer bonding, pp. 135–188.

[141] J. Bickford, S. S. Lau, and P. K. L. Yu, "GaAs/Si metal wafer bonding for hetereogeneous integrated circuits," in *International Conference on Solid-State and Integrated-Circuit Technology*, 2008, pp. 1180–1183.

[142] O. Cojocari, I. Oprea, A. Walber, and H. Gibson, "Schottky based THz MICs," in *European Microwave Integrated Circuits Conference*, 2011, pp. 232–235.

[143] J. Chung, E. Piner, and T. Palacios, "N-face GaN/AlGaN HEMTs fabricated through layer transfer technology," *IEEE Electron Device Letters*, vol. 30, pp. 113–116, 2009.

[144] T. Kraemer, I. Ostermay, T. Jensen, T. K. Johansen, F. J. Schmuckle, A. Thies, V. Krozer, W. Heinrich, O. Krueger, G. Traenkle, M. Lisker, A. Trusch, P. Kulse, and B. Tillack, "InP-DHBT-on-BiCMOS technolofy with f_T/f_{max} of 400/350 GHz for heterogeneous integrated millimeter-wave sources," *IEEE Tranasctions on Electron Devices*, vol. 60, pp. 2209–2216, 2013.

[145] M. Hossain, T. Kraemer, I. Ostermay, T. Jensen, B. Janke, Y. Borokhovych, M. Lisker, S. Glisic, M. Elkhouly, J. Borngraeber, B. Tillack, C. Meliani, O. Krueger, V. Krozer, and W. Heinrich, "A 280 GHz hetero-integrated frequency source in InP-on-BiCMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 24, pp. 469–471, 2014.

[146] G. Roelkens, J. van Campenhout, J. Bouckeart, D. van Thourhout, P. R. Romeo, P. Regreny, A. Kazmierczak, C. Seassal, X. Letartre, G. Holling, J. M. Fedeli, L. D. Cioccio, and C. Lagaha-Blanchard, "III-V/Si photonics by die-to-wafer bonding," *Materials Today*, vol. 10, pp. 36–43, 2007.

[147] J. Yang, Z. Peng, D. Cheong, and R. Kleiman, "Fabrication of high-efficiency III-V on silicon multijunction solar cells by direct metal interconnect," *IEEE Journal of Photovoltaics*, vol. 4, pp. 1149–1155, 2014.

[148] M. Alexe, V. Dragoi, M. Reiche, and U. Gösele, "Low temperature GaAs/Si direct wafer bonding," *Electronics Letters*, vol. 36, pp. 677–678, 2000.

[149] D. Liang and J. E. Browers, "Highly efficient vertical outgassing channels for low-temperature InP-to-silicon direct wafer bonding on the silion-on-insulator," *Journal of Vacuum Science and Technology B*, vol. 26, pp. 1560–1568, 2008.

[150] R. Bower and F. Y. Chin, "Low temperature direct silicon wafer bonding using argon activation," *Japanese Journal of Applied Physics*, vol. 36, pp. 527–528, 1997.

[151] H. H. Chang, A. W. Fang, M. N. Sysak, H. Park, R. Jones, O. Cohen, O. Raday, M. J. Paniccia, and J. E. Bowers, "1310 nm silicon evanescent laser," *Optics Express*, vol. 15, pp. 11 466–11 471, 2007.

[152] R. McClelland, C. Bozler, and J. Fan, "A technique for producing epitaxial films on reuseable substrates," *Applied Physics Letters*, vol. 37, pp. 560–562, 1980.

[153] M. Bruel, "Silicon on insulator material technology," *Electronics Letters*, vol. 31, pp. 1201–1202, 1995.

[154] E. Jalaguier, B. Aspar, S. Pocas, J. F. Michaud, M. Zussy, A. M. Papon, and M. Bruel, "Transfer of 3inch GaAs film on silicon substrate by proton implantation process," *Electronics Letters*, vol. 34, pp. 408–409, 1998.

[155] Q. Y. Tong, Y. L. Chao, L. J. Huang, and U. Gösele, "Low temperature InP layer transfer," *Electronics Letters*, vol. 35, pp. 341–342, 1999.

[156] L. D. Cioccio, E. Jalaguier, and F. Ltertre, "III-V layer transfer onto silicon and applications," *Physica Status Solidi*, vol. 202, pp. 509–515, 2005.

[157] M. Konagai, M. Sugimoto, and K. Takahashi, "High efficiency GaAs thin film solar cells by peeled film technology," *Journal of Crystal Growth*, vol. 45, pp. 277–280, 1978.

[158] C. Cheng, K. Shiu, N. Li, S. Han, L. Shi, and D. Sadan, "Epitaxial lift-off for gallium arsenide substrate reuse and flexible electronics," *Nature Communications*, vol. 4, pp. 1–7, 2013.

[159] E. Yablonovich, D. M. Hwang, T. J. Gmitter, L. T. Florez, and J. P. Harbison, "Van der Waals bonding of GaAs epitaxial films onto arbitrary substrates," *Applied Physics Letters*, vol. 56, pp. 2419–2421, 1990.

[160] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding: science and technology.* John Wiley & Sons, Inc., 1999, ch. Thinning procedure, pp. 137–173.

[161] K. Lee, D. Zimmerman, X. Xiao, K. Sun, and S. Forrest, "Reuse of GaAs substrates for epitaxial lift-off by employing protection layers," *Journal of Applied Physics*, vol. 111, pp. 033 527–1 – 033 527–6, 2012.

[162] P. G. Young, S. A. Alterovitz, R. A. Mena, and E. D. Smith, "RF properties of epitaxial lift-offg HEMT devices," *IEEE Tranasctions on Electron Devices*, vol. 40, pp. 1905–1909, 1993.

[163] J. C. Fan, C. P. Lee, J. A. Hwang, and J. H. Hwang, "AlGaAs/GaAs heterostrucutre bipolar transistors on Si substrate using epitaxial lift-off," *IEEE Electron Device Letters*, vol. 16, pp. 393–395, 1995.

[164] I. Pollentier, P. Demeester, A. Ackaert, L. Buydens, P. van Daele, and R. Baets, "Epitaxial lift-off GaAs LEDs to Si for fabrication of opto-electronic integrated circuits," *Electronics Letters*, vol. 26, pp. 193–194, 1990.

[165] K. Lee, K.-T. Shiu, J. D. Zimmerman, C. K. Renshaw, and S. R. Forrest, "Multiple growth of epitaxial lift-off solar cells from a single InP substrate," *Applied Physics Letters*, vol. 97, p. 101107, 2010.

[166] R. Williams, *Modern GaAs processing methods.* Artech House, 1990, ch. Ohmic contacts, pp. 211–240.

[167] M. Wiegand, M. Reiche, and U. Gösele, "Time dependent surface properties and wafer bonding of O_2-plasma-treated silicon (100) surfaces," *Journal of The Electrochemical Society*, vol. 147, pp. 2734–2740, 2000.

[168] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding: science and technology.* John Wiley & Sons, Inc., 1999, ch. Thermal treatment of bonded wafer pairs, pp. 103–135.

[169] E. F. Chor, W. K. Chong, and C. H. Heng, "Alternative (Pd,Ti,Au) cotnacts to (Pt,Ti,Au) contacts to $In_{0.53}Ga_{0.47}As$," *Journal of Applied Physis*, vol. 84, pp. 2977–2979, 1998.

[170] D. K. Schroder, *Semiconductor material and device characterisation.* John Wiley & Sons, Inc., 2006.

[171] A. Y. Tang, V. Drakinskiy, K. Yland, J. Stenarson, T. Bryllert, and J. Stake, "Analytical extraction of a Schottky diode model based on broadband S-parameters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, pp. 1870–1878, 2013.

[172] A. Pavalotsky, D. Meledin, C. Risacher, M. Pantaleev, and V. Belitsky, "Micromachining approach in fabricating of THz waveguide components," *Michromechanics Journal*, vol. 36, pp. 683–6986, 2005.

[173] C. H. Smith, X. Hu, and S. Baker, "Development of a multi-layer SU-8 process for terahertz frequency waveguide blocks," in *IEEE MTT-S International Microwave Symposium*, 2005, pp. 439–442.

[174] R. B. Bass, J. C. Schultz, A. W. Lichtenberger, R. M. Weikle, S. K. Pan, E. Bryertron, C. K. Walker, and J. Kooi, "Ultr-thin silicon chips for submillimeter-wave applications," in *International Symposium on Space Terahertz Technology*, 2004, pp. 392–399.

Appendix

Epitaxial transfer

1. Silicon wafer preparation	
Silicon cleaning	
Solution	NH_4:H_2O_2:H_2O
Content	1:5:20
Time	10 min
Temperature	60 °C
Water rinse	
Native oxide removal	
Solution	2% HF
Time	30 s
Temperature	RT
Water rinse	
2. Plasma oxidation	
ICP power	800 W
Electrode power	15 W
Plasma	O_2 20 sccm
Gas pressure	20 mTorr
Time	30 s
3. Wafer bonding	
Pressure	1,000 mbar
Temperature	50 °C
Time	4 h
4. InP substrate wet etch removal	
Etchant	HCl:H_2O
Content	5:1
Temperature	RT

Sputter deposition of 100 nm thick SiO_2

Substrate cleaning	
Plasma	Ar 30 sccm
Power	40 W
Pressure	5 mTorr
Time	30 s
SiO_2 deposition	
Plasma	O_2 5sccm, Ar 30 sccm
RF power	250 W
Pressure	10 mTorr
Time	7 min

Photolithography for defining electroplating area in AZ4533

Dehydration bake	100 °C, 60 s
Spin resist	4000 rpm, 30 s
Bake	100 °C, 90 s
Dehydration	RT, 15 min
Edge beak exposure	120 s
Develop	AZ351:DI (1:5), 100 s
Pattern exposure	30 s
Develop	AZ351:DI (1:5), 100 s
Descum	20 s