CHALMERS

Design of a drive stage of a Mosfet SiC converter

Master of Science Thesis

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Abstract

This thesis is about studying the gate driving of a Mosfet.

One step was to build a new circuit board for this investigation using the software Target.

First experiments were made that aim to test the driving circuit using an R,C load instead of a Mosfet. When comparing with the simulation, it appears that the gate driver operates as quick and normal as expected when it is used with an R,C load unless R and C are very small (smaller than what it would be using a Mosfet). However, when it is connected to a Mosfet and an R,L load, it doesn't react as fast as expected with the increasing drain-source voltage.

Finally, the last part but not the least of this project consists of investigating the switching losses in a Mosfet and an SiC Mosfet. The result are not conclusive so far since the current measurement is biased.

Keywords

Loss computation, Mosfet, Vehicle application, Power electronics, SiC Mosfet, Switching phenomena.

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Contents

1

Introduction

NOWADAYS, THE FOCUS is more and more on environmental issues. The global warming, the environmental degradation and the resource depletion lead to lots of investigations including researches on how to reduce the emissions and enhance the efficiency of the vehicles.

1.1 Problem background

Hybrid and electric vehicles seem to be a response for the changes in the energy domain towards more sustainable solutions. In such vehicles, power electronic devices have a great influence on the efficiency of the vehicles. Among those power electronic devices, there are power electronic converters whose purpose is to convert the electrical power from a certain voltage or current form into another one. The losses in the converters are essentially originating from conduction losses and switching losses.

This thesis deals with switching losses in Mosfets and SiC Mosfets. The latter is interesting in terms of sustainable development since SiC components provides a higher band gap and thermal conductivity as well as quicker switchings. So far, a first circuit test has been done. However, some improvements are needed such as being able to maintain the driving gate voltage at a constant level when a current pulse is sent to the gate and making the current and voltage measurements easier.

Above is the first aspect of this thesis work. Another big part of the project is to better predict the switching losses from the information given in data sheets. Indeed, for IGBTs the phenomenon is quite well described in data sheets while for Mosfets some key times are given, but only valid for specific conditions.

1.2 Purpose of work

The main purpose of this thesis is to enhance the knowledge of how to get accurate switching loss values for Mosfets in a real implementation. In order to fulfill this aim, the following steps are needed:

- Improvement of an old existing set-up, in particular regarding the driving circuit.
- Measurements of the switching losses with the new design.
- Mathematical modeling of the switching process in Mosfets.

Thus, another way to formulate the objective of the work is : to get the theory to match the measurements as much as possible.

2

Background theory

In this chapter, the backgroung theory needed to achieve the project is briefly presented. There is also a little description of the softwares used.

2.1 Power electronics converters

2.1.1 Half-bridge converter

Figure 2.1 is a representation of a half-bridge converter in the case where the capacitors C_1 and C_2 are equal.

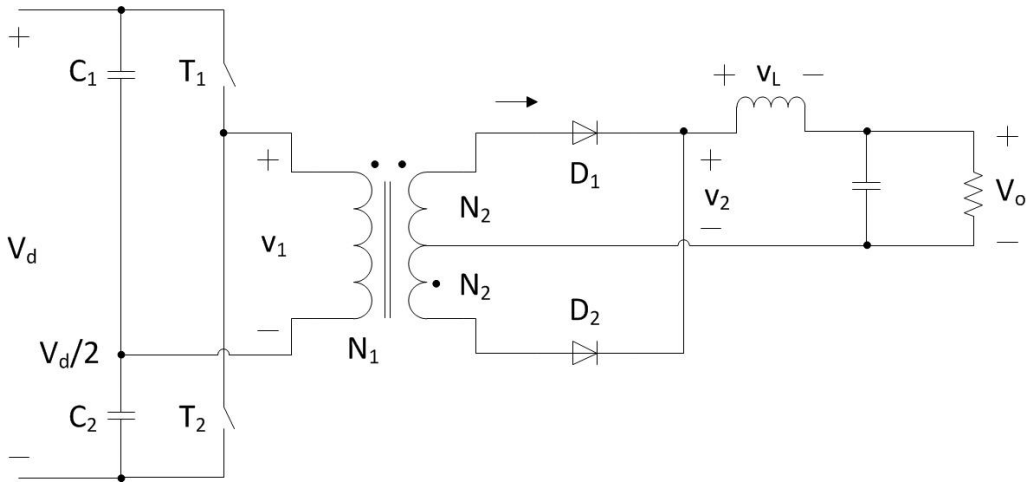


Figure 2.1: Half-bridge converter when $C_1 = C_2$

In such a device, the switches T_1 and T_2 are alternatively on during a time called t_{on}. There is a time when both switches are off. This time is called Δ.

When T_1 is turned on, the circuit becomes as it is shown in Figure 2.2.

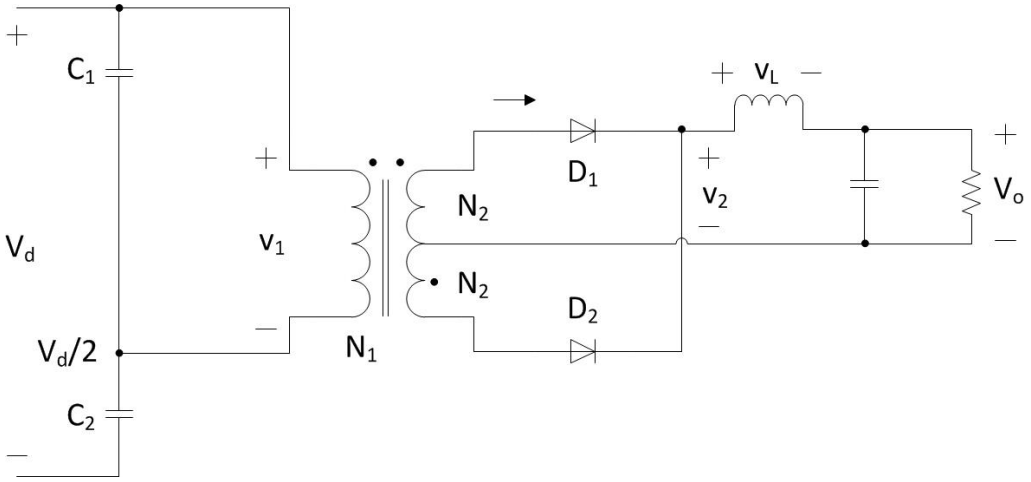


Figure 2.2: Half-bridge circuit during the time t_{on}

Kirchhoff's law yields

$$v_{oi} - v_L - V_o = 0$$

As $\frac{v_2}{V_d/2} = \frac{N_2}{N_1}$ (equation of the transformer), the inductor voltage is

$$v_L = v_2 - V_o = \frac{N_2}{N_1}\frac{V_d}{2} - V_o \qquad \text{if } 0 < t < t_{on} \tag{2.1}$$

During the time Δ, when T_1 and T_2 are off, the circuit becomes as in Figure 2.3.

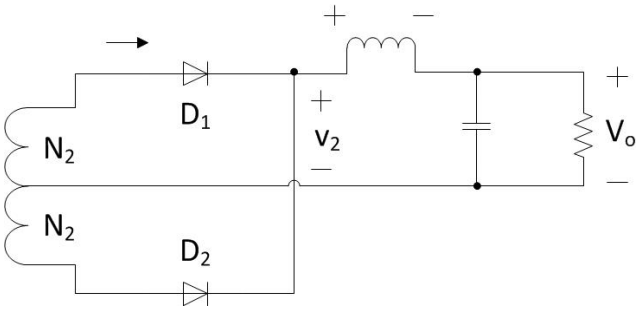


Figure 2.3: Half-bridge circuit during the time Δ

The voltage v_2 equals zero hence,

$$v_L = -V_o \qquad \text{if } t_{on} < t < t_{on} + \Delta \tag{2.2}$$

The average value of v_L can be computed as follows

$$\begin{aligned} v_{L,av} &= \frac{2}{T_s}\int_0^{T_s/2} v_L dt \\ &= \frac{2}{T_s}\int_0^{t_{on}} v_L dt + \frac{2}{T_s}\int_{t_{on}}^{t_{on}+\Delta} v_L dt \\ &= \left(\frac{N_2}{N_1}\frac{V_d}{2} - V_o\right) t_{on} - V_o\Delta \end{aligned} \tag{2.3}$$

where $\frac{T_s}{2}$ is the period and is equal to $t_{on} + \Delta$.

Defining $D = \frac{t_{on}}{T_s}$ and equating $v_{L,av}$ to zero in (2.3) gives

$$t_{on}\frac{N_2}{N_1}\frac{V_d}{2} = V_o(t_{on} + \Delta)$$

and therefore,

$$D\frac{N_2}{N_1}\frac{V_d}{2} = \frac{V_o}{V_d} \tag{2.4}$$

Equation (2.4) is used for the computation of the average value of v_2 as

$$\begin{aligned} v_{2,av} &= \frac{2}{T_s}\int_0^{T_s/2} v_2 dt \\ &= \frac{2}{T_s}\int_0^{t_{on}} v_2 dt + \frac{2}{T_s}\int_{t_{on}}^{t_{on}+\Delta} v_2 dt \\ &= \frac{2}{T_s}\int_0^{t_{on}} \frac{N_2}{N_1}\frac{V_d}{2} dt \\ &= D\frac{N_2}{N_1}V_d \\ &= V_o \end{aligned} \tag{2.5}$$

2.1.2 Mosfet

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are special kinds of Field-Effect Transistors (FETs) that has gradually replaced the Bipolar Junction Transistors (BJTs) especially for the applications where quick switchings are required. In particular, they are used in Complementary Metal Oxide Semiconductor (CMOS) technology which demands less energy than Transistor-Transistor Logic (TTL) technology.

As all FETs, they use an electric field to command the conductivity of a channel (composed of one type of charge carrier) of a semiconductor material. The current through the output terminals of the transistor is driven by applying a signal to the gate.

Figure 2.4 shows the different layers of a MOSFET.

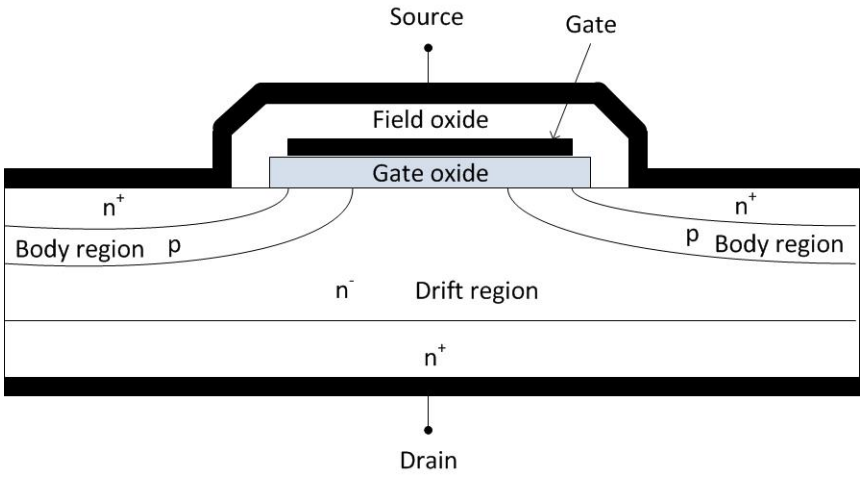
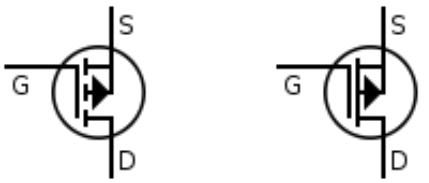


Figure 2.4: MOSFET structure [1] (cross-section)

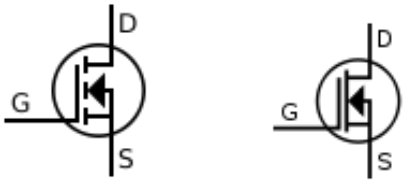
There are two classes of MOSFETs: enhancement-mode and depletion-mode MOSFETs. In depletion-mode (the less common class of MOSFETs), the transistor is normally ON [4]: even without a gate-source voltage, the transistor is a conductor. MOSFETs can be divided into two other groups according to the type of charge carriers put in the channel (2.4). nMOSFETS are made with an n-type channel and pMOSFETs with a p-type channel.

Figure 2.5 presents the different symbols used to represent a MOSFET.



(a) p-type, enhancement-mode

(b) p-type, depletion-mode



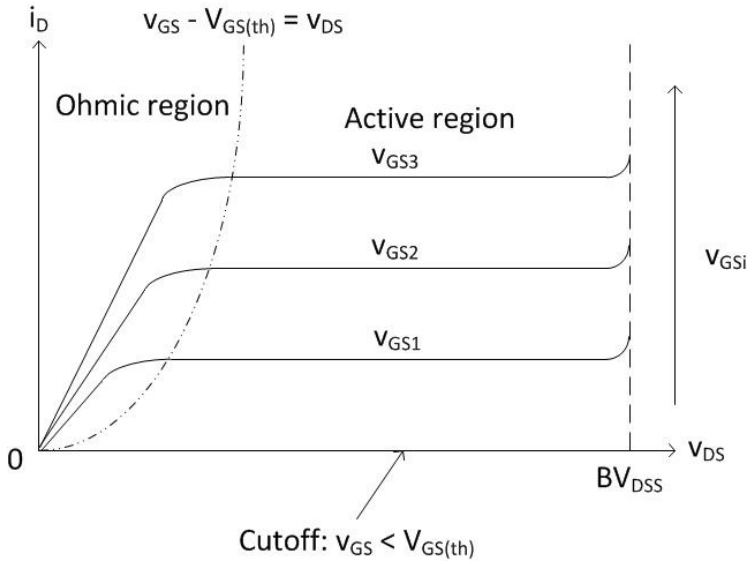
(c) n-type, enhancement-mode

(d) n-type, depletion-mode

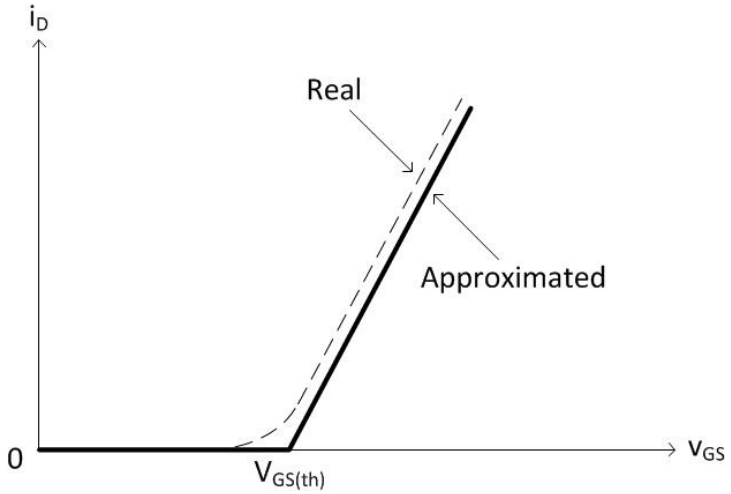
Figure 2.5: The different symbols for each type of MOSFETs [5]

2.1.3 Current-voltage characteristics of an nMOSFET in enhancement mode

Two principal graphs can provide a good understanding of the behavior of a MOSFET: the output characteristic (Figure 2.6(a)) and the transfer curve (Figure 2.6(b)).



(a) $i_D - v_{DS}$ characteristics



(b) Transfer curve

Figure 2.6: I-V characteristics of an nMOSFET in enhancement mode [1]

The first graphic (Figure 2.6(a)) can be split into three regions: cutoff, ohmic region and active region.

Cutoff occurs when v_{GS}, the gate-source voltage, is lower than $V_{GS(th)}$, the so called threshold voltage. This value is usually a few volts for power MOSFETs.

Once v_{GS} is higher than $V_{GS(th)}$, the MOSFET is either in the ohmic region or in the active region depending on whether v_{DS}, the drain-source voltage, is higher or lower than the difference between v_{GS} and $V_{GS(th)}$.

In the active region, v_{DS} is higher than the difference between v_{GS} and $V_{GS(th)}$. The drain current does not depend on v_{DS} anymore but on v_{GS}, according to

$$i_D = K(v_{GS} - V_{GS(th)})^2 \tag{2.6}$$

However, as it can be seen in Figure 2.6(b), (2.6) is valid only at low values of the drain current. Otherwise, the drain current varies linearly with the gate-source voltage. Actually, (2.6) is well-followed by logic-level MOSFETs [1]. The power MOSFETs' behavior in the active region is better represented by the transfer curve shown on Figure 2.6(b).

BV_{DSS} in Figure 2.6(a) is called the breakdown voltage. Over that voltage, the drain-body junction of the MOSFET suffers an avalanche breakdown [1] which can damage the device [6].

Finally, pMOSFETs have the same behavior except for the sign of the different currents and voltages [4].

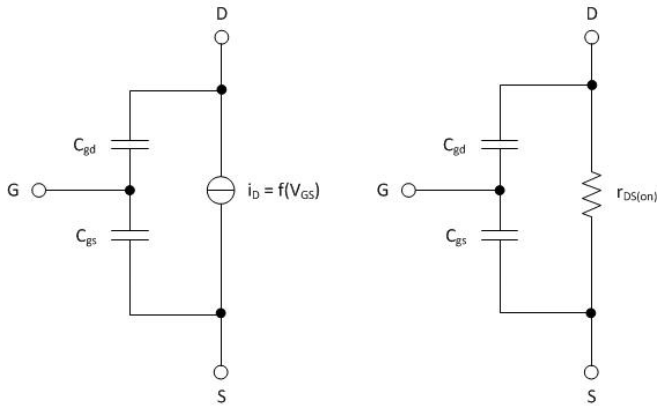
2.1.4 Circuit models for the study of the switching process in MOSFETs [1]

To investigate the switching process in MOSFETs, it is of importance to model the transistor. The circuit models are based on the parasitic capacitances existing between the different terminals of the MOSFET (gate, drain and source) and on the region where the MOSFET is operating. Usually, the charge accumulation is modeled with three stray capacitances: the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd} and the drain-source capacitance C_{ds}. The latest is not part of the different circuit models since it has no influence on the switching characteristics or waveforms.

Two circuit models will be used for the study of the switching process in MOSFETs: one is valid for cutoff and the active region (Figure 2.7(a)) and the other one is used for the ohmic region (Figure 2.7(b)).

The current source shown in the first model (Figure) is driven by the gate voltage. In cutoff state ($v_{GS} < V_{GS(th)}$), the current source is zero. In the active region, it is equal to: $g_m(v_{GS} - V_{GS(th)})$. g_m is called the transconductance and is the slope of the transfer characteristic (Figure 2.6(b)).

For the ohmic region, the current source is replaced in the equivalent circuit by a resistance: the on-state resistance $r_{DS(on)}$. It represents the ohmic losses, essentially



(a) Cutoff and active region (b) Ohmic region

Figure 2.7: The different models for power MOSFETs [1]

coming from the drain drift region of the device and a bit from the channel.

2.1.5 Switching waveforms for MOSFETs

In this section, the switching waveforms of a MOSFET embedded in a converter such as described in Figure 2.8 will be studied.

The MOSFET is replaced by its equivalent transient model which is composed of the capacitances C_{gd} and C_{gs} and either a current source in the active region or the on-state resistance $r_{DS(on)}$ in the ohmic region. C_{ds} is not represented because it is not very essential for the establishment of the switching waveforms. C_{gs} is assumed to be constant. As the voltage change across C_{gd} is much more important than the one in C_{gs}, C_{gd} cannot be considered as a constant [1]. A simple hypothesis is to approximate C_{gd} by two constant values: C_{gd1} and C_{gd2}. In the ohmic region ($v_{DS} < v_{GS}$), C_{gd} is equal to C_{gd2}. In the active region, it is equal to C_{gd1}.

The free-wheeling diode D_f is not ideal: it has a reverse-recovery current I_{rr}.

Turn-on process [1]

The turn-on waveforms can be seen in Figure 3.6(a).Between t_0 and t_1, the gate-source voltage, which was initially zero, reaches the threshold voltage $V_{GS(th)}$ as V_{GG} is applied to the gate. This time is called the turn-on delay time $t_{d(on)}$. The current flows through the free-wheeling diode D_f and the capacitances C_{gd} and C_{gs}. Therefore, the gate-source voltage rises exponentially with the time constant: $\tau_1 = R_g(C_{gs} + C_{gd1})$. The following equations apply during the turn-on delay time,

$$i_{GS} = \frac{V_{GG} - v_{GS}}{R_g} = C_{gs}\frac{dv_{GS}}{dt} - C_{gd1}\frac{d(V_{GG} - v_{GS})}{dt} \tag{2.7}$$

Equation (2.7) leads to the differential equation

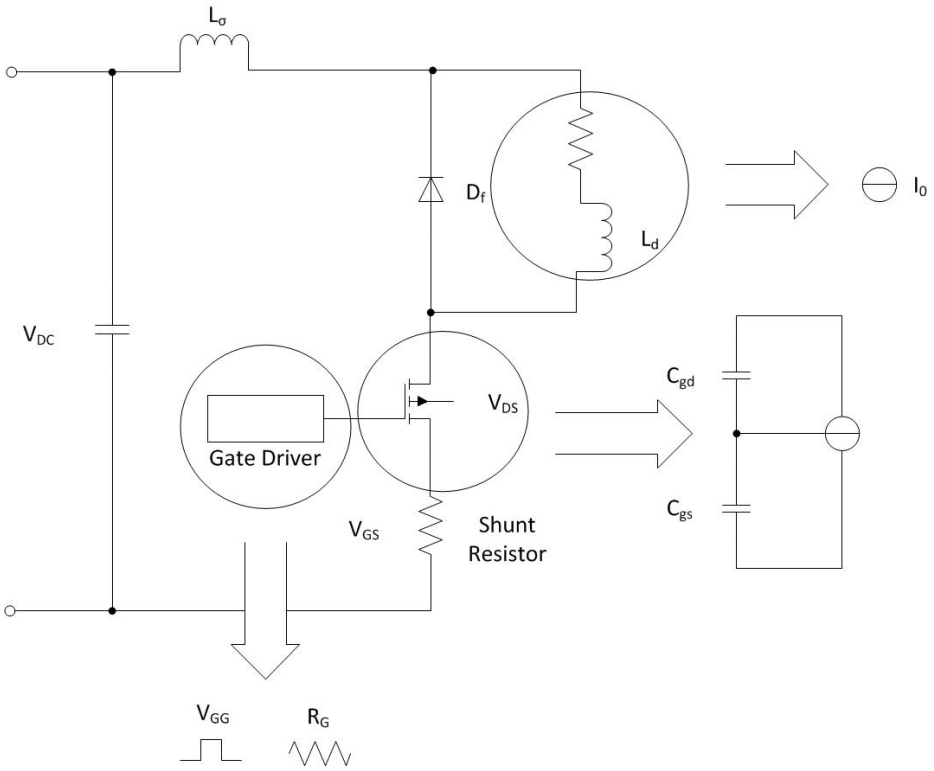


Figure 2.8: Modeling circuit for the analysis of the switching process [2]

$$\frac{dv_{GS}}{dt} = -\frac{v_{GS}}{\tau_1} + \frac{V_{GG}}{\tau_1} \tag{2.8}$$

The solution of (2.8) is

$$v_{GS} = V_{GG}\left(1 - e^{-\frac{t-t_0}{\tau_1}}\right) \tag{2.9}$$

The turn-on delay time can be inferred from (2.9) by noticing that $v_{GS}(t_1) = V_{GS(th)}$ which gives

$$t_{d(on)} = -\tau_1 ln\left(1 - \frac{V_{GS(th)}}{V_{GG}}\right) \tag{2.10}$$

Once V_{GG} is equal to $V_{GS(th)}$ at time t_1, the drain current i_{DS} starts to rise linearly until it reaches $I_0 + I_{rr}$ at time t_2. This time interval is referred to as the current rise time t_{ri}. Meanwhile, v_{GS} keeps on increasing exponentially with the same time constant as above. The drain-source voltage v_{DS} suffers a little drop due to the increase of the drain current and then it remains identical at V_{DC} until i_{DS} reaches $I_0 + I_{rr}$. The new equations that are valid during the current rise time are

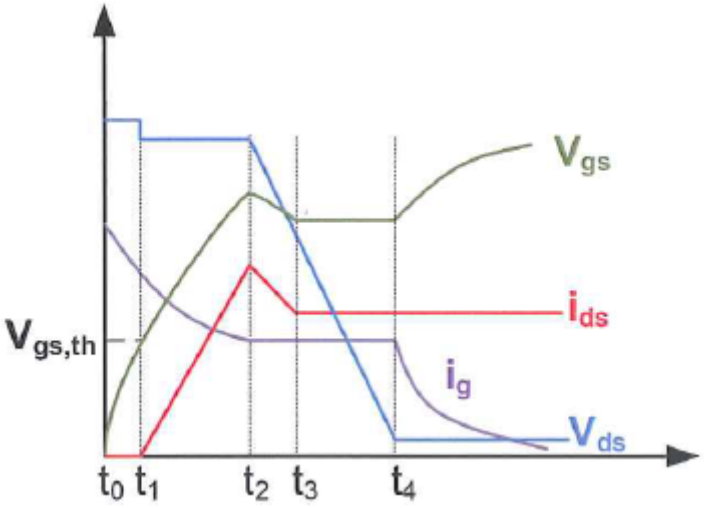


Figure 2.9: MOSFET turn-on waveforms [2]

$$v_{DS} = V_{DC} - (L_\sigma + L_d)\frac{di_{DS}}{dt} \tag{2.11}$$

and

$$i_{DS} = g_m(v_{GS} - V_{GS(th)}) \tag{2.12}$$

The current rise time can be computed as explained in [7] as

$$t_{ri} = -\tau_1 ln\left(\frac{g_m(V_{GG} - V_{GS(th)})}{g_m(V_{GG} - V_{GS(th)}) - (I_0 + I_{rr})}\right) \tag{2.13}$$

At time t_2, the free-wheeling diode switches off. i_{DS} and v_{GS} decrease until i_{DS} reaches I_0 when the free-wheeling diode recovers to zero. v_{GS} drops from $V_{GS(th)} + \frac{I_0 + I_{rr}}{g_m}$ to $V_{GS(th)} + \frac{I_0}{g_m}$.

At time t_3, the drain-source current becomes constant and remains at I_0 until the end of the turn-on process. The gate-source voltage is temporarily constant. The gate current is also constant and flows completely through C_{gd1} first, and then through C_{gd2} when the MOSFET enters the ohmic region. The drain-source voltage can be calculated from the next equation as

$$i_{GS} = -C_{gd}\frac{dv_{DS}}{dt} = \frac{V_{GG} - V_{GS,I_0}}{R_G} \tag{2.14}$$

where, V_{GS,I_0} is the gate-source voltage corresponding to the drain-source current I_0 which can be deduced from Figure 2.6(b). Hence,

$$v_{DS} = -\frac{V_{GG} - V_{GS,I_0}}{R_G C_{gd}}(t - t_2) + V_{dc} \tag{2.15}$$

In (2.15), C_{gd} should be replaced by C_{gd1} in the active region and C_{gd2} in the ohmic region (this change occurs between time t_3 and time t_4). However, in Figure 3.6(a), it is taken as a constant from time t_2 to time t_4.

The drain-source voltage drops until it reaches its on-state value $r_{DS(on)}I_0$. It remains constant while the gate-source voltage begins to increase exponentially again with the time constant $\tau_2 = R_g(C_{gs} + C_{gd2})$. The MOSFET is said to be in its steady state mode.

Turn-off process [2]

Basically, the turn-off process follows the same principle as the turn-on process but in the opposite way. The turn-off waveforms of a MOSFET are represented in Figure 3.6(b).

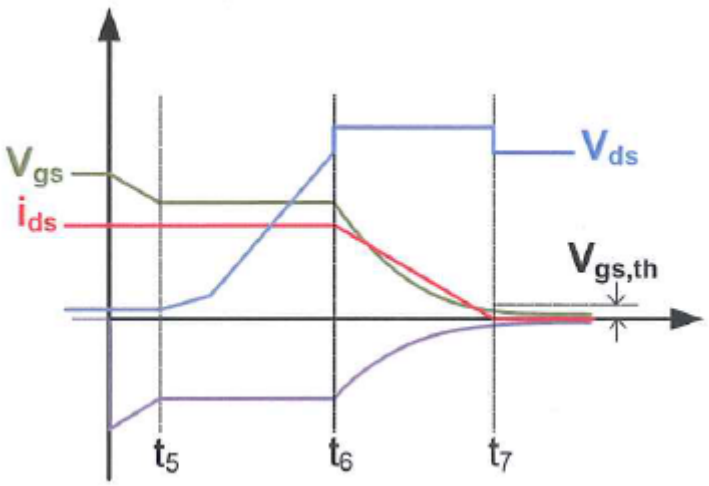


Figure 2.10: MOSFET turn-off waveforms [2]

The MOSFET switches off when the gate-source voltage starts decreasing. This causes the gate-source C_{gs} and the gate-drain C_{gd} capacitors to discharge through the resistance R_G. The equations valid until time t_5 are

$$i_{GS} = \frac{-V_{GS}}{R_G} = (C_{gs} + C_{gd2})\frac{dv_{GS}}{dt} \tag{2.16}$$

and

$$v_{GS} = V_{GG}e^{-(t-t_i)/\tau_2} \tag{2.17}$$

where t_i is the time when the turn-off process starts. Note that the gate driver source is now zero and not V_{GG} anymore.

v_{GS} stops falling when it reaches the value V_{GS,I_0} and remains at this value until time t_6, giving,

$$v_{GS,I_0} = \frac{I_0}{g_m} + V_{GS(th)} \tag{2.18}$$

The time between t_i and t_5 can be calculated using (2.17) and (2.18), giving

$$v_{GS}(t_5) = v_{GS,I_0} = \frac{I_0}{g_m} + V_{GS(th)} = V_{GG}e^{-(t_5-t_i)/\tau_2} \tag{2.19}$$

Thus,

$$t_{d(off)} = t_5 - t_i = \tau_2 ln\left(\frac{V_{GG}}{\frac{I_0}{g_m} + V_{GS(th)}}\right) \tag{2.20}$$

From t_5 to t_6, the drain-source current i_{DS} is also constant and is equal to I_0.

As v_{GS} is constant, all the current comes from the capacitance C_{gd} and the gate current can be expressed as follows,

$$i_{GS} = C_{gd}\frac{dV_{GD}}{dt} = C_{gd}\frac{d(V_{DS} - V_{GS})}{dt} = -C_{gd}\frac{dV_{DS}}{dt} \tag{2.21}$$

From (2.21) and knowing that $i_{GS} = -\frac{v_{GS}}{R_G} = -\frac{\frac{I_0}{g_m} + V_{GS(th)}}{R_G}$, the drain-source voltage can be derived,

$$v_{DS} = \frac{\frac{I_0}{g_m} + V_{GS(th)}}{R_G C_{gd}}(t - t_5) + K \tag{2.22}$$

Where K is the on-state value of the drain-source voltage: $r_{DS(on)}I_0$ and C_{gd} is first equal to C_{gd2} and then to C_{gd1}.

The drain-source voltage v_{DS} rises until it is equal to the dc voltage v_{dc} at time t_6. Then, the free-wheeling diode turns on and the drain-source current i_{DS} begins to decrease. The following equations describe the drain-source current and the gate-source voltage during the interval of time t_6 to t_7,

$$i_{DS} = g_m(v_{GS} - V_{GS(th)}) \tag{2.23}$$

$$v_{GS} = \left(\frac{I_0}{g_m} + V_{GS(th)}\right)e^{-(t-t_6)/\tau_1} \tag{2.24}$$

Equation (2.24) is derived from

$$i_{GS} = -\frac{v_{GS}}{R_G} = (C_{gd1} + C_{gs})\frac{dv_{GS}}{dt} = \tau_1\frac{dv_{GS}}{dt} \tag{2.25}$$

and

$$v_{GS}(t_6) = -\frac{I_0}{g_m} + V_{GS(th)} \tag{2.26}$$

One can derive the current fall time t_{fi} using (2.24) at time t_7, and then

$$v_{GS}(t_7) = \left(\frac{I_0}{g_m} + V_{GS(th)}\right) e^{-t_{fi}/\tau_1} \tag{2.27}$$

Hence,

$$t_{fi} = \tau_1 ln \frac{V_{GS,I_0}}{V_{GS(th)}} \tag{2.28}$$

Note that the step of voltage shown in Figure 3.6(b) on the drain-source voltage curve is due to the parasitic inductance L_σ,

$$v_{DS} = V_{dc} + (L_\sigma + L_d)\frac{di_{DS}}{dt} \tag{2.29}$$

Moreover, the slope of i_{DS} between t_6 and t_7 is $\dfrac{-I_0}{t_{fi}}$.

Finally, the MOSFET is completely switched off when v_{GS} goes under the threshold voltage $v_{GS(th)}$.

2.1.6 Approximate modeling of the switching losses

For this model, the overshoot in v_{DS} shown in Figure 3.6(a) and Figure 3.6(b) is not considered. However, the reverse recovery of the free-wheeling diode occurring during the turn-on process is taken into account.

Considering Figure 3.6(a) and the assumptions made above, the turn-on switching loss energy is derived as follows,

$$
\begin{aligned}
E_{on} &= \int_{t_1}^{t_2} v_{DS} i_{DS} dt + \int_{t_2}^{t_3} v_{DS} i_{DS} dt + \int_{t_3}^{t_4} v_{DS} i_{DS} dt \\
E_{t_1-t_2} &= V_{dc} \frac{I_0 (t_2 - t_1)}{2} \\
E_{t_2-t_3} &= V_{dc}(t_3 - t_2) \left(I_0 + I_{rr} - \frac{I_{rr}}{2} \right) = V_{dc}(t_3 - t_2) \left(I_0 + \frac{I_{rr}}{2} \right) \\
E_{t_3-t_4} &= \int_{t_3}^{t_4} v_{DS} i_{DS} dt \\
&= \int_{t_3}^{t_4} \left(\frac{V_{DS(on)} - V_{dc}}{t_4 - t_3} (t - t_3) + V_{dc} \right) \left(\frac{-I_{rr}}{t_4 - t_3} (t - t_3) + I_0 + I_{rr} \right) \\
&= (t_4 - t_3) \left(\frac{V_{dc} I_{rr}}{3} - \frac{V_{DS(on)} I_{rr}}{3} + \frac{V_{DS(on)} I_0}{2} + \frac{V_{DS(on)} I_{rr}}{2} + \frac{V_{dc} I_0}{2} \right) \\
&\approx (t_4 - t_3) V_{dc} \left(\frac{I_0}{2} + \frac{I_{rr}}{3} \right) \text{ since } V_{dc} >> V_{DS(on)} \\
E_{on} &= V_{dc} \frac{I_0 (t_2 - t_1)}{2} + V_{dc}(t_3 - t_2) \left(I_0 + \frac{I_{rr}}{2} \right) + (t_4 - t_3) V_{dc} \left(\frac{I_0}{2} + \frac{I_{rr}}{3} \right)
\end{aligned}
\tag{2.30}
$$

The switching losses calculations during turn-off process are made considering Figure 3.6(b) and the following assumption: v_{DS} linearly rises from zero to V_{dc}. Thus,

$$
\begin{aligned}
E_{off} &= \int_{t_5}^{t_6} v_{DS} i_{DS} dt + \int_{t_6}^{t_7} v_{DS} i_{DS} dt \\
&= I_0 \int_{t_5}^{t_6} v_{DS} dt + V_{dc} \int_{t_6}^{t_7} i_{DS} dt \\
&= \frac{1}{2} \times I_0 (t_6 - t_5) V_{dc} + V_{dc}(t_7 - t_6) I_0 \\
&= \frac{1}{2} \times I_0 V_{dc} (t_7 - t_5) \\
&= \frac{1}{2} \times I_0 V_{dc} t_{off}
\end{aligned}
\tag{2.31}
$$

The turn-off switching losses are first calculated for specific $V_{dc,ref}$ and $I_{0,ref}$. Then, for other voltages and currents, they are obtained as follows [2]

$$
E_{on} = E_{on,ref} \left(\frac{V_{dc}}{V_{dc,ref}} \right)^{k_{V,on}} \left(\frac{I_0}{I_{0,ref}} \right)^{k_{I,on}} \tag{2.32}
$$

$$
E_{off} = E_{off,ref} \left(\frac{V_{dc}}{V_{dc,ref}} \right)^{k_{V,off}} \left(\frac{I_0}{I_{0,ref}} \right)^{k_{I,off}} \tag{2.33}
$$

where $k_{V,on}$, $k_{I,on}$, $k_{V,off}$ and $k_{I,off}$ can either be found in the data-sheets or estimated to be one if not presented in the data-sheets.

2.2 R-C circuit

This section aims to establish the equations that govern the behavior of an R-C circuit (Figure 2.11).

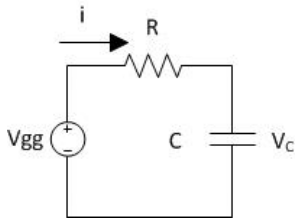


Figure 2.11: R-C circuit

First, Kirchhoff's law gives

$$V_{gg} - Ri - V_C = 0$$

As $i = C\frac{dV_C}{dt}$, the equation above becomes

$$V_{gg} - RC\frac{dV_C}{dt} - V_C = 0$$

Thus, the following differential equation is obtained as follows,

$$V_C' + \frac{V_C}{RC} = \frac{V_{gg}}{RC} \tag{2.34}$$

The solution of (2.34) can be written as the sum of the solution of the homogeneous equation and a particular solution of the complete equation. Hence,

$$V_C = V_{C,h} + V_{C,p} \tag{2.35}$$

2.2.1 Homogeneous solution

The homogeneous equation is

$$RCV_C' + V_C = 0 \tag{2.36}$$

which gives

$$\frac{dV_C}{V_C} = -\frac{dt}{RC}$$

and,

$$d(ln(V_C)) = -\frac{1}{RC}dt$$

After integration, the result is

$$ln(V_C) = -\frac{1}{RC}t + K$$

where K is a constant.

Finally, the homogeneous solution is

$$V_{C,h} = K' e^{-\frac{t}{RC}} \tag{2.37}$$

where K' is a constant such as $K' = e^K$.

2.2.2 Particular solution

Particular solutions of (2.34) can be written as follows,

$$V_{C,p} = C(t) e^{-\frac{t}{RC}} \tag{2.38}$$

Using (2.38) in (2.34) gives

$$C'(t) = \frac{V_{gg}}{RC} e^{\frac{t}{RC}} \tag{2.39}$$

as $V'_{C,p} = C'(t) e^{-\frac{t}{RC}} - \frac{1}{RC} C(t) e^{-\frac{t}{RC}}$.

Thus, $C(t)$ can be chosen as

$$C(t) = V_{gg} e^{\frac{t}{RC}} \tag{2.40}$$

So, a particular solution can be

$$V_{C,p} = C(t) e^{-\frac{t}{RC}} = V_{gg} \tag{2.41}$$

2.2.3 General solution

The solution of the complete equation (2.34) is obtained thanks to (2.35), (2.37) and (2.41), giving,

$$V_C = K' e^{-\frac{t}{RC}} + V_{gg} \tag{2.42}$$

The initial condition on V_C is: $V_C(0) = V_{gg,min}$ so the constant K' is equal to $V_{gg,min} - V_{gg}$ and the solution of the general equation becomes

$$V_C = (V_{gg,min} - V_{gg})e^{-\frac{t}{RC}} + V_{gg} \tag{2.43}$$

2.2.4 Time constant

The time constant of the R-C circuit is defined as

$$\tau = RC \tag{2.44}$$

At the time $t = \tau$, the voltage across the capacitor is

$$\begin{aligned} V_C(\tau) &= (V_{gg,min} - V_{gg})e^{-1} + V_{gg} \\ &\approx 0{,}37 \times V_{gg,min} + 0{,}63 \times V_{gg} \end{aligned} \tag{2.45}$$

2.2.5 Current

Once the voltage over the capacitor is determined with (2.43), the current can be computed as follows

$$\begin{aligned} i &= C\frac{dV_C}{dt} \\ &= C\frac{d\left((V_{gg,min} - V_{gg})e^{-\frac{t}{RC}} + V_{gg}\right)}{dt} \\ &= \frac{1}{R}(V_{gg} - V_{gg,min})e^{-\frac{t}{RC}} \end{aligned} \tag{2.46}$$

2.3 PCB design

2.3.1 Tracing of the tracks [3]

Two parameters are really important regarding the tracing of the tracks in a circuit board: the space between two tracks and the width of the tracks.

If the tracks are too close to each other, as no material is completely insulating, a leakage current could appear. Graphics representing the distance between two tracks over the nominal voltage between the tracks can be easily found. It also gives the corresponding disruptive voltage.

The width of the tracks depends on the current and the thickness of the copper layer. Graphics giving the width of the tracks as a function of the current and the thickness of the copper layer also exist.

2.3.2 Mechanical and thermal conditions [3]

A common issue with circuit boards is the separation of the tracks from the board. To avoid a lack of adherence, it is advisable to increase the tracks width.

The same problem may occur with the pads. To prevent this problem from happening, it is possible to increase the ratio $\phi_{pad}/\phi_{drillhole}$, to use square pads (more adherence for the same space) or to metallize the drill-holes (which decreases ϕ_{pad}).

When the temperature gets higher, the circuit board may be damaged. That is why it is, in certain cases, good to criss-cross the ground plane as it reduces the distortions caused by high temperatures (dilatation).

Finally, when soldering, it may be difficult to heat the pads when they are connected to large tracks or to the ground plane. That is the reason why thermal pads are sometimes used.

2.3.3 Advices for conception and implantation [3]

Here is a non-comprehensive list of advices concerning the placement of the components on the circuit boards:

- First, place the connectors
- Potentiometers requiring screw drivers to be set should be placed at the edge of the board
- It is better to place the components in parallel as much as possible to save place and make it easier to visualize
- Polarized components should be oriented in the same way to avoid insertion mistakes
- Some components may have effects on other components. For instance, a power resistor may reach high temperatures and have an influence on an electrolytic capacitor
- Two components cannot be in contact, otherwise it could induce leakage current or short circuits
- It is also a good idea to gather components according to their functions in the circuit.

Some advices about the rooting step are stated in the following list:

- The conductive pattern should be equally allocated on the circuit board
- Connecting more than two tracks to the same pin should be avoided as much as possible

- Tracks wider than 1cm should be streaked (same reasons as for the ground plane in section2.2.2)
- Loops should be avoided to prevent electromagnetic fields.

2.4 Soldering process

A good soldering is all about solder the components in a logical order and take care of the iron.

Components should be soldered downward in the following order: wires, integrated circuit, resistors and diodes, lain transistors and regulators, small and medium capacitors, connectors, connecting blocks, big capacitors, straight transistors and regulators.

The iron should be well heated before soldering. After soldering, the iron must be cleaned with a damp sponge (never scratch the iron!). Melting down some welding on the end of the iron avoids the oxidation.

2.5 Softwares

This section presents briefly the softwares that have been used throughout this project.

2.5.1 Target 3001

Target is a software used to design PCB. The steps for designing a PCB with target are the following: importation of the components, wiring of the pins, choice of the size of the PCB, importation of the packages, rooting and generating of the ground plane.

2.5.2 Matlab

MATLAB (MATrix LABoratory) is a programming and development software usually used for numerical computing.

2.5.3 Latex

Latex is a language commonly used in the scientific community for the writing of reports.

3

Case set-up

This section presents the model used to describe the switching process in Mosfets and derive the switching losses. It also shows the measurement circuit and how it has been designed. Finally, the measurement process is explained.

3.1 Experimental circuit

3.1.1 Circuit

In order to measure the different times involved in the switching process of the Mosfets and thus compute the switching losses, a special circuit needs to be designed. This circuit must supply and control the Mosfet. Figure 3.1 presents the functionalities that should provide the circuit.

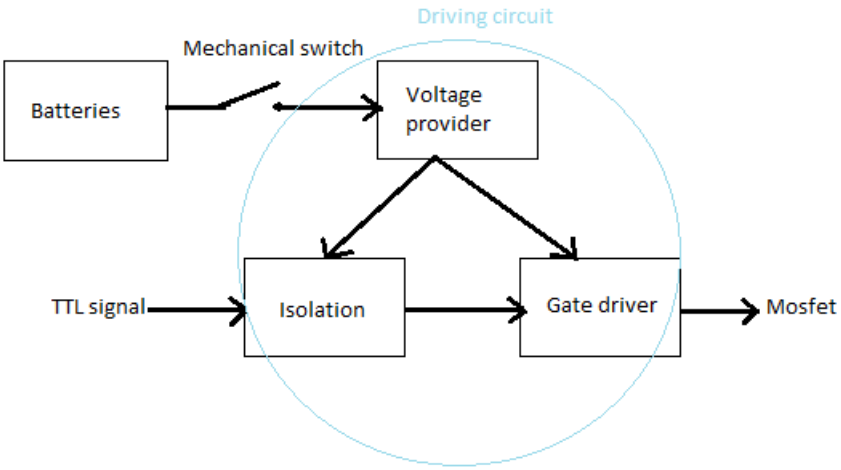


Figure 3.1: Blocks diagram of the measurement circuit

The voltage provider adjusts the voltage given by the 9V-batteries to a suitable level for the isolation and the gate driver stages. The isolation is to make the circuit safer and to avoid ElectroMagnetic Interference (EMI) issues. Finally, the gate driver controls the switchings of the Mosfet.

3.1.2 Design of the circuit

In Figure 3.2, the electric schematic of the measurement circuit is presented.

The power supplier stage contains several capacitors for stabilization purpose: the current has to be as smooth as possible. During switch off, the current flows through the free-wheeling diode FWD1.

The positive voltage supplier is supplied by three 9 V-batteries in series and can deliver a voltage between 1.2 and 25 V thanks to the adjustable regulator [8] and the potentiometer. In reality, a voltage range is needed from 12 V to 20 V. The Zener diode D3 is to protect the isolator stage. It ensures a minimum voltage to the isolator stage.

The negative voltage supplier works roughly in the same way as the positive voltage supplier. The negative regulator [9] can provide voltages between -37 and -1.2 V. However, in this case, only voltages between -4 and 0 V are required. That is why it is supplied by one 9V-battery and diodes D4 and D1 have been added in comparison with the positive voltage supplier.

Resistor R5 and capacitor C3 at the input of the isolation is an R-C filter. The capacitor discharges into the high value resistor R6. The aim of capacitor C4 is to stabilize the voltage.

The input and the output voltage of the driving circuit [10] must not be disrupted which is why there are several capacitors and a filter at the input of this stage.

In some cases, modeling the inductance of the wires (if the wires are long) is needed. Thus, inductors J7 and J8 have been put on the circuit but they might not be used.

In Figure 3.3 the 3D view of the PCB is shown. One requirement while designing the PCB was to make the gate driver stage as compact as possible to avoid disturbances, get the lowest inductance possible and thus make the measurement more accurate. The wires linking the power supplier to the Mosfet should be short for the same reason.

Because the switching frequency may be high, the capacitors should quickly react. Thus ceramic capacitors have been chosen instead of electrolytic capacitors since these are slow.

Finally, the PCB should be designed in such a way to make the measurement easy (measuring devices must fit in the strategical points).

3.1.3 Measurement process

Tests with only R and C

First, the circuit is tested with an R-C load (Figure 3.4(a)). The input signal applied to the gate driver is represented in Figure 3.4(b). Its frequency is 300 Hz.

From the datasheets [11, 12, 13, 14] of the transistors that will be tested later, the values of the internal capacitance and resistance have been found. The capacitance is a few nano Farads and the resistance is a few Ohms. The components have been chosen in order to fit as much as possible to those values. Table 3.1 sums up the different tests that have been done.

Table 3.1: Preliminary tests on the driving circuit

Test	R (Ohm)	C (nF)
1	10 + 1	2.2
2	4.7 + 1	2.2
3	1 + 1	2.2
4	10 + 1	15
5	4.7 + 1	15
6	1 + 1	15

The details about the components used are shown in Table 3.2. Those values come from the datasheets of the components [15, 16, 17, 18, 19].

Table 3.2: Components specifications

Test	R_1 (Ohm)	$\frac{\Delta R_1}{R_1}$ (%)	R_2 (Ohm)	$\frac{\Delta R_2}{R_2}$ (%)	C (nF)	$\frac{\Delta C}{C}$ (%)
1	10	1	1	1	2.2	10
2	4.7	1	1	1	2.2	10
3	1	1	1	1	2.2	10
4	10	1	1	1	15	20
5	4.7	1	1	1	15	20
6	1	1	1	1	15	20

Once the test circuit is set up and run, the experimental time constants τ can be found using (2.45).

Test with a power Mosfet when the drain-source voltage is zero

Several tests are made with a power Mosfet [11] to check the operation of the circuit when used with a Mosfet. The drain and the source are short-circuited so the voltage v_{DS} is equal to zero. When the drain-source voltage is zero, the internal capacitance of the Mosfet can be approximated to be 8.7 nF (Fig. 5 from the datasheet of the component [11]). The value of the internal resistance is unknown. Hence, the first three tests aim

to get an approximate value of the internal resistance of the Mosfet. The circuit is run with three different values of the gate resistor: 4.7, 2.35 and 3.2 Ω. For each case, the time constant τ is determined. Then the internal resistance R_i is computed as

$$R_i = \frac{\tau}{C} - R_g \tag{3.1}$$

Once the internal resistance of the Mosfet is approximately known, the internal capacitance of the Mosfet can be found - more precisely than in the data sheet. A gate resistor much higher than the internal resistance of the Mosfet is used so the effect of the latest is insignificant. The internal capacitance is therefore,

$$C = \frac{\tau}{R_i + R_g} \approx \frac{\tau}{R_g} \tag{3.2}$$

Test with a power Mosfet and an R-L load when the drain-source voltage changes

When the circuit is completely mounted on the PCB, the load part is added. The load is composed of several power resistors in series (1 Ω, 1 Ω and 8 Ω) and a 40 mH inductance. The current through the resistors doesn't exceed 1 A so they don't get heated as the losses over those resistors are Ri^2. The circuit is operated for three different drain-source voltages v_{DS} (10, 20 and 30 V) with a frequency that is about 900 Hz. It is also tested when v_{DS} is zero in order to check the operating of the circuit when the load is added.

Si-Mosfet switching

The switching process is investigated with the same Mosfet and parameters used in Section 3.1.3.

SiC-Mosfet switching

New tests are made with a different Mosfet, an SiC Mosfet [13]. The tests are performed for different DC voltages and different loads, hence for different currents I_0. The frequency is still 900 Hz and the inductance used is about 40 mH. The different cases studied are shown in Table 3.3.

Table 3.3: Tests on an SiC Mosfet

Test	V_{dc} (V)	I_0 (A)	R (Ω)
1	40	1.5	8//8 + 8//8
2	40	3.5	8//8
3	60	1.5	3 × (8//8)
4	60	3.5	8//8 + 8//8//8//8

The values in Table 3.3 are just approximations. Moreover, the resistors used are supposed to be 8 Ω resistors but it's actually about 12 Ω. Finally, those resistors are adjusted such as they don't get heated ($P = Ri^2$).

3.2 Simulation model

3.2.1 Tests with only R and C

The theoretical curve of the charge of the capacitor in the six cases to be studied is drawn using (2.43) and (2.46). The curves obtained are shown in Figure 3.5. These simulations are made using the measured value of the gate voltage V_{gg}

Then, each time constant τ is computed using (2.44). The results are presented in Table 3.4.

Table 3.4: Theoretical time constants

Test	R (Ohm)	C (nF)	τ_{th} (ns)
1	11	2.2	24.2
2	5.7	2.2	12.5
3	2	2.2	4.4
4	11	15	165
5	5.7	15	85.5
6	2	15	30

3.2.2 Si-Mosfet switching

The switching losses are computed for the case when $V_{dc} = 30$ V.

Approximated method

A first approximation of the switching losses of the Mosfet [11] is made based on (2.30) and (2.31). Table 3.5 shows the parameters used for the calculations that are given in the data sheet of the component [11].

Knowing the area Q_{rr} of a triangle and its base t_{rr}, the height I_{rr} can be computed as follows

$$I_{rr} = \frac{2Q_{rr}}{t_{rr}} \approx 22\ A \tag{3.3}$$

Thus, the switching losses for the specific voltage and current given in Table 3.5 are

Table 3.5: Useful parameters of the power Mosfet

Parameter	Symbol	Value
Voltage reference	$V_{DS,ref}$	300 V
Current reference	$I_{DS,ref}$	16 A
Turn-on delay time	$t_{d(on)}$	19 ns
Rise time	t_r	54 ns
Turn-off delay time	$t_{d(off)}$	110 ns
Fall time	t_f	56 ns
Body diode reverse recovery time	t_{rr}	610 ns
Body diode reverse recovery charge	Q_{rr}	6.6 μs

$$\begin{aligned} E_{on,ref} &= 740.6\ \mu J \\ E_{off,ref} &= 132\ \mu J \end{aligned} \tag{3.4}$$

Hence, using (2.32) and (2.33), it gives the values presented in Table 3.6.

Table 3.6: Approximation of the switching losses

ON/OFF	V_{dc} (V)	I_0 (A)	Approximation (μJ)
ON	30	0.8	3.7
OFF	30	0.8	0.66

Simulation

The simulation gives a more accurate prediction of the switching losses since some of the parameters used are taken directly from the measurement. Those parameters are presented in Table 3.10.

The theoretical curves are given for both turn-on and turn-off switching processes in Figure 3.6(a) and Figure 3.6(b). The simulated switching losses during the turning-on are 1.6 μJ and during the turning-off they are 0.12 μJ.

3.2.3 SiC-Mosfet switching

Approximated method

A first approximation of the switching losses of the Mosfet [11] is made based on (2.30) and (2.31). Table 3.8 shows the parameters used for the calculations that are given in the data sheet of the component [13].

Table 3.7: Parameters used for the simulation with the power Mosfet

Parameter	Symbol	Value
Current reference	$I_{DS,ref}$	16 A
Input current	I_0	0.8 A
Reverse recovery current	I_{rr}	3 A
Drain-source voltage	V_{dc}	30 V
Gate voltage	V_{gg}	24 V
Threshold voltage	$V_{GS,th}$	3 V
Input capacitance at low V_{DS}	$C_{iss,lv}$	9.1 nF
Input capacitance at high V_{DS}	$C_{iss,hv}$	3.8 nF
Reverse transfer capacitance at low V_{DS}	$C_{rss,lv}$	4.3 nF
Reverse transfer capacitance at high V_{DS}	$C_{rss,hv}$	50 pF
Drain-source resistance	R_{DS}	1 Ω
Gate resistance	R_g	4.7 Ω

Table 3.8: Useful parameters of the SiC Mosfet

Parameter	Symbol	Value
Voltage reference	$V_{DS,ref}$	400 V
Current reference	$I_{DS,ref}$	10 A
Reverse recovery current	I_{rr}	2.4 A
Turn-on delay time	$t_{d(on)}$	37 ns
Rise time	t_r	33 ns
Turn-off delay time	$t_{d(off)}$	70 ns
Fall time	t_f	28 ns
Body diode reverse recovery time	t_{rr}	37 ns

Then, the switching losses for the specific voltage and current given in Table 3.8 are

$$\begin{aligned} E_{on,ref} &= 307.7\ \mu J \\ E_{off,ref} &= 56\ \mu J \end{aligned} \tag{3.5}$$

Hence, using (2.32) and (2.33), it gives the values presented in Table 3.9.

Table 3.9: Approximation of the switching losses for the SiC Mosfet

ON/OFF	V_{dc} (V)	I_0 (A)	Approximation (μJ)
ON	43	1.6	5.3
OFF	43	1.6	0.96
ON	40	3.8	11.7
OFF	40	3.8	2.1
ON	65	1.6	8.0
OFF	65	1.6	1.5
ON	62	3.8	18.1
OFF	62	3.8	3.3

Simulation

The simulation gives a more accurate prediction of the switching losses since some of the parameters used are taken directly from the measurement. Those parameters are presented in Table 3.10.

Table 3.10: Parameters used for the simulation with an SiC Mosfet

Parameter	Symbol	Value
Current reference	$I_{DS,ref}$	10 A
Reverse recovery current	I_{rr}	2.4 A
Gate voltage	V_{gg}	20 V
Threshold voltage	$V_{GS,th}$	3 V
Input capacitance at low V_{DS}	$C_{iss,lv}$	3.4 nF
Input capacitance at high V_{DS}	$C_{iss,hv}$	2 nF
Reverse transfer capacitance at low V_{DS}	$C_{rss,lv}$	2 nF
Reverse transfer capacitance at high V_{DS}	$C_{rss,hv}$	20 pF
Drain-source resistance	R_{DS}	1 Ω
Gate resistance	R_g	6.5 Ω

The input currents and drain-source voltages are those from Table 3.9.

The theoretical curves are given for both turn-on and turn-off switching processes in Figure 3.7, Figure 3.8, Figure 3.9 and Figure 3.10. The simulated switching losses during the turn-on and during the turn-off are given in Table.

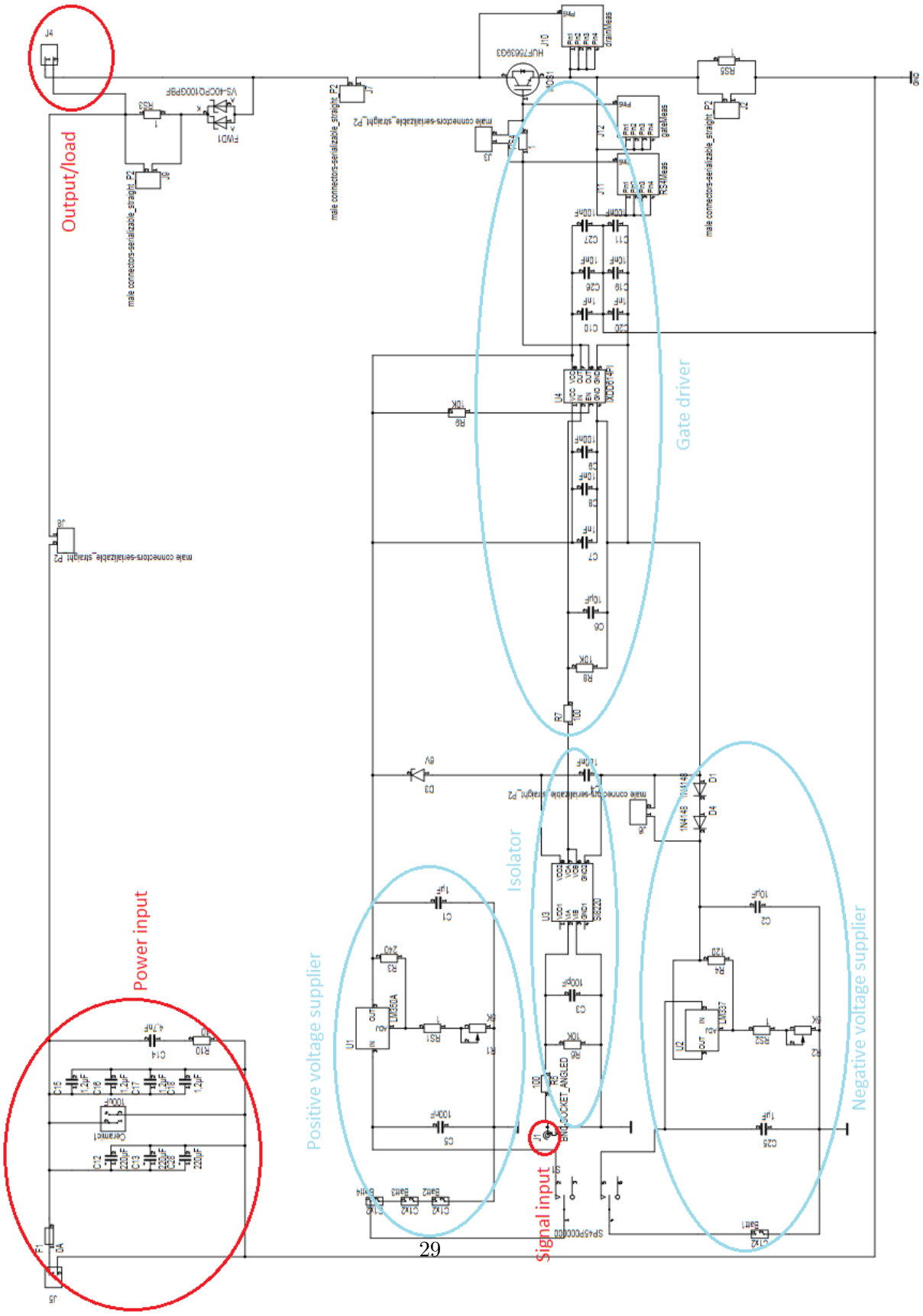
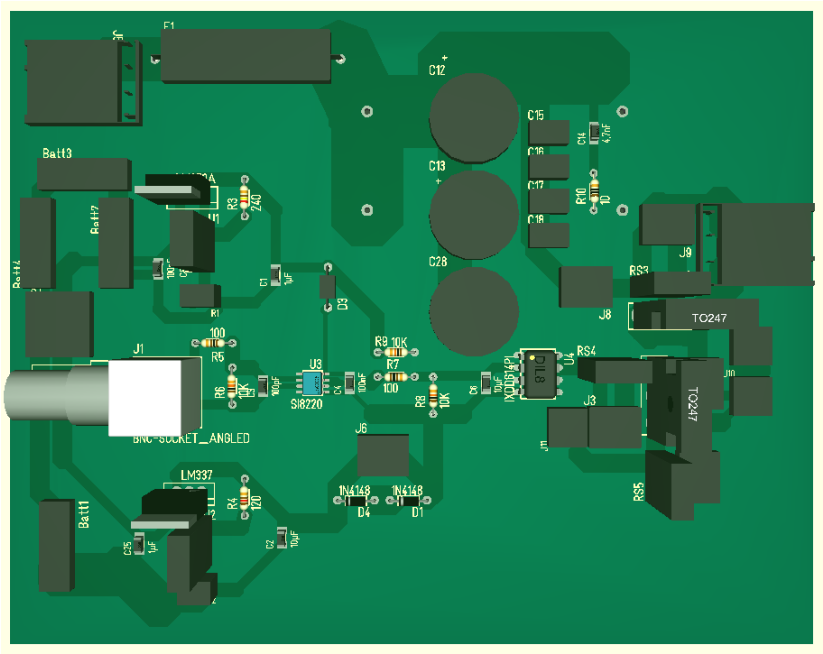
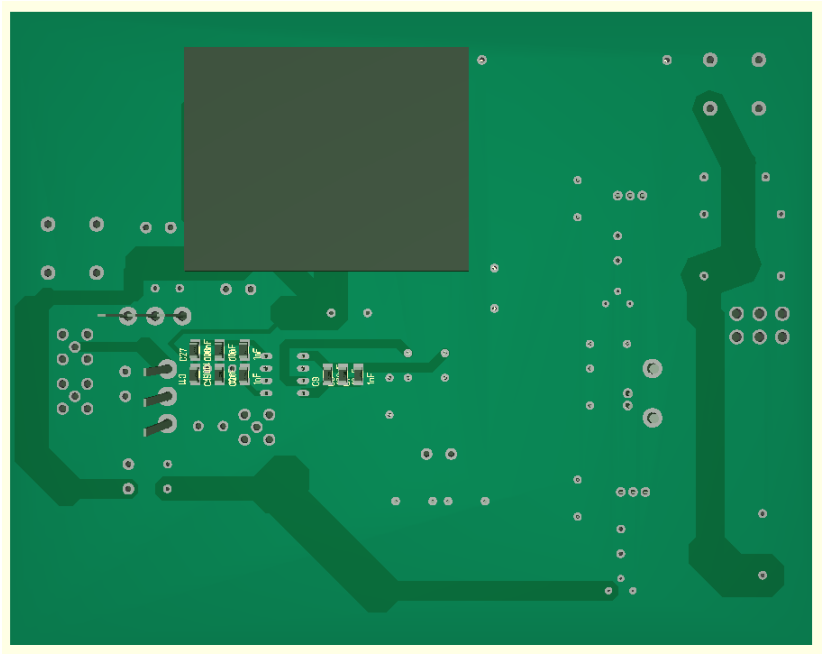


Figure 3.2: Gate driving circuit

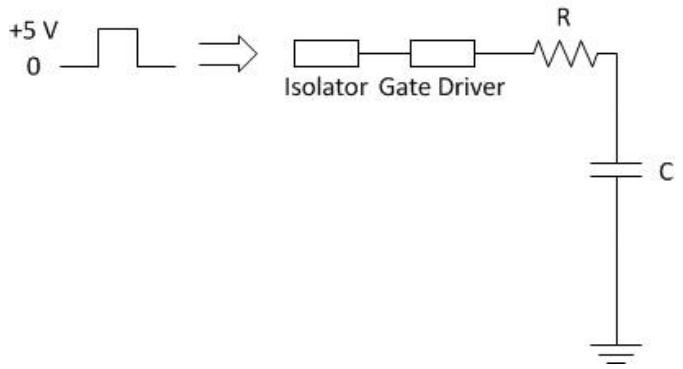


(a) Top

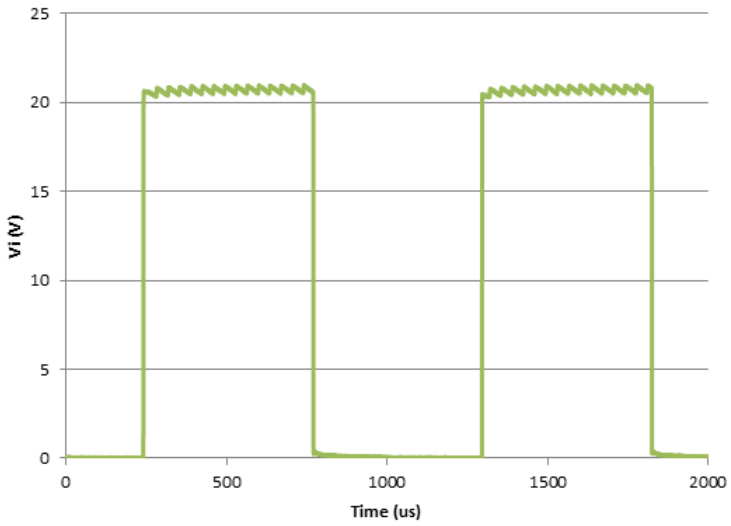


(b) Bottom

Figure 3.3: PCB

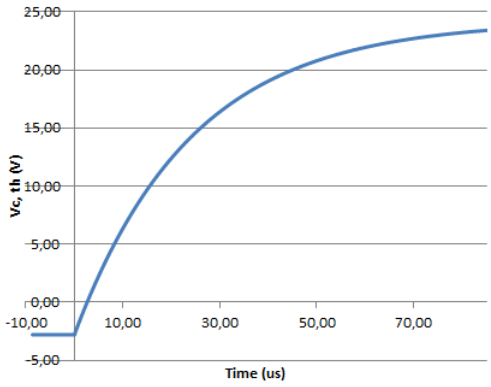


(a) Test circuit

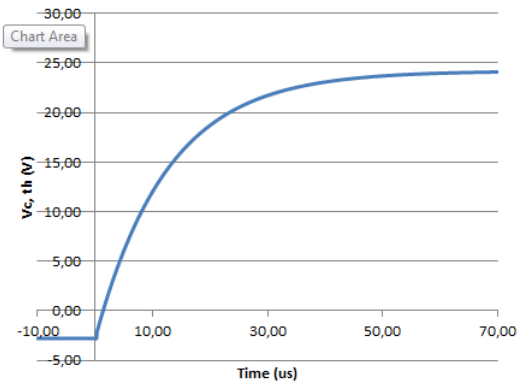


(b) Input signal to the gate driver

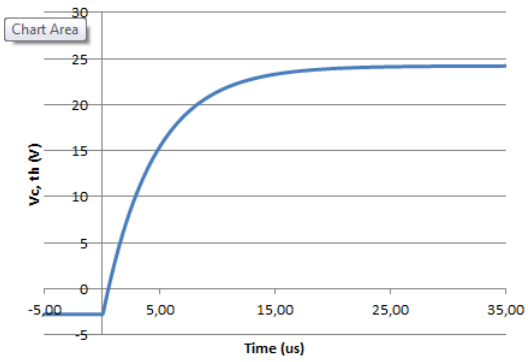
Figure 3.4: Circuit and input signal used for the test on the driving circuit



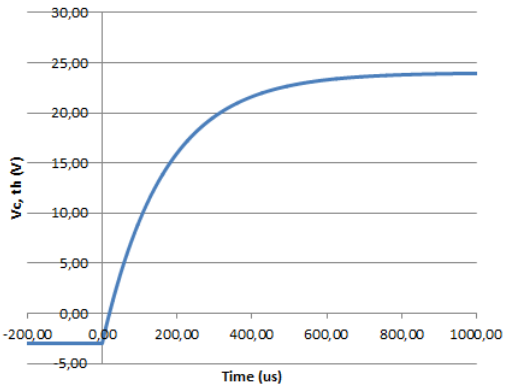
(a) Test 1: $R = 11$ Ohms and $C = 2.2$ nF



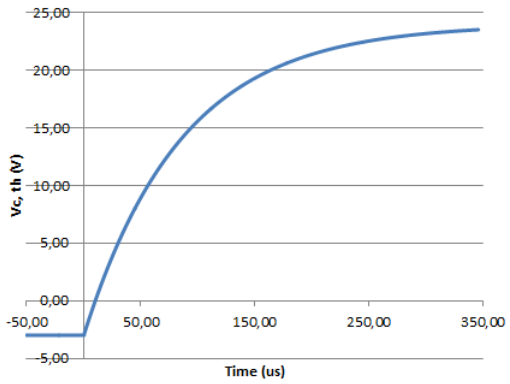
(b) Test 2: $R = 5.7$ Ohms and $C = 2.2$ nF



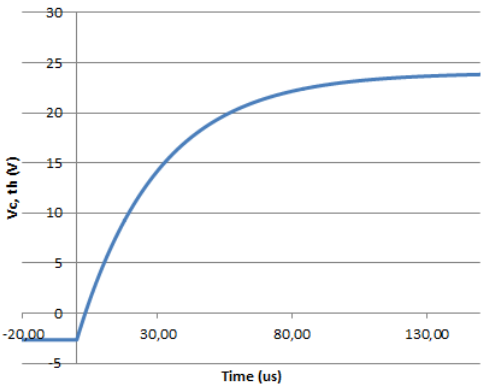
(c) Test 3: $R = 2$ Ohms and $C = 2.2$ nF



(d) Test 4: $R = 11$ Ohms and $C = 15$ nF

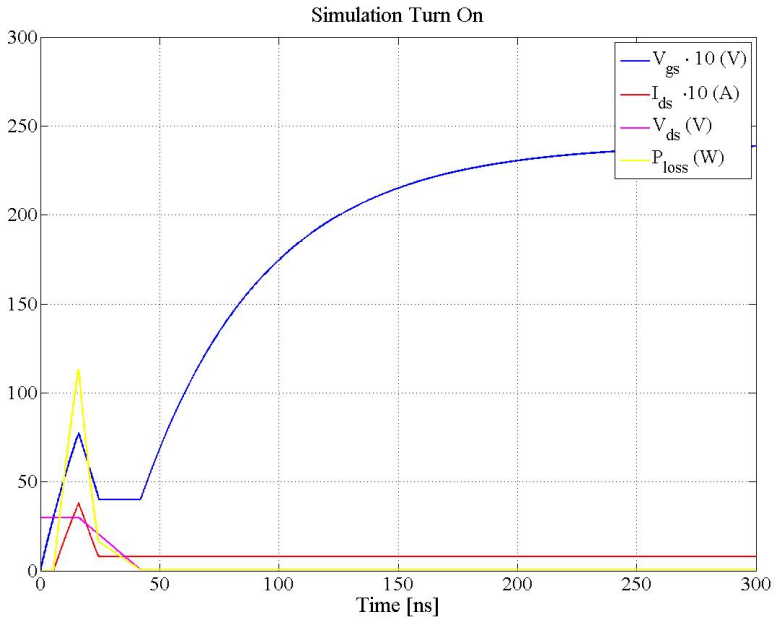


(e) Test 5: $R = 5.7$ Ohms and $C = 15$ nF

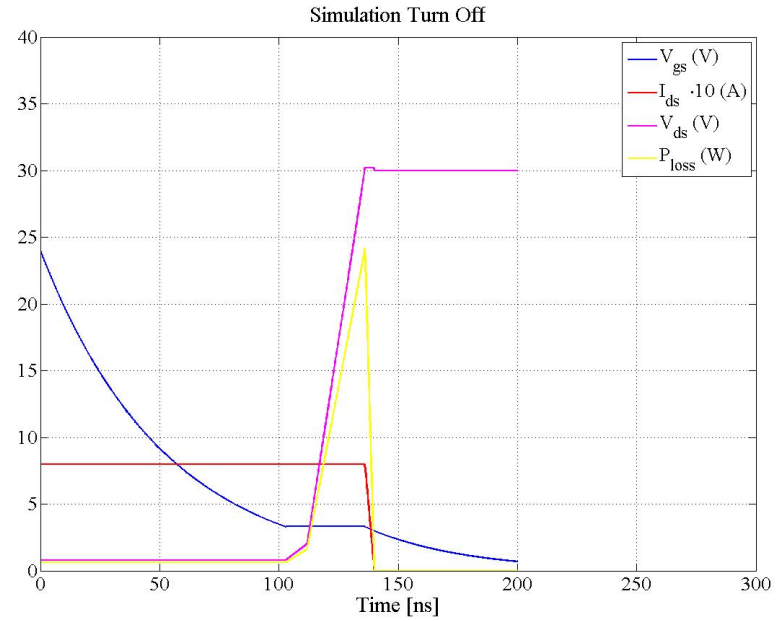


(f) Test 6: $R = 2$ Ohms and $C = 15$ nF

Figure 3.5: Theoretical curves obtained from the different cases to be studied

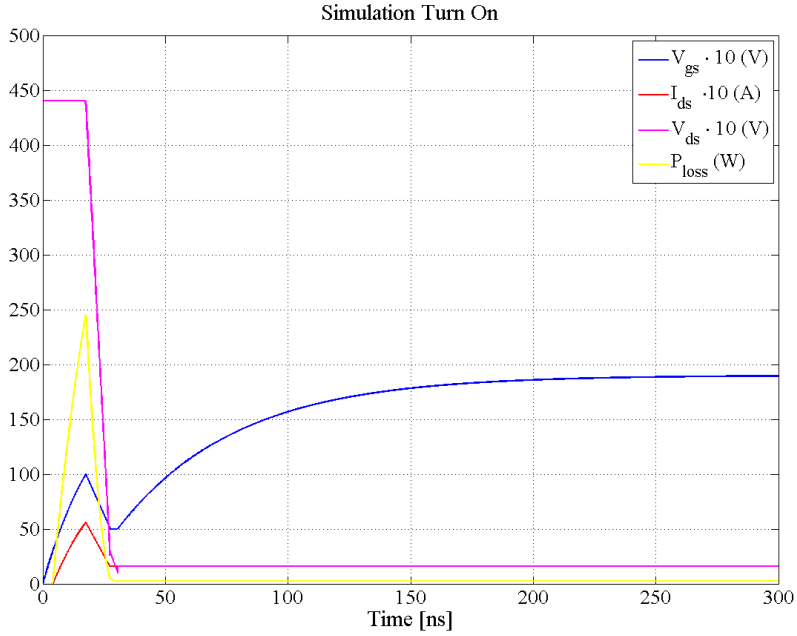


(a) Simulation of the turn-on process

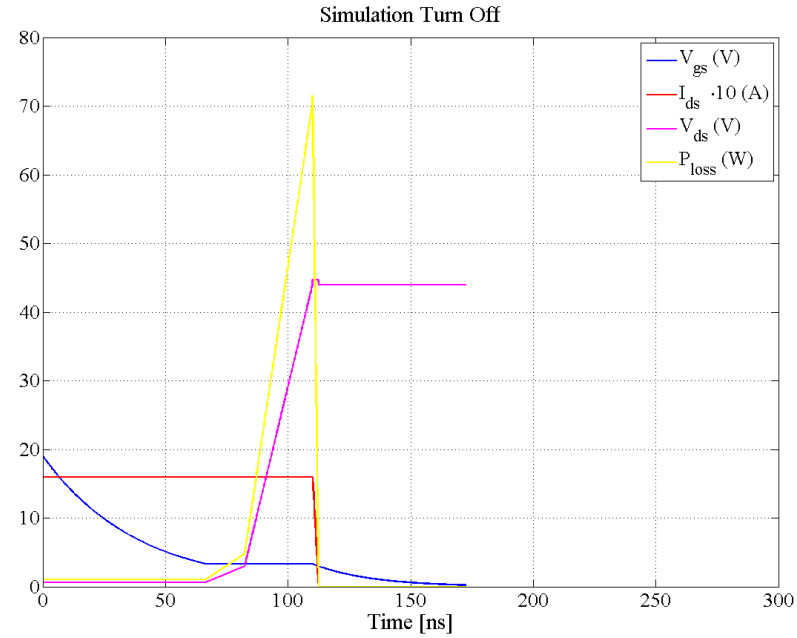


(b) Simulation of the turn-off process

Figure 3.6: Theoretical curves obtained for $V_{dc} = 30$ V and $R_g = 4.7\ \Omega$ for a power Mosfet

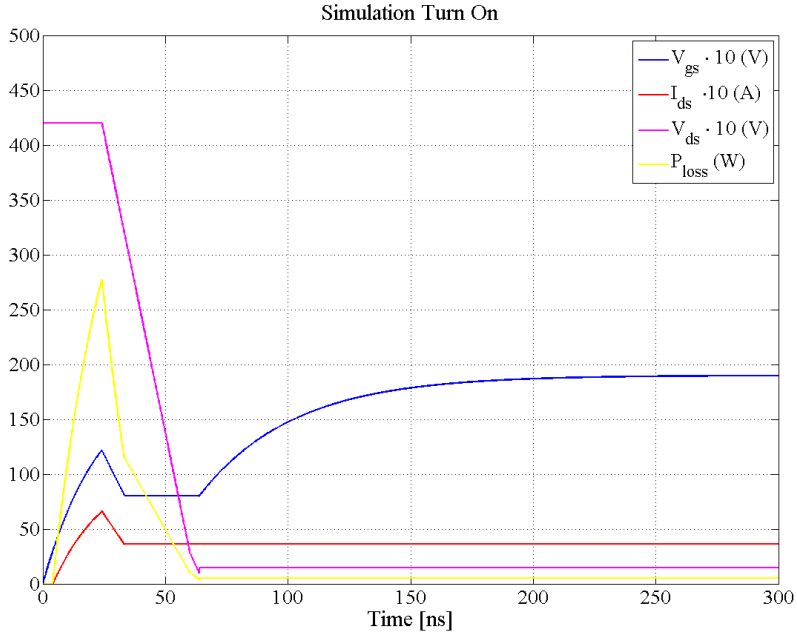


(a) Simulation of the turn-on process

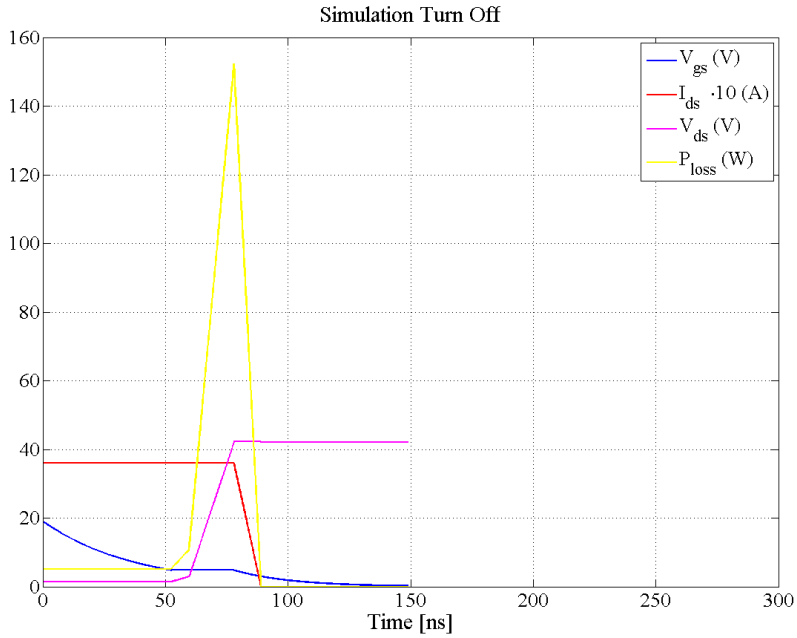


(b) Simulation of the turn-off process

Figure 3.7: Theoretical curves obtained for $V_{dc} \approx 40$ V, $i_0 \approx 1.5$ A and $R_g = 4.7\ \Omega$ for an SiC Mosfet

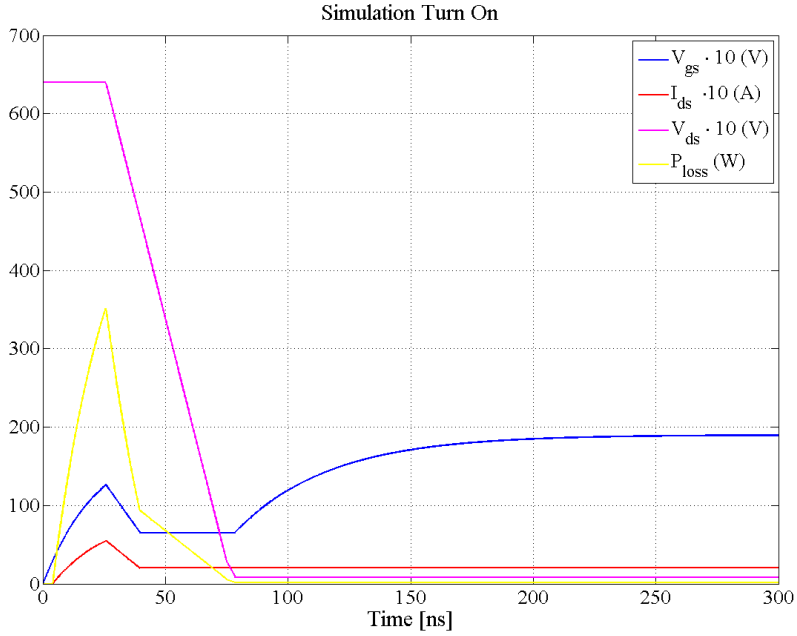


(a) Simulation of the turn-on process

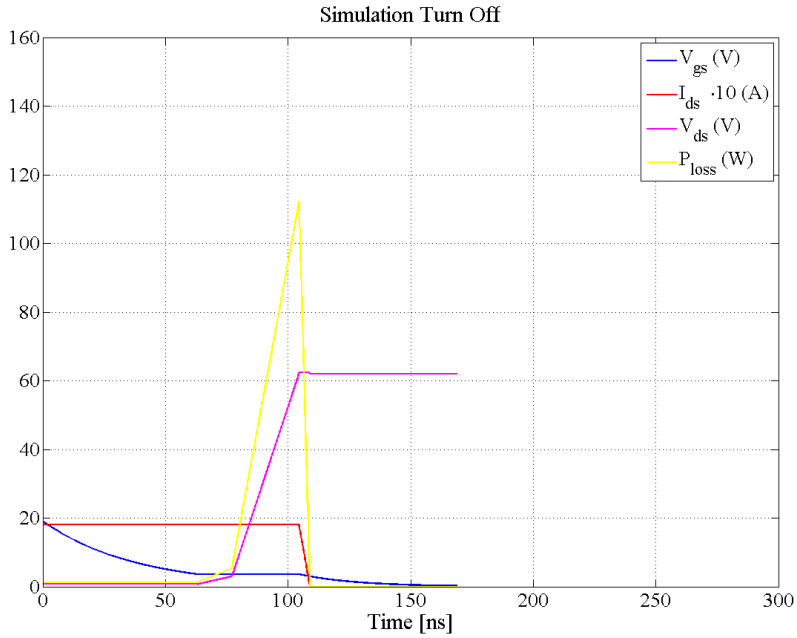


(b) Simulation of the turn-off process

Figure 3.8: Theoretical curves obtained for $V_{dc} \approx 40$ V, $i_0 \approx 3.5$ A and $R_g = 4.7\ \Omega$ for an SiC Mosfet

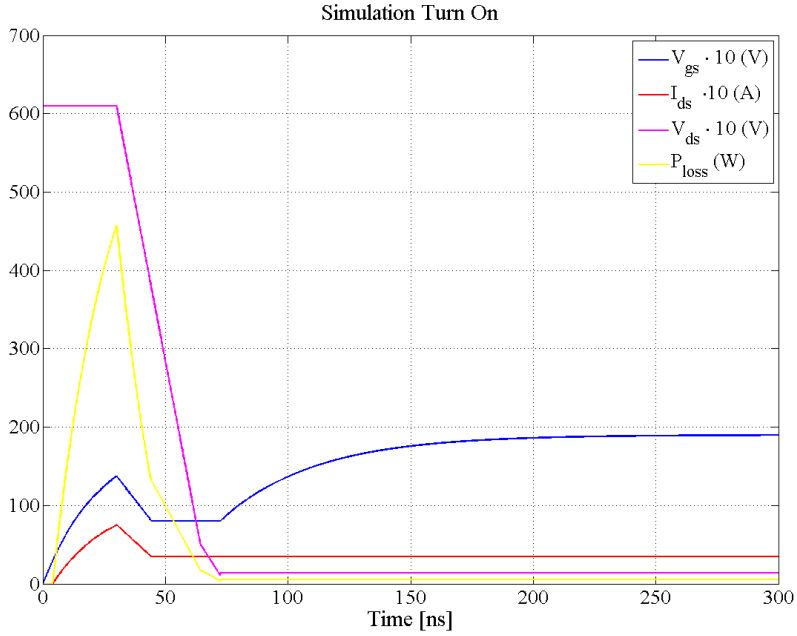


(a) Simulation of the turn-on process

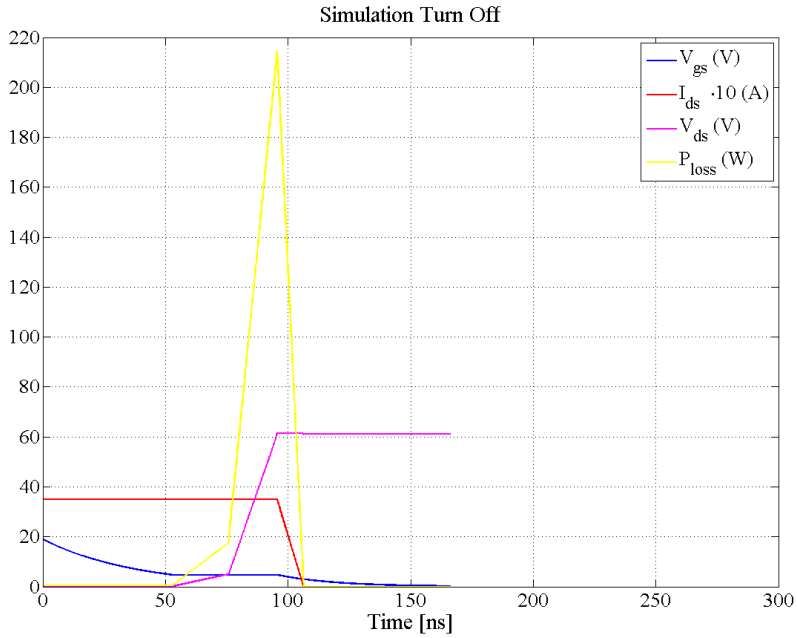


(b) Simulation of the turn-off process

Figure 3.9: Theoretical curves obtained for $V_{dc} \approx 60$ V, $i_0 \approx 1.5$ A and $R_g = 4.7\ \Omega$ for an SiC Mosfet



(a) Simulation of the turn-on process



(b) Simulation of the turn-off process

Figure 3.10: Theoretical curves obtained for $V_{dc} \approx 60$ V, $i_0 \approx 3.5$ A and $R_g = 4.7\ \Omega$ for an SiC Mosfet

4

Analysis

This chapter aims to present and investigate the results of both simulation and measurements. First, the results from the preliminary tests on the driving circuit are presented. Then, the results from the switching loss study are given.

4.1 Driving circuit

4.1.1 Test with only R and C

The circuit has been operated with an R-C load such as described in Figure 3.4(a).

The charge of the capacitor for the three tests are presented in Figure 4.1 and Figure 4.2. The theoretical curves (V_C, th) are also drawn in this figure. These has been obtained such as explained in Section 3.2.1.

Table 4.1 shows the results obtained after the experiments.

Table 4.1: Preliminary tests on the driving circuit

Test	R (Ohm)	C (nF)	τ_{th} (ns)	τ_{exp} (ns)	$\Delta\tau$ (ns)
1	11	2.2	24.2	26.4	4.9
2	5.7	2.2	12.5	20.3	3.5
3	2	2.2	4.4	8.2	2.6
4	11	15	165	179.2	38.3
5	5.7	15	85.5	97.7	20.9
6	2	15	30	32.6	8.6

The errors on the experimental values are calculated using the values shown in Table 3.2 and according to (4.1).

$$\Delta\tau_1 = (R_1 + R_2)C \times \frac{\Delta C}{C} + 2(R_1 + R_2)C \times \frac{\Delta R}{R} + \Delta_{osc} \tag{4.1}$$

The results from tests 1, 4, 5 and 6 are satisfying as the theoretical values of the time constants are in the range of the experimental values. Although, it is not the case for the second and the third test. The results are quite good for the highest value of the capacitor (15 nF). When the capacitor is lower (2.2 nF), the experimental time constants roll away from the theory as the resistance gets lower.

Moreover, all experimental curves (Figure 4.1 and Figure 4.2) show a voltage drop at the beginning of the charge and the voltage V_{gg} seems disturbed by a noise. The voltage drops through the capacitor match with a voltage drop of the voltage from the gate driver V_{gg}.

Finally, two cases catch the attention: test 3 (Figure (4.1(c))) and test 6 (Figure (4.2(c))). In test 3, there are great oscillations on the voltages V_{gg} and V_C. On the other hand, in test 6, there is a high voltage drop (about 7 V) for the gate voltage V_{gg}, the highest of all cases.

In order to analyze those phenomena, the focus will be on the tests with a resistance $R = 5.7\ \Omega$. This case best fits with the value of the internal resistances of the Mosfets that will be studied later.

4.1.2 Extensive testing on the case $R = 5.7\ \Omega$

Study of the disturbances on the gate voltage

In the preliminary tests some disturbances on the gate voltage had been seen. A first hypothesis could be that the capacitors supposed to filter the gate voltage (C10, C11, C19, C20, C26 and C27) are, somehow, introducing a noise to the the gate voltage.

To check whether those capacitors have a bad effect on the gate voltage and try to investigate the cause, further tests are made on case 2 (Figure (4.1(b))). The SMD capacitors are removed step by step: first, the biggest ones (100 nF) and then, all of them. The voltages V_{gg} and V_C and the gate current in both cases (Figure (4.3(b)) and Figure (4.3(c))) are compared with the ones when all SMD capacitors are soldered on the circuit board (Figure (4.3(a))).

The first observation is that the SMD capacitors are beneficial to the operation of the circuit. Indeed, when withdrawing the capacitors, the voltages V_{gg} and V_C gets more disturbed. Therefore, they are placed on the circuit board for the future experiments.

Another observation can be made on the measurement process of the current. It has been determined both with a Rogowski coil and thanks to the shunt resistor method. Indeed, the Rogowski coil cannot be trusted for the time when the current is almost constant since it works for frequencies between 50 Hz and 50 MHz. Moreover, the Rogowski coil introduces a delay. On the other hand, the peaks of current observed with the shunt

resistor method are higher than the ones observed with the Rogowski coil. In order to know which of the two methods that can be trusted, a simple test is made (R,C circuit) and the result on the current is compared to the theory. This test shows that the peak of current from the shunt resistor method is higher than it should be. This is because it happens during a very short time (few nanoseconds) and therefore $L\frac{di}{dt}$ gets very high. On the contrary, the results from the Rogowski coil are lower than expected. As the Rogowski coil introduces a delay and the too high peak of current shown by the shunt resistor method can be compensated, the method to measure the current that will be used in the next experiments is the shunt resistor one.

Behavior of the gate driver when the capacitance varies

The gate voltage, the voltage through the capacitor and the gate current when the capacitor goes from 1 nF to 15 nF are shown in Figure (4.4) and Figure (4.5).

When the capacitance is low (1 nF and 2.2 nF), there is an overshoot on the gate voltage and the voltage through the capacitor which is higher as the capacitance gets lower.

On the contrary, when the capacitance is higher than 4.7 nF, there is a voltage drop on both voltages. The voltage drop is more important as the capacitance is greater.

4.1.3 Limits of the gate driver

The limits of the gate driver occur for both very low capacitances (1 nF case in Figure (4.4)) and high capacitances (15 nF case in Figure (4.4)). It results in an overshoot and oscillations (low capacitances) on the voltages or, on the contrary, in a voltage drop (great capacitances). These phenomena are worse when the resistor is lower (Figure (4.1(c)) and Figure (4.2(c))).

4.1.4 Test with a power Mosfet when the drain-source voltage is zero

The results from the tests with a Mosfet and three different gate resistors are given in Table 4.2. The internal resistance is calculated with the hypothesis than C is equal to 8.7 nF (3.1).

Table 4.2: Computation of the internal resistance of the Mosfet

Test	R (Ohm)	τ_{th} (ns)	R_i (Ohm)
1	4.7	45	0.5
2	3.2	33.4	0.7
3	2.35	28.4	0.9

The experiment is not very accurate. However, we can assume that the internal resistance is less than 1 Ω.

With a gate resistor of 20 Ω, the effect of the internal resistance R_i is insignificant. So the internal capacitance can be computed as in (3.2). This test leads to an internal capacitance of 9.1 nF, which is slightly higher than the first approximation.

4.1.5 Test with a power Mosfet and an R,L load when the drain-source voltage changes

So far, the driving circuit has been tested without any load. This time, an R,L load is added and the circuit is operated for different values of the drain-source voltage v_{DS} (0, 10, 20 and 30V). In this case, the gate resistance is 4.7 Ω and the input signal frequency is about 900 Hz. The value of the inductance is about 40 mH. The results of those measurements can be seen in Figures (4.6), (4.7), (4.8) and (4.9) for both turning on and turning off processes.

When comparing the voltages v_{GS} and V_{gg}, it can be seen how quick the circuit reacts. The rise time is slightly lower with the increasing drain-source voltage. However, it should be quicker since the internal capacitance C_{gd} of the Mosfet is supposed to go from 4.2 nF to almost 0 nF and the other internal capacitance C_{gs} from 4.8 nF to 4 nF [11].

The current i_{DS} and the voltage v_{DS} will be used to compute the switching losses in Section 4.2.1. As explained earlier, the drain current is picked up with both the Rogowski coil and through a shunt resistor. The values from the Rogowski coil have been shifted since this method introduces a delay. The values of the peak of current are the ones from the Rogowski coil and the DC values the ones from the shunt resistor method.

4.2 Measurements

4.2.1 Results with the power Mosfet

The switching losses for the case $V_{dc} = 30$ V are presented in Figure 4.10. For this test, the gate resistance is 4.7 Ω, the gate voltage is 24 V and the current I_0 is 0.8 A.

The switching energy losses are the area under the power curve. It gives about 1.86 μJ for the turn-on process and 0.5 μJ the turn-off process. The approximated method says 3.7 and 0.66 μJ and the simulation gives 1.6 and 0.43 μJ.

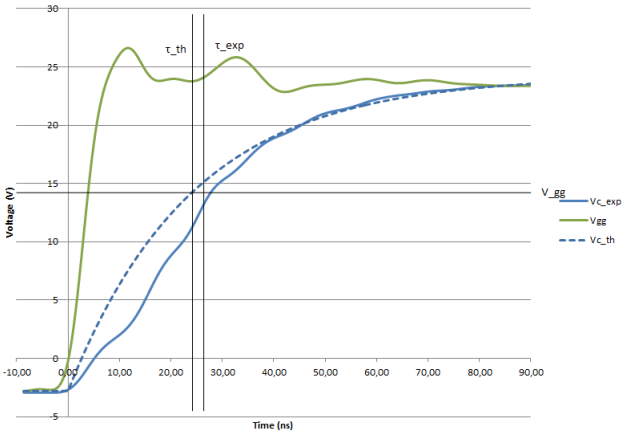
4.2.2 Results with the SiC Mosfet

When the Mosfet is an SiC Mosfet, the curves obtained for the switch-on and the swith-off processes are those presented in Figure 4.11, Figure 4.13, Figure 4.15 and Figure 4.17. The current presents high oscillations. It can be compensated by taking into account the inductance of the circuit ($L\frac{di}{dt}$).

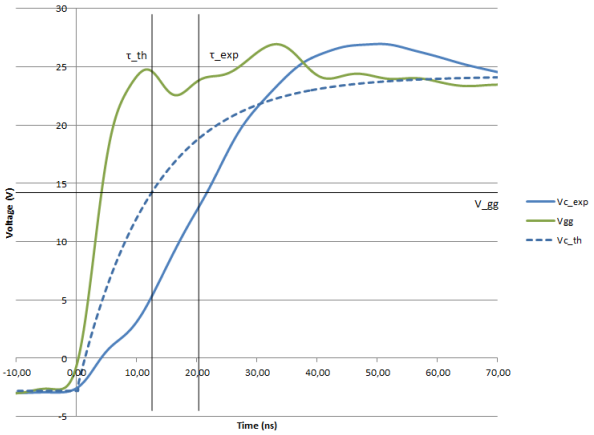
The power losses are shown in Figure 4.12, Figure 4.14, Figure 4.16 and Figure 4.18. Table 4.3 sums up the results obtained from the three different methods. The results are similar for the simulation and the measurements. However, it is quite far from the approximation method.

Table 4.3: Comparison of the switching energy losses for the SiC Mosfet

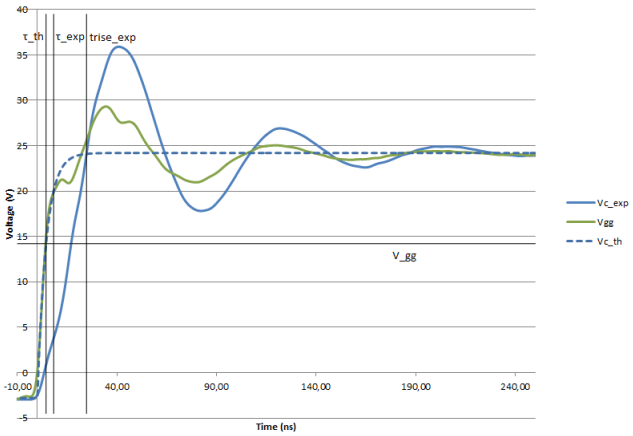
ON/OFF	V_{dc} (V)	I_0 (A)	Approximation (μJ)	Simulation (μJ)	Measurement (μJ)
ON	43	1.6	5.3	5.0	5.2
OFF	43	1.6	0.96	1.3	1.0
ON	40	3.8	11.7	9.3	9.7
OFF	40	3.8	2.1	2.7	2.7
ON	65	1.6	8.0	9.6	9.9
OFF	65	1.6	1.5	2.0	1.7
ON	62	3.8	18.1	15.1	16.8
OFF	62	3.8	3.3	3.7	3.2



(a) Test 1: $R = 11$ Ohms and $C = 2.2$ nF

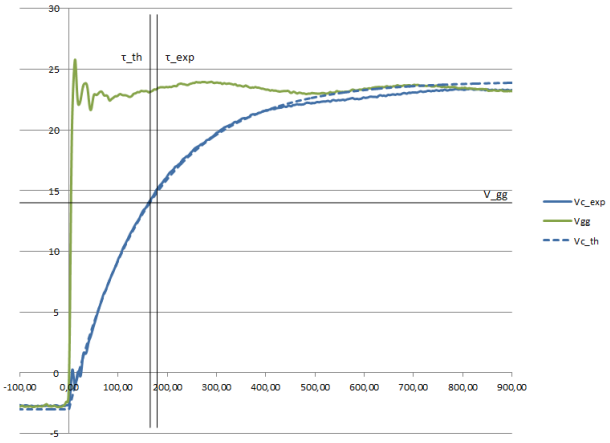


(b) Test 2: $R = 5.7$ Ohms and $C = 2.2$ nF

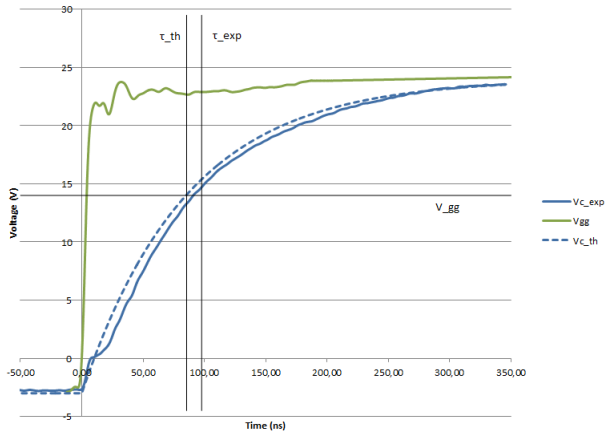


(c) Test 3: $R = 2$ Ohms and $C = 2.2$ nF

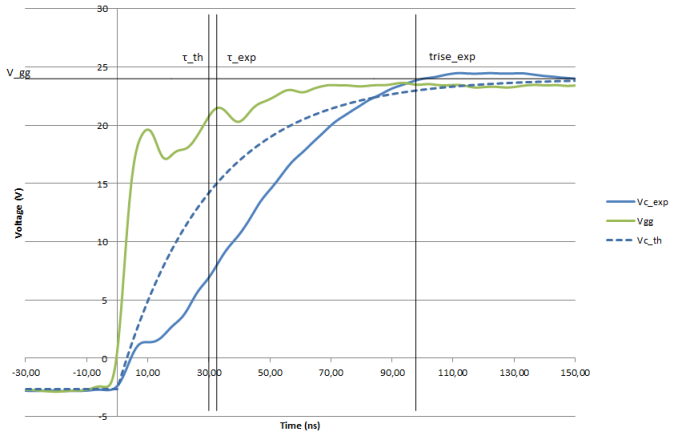
Figure 4.1: Curves obtained with 2.2 nF



(a) Test 4: $R = 11$ Ohms and $C = 15$ nF

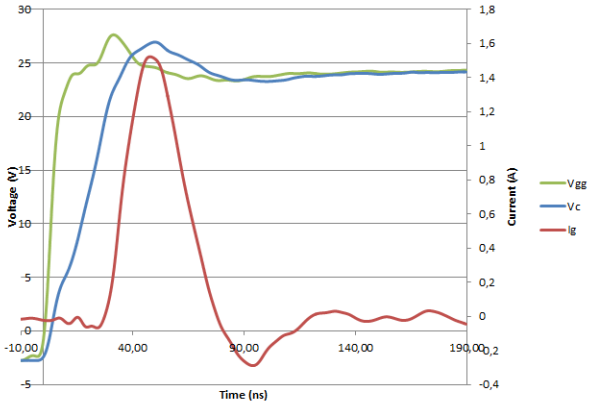


(b) Test 5: $R = 5.7$ Ohms and $C = 15$ nF

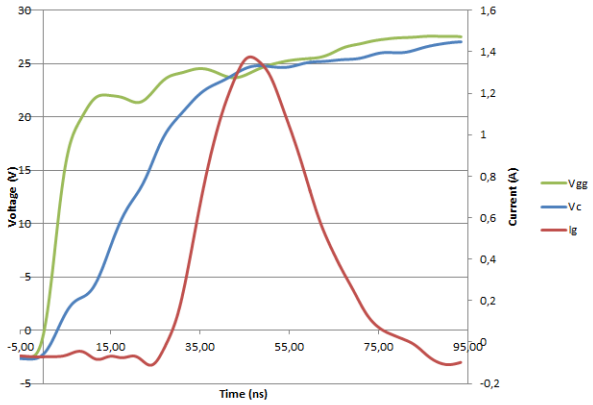


(c) Test 6: $R = 2$ Ohms and $C = 15$ nF

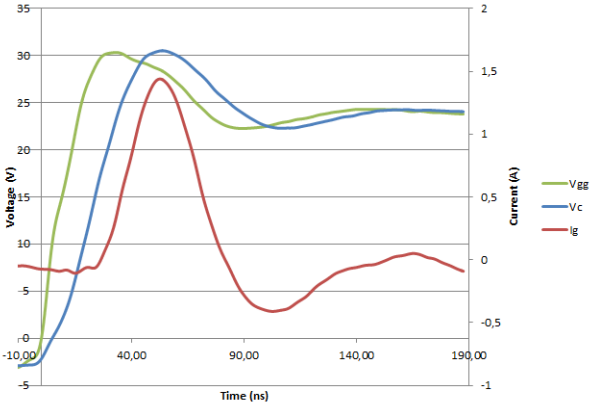
Figure 4.2: Curves obtained with 15 nF



(a) Test : with C10, C20, C19, C26, C11 and C27

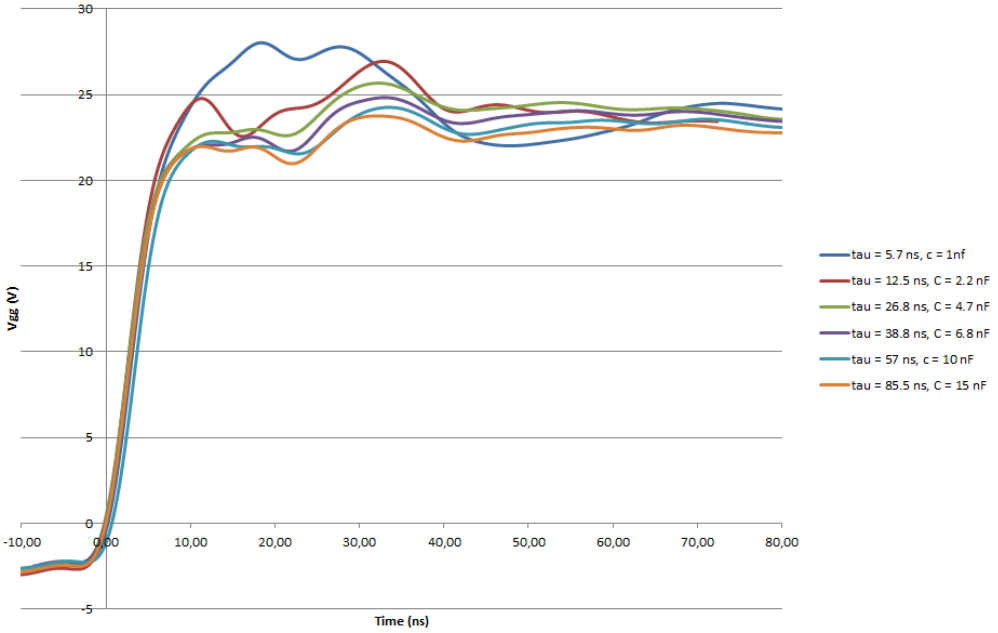


(b) Test : without C11 and C27 (200nF in total)

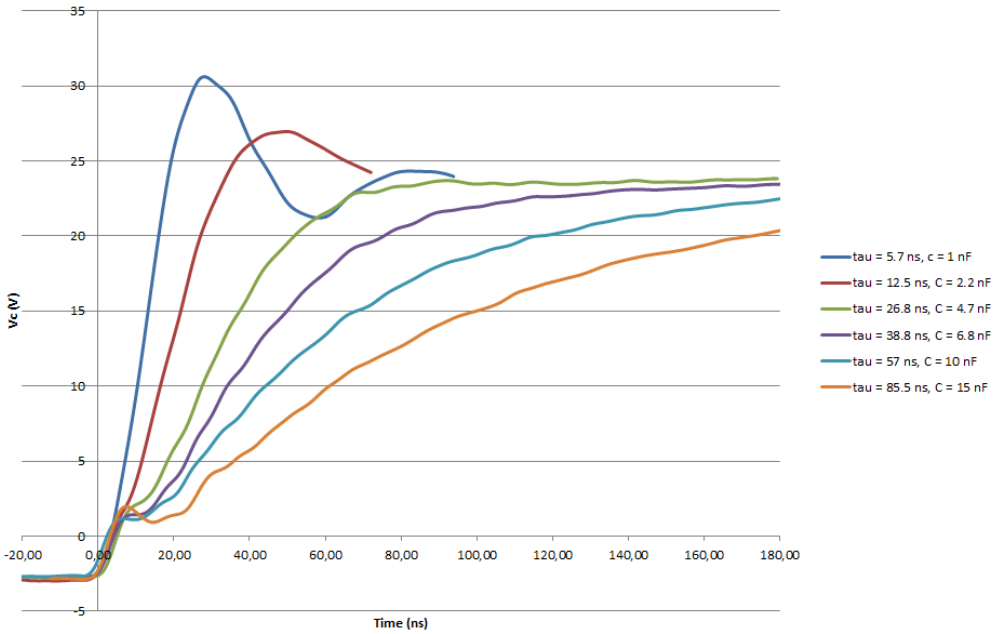


(c) Test : without C10, C20, C19, C26, C11 and C27 (222nF in total)

Figure 4.3: Results when withdrawing the SMD capacitors

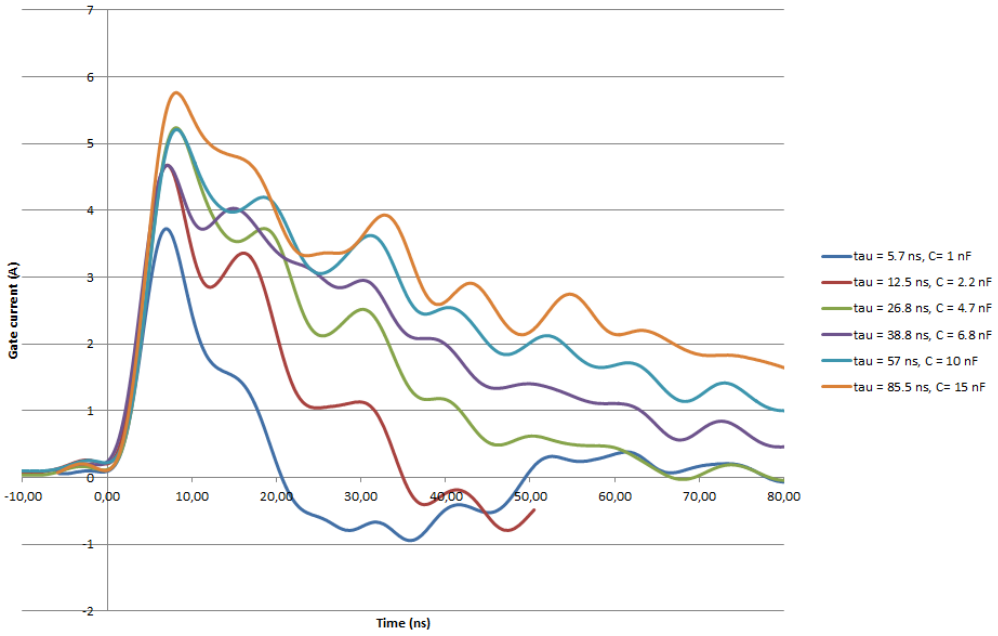


(a) Gate voltage

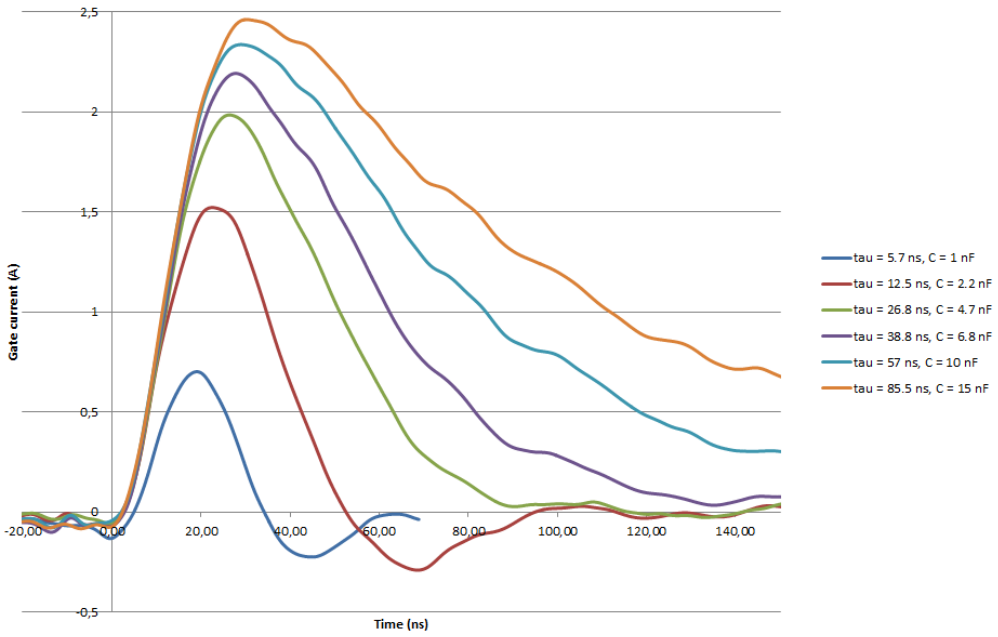


(b) Voltage through the capacitors

Figure 4.4: Gate voltage and voltage throug the different capacitors when $R = 5.7\Omega$

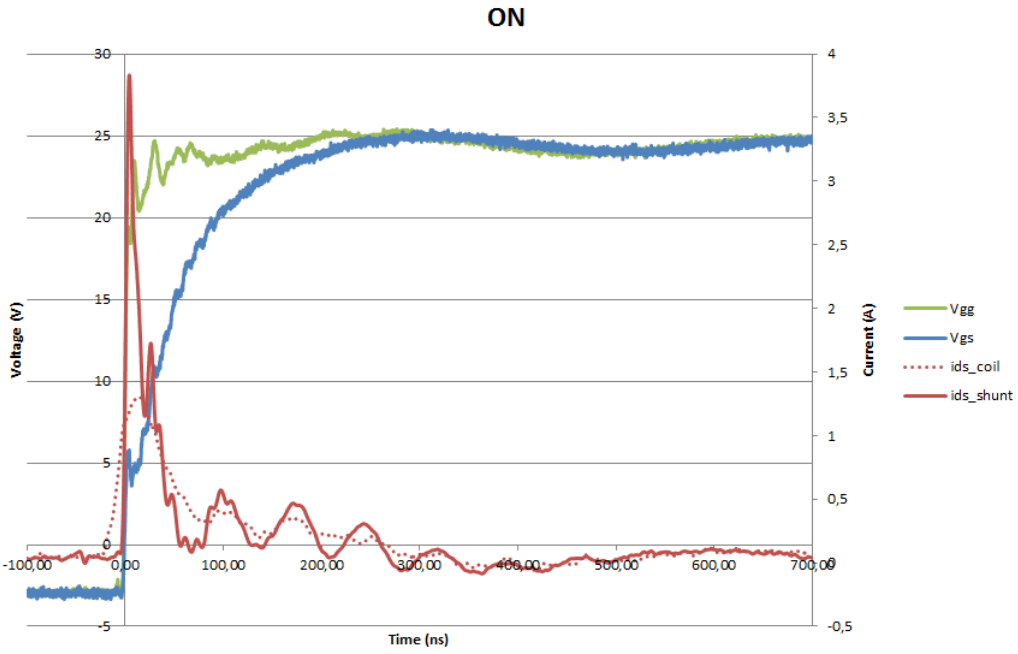


(a) Gate current determined with the shunt resistor method

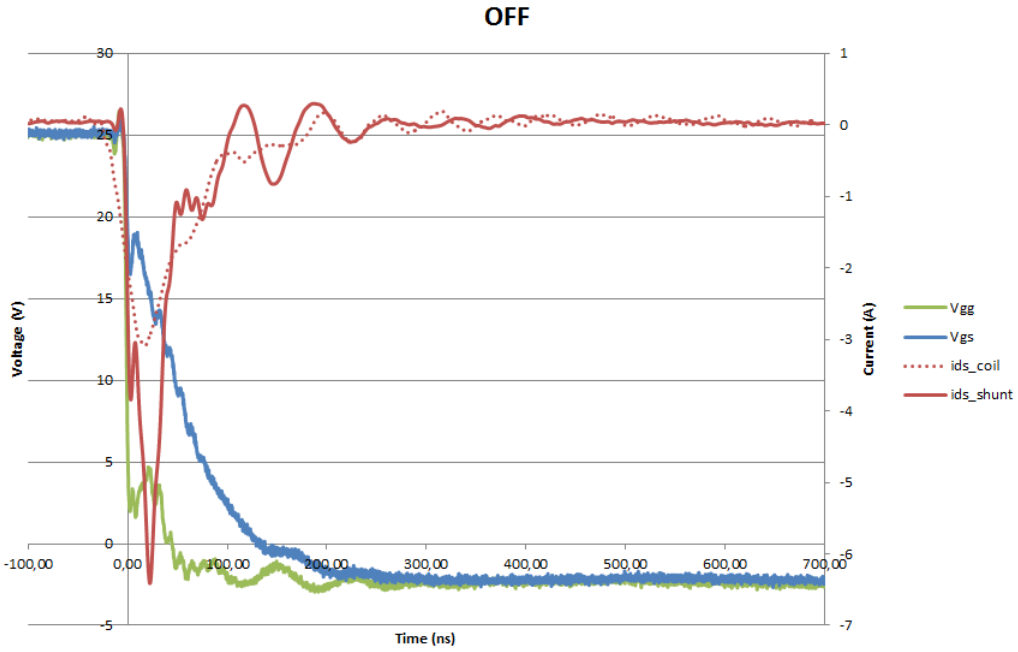


(b) Gate current determined with the Rogowski coil

Figure 4.5: Gate current for different values of the capacitor and $R = 5.7\Omega$

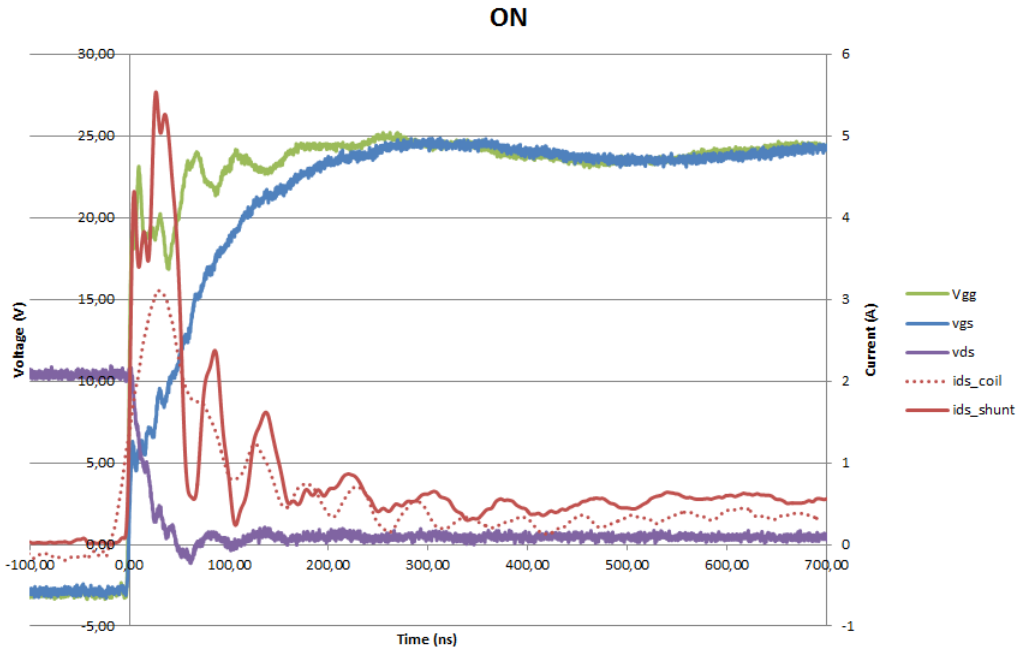


(a) On



(b) Off

Figure 4.6: Power Mosfet voltages and current when the drain-source voltage is zero and $R_g = 4.7$ Ohms



(a) On

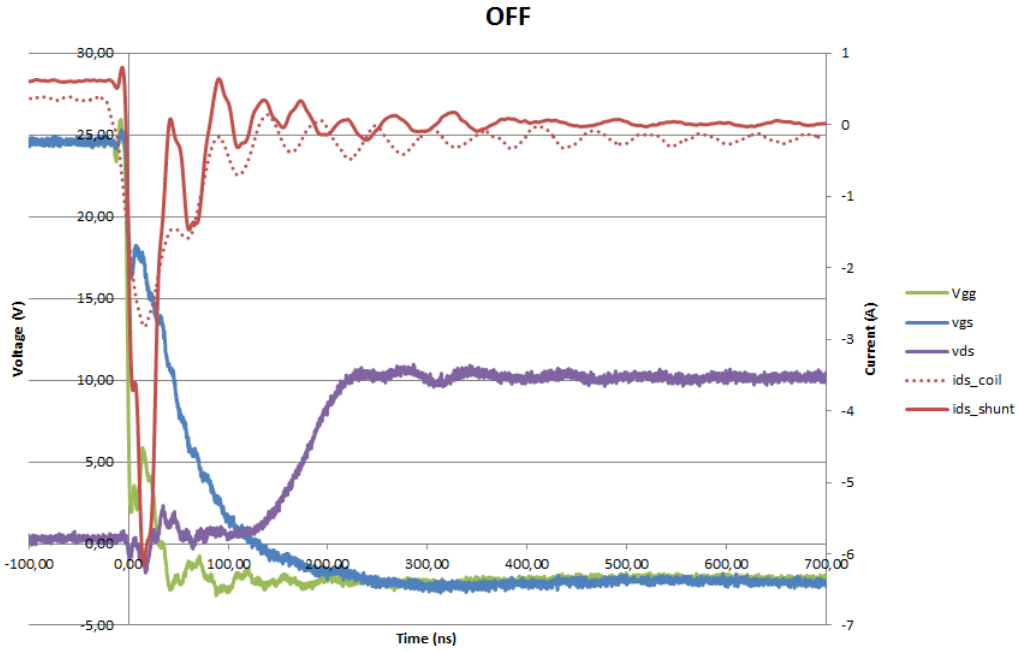


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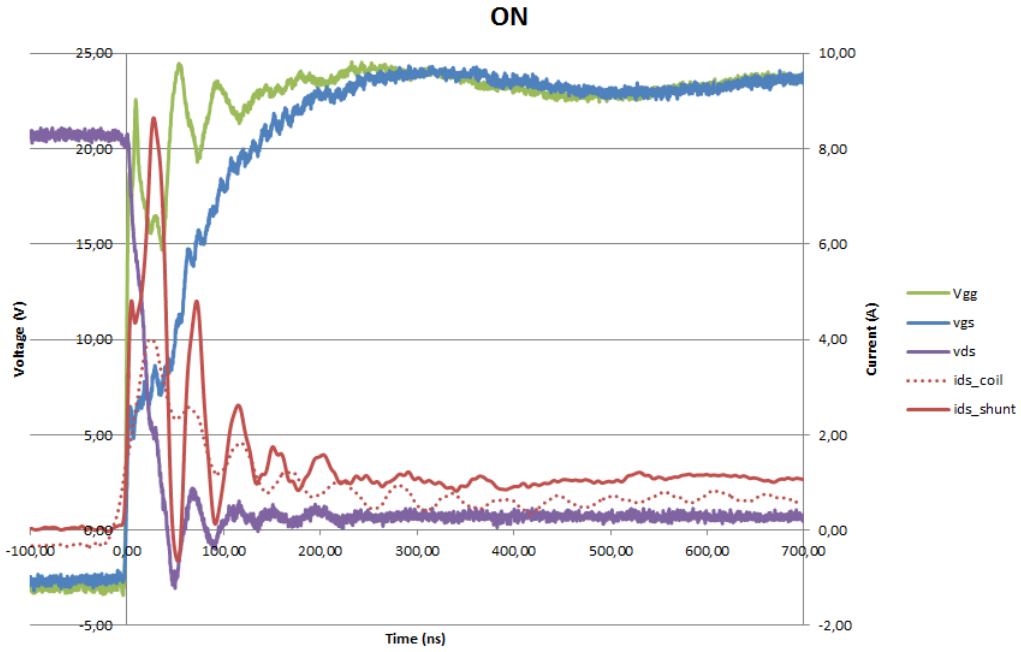
Figure 4.7: Power Mosfet voltages and current when the drain-source voltage is 10 V and $R_g = 4.7$ Ohms



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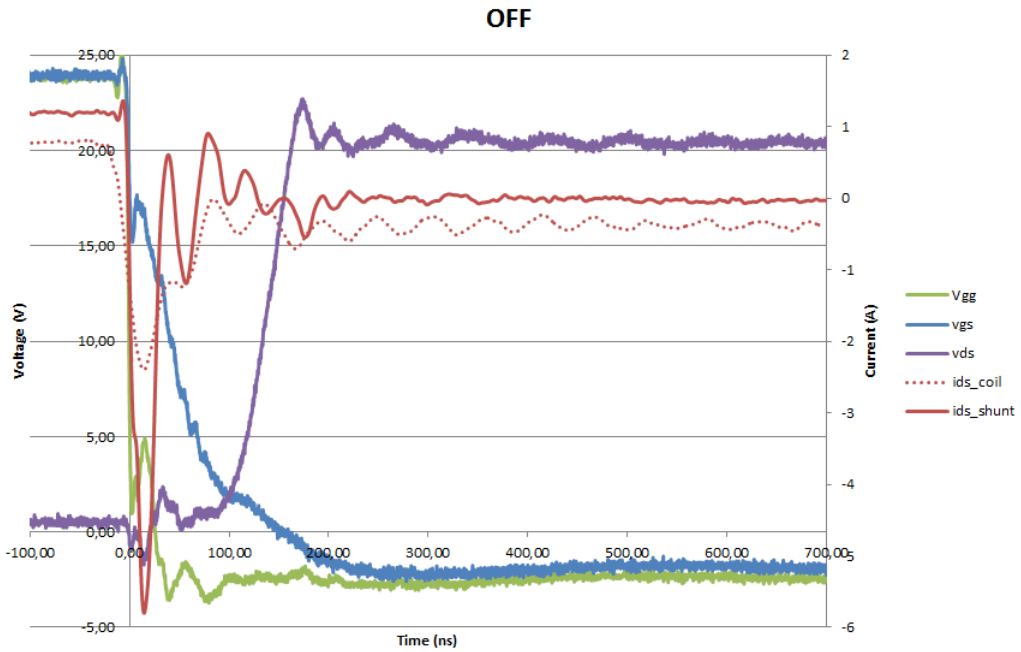
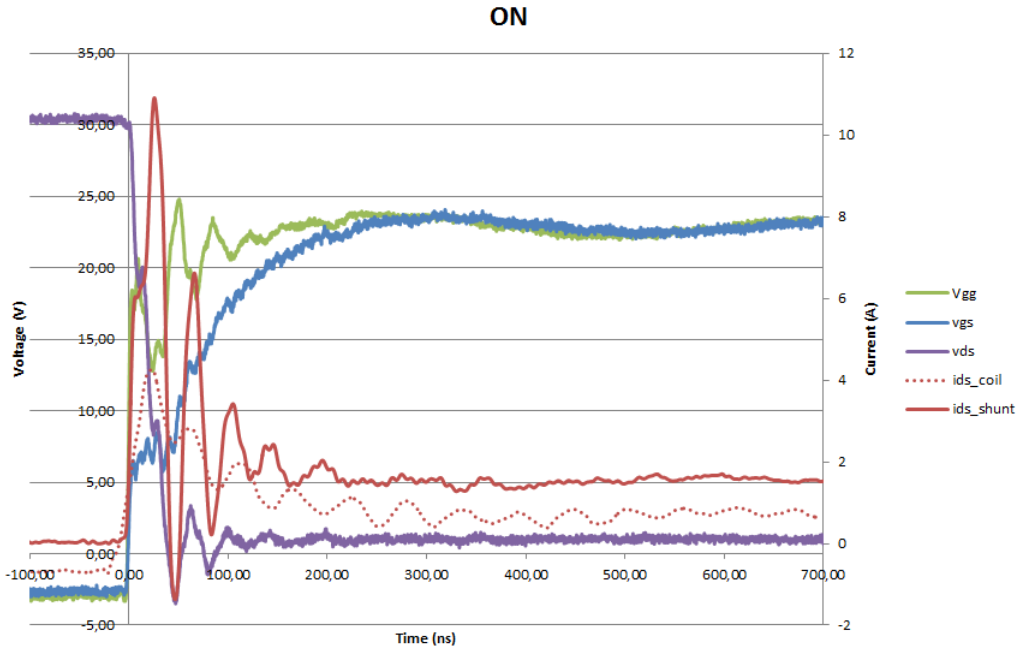


(b) Off

Figure 4.8: Power Mosfet voltages and current when the drain-source voltage is 20 V and $R_g = 4.7$ Ohms



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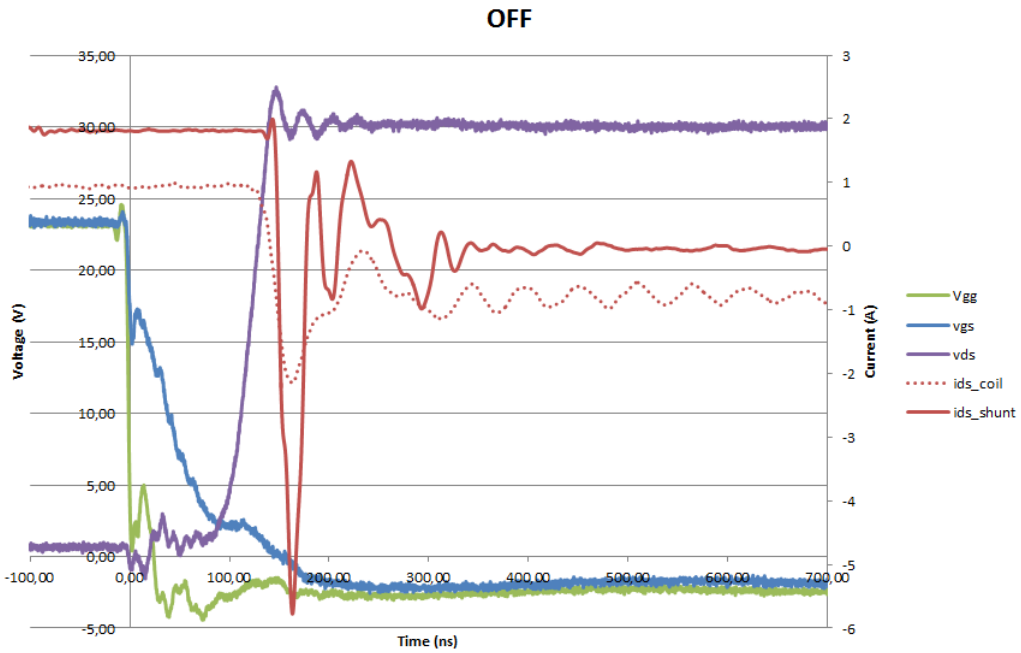

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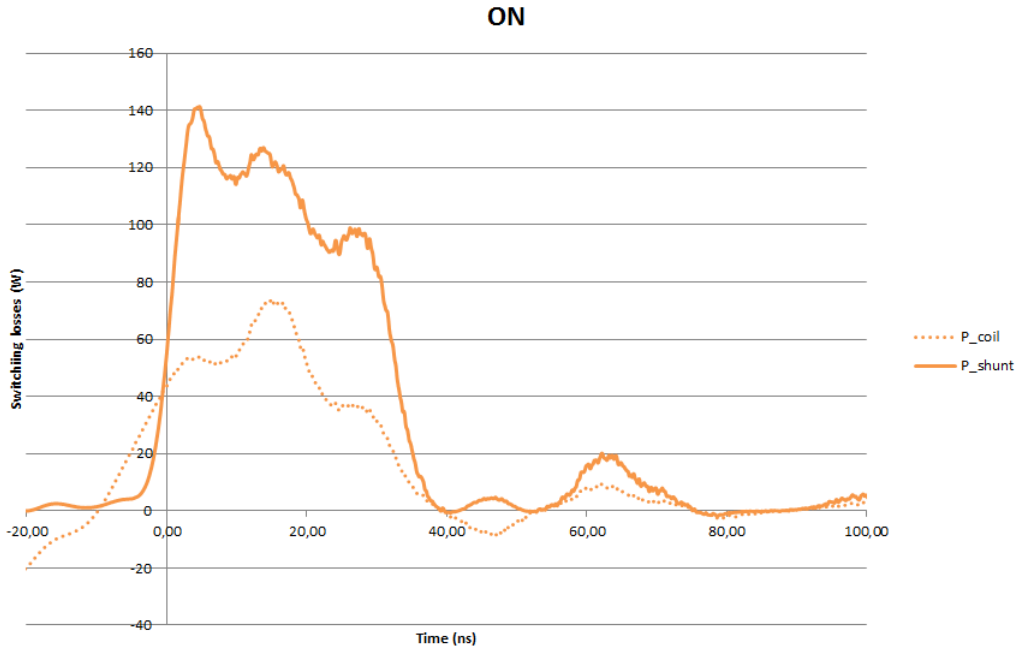
Figure 4.9: Power Mosfet voltages and current when the drain-source voltage is 30 V and $R_g = 4.7$ Ohms



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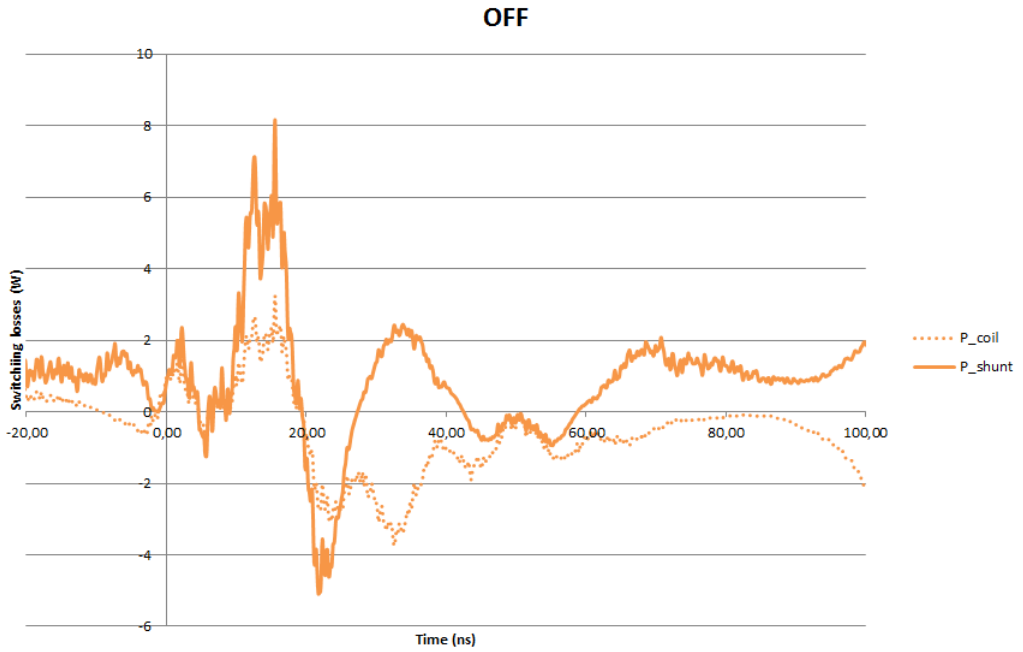
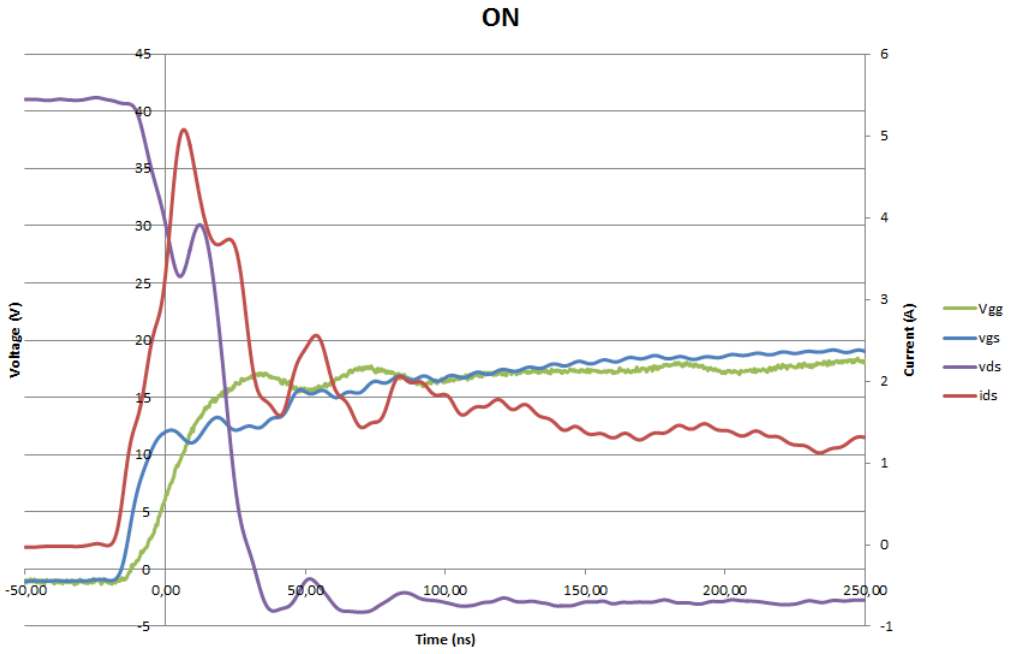


(b) Off

Figure 4.10: Power Mosfet switching losses when the drain-source voltage is 30 V and R_g = 4.7 Ohms



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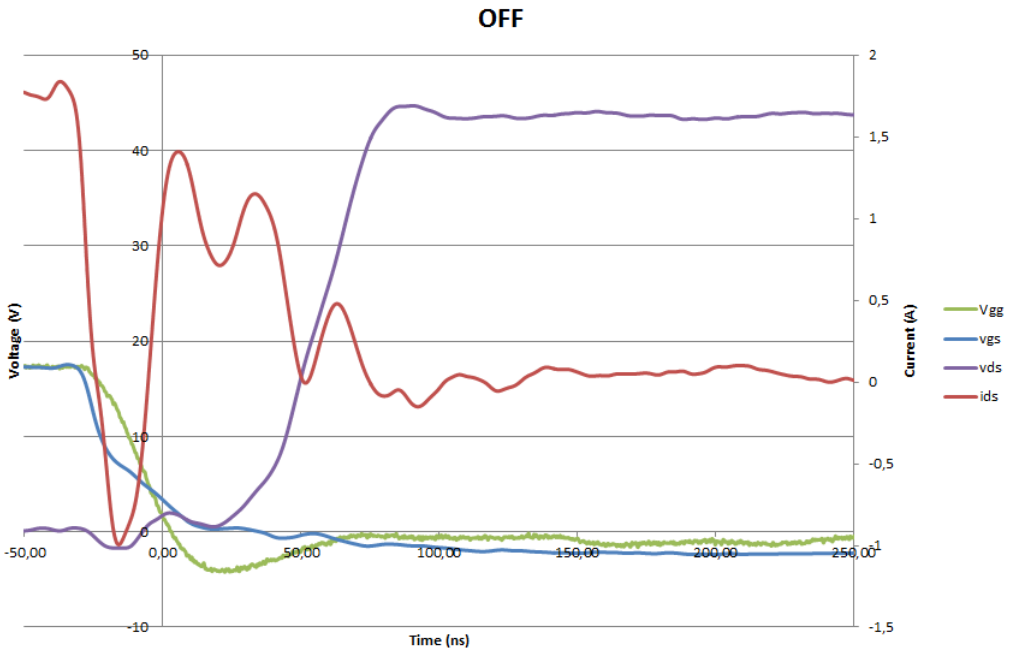
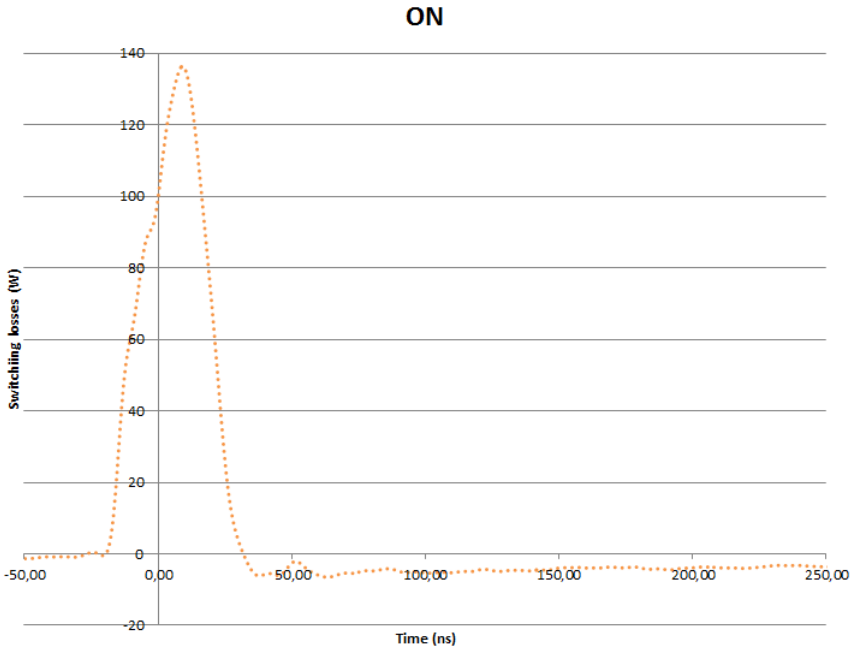


(b) Off

Figure 4.11: SiC Mosfet voltages and current when $V_{dc} \approx 40$ V, $i_0 \approx 1.5$ A and $R_g = 4.7$ Ω



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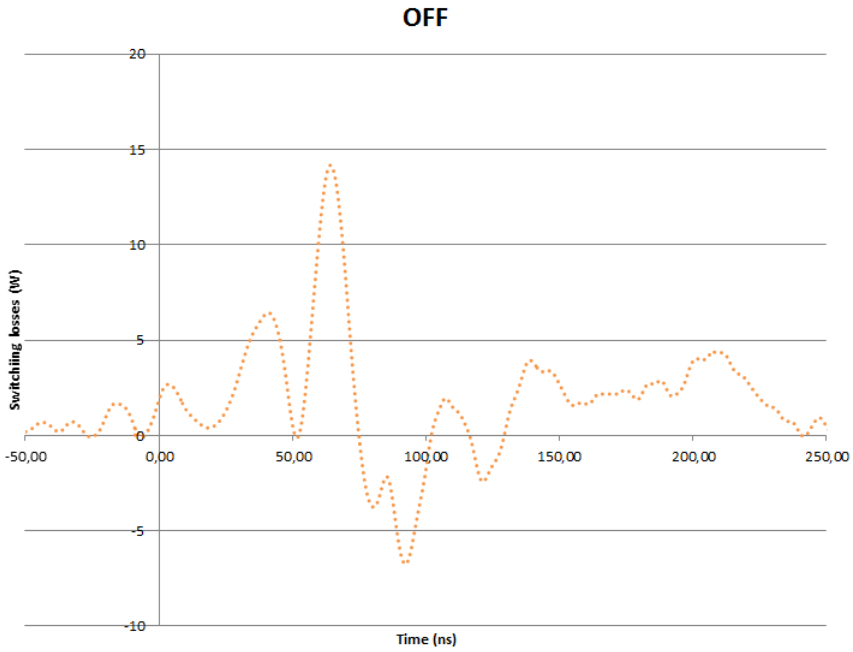
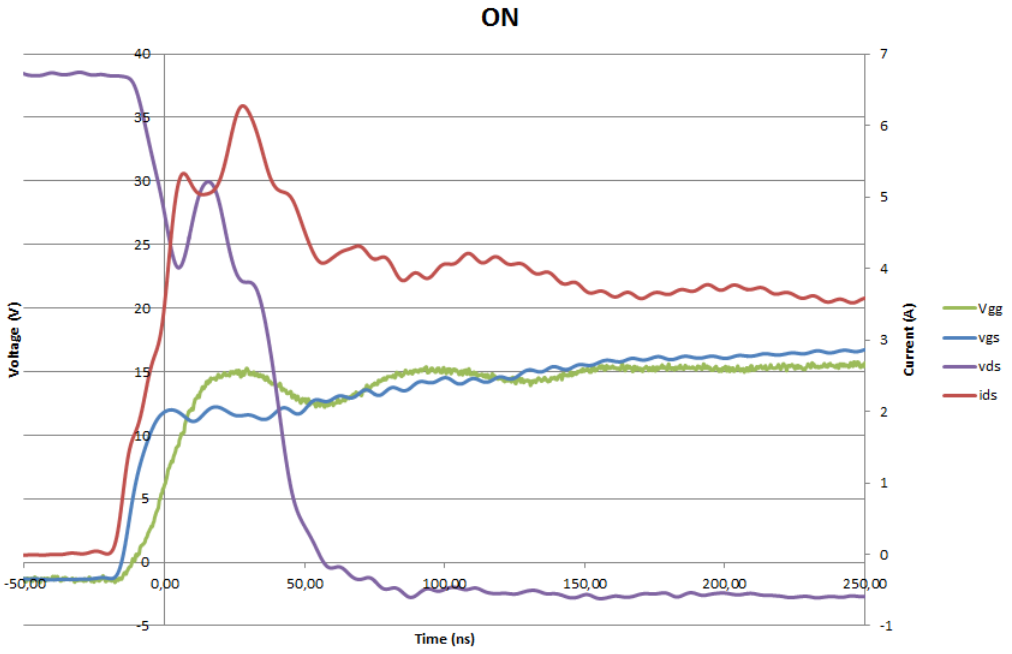


(b) Off

Figure 4.12: Power Mosfet switching losses when $V_{dc} \approx 40$ V, $i_0 \approx 1.5$ A and $R_g = 4.7\ \Omega$



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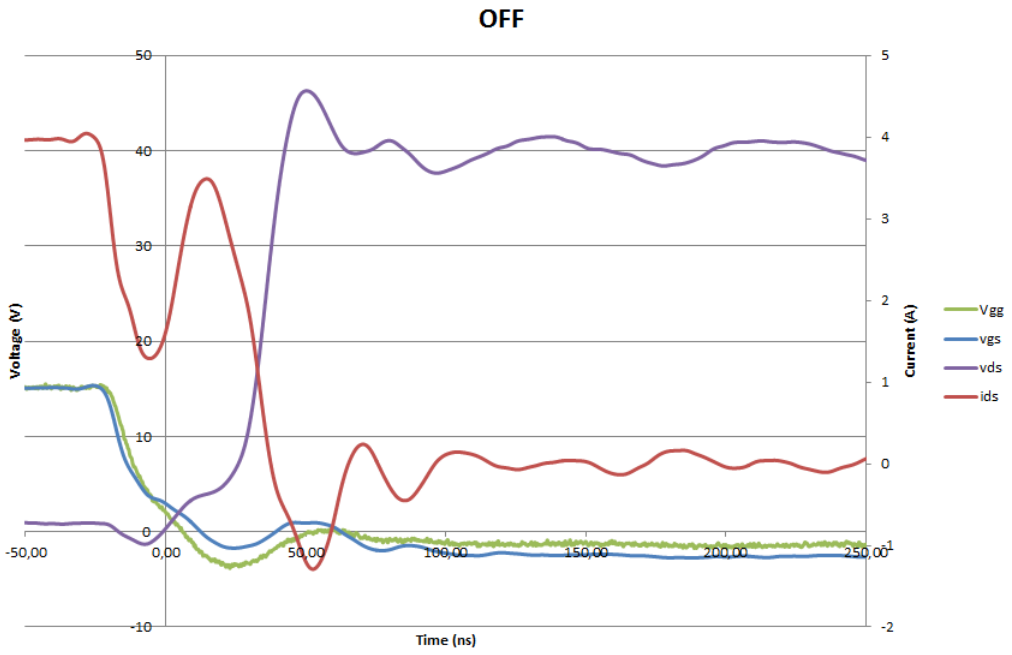
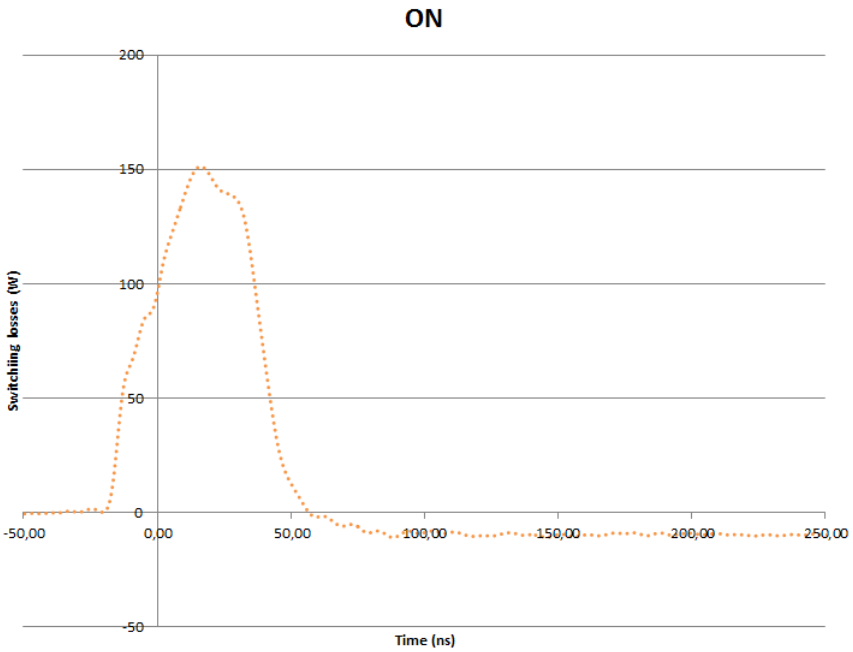


(b) Off

Figure 4.13: SiC Mosfet voltages and current when $V_{dc} \approx 40$ V, $i_0 \approx 3.5$ A and $R_g = 4.7$ Ω



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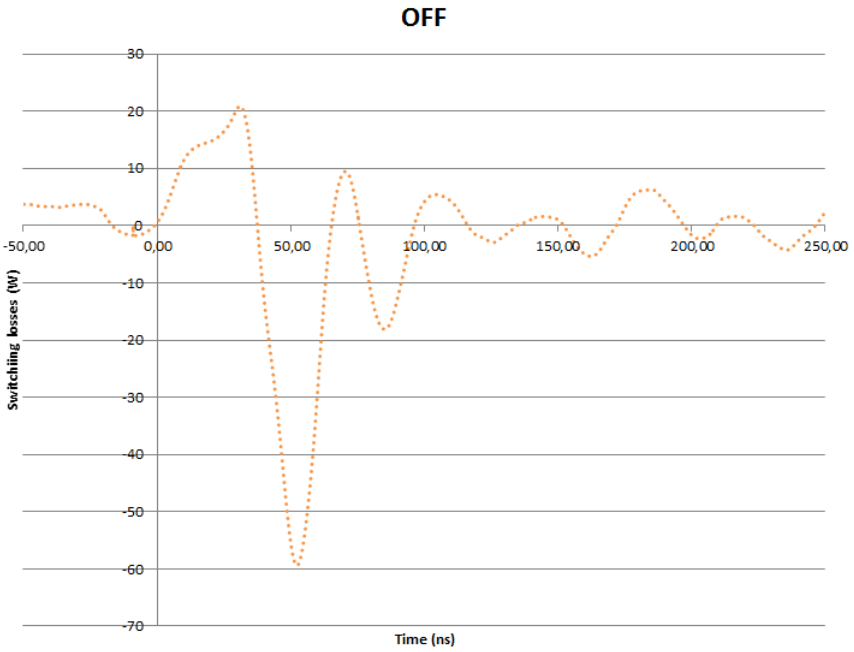
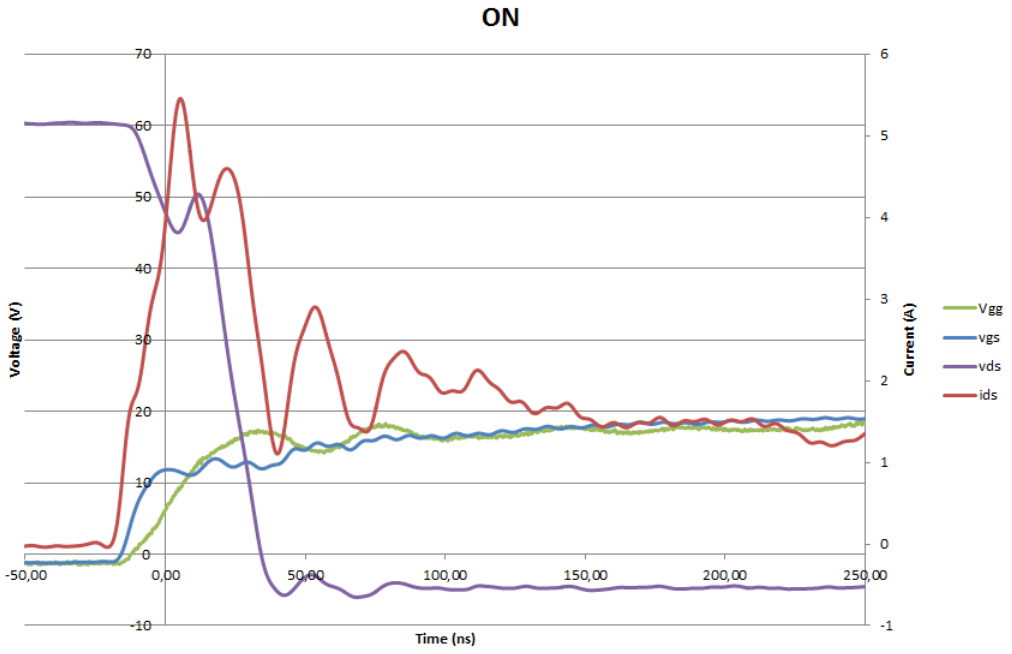
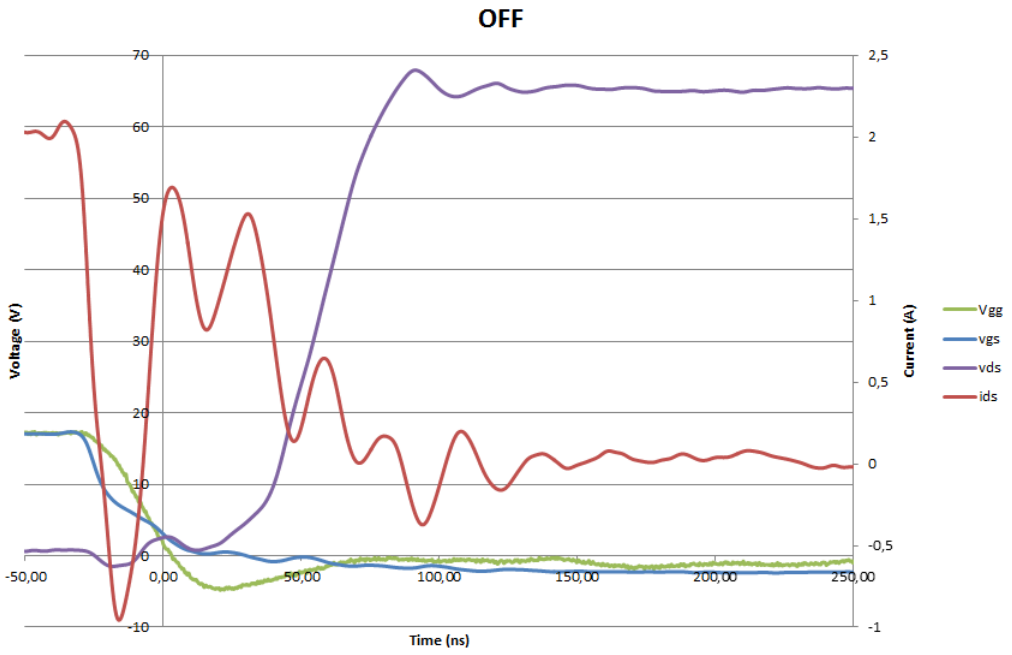


(b) Off

Figure 4.14: Power Mosfet switching losses when $V_{dc} \approx 40$ V, $i_0 \approx 3.5$ A and $R_g = 4.7\ \Omega$

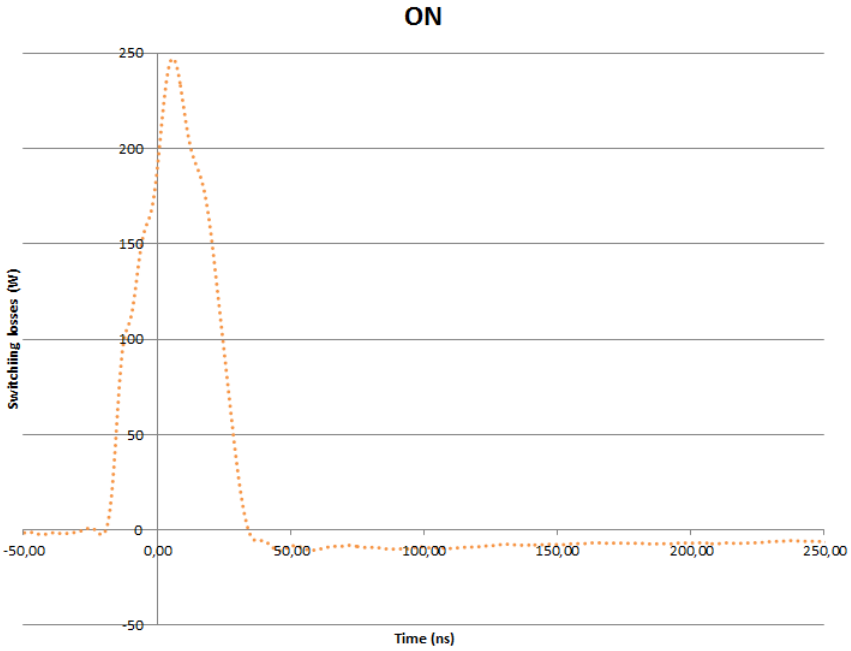


(a) On

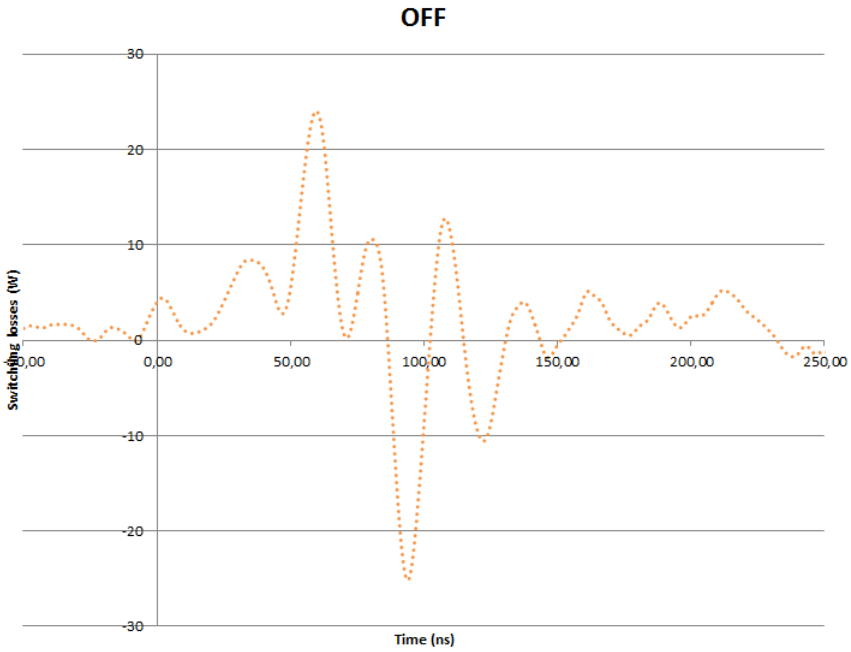


(b) Off

Figure 4.15: SiC Mosfet voltages and current when $V_{dc} \approx 60$ V, $i_0 \approx 1.5$ A and $R_g = 4.7$ Ω

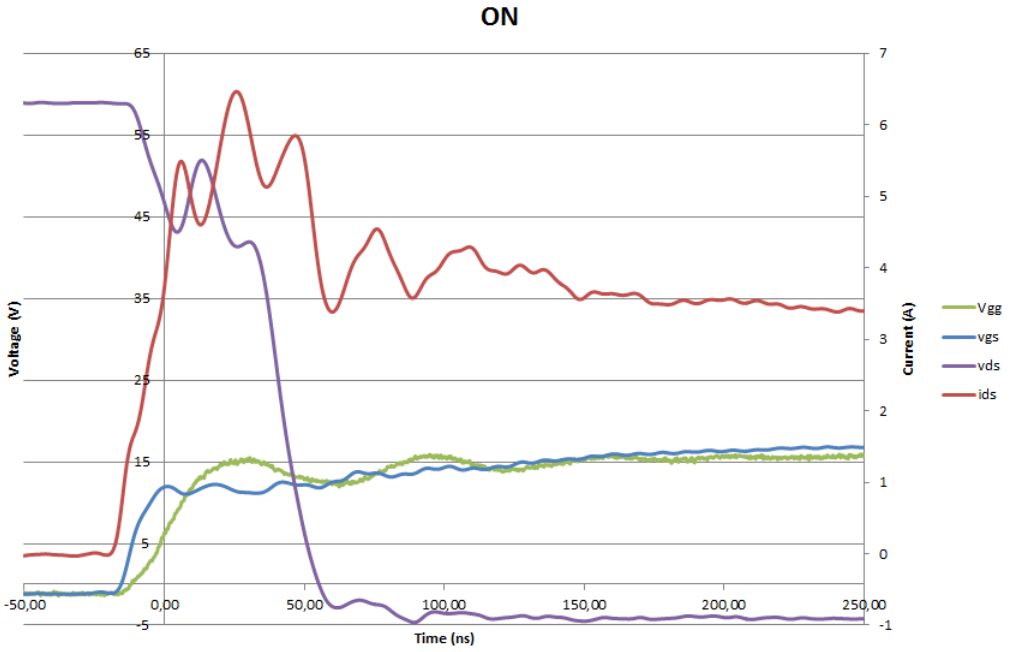


(a) On



(b) Off

Figure 4.16: Power Mosfet switching losses when $V_{dc} \approx 60$ V, $i_0 \approx 1.5$ A and $R_g = 4.7\ \Omega$



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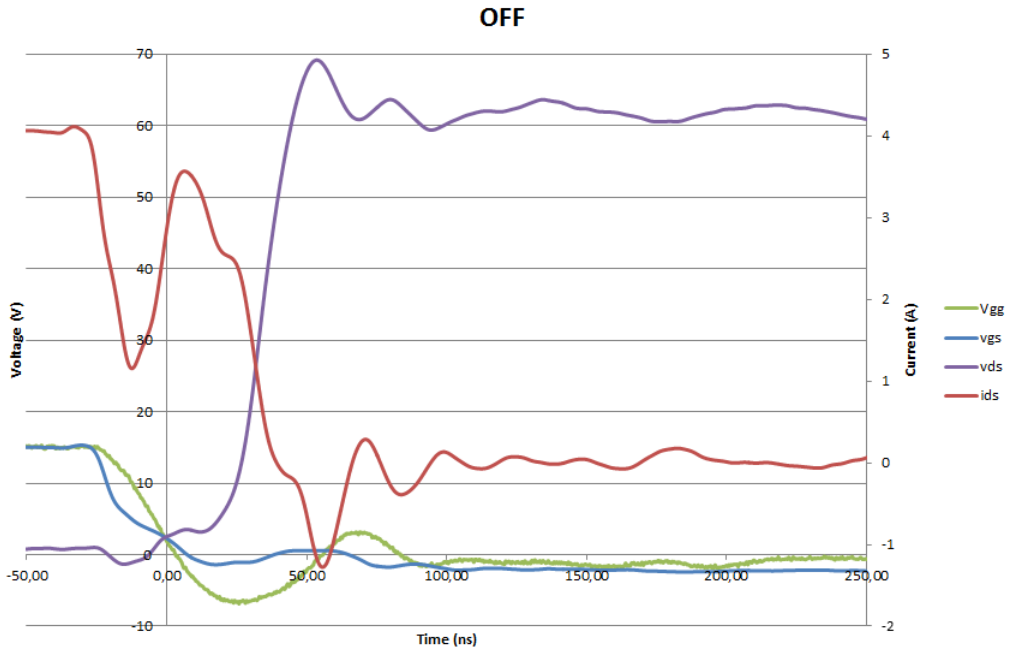
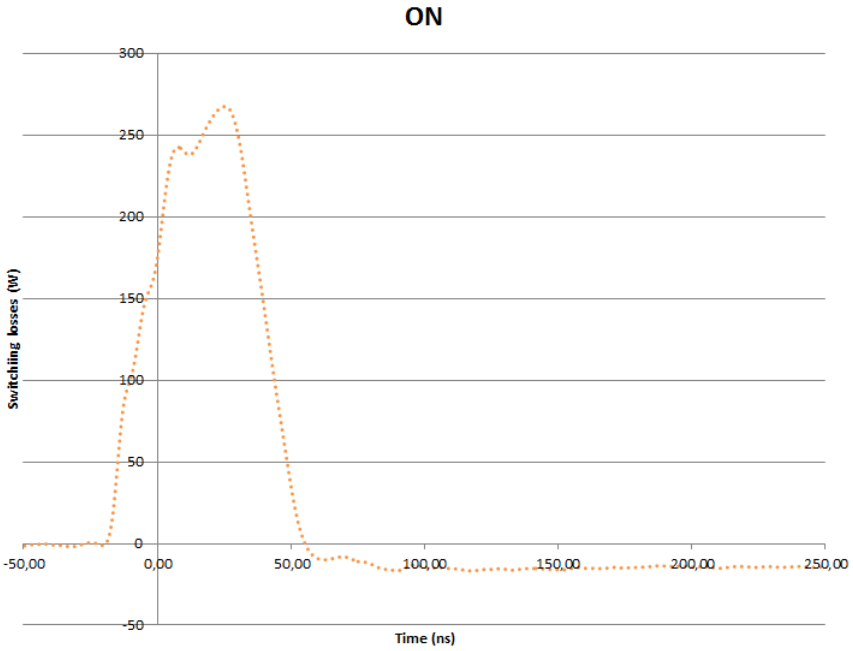


(b) Off

Figure 4.17: SiC Mosfet voltages and current when $V_{dc} \approx 60$ V, $i_0 \approx 3.5$ A and $R_g = 4.7$ Ω



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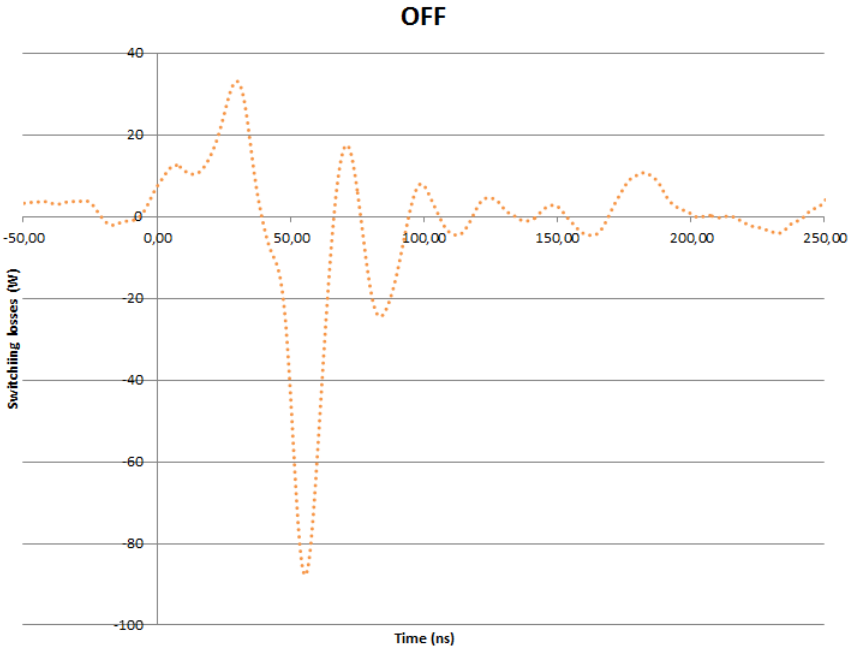

(b) Off

Figure 4.18: Power Mosfet switching losses when $V_{dc} \approx 60$ V, $i_0 \approx 3.5$ A and $R_g = 4.7\ \Omega$

5

Conclusion

The purpose of this conclusion is threefold. First, a comparison between the theoretical values and the experimental results is held in order to show how they match to each other. Then, another comparison is made but with the old set-up. Finally, the last part gives an outlook of what could be done to get better results or to follow on this project.

5.1 Comparison between theory and measurements

The results from the measurements are close to those from the simulation. It is however quite far from the approximation method. This is exactly why the simulation is needed to determine the switching losses. Indeed, the information from the data-sheets are not accurate enough to provide a good prediction of the switching losses.

The difference between simulation and reality can come from the measurement process (inductance of the cables and the circuit) or from the modeling of the internal capacitances in the simulation. Indeed, C_{iss} and C_{rss} change non-linearly with the increasing drain-source voltage and it has been modeled as two discrete values, one for the low voltages and another one for the high voltages.

5.2 Comparison with the old set-up

So far, the new set-up doesn't seem to be any better than the previous one mostly regarding the comparison between the theoretical switching losses and the measured switching losses. However, the measurements have been made using a much lower drain-source voltage than with the old set-up.

5.3 Future work

Regarding the circuit board, a separate board for the different power suppliers would ease the operating of the measurements. This other circuit board could also show the state of the batteries (on/off) and their level of charge.

During the measurements, the results were a bit disturbed by a noise. This could be fixed using a special device that improve the quality of the measurements by using a bi-coaxial cable instead of the usual probes. Then, the ground is directly connected to the circuit board so it reduces the negative effect of the inductance of the cable connected to the ground with an usual probe.

Moreover, in order to get a better comparison between the old and the new set-up, the measurements could be done with the same parameters in both case (same Mosfet, voltage and current).

Finally, as a priority, the measurement method of the current should be improved. Indeed, it degrades considerably the accuracy of the switching losses calculations.

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