SIS Tunnel Junction's Specific Capacitance Direct Measurement

Parisa Yadranjee Aghdam, Hawal Rashid, Vincent Desmaris, Alexey Pavolotsky, Victor Belitsky

***Abstract*—The need for operating frequencies well into THz region with higher sensitivity and wider bandwidth pushes superconductor-insulator-superconductor (SIS) technology towards junctions with more transparent barrier and higher current densities. Obtaining accurate knowledge of the specific capacitance, which is related to the transparency of the junctions, leads to a precise design of the tuning circuitry. Previously, characterization of the SIS junction's specific capacitance involved complex measurements providing data relying on various model fitting. Herein, we present the characterization of the specific capacitance by directly measuring the impedance of the SIS tunnel junction at microwave frequencies (~3 GHz).**

***Index Terms*—SIS junction, S-parameter measurements, specific capacitance.**

I. INTRODUCTION

Superconductor-Insulator-Superconductor (SIS) mixers have been the workhorse in radio astronomy receivers. SIS mixers with Nb/Al-AlO_x/Nb trilayer are commonly recognized for their lowest noise performance at operating frequencies below Nb gap frequency (c.a. 700GHz) [1]. An SIS junction is characterized by its intrinsic capacitance (C) being in parallel with the nonlinear tunnel resistance (R). The linear part of R in which the junction is biased above the gap is called the normal resistance (R_n). The R_nA product where A is the SIS junction area, defines the SIS junction Q-factor value and if it is reduced the junction operation band could be increased [2]. Additionally, the R_nA value is a measure of the transparency of the barrier; the lower the R_nA value the higher the critical current density of the junction [3]. Since the tunnel barrier in the Nb/Al-AlO_x/Nb trilayer is formed by the thermal oxidation of the Al layer, the non-uniformity of the insulator's thickness becomes more significant at thinner tunnel barriers. Therefore, at very low barrier thicknesses, the junction quality degrades which manifests itself in an increase of the sub-gap region's resistance and additional shot noise [4]. Since it is neither possible to uniquely define a uniform barrier thickness, nor assign a relative permittivity (ε_r) to the barrier's insulator (AlO_x), the junction capacitance is determined as a function of R_nA product. Its value can be measured from the DC IV characteristics of the junction and using prior knowledge of the junction area. Thus, the specific capacitance (C/A) is semi-empirically predicted to be inversely proportional to R_nA [2]. However, experiments have shown that at very low barrier thicknesses, the specific capacitance deviates from estimated values. Furthermore, depending on the trilayer deposition techniques, inconsistent values of specific capacitance have been reported. Therefore, there is a clear demand for the method to accurately measure the capacitance.

So far, the most commonly used methods to estimate the specific capacitance were based on analysis of Fiske steps [5], SQUID structures [6] or McCumber parameter [7]. In these methods, the capacitance is calculated by indirect measurement of its effects, e.g. resonance. Thus, the estimated value is accompanied with high uncertainty levels that depend not only on the accuracy of the aforementioned measurements, but also on the assumptions made in the employed models.

In another method, escape rate from the tilted washboard potential is studied while microwave signal is applied to the junction [8]. In this method, aka time-resolved measurement, quite high accuracy is reported. However, for the SIS junctions with R_nA in the range of interest, this calls for measurements at 100 GHz and above thus technically challenging.

In this paper, we present a method for characterization of the specific capacitance, which uses S-parameters direct measurements and analysis of the junction. Since on practice, the impedance of the junction is often very small compared to the 50 Ω impedance of a microwave measurement system and stray impedances, the reflection coefficient from the junction is rather masked by a very large mismatch. However, nowadays, the progress in the measurement equipment and calibration techniques allows this type of measurements to be performed at satisfactory accuracy level. In this paper, the measurement and calibration method is discussed and initial results are presented.

II. JUNCTION FABRICATION AND DC CHARACTERIZATION

The Nb/Al-AlO_x/Nb SIS junctions were fabricated in-house [9] with R_nA product of 30 Ω.μm^2. A superconducting microstripline of 50 Ω on a high-resistivity Si substrate mounted into a fixture, connects the junction to the SMA connector. The junctions with various sizes were fabricated, from which the resulting R_nA value and device areas were estimated. From the semi-empirical relation (1) and (2), the approximate value of the specific capacitance (C_s) and the junction capacitance (C) can be predicted.

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$$C_s = [0.3/\ln(R_nA)] \quad (1)$$

$$C = C_sA \quad (2)$$

III. One-Port Measurements

A voltage biased SIS junction equivalent circuit is represented as a resistance (R) in parallel with the junction capacitance (C). Accordingly, the admittance of the junction can be shown as in (3). The S-parameter (S_{11}) can be measured with a Vector Network Analyzer (VNA). The S_{11} is now converted to Y_{11}, see (4).

$$Y_{11} = [1/R + jC\omega] \quad (3)$$

$$Y_{11} = Y_0[(1-S_{11})/(1+S_{11})] \quad (4)$$

IV. Measurement Setup

The first challenge in the measurement of the SIS junction's impedance is the calibration. The temperature gradient through long stainless steel cables would alter the length and propagation characteristics of the cables. Consequently, a de-embedding method on top of the ambient temperature calibration is required to exclude the aforementioned effects.

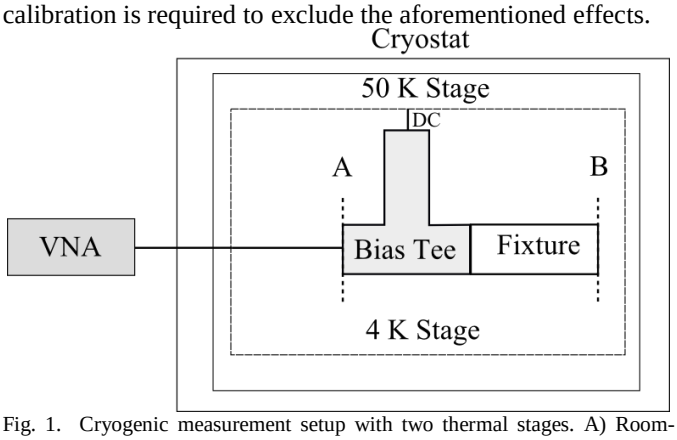

Fig. 1. Cryogenic measurement setup with two thermal stages. A) Room-temperature calibration plane. B) The DUT's reference plane

V. Calibration

Amongst calibration methods for one-port setups, the Short-Open-Load (SOL) can calibrate out the unwanted effects and move the reference plane of the measurements to the DUT's plane. However, this requires three cooling cycles in addition to the DUT measurement. Herein, we have improved time efficiency by an insignificant compromise of the calibration accuracy. In this calibration method [10], short-open-load calibration is performed at room temperature at the A plane shown in Fig. 1. A short circuit standard, which replicates the DUT geometry is fabricated by removing the AlO_x layer, the top and bottom electrodes are shortened. This short circuit cal-unit is cooled down to 4K. Exploiting the Direct Fixture Compensation (DFC) feature of the Rhode & Schwarz ZVA40, the measurements reference plane is moved to the DUT's. Also, it should be noted that this calibration method, which uses DFC, is considered to have decent accuracy only if the setup is lossless.

VI. Measurement Results

At the first iteration of the measurements, thin film capacitors with known capacitance values were measured to assess the accuracy of the measurements. Later, an SIS junction with the estimated capacitance of ~ 0.9 pF was measured, see Fig.2.

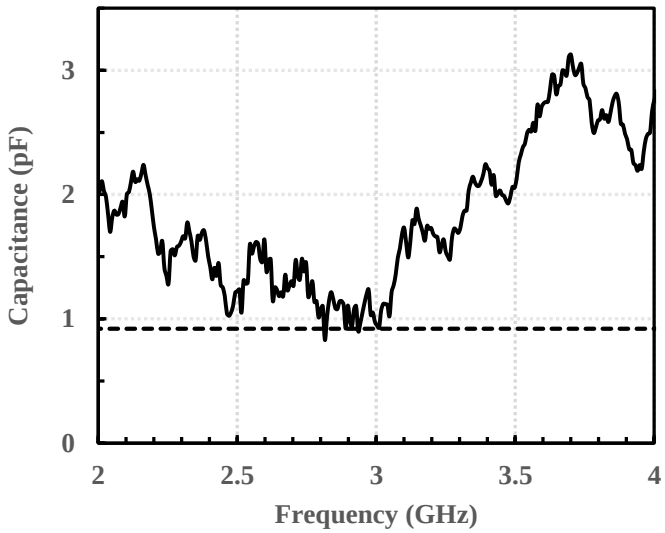

Fig. 2. Capacitance of a SIS junction (solid line) and its estimated value (dashed line) shows a good agreement in the middle of the band.

VII. Conclusion

In this paper we have proposed a new measurement method for the specific capacitance of SIS junction. Developing such measurement method for a complex device parameter such as SIS junctions' specific capacitance requires extensive studies and comparison of the measurements and models. Then, the measurement uncertainties can be approximated and the device parameter can be determined. The uncertainties of this measurement method can mainly stem from the losses. This can be improved by employing new techniques which are not dependent on using terminated lossless transmission line definition for input impedance.

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