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Design and Modelling of a 2 W MMIC Ku-band Power Amplifier for TT&C Transmitters

A collaboration between Chalmers University of Technology and Kongsberg Norspace

Master's thesis in Wireless, Photonics and Space Engineering

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Microwave Electronics Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
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Master's thesis

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Abstract

The *Telemetry, Tracking and Command*, TT&C, communication subsystem is the lifeline of a satellite and is a way to remotely monitor its status. The subsystem can confirm position and angle in relation to the base station as well as make small adjustments to its orbit if needed. The system constantly receives and transmits information and is active from launch to the end of the life cycle where the data is sent by the telemetry transmitter using phase modulation.

In order to minimize power consumption and to ensure a reliable operation of the TT&C subsystem, the output amplifier of the telemetry transmitter must be designed with great care. As collaboration between Chalmers University of Technology and Kongsberg Norspace, the aim of the thesis was to design a 2 W MMIC power amplifier as well as measuring important parameters of a commercial equivalent to use as a benchmark. By investigating different topologies and techniques the amplifier size and channel temperatures were kept down while the design achieved the desired output power.

Various processes and bias points were reviewed before selecting PPH25X from UMS as a base for the MMIC design. PPH25X is a space qualified process using pHEMT transistors that possess high power density to ensure the wanted output power. The simulated amplifier uses three stages with 14 active devices in total to keep the temperature down in the output stage. Different techniques were used to make the active devices stable and to achieve a flat gain throughout the band. The final design achieved a $P_{1\,dB}$ of 33.3 ± 0.3 dBm with a gain and gain variations of 25.4 dB and $0.45\,^{dB}/_{500\,MHz}$ respectively, at a maximum channel temperature of 95 °C.

Keywords: MMIC, Ku-Band, 2W,TT&C, Power Amplifier, Negative Feedback, PPH25X

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Nomenclature

f_c	Cut-off frequency
F_N	Noise figure
G_{TU}	Unilateral Transducer Gain
G_T	Transducer Gain
GS	Ground station
K	Stability factor
$P_{1\,\mathrm{dB}}$	Output power at 1 dB compression
PAE	Power added efficiency
RL	Return Loss
SC	Spacecraft
U	Unilateral Figure of Merit
Z_c	Characteristic Impedance
DRC	Design Rule Checking
DUT	Device Under Test
EM	Electromagnetic
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
LNA	Low Noise Amplifier
MoM	Moment of Methods
NF	Negative Feedback
PA	Power Amplifier
RF	Radio Frequency
Si	Silicon
SiC	Silicon Carbide
SMPA	Switch Mode Power Amplifier
SNR	Signal-to-Noise Ratio
TT&C	Telemetry, Tracking & Command
VNA	Vector Network Analyser

Contents

1 Introduction

1.1 Background

The Telemetry, Tracking, and Control (TT&C) is a subsystem that is critical to ensure a connection between the ground station and the satellite. The *telemetry* function provides status updates of the spacecraft's resources such as propellant supply and charging status of batteries but also readings from sun- and star trackers where the latter is used to determine the attitude.

Tracking adds further information of the spacecraft's location and helps to determine where it is heading. By locating and locking onto the transmissions from the ground station with the TT&C system, see figure 1.1, it is possible to deduce the line-of-sight distance, d to the station as well as the radial velocity of the spacecraft $\vec{v}_{radial}$. This is generally done with phase coherence but could also be achieved by Doppler shift.

Command or control is the final element of the TT&C subsystem and relies on the former two to make small adjustments to the spacecraft's orbit and to ensure a continuous operation without any interruptions. This can include reconfiguring and adapting the satellite for new missions e.g. deploying solar arrays or turning on and off thrusters [15]. Simplified, the TT&C is the lifeline of a satellite and maintains active from launch until the end of the life cycle where the signal is amplified by the power amplifier before being transmitted. The power amplifier is therefore a vital subcomponent of the TT&C system and a necessity for operation.

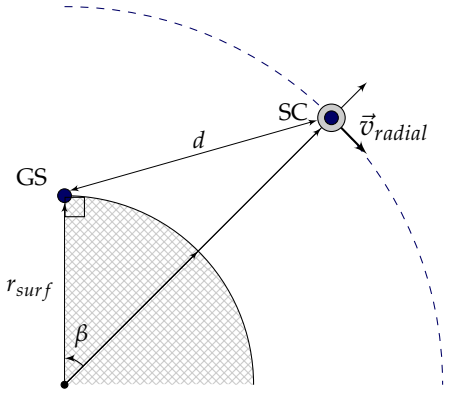

FIGURE 1.1: *The radial velocity of the SpaceCraft (SC) and the Ground Station (GS).*

1.2 Purpose

In the TT&C transmitter chain, the Power Amplifier (PA) is one of the most critical components with a large output power and a high power consumption to follow [4]. With the lack of means to cool the amplifier down it is crucial to keep the efficiency up. In turn, an amplifier with a lower working temperature has a longer life expectancy compared to that of a hotter [5]. In combination with the limited power output in a satellite, the PA's are a natural topic of investigation for reducing the power consumption of the transmitter chain.

1.3 Aim and technical specifications

The goal of the thesis is to present a design of a 2 W Ku-band power amplifier for TT&C transmitters. Based on Monolithic Microwave Integrated Circuit (MMIC) technology the amplifier should be fully consistent with the specifications below in table 1.1 as well as keeping the costs and layout size down.

In addition to the MMIC based amplifier, a commercial design will be evaluated. The measurements will cover all the grounds to be able to use the data as a benchmark for the simulated design. This, to see whether or not the simulated design could be an alternative to the commercial counterparts, for future TT&C applications.

Table 1.1: 2 W Ku-band Power Amplifier Specification

Linear gain	$> 25\,\text{dB}$
Frequency band	$10.7 - 12.75\,\text{GHz}$
Gain flatness	$< {}^{0.5\,\text{dB}}/_{500\,\text{MHz}}$
$P_{1\,\text{dB}}$	$> 33\,\text{dBm}$
Noise figure	$< 7\,\text{dB}$
Input and output return loss	$> 15\,\text{dB}$
DC power consumption	$< 9000\,\text{mW}$
$T_{channel,junction}$	$< 115°C$
$T_{rear-side}$	$(-30, 75)°\text{C}$

1.4 Thesis outline

Chapter 2 and 3 describes the most essential tools that will be used throughout the design phase and will serve as a base for the material and process selection; chapter 2 covers the different types of active devices that are available as well as some considerations concerning temperature, noise and stability. Chapter 3 on the other hand, aims on the different classes of operation of the active device.

The commercial amplifier is reviewed in chapter 4 with large and small signal measurements. The measurements covers the technical specifications that were presented in section 1.3 and are used in chapter 5 where the MMIC design is discussed. Finally, in chapter 6 the results are discussed and summarized and ideas for future work are presented.

2 Theory

The following paragraphs provide the theory and tools that will be used in the upcoming chapters. Starting with efficiency and noise calculations, the chapter and ends with a brief review of different active devices and materials.

2.1 Efficiency

One of the most crucial parameters in amplifier design is the efficiency. Efficiency is a way of measuring the amount of supplied power that is converted into signal power when the remainder is dissipated as unwanted heat. The definition of drain efficiency is stated in equation (2.1).

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.1}$$

Since the drain efficiency does not take the input power into account it can be misleading. A second way of measuring the efficiency was therefore introduced based on the gain called Power Added Efficiency (PAE), see equation (2.2). The equations assume a linear scale and by combining the two it is possible to rewrite the expression to equations (2.3).

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.2}$$

$$PAE = \eta_{drain} \cdot \frac{G-1}{G}. \tag{2.3}$$

PAE is common figure of merit and will henceforth, be used exclusively throughout the thesis.

2.2 Matching networks and stability considerations

All amplifiers are more or less prone to oscillation due to the sensitive terminals of the semiconductor devices. The aim of this chapter is to describe a basic methodology to stabilize an amplifier using small signal, S-parameters.

2.2.1 Unconditionally stable

In terms of size and performance, MMIC circuits are unsurpassed but the same traits often makes modifications after production inconceivable. It is therefore essential that the circuit does not suffer from drawbacks such as instability.

For an amplifier to be unconditionally stable it needs to satisfy the criteria stated in equation (2.4), both inside and outside the specified bandwidth.

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.4a}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.4b}$$

2.2.2 Unilateral and bilateral devices

It is often wise to review whether the device can be considered unilateral opposed to bilateral i.e. if the input depends on the output and vice versa. A bilateral device can impede the matching procedure notably since small variations at one side can have a large overall impact. The analysis is normally done by reviewing the amplifiers scattering matrix and its S_{12} parameter. If S_{12} is close to- or zero, a unilateral figure of merit U, could be calculated with equations (2.5) and (2.6). Where the transducer gain G_T respectively unilateral transducer gain G_{TU} are given by equations (2.7, 2.8). The acceptable level of error depends on the application but ~ 0.1 dB is considered a good rule of thumb [10, 16].

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{(1 - |S_{11}|^2)\,(1 - |S_{22}|^2)} \tag{2.5}$$

$$\frac{1}{(1+U)^2} < \frac{G_{TU}}{G_T} < \frac{1}{(1-U)^2} \tag{2.6}$$

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.7}$$

$$G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}. \tag{2.8}$$

2.2.3 Stability circles and resistive loading

An alternative, graphical method to stabilize an amplifier is to use stability circles in a Smith Chart (SC), see figure 2.1. The stability circles represent an area within the SC for which the amplifier is either stable or unstable depending on the scattering parameters S_{11} and S_{22}. An $|S_{11}| < 1$ corresponds to a stable circuit if Γ_S is located outside- while $|S_{11}| \geq 1$ inside, the circle. Where Γ_S and Γ_L are the reflection coefficients seen from the the active device as can be seen in figure 2.2.

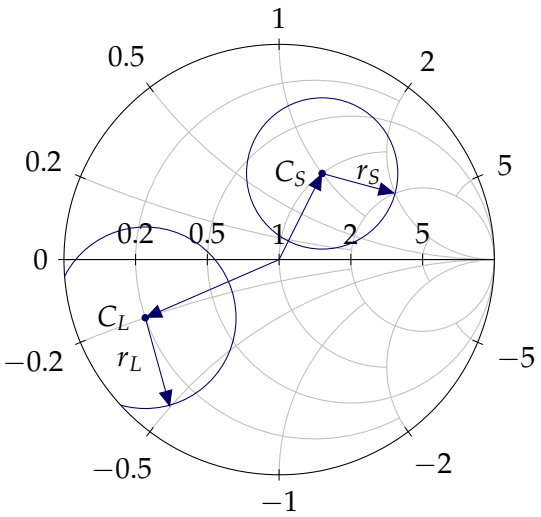

FIGURE 2.1: *Input and output stability circles for a potentially unstable device.*

An unconditionally stable amplifier would therefore correspond to an input and an output circle that are located outside the SC for $\Gamma_{S,L} < 1$. Regardless of which point is chosen for Γ_L and Γ_S, they will remain outside the stability circle and thus satisfying the stability conditions. Furthermore, a $\Gamma_{S,L} \geq 1$ can never become unconditionally stable. The circle would have to enclose the SC which would imply a $\Gamma_{S,L} = 0$ or $Z_L = Z_0$, where Z_0 is the characteristic impedance [10]. The equations for the stability circles are given by equation (2.9) where $C_{S,L}$ is the center of the circle and $r_{S,L}$ is the radius.

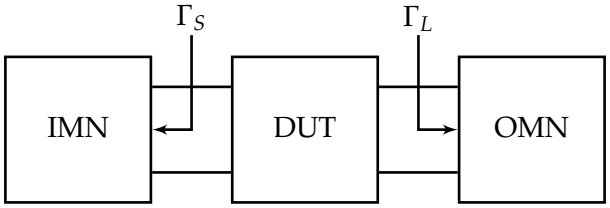

FIGURE 2.2: *A two-port network with reflection coefficients Γ_S and Γ_L where IMN and OMN are the Input- and Output Matching Networks and the DUT is the Device Under Test*

$$C_S = \frac{(S_{11} - S_{22}^* \Delta)^*}{|S_{11}|^2 - |\Delta|^2} \tag{2.9a}$$

$$C_L = \frac{(S_{22} - S_{11}^* \Delta)^*}{|S_{22}|^2 - |\Delta|^2} \tag{2.9b}$$

$$r_S = \left| \frac{S_{12} S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.9c}$$

$$r_L = \left| \frac{S_{12} S_{22}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.9d}$$

A common way of stabilizing an amplifier is to connect a shunt or a series resistor on either the input or output, commonly known as *resistive loading*. The placement of the resistor is dependant of the application; a resistor on the input will reduce the amplitude of the input signal and lower the Signal-to-Noise Ratio (SNR). While it is generally an acceptable approach for a PA, it could notably affect the noise performance of a Low Noise Amplifier (LNA).

On the other hand, a resistor on the output would significantly reduce the output power of an power amplifier. The amplifier would not be able to differentiate the resistor from the load and a significant part of the output power would be lost in dissipated heat.

With the currently available simulation tools, a simple way of calculating the normalized resistor values would be to use the equation (2.10a) for the shunt resistor, $\bar{g}_{S,L}$, and (2.10b) for a series resistor, $\bar{r}_{S,L}$.

$$\bar{g}_{S,L} = \frac{(r_{S,L} + 1)^2 - |C_{S,L}|^2}{|C_{S,L} + 1|^2 - r_{S,L}^2} \tag{2.10a}$$

$$\bar{r}_{S,L} = \frac{(r_{S,L} + 1)^2 - |C_{S,L}|^2}{|C_{S,L} - 1|^2 - r_{S,L}^2} \tag{2.10b}$$

Where $C_{S,L}$ and $r_{S,L}$ are substituted with respective variables found in equation (2.9) [8].

2.3 Noise considerations

The Noise figure F_N, is often overlooked in power amplifier design since the signal is usually amplified by a preceding driver stage and has therefore a high SNR. While F_N is uncritical for power amplifiers, it is an important parameter in general amplifier design and is therefore discussed here.

In figure 2.3 a cascaded system is depicted where each block represents either a component in a system or a stage in an amplifier. By evaluating equation (2.11) it becomes apparent that the first components in the chain have the largest impact on the noise performance. The noise contributions from the following components are inversely scaled by the the gain, of the earlier stages. Thus, to maximise the noise performance the first stages should have as low noise as possible and high gain while the final components in the cascaded system are less critical for the overall noise performance [16].

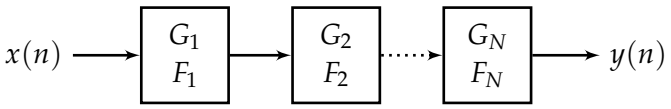

FIGURE 2.3: *The noise figure in a cascaded system.*

$$F_{N,Cascade} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2.11}$$

2.4 Analytical temperature modelling

Temperature estimation of a device is an essential tool when designing an amplifier and will influence the entire design phase. By lowering the temperatures of a circuit the long-term reliability increases which is highly desirable in space applications.

Darwish et al. has presented a model to accurately determine the temperature of FETs and pHEMTs [5, 6]. The model which the author verified by experiments, proved to deviate with less than 2 % compared to the measured values and will henceforth be used to determine the temperature of an active device.

To increase the accuracy of the model the author divides the device into two regions, region-I and II, see figure 2.4. In region I, the heat is propagated radially out from the channel whereas in region II the heat is propagating downwards [6]. The two regions are thereafter summarized achieve the total thermal resistance, θ_{total} (2.12).

$$\theta_{total} = \theta_{\mathrm{I}} + \theta_{\mathrm{II}} \tag{2.12}$$

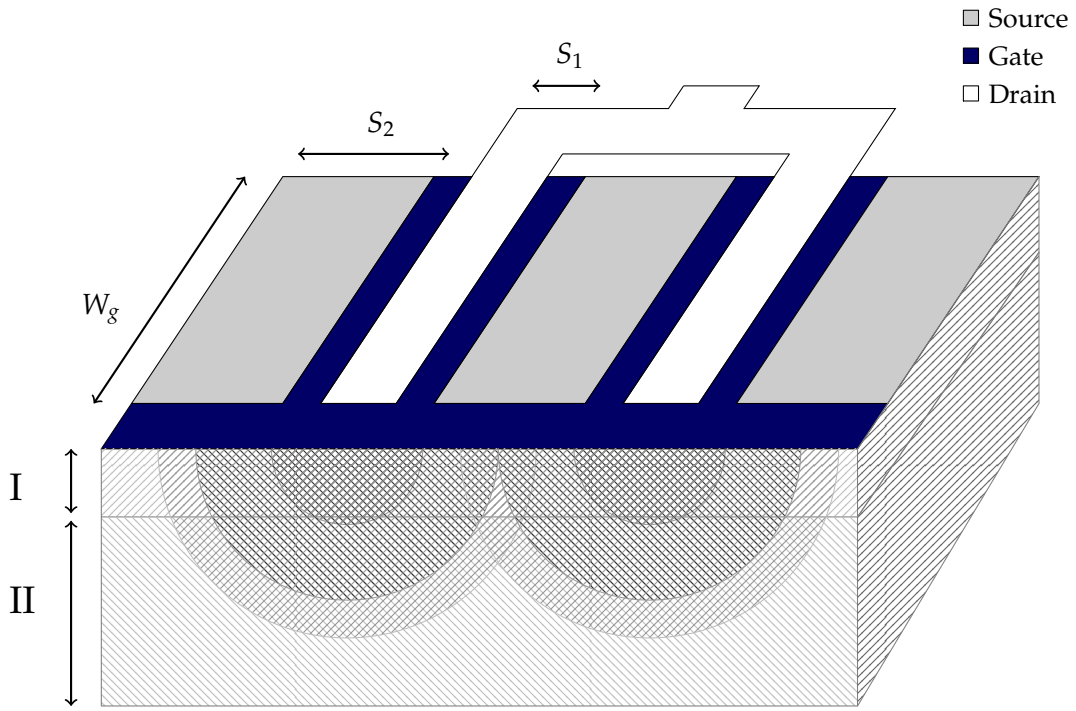

FIGURE 2.4: *The thermal propagation in the active device.*

The two different regions properties are modelled by equations (2.13) and (2.14) which are stated below.

$$\theta_1 = \frac{1}{\pi W_g k} \cdot \ln\left[\frac{f\left(g(\sqrt{2}s)+1\right)-1}{f\left(g(\sqrt{2}s)+1\right)+1} \cdot \frac{f\left(g(L_g)\right)+1}{f\left(g(L_g)\right)-1}\right] \tag{2.13a}$$

$$g(y) = \left(\frac{W_g}{y}\right)^2 \tag{2.13b}$$

$$f(x) = \sqrt{\frac{\sqrt{x}+1}{\sqrt{x}-1}} \tag{2.13c}$$

$$g(y) = \left(\frac{W_g}{y}\right)^2 \tag{2.13d}$$

$$\theta_2 = \frac{1}{2\pi s k} \cdot \ln\left[\frac{h(2.3t)}{h(s)}\right] \tag{2.14a}$$

$$h(x) = \frac{\sqrt{2x^2+W_g^2}+\sqrt{2}x}{\sqrt{2x^2+W_g^2}-\sqrt{2}x}. \tag{2.14b}$$

By rewriting equations (2.13, 2.14) the total thermal resistance can be expressed as equation (2.15), where parameters L_g, t, s and k are the total gate length, substrate thickness, finger spacing and thermal conductivity respectively.

$$\theta_{total} = \frac{1}{\pi W_g k} \cdot \ln \frac{V\left[f\left(g[\sqrt{2}s]+1\right)\right]}{V\left[f\left(g[L_g]\right)\right]} + \frac{1}{2\pi s k} \cdot \ln\left(\frac{h(2.3t)}{h(s)}\right) \tag{2.15a}$$

$$V(z) = \frac{z-1}{z+1} \tag{2.15b}$$

Where the channel temperature, $T_{channel}$ is the product of the total thermal resistance and the dissipated power in the device,

$$T_{channel} = \theta_{total} \cdot P_{diss} \tag{2.16}$$

Equation (2.15) does not account for variations in the thermal conductivity so to improve the accuracy further a Kirchoff transformation was applied to equation (2.16). The final expression can be viewed in equation (2.17) where the thermal conductivity is valid for GaAs devices.

$$T_{channel} = \left(T_0^{-0.23} - 0.23 \left[\theta_{tot}^{s} P \right] T_0^{-1.23} \right)^{-1/0.23} \tag{2.17a}$$

$$k(T) = 56873 T^{-1.23} \,\mathrm{W/m\,K}. \tag{2.17b}$$

2.5 Different types of active devices

The following section will briefly discuss the different types of active devices that are available for MMIC processes. By reviewing the operation and properties, the aim of this section is to aid the selection of a specific device for the modelled amplifier.

2.5.1 Bipolar junction transistors

Bipolar junction transistors operates similarly to FET. According to [12], a common misconception of Bipolar transistors that it is a current controlled device. It is probably due to the current gain beta β, which is a ratio between the base current and the collector current. This transistor type is indeed voltage controlled and it is quite similar to FET operations. The difference is that it requires different control voltages on base. Typically biased with V_{CC} +5 V on the collector while the emitter is grounded, so that current can flow from collector to emitter. In other words, the current is controlled by the voltage V_{BE}. If $V_{BE} = 0$ V, then the transistor is switched "off" and no current will pass. Instead if the voltage between the base and the emitter is larger than 0.7 V, $V_{BE} > 0.7$ V, then the current will start to flow and the transistor will be switched "on" [12].

Bipolar transistor regions (collector, base and emitter) can either be doped n-p-n or p-n-p, where n-type is for negative charge and p-type is for positive charge, leading it to have a p-n junction. An example of a n-p-n doped BJT can be seen in figure 2.5.

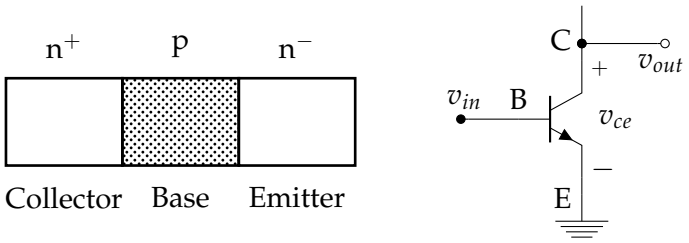

FIGURE 2.5: *The figure shows a n-p-n doped BJT.*

2.5.2 Heterojunction Bipolar Transistor, HBT

Heterojunction bipolar transistors are similar to BJT. The difference is the base-emitter junction which is a junction between two different substrates. Examples of different base-emitter substrates are, AlGaAs emitter and GaAs base, InGaP emitter and GaAs base, InP emitter and InGaAs base [17]. It is wanted to have high injection efficiency which is a ratio between electrons that are injected from emitter into the base and holes that are injected from the base into the emitter. HBT obtaines its injection efficiency by having different band-gap energy levels at the junction. This means that the base can get heavily doped which leads to less base resistance. By having the base resistance reduced, the device transit time is also reduced. Leading the device to have increased frequency response [17].

2.5.3 Field Effect Transistor, FET

The basic principle of how FETs operate is that it is typically biased with a positive drain voltage, V_{DD}, while the source is grounded. The resulting effect is that current can flow from drain to source, known as the drain current I_D. The gate source voltage, V_{GS} is controlling the drain current. For example, if the $V_{GS} = 0$ V then the drain current can pass which means that the FET is switched on. Instead if the gate voltage is large or negative enough, for example -5 V, then no current will pass. The effect will be that the transistor is switched off.

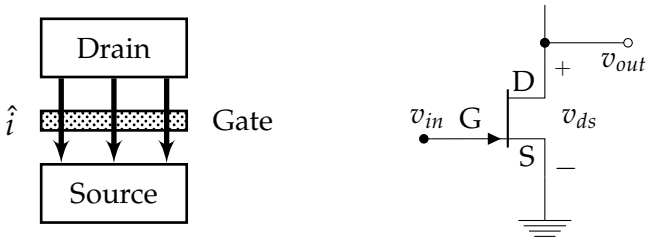

FIGURE 2.6: *The figure gives a top view of a FET where it shows the current-flow.*

The figure 2.6 shows a top view of a FET. The current is flowing across the substrate surface and passing under the gate contact [12]. Figure 2.6 is an example when one gate finger is used but in power amplifiers, several gate fingers are used where the fingers are interconnected with the drain and source terminals.

Couple of examples of FETs are metal-semiconductor field effect transistor MESFET and high electron-mobility transistor HEMT.

2.5.4 Metal Semiconductor Field Effect Transistor, MESFET

The name metal semiconductor field effect transistor is called because there is a metal to semiconductor junction at the gate contact [12]. A MESFET consists of two ohmic contacts (gate and source) and metal-semiconductor Schottky barrier (gate) [17]. When operational, the current passes via conduction channel from source to drain under the gate contact. The current flow is parallel to the surface of the device while in bipolar device, the current travels perpendicular to the surface. Also MESFET is unipolar which means that current is carried either by electrons or holes. This is also different from bipolar devices. In bipolar devices the transport relies both from electrons and holes. In general MESFETs, the current is carried by electron which makes the channel n-type.

2.5.5 High Electron Mobility Transistor, HEMT

HEMTs are similar to any other FETs in operation. The difference is that the channel has a junction of two different semiconductor materials. This gives the free electrons a higher channel mobility. Also other improvements are high frequency noise and gain charateristics [17]. An example of a HEMT would be a material combination between GaAs with AlGaAs where AlGaAs forms doped and undoped layers.

The process selection for MMICs for PAs is mostly determined by operating frequency and efficiency required. At low microwave frequencies, <10 GHz, MESFET and HBT can be used. HBT is usually more efficient. Instead at millimeter-wave frequencies, >10 GHz, high electron mobility are most common used processes [12].

3 Class of operation

One of most important aspects when deciding on amplifier topology, is the amplifier application. All topologies have their benefits and drawbacks depending on what the desired application is. Switching Mode Power Amplifiers (SMPAs) with their subclasses were therefore rejected as the design operates within the Ku-band. At these frequencies and with the limited selection of space qualified processes, active devices cannot act as a switch due to the inability to sweep fast enough through the linear region [4]. The following chapter will thus only describe different linear classes and in end of the chapter, a class will be chosen for the power amplifier design in this thesis.

3.1 Class A

The conduction angle of a class A amplifier is 2π. This means that the transistor is conducting during a whole cycle of the input signal, see figure 3.1. This amplifier class has excellent linearity which means that the output signal has a good resemblance of the input signal. For example, if the RF signal is sinusoidal, then the output current will also be sinusoidal. A big drawback of this amplifier, is that it has low efficiency.

In order to calculate the maximum efficiency this class can obtain, the bias point needs to be defined. The DC current and voltage is biased at $I_{max}/2$ and $V_{max}/2$, respectively. Using the defined bias points, one can calculate the maximum efficiency class A can obtain [4], see below.

$$I_{DC} = \frac{I_{max}}{2} \quad V_{DC} = \frac{V_{max}}{2} \tag{3.1}$$

$$P_{DC} = 1/4 \cdot I_{max} V_{max} \tag{3.2}$$

$$P_{RF} = 1/2 \cdot V_{RF} \cdot I_{RF} = 1/8 \cdot V_{max} \cdot I_{max} \tag{3.3}$$

Where P_{DC} is the DC power for the given bias points and P_{RF} is the RF output power. To calculate the efficiency, one can use the equation (2.1).

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{1/8 \cdot V_{max} \cdot I_{max}}{1/4 \cdot V_{max} \cdot I_{max}} = 50\% \tag{3.4}$$

The maximum efficiency a class A amplifier can obtain is 50 %. Other advantages this class has are high gain, low distortion, broad bandwidth and good noise figure [2].

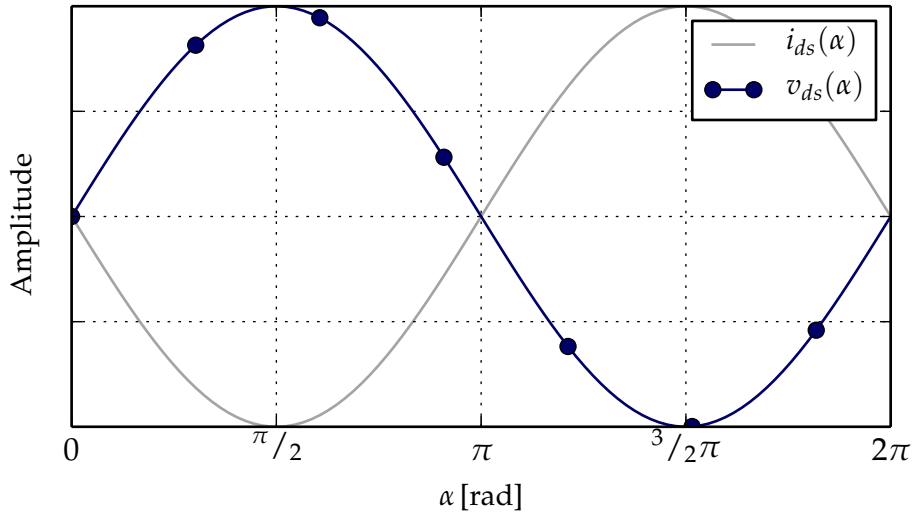

FIGURE 3.1: *Class A biasing, the device stays active throughout the* 2π *interval.*

3.2 Class B

The conduction of a class B amplifier is half of the input signal cycle. In other words, it has a conduction angle of π, see figure 3.2. This type of amplifier class is biased at the pinch-off, where it stops conducting. As an example for where the pinch-off is, see figure 3.3. The advantage of this class compared to class A, is that it has higher efficiency. It can be shown by defining the biasing points,

$$I_{DC} = \frac{I_{max}}{\pi} \quad V_{DC} = \frac{V_{max}}{2} \tag{3.5}$$

where the DC power becomes,

$$P_{DC} = {}^{1}/_{2\pi} \cdot I_{max} V_{max}. \tag{3.6}$$

Finally, equations (3.3) and (2.1) can be used to obtain the final expression for the drain efficiency.

$$\eta = {}^{\pi}/_{4} \cdot \frac{I_{max} \cdot V_{max}}{I_{max} \cdot V_{max}} = 78.5\% \tag{3.7}$$

The difference from class A is that it has a current bias point on the pinch-off. This makes the effectivity to increase. However, it is less linear and will produce harmonic distortion [18].

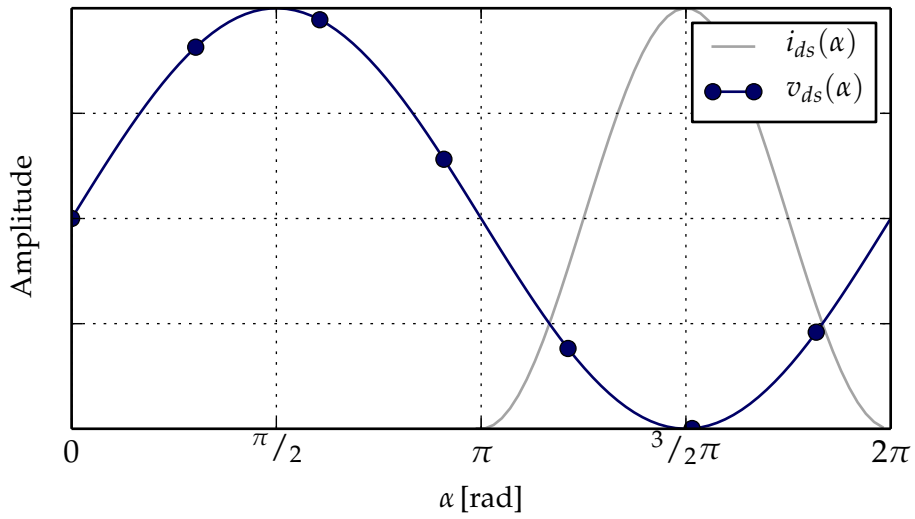

FIGURE 3.2: *Class B biasing, the device stays active throughout the π interval.*

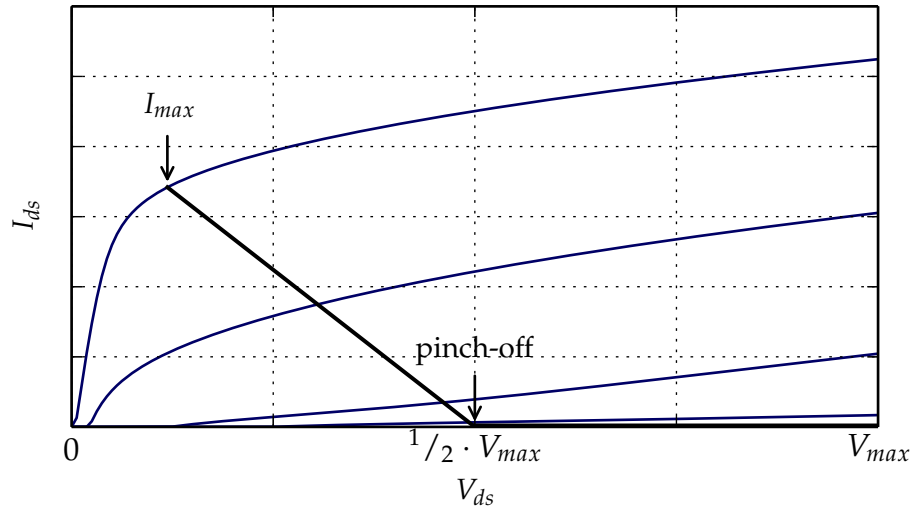

FIGURE 3.3: *The figure shows the IV characteristic for a class B amplifier.*

3.3 Class AB

In terms of linearity and efficiency, this class is a compromise between class A and class B. The conduction angle is between π and $2\,\pi$. Varying the bias point will result in a variation in linearity and efficiency. This is because of the presence of higher order harmonic waves and the DC component. According to [4], these waveforms can be analysed by using the equations below.

$$I_{DC} = \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot d\theta \tag{3.8}$$

Where I_{DC} is the DC component, α is the conduction angle and I_{max} is the saturated point. Expression for the higher order harmonic waves can be seen below.

$$I_n = \frac{1}{\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot \cos n\theta d\theta \tag{3.9}$$

I_n is the current waveform for nth order. For simplicity, $n = 5$ will be used. The DC component and the fundamental order which is the first order of the harmonic wave is evaluated.

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2 \cdot \sin(\alpha/2) - \alpha \cdot cos(\alpha/2)}{1 - cos(\alpha/2)} \tag{3.10}$$

$$I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \tag{3.11}$$

Equation (3.10) and (3.11) is the case when $n = 5$. Using these informations, a plot can be obtained.

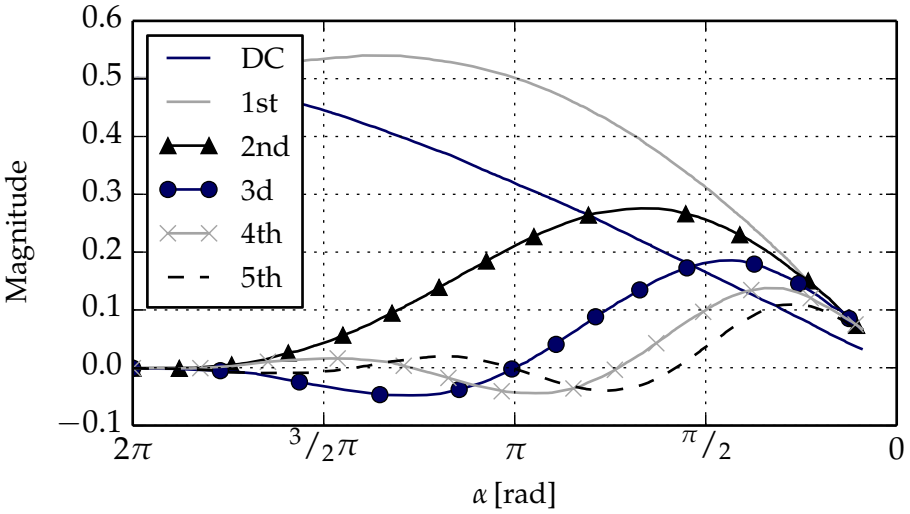

FIGURE 3.4: *The figure is showing the fifth order waveforms as function of the conduction angle.*

It can be seen from figure 3.4 that when the conduction angle is 2π, the amplitude of the drain current is $I_{max}/2$. This is the case when class A is used. Instead if class B is used, the amplitude becomes I_{max}/π when the angle is π. Between in those angles, class AB is born.

Class AB is biased between the cut off and class A biasing point. Choosing the bias point can be challenging because it is a trade off between efficiency and linearity. The most common is to choose the bias point close to the "pinch-off" (deep class AB) so the conduction angle becomes close to π. This is because of the fundamental which is then higher than class A fundamental. Also, the DC component is decreasing as the conduction angle decreases. These two effects make the efficiency be higher for class AB and class B comparing with class A. As it is more efficient, it is also less linear. This is because of the higher order of harmonic modes that are present. For class B, the odd harmonics modes are neglected but for class AB, it cannot be neglected.
For power amplifiers, it is important to have high output power and efficiency. Therefore it is important to analyse the output power and efficiency for different conduction angles. Below can it be seen mathematical expressions when the RF output power and efficiency is α dependant.

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} = \frac{\frac{V_{DC} \cdot I_1}{2}}{V_{DC} \cdot I_{DC}} = \frac{1}{2} \cdot \frac{I_1}{I_{DC}} \tag{3.12}$$

Using equation (3.10) and (3.11), the final expression for η_{drain} and RF output power can be obtained.

$$\eta_{drain} = \frac{1}{4} \cdot \frac{\alpha - \sin\alpha}{\sin(\alpha/2) - \alpha/2 \cdot \cos(\alpha/2)} \tag{3.13}$$

$$P_{out} = \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \tag{3.14}$$

One can use equation (3.13) and (3.14) in order to obtain a figure, see figure below.

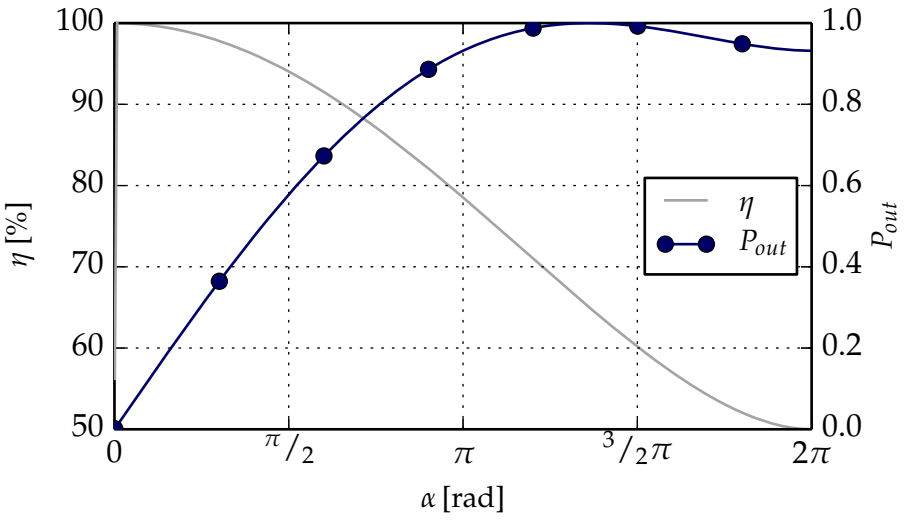

FIGURE 3.5: *The figure is showing the output power and efficiency over the conduction angle.*

As it can be seen from the figure 3.5, the RF output power is increasing between $0 < \alpha < \pi$ and is at its peak between $\pi < \alpha < 2\pi$. The efficiency is at its peak at $\alpha = 0$ and is decreasing significantly when the conduction angle is approaching to 2π.

3.4 Class C

This class has a conduction angle of less than π, see figure 3.6. This makes it to have the highest efficiency compared to all of the other classes. As it has higher efficiency, it will also have lowest output power, see figure 3.5. In theory, if the conduction angle goes to 0 degrees, the efficiency will reach 100%. Also when the efficiency reaches 100%, the output power goes towards 0.

It is important to note that this class is the poorest one in terms of linearity compared with all other classes. Poor linearity is because of the high harmonic levels that are present, which makes the output signal highly distorted.

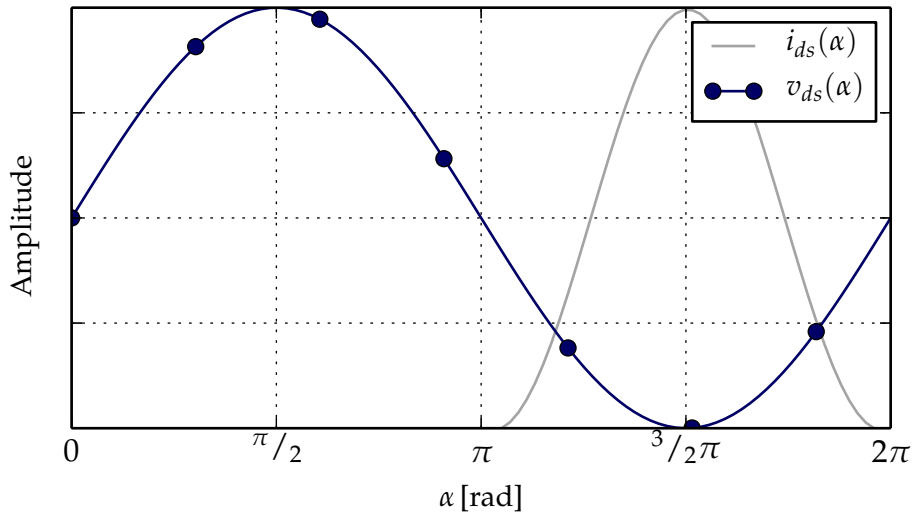

FIGURE 3.6: *Class C biasing, the device stays active in a region less than π interval.*

3.5 Summary

In this section, all presented classes has been summarized and compared with each other. Also in the end of this section, a class will be chosen for the PA that will be designed later on.

To start with, one of the main differences between class A, class B, class AB and class C is the conduction angles. Thus giving different linearities, efficiencies and output powers. Figure 3.4 is showing the waveforms for different classes. It can be seen that the fundamental wave is at its highest peak when $\pi < \alpha < 2\pi$ while the DC component is decreasing. This is for class AB. Because of this behaviour, class AB has highest output power. This can also be seen in figure 3.5.

In terms of linearity, class A is the superior one. Figure 3.4 is showing no presence of higher order harmonic waves when $\alpha = 2\pi$ leading this class to be most linear. For class C, it can obtain 100 % efficiency when the output power goes to 0. Even if this class can obtain high efficiency, it cannot deliver high output power. Also note that class C is the poorest in terms of linearity because in the region $0 < \alpha < \pi$, the fundamental wave is low while the even and odd harmonic waves are present.

For our design the best choice is class AB. This is because the design should deliver as much output power as possible. Also it can obtain a theoretical efficiency between 50 -78.5 %.

4 Commercial prototype

For evaluation purposes, measurements of a commercial design were conducted and evaluated at the facilities of Kongsberg Norspace in Horten, Norway. The amplifier would be used as a benchmark as well as giving input and ideas on how the own design could be implemented.

4.1 Equipment and specifications

The HMC1053 by Hittite was chosen as the commercial counterpart and its specifications can be viewed in table 4.1. The amplifier deviated from the desired specifications but assumption was that by using a lowered bias; a result that was more consistent with the desired specifications, could be achieved.

Table 4.1: Typical properties of Hittite HMC1053 at room temperature with $I_{DD} = 2400\,\text{mA}$ and $V_{DD} = 7\,\text{V}$.

Property	HMC1053	Requested
Frequency range	9-14 GHz	10.7-12.75 GHz
Gain	34 dB	>25 dB
Input Return Loss	30 dB	>15 dB
Output Return Loss	19 dB	>15 dB
$P_{1\,\text{dB}}$	35.5 dBm	≥33 dBm

The set up can be viewed in figures 4.1 and 4.2 where the tools that were used to measure the properties of the amplifier are specified in table 4.2. The Vector Network Analyser (VNA) was rated for measurements up to 40 GHz and the attenuators approved for Ku-band (10.7–12.75 GHz) applications. An HP E3631A, one of the power supplies, was used to bias the gates on the amplifier and since there was only one output on the power supply, a bond wire was connected on the outside of the gate capacitors, see figure 4.3.

Adding bond wires introduces extra inductance which in turn could make an amplifier unstable, however there were no tendencies for oscillations observed during the measurements. Unlike the E3631A, Hewlett Packard E3632A has two outputs that were used to supply both drains with voltage.

Table 4.2: The test equipment used to measure the amplifier properties.

Type	Quantity	Description
Network Analysers	1	Rohde & Schwartz ZVA40
Power Supplies	1	Hewlett Packard E3632A
	1	Hewlett Packard E3631A
Attenuators (Ku)	2	10 dB, 2 W
	1	20 dB, 20 W

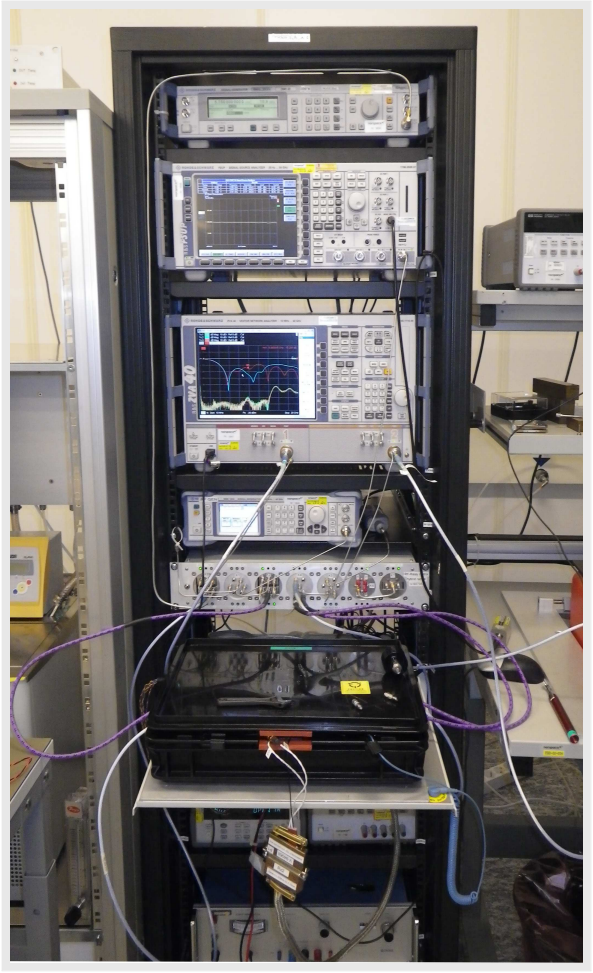

FIGURE 4.1: *The equipment used to measure the small and large signal parameters.*

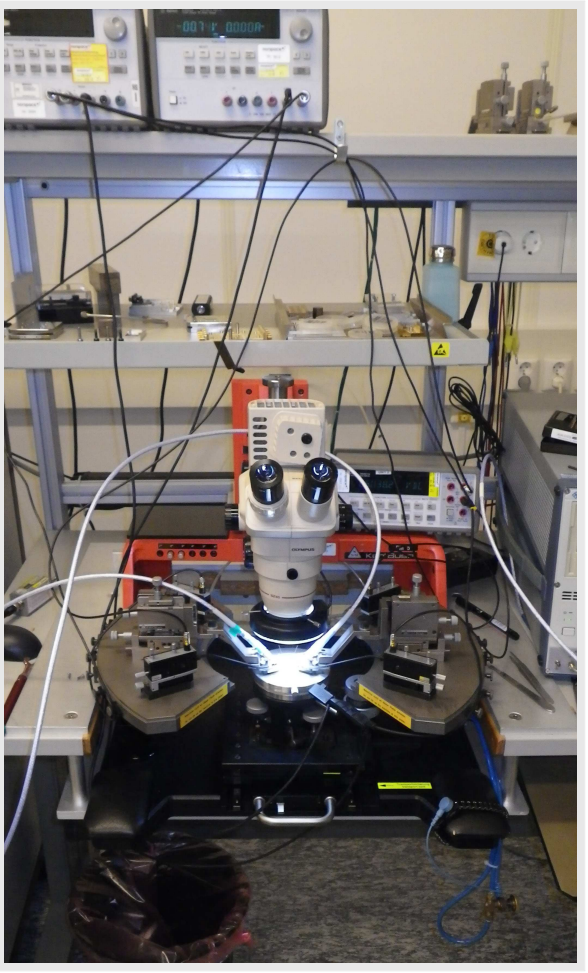

FIGURE 4.2: *HMC1053 mounted on the probe station and held in place with vacuum.*

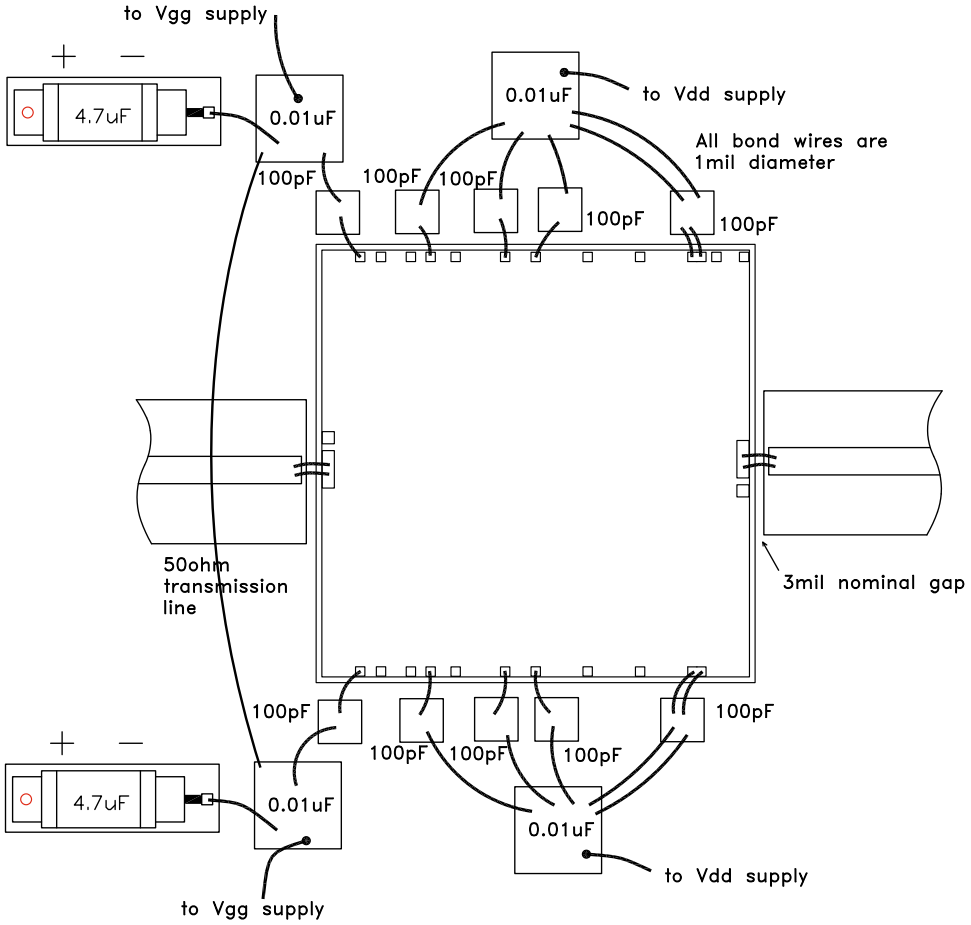

FIGURE 4.3: *Assembly diagram from the Hittite HMC1053 manual with added bond wire connecting the gates [11].*

4.2 Fixture and assembly

Before any large signal measurements could be done, attenuators were put in front of the input and output of the VNA. The attenuators were used as a precaution to prevent the power amplifier from damaging any of the ports. The measuring set up can be viewed in figure 4.4 where DUT and L represents the amplifier and attenuators respectively.

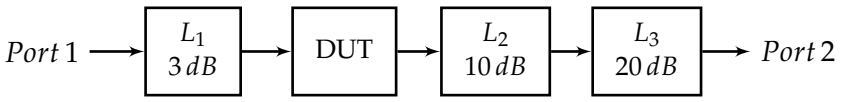

FIGURE 4.4: *The set up for measuring large signal parameters.*

During the measurements of the compression point $P_{1\,\mathrm{dB}}$, the attenuator L_1 was changed from 10 dB, 5 dB and finally to 3 dB. With the highest attenuation as a starting point, it became clear that the output power from the VNA got saturated i.e. the increase in output power did not correspond to the increase in gain. Since it was unknown at what output power the VNA started to affect the measurements, the reduction of attenuation was done in steps. Primarily due to the fear of damaging the input of the VNA (*Port* 2 in figure 4.4). *Note that even if L_1 was reduced to change the output power in the large signal measurements, its function is mainly to reduce the reflected power between the DUT and the VNA. For small signal measurements on the other hand, the mismatch is normally compensated for by the calibration procedure.*

4.2.1 Calibration and bias procedure

Before any measurements could be done, the VNA had to be calibrated so that the cables used for the ports, became parts of the system. This was done by using three different calibration standards; namely *open*, *short* and *through*. Ideally the calibration should have been done with the probes and a calibration substrate. However it was neglected due to assumption that the error introduced by the probe was negligible and due to the limited available time in the lab. Some quick tests were done after the measurements and the deviation in gain was estimated to somewhere around 0.5 dB.

The procedure for the biasing was performed in the following fashion; both the power supplies were turned off so that there was no current flowing. The probes were then put on top of the 0.1 μF capacitor according to figure 4.3 where the amplifier was mounted on top of a conducting substrate that acted as a ground plane, see figure 4.5. The gate voltage was then turned down so that the semiconductor devices in the amplifier were in pinch-off. When it was clear that no current could flow, the drain voltage was turned up to the operating voltage. As the final step, the gate voltage was slowly turned up so that current could flow.

Since the drain current was around 2400 mA, there was a voltage drop that had to be accounted for. It was easily resolved by using a separate voltmeter while turning up the drain voltage. However, increasing the voltage the second time should be done with caution since some of the devices suffer from second order effects [13]. That is, the drain current could be dependent on the drain voltage, by increasing the drain voltage the drain current could increase simultaneously.

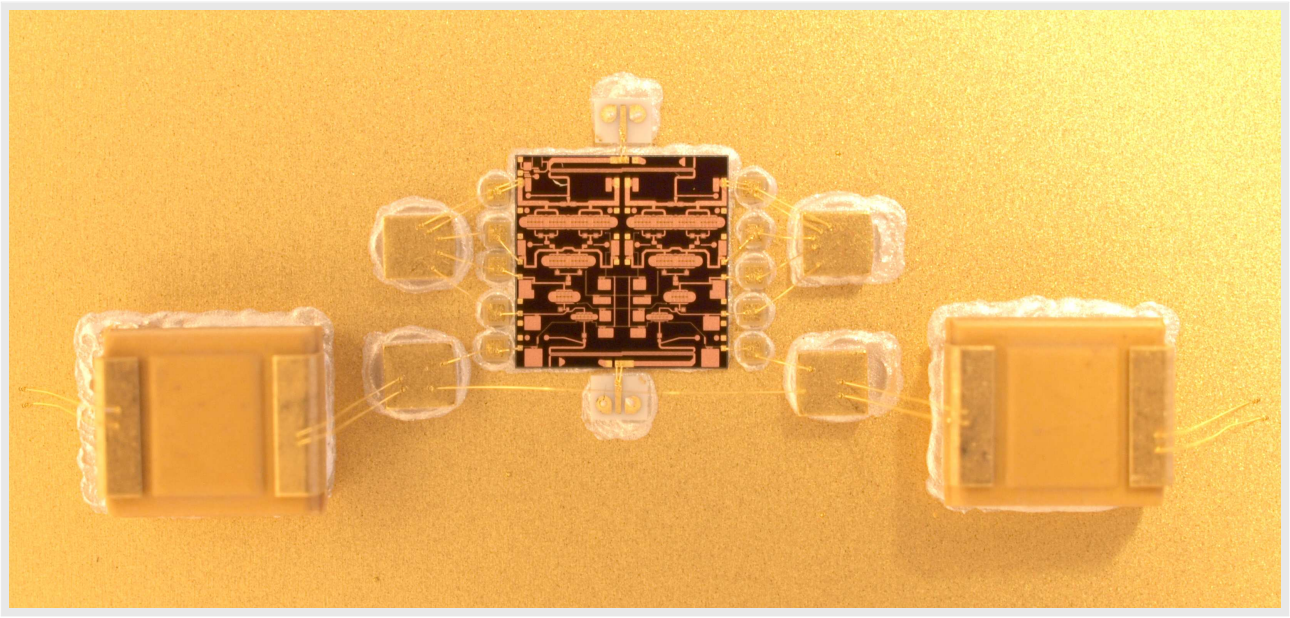

FIGURE 4.5: *The amplifier mounted on a substrate with epoxy and interconnected via bond wires.*

4.2.2 Compression point

Power sweeps were performed at three different frequencies, the lower 10.7 GHz, upper limit 12.75 GHz and in the middle of the frequency band, 11.75 GHz. The expectation was that the amplifier would have higher gain and generally be more consistent with the wanted specifications towards the center frequency rather than the outer borders of the frequency range which proved to be valid.

$P_{1\,\mathrm{dB}}$ was calculated by using a reference point in the middle ($P_{in} = -10\,\mathrm{dBm}$), of the power sweep where the gain is linear. A marker was then moved up to the point until the gain had been reduced by 1 dB. The approach is depicted in picture 4.6.

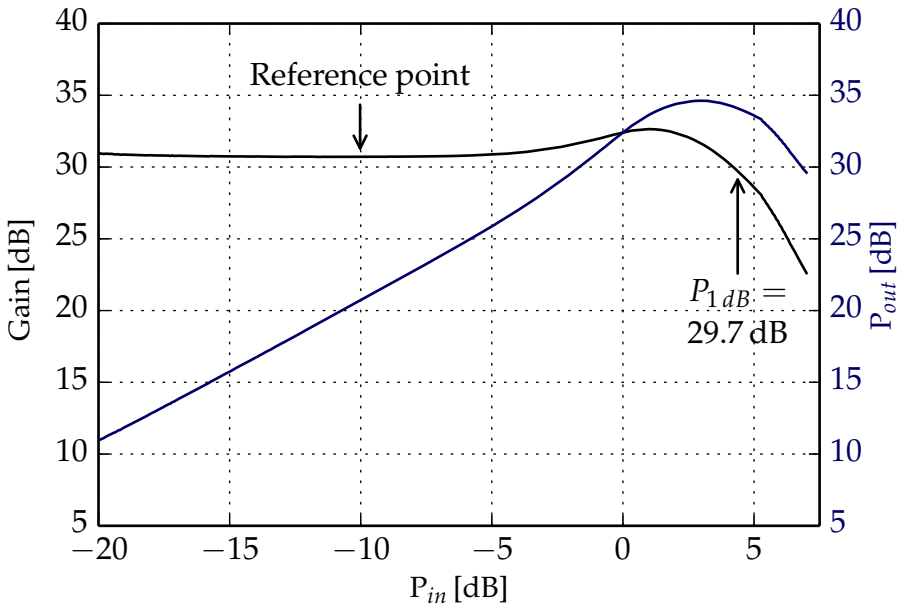

FIGURE 4.6: *The power sweep for HMC1053 at* 10.7 GHz *with* $V_{DD} = 5\,\mathrm{V}$ *and* $I_{DD} = 2400\,\mathrm{mA}$.

Viewing figure 4.6, there is an increase in gain at a $P_{in} = 0\,\mathrm{dB}$ which could be the result of a number of things but there were two main causes that stood out; the amplifier was not cooled during the measurements so thermal related problems is a likely cause. Another reason could be the bias settings that were used during the measurements. Similar behaviour has also been spotted during the design phase when the bias has been less than adequate.

The heat problems and the lack of means to cool the amplifier down further led to that the higher bias settings were left out. The result for all the measured bias settings can be seen in figure 4.7.

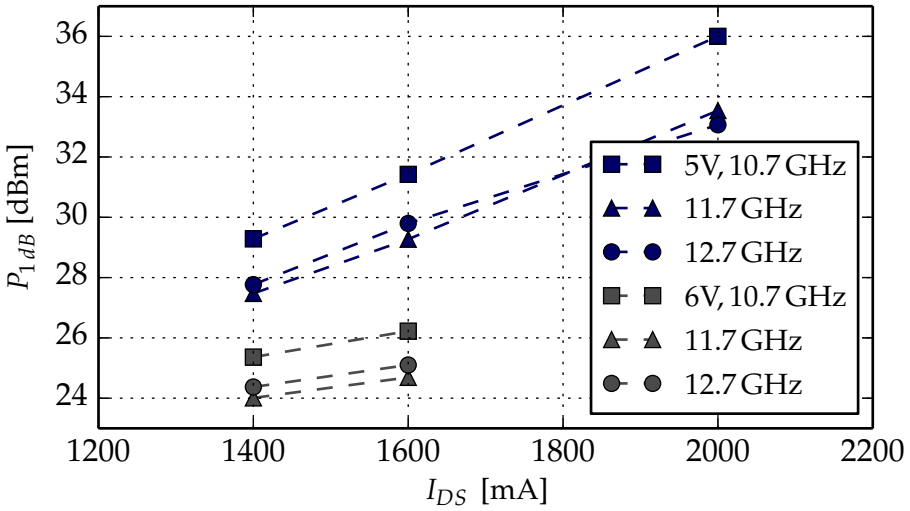

FIGURE 4.7: *Compression point as a function of bias current.*

4.2.3 Small signal gain

The scattering parameters of the amplifier were measured as a complement to the power sweep. The measurement was done by using a VNA and by sweeping the frequency instead of the input power. By obtaining the parameters it is possible to extract the isolation, gain, stability and reflection coefficients.

The *S*-parameters were measured between 10 MHz and 20 GHz and where the gain corresponds to the S_{21} parameter. To see how the gain scales with different bias settings - the bias settings were looped through and the values were stored away. The minimum gain within the frequency range was stored and the result can be seen in figure 4.8.

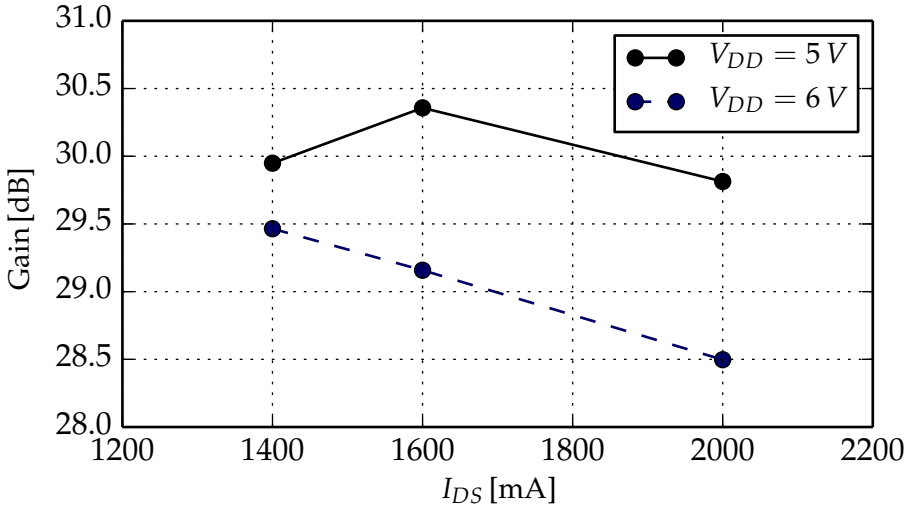

FIGURE 4.8: *The minimum gain within* $10.7 - 12.75$ GHz.

Surprisingly the gain is higher at 5 V compared to that of 6 V. With a lower compression point as well, see in subsection 4.2.2, it begs the question if the behaviour might be temperature related as the compression point generally scale along with the bias current and voltage.

In the project description it was specified that the MMIC design could not have gain fluctuations that exceed 0.5 dB per 500 MHz. To see if the commercial counterpart met the specifications an interval of 500 MHz was used, see the "box" in figure 4.9. Ideally the gain variations should have been measured at 1 dB compression, but since no such measurements were performed the small signal data was used in its place. The difference was then calculated by subtracting the lowest gain from the highest within the box, which in turn, was then moved one sample, 20 MHz up. The described procedure continued until the box reached the end of the frequency range.

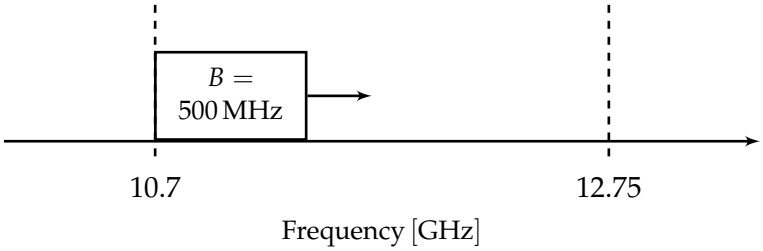

FIGURE 4.9: *Calculating the gain flatness.*

The same method was applied to all the *S*-parameter measurements and the highest value from each bias setting was extracted. This was done to see if the variation in gain was affected by the different bias settings. As can be viewed in figure 4.10, higher drain voltage reduced the variance in gain. In fact, it was only at 6 V that the amplifier could achieve a gain that was stable enough to be used.

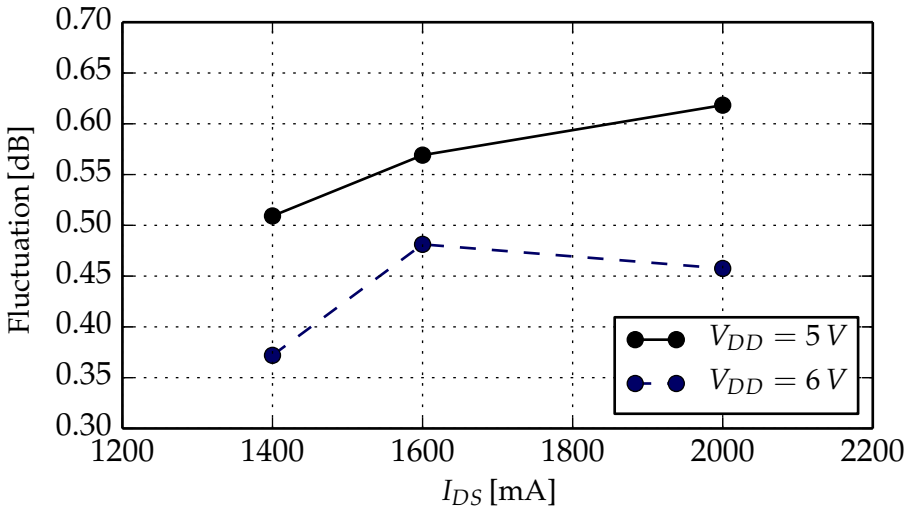

FIGURE 4.10: *The maximum fluctuation in gain for the different bias currents and voltages*

4.2.4 Stability

There were no tendencies for stability issues when the amplifier was correctly terminated which was verified by the Rollet-factor. In figure 4.11 the stability factor K and $|\Delta|$ were depicted for $V_{DS} = 5\,\text{V}$ and $I_{DS} = 2400\,\text{mA}$ in figure 4.11.

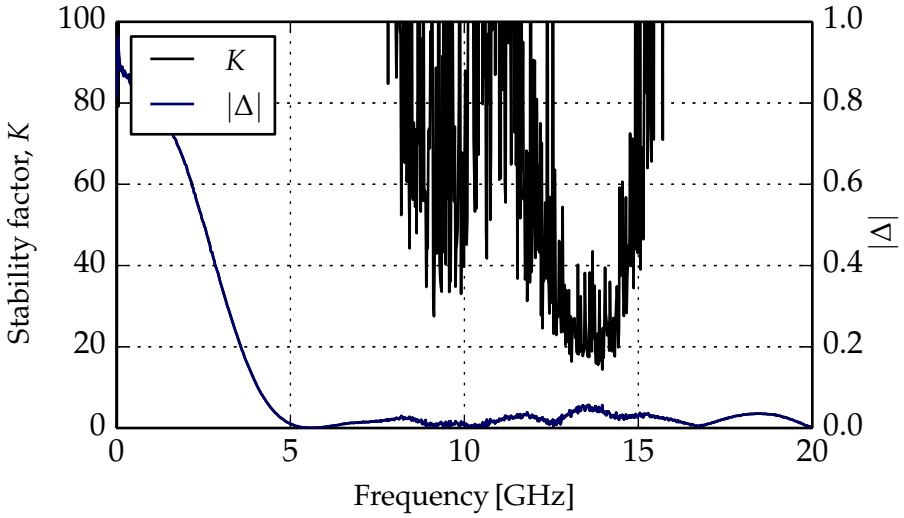

FIGURE 4.11: *Stability factor K and* $|\Delta|$ *at* 10.7 GHz *with* $V_{DD} = 5\,\text{V}$ *and* $I_{DS} = 2400\,\text{mA}$.

Since the results were consistent with the criteria in subsection 2.2.1 the same calculations were done to all bias settings. If there are points that are on the verge of being unstable, it is easy to locate and exclude the specific bias setting. In figure 4.12 both stability factor K and $|\Delta|$ are depicted and it can be seen that an increase in drain current helps stabilizing the amplifier while a high drain voltage reduced the stability.

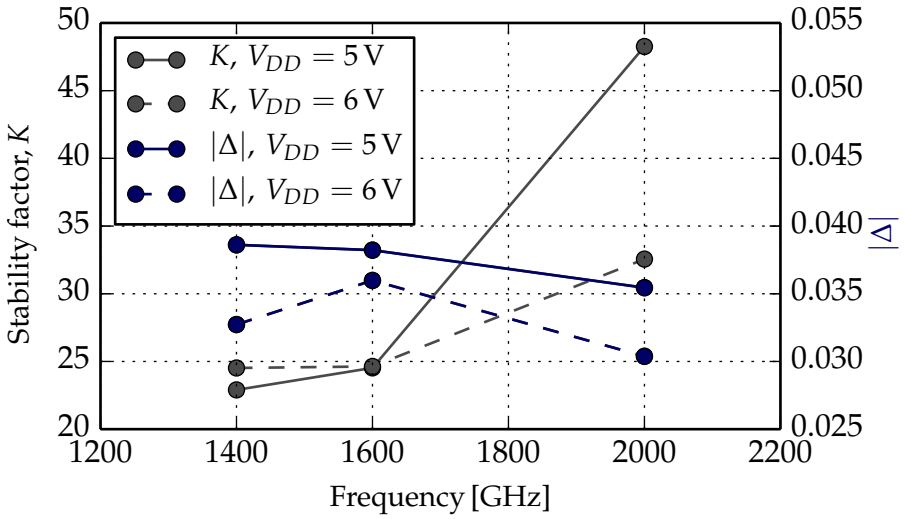

FIGURE 4.12: *Stability factor K and* $|\Delta|$ *for the different bias settings.*

4.2.5 Input and output return loss

Well matched circuits are crucial for systems to work properly and poor matching could result in not only standing waves but also a low power transfer. To measure the power transfer, *S*-parameters S_{11} and S_{22} are defined as the reflected power of a two-port at the input respectively output as can be seen figure 4.13. *Note that the return loss is defined as a non-negative number, which is why the specifications in chapter 1.3 are referred to as positive, see equation* (4.1).

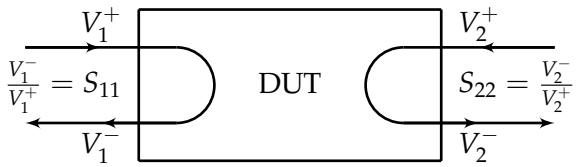

FIGURE 4.13: *The definition of S_{11} and S_{22}.*

$$RL_{in} = -20 \cdot \log_{10} |S_{11}| \tag{4.1a}$$

$$RL_{out} = -20 \cdot \log_{10} |S_{22}| \tag{4.1b}$$

According to the specifications the amplifier should sustain a return loss of 15 dB or more i.e. *S*-parameters S_{11} and S_{22} should be lower than -15 dB. A moving average was applied to the different bias settings to remove excess noise and the worst results were then stored. The results can be seen in figure 4.14. S_{11} fulfils the criteria at all bias settings while the output reflection coefficient on the other hand, only stays below 15 dB at 6 V and 1400 mA respectively 1600 mA

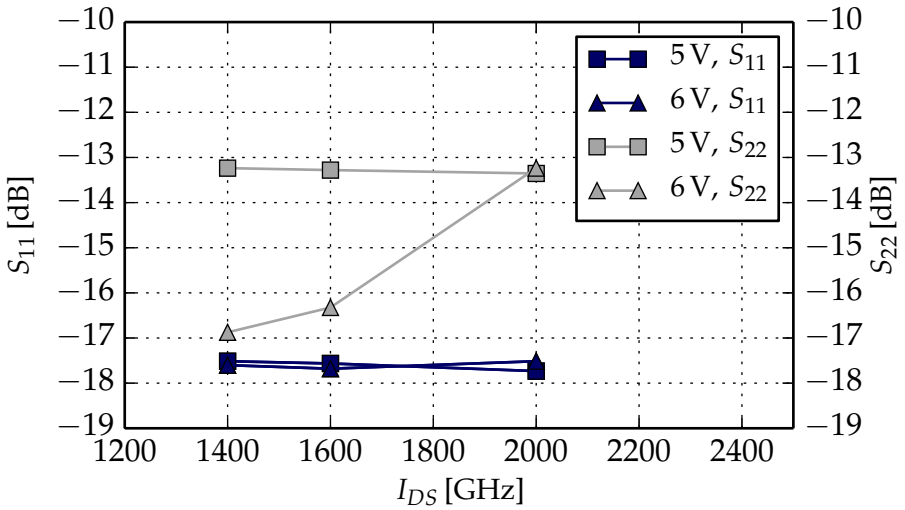

FIGURE 4.14: *Input and output return loss for different bias settings.*

4.3 Efficiency

In this section, the efficiency of the HMC1053 amplifier will be considered. The theory behind it is well explained in chapter 2.1 and will be applied for the HMC1053 amplifier.

In order to estimate the drain efficiency and the PAE, one need to do a power sweep and measure the $P_{1\,\mathrm{dB}}$, Gain and the drain current I_{DS}. As the input signal P_{in} is swept, the drain current starts to vary. The figure 4.6 is an example of a power sweep measurement performed at Kongsberg Norspace in Horten, Norway. It can be seen from the example figure that there are no measurements performed for how the drain currents are varying. Therefore calculations of the efficiencies cannot be performed.

Still it is important to estimate the PAE and the η_{drain} because the temperature model that will be created in the next section will depend on them. As we lacked the data, we decided to use the data from [11]. The amplifier is featured with a $PAE = 26\,\%$ and $\eta_{drain} = 26.5\,\%$ while the DC supply is +7 V at 2400 mA.

The next section will calculate the channel temperature of the HMC1053 and will compare it with the required channel temperature stated in table 1.1.

4.4 Temperature

In this section, the temperature of the amplifier will be calculated. As explained in section 2.4, the temperature of the amplifier is important because the reliability is important for space applications. It is wanted to have as low channel temperature as possible. To calculate the temperature, one can use equation (2.16) available in section 2.4. The total thermal resistivity, θ_{tot}, depends on the thermal conductivity and the geometry of the transistor. Instead of calculating the thermal resistivity, the value of it can be read directly from the data sheet for HMC1053 amplifier [11]. The value of the thermal resistivity is, $\theta_{channel-bottom} = 3.27\ ^{\circ}\mathrm{C}/W$. Note that the $\theta_{channel-bottom}$ is the thermal resistivity from channel to die bottom and not the total.

$$T_{channel-rear} = \theta_{channel-bottom} \cdot P_{diss} \tag{4.2}$$

The equation above is describing the temperature increase from rear to channel for the MMIC amplifier. Therefore the rear temperature is added into the equation (4.2) in order to calculate the channel temperature.

$$T_{channel} = T_{rear} + \theta_{channel-bottom} \cdot P_{diss} \tag{4.3}$$

The dissipated power, P_{diss}, can be thought as how much DC power that is not converted to output power and lost as heat. To visualize this, see the figure below.

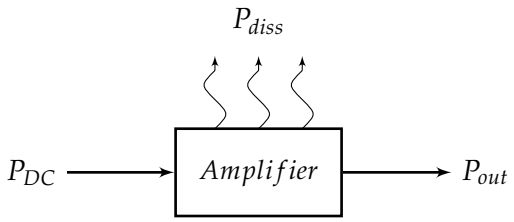

FIGURE 4.15: *Realization of the dissipated power.*

In section 4.3, the efficiency of the amplifier is calculated. Therefore it is practical if a mathematical expression is derived for P_{diss} when it is efficiency dependant.

$$P_{diss} = P_{DC} - P_{out} \tag{4.4}$$

Using equation (2.1) and substituting for P_{out}, the final expression for P_{diss} becomes,

$$P_{diss} = P_{DC} \cdot (1 - \eta_{drain}). \tag{4.5}$$

The summarized equation for $T_{channel}$ can be expressed by using equation (4.3) and (4.5).

$$T_{channel} = T_{rear} + \theta_{channel-bottom} \cdot P_{DC}(1 - \eta_{drain}) \tag{4.6}$$

Assuming the worst case scenario, the maximum rear temperature that is allowed can be read from [11], T_{rear} =85 °C.

The results shows that the HMC1053 amplifier channel temperature is at 125.4 °C when it is supplied with +7 V and 2400 mA. Comparing the result with table 1.1, the specified requirement should not exceed 115 °C. So one can conclude that HMC1053 is having a higher channel temperature.

5 MMIC Design

The following chapter will in detail investigate the necessary steps to design a MMIC PA for Ku-band applications. The inquiry will take both temperature and size into account while satisfying the earlier specified criteria.

5.1 Transistor technology and process decisions

In order to choose a transistor technology, a consideration between GaN FET, GaAs pHEMT and InP HEMT was made. According to [12], InP HEMT is most common when the frequency ranges between 50–100 GHz. As our design requires a frequency 10.7–12.75 GHz, InP HEMT is rejected and GaN and GaAs pHEMT is the most suited technologies. Further investigations showed that the availability of space qualified processes were limited at the time a process was chosen. Therefore a GaAs pHEMT technology was chosen.

After extensive research of different types of processes, the available processes were the PPH25 GaAs pHEMT and PPH25X GaAs pHEMT [20]. The specification comparison between PPH25 and PPH25X is summarized with a table below.

Table 5.1: Comparison between PPH25 and PPH25X processes.

Process	PPH25	PPH25X
Power density	700 $^{mW}/_{\text{mm}}$	900 $^{mW}/_{\text{mm}}$
L_{Gate}	0.25 μm	0.25 μm
$I_{DS}(g_{max})$	200 $^{mA}/_{\text{mm}}$	170 $^{mA}/_{\text{mm}}$
$^{V_{BDS}}/_{V_{BCE}}$	> 12 V	> 18 V
f_c	50 GHz	45 GHz
V_{pinch}	-0.9 V	-0.9 V
$^{g_m\, max}/_{\beta}$	450 mS/mm	400 mS/mm

One can see from the table 5.1 that the PPH25X is having higher power density compared to PPH25 even though it has less transconductance g_m. This means that the PPH25X can deliver more output power with the cost of reduced gain. As the design is required to deliver 2 W at the output, the chosen process is PPH25X. Note that the chosen process has been verified as a space qualified process.

5.2 Power budget

When designing a power amplifier, it is important to be structured. Power budget is a method that gives a notion of how much output power and gain is required from each stage in order to obtain the desired output power. According to [12], the method starts with a couple of assumptions namely,

- Matching network suffers with 0.5 dB loss.
- Power splitters and combiners suffers with 0.5 dB loss.

By knowing the desired output power, 33 dBm, one can decide the required output power from each transistor at each stage. The question is whether to design a two stage amplifier or three stage

amplifier, also how many transistors should be at each stage. There are several cases to analyse before proceeding. In order to see which case to use, it must fulfil the three requirements stated below.

- The output power must be at least 33 dBm.
- The channel temperature cannot exceed 115 °C.
- The overall chip gain must be above 25 dB.

Next step is to analyse different cases where one starts at the output of the last stage and works backwards. Note that in order to obtain >25 dB overall chip gain and an output power >33 dBm, the input power cannot exceed 8 dBm.

It is most wanted to have fewer gain stages because it reduces the complexity of the design and improves the PAE. The reason is related to equation (2.2), the DC power is significantly reduced when fewer gain stages are used.

Below are three different cases presented. In the input and the output at each transistor, there are matching networks who suffers from losses. The assumed value for the loss is 0.5 dB as stated above. The first and the second case are two stage amplifiers while the third case is a three stage amplifier. All three cases are assuming a possible gain value for each transistor without exceeding 115 °C.

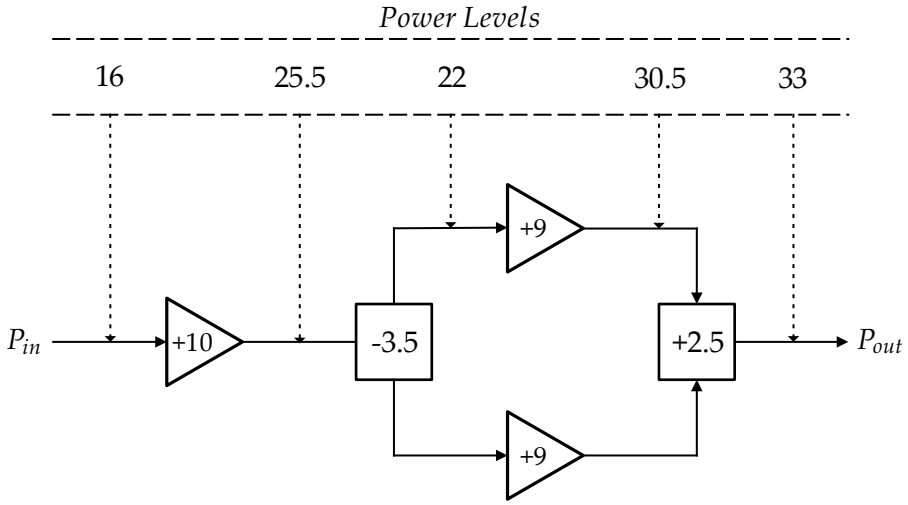

FIGURE 5.1: *The first case is illustrating a two stage amplifier with two transistors at the last stage.*

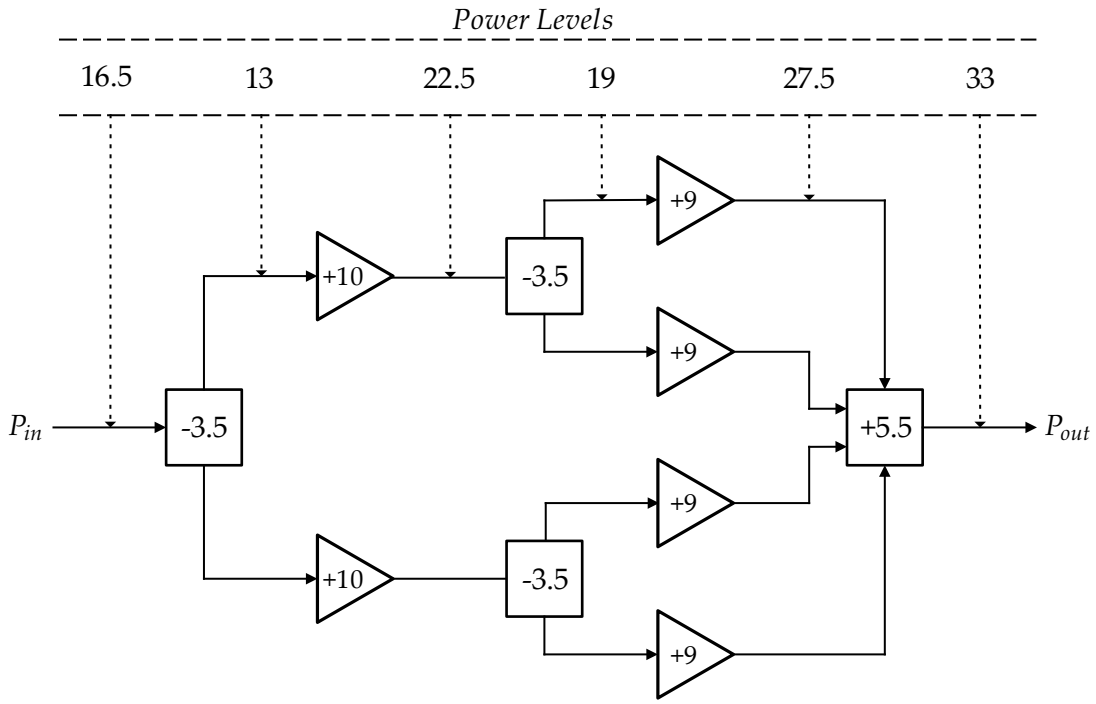

FIGURE 5.2: *The second case is illustrating a two stage amplifier with four transistors at the last stage.*

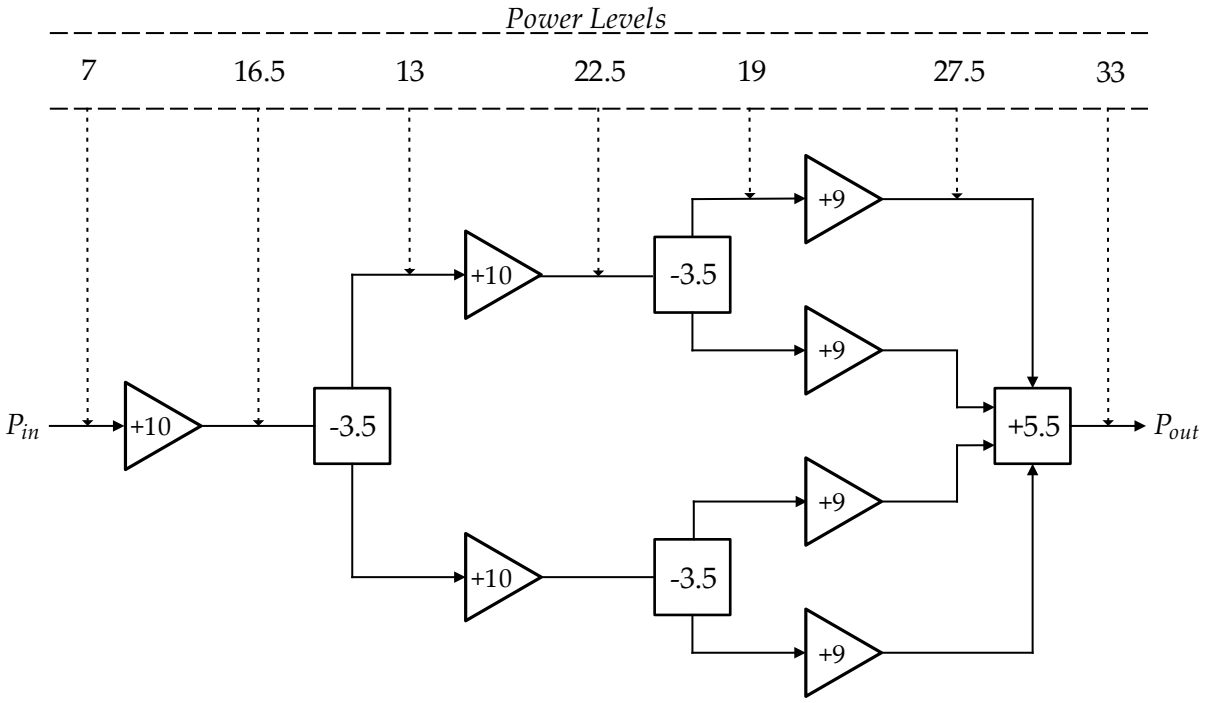

FIGURE 5.3: *The third case is illustrating a three stage amplifier with eight transistors at the last stage.*

In the first case, there is only one power divider and combiner. The divider is having a power reduction of 3.5 dB. The initial 3 dB reduction is because the power is split into half. Same principle

for the combiner but instead the power is combined. In the first stage it has only one transistor while in the last stage it has two transistors. In order to calculate the overall chip gain, one can use the equation (5.1).

$$\text{Gain} = P_{out} - P_{in} \tag{5.1}$$

The overall chip gain for the first case is 17 dB. Therefore this design cannot be used and is rejected.

The second case design is more complex compared to the first case. It has three power dividers and two combiners. The combiner is combining power from four transistors at the last stage, which makes the power level increase by 6 dB. This design is having a overall chip of 16.5 dB which makes this design even worse and is also rejected.

It was realized that it was necessary to design a three stage amplifier in order to obtain the required >25 dB gain. The third case is similar to the second case. The difference is that it has one extra gain stage at the input. Also the amount of transistors are doubled at each stage. This gives a total of 14 transistors. Note that in figure 5.3, the amplifier-sign is having two parallel transistors, a power cell. Power cells will be discussed later in chapter 5.5.4. This design makes the input power drop to 7 dBm which gives an overall chip gain above 25 dB.

All three cases were analysed and the only case that fulfills the three requirements stated above is the third case. Therefore case 3 will be chosen for our design.

5.3 Geometrical design of a transistor

It is important to lay focus on the geometry of the transistor because it affects the output power, gain and the temperature. If one wants to increase the size of the transistor, then the output power will increase. It is because the output power is proportional and a function of the drain voltage, drain current and the efficiency. Instead, if the size of the device decreases then the gain will increase. This is because the gain is inversely proportional to the device size [12].

The maximum number of fingers the chosen transistor can have are 12 with each finger can have a maximum gate width of 125 μm. This gives a total gate width of 1500 μm, see figure 5.4.

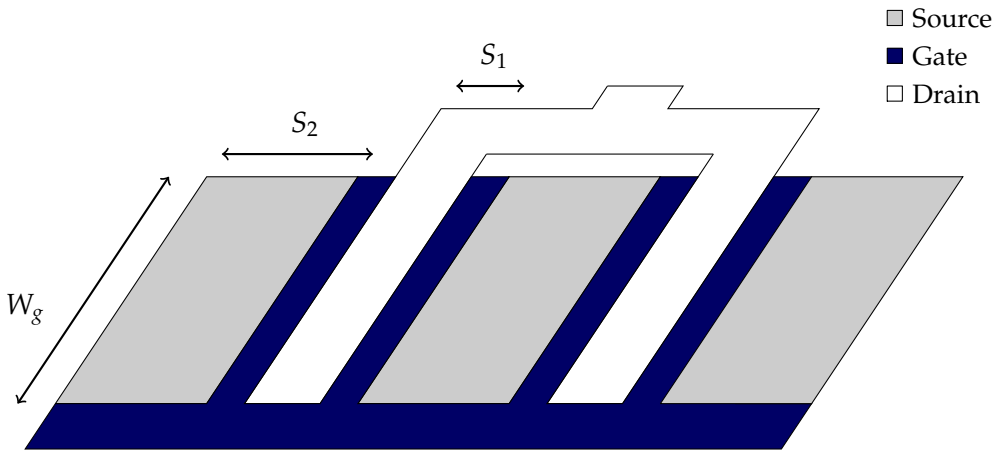

FIGURE 5.4: *The definition of parameters W_g, s_1 and s_2.*

The spacing between the fingers are, $s_1 = 22.5\,\mu$m while between the next couple are, $s_2 = 40\,\mu$m. Recall from chapter 2.4, Darwish presents the spacing as s which is fixed. For this case, our transistor has a fixed spacing s_1 and s_2. Therefore an equivalent spacing is done by taking the mean value of s_1 and s_2 when the temperature is calculated.

From the previous section 5.2, the chosen design is a three stage amplifier. The question arises then why not use only one transistor. Considering the output power, one can simply calculate the maximum power only one transistor can deliver to the output. According to the specifications, PPH25X is having a power density 900 mW/mm and total gate width 1500 μm which gives a maximum output power of 31.3 dBm.

$$P_{out,max} = 10 \cdot \log_{10}(900 \cdot 1.500) = 31.3\text{dBm} \tag{5.2}$$

Only one transistor can not deliver enough of power. The required output power should at least be 33 dBm. Also the design is limited to the temperature. Having only one transistor with maximum fingers and gate width, the temperature would exceed 115 °C.

The chosen geometrical design of the transistors are a gate width of 75 μm with 10 fingers. This gate width reduction is due to the usage of the power cells which will be discussed more in detail in chapter 5.5.4.

5.4 Biaspoint

In order to choose a bias point, a DC and bias point simulation is performed . It is wanted to choose a bias point that gives as high transconductance as possible but also in the region of a class AB amplifier.

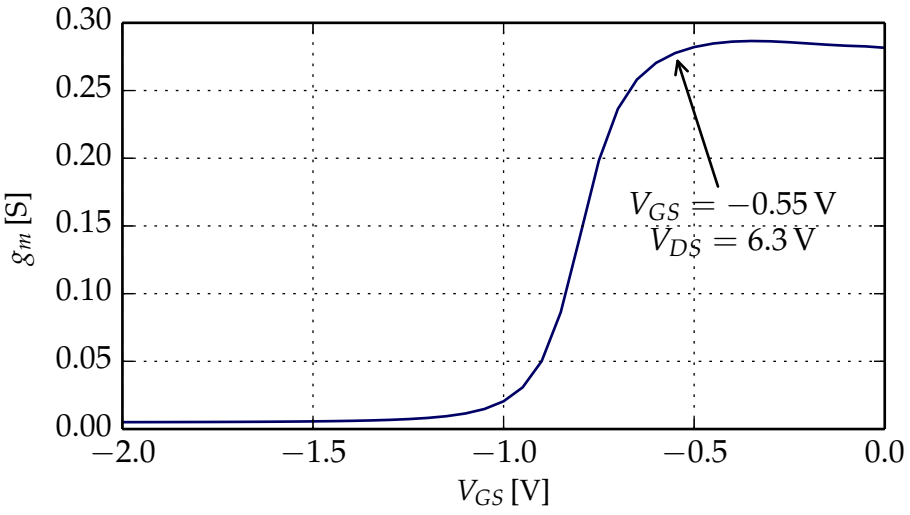

FIGURE 5.5: *The figure shows the transconductance g_m over the gate voltage V_{GS}.*

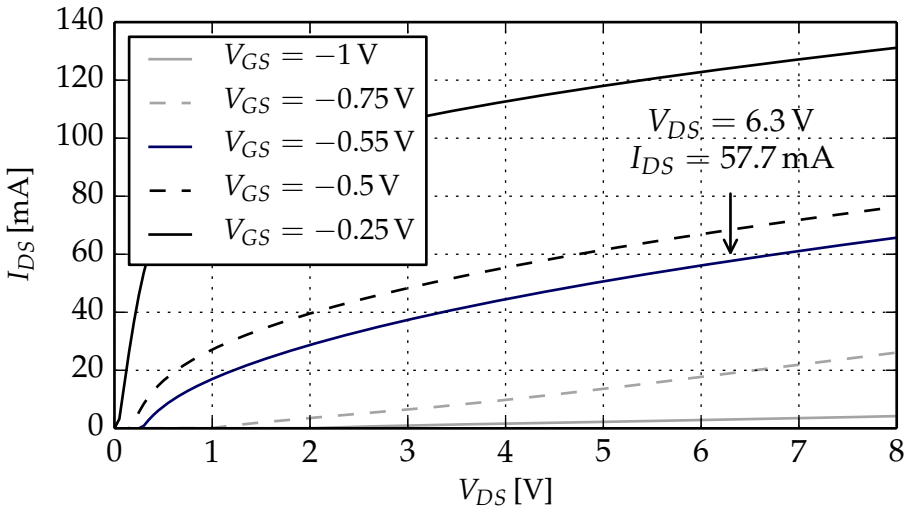

FIGURE 5.6: *The figure shows the drain current I_{DS} over the drain voltage V_{DS}.*

The simulations suggest that the gate voltage should be set to -0.4 V because the transconductance is at its peak at that point. The choice of our class of operation is class AB. Therefore the bias point is set to $I_{DC} < {}^{I_{max}}/_{2}$. As -0.4 V is not in an acceptable region for class AB, the chosen gate bias is close to -0.6 V while the drain voltage V_{DS} is set between 6–7 V. Thus giving us a drain current I_{DS} close to 60 mA. Note that the chosen bias point is in a class AB region.

5.5 Bias and stability networks

In addition to supplying the gate and drain with voltage and setting the bias point, the bias networks introduce robustness to the circuit. Within the frequency band the bias should withstand different loads and impedances introduced by either bond wires or probes that supply the amplifier with power. In the following section, different bias network will be discussed and as well as measures to ensure an unconditionally stable amplifier.

To get an initial idea of what type of topology to use for the bias networks there were a few factors that were taken into account. Firstly, while lumped capacitors are usually considered a good measure to use in MMIC designs but inductors are generally sensitive to large DC-currents [12, 23]. As a result inductors can not be used in parts of the circuit that supplies voltage to the drain of an active device. Another factor that had to be taken into account was the current limitations of air bridges. The air bridges were limited to 150 mA which is more than enough to bias the gates but on the lower end of what is possible to use on the drain of the output stage. Like the power budget in section 5.2 a small sketch was made to minimize the chance of problems arising during the design process, see figure 5.7.

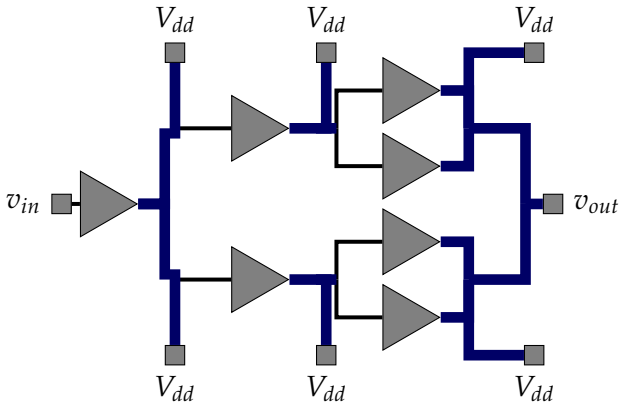

FIGURE 5.7: *A sketch of the drain bias network used in the final design.*

5.5.1 Gate bias network

The gate has generally high impedance with low currents as a result. Lumped components are therefore favourable due to the smaller size compared to stubs at Ku-band frequencies. The network consists of an inductor and a bypass capacitor and is depicted in figure 5.8. The inductor prohibits the fundamental signal from travelling up through the bias network, shortening the gate. Instead the bias network should remain as transparent to the signal path as possible. As an extra precaution a shunt capacitor was placed between the inductor and the bias pad. The tuned capacitor will act as ground for any RF signal, originating from the bias pad.

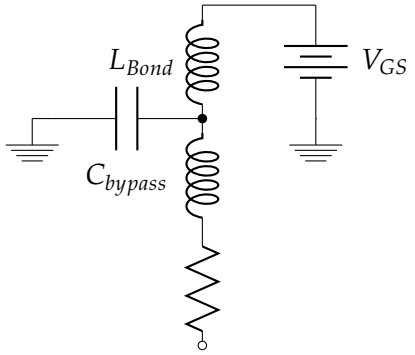

FIGURE 5.8: *The gate bias network with bond wire included.*

5.5.2 Drain bias network

The drain features larger currents than the inductors could withstand [23] so reusing the bias network from the input was not an option. Instead the shunt capacitor was used in combination with a quarter wave transmission line, see figures 5.9 and 5.10. The capacitor was tuned so that the fundamental frequency would see ground, while the quarter wave transmission line turned the load 180° to open circuit. The transmission lines are fairly narrowband so the circuit has two functions. The fundamental passes the bias network unaffected while the overtones gets grounded - one of the fundamental conditions for deep class-AB operation and to achieve a sinusoidal output signal.

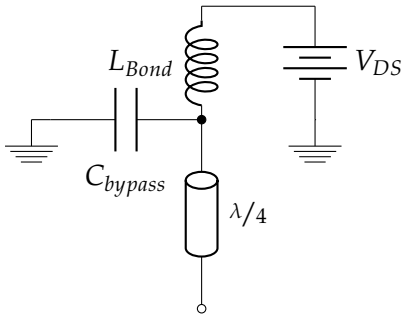

FIGURE 5.9: *The drain bias network with a quarter wave transmission line.*

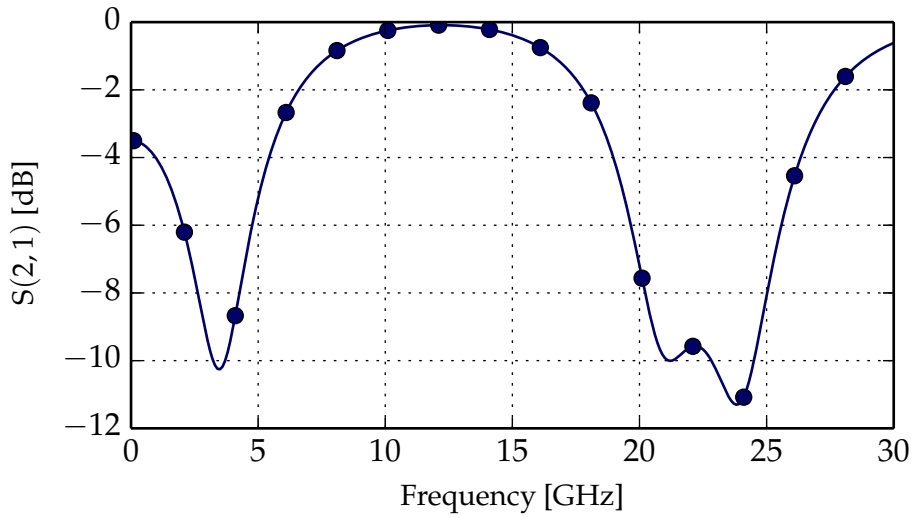

FIGURE 5.10: *The resulting frequency response at the drain with the bias network inserted.*

5.5.3 Stability and feedback

A common problem with active devices is that the optimal load on the input and output may result in instability issues. In the following chapter a few techniques will be mentioned that were used to ensure unconditional stability.

Negative feedback

All the active devices in the circuit feature a network of lumped components that connects the drain to the gate to let parts of the signal back to the input, see figure 5.11. By adjusting the network it is possible to increase or decrease the Negative Feedback (NF).

Stability, gain linearity over frequency and the matching procedure can all be enhanced by applying NF [2]. The downside is that the benefits come at a cost of gain and will thus reduce the theoretical *PAE* as well as an increase in circuit cost and size. That being said, an additional, separate stabilizing circuit and a more complex matching network may impose an even larger area of the wafer.

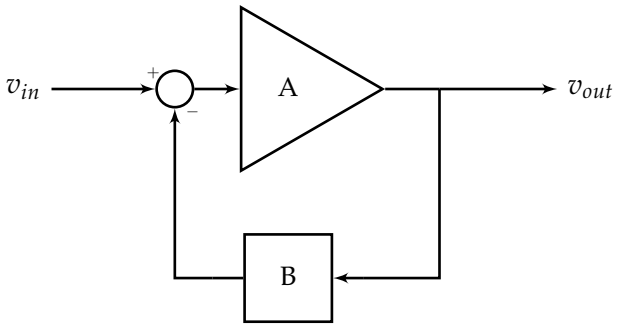

FIGURE 5.11: *A system that utilizes feedback to feed parts of the signal back to the input.*

The NF in the circuit was designed with stability in mind but improvements were noticeable in all areas mentioned in the section above. Each stage of the circuit suffered from stability issues around 7 GHz which appeared as a negative spike in the stability factor. To ensure unconditional

stability, the LRC network in figure 5.12 was applied, where the capacitor is essential to block the DC-component. In combination with the resistor and inductor the capacitor becomes an inverted notch-filter that feeds a small part of the band back to the input and thus dampening it. The resulting transfer function for the feedback network that targets 7 GHz is shown in figure 5.13. The network affects the fundamental band as well but in a way that compensates for the decline in gain at higher frequencies [7] and is otherwise scalable to some extent with the resistor.

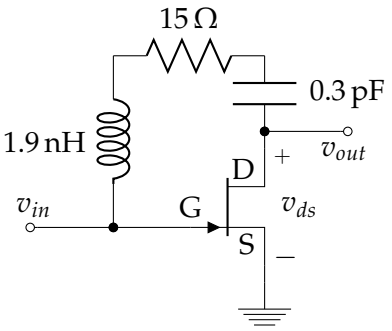

FIGURE 5.12: *The final feedback network with the values used in the output stage.*

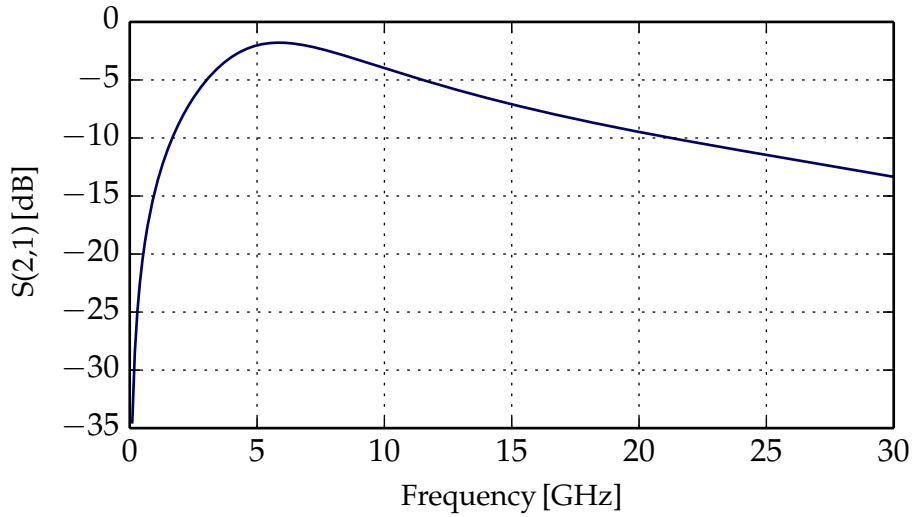

FIGURE 5.13: *The frequency response of the LRC feedback network.*

Gain compensation

Another common practice to improve stability is to introduce a parallel RC filter in front of each gate, depicted in figure 5.14. The circuit is a simple high pass filter will lower the gain at all lower frequencies outside as well as inside the band. In other words, in addition to flatten the gain, the circuit helps to stabilize the unstable 7 GHz region, mentioned in section 5.5.3.

However in the design, the main reason for the added circuitry was to compensate for the decrease in gain at higher frequencies, see figure 5.15. There are no ways of increasing the gain with passive components so instead the circuit flattens the gain in the lower end of the band.

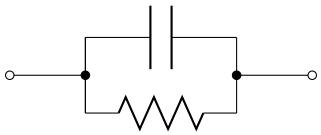

FIGURE 5.14: *The gain compensation network used in all stages.*

The resulting *Rollett* or stability factor K can be viewed in figure 5.16. The plot only depicts frequencies up to 30 GHz but with the decreasing nature of the active devices, the second and third harmonics magnitude will be negligible.

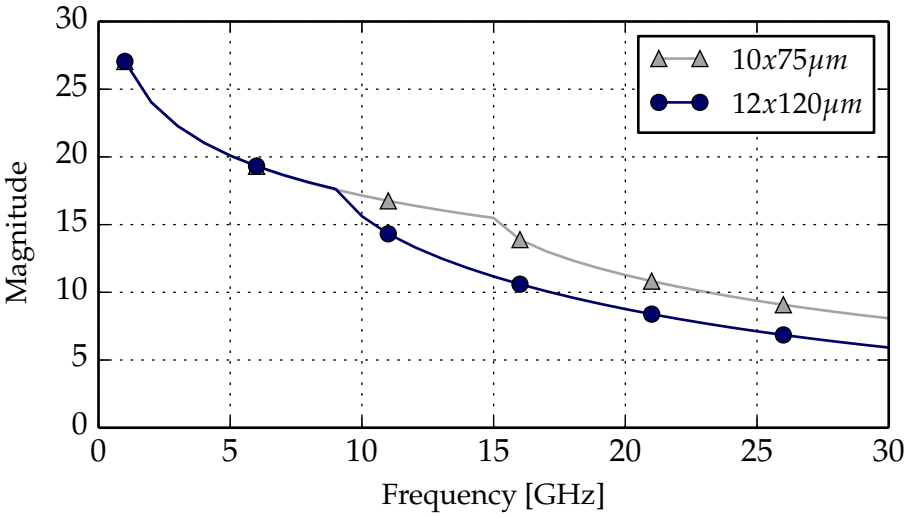

FIGURE 5.15: *The transition frequency f_T of two active devices with ten and twelve fingers.*

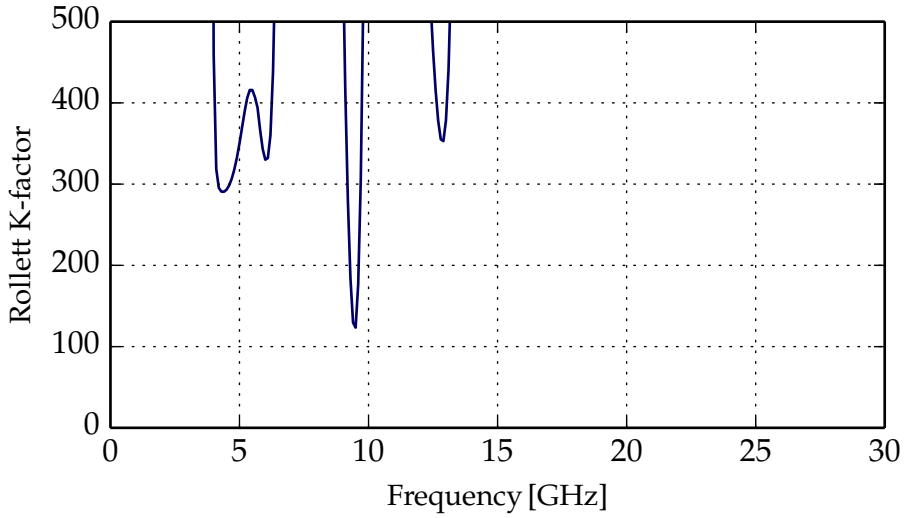

FIGURE 5.16: *The Rollett factor of the designed amplifier.*

The Rollett factor magnitude is well above one as mentioned in subsection 2.2.1 but without the ability to modify the circuit after production it could prove helpful with process variations.

5.5.4 Power cells

In the second stage, it was not possible to efficiently utilize the bias networks mentioned earlier in chapter sections 5.5.1 and 5.5.2, without using air bridges. The output power from two active devices was not enough to feed the output stage and increasing the size of the transistors would have led to lower impedance and gain. Therefore, *power cells* or *parallel devices* were used. The power cells consists of two or more active devices in parallel with interconnected drains and gates. By connecting the devices the impedance is halved, however the increase in output power and gain made it possible to reduce the size further and thus increase the impedance.

To further improve the matching properties, the power cells were with the negative feedback and the gain compensation network mentioned in 5.5.3 respectively 5.5.3. With the final combined circuit viewable in figure 5.17, it was possible to achieve the wanted output power while having a flat gain and stable operation.

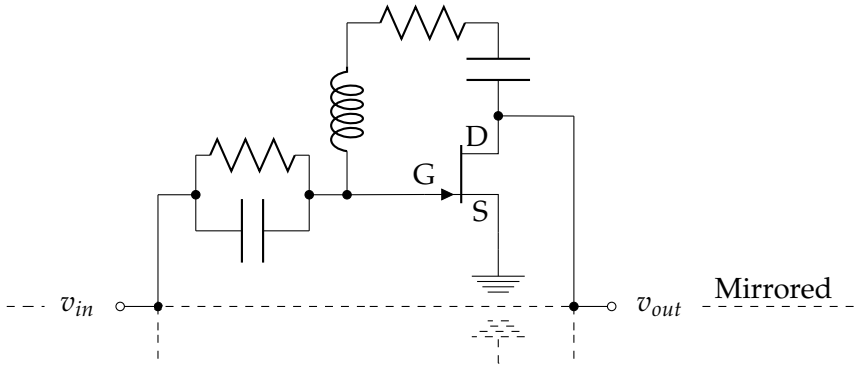

FIGURE 5.17: *Half of the final power cell network.*

5.6 Matching networks

Matching networks are often used to maximize the performance of active devices. Similar to power matching at DC, a specific load gives maximum power transfer and a minimal reflected signal. In the following chapter, different topologies for matching networks will be revised and presented.

5.6.1 Bus-bar power combiner

The output stage of the design uses 14 active devices to achieve the specified output power at a low working temperature. The outputs were connected with a bus-bar i.e. a microstrip that connects the drain of the transistors with equal spacing. This makes it possible to bias the circuit from either the top of the circuit or the bottom depending on what is most beneficial. Due to equal spacing, the phase delay will be equal for all branches.

Once the optimal load was determined, multiple matching networks were reviewed. By using super-position and S-parameter optimization it was possible to adapt the bus-bar so that it matched the optimal load, $Z_L \approx 14.6 + j25.7\,\Omega$. However, since the matching networks can never result in a perfect match it could only be used as an initial approximation. This is especially true to active devices that are bilateral since a poor matching on either sides of the device, affects the other. An optimization was therefore performed to find a local minimum with both the bus-bar and the input matching network in place.

The final bus-bar which achieved the best match with the lowest loss can be viewed in figure 5.19. Like the bias networks reviewed in section 5.5.2, the bus-bar employs a quarter wave transmission

line and a by-pass capacitor to reduce amplitude of the harmonics. There is also an output capacitor to remove any DC-component from the signal which in turn could change the bias or damage any following circuitry.

With an attenuation of less than 0.6 dB throughout the band, the bus-bar achieved a return loss of 15.4 dB or better and the results are depicted in figure 5.18.

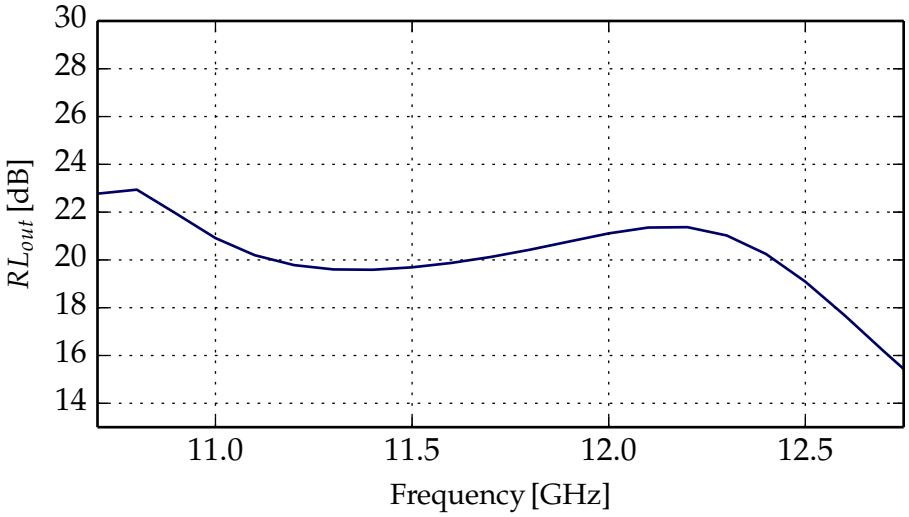

FIGURE 5.18: *The return loss of the output stage and bus-bar.*

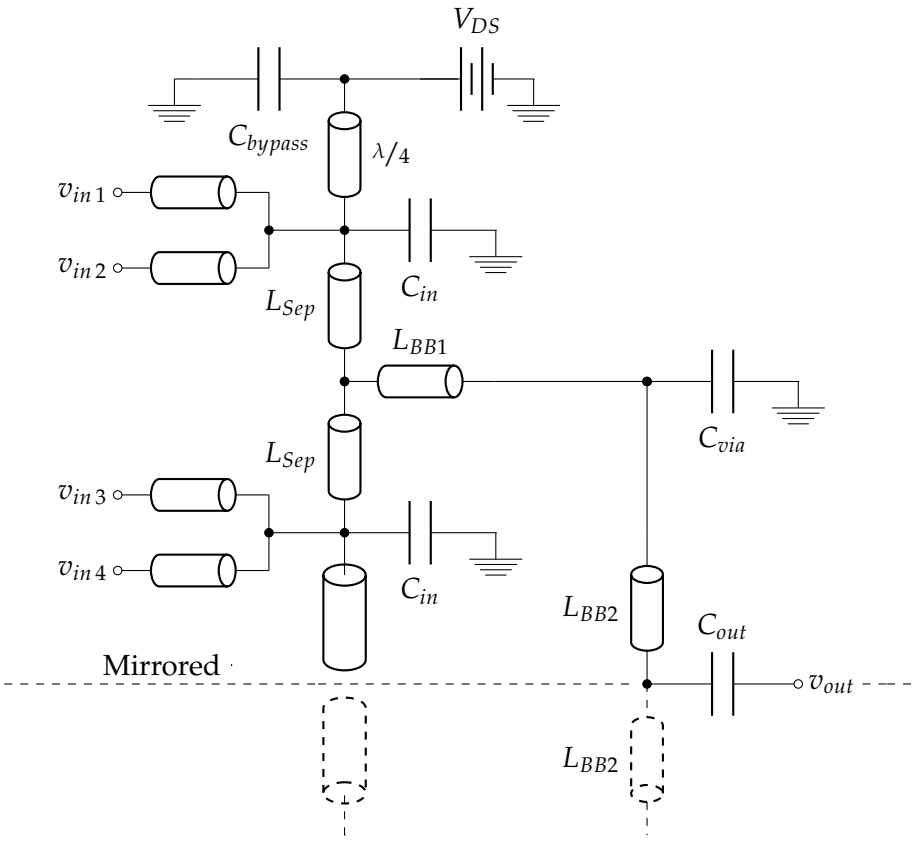

FIGURE 5.19: *A basic schematic of the bus-bar where the C_{via} and attached ground, represents a MIM over via capacitor*

5.6.2 Power splitters, input matching and noise performance

There are multiple power splitters available, all with different traits and qualities which makes them favourable in different situations and applications. Three of the more common ones are Lange, Rat-race and Wilkinson power splitters where the two latter use quarter-wave transmission lines [21].

Quarter-wave transmission lines are necessary and are used in some parts of the design, in particular the drain bias. However with the chosen process PPH25X and at 10 GHz, a quarter wave corresponds to a microstrip with the length of 2.1 mm. Despite being folded the microstrips would have resulted in an substantial increase in the size of the design. The Lange coupler on the other hand uses air bridges which for this process are limited to currents up to 150 mA. While being implementable, the Lange coupler is mostly utilized in wideband applications [14] and would still require additional passive components.

A procedure similar to the one used in chapter 5.6.1 for the bus-bar, was therefore used to find a suitable power splitter. Numerous matching networks were reviewed where the one with the lowest attenuation and matching properties selected and modified into a power splitter. The resulting power splitter can be seen in figure 5.20 and was used in the second and third stage. To allow for biasing from only one of the sides of the amplifier, a resistor was connected between the two power splitters marked as R_{PS}. As with the bus-bar, there were no phase compensation done to the power splitter so it relies on equal length and propagation delay.

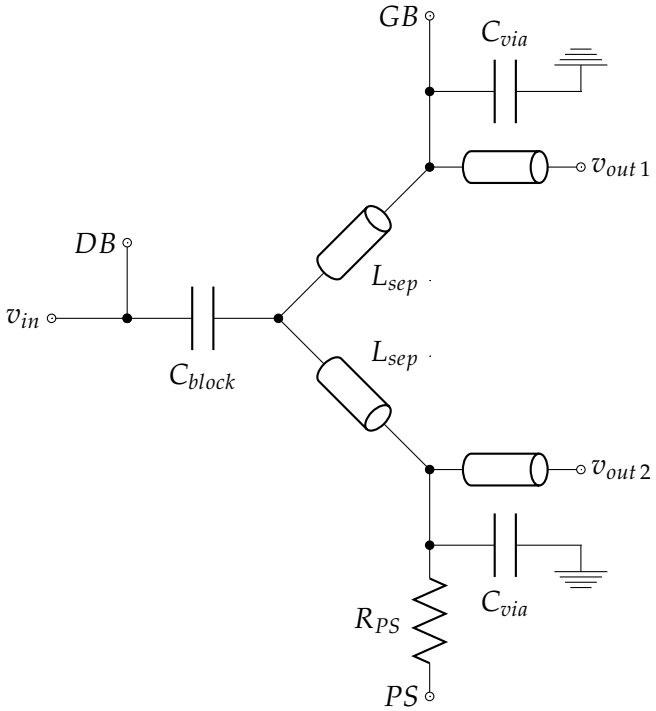

FIGURE 5.20: *A basic schematic of the power splitter where DB respectively GB are the drain and gate bias circuits. The variables PS and C_{via} represent the second power splitter and a MIM over via capacitor.*

Unlike the second and third stage, the first stage uses a normal matching network but with a similar selection of components. The power splitter was removed and a folded transmission line was used in its place. The transmission line imposes larger area than that of a corresponding inductor but resulted in a lower attenuation and a better match. The matching network is shown in figure 5.21 and the resulting return loss in figure 5.22. Recalling section 2.3 the lower attenuation in the input matching network also helps to improve the noise figure of the system which can be calculated by reviewing the S-parameters. The noise figure was calculated to a maximum of 5.6 dB and as low as 4.8 dB in the center of the band, see figure 5.23.

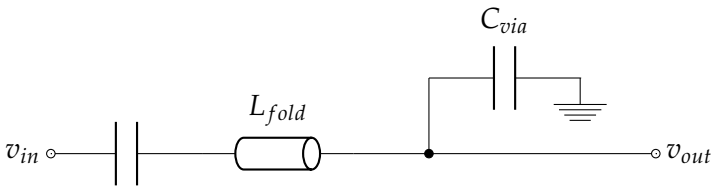

FIGURE 5.21: *The input matching network with a folded transmission line* L_{fold}.

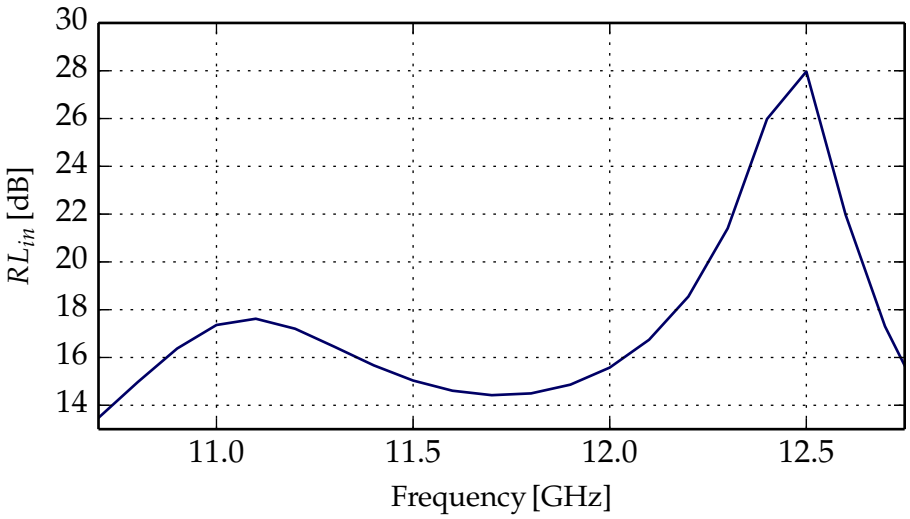

FIGURE 5.22: *The return loss of the input stage with the lowest return loss of 13.5 dB at 10.7 GHz.*

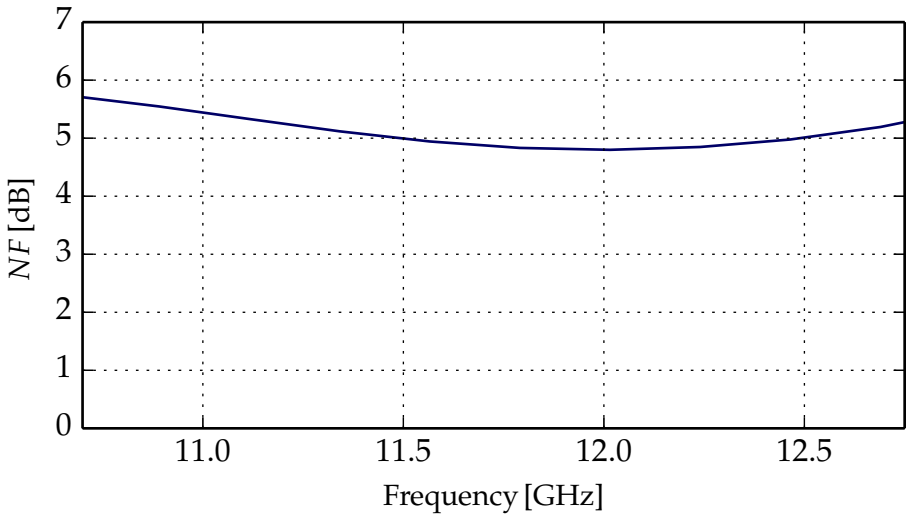

FIGURE 5.23: *The noise figure of the amplifier.*

5.7 Layout routing and size

The production costs of a MMIC circuit is the proportional to the area of which the circuit impose on the wafer. The design choices must therefore be taken with great care and with both layout size and routing in mind. In this section, size and common layout problems will be reviewed along with the tools to prevent them.

When designing an amplifier there are always compromises that have to be made and it is therefore not uncommon for amplifiers to be tailored for specific purposes. The designed amplifier is no exception where the temperature restrictions resulted indirectly in an increase in layout size. The final amplifier design has a footprint of $4594 \times 5054\,\mu m$ and can be viewed in figure 5.25. The large circuit size is a result of the high amount of active devices in the output stage in combination with the negative feedback networks, both which were a necessity to achieve the specified output power. Additionally, the quarter-wave bias networks and the spacing required to reduce coupling, or even merging of microstrips due to process variations, increases the size even further [12].

To ensure that the fabricated circuit will perform as intended there are a few different tools that could be employed. The PPH25X includes parameters for the Design Rule Checking, DRC, tool that is available in ADS. The tool investigates whether the microstrips and components are adequately separated and was applied to the designed amplifier [12]. DRC should preferably be used in combination with Monte Carlo simulations which varies parameters of choice to see how the design responds to e.g. process variations [22]. Note that even though the designed amplifier did not feature any, there are circuits such as the band-pass filter in figure 5.24 that takes advantage of coupling [1].

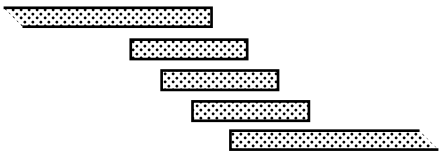

FIGURE 5.24: *A microstrip band-pass filter, utilizing coupling to attenuate the signal outside the frequency band.*

To review the coupling, electromagnetic, EM tools are used such as Momentum simulations in ADS. Based on Method of Moments, MoM, the tool divides the circuit in a fine mesh and solves the EM properties for each segment [9]. Neither the Monte Carlo nor the Momentum simulations were performed on the complete circuit since they were considered to be outside the scope of this thesis, however should the design be produced, it would be an advisable complement to the DRC.

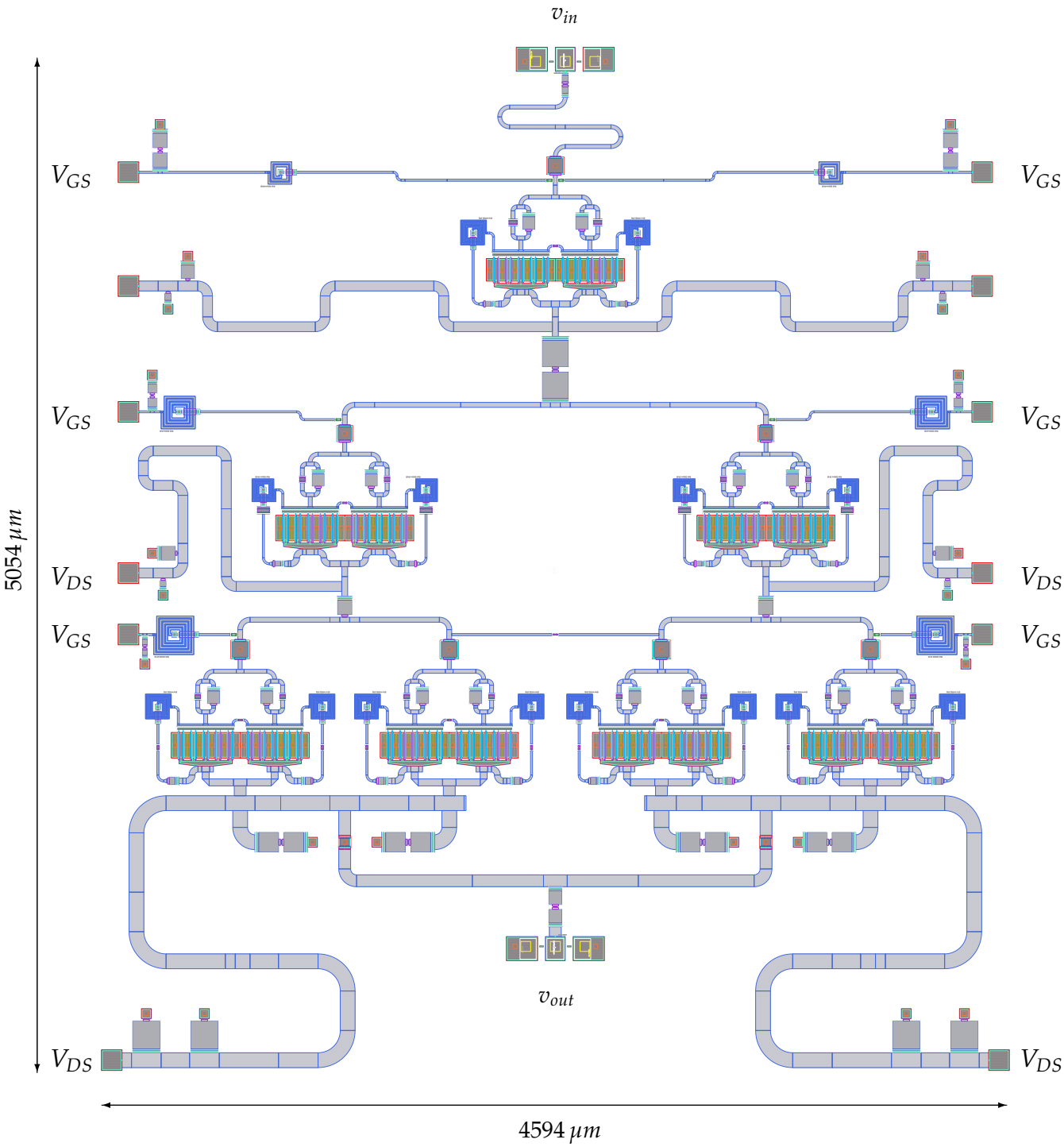

FIGURE 5.25: *An overview of the designed amplifier where V_{DS} and V_{GS} represents the drain and gate supply pads respectively.*

5.8 Temperature and Power

As two of the main pillars of the thesis, power and temperature influenced the entire design procedure. In the following chapter, the power consumption and output power will be reviewed as well as the temperature generated by the circuit.

5.8.1 Temperature and efficiency

The output stage is the most power consuming part of the amplifier and was therefore used as a starting point for the design. The output consists of eight pHEMTs to divide the generated heat. In turn, it allows for lower bias settings and smaller devices but the lower bias also reduces the voltage swing that has to be made up for with higher currents. Inductors are therefore not used in the output matching network of the third stage.

Using smaller active devices is a compelling alternative since they have a higher gain and impedance compared to that of the larger counterpart. It is also beneficial when using the power cells mentioned in section 5.5.4, since the increase in impedance eases the matching phase.

The total power consumption of the amplifier at 1 dB-compression can be viewed in figure 5.26 and the power consumed by one of the output devices in figure 5.27. Both plots have similar features as the output stage is the largest contributor to the power consumption and therefore also generates the highest temperatures despite the large number of active devices. To ensure that the temperatures did not exceed the maximum rating of 115 °C the temperature equations from section 2.4 was used and the result is depicted in figure 5.28. The maximum dissipated power in the output devices is approximately 442 mW which corresponds to a temperature of 95 °C, well below the specified temperature limit.

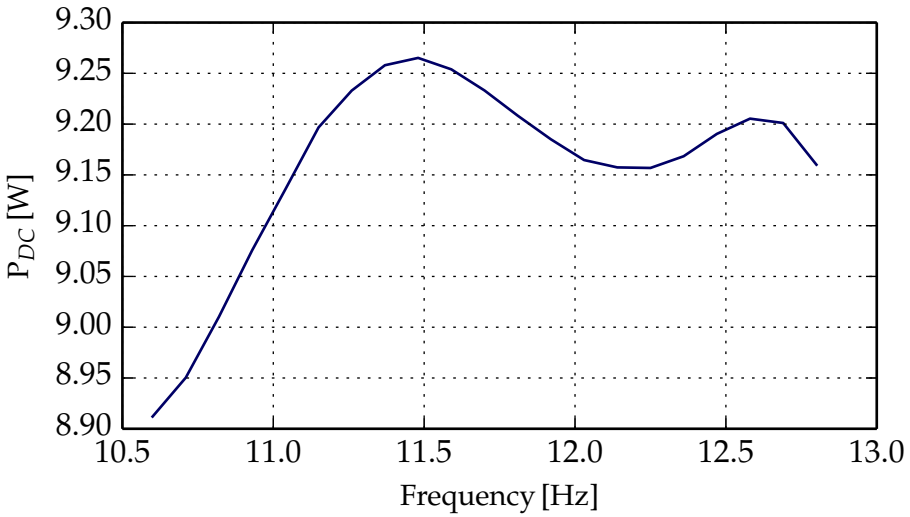

FIGURE 5.26: *The power consumption of the amplifier within the bandwidth and at* $P_{1\,dB}$.

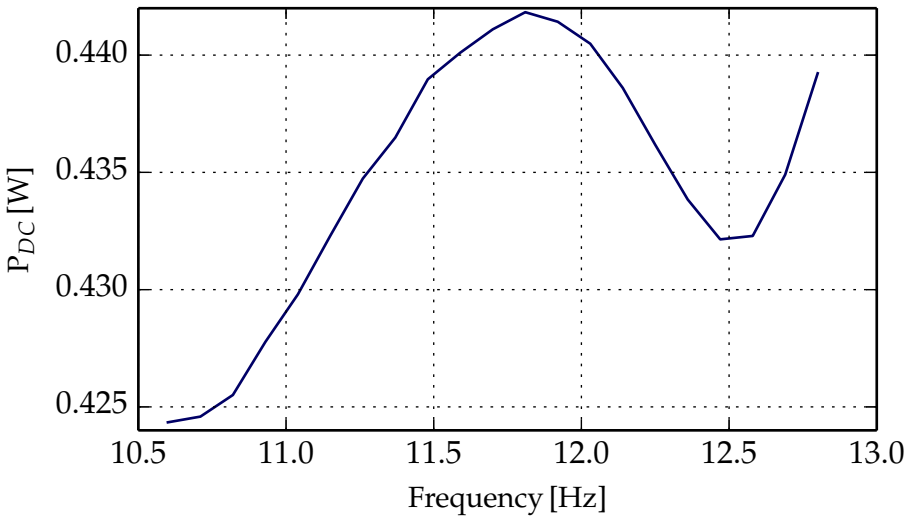

FIGURE 5.27: *The power converted into heat at $P_{1\,dB}$ in one of the active devices located at the output.*

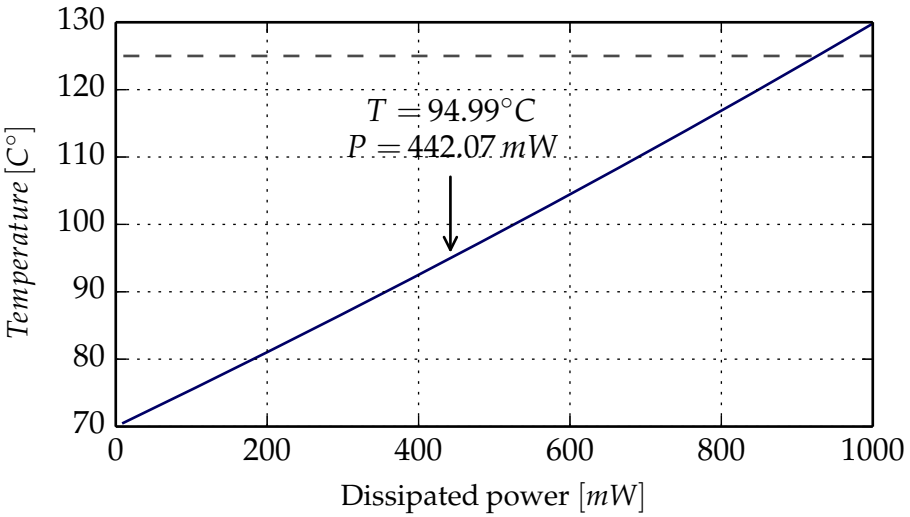

FIGURE 5.28: *The highest simulated temperature of one of the pHEMTs in the output stage, within the bandwidth and at $P_{1\,dB}$ (P_{in}=8 dB).*

5.8.2 Gain and output power

The resulting output power and gain of the complete amplifier is shown in figure 5.29. The $P_{1\,\mathrm{dB}}$ occurs at an input signal of 8 dB and the output power as function of frequency is shown in figure 5.30. To verify that the variation in gain was not higher than the specified in chapter 1.3 a moving average was applied to the data and the result is plotted in figure 5.31. As can be seen in the figure, the highest variation in gain was $^{0.45\,\mathrm{dB}}/_{500\,\mathrm{MHz}}$ and below the specified $^{0.5\,\mathrm{dB}}/_{500\,\mathrm{MHz}}$.

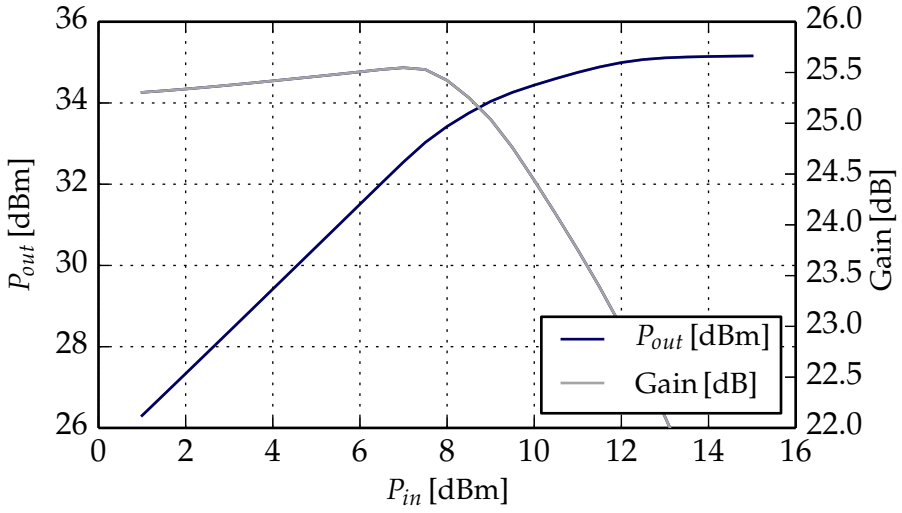

FIGURE 5.29: *Output power P_{del} and Gain as a function of input power P_{in} at the center of the band, f=11.725 GHz.*

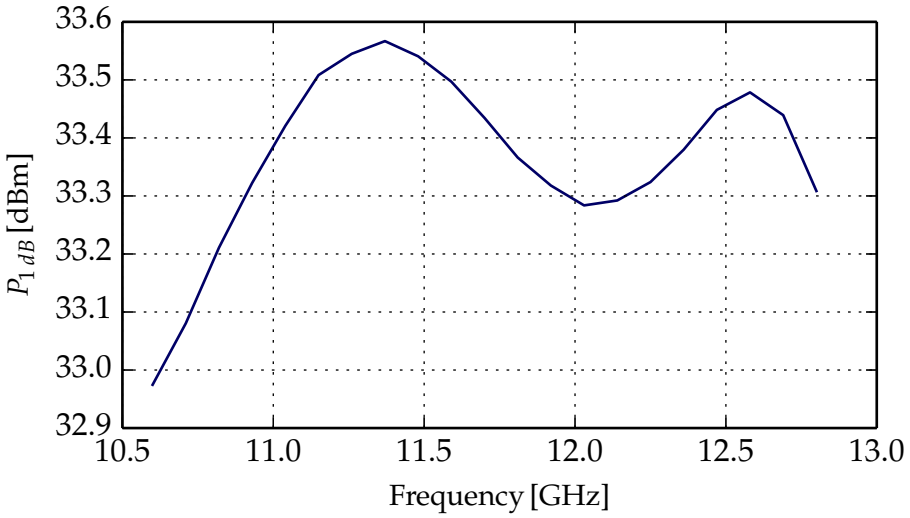

FIGURE 5.30: *Output power $P_{1\,dB}$ and Gain as a function of input power P_{in} at the center of the band, f=11.725 GHz.*

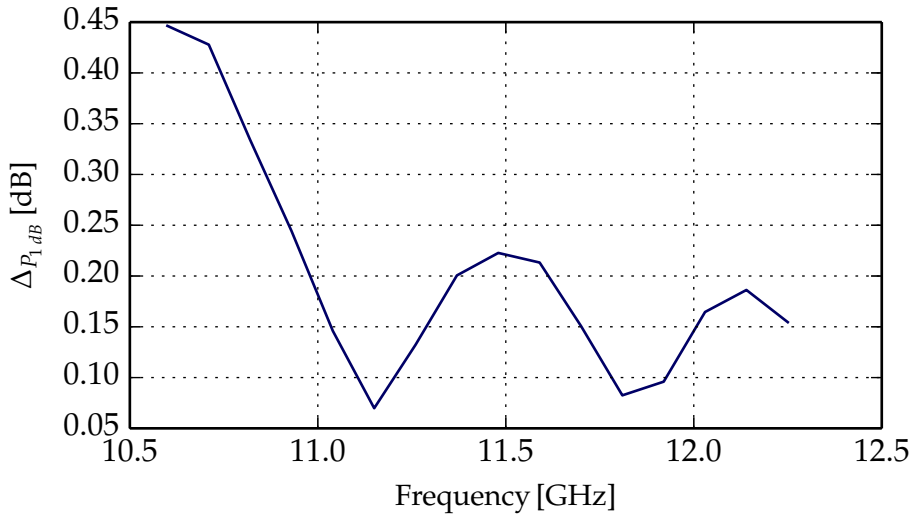

FIGURE 5.31: *Gain variations per 500 MHz, extracted from the data in figure 5.30 with a moving average.*

The efficiency of the final complete amplifier was calculated with the output power and the consumption available from section 5.8.1 where result is depicted in figures 5.26 and 5.33 as function of input power and frequency respectively. As shown in the figures, the amplifier achieves an efficiency of approximately 23.5 % at 1 dB-compression, occurring at a $P_{in} = 8$ dB. At 3 dB-compression ($P_{in} = 12.4$ dB) the PAE reaches 31 %.

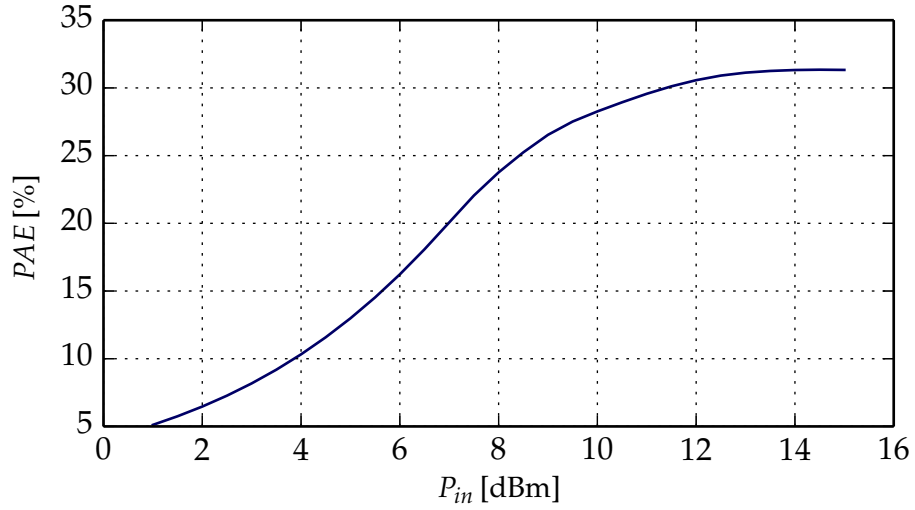

FIGURE 5.32: *The efficiency as a function of input power at 11.7 GHz.*

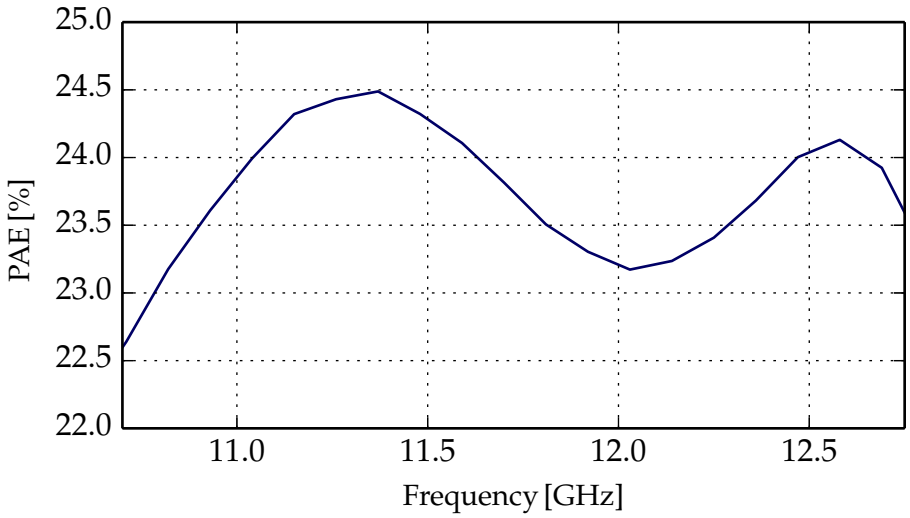

FIGURE 5.33: *The variations in PAE within the Ku-band at 1 dB-compression and* $P_{in} = 8\,\mathrm{dB}$.

6 Conclusion and future work

A MMIC 2 W TT&C amplifier operating at the Ku-band has been modelled and presented. Based on the PPH25X process from UMS, the model utilized 14 active devices to achieve the specifications in table 6.1. As a part of the study a commercial amplifier, Hittite HMC1053 have been investigated for the comparison of the two. Covering both small and large signal parameters, the measurements were made with a VNA from Rohde & Schwartz and aimed at giving a comprehensive coverage. The bias settings of the amplifier were therefore varied throughout the process and the results can be viewed in table 6.2.

Comparing the two different designs it is apparent that there were complications during the measurements of the higher bias settings. The output power decreases at a higher drain voltage despite the increase in voltage swing. Similar behaviour has been spotted in earlier work as a result of high temperature [3, 19]. Reviewing the power consumption and the lack of means to cool the during the measurements, temperature problems not only seems probable - but a likely cause. The chuck on which the amplifier was mounted on, see figure 6.1, is made out of solid steel and got increasingly hot whilst the measurements were being performed. In turn, this meant that the surrounding temperature got warmer than anticipated. Since the increase in temperature of the backplate or chuck was not recorded, it was left out in the analysis in section 4.4. It is therefore hard to draw conclusions from the measured data and further measurements is advisable.

Apart from the input return loss and the power consumption at 1–dB compression the properties of the designed amplifier were consistent with the specifications. Overall, the simulated amplifier surpassed the requested criteria with temperatures well below the requested 115 °C. The lower operating temperature will increase life expectancy of the amplifier [6] but at a cost of size. The large amount of active devices takes up a larger area and for future work it would be advisable to review the topology. A second bus-bar connecting the drains of the second stage would make it possible to bias only one of the sides of the amplifier while achieving the wanted class of operation. It would also remove the need of using power cells which halves the impedance of the active devices. Another approach would be to reduce the number- and increase the size of the output devices instead. In conjunction with negative feedback and careful matching it could potentially reduce the amplifier size notably.

Table 6.1: The desired and achieved specifications of the complete design, biased at $V_{DS} = 6.3\,\text{V}$ and with an I_{DS} of 1300 mA ($V_{gs} = -0.55\,\text{V}$).

Attribute	Desired	Achieved
Linear gain	$> 25\,\text{dB}$	$> 25.4\,\text{dB}$
Frequency band	$10.7 - 12.75\,\text{GHz}$	$10.7 - 12.75\,\text{GHz}$
Gain flatness	$<0.5\,\text{dB}/500\,\text{MHz}$	$<0.45\,\text{dB}/500\,\text{MHz}$
$P_{1\,\text{dB}}$	$> 33\,\text{dBm}$	$33.27 \pm 0.30\,\text{dBm}$
Noise figure	$< 7\,\text{dB}$	$5.2 \pm 0.4\,\text{dB}$
Input return loss	$> 15\,\text{dB}$	$20.85 \pm 7.15\,\text{dB}$
Output return loss	$> 15\,\text{dB}$	$19.2 \pm 3.8\,\text{dB}$
$P_{DC,\,Small-Signal}$	–	8300 mW
$P_{DC,1\,\text{dB}}$	$< 9000\,\text{mW}$	$< 9250\,\text{mW}$
$T_{channel,junction}$	$<115\,^\circ\text{C}$	$<95\,^\circ\text{C}$

Table 6.2: Measurements of HMC1053 by Hittite at different bias settings (10.7–12.75 GHz).

5 V	1400 mA	1600 mA	2000 mA
Gain [dB]	> 29.9	> 30.3	> 29.8
$\Delta P_{1\,dB}$ [dB/500 MHz]	< 0.5	< 0.57	< 0.61
$P_{1\,dB}$ [dB]	> 27.3	> 29.1	> 32.9
$P_{DC,\,Small-Signal}$ [mW]	7000	8000	10000
RL_{in} [dB]	> 17.5	> 17.7	> 17.8
RL_{out} [dB]	> 13.3	> 13.4	> 13.4
6 V	**1400 mA**	**1600 mA**	**2000 mA**
Gain [dB]	> 29.4	> 29.1	> 28.5
$\Delta P_{1\,dB}$ [dB/500 MHz]	< 0.36	< 0.48	< 0.45
$P_{1\,dB}$ [dB]	> 23.7	> 24.5	–
$P_{DC,\,Small-Signal}$ [mW]	8400	9600	12000
RL_{in} [dB]	> 17	> 16.4	> 13.4
RL_{out} [dB]	> 17.6	> 17.5	> 17.6

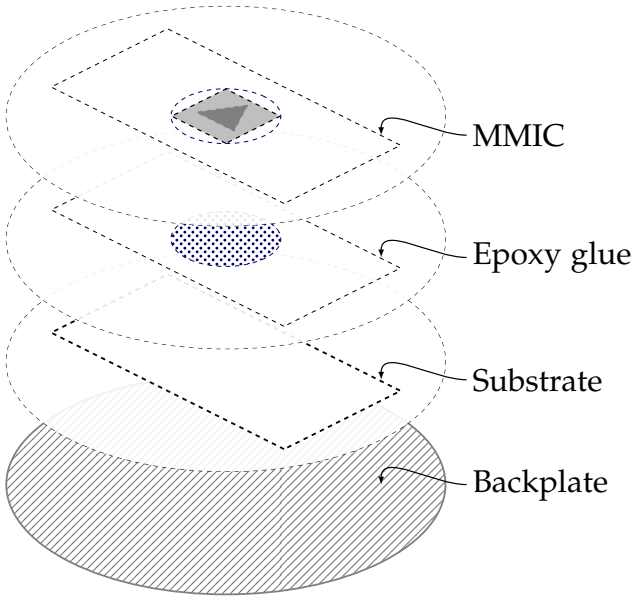

Figure 6.1: *The different layers of the MMIC setup as it was mounted on top of the backplate of the probe station.*

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A Appendix

A.1 Listings

```
"""
Function: Gain fluctuations
Author: Lars Backefeldt
"""

from pylab import *

def gainFluc(ntwk, f1, f2):
    #ntwk is an imported touchstone file with skrf.
    #Finding indexes for desired frequency range
    idx1 = np.argmin(abs(ntwk.f - f1))
    idx2 = np.argmin(abs(ntwk.f - f2))
    #Extracting S21 from the Network
    s21=ntwk.s[idx1:idx2,1,0]
    #Stepsize
    dfreq=(ntwk.f[2]-ntwk.f[1])
    #Number of steps in a 500MHz range
    step=round(500*1e6/dfreq)
    #Dummy array filled with zeros. The step is just so that the interval doesnt
        exceed the boundry
    dummy=zeros((idx2-idx1-step))
    for i in arange(len(dummy)):
        dummy2=zeros(step)
        for j in arange(step):       #Scanning within the 500MHz
            dummy2[j]=20*log10(abs(s21[i+j])) #Converting magnitude to dB
        dummy[i]=max(dummy2)-min(dummy2) #Max diff in range
    return dummy;
```

```
"""
Function: Compression point
Author: Lars Backefeldt
"""
from pylab import *

def gainComp(powerSweep,linpoint):
    #Powersweep is an array with Gain, Pin and Pout

    #Find the index of Minus 20dBm
    #The gain dips for some of the plots before Pin=-20dbm
    idxM20 = argmin(abs(powerSweep[1]+20))
    #Find the index of linpoint (~-10dBm)
    idxM10 = argmin(abs(powerSweep[1]-linpoint))
    #Find the index where the gain has gone down 1dB
    idxM1 = argmin(abs(powerSweep[0,idxM20:(len(powerSweep[0])-1)]-(powerSweep[0,
        idxM10]-1)))
    #
    compPoint=powerSweep[2,(idxM1+idxM20)]
    #compPoint=powerSweep[2,idxM1]-powerSweep[2,idxM10]
    return compPoint;
```