

THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

# Symmetrical FET Modeling

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Göteborg, Sweden, 2014

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# Abstract

This thesis deals with empirical modeling of symmetrical Field-Effect Transistors (FETs). It covers three distinct topics within the areas of modeling and parameter extraction of microwave FETs.

First, the symmetry of FET devices is addressed. Such devices are often used in transceivers as a building block for switches. These devices are intrinsically symmetrical around the gate. Hence, their source and drain terminals are interchangeable. For these devices, the extraction of small signal model parameters is addressed. It is shown that the commonly used small-signal FET model does not translate the intrinsic symmetry of the device into its equivalent circuit. Thus, a big opportunity of reducing the number of measurement points and the complexity of modeling is overlooked. Therefore, a new small-signal model is proposed to address the intrinsic symmetry present in such devices.

Second, the small-signal parameters of the symmetrical model are further improved using a modified optimizer based extraction and a new error expression. This new error function improves the extraction result, and ensures that the symmetry of the device is taken into the account.

Finally, the symmetrical small-signal model is extended to find the symmetry in a large-signal model. This leads to the reduction of the intrinsic model so that one current and one charge expression is sufficient to represent its nonlinear behavior.

While the modeling procedure is inspired from switch FETs, commonly available devices are symmetrical except for high power transistors. Hence, the modeling procedure which is not limited to switch FETs, can be applied across various device technologies e.g., MOSFET, GaAs pHEMTs/mHEMTs, InP transistors, etc. The applications are also not limited to switches, but include resistive mixers, switch mode oscillators etc.

**Keywords:** FET, GaAs, GaN, nonlinear model, small-signal model, switch model, symmetrical model.



# List of Publications

## Appended Publications

This thesis is based on work contained in the following papers:

- [A] A. Prasad, C. Fager, M. Thorsell, C. M. Andersson, and K. Yhland  
"Symmetrical Large-Signal Modeling of Microwave Switch FETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 8, pp. 1590–1598, 2014.
- [B] A. Prasad, C. Fager, M. Thorsell, C. M. Andersson, and K. Yhland  
"Symmetrical Modeling of GaN HEMTs," accepted for publication in *IEEE Compound Semiconductor IC Symposium*, 2014



# Notations and abbreviations

## Notations

$C_{ds}$	Intrinsic drain-source capacitance
$C_{gd}$	Intrinsic gate-drain capacitance
$C_{gs}$	Intrinsic gate-source capacitance
$C_m$	Intrinsic transcapacitance dependent on gate-source voltage for constant drain-source voltage
$C_m^+$	Intrinsic transcapacitance dependent on gate-source voltage for constant gate-drain voltage
$C_m^-$	Intrinsic transcapacitance dependent on gate-drain voltage for constant gate-source voltage
$g_m$	Intrinsic transconductance dependent on gate-source voltage for constant drain-source voltage
$g_m^+$	Intrinsic transconductance dependent on gate-source voltage for constant gate-drain voltage
$g_m^-$	Intrinsic transconductance dependent on gate-drain voltage for constant gate-source voltage
$I_{ds}$	Drain-source current
$P_{in}$	Incident power
$P_{refl}$	Reflected power
$Q_d$	Drain charge expression
$Q_d^{sym}$	Symmetrical drain charge expression
$Q_g$	Gate charge expression
$Q_s^{sym}$	Symmetrical source charge expression
$V_{ds}$	Intrinsic drain-source voltage
$V_{dse}$	Extrinsic drain-source voltage
$V_{gd}$	Intrinsic gate-drain voltage
$V_{gde}$	Extrinsic gate-drain voltage
$V_{gs}$	Intrinsic gate-source voltage
$V_{gse}$	Extrinsic gate-source voltage
$Y_{int}$	Intrinsic admittance matrix for small signal model
$Y_{int}^{sym}$	Intrinsic admittance matrix for symmetrical small-signal model

$\tau$	Current source delay
$\epsilon$	Modeling error
$\epsilon^-$	Modeling error contribution in negative $V_{ds}$ region
$\epsilon^+$	Modeling error contribution in positive $V_{ds}$ region

## Abbreviations

ACPR	Adjacent Channel Power Ratio
CAD	Computer Aided Design
DC	Direct Current
DUT	Device Under Test
FET	Field Effect Transistor
FP	Field Plate
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GPS	Global Positioning System
GSM	Global System for Mobile communications (originally Groupe Spécial Mobile)
HEMT	High Electron Mobility Transistor
LDMOS	Laterally Diffused Metal Oxide Semiconductor
mHEMT	Metamorphic High Electron Mobility Transistor
NL	Nonlinear
pHEMT	Pseudomorphic High Electron Mobility Transistor
RADAR	RADio Detection And Ranging
RF	Radio Frequency
VCCS	Voltage Controlled Current Source



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# Chapter 1

## Introduction

The history of wireless communication starts with the work of Michael Faraday, James Clerk Maxwell, Oliver Lodge, Heinrich Hertz, Jagadish Chandra Bose, the 1909 Nobel Prize winner physicists Guglielmo Marconi and Karl Ferdinand Braun. Michael Faraday's work with the electric current carrying conductor and its local magnetic field inspired Maxwell who mathematically predicted the existence of electromagnetic waves of diverse wavelengths in 1865 [1]. Later, Oliver Lodge and Heinrich Hertz confirmed the existence of electromagnetic waves in free space. Lodge's work caught the attention of scientists in different countries including J. C. Bose in India who in 1894 gave the first public demonstration of wireless transmission using electromagnetic waves to ring a bell and to explode a small charge of gunpowder from a distance [2]. The wavelengths Bose used for his microwave experiments ranged from 2.5 cm to 5 mm (12 GHz to 60 GHz) [3]. Apart from Bose, the results from Hertz also inspired Marconi, who made his first successful radio transmission experiments in 1895. He managed to send the information over a distance of 3 km. By 1901, the first transatlantic transmission was carried out between Poldhu in Cornwall and St. John's in Newfoundland at a distance of 3200 km. It was Bose's diode detector which received Marconi's first transatlantic wireless signal [3], where the frequency of the wave used for the demonstration was 167 kHz [4].

Today, the microwave frequency bands are densely populated with various applications like RADAR, satellite cellular telephone, GSM mobile, GPS, third and fourth generation cellular services, Bluetooth, etc. There are hard requirements on applications for spectrum utilization and also a constant push to move up in frequency for higher data rates. To reach high spectral efficiency, complex modulation schemes are used, which in turn require low distortion. Therefore, thorough understanding of the signal distorting mechanisms is required. In such applications, transistors are one of the key components of amplifiers, mixers, oscillators, switches, etc., and a major source of signal distortion. With the demands for higher performance, rapid prototyping, as well as lower cost for such systems and circuits, computer aided design (CAD) and simulation tools together with models for circuit elements have become increasingly important. To predict intermodulation, output power, efficiency, etc., with high accuracy, a good nonlinear model for the transistor is required.

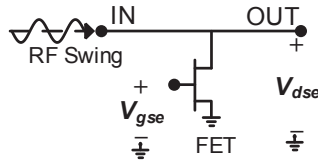


Figure 1.1: A FET operating as shunt element in switch circuit where the drain-source voltage becomes negative over a cycle of RF swing.

There are various nonlinear models available for different field-effect transistor (FET) technologies. More than often, these transistors operate as an amplifier. Hence more focus is given to model the transistors in such operating conditions. However, every model has its constraints. Unlike in amplifiers, FETs used in switch circuits have a different operating region. While the drain-source voltage in amplifiers never goes negative (except for a highly mismatched case), transistors used as shunt elements in switches also operate in the negative drain-source voltage region (see Fig. 1.1). Hence transistor models suited for amplifiers do not necessarily predict the correct behavior when operated as switch elements. There are some models available for switch FETs. Such transistors are often symmetrical around the gate (see Fig. 1.2a), a property which can drastically reduce the modeling complexity and is addressed in the thesis. The modeling procedure discussed in this thesis is not restricted to transistors used in switch circuits but is generic. Therefore the procedure can be applied for any symmetrical device e.g., MOSFET, GaAs pHEMTs/mHEMTs, InP HEMTs, etc., except power FETs (see Fig. 1.2b) where field-plates disturb the symmetry of the device [5–11].

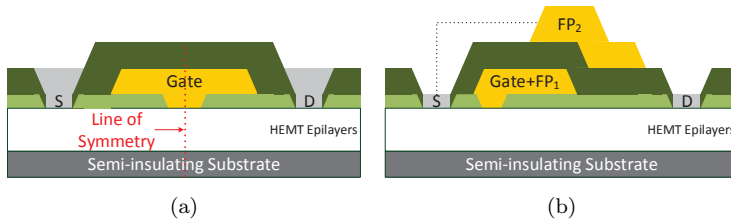


Figure 1.2: Cross-section of FETs used for switches and amplifiers: (a) symmetrical FET, (b) unsymmetrical power GaN FET with field plates [12, Fig. 1].

In this thesis, a new nonlinear modeling procedure is developed for symmetrical FETs. The discussion starts with the traditional small signal model. From that, a new symmetrical small signal model is created in Chapter 2. This model reflects the symmetry of the device forming a basis for a simplification of the nonlinear modeling procedure [Paper A]. Further in the chapter, a modified optimization based extraction is used as a tool to improve the small signal extraction result for a symmetrical FET [Paper B]. In Chapter 3, a new nonlinear modeling technique is described where it is shown that only one charge function is required to model the reactive part of the device [Paper A]. Finally, the modeling procedure only dependent on the symmetry can be extended to various other FET technologies and used to model transistors for different applications, and thus setting up the path for the future work.

## Chapter 2

# Small Signal FET Model

Transistors are used extensively in microwave circuits and are excited with varying terminal voltages. If the excitations are small enough, the nonlinear operation of the device can be linearized at the operating point. Such an operation can be modeled by an equivalent circuit called small signal model. It consists of linear elements like resistors, transconductors, capacitors, etc., to represent the small signal currents and charges in the device. These element values are directly obtained from the partial derivatives of the currents and terminal charges. Small-signal models are good approximation for the transistors in many applications like small-signal amplifiers, oscillators etc. Moreover, they also serve as a basis for empirical nonlinear models, as will be described in Chapter 3.

In this chapter, a new perspective on small-signal modeling is discussed based on existing research and a new equivalent circuit is proposed for symmetrical FETs. The first section of this chapter gives an overview on the traditional small signal model and the development of a symmetrical equivalent circuit. Furthermore, the direct extraction method for the two models and its results are briefly described in Section 2.3. Finally in Section 2.4, a modified optimization based extraction is discussed which considers the symmetry present in the device during extraction of small signal intrinsic model parameters.

### 2.1 Traditional small signal model

The traditional small-signal model for FETs shown in Fig. 2.1 can be divided into two parts, extrinsic and intrinsic [13]. The extrinsic parameters (parasitics) are bias independent elements which represent the connections to access the intrinsic device. The intrinsic parameters are commonly bias dependent and represent the physical operation of the active device. The 16-parameter model shown in Fig. 2.1 is valid up to very high frequencies [13], and the model along with its variations has been widely used in previous modeling and circuit design work [13–25]. Each of these models has the same intrinsic core. First, all of them have the two control voltages taken across the gate-source and drain-source nodes. Second, they contain one voltage controlled current source (VCCS) with the dependent voltage across the gate-source capacitance

$i_{ds} = g_m \cdot V_{gs}$  and one conductance  $g_{ds}$ . The parameters  $g_m$  and  $g_{ds}$  are computed from the derivatives of the resistive drain to source current  $I_{ds}$  as

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{const}} \quad (2.1a)$$

$$g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{gs}=\text{const}} \quad (2.1b)$$

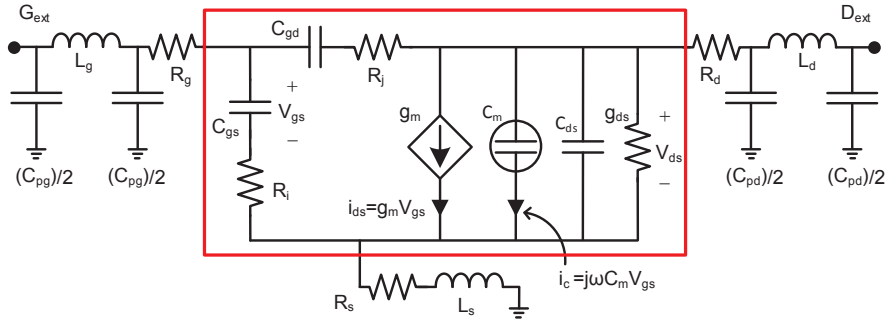


Figure 2.1: The traditional small signal model of a common source field-effect transistor containing 16 parameters. The intrinsic part is shown inside the red rectangle.

The model shown in Fig. 2.1 is valid for both symmetrical and unsymmetrical devices (see Fig. 1.2). However, due to the symmetry present in FETs (see Fig. 1.2a), the intrinsic source and drain ports are interchangeable. Therefore, a new equivalent circuit is developed in the next section where the device symmetry around the gate is exploited.

## 2.2 Symmetrical small signal model

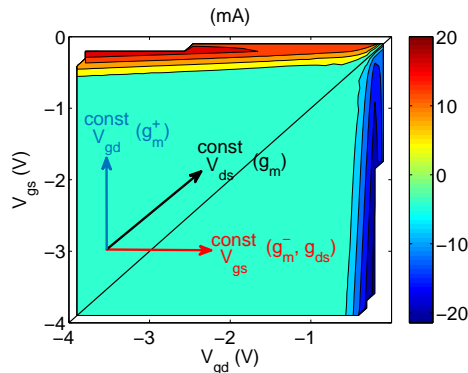


Figure 2.2: Contour plot of drain to source current of a symmetrical FET illustrating the direction of current derivatives for parameters  $g_m$ ,  $g_{ds}$ ,  $g_m^+$  and  $g_m^-$ .

For a symmetrical device, the measured drain-source DC current shows the symmetry in  $(V_{gs}, V_{gd})$  bias grid, see Fig. 2.2. Therefore,  $(V_{gs}, V_{gd})$  is a

better set of control voltages than  $(V_{gs}, V_{ds})$  to understand the symmetry in the small signal model parameters [Paper A]. In the new control voltage set, whenever  $V_{gs}$  and  $V_{gd}$  are interchanged, the intrinsic parameters like  $(C_{gs}, C_{gd})$  and  $(R_i, R_j)$  are interchanged thus existing in pairs. However, the VCCS in the traditional model has the control voltage across  $C_{gs}$ , see Fig. 2.1. When the drain and source terminals are interchanged, the control voltage for the VCCS must also be taken across  $C_{gd}$  and not across  $C_{gs}$ . Therefore, the current source  $g_m$  (see Fig. 2.1) is divided into two independent VCCS controlled by  $V_{gs}$  and  $V_{gd}$  respectively. The two new current sources are  $i_{ds}^+ = g_m^+ \cdot V_{gs}$  and  $i_{ds}^- = g_m^- \cdot V_{gd}$  where,  $g_m^+$  and  $g_m^-$  correspond to the derivatives of the resistive drain to source current (see Fig. 2.2) as

$$g_m^+ = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{gd}=\text{const}} \quad (2.2a)$$

$$g_m^- = \left. \frac{-\partial I_{ds}}{\partial V_{gd}} \right|_{V_{gs}=\text{const}} \quad (2.2b)$$

Thus in the positive  $V_{ds}$  region,  $g_m^+$  dominates over  $g_m^-$  and vice-versa. Note that  $g_m$  of the traditional model and  $g_m^+$  of the modified model are different. While  $g_m$  is a derivative in constant  $V_{ds}$  direction,  $g_m^+$  is a derivative in constant  $V_{gd}$  direction as seen in Fig. 2.2. Thus,  $g_m^+$  and  $g_m^-$  line up with the symmetry of the device observed in the  $(V_{gs}, V_{gd})$  bias grid. Moreover, since the FET is a three terminal device, the two current-sources  $i_{ds}^+$  and  $i_{ds}^-$  are sufficient to model the small-signal resistive current, thereby making  $g_{ds}$  redundant. The resulting equivalent circuit is shown in Fig. 2.3.

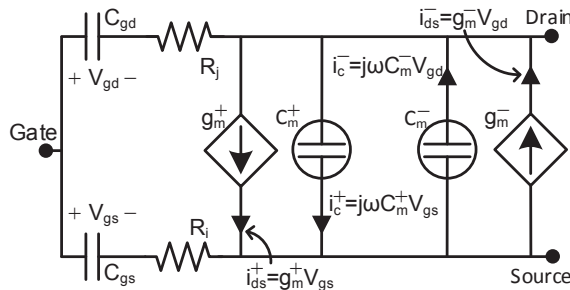


Figure 2.3: Proposed symmetrical small signal intrinsic model with two anti-parallel current sources and two transcapacitances.

While it is easy to measure current, we cannot measure charge. Therefore, we cannot plot the terminal charges in the  $(V_{gs}, V_{gd})$  bias grid to illustrate the derivation of the transcapacitance in Fig. 2.3. However, the same reasoning is applied to the transcapacitance  $C_m$  in the traditional small signal model. Hence,  $C_m$  and  $C_{ds}$  are replaced by  $C_m^+$  and  $C_m^-$  to build the symmetrical small signal model shown in Fig. 2.3. Similar to  $g_m^+$  and  $g_m^-$ ,  $C_m^+$  and  $C_m^-$  are derivatives of the drain and source charges in constant  $V_{gd}$  and  $V_{gs}$  directions respectively. Thus in the new model, all the intrinsic parameters exist in pairs and their derivatives align to the set of control voltages  $(V_{gs} - V_{gd})$ . The parameter extraction method for both the traditional and symmetrical models is briefly described in the next section.

## 2.3 Parameter extraction and model validation

This section briefly describes the direct extraction method and results of the traditional (Fig. 2.1) and symmetrical small signal models (Fig. 2.3). The parameter extraction method follows the basic principle of first extracting the extrinsic parameters from the S-parameter measurements [13, 14, 26–30]. Extrinsic parameters are extracted using cold FET measurements under pinch-off and forward gate bias conditions. While the measurement at pinch-off is taken to extract the gate-pad capacitance, the measurement at forward bias is used to extract the extrinsic series parameters  $L_g$ ,  $L_s$ ,  $L_d$ ,  $R_d$  and  $R_s$ . The drain-pad capacitance  $C_{pd}$  is set equal to  $C_{pg}$  assuming the gate and drain networks are symmetrical. Note that the extraction of the extrinsic parameters is independent of the intrinsic small signal model chosen. Therefore once extracted, the extrinsic parameters are de-embedded from the measurements to find the intrinsic admittance matrix [14] which is then used for the extraction of intrinsic parameters.

### 2.3.1 Traditional model parameter extraction

The intrinsic model parameters are extracted from the deembedded admittance matrix using the admittance relation of the equivalent circuit [13]. For the present analysis, the traditional model shown in Fig. 2.1 (and the symmetrical model) is simplified by neglecting the intrinsic resistances ( $R_i$  and  $R_j$ ) present in series with the gate-source and gate-drain capacitances. However, note that their effects will appear mainly at higher frequencies [19]. The simplified intrinsic common source Y-parameters for the traditional model are then given by

$$\mathbf{Y}_{\text{int}} = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ g_m + j\omega(C_m - C_{gd}) & g_{ds} + j\omega(C_{ds} + C_{gd}) \end{bmatrix}. \quad (2.3)$$

Once the intrinsic admittance relation of the equivalent circuit is known, the parameters are extracted by applying a reverse analytical solution using the deembedded admittance matrix. The extracted parameters are shown in Fig. 2.4 for a commercial GaAs pHEMT device<sup>1</sup> as an example. The parameters  $C_{gs}$  and  $C_{gd}$  are clearly mirrors of each other as expected from a symmetrical device. From Fig. 2.4c, transconductance  $g_m$  seems to contain a symmetry between the positive and negative  $V_{ds}$  region due to the current derivative in constant  $V_{ds}$  direction. However,  $C_{ds}$  does not show any such behavior irrespective of the device being symmetrical. Furthermore, the extracted  $C_{ds}$  is negative in the negative  $V_{ds}$  region, see Fig. 2.4d. The reason for  $C_{ds}$  becoming negative is clarified in the context of the symmetrical model in the next section.

### 2.3.2 Symmetrical model parameter extraction

Extraction of the intrinsic parameters for the symmetrical model (see Fig. 2.3) follows the same procedure as described for the traditional model in the previous section. The intrinsic admittance matrix of the symmetrical model is

<sup>1</sup>WIN Semiconductor PP10  $2 \times 25\mu\text{m}$  on-wafer GaAs pHEMT MMIC process



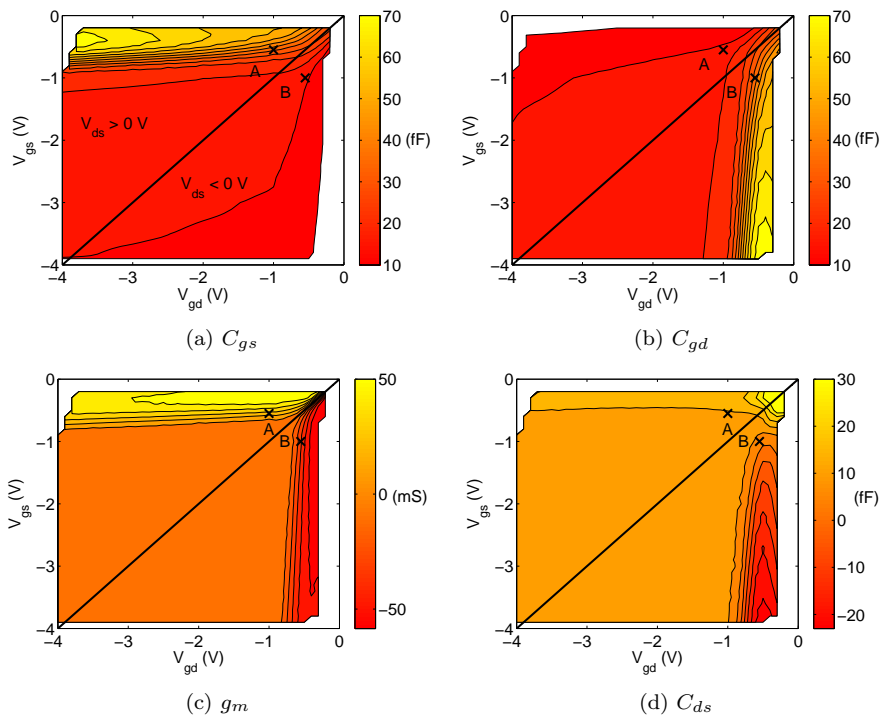


Figure 2.4: Bias dependence of the traditional small signal model intrinsic parameters of the DUT in an intrinsic  $V_{gs} - V_{gd}$  bias grid (a)  $C_{gs}$  (fF), (b)  $C_{gd}$  (fF), (c)  $g_m$  (mS), (d)  $C_{ds}$  (fF).

given by

$$\mathbf{Y}_{\text{int}}^{\text{sym}} = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ j\omega(C_m^+ - C_{gd} - C_m^-) + g_m^+ - g_m^- & j\omega(C_{gd} + C_m^-) + g_m^- \end{bmatrix} \quad (2.4)$$

where again the parameters  $R_i$  and  $R_j$  are neglected for simplification of the analysis. The new parameters in (2.4) are related to the traditional model parameters in (2.3) as

$$g_m^- = g_{ds} \quad (2.5a)$$

$$g_m^+ = g_{ds} + g_m \quad (2.5b)$$

$$C_m^- = C_{ds} \quad (2.5c)$$

$$C_m^+ = C_{ds} + C_m. \quad (2.5d)$$

Using (2.5), the proposed model parameters can also be directly calculated from the traditional model parameters and are shown in Fig. 2.5.

For the symmetrical small signal model, the results clearly show that the parameters  $(g_m^+, g_m^-)$ ,  $(C_m^+, C_m^-)$  in Fig. 2.5 and  $(C_{gs}, C_{gd})$  in Fig. 2.4 exist in pairs and are mirrors of one another along  $V_{ds} = 0$  V. This confirms the proposed symmetry for the device under test (DUT). Therefore, the parameters of the proposed model in the negative  $V_{ds}$  region can be calculated by mirroring their corresponding parameters from the positive  $V_{ds}$  bias region. The number of measurement points can thus effectively be halved. Furthermore since

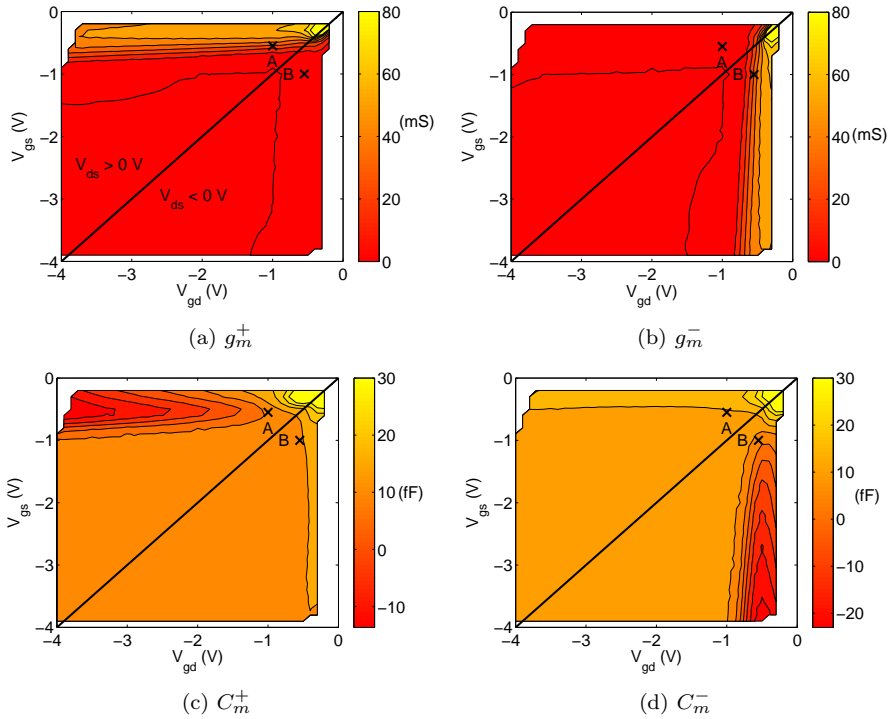


Figure 2.5: Bias dependence of the symmetrical small signal model intrinsic parameters of the DUT in an intrinsic  $V_{gs} - V_{gd}$  bias grid covering both the positive and negative  $V_{ds}$  region: (a)  $g_m^+$  (mS), (b)  $g_m^-$  (mS), (c)  $C_m^+$  (fF), and (d)  $C_m^-$  (fF).

$C_{ds}$  and  $C_m^-$  are equal as given by (2.5c),  $C_{ds}$  in the negative  $V_{ds}$  region (see Fig. 2.4d) is effectively a transcapacitor represented by  $C_m^-$  in the symmetrical model (see Fig. 2.5d). This explains why  $C_{ds}$  is negative in Fig. 2.4d.

### 2.3.3 Validation of model symmetry

For the validation of symmetry in the model shown in Fig. 2.3, the intrinsic model parameters in the negative  $V_{ds}$  region are obtained by mirroring the extracted model in the positive  $V_{ds}$  region. The model is validated by comparing the mirrored model to the corresponding S-parameter measurements in the negative  $V_{ds}$  region. The difference between the measured and simulated S-parameters using the mirrored model is computed using a mean square error (MSE) as

$$\epsilon = \sum_{j=1}^2 \sum_{k=1}^2 \frac{1}{\max |S_{jk}|^2} \sum_{i=1}^N |S_{jk}(\omega_i) - S_{jk}^{\text{mod}}(\omega_i)|^2. \quad (2.6)$$

The maximum modeling error given by (2.6) is obtained at bias point B where the model is mirrored from bias point A, marked in Fig. 2.4 and 2.5. For the validity of the symmetry in the model, S-parameters are compared at both bias point A and B and are shown in Fig. 2.6. The agreement between the simulated

model and measurements at bias point A validates the symmetrical model in the positive  $V_{ds}$  region. Whereas at B, which is the point of maximum modeling error, the agreement validates that the model can be mirrored. Therefore, symmetrical devices can be modeled by the equivalent circuit given in Fig. 2.3 and mirrored as

$$C_{gd}(V_{gd}, V_{gs}) = C_{gs}(V_{gs}, V_{gd}) \quad (2.7a)$$

$$C_m^-(V_{gd}, V_{gs}) = C_m^+(V_{gs}, V_{gd}) \quad (2.7b)$$

$$g_m^-(V_{gd}, V_{gs}) = g_m^+(V_{gs}, V_{gd}). \quad (2.7c)$$

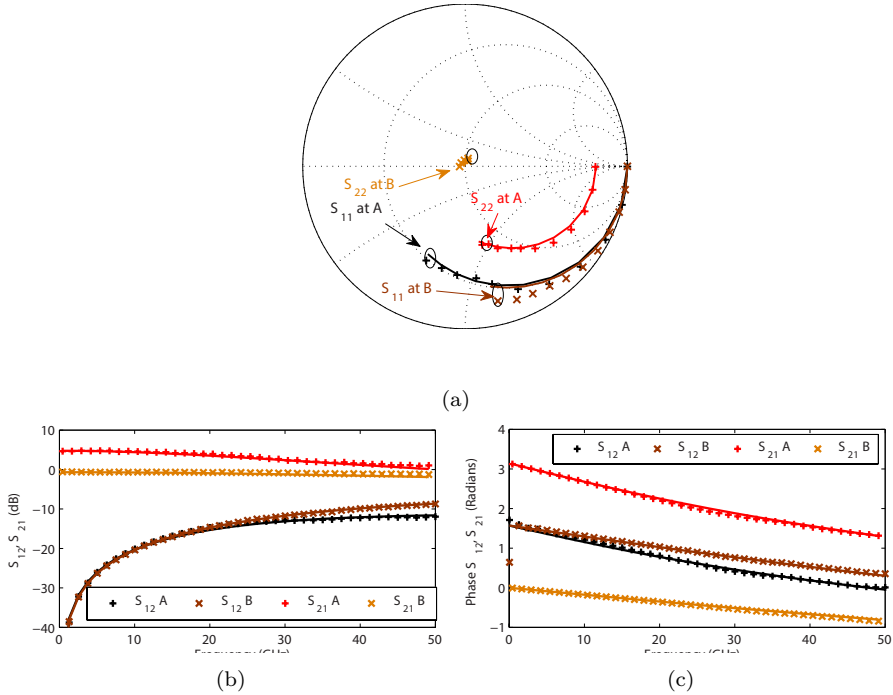


Figure 2.6: Comparison of S-parameters (a)  $S_{11}$  and  $S_{22}$ , (b)  $\text{dB}(S_{12}, S_{21})$ , (c)  $\text{phase}(S_{12}, S_{21})$  from 100 MHz to 50 GHz between measured (+: Bias A -  $V_{gs} = -0.55$  V,  $V_{gd} = -1$  V,  $\times$ : Bias B -  $V_{gs} = -1$  V,  $V_{gd} = -0.55$  V) and model(-). The model at B is obtained from the extracted model at A, see Fig. 2.4 and 2.5.

## 2.4 Optimizing model parameters

The direct extraction method solely relying on the analytical solution assumes the S-parameter measurements being almost ideal. As the measurement uncertainties increase, difficulties in extracting the model parameters accurately also increase. Moreover two sets of cold S-parameter measurements cannot determine all the extrinsic parameters uniquely. This greatly influences the extraction of intrinsic elements [19, 31]. Therefore optimizing the parameters helps to reduce the effects of measurement uncertainties [32–36]. However,

the optimizer based extraction is computationally more intensive and it can converge to a local minima. Therefore the sequential single parameter optimization proposed in [32, 33, 36] is used which is more robust against local minima. For better convergence, direct extraction results are used as seeds to the optimizer [37–40]. The modeling error  $\epsilon$  used for optimization is given by (2.6). To account for the symmetry, the optimizer is modified for extracting the intrinsic parameters and is verified for a commercial GaN device<sup>2</sup> [Paper B].

### 2.4.1 Multibias extraction of parasitics

To extract the parasitics (or extrinsic parameters), the multibias extraction method from [36] is used. The method is based on the sequential single parameter optimization [32, 33] at several bias points in different operating regions, see Fig. 2.7. Since the parasitics are bias independent, the method significantly improves the estimation of the parasitics. Once the parasitics are extracted, the intrinsic parameters are extracted using a modified optimizer based extraction described in the next section.

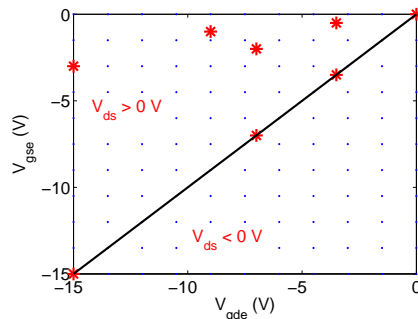


Figure 2.7: Location of bias points (\*) for the multibias extraction in extrinsic  $V_{gse} - V_{gde}$  bias grid.

### 2.4.2 Optimization of the symmetrical intrinsic parameters

For the optimization based extraction, if the extrinsic resistance  $R_s$  and  $R_d$  are similar [Paper B, Table I], intrinsic parameters can also be mirrored in the extrinsic  $V_{gse} - V_{gde}$  bias grid. Therefore, the parameters can be optimized in the extrinsic bias grid without the need of any interpolation algorithms. Furthermore, for the symmetrical model, the first important change in the optimizer from [32, 33] is to optimize the intrinsic parameters for a bias point together with the mirrored bias point in the other half using the same seed value, see Fig. 2.8. Moreover, the error function for such an optimization process must have contributions from both the regions with equal weights.

While the main reason to use an optimizer is to reduce the modeling error, it is also important to obtain parameter values that are easier to fit into a nonlinear model. Therefore, the direct extraction results are used as seeds

<sup>2</sup> $8 \times 100\mu\text{m}$  UMS GH25-10 V9C on-wafer GaN process

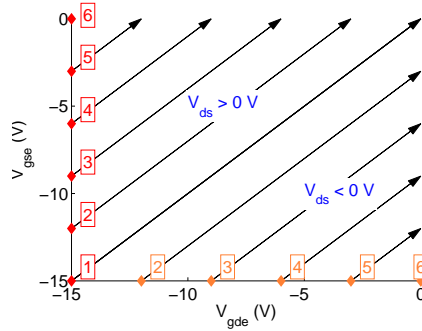


Figure 2.8: Arrows showing the direction of optimization with direct extraction results used as seed shown by red ( $\diamond$ ) in extrinsic  $V_{gse} - V_{gde}$  bias grid. The orange ( $\diamond$ ) represent the mirrored seeds for optimization in negative  $V_{ds}$  region and number inside red and orange  $\square$  represent sweep iterations.

at the first bias point and the optimized parameters are used as seed at the subsequent bias points. This procedure is repeated for each sweep in the bias grid to ensure smoothness, see Fig. 2.8. Note that the optimizer will face high gradient change in  $C_{gs}$ ,  $g_m^+$  and  $C_m^+$  along the constant gate-drain voltage and in parameters  $C_{gd}$ ,  $g_m^-$  and  $C_m^-$  along the constant gate-source voltage. Therefore, the sweep direction (or direction of optimization) is chosen along the constant extrinsic drain-source voltage  $V_{dse}$ , see Fig. 2.8. The detailed steps of optimization based extraction is described in section III in [Paper B].

### 2.4.3 Optimized parameters and model validation

Three of the six intrinsic parameters extracted using the modified sequential optimization method are shown in Fig. 2.9. The high gradient change is clearly visible along constant  $V_{gde}$  direction from the concentration of contour lines. The remaining intrinsic parameters ( $C_{gd}$ ,  $C_m^-$ , and  $g_m^-$ ) are mirrored using (2.7).

The benefit of the optimizer based extraction is to find a minima for the specified error function and obtain results better than the direct extraction. Therefore, the modeling error given by (2.6) is compared for the direct and modified optimizer based extraction in Fig. 2.10. While an improvement is observed for the modified optimizer compared to the direct extraction results, the optimizer based extraction shows higher error at  $V_{gse} = -3.25$  V,  $V_{gde} = -3.25$  V. This bias point is on the  $V_{dse} = 0$  V line where the optimizer fails to model the steep gradient in all the intrinsic parameters near pinch-off of the transistor, see Fig. 2.9. This rise in error can be reduced by several simple techniques. First, a dense measurement grid around pinch-off will help the optimizer to model the change in parameter values in smaller step sizes. Second, to use the direct extraction results at the points where the optimizer is showing a rise in the error. And third, to use selective seeds, where the optimizer can choose whether to use the direct extraction result or the parameters from the previous or nearest optimized point as the seed value by comparing the initial error. While the increase in error is limited to a very small region, the overall improvement in the modeling error verifies the applicability of the

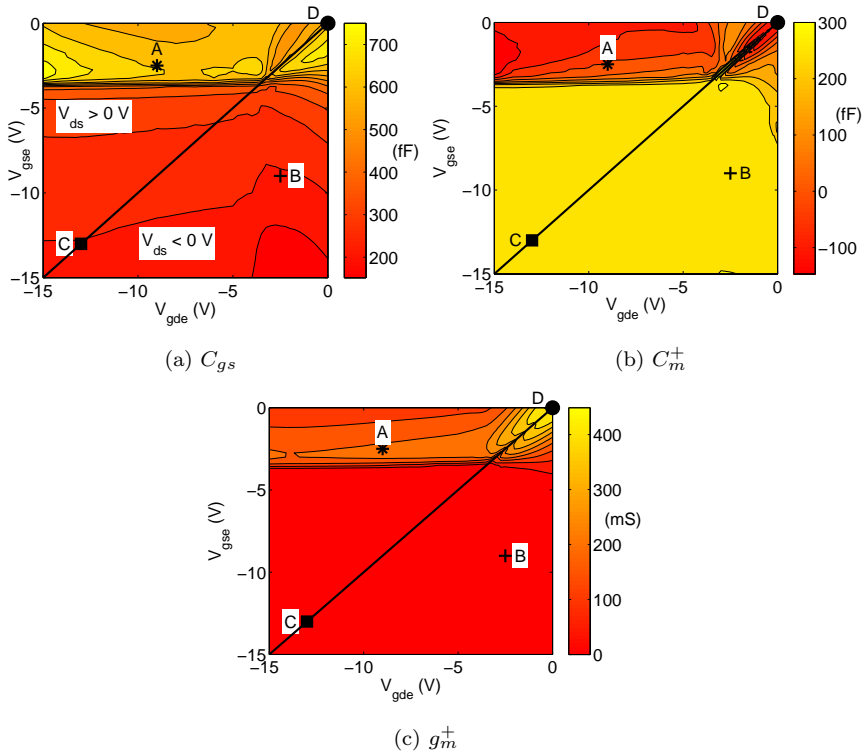


Figure 2.9: Optimized small signal model intrinsic parameters in an extrinsic  $V_{gse} - V_{gde}$  bias grid for a commercial GaN HEMT: (a)  $C_{gs}$  (fF), (b)  $C_m^+$  (fF), and (c)  $g_m^+$  (mS).

modified optimizer for extraction of the symmetrical model parameters. To verify the optimized results, S-parameters are simulated at four bias points A–D (marked in Fig. 2.9 and 2.10) and compared to the measurements, see Fig. 2.11. A good match at all four bias points validate the modified optimizer based extraction procedure.

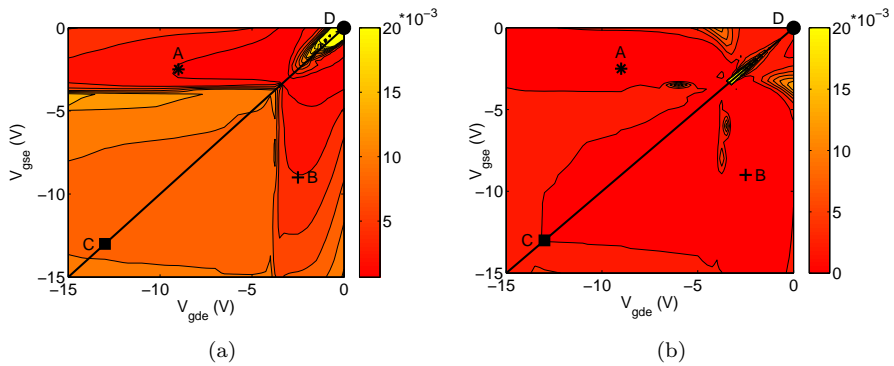


Figure 2.10: Comparison of the modeling error  $\epsilon$  between the direct extraction (left) and the modified optimizer based extraction (right) for the GaN DUT.

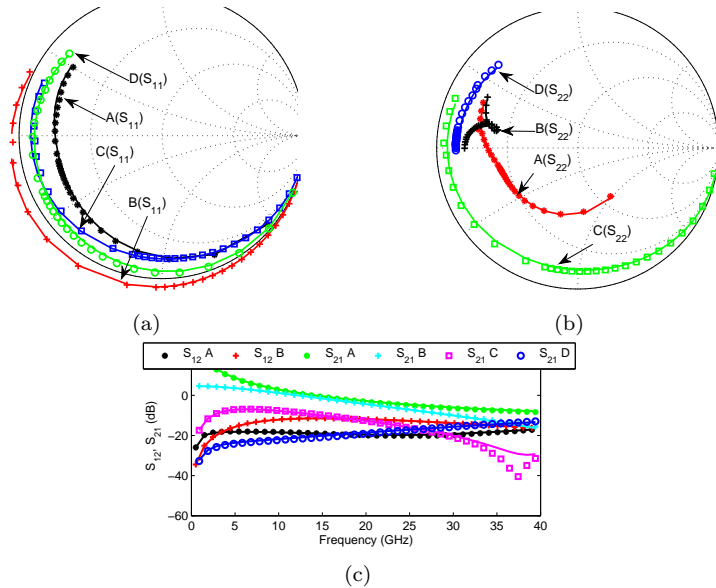


Figure 2.11: Comparison between measured(marker) and model(-) S-parameters (a)  $S_{11}$ , (b)  $S_{22}$  and (c)  $S_{21}$  and  $S_{12}$  from 500 MHz to 40 GHz at bias points A–D (marked in Fig. 2.9 and 2.10) for the GaN DUT.





## Chapter 3

# Nonlinear FET Model

Microwave devices are often excited with large input signals causing them to operate nonlinearly. For that purpose, the small signal models discussed in Chapter 2 are not sufficient to predict the behavior of a transistor and a nonlinear model is essential. There are three major approaches for modeling the nonlinearities of a transistor. The first one is the physical model where the model is derived from the geometry and material data. This provides a direct link between the physical parameters and the electrical performance, and most models of silicon based transistors are derived this way [41]. The second method is based on look-up tables where measured data provides a complete experimental characterization of the electrical behavior e.g., [42]. However, look-up table based models in general do not have the possibility of extrapolation beyond the describing data set [29, pp. 130–135]. The third category is empirical models where the device model is created using linear and nonlinear lumped elements as shown in Fig. 3.1.

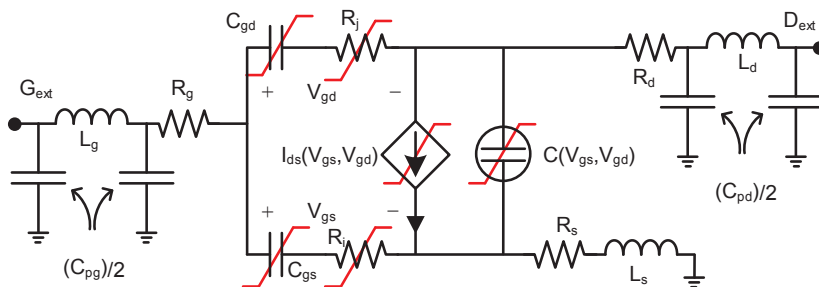


Figure 3.1: Nonlinear equivalent circuit for an FET showing linear and nonlinear elements in common source configuration.

The empirical model shown in Fig. 3.1 is related to the small signal model in Fig. 2.3 and is commonly used for microwave FETs. The linear and nonlinear parameters in the nonlinear model are related to the small signal bias independent and dependent parameters respectively. Since the small signal model is a linearization of the equivalent circuit in Fig. 3.1, the current and charge (or capacitance) expressions can be obtained from the extracted small signal parameters [29, pp. 139–152]. The analytical expressions for the cur-

rents and terminal charges in nonlinear models are different due to the different current and charge profiles (e.g. [15,16] for GaAs, [23,43] for GaN, [44] for LD-MOS, etc.). While many of these models are not defined for negative  $V_{ds}$  bias e.g., [15,16,43–56], the discussion in this chapter is limited to nonlinear models valid in both the positive and negative  $V_{ds}$  region.

This chapter proceeds with a brief overview on available symmetrical nonlinear models. In section 3.2, the symmetry in the intrinsic capacitances of the small signal model discussed in previous chapter is extended to a nonlinear charge model [Paper A]. It is shown that only one charge expression is required to model the reactive part of a symmetrical device. Furthermore, in section 3.3 and 3.4, a nonlinear model is developed for the GaAs pHEMT used in Chapter 2 and verified with S-parameters and large-signal waveform measurements.

### 3.1 Symmetrical models: An overview

The need for symmetrical models arises from the operation of transistors in both the positive and negative  $V_{ds}$  region. There are a few models available which target specific applications e.g., [18] for FETs in resistive mixers, [23,25] for FETs in switches. Table 3.1 gives an overview of the symmetrical FET models that have been published. These models consider the symmetry in the drain to source current expressions, which means that the same parameters are used in the positive and negative  $V_{ds}$  region. Yet for these models, the reactive part of the device is still dependent on two or more charge or capacitance expressions. While the model in [57] has a constant  $C_{ds}$  which is not valid in the negative  $V_{ds}$  region, see Fig. 2.4d, the Yhland model [18] contains constant  $C_{ds}$ ,  $C_{gs}$ ,  $C_{gd}$  limiting its use at high microwave frequencies. Moreover, the model in [23] contains three nonlinear capacitances and the model in [25] contain two nonlinear charge expressions from the gate and drain terminals. Neither of these models does use the symmetry present in the reactive currents and terminal charges in the device, see Fig. 2.3. In the next section, the symmetry in the terminal charges is discussed which is dependent on the symmetrical small signal model (see Fig. 2.3) in Chapter 2.

Table 3.1: List of symmetrical FET models

Model name	Charge model
Chalmers Model [57, 58]	One nonlinear charge model (for $C_{gs}$ and $C_{gd}$ ), one constant for $C_{ds}$
Yhland model [18, 59]	Three constants for $C_{ds}$ , $C_{gs}$ , $C_{gd}$
Switch model [25]	Two nonlinear charge expression
Switch model [23]	Three nonlinear capacitance model (for $C_{gs}$ , $C_{gd}$ and $C_{ds}$ )
Paper A	One charge expression

## 3.2 Charge model

Modeling the nonlinear charges in a device is critical to accurately predict bias dependent S-parameters, harmonic and intermodulation distortion, ACPR etc. [60]. The contribution of the charge to the current at node  $i$  is expressed as [29, eq. 5.9]

$$I_i(t) = \frac{dQ_i(V_1(t), V_2(t))}{dt} \quad (3.1)$$

where,  $V_1(t)$  and  $V_2(t)$  are the two independent intrinsic voltages of a three terminal device. For a FET, the two independent voltages commonly chosen are across the gate-source and drain-source terminals respectively. Therefore, the gate and drain charge functions  $Q_g(V_{gs}, V_{ds})$  and  $Q_d(V_{gs}, V_{ds})$  are typically used to define the reactive currents in nonlinear transistor models. However, since the drain and source terminals of a symmetrical device are identical, it is advantageous to instead model the drain charge  $Q_d^{\text{sym}}(V_{gs}(t), V_{gd}(t))$  and the source charge  $Q_s^{\text{sym}}(V_{gs}(t), V_{gd}(t))$ . Using (3.1), the reactive currents at the source and drain terminals can then be written as

$$\begin{bmatrix} I_s(t) \\ I_d(t) \end{bmatrix} = \begin{bmatrix} dQ_s^{\text{sym}}/dt \\ dQ_d^{\text{sym}}/dt \end{bmatrix} = \begin{bmatrix} \partial Q_s^{\text{sym}}/\partial V_{gs} & \partial Q_s^{\text{sym}}/\partial V_{gd} \\ \partial Q_d^{\text{sym}}/\partial V_{gs} & \partial Q_d^{\text{sym}}/\partial V_{gd} \end{bmatrix} \cdot \begin{bmatrix} dV_{gs}(t)/dt \\ dV_{gd}(t)/dt \end{bmatrix}. \quad (3.2a)$$

The partial derivatives of the charges at the source and drain port can further be computed as

$$\left. \frac{\partial Q_s^{\text{sym}}}{\partial V_{gs}} \right|_{V_{gd}=\text{const}} = -C_{gs} - C_m^+ \quad (3.3a)$$

$$\left. \frac{\partial Q_s^{\text{sym}}}{\partial V_{gd}} \right|_{V_{gs}=\text{const}} = C_m^- \quad (3.3b)$$

$$\left. \frac{\partial Q_d^{\text{sym}}}{\partial V_{gd}} \right|_{V_{gs}=\text{const}} = -C_{gd} - C_m^- \quad (3.3c)$$

$$\left. \frac{\partial Q_d^{\text{sym}}}{\partial V_{gs}} \right|_{V_{gd}=\text{const}} = C_m^+ \quad (3.3d)$$

where,  $C_{gs}$ ,  $C_{gd}$ ,  $C_m^+$  and  $C_m^-$  correspond to the small signal model parameters defined in Section 2.2, see Fig. 2.3. From (2.7) and (3.3), the partial derivatives of  $Q_s^{\text{sym}}$  and  $Q_d^{\text{sym}}$  are symmetrical. Therefore the charge functions are also symmetrical according to

$$Q_s^{\text{sym}}(V_{gs}, V_{gd}) = Q_d^{\text{sym}}(V_{gd}, V_{gs}). \quad (3.4)$$

Consequently, it is sufficient to model either  $Q_s^{\text{sym}}$  or  $Q_d^{\text{sym}}$  to define the reactive part of the intrinsic device. Thus, compared to modeling the gate and drain charges independently as in traditional models, the symmetry simplifies the modeling procedure with only one charge model needed. In the next section, a symmetrical nonlinear model is developed to exemplify how this is performed.

### 3.3 Symmetrical nonlinear model example

For the symmetrical nonlinear model, the extrinsic and intrinsic small signal parameters extracted for the commercial GaAs pHEMT device<sup>1</sup> in Chapter 2 are used. The current and charge model is briefly described in the following subsections, respectively.

#### 3.3.1 Nonlinear Current Model

To model the extracted small signal parameters  $g_m^+$  and  $g_m^-$  of the GaAs pHEMT, the drain to source current ( $I_{ds}$ ) model in [18] is used. The model parameters are obtained by manual fitting of the measured and modeled DC data and are listed in Table 3.2. The comparison of the modeled and measured current is shown in Fig. 3.2a validating the accuracy of the current model. Although the measured current is symmetrical in  $V_{gs}-V_{gd}$  bias grid (see Fig. 3.2b), the current characteristics is not symmetrical in Fig. 3.2a since it is along constant  $V_{gs}$  lines.

Table 3.2: Model parameters for current [18].

Parameter	$\phi$	$g$	$a$	$b$	$c$	$d$
Value	$3^\circ$	0.043 A	$0.02 \text{ V}^{-1}$	$2.8 \text{ V}^{-1}$	0.23 V	$12 \text{ V}^{-1}$

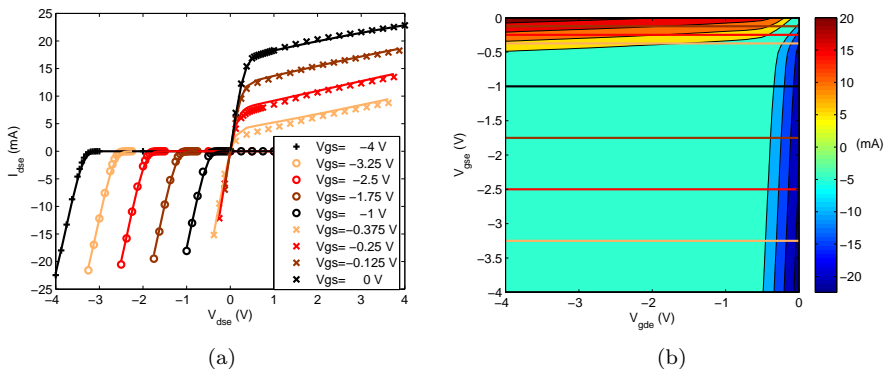


Figure 3.2: Yhland symmetrical current model for the GaAs DUT showing (a) comparison of measured(marker) versus modeled(-) I-V characteristics, (b) contour plot of  $I_{ds}$  with the constant  $V_{gs}$  sweeps in the left figure drawn in corresponding colors.

#### 3.3.2 Nonlinear Charge Model

For a symmetrical device, since it is sufficient to model one charge expression as explained in section 3.2, the source-charge  $Q_s^{\text{sym}}$  is considered in this example. Due to charge conservation,  $Q_s^{\text{sym}}$  is related to the traditional gate and drain charges,  $Q_g$  and  $Q_d$ , respectively, by

$$Q_s^{\text{sym}}(V_{gs}, V_{gd}) = -Q_g(V_{gs}, V_{gd}) - Q_d(V_{gs}, V_{gd}). \quad (3.5)$$

<sup>1</sup>WIN Semiconductor PP10  $2 \times 25 \mu\text{m}$  on-wafer GaAs pHEMT MMIC process

A combination of the gate and drain charge models from [25] and [61] are used to manually fit the extracted small-signal intrinsic capacitances presented in Fig. 2.4 and 2.5. Furthermore, a reduction function  $R(V_a)$  from [44, eq. (7)] is introduced in [61, eq. (15)] to correct the behavior at high  $V_{gs}$  and  $V_{gd}$ . The modified expression [61, eq. (15)], including the reduction function  $R(V_a)$  is given by

$$f(V_a, V_b) = C_0 \cdot \left[ V_a + C_f \cdot \log \left( \cosh(S_g \cdot W(V_a, V_b)) / S_g \right) - R(V_a) \right] \quad (3.6)$$

where,

$$W(V_a, V_b) = V_a - \eta \cdot V_a \cdot V_b - D_c \cdot \tanh(D_k \cdot V_b) \quad (3.7)$$

$$R(V_a) = (a_1/m_2) \cdot \ln \left( 1 + e^{m_2 \cdot (V_a - V_r)} \right). \quad (3.8)$$

The complete source charge expression becomes

$$Q_s^{\text{sym}}(V_{gs}, V_{gd}) = \underbrace{f(V_{gs}, V_{gd})}_{(3.6)} + \underbrace{C_{gs0} \cdot V_{gs}}_{[61, \text{eq. (13)}]} + \underbrace{f(V_{gd}, V_{gs})}_{(3.6)} + \underbrace{C_{gd0} \cdot V_{gd}}_{[61, \text{eq. (14)}]} + \underbrace{Q_d(V_{gs}, V_{gd})}_{[25, \text{eq. (A-2)}]}. \quad (3.9)$$

The parameters for the charge expression using manual fitting are listed in Table 3.3. The drain charge function  $Q_d^{\text{sym}}$  is obtained using (3.4).

Table 3.3: Fitting parameters of the charge model from [25,61] and (3.8).

Parameter	Value	Parameter	Value
$C_{gs0}$	19 fF	$C_{gd0}$	19 fF
$C_0$	1.1 fF	$C_f$	5.3 V
$S_g$	5 V <sup>-1</sup>	$a_1$	20
$m_2$	8 V <sup>-1</sup>	$V_r$	-0.15 V
$\eta$	0.03 V <sup>-2</sup>	$D_c$	0.53 V
$D_k$	1 V	$C_{ds0}$	14 fF
$C_{ds1}$	1.1 fF V <sup>-1</sup>	$C_{ds8}$	$-4.2 \times 10^{-7}$ fF V <sup>-8</sup>
$C_{ds13}$	$3.5 \times 10^{-12}$ fF V <sup>-13</sup>	$V_{gs0}$	-9.7 V

Fig. 3.3 shows the comparison between the extracted and modeled small signal capacitances. Even though some mismatch is observed in  $C_m^+$  at high  $V_{gs} - V_{gd}$ , we conclude that a common charge function is sufficient to create the complete nonlinear model (see Fig. 3.4) for the large-signal measurements in the following section.

### 3.4 Model Validation

The symmetrical modeling of FETs in this thesis is motivated from switches where transistors are often used in shunt configuration. Therefore, the small- and large-signal measurements of the DUT in common-source configuration are verified at the on/off operating points of transistors when used in switch circuits.

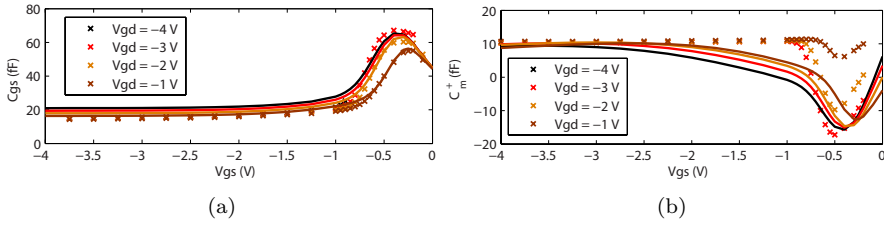


Figure 3.3: Comparison of (a)  $C_{gs}$  versus  $V_{gs}$  and (b)  $C_m^+$  versus  $V_{gs}$  between extracted small-signal capacitance ( $\times$ ) and modeled capacitance ( $-$ ) obtained using charge expression (3.9).

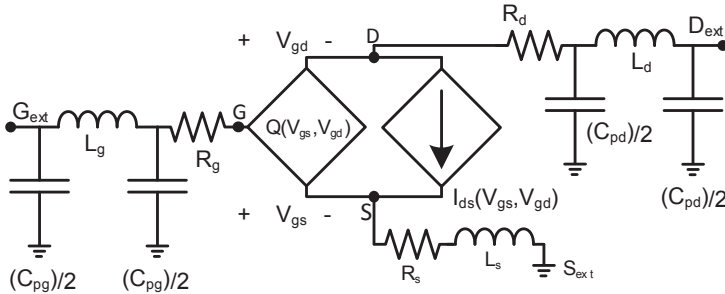


Figure 3.4: Proposed large signal model for a symmetrical common source device.

### 3.4.1 Small signal verification

For small signal verification, the drain-source bias is kept fixed at 0 V volts while the gate-source voltage is set at 0 V for the ON state and -4 V for the OFF state of the switch. Measured and simulated S-parameters are compared and shown in Fig. 3.5. Some mismatch is observed in the phase of  $S_{11}$  at the ON state due to the mismatch in  $C_m^+$ , see Fig. 3.5a. Hence, further improvements are required in the charge model to correctly predict the extracted small-signal capacitances.

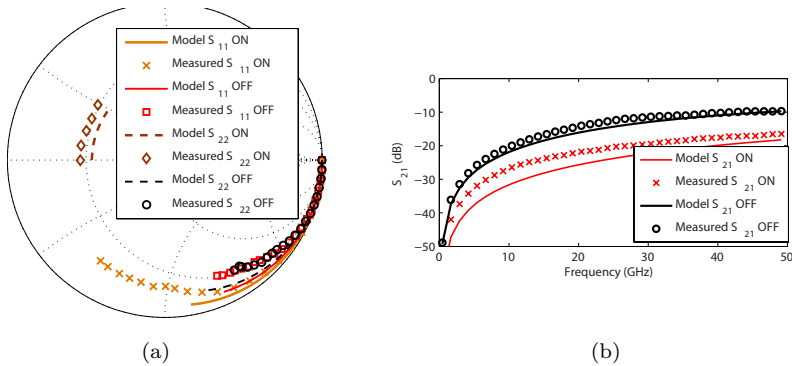


Figure 3.5: Measured ( $\times$ -ON,  $\circ$ -OFF) and modeled ( $-$ ) S-parameters (a)  $S_{11}$  and  $S_{22}$ , (b)  $S_{21}$  from 100 MHz to 50 GHz at ON and OFF-state of a switch.

### 3.4.2 Large-Signal Verification

Large-signal measurements are performed with the large-signal network analyzer (LSNA) (Maury MT4463) to emulate the operation of the DUT in a real high power shunt switch operation. The measurement setup is shown in Fig. 3.6, where the extrinsic gate is terminated in  $50\ \Omega$ . The drain-source bias is kept fixed at  $0\ \text{V}$  volts while the gate-source voltage is set at  $0\ \text{V}$  for the ON state and  $-2.5\ \text{V}$  for the OFF state to allow a large RF swing. The DUT is excited with RF at the drain terminal similar to shunt switch operation (see Fig. 1.1) and the incident and reflected waves are measured at both the drain and gate terminals.

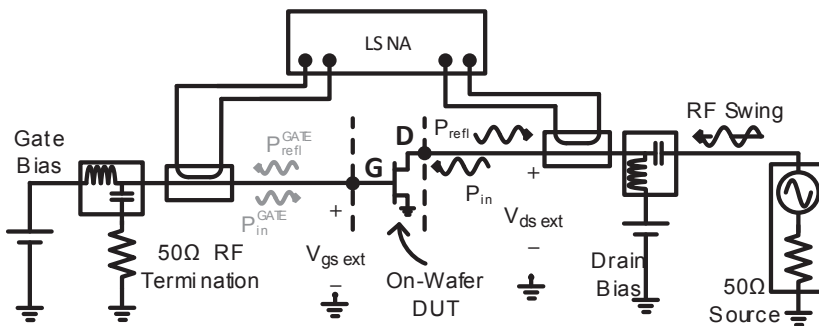


Figure 3.6: Large signal measurement setup with LSNA, signal source and on-wafer DUT with  $50\ \Omega$  RF termination at gate. The reference plane of measurement is at the probe tips.

To predict the harmonic response of the model with correct harmonic terminations seen during the measurements, the measured incident waves at the fundamental and the higher harmonics are injected in the respective ports during simulations. Furthermore, the incident voltage wave at the gate terminal (see Fig. 3.6) is also used in the simulation to compensate any mismatch due to the  $50\ \Omega$  RF termination. At low frequencies, the harmonics are generated mainly by the nonlinear current source and at higher frequencies, the harmonics are also dependent on reactive currents generated by the nonlinear charge model. Therefore, to validate the current and charge model, the simulated and measured reflected power are compared for varying incident RF power at  $600\ \text{MHz}$  and  $16\ \text{GHz}$ , respectively.

Fig. 3.7 shows the comparison between the simulated and measured harmonics at the ON state of the shunt switch. The good agreement in Fig. 3.7a ( $600\ \text{MHz}$ ) validates the nonlinear current model and in Fig. 3.7b ( $16\ \text{GHz}$ ), it validates the nonlinear charge model for the GaAs pHEMT. At power levels below the noise floor of the measurement setup, according to the simulation procedure outlined above, the measured noise is injected into the model simulation causing the noisy model response. This injected noise will also influence the phase of the reflected wave at higher harmonics. Therefore, the phase of the measured and simulated reflected wave at the fundamental frequency of the measurements are compared in Fig. 3.8 showing good agreement. Thus, the validation using both small- and large-signal measurements confirm the accuracy of the model and the overall symmetrical modeling procedure.

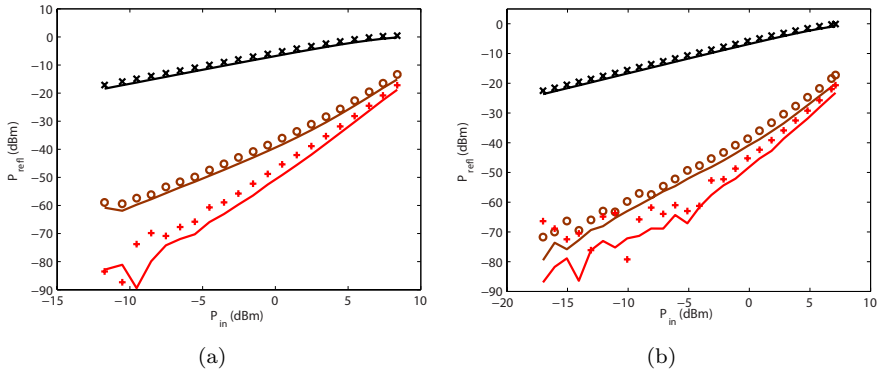


Figure 3.7: Comparison between magnitude of the measured (fundamental frequency:  $\times$ , second harmonic:  $\circ$  and, third harmonic:  $+$ ) and simulated(-) reflected versus incident power at the drain of the DUT at (a) 600 MHz, (b) 16 GHz at the ON state ( $V_{gse} = 0$  V,  $V_{dse} = 0$  V). For OFF-state validation, see Fig. 14 in [Paper A].

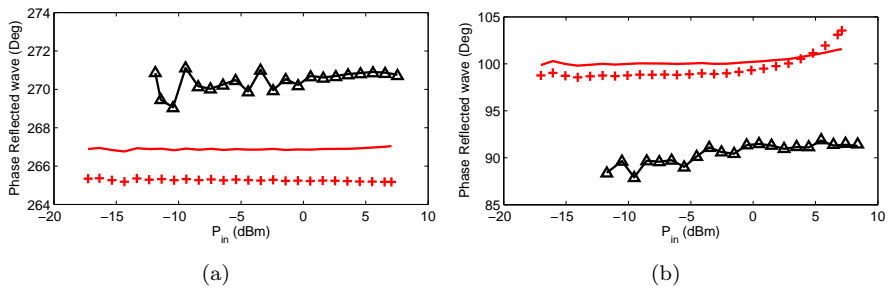


Figure 3.8: Comparison between the model (-) and measured ( $\Delta$ : 600 MHz,  $+$ : 16 GHz) phase of the reflected wave ( $P_{refl}$ ) at the drain port for the fundamental frequencies (a) at OFF state ( $V_{gse} = -2.5$  V,  $V_{dse} = 0$  V, and (b) at ON state ( $V_{gse} = 0$  V,  $V_{dse} = 0$  V of the DUT.



# Chapter 4

## Conclusions

In this thesis, the emphasis is on the device symmetry as an important feature to simplify the empirical modeling and parameters extraction methods for FETs. While the modeling procedure is based on existing techniques, the device symmetry leads to a new small-signal equivalent model. The proposed model allows mirroring of the parameters between the positive and negative drain-source regions, thus reducing the number of measurements by half [Paper A]. The work is validated using a commercial GaAs FET. Further, the symmetrical equivalent model parameters are optimized using a modified optimization based extraction to take the symmetry into consideration [Paper B]. The optimization of parameters was performed on a commercial GaN HEMT showing that the symmetrical equivalent circuit is also a generic FET small signal model. Furthermore, the symmetrical small-signal model was extended to a nonlinear model, where a proper use of the device symmetry allowed the reactive parts of the intrinsic device to be modeled using a single common charge expression. Thus, effectively simplifying the nonlinear model and reducing the number of charge expressions to define the model [Paper A]. Even though the modeling work is motivated from transistors used in switch circuits, the procedure is generic to all symmetrical FETs and can be extended to other technologies.

### 4.1 Future work

During the work with this thesis, several interesting topics for future work have emerged and are hereby listed:

- Better and robust extraction of the common charge function with reduced number of parameters.
  - Further work is required to improve the charge model developed for the GaAs DUT based on existing expressions. A common charge expression also opens up the possibility of modeling the nonlinear reactive part of a symmetrical device with fewer parameters.
- To validate the model with an MMIC circuit design.

- To investigate and model symmetrical transistors from other technologies.
  - Except for power FETs, commonly available transistors are symmetrical. Hence, the modeling procedure described in this thesis can be extended to other FET device technologies.
- To investigate and implement the effects of field plates on the intrinsic equivalent circuit in the symmetrical model.
  - Field plates in power FETs disturb the intrinsic symmetry. Hence an investigation and comparison between intrinsic model parameters extracted for a symmetrical device, unsymmetrical device with and without field-plates in the same technology would be interesting. This might give an insight on whether or not power FETs can be modeled using a symmetrical intrinsic core with one or more parameter corresponding to the effect of field-plates present in the device.
- To investigate for symmetry and model the extrinsic parameters of a common gate device.
  - During modeling, extrinsic parameters are commonly extracted for a device in common source configuration. However, a full three-port model of a FET would enable better prediction of measurements for cases where the source terminals of transistors are not grounded.

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# Bibliography

- [1] D. Emerson, “The work of Jagadis Chandra Bose: 100 years of millimeter-wave research,” *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 12, pp. 2267–2273, Dec 1997.
- [2] T. Sarkar and D. L. Sengupta, “An appreciation of J.C. Bose’s pioneering work in millimeter waves,” *IEEE Antennas and Propagation Magazine*, vol. 39, no. 5, pp. 55–62, Oct 1997.
- [3] P. Bondyopadhyay, “Sir J.C. Bose diode detector received Marconi’s first transatlantic wireless signal of December 1901 (the “Italian Navy Coherer” Scandal Revisited),” *Proceedings of the IEEE*, vol. 86, no. 1, pp. 259–285, Jan 1998.
- [4] —, “Guglielmo Marconi - The father of long distance radio communication - An engineer’s tribute,” in *Microwave Conference, 1995. 25th European*, vol. 2, Sept 1995, pp. 879–885.
- [5] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. DenBaars, and U. Mishra, “High breakdown GaN HEMT with overlapping gate structure,” *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 421–423, Sept 2000.
- [6] S. Karmalkar and U. K. Mishra, “Enhancement of breakdown voltage in AlGaIn/GaN high electron mobility transistors using a field plate,” *IEEE Trans. Electron. Devices*, vol. 48, no. 8, pp. 1515–1521, Aug 2001.
- [7] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, “10-W/mm AlGaIn-GaN HFET with a field modulating plate,” *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 289–291, May 2003.
- [8] A. Wakejima, K. Ota, K. Matsunaga, and M. Kuzuhara, “A GaAs-based field-modulating plate HFET with improved WCDMA peak-output-power characteristics,” *IEEE Trans. Electron. Devices*, vol. 50, no. 9, pp. 1983–1987, Sept 2003.
- [9] Y. F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, and P. Parikh, “30-W/mm GaN HEMTs by field plate optimization,” *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, March 2004.
- [10] S. Karmalkar, M. Shur, G. Simin, and M. A. Khan, “Field-plate engineering for HFETs,” *IEEE Trans. Electron. Devices*, vol. 52, no. 12, pp. 2534–2540, Dec 2005.

- [11] C.-Y. Chiang, H.-T. Hsu, and E. Y. Chang, "Effect of Field Plate on the RF Performance of AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT Devices," *Physics Procedia*, vol. 25, pp. 86 – 91, 2012, international Conference on Solid State Devices and Materials Science, April 1-2, 2012, Macao.
- [12] R. Pengelly, S. Wood, J. Milligan, S. Sheppard, and W. Pribble, "A Review of Ga<sub>N</sub> on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, June 2012.
- [13] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath, "Accurate small-signal modeling of HFET's for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 3, pp. 432–437, 1996.
- [14] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, Jul 1988.
- [15] W. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 33, no. 12, pp. 1383–1394, 1985.
- [16] I. Angelov, H. Zirath, and N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2258–2266, 1992.
- [17] W. Curtice, J. Pla, D. Bridges, T. Liang, and E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2, June 1999, pp. 419–422.
- [18] K. Yhland, N. Rorsman, M. Garcia, and H. Merkel, "A symmetrical nonlinear HFET/MESFET model suitable for intermodulation analysis of amplifiers and resistive mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 1, pp. 15–22, 2000.
- [19] C. Fager, L. Linner, and J. Pedro, "Optimal parameter extraction and uncertainty estimation in intrinsic FET small-signal models," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 12, pp. 2797–2803, 2002.
- [20] M. Wren and T. Brazil, "Enhanced prediction of pHEMT nonlinear distortion using a novel charge conservative model," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 1, 2004, pp. 31–34.
- [21] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to Ga<sub>N</sub> devices," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 11, pp. 3440–3448, Nov 2005.
- [22] W. Choi, G. Jung, J. Kim, and Y. Kwon, "Scalable Small-Signal Modeling of RF CMOS FET Based on 3-D EM-Based Extraction of Parasitic Effects and Its Application to Millimeter-Wave Amplifier Design," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3345–3353, Dec 2009.

- [23] G. Callet, J. Faraj, O. Jardel, C. Charbonniaud, J.-C. Jacquet, T. Reveyrand, E. Morvan, S. Piotrowicz, J.-P. Teyssier, and R. Quéré, “A new nonlinear HEMT model for AlGa<sub>N</sub>/Ga<sub>N</sub> switch applications,” *Int. J. Microw. Wireless Technol. (Special Issue)*, vol. 2, no. 3-4, pp. 283–291, Jul. 2010.
- [24] B. S. Mahalakshmi, S. Manikantan, P. Bhavana, M. P. Anand, R. SaiEknath, and M. N. Devi, “Small signal modelling of Ga<sub>N</sub> HEMT at 70GHz,” in *International Conference on Signal Processing and Integrated Networks (SPIN)*, Feb 2014, pp. 739–743.
- [25] S. Takatani and C.-D. Chen, “Nonlinear Steady-State III-V FET Model for Microwave Antenna Switch Applications,” *IEEE Trans. Electron. Devices*, vol. 58, no. 12, pp. 4301–4308, 2011.
- [26] W. Curtice and R. Camisa, “Self-Consistent GaAs FET Models for Amplifier Design and Device Diagnostics,” *IEEE Trans. Microw. Theory Techn.*, vol. 32, no. 12, pp. 1573–1578, Dec 1984.
- [27] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, “A new and reliable direct parasitic extraction method for MESFETs and HEMTs,” in *EuMIC*, Sept 1993, pp. 451–453.
- [28] T.-H. Chen and M. Kumar, “Novel GaAs FET modeling technique for MMICs,” in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1988. Technical Digest 1988., 10th Annual IEEE*, Nov 1988, pp. 49–52.
- [29] M. Rudolph, C. Fager, and D. Root, *Nonlinear Transistor Model Parameter Extraction Techniques*, ser. The Cambridge RF and Microwave Engineering Series. Cambridge University Press, 2011.
- [30] E. Arnold, M. Golio, M. Miller, and B. Beckwith, “Direct extraction of gaas mesfet intrinsic element and parasitic inductance values,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1990, pp. 359–362 vol.1.
- [31] F. King, P. Winson, A. Snider, L. Dunleavy, and D. Levinson, “Math methods in transistor modeling: Condition numbers for parameter extraction,” *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 9, pp. 1313–1314, Sep 1998.
- [32] C. van Niekerk and P. Meyer, “A new approach for the extraction of an fet equivalent circuit from measured s parameters,” *Microwave and Optical Technology Letters*, vol. 11, no. 5, pp. 281–284, 1996.
- [33] H. Kondoh, “An Accurate FET Modelling from Measured S-Parameters,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 1986, pp. 377–380.
- [34] A. Patterson, V. Fusco, J. J. McKeown, and J. Stewart, “A systematic optimization strategy for microwave device modelling,” *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 3, pp. 395–405, Mar 1993.
- [35] C. van Niekerk and P. Meyer, “Performance and limitations of decomposition-based parameter extraction procedures for FET small-signal models,” *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 11, pp. 1620–1627, Nov 1998.

- [36] C. van Niekerk, P. Meyer, D. M. M. P. Schreurs, and P. Winson, "A robust integrated multibias parameter-extraction method for MESFET and HEMT models," *IEEE Trans. Microw. Theory Techn.*, vol. 48, no. 5, pp. 777–786, May 2000.
- [37] K. Shirakawa, H. Oikawa, T. Shimura, Y. Kawasaki, Y. Ohashi, T. Saito, and Y. Daido, "An approach to determining an equivalent circuit for HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 3, pp. 499–503, Mar 1995.
- [38] B.-L. Ooi, M.-S. Leong, and P.-S. Kooi, "A novel approach for determining the GaAs MESFET small-signal equivalent-circuit elements," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 12, pp. 2084–2088, Dec 1997.
- [39] F. Lin and G. Kompas, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search—a new concept," *IEEE Trans. Microw. Theory Techn.*, vol. 42, no. 7, pp. 1114–1121, Jul 1994.
- [40] C. Campbell and S. Brown, "An analytic method to determine GaAs FET parasitic inductances and drain resistance under active bias conditions," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 7, pp. 1241–1247, Jul 2001.
- [41] Y. Tsvividis, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 1999.
- [42] A. Rofougaran and A. Abidi, "A table lookup FET model for accurate analog circuit simulation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 12, no. 2, pp. 324–335, Feb 1993.
- [43] I. Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman, V. Desmaris, M. Sudow, and H. Zirath, "Large-signal modelling and comparison of AlGaIn/GaN HEMTs and SiC MESFETs," in *APMC*, Dec 2006, pp. 279–282.
- [44] C. Fager, J. Pedro, N. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 12, pp. 2834–2842, Dec 2002.
- [45] A. McCamant, G. McCormack, and D. Smith, "An improved GaAs MESFET model for SPICE," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 6, pp. 822–824, Jun 1990.
- [46] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the Chalmers nonlinear HEMT and MESFET model," *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 10, pp. 1664–1674, Oct 1996.
- [47] L.-S. Liu, J.-G. Ma, and G.-I. Ng, "Electrothermal Large-Signal Model of III-V FETs Including Frequency Dispersion and Charge Conservation," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3106–3117, 2009.



- [48] K. Yuk and G. Branner, "An Empirical Large-Signal Model for SiC MESFETs With Self-Heating Thermal Model," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 11, pp. 2671–2680, Nov 2008.
- [49] W. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 5, pp. 448–456, May 1980.
- [50] J. Pedro, "A physics-based MESFET empirical model," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1994, pp. 973–976 vol.2.
- [51] D. Halchin, M. Miller, M. Golio, and S. Tehrani, "HEMT models for large signal circuit simulation," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1994, pp. 985–988 vol.2.
- [52] Agilent Technologies, "TriQuint Scalable Nonlinear GaAsFET Model." [Online]. Available: [http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/TOM\\_Model\\_\(TriQuint\\_Scalable\\_Nonlinear\\_GaAsFET\\_Model\).html](http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/TOM_Model_(TriQuint_Scalable_Nonlinear_GaAsFET_Model).html)
- [53] —, "TriQuint TOM3 Scalable Nonlinear FET Model." [Online]. Available: [http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/TOM3\\_Model\\_\(TriQuint\\_TOM3\\_Scalable\\_Nonlinear\\_FET\\_Model\).html](http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/TOM3_Model_(TriQuint_TOM3_Scalable_Nonlinear_FET_Model).html)
- [54] —, "Tajima GaAsFET Model." [Online]. Available: [http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Tajima\\_Model\\_\(Tajima\\_GaAsFET\\_Model\).html](http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Tajima_Model_(Tajima_GaAsFET_Model).html)
- [55] —, "Materka GaAsFET Model." [Online]. Available: [http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Materka\\_Model\\_\(Materka\\_GaAsFET\\_Model\).html](http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Materka_Model_(Materka_GaAsFET_Model).html)
- [56] H. Statz, P. Newman, I. Smith, R. A. Pucel, and H. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron. Devices*, vol. 34, no. 2, pp. 160–169, Feb 1987.
- [57] I. Angelov, V. Desmaris, K. Dynefors, P. A. Nilsson, N. Rorsman, and H. Zirath, "On the large-signal modelling of AlGaIn/GaN HEMTs and SiC MESFETs," in *Proceeding of the 13th Gass Symposium Paris*, Oct 2005, pp. 309–312.
- [58] Agilent Technologies, "Angelov Nonlinear GaAsFET Model." [Online]. Available: [http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Angelov\\_Model\\_\(Angelov\\_\(Chalmers\)\\_Nonlinear\\_GaAsFET\\_Model\).html](http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Angelov_Model_(Angelov_(Chalmers)_Nonlinear_GaAsFET_Model).html)
- [59] AWR Corporation, "Yhland MESFET Model." [Online]. Available: <https://awrcorp.com/download/faq/english/docs/Elements/yhland.htm>
- [60] D. Root, "Nonlinear charge modeling for FET large-signal simulation and its importance for IP3 and ACPR in communication circuits," in *IEEE Midwest Circuits Syst. Symp.*, vol. 2, 2001, pp. 768–772 vol.2.

- [61] C.-J. Wei, Y. Tkachenko, and D. Bartle, “An accurate large-signal model of GaAs MESFET which accounts for charge conservation, dispersion, and self-heating,” *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 11, pp. 1638–1644, 1998.