CHALMERS

Structured LNA Design for Next Generation Mobile Communication

Master of Science Thesis in the Master Degree Program Radio and Space Science Engineering

Sohaib Maalik

Department of Microtechnology and Nanoscience – MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
SE-41 296 Göteborg, Sweden, 2013
Report No. XXXX

Thesis Supervisors:

Herbert Zirath — Herbert.Zirath@chalmers.se
Professor, Head of Microwave Electronics Laboratory
Chalmers university of technology, Göteborg, Sweden

Rob Krosschell — Rob.Krosschell@nxp.com
Principal Design Engineer BL RFSS
NXP Semiconductors, Nijmegen, Netherlands

Examiner: Professor Herbert Zirath

Head of Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience – MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
SE-41 296 Göteborg, Sweden, 2013
Telephone: +46 (0)31 – 772 1000

Structured LNA Design for Next Generation Mobile Communication
Sohaib Maalik

Technical Report no XXXX: XX
Department of Microtechnology and Nanoscience – MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
SE-41 296 Göteborg, Sweden
Telephone: +46 (0)31 – 772 1000

Printed By Chalmers Reproservice
Göteborg, Sweden 2013

ABSTRACT

Ever increasing demands of higher data rates in wireless communication domain lead to deployment of higher frequency bands for wireless transceivers. This thesis work has focused on the low noise amplifier (LNA) design for radio base station receiver front end for next generation mobile communication long term evolution (LTE) standard, within frequency band of 3.4-3.8 GHz using NXP semiconductors 0.25 µm SiGe:C BiCMOS technology having $f_t/f_{max}$of 180/200 GHz. To fulfill the required set of LNA performance goals feedback cascode configuration has been utilized. Four variants of LNA using different combinations of LV-HV NPN transistors were designed, simulated and taped out using cadence virtuoso analog design environment (ADE) tool. The two main variants, single stage LNAs having bandwidth of 200MHz each with design frequencies of 3.5 GHz and 3.7 GHz respectively were fabricated and measured. The LNAs exhibit noise figure of under 1 dB, input/output match of better than -14/-4 dB, gain of better than 16.5 dB, input referred P1dB compression point (P1dB) of -10 dBm and input third order intercept point (IIP3) of around 0 dBm with 75 mw power consumption. The good agreement between simulated and measured results proved the viability of the design for next generation mobile communication LTE standard.

Keywords: Low Noise Amplifier, SiGe BiCMOS, LTE, Radio Base Station Receiver, Wireless Communication, Cascode.

Acknowledgments

First of all, thanks to God almighty who gave me the strength to complete this project in such a short time span. Without God's blessings it would be impossible.

I would like to pay my deepest gratitude to Mr. Rob Krösschell, my supervisor at NXP Semiconductors for giving me the chance to work on this wonderful research project. Without his guidance and continuous support throughout the work, it would not be possible to complete the project with such excellent results. I would also like to say thanks to Professor Herbert Zirath, for agreeing to be my academic supervisor for this thesis work and his continuous feedback and support whenever it was needed.

I am deeply indebted to all the people of radio frequency small signal (RFSS) LNA group at NXP Semiconductors who shared their expertise and knowledge with me. Alexander Simin for his continuous support whenever needed, Michel Groenewegen for his temporary supervision in the absence of Rob and last but not least Hassan Gul, without whom I would have never been able to see and understand the analytical side of LNAs like I do now. My discussions with him over analytical derivations gave me a new insight of looking in to things. I have learned and improved a lot because of all of you during this 10 months duration.

I dedicate this work to my beloved parents and family who are a constant pillar of support throughout my life no matter what I do.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

Abbreviation	Description
ADE	Analog Design Environment
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BL RFSS	Business Line Radio Frequency Small Signal
CB	Common Base
CE	Common Emitter
CMOS	Complementary Metal Oxide Semiconductor
DRC	Design Rule Check
DTI	Deep Trench Isolation
ESD	Electrostatic Discharge
f_t	Cut-off Frequency
f_{max}	Maximum Oscillation Frequency
FOM	Figure-Of-Merit
GSM	Global System for Mobile Communications
Gallium Arsenide	GaAs
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
H_{FE}	Small signal Forward Current gain
HV	High Voltage
IC	Integrated Circuit
IIP3	Third-order Intermodulation Intercept Point with respect to input
P1dB	P1dB compression point with respect to input
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LV	Low Voltage
LVS	Layout versus Schematic
MIM	Metal-Insulator-Metal
MOST	Metal Oxide Semiconductor Transistor
NMOS	Negative-Channel Metal Oxide Semiconductor
NPN	Negative-Positive-Negative
PNP	Positive-Negative-Positive
PMOS	Positive-Channel Metal Oxide Semiconductor
RFIC	Radio Frequency Integrated Circuit
SiGe	Silicon-Germanium
SG	Signal Generator
SA	Spectrum analyzer
STI	Shallow Trench Isolation
VGA	Variable gain amplifier
VNA	Vector Network Analyzer
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

Chapter 1

INTRODUCTION

1.1- History and Background

The ever increasing demand of higher data rates in wireless broad band communication has led to deployment of higher frequency bands in recent years. The domain of wireless communication has seen explosive growth due to rapid evolution of a series of standard generations from the traditional Global System for Mobile Communication (GSM) to 4G Long Term Evolution (LTE) standard and still growing. As a result wireless radio systems hardware needed to be upgraded so that it can support multiple standards at the same time. The first digital cellular system wireless communication standard GSM proved to be the major starting point of an incredible research and development in the area of integrated circuits (IC) electronics for wireless communication networks.

This rapid development in mobile communication field coupled with continuous progression in semiconductor technology field results in miniaturized integrated circuits development for mobile communication systems. Low noise amplifier (LNA) is one of the most critical components of any wireless communication systems. It is usually placed after the bandpass filter or often directly connected to the antenna at the receiver front end side of radio base station transceivers [1, 4]. Due to the ever increasing demands on receiver sensitivity requirements in wireless communication systems, it is essential to have a LNA with high performance in the receiver chain of wireless communication system in order to ensure reliable data communication. Excessive noise in wireless communication which is largely produced at the receiver front end electronic circuitry is an inherent problem. To overcome this problem, it is necessary to have a LNA which can amplify the weak received signal at the receiver input without adding too much of its own noise to it.

1.2- Thesis Objective

The prime focus of this thesis work was to provide a solid structured design method for development and optimization of LNA for a given set of performance parameters as shown in Table 1 for wireless communication LTE standard for radio base station receiver front end. An important aspect of the work was to estimate the parasitic effects of IC package model on circuit performance behavior at an early stage of design in order to lower the design iteration time. To achieve this objective, simulations were performed including the IC package model and results

are notified. However, LNAs were fabricated without IC package model and measurements were done on wafer probe level. Furthermore, the aim was also to find the relationships between often contradictory performance parameters requirements.

Parameter	Conditions	Min	Typical	Max	Units
Supply Current				50	mA
Supply Voltage		3		5 (± 0.5)	V
Bandwidth	3.4 – 3.8 GHz	0.2		0.4	GHz
Stability	Unconditionally Stable				
Noise Figure				1	dB
Gain		17	18	19	dB
S11,S22				-20, - 15	dB
S12				-30	dB
IIp3	Pin=-30 dBm; ΔF=1MHz	0			dBm
$P_{1\text{-}dB,input}$		-7			dBm
Gain Flatness				1	dB
Source, Load impedance			50		Ω
Ambient Temperature		-40	27	100	C°

Table 1- Low noise amplifier specifications

The work was carried out at NXP Semiconductors, business line radio frequency small signal (BL RFSS) group, Nijmegen Netherlands and included the design and measurements of two LNAs each having bandwidth of 200 MHz and covering the frequency range of 3.4 to 3.8 GHz for radio base station receiver front end using advanced high-speed 0.25 µm silicon-germanium (SiGe) bipolar complementary metal oxide semiconductor (BiCMOS) technology satisfying the given performance parameters values such as noise figure, high gain, linearity, input and output return loss as listed in Table 1.

1.3- Report Organization

In chapter 2, NXP Semiconductors advanced high-speed 0.25 µm SiGe BiCMOS technology QUBIC4Xi will be discussed in detail. The chapter starts with the explanation of basics of BiCMOS technology and its evolution over time. A brief comparison of BiCMOS with other RF semiconductor technologies is also presented. Then, NXP Semiconductors QUBIC4 platform based on Si and SiGe BiCMOS technology is introduced. The negative-channel metal oxide semiconductor (NMOS) and positive-channel metal oxide semiconductor (PMOS) devices with

vertical negative-positive-negative (NPN) transistors, mono- and poly-silicon resistors, diodes, capacitors, inductors and five layers of metal interconnect for QUBiC4Xi technology is explained. The speed of the transistors in terms of cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) are also discussed.

The theoretical and analytical basics of bipolar junction transistors (BJT) and cascode amplifier are given in detail in chapter 3. Also, basics performance parameters of a LNA are included in the chapter along with discussion on requirements, challenges and limitations in the design of a LNA specifically for radio base station receiver front end which is the intended application of this project work.

Chapter 4 belongs to the detailed design procedure and simulation results of LNA with feedback cascode configuration on schematic level. In state of the art LNAs, the cascode configuration where a common emitter (CE) stage is used to drive a common base (CB) stage is commonly used. The LNA is designed, simulated and taped out using Cadence virtuoso analog design environment (ADE) tool [5]. The schematic simulation results have shown that the LNA fulfills most of the performance parameters which have been set at the start of project. The comparison of LNAs designed in this work with other commercially available LNAs for same frequency band is also included in the chapter.

In chapter 5, floorplanning and layout procedure of the hierarchical LNA circuit is discussed in detail. The simulated results of LNA with extracted versions of core and coils sections with and without the inclusion of IC package model are described in detail.

The detailed description of lab environment and measurement setup used to measure the fabricated LNAs are part of Chapter 6. The measurements are performed on wafer level and therefore measurement results and their comparison with extracted simulation results of chapter 5 without IC package model are included in this chapter.

The report is concluded with some suggestions for future work in the final chapter 7.

Chapter 2

QUBiC4Xi SiGe BiCMOS Process

2.1- Evolution of SiGe BiCMOS Technology

SiGe BiCMOS technology has seen phenomenal advancement over the last decade from its humble beginning in the late 1980s [6]. It is an evolved technology which integrates high performance heterojunction bipolar transistors (HBT) with state-of-the-art complementary metal oxide semiconductor (CMOS) transistors in the most appropriate way to take full advantage of characteristics of each type of transistor both at circuit and system levels. For RF communication circuits and applications SiGe BiCMOS HBT exhibit same level of performance with much less power consumption as compared to CMOS only transistors. Even though CMOS technology provide good performance in several figure of merits such as f_t, f_{max} and linearity but high level of integration and superior noise performance of SiGe BiCMOS for RF design makes it an ideal choice for designers. A comparison of CMOS technology with conventional Si BJT and BiCMOS HBT in terms of important figure of merits is listed in Table 2.

Parameter	CMOS	Si BJT	SiGe BJT
f_t	High	High	High
f_{max}	High	High	High
Linearity	Best	Good	Better
1/f noise	Poor	Good	Good
Broadband noise	Poor	Good	Good
Transconductance	Poor	Good	Good

Table 2- Comparison of CMOS with conventional and SiGe BJTs [7]

2.2- GaAs VS SiGe BiCMOS for RF Applications

In semiconductor industry, debate about technology superiority between GaAs and silicon (especially SiGe BiCMOS) for radio frequency integrated circuit (RFIC) applications is going on for a long period of time now. Over the years Gallium Arsenide (GaAs) has struggled to establish itself as the lone RF semiconductor technology mainly due to its high cost of substrate materials and relatively small scale of manufacturing operations as compared to its silicon competitors [8]. Even then GaAs is widely used in RF front end of wireless systems particularly in power amplifier domain due to its outstanding RF characteristics [9, 10]. However, SiGe BiCMOS technology has emerged quite strongly over the past several years as a strong

competitor to GaAs. The main advantages it possesses over its counterpart are high performance, high level of integration and low cost attributes for large volumes of production [8]. High level of integration here refers to the fact that it is possible to place Analog/RF, mixed signals and digital building blocks in a circuit on a single chip hence giving rise to miniaturization of electronics hardware. Furthermore, SiGe BiCMOS technology suits more for large scale production due to its large base of silicon foundries as compared to much smaller GaAs foundry [11]. Thus, SiGe BiCMOS technology has replaced GaAs in radio transceivers of wireless systems particularly on the receiver end [12, 13]. It does not mean that GaAs is going to phase out anytime soon compared to SiGe BiCMOS, however the technology choice strongly depends on the type of application which is being targeted. For mass market products such as wireless local area network (WLAN), wireless personal area network (WPAN) and radio base transceiver stations circuits SiGe BiCMOS technology is more suitable due to its low cost, superior performance and high level of integration. Whereas, for low volume products such as space instruments, radio meters and certain radar systems GaAs is preferred choice due to its power handling capability, noise performance and high quality passive circuitry [11]. This project is focused on the low noise amplifier design for radio base station receiver front end application and it is authors' strong belief that SiGe BiCMOS technology will continue to outperform its GaAs counterpart in this domain for the foreseeable future.

2.3- QUBiC4 Platform

QUBiC4Xi process family is part of QUBiC4 platform developed at NXP Semiconductors based on advanced high-speed BiCMOS technology. QUBiC4 platform offers 0.25 µm NMOS and PMOS devices, high speed, high voltage (HV) and low voltage (LV) vertical NPN transistors, lateral and vertical PNP transistors, thin film, mono- and poly-silicon resistors, diodes, capacitors including a high density metal-insulator-metal (MIM) capacitor and five layers of metal interconnect. QUBiC4 is electrically compatible with the NXP C050 CMOS process, with 0.25 µm gate length, 5.3 nm gate oxide, shallow trench isolation (STI) and deep trench isolation (DTI) [14]. The QUBiC4 platform consist of two more processes families namely QUBiC4+ and QUBiC4X apart from QUBiC4Xi.

The transistor cut-off frequency f_t and maximum frequency of oscillation f_{max} are traditional figure-of-merits (FOM) for any technology process. The cut-off frequency f_t is the frequency at which the current gain becomes equal to unity whereas at maximum oscillation frequency f_{max} power gain becomes equal to unity. In general, f_{max} is always equal to or greater than the f_t. It is extremely difficult to measure cut-off frequency f_t due to the high frequencies involved and it is generally obtained through interpolation. The FOM f_t and f_{max} are usually used to compare transistors based on different technology processes.

The QUBiC4 platform has evolved over the time and different application specific family processes are developed while improving their performance and speed. The NPN transistor

performance for family processes QUBiC4+, QUBiC4X and QUBiC4Xi belonging to QUBiC4 platform in terms of speed i.e. cut-off frequency f_t versus the collector-emitter breakdown voltage BV_{CEO} is presented in Figure 1.

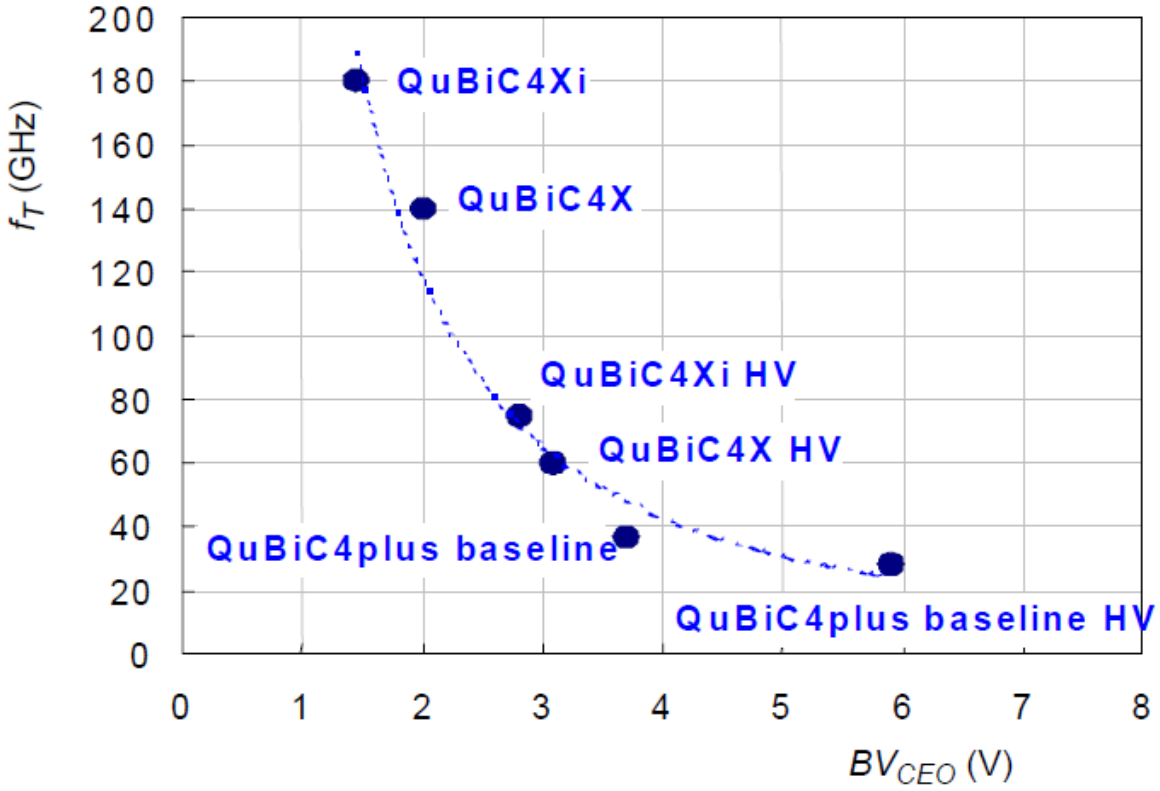


Figure 1- NPN transistor performance in QUBiC4 platform in terms of f_T VS BV_{CEO} [14]

The different family processes belonging to QUBiC4 platform differ in terms of construction, performance and application voltage of NPN transistor [14]. The first family process QUBiC4+ in QUBiC4 platform uses a double poly silicon NPN transistor and has a peak f_t of 37 GHz and a maximum supply voltage of 3V [14]. In second QUBiC4X family process SiGe is added to form HBT which resulted in increase of peak f_t from 37 GHz to 137 GHz as compared to QUBiC4+ but at the cost of reduced voltage supporting capability of around 2V. Increase in peak f_t has resulted in boost of RF performance. The latest QUBiC4Xi family process has even further boosted the RF performance with achieved peak f_t of 180 GHz with SiGe NPN transistor at a cost of further reduction in voltage supporting capability of around 1.5V. The evolution of technology in QUBiC4 platform for the three family processes in terms of FOM such as peak f_t, f_{max}, small signal forward current gain h_{FE} and voltage handling capabilities for collector-emitter and collector-base junctions are summarized in Table 3.

	QUBiC4+		QUBiC4X		QUBiC4Xi		Unit
Technology Type	Si BT	Si HV BT	SiGe:C HBT	SiGe:C HV HBT	SiGe:C HBT	SiGe:C HV HBT	
Peak f_t	37	28	110	60	180	90	GHz
f_{max}	90	70	140	120	200	200	GHz
I_c at Peak f_T	0.75	0.5	3.5	0.8	8	2	$mA/\mu m^2$
h_{FE}	150	140	320	320	1800	1500	
BV_{CEO} Min.	3.3	5.5	1.5	3.1	1.0	2.0	V
Typ.	3.8	5.9	2.0	3.5	1.5	2.5	
BV_{CBO} Min.	11	12.5	3.5	10	2.5	9.5	V
Typ.	16	18	5.5	13.4	4.5	11.5	

Table 3- NXP Semiconductor QUBiC4 platform NPN LV and HV transistor comparison in different family processes [14]

It can be seen from the table that in each family process of QUBiC4 platform transistors are available in both LV and HV versions. In LV transistors higher peak f_t is achieved at the cost of lower voltage handling capability of the transistors. The selection of technology process and transistor type solely depends on the type of application for which it is being used. For the present work, the intended application was the design of a LNA for radio base station receiver front end, for which QUBiC4Xi family process has been used due to its high speed and superior performance compared to other two family processes of QUBiC4 platform.

2.3.1- QUBiC4Xi Technology

QUBiC4Xi is state of the art technology developed using 0.25 µm SiGe BiCMOS process. It has been optimized to provide high cut-off frequency f_t of 180 GHz for high speed analog and mixed signal applications. The library based on QUBiC4Xi technology contains a wide variety of metal oxide semiconductor transistors (MOST), bipolar transistors in both HV and LV versions to facilitate a wide application range. It also contains different types of active and passive circuitry components such as diodes, electrostatic discharge diodes (ESD), capacitors, inductors, transmission lines, resistors etc. Table 4 lists the main devices used in this work and their brief description which are part of the large QUBiC4Xi library. Five different bipolar junction transistors (BJT) are available in QUBiC4Xi library in both LV and HV versions. The transistors differ from each other in terms of their layout style as a result of which they differ in terms of performance from each other. Out of these five transistors bnyhv transistor has been selected to use for the LNA design in this project. The main reason for its selection over other transistors was that it has been developed and optimized for high speed and low noise applications [15].

Category	Device ID	Description
Bipolar	bna	BNA NPN Transistor
	bnahv	BNA NPN HV Transistor
	bnc	BNC NPN Transistor
	bnchv	BNC HV NPN Transistor
	bnd	BND NPN Transistor
	bndhv	BND HV NPN Transistor
	bny	BNY NPN Transistor
	bnyhv	BNY HV NPN Transistor
	Pa	PA NPN Transistor
	pahv	PNA HV NPN Transistor
Diode	AntProtN	n+/pwell Antenna Protection Diode
	AntProtP	P+/nwell Antenna Protection Diode
	diodeDBV	ESD diode
Capacitor	capMIM	MIM Capacitor
	capPSPSB	POLY-PSB Capacitor
Resistor	res3N	Low Rsheet n+ ACTIVE Resistor
	resPZ	p- Polysilicon Resistor
Inductor	indSeS	Shielded single ended inductor
Transmission	Tline_se_b	Bended Single-ended transmission line
	Tline_se_s	Straight single-ended transmission line
Seal ring	sealringPSB	Seal ring with PSB

Table 4- QUBiC4Xi supported devices used in the project [16]

A bnyhv transistor consists of multiple dotted emitters which results in enhanced current spreading in collector and improved connection with the base [15]. Due to this structure, both f_t and f_{max} improves significantly and so as the minimum noise figure. Furthermore, bnyhv transistor handles the large current densities close to peak f_t in the best possible way [15]. The naming convention of bnyhv transistor is as follows: BNYHV04X10E5 refers to a bnyhv transistor with 5 emitters, each having width of 0.4 µm and length of 1.0 µm [15]. The default values and possible range for variation of emitter length, width and number of emitters for bhyhv transistor are summarized in Table 5.

Description	Range	Default
Emitter width	0.2-2.3 µm	0.4 µm
Emitter length	1-20.7 µm	1.3 µm
Number of Emitters	2-20	4
Number of Emitters in Parallel	1	1

Table 5- bnyhv NPN transistor parameters description in QUBiC4Xi [15]

A typical top view of bnyhv transistor with 4 emitter dots and 3 base contact fingers and corresponding detailed cross sectional schematic view is shown in Figures 2 and 3 respectively.

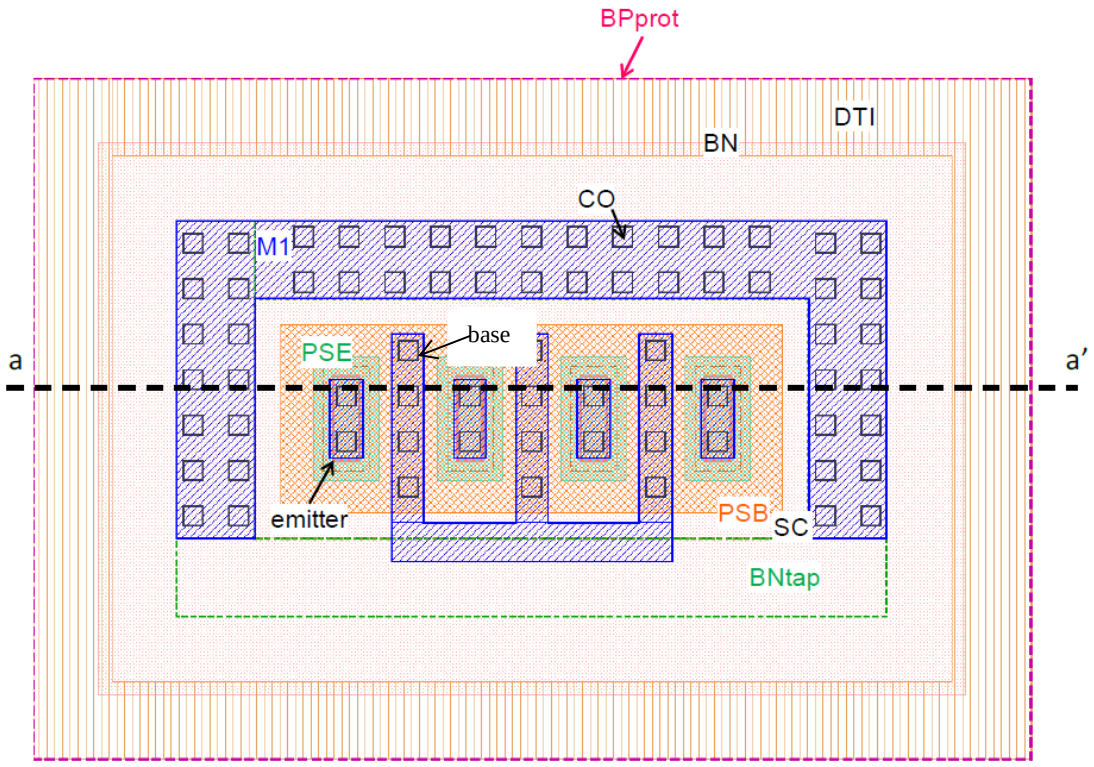


Figure 2- Top view of bnyhv transistor in QUBiC4Xi technology with size BNYHV04X10E4 [15]

It can be seen clearly that multiple emitter dots are separated by base contact fingers. Active area isolation is obtained by STI, which also reduces NPN base-collector capacitance improving $f_{max.}$ Also, deep DTI is used to isolate collector terminals and to decrease the collector-substrate capacitance.

Picture not included in academic version of report due to NXP rules

Figure 3- Schematic cross-sectional view of bnyhv transistor in QUBiC4Xi technology with size BNYHV04X10E4 [15]

In passive circuitry components available in QUBiC4Xi library, capMIM and resPZ have been used wherever high value capacitors and resistors were needed respectively. For low capacitance and resistance capPSPSB and res3N have been used respectively. Inductor indSeS has been used in the design since it has shield protection which prevents any parasitic coupling with the substrate. Moreover, this inductor type provides the additional flexibility of changing the inductor input and output nodes with a 90° step size. For electrostatic discharge (ESD) protection diodeDBV have been used whereas diode AntProtN was used for protection against plasma induced charging which can arise during the manufacturing process.

Chapter 3

Low Noise Amplifier and BJT Theory

3.1- Low Noise Amplifier Performance parameters

The low noise amplifier always operates in class A, which conducts over the whole of the input signal cycle [17]. In wireless communication systems receiver sensitivity is set by the lowest level of detectable signal at the receiver end. LNA plays an important role in enhancing the quality of receiver chain in wireless communication systems as its main function is to amplify the received signal with addition of as little noise as possible. Therefore, a LNA design should be exhaustively thought through according to the system requirements based on figure of merits such as stability, low noise figure, good gain and excellent matching performance. Often these contradictory performance parameters in the design of a LNA pose quite challenging tasks for the designer. This section, briefly describe these performance parameters since understanding their role and relation with each other in LNA performance is vital. For in depth study of these parameters any standard RF electronics book can be consulted.

3.1.1- Stability

The stability is the most critical parameter to determine the correct functioning of any amplifier. An amplifier should be unconditionally stable regardless of its frequency of operation. An amplifier is generally represented as a two port network and to design an unconditionally stable LNA is the goal of the designer. The unconditional stability refers to the fact that for any passive load impedance presented at the input or output of LNA, there will be no oscillations. There are various ways to check the stability of LNA. The most commonly used method is to calculate Rollett stability factor (K- factor) using the S-parameters of the amplifier.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad \textbf{(3.1)}$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$

When $K > 1$ and $|\Delta| < 1$, the LNA is said to be unconditionally stable. This is also called small signal stability test which is valid for a specific bias and frequency point. To ensure the stability of amplifier over a wide range of frequency points, it is essential to perform the K-factor test for a frequency sweep. Also, feedback loop analysis if they are part of the LNA circuit should be performed to accurately characterize the stability behavior of LNA. The large signal

stability test, by performing transient analysis on a step input signal with maximum amplitude is also a way to determine the stability of amplifier.

3.1.2- S-Parameters

The important performance parameters of a LNA such as input S_{11} and output S_{22} reflection coefficients, gain S_{21} and reverse isolation S_{12} are calculated using S-parameters of the two port network. Input and output reflection coefficients indicate how well the LNA is matched to source and load impedance respectively; usually; 50Ω at the design frequency point or frequency band of interest. There are various definitions available for gain of LNA in the literature such as transducer power gain, available power gain and operating power gain. However, transducer power gain is the most accurate way of expressing gain since it takes in to account the power available from the source and power delivered to the load. However, the scalar logarithmic (dB) expression for gain S_{21} which is used for gain calculation in this report is given by

$$g = 20\log|S_{21}|\ dB \quad \textbf{(3.2)}$$

Reverse isolation S_{12} is a measure of how well input and output ports of LNA are isolated from each other.

3.1.3- Noise Figure

Noise figure (F) is a measure of degradation in the signal-to-noise ratio between the input and output ports of the LNA. It is usually expressed as

$$F = \frac{S_i/N_i}{S_o/N_o} \quad \textbf{(3.3)}$$

Where S_i and N_i are the input signal and noise powers, and S_o and N_o are the output signal and noise powers respectively. It is obvious from Equation (3.3) that noise figure will be higher for a noisy two port network since output signal-to-noise ratio will be reduced due to more increase in output noise power compared to output signal power. Therefore, for LNA it is desirable to have as low noise figure as possible. In case the LNA consist of multiple stages then the noise figure is calculated using Friis equation

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots \quad \textbf{(3.4)}$$

Where F_{total} is the overall noise figure of the multi-stage LNA whereas F_1, F_2, F_3, G_1, $G_2$and G_3 are noise figures and gains for first, second and third stages respectively. It is clear from Equation (3.4) that noise figure of first stage dominates the noise performance of multi-stage LNA. Therefore, in design of multi-stage LNA, first stage is optimized for lowest possible noise figure to achieve excellent noise figure performance for overall system.

3.1.4- Linearity

In LNA design, figure of merits most commonly used to characterize linearity are P1-dB compression point and third order intercept point (IP3) either with respect to input or output. Ideally output power of an amplifier increases linearly with increase in its input power level but in reality after a certain input power level the output power starts getting saturated due to the non-linearities, especially the third order, of the amplifier. The point where output power level of

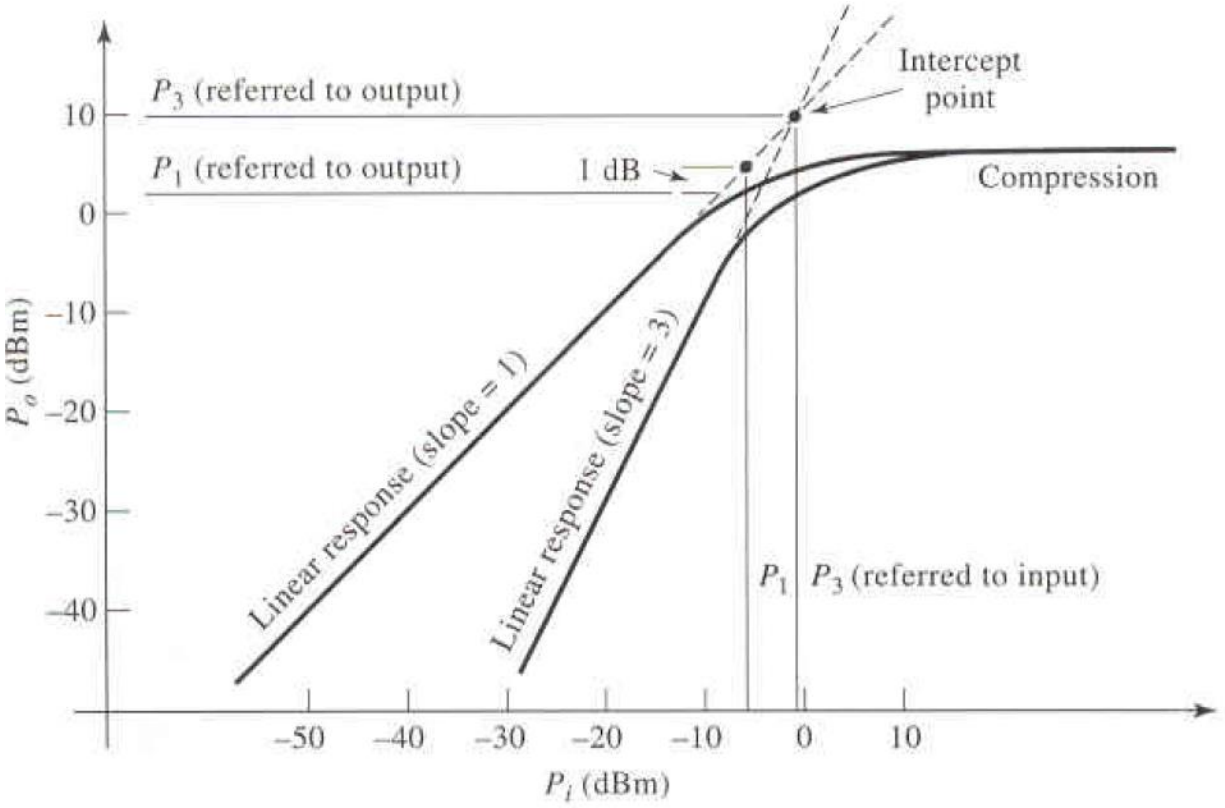


Figure 4- P1-dB compression point and third order intercept point (IP3) of an amplifier [18]

amplifier gets 1dB below from its ideal output power characteristics is said to be P1-dB compression point. The dynamic range in which a low noise amplifier works as desired is defined from the noise floor of the system to the third order intercept point with respect to input or output where intermodulation distortion becomes unacceptable.

3.1.5- Trade-offs among LNA Performance parameters

It is impossible to design a low noise amplifier with maximum performances in all of the performance parameters described above. The parameters such as stability, noise figure, gain, linearity, input and output matching are equally important in the design of a LNA but they are interdependent and do not always work in favor of each other. Therefore, it is the designer task to very carefully take into consideration the unavoidable trade-offs among these parameters keeping in mind the specific application for which LNA design is being intended.

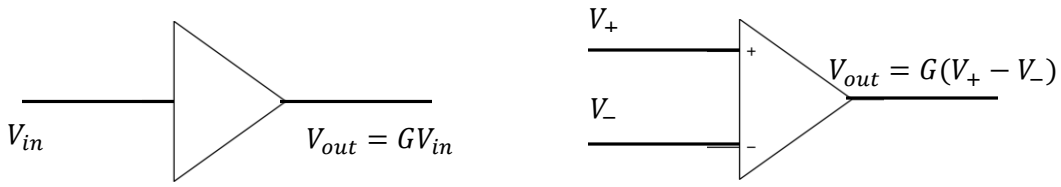
It is always a priority to have an unconditionally stable LNA. To achieve this different strategies are used resulting in compromise on performance of one or more other parameters. For example, to ensure stability resistive loading at output of LNA is commonly used which results in lower gain and lower P1-dB compression points. Similarly, input return loss of the LNA is most often sacrificed to achieve lowest possible noise figure since both are not achievable at the same time. Moreover, output matching network of LNA is usually designed to achieve maximum gain by means of conjugate matching. But with increasing demands on high linearity of LNAs, the trade-off between excellent IP3 and gain must be considered.

3.2- Low Noise Amplifier Topologies

A lot of work has been done in Low noise amplifier design domain over the years. Consequently amplifiers based on different topologies have been designed and implemented. This discussion will take a brief overview of different design topologies of low noise amplifiers presented in literature and describe their advantages and shortcomings in one way or another. Even though it is a tough task to generalize the categorization of low noise amplifier topologies, here I have divided the existent LNA topologies in to three main categories of single-transistor based, multi-stage and cascode-based topologies. These topologies are used both in single-ended and differential LNA designs. Therefore, first brief description about single-ended and differential low noise amplifiers is presented followed by the discussion about various topologies. Finally, wideband and multi-band LNAs are also discussed since they have gained a lot of importance in recent years due to evolution of multi-standard mobile and data communication frequency bands.

3.2.1- Single-ended and Differential LNAs

A block diagram of single-ended and differential amplifiers is presented in Figure 5. As the name



(a)- Single-ended amplifier **(b)- Differential amplifier**

Figure 5- Block diagram representation of Single-ended and Differential LNA

suggests, a single-ended amplifier has only one input and output signal level and all voltages are taken into account with reference to the common ground. A single-ended amplifier simply takes an input signal and delivers it at the output by simply amplifying it with gain of the amplifier. On the other hand, ideally a differential amplifier has two input signal voltage levels and instead of

amplifying the particular voltages it amplifies the difference between them. There are two types of gain associated with a differential LNA, differential-mode gain and common-mode gain. It is always desired to minimize the common-mode gain while maximizing the differential-mode gain. The figure of merit to determine the performance of a differential amplifier is known as common-mode rejection ratio, which is simply the ratio between differential-mode gain and the common-mode gain. In an ideal or perfectly symmetrical differential amplifier, common-mode gain is zero and as a result common-mode rejection ratio is infinite. Differential low noise amplifiers are generally realized by duplicating the single-ended LNA circuit; as a result they can be analyzed and explained using their single-ended counterparts as a starting point [19, 20].

3.2.2- Single-transistor based LNAs

There are numerous low noise amplifier topologies which use single transistor. The salient featu-

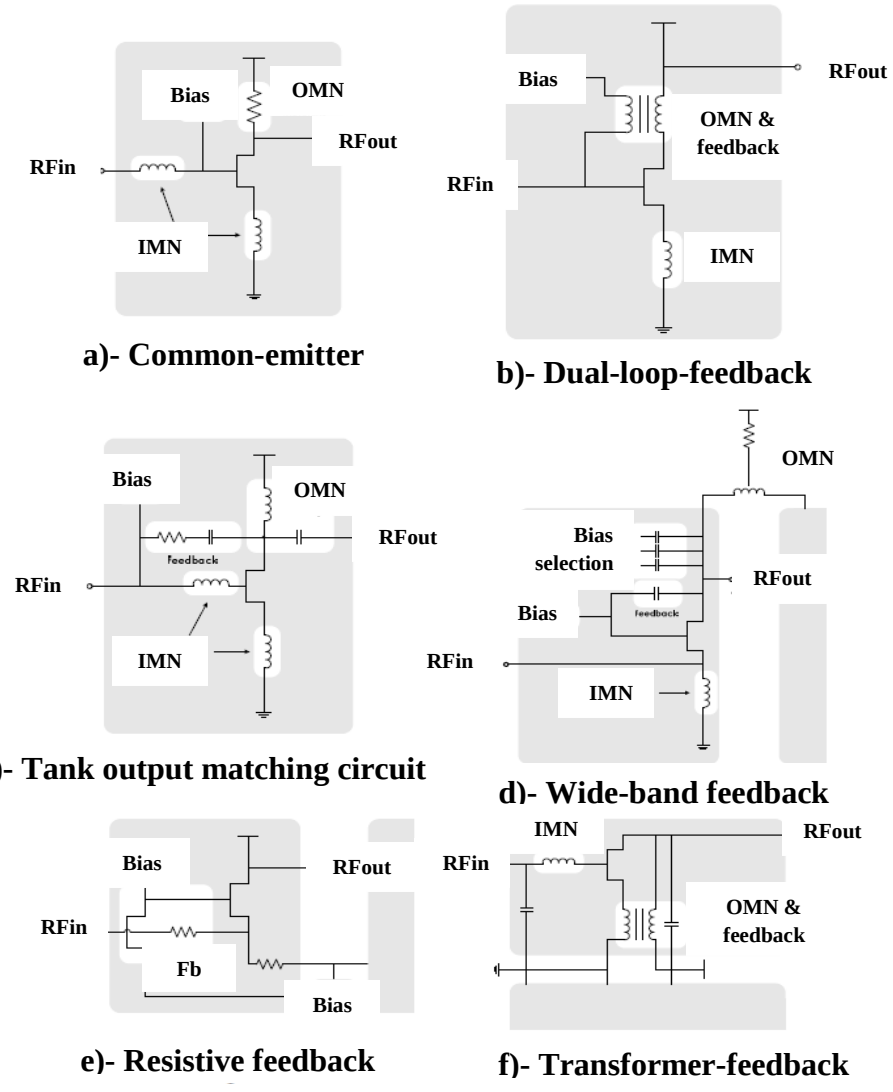


Figure 6- Single-transistor LNAs [21]

-res of these amplifiers include smaller chip area, low power consumption and supply voltages [21]. Due to a single transistor involved noise analyses of such amplifiers are much simpler but at the same time reverse isolation is very low. Moreover, since input and output impedance matching networks are interdependent, it is quite difficult to obtain a solution where both lowest noise figure at input and optimum power transfer at output of the amplifier can be obtained [21]. Figure 6 show various configurations of most commonly used single-transistor based LNAs.

3.2.3- Multi-stage LNAs

It is a common practice to design multi-stage LNAs in order to fulfill ever increasing demand of high gain. The simplest realization of a multi-stage LNA can be that of a common-emitter input stage cascaded with one or more similar stages. Apart from having good input and output impedance matching networks in a multi-stage LNA, it is of extreme importance to have properly designed inter-stage matching networks as well in order to ensure an unconditionally stable amplifier [22]. To achieve a good multi-stage LNA design, it is essential to design the first stage having minimum noise figure and usage of low-pass network at the output stage to achieve improved linearity. Moreover, usage of bandpass networks at the input and inter-stages provide good matching and gain forming which enhances the stability of such amplifiers [23]. The drawbacks of such designs are that they occupy large chip area and consume high power since each transistor in the design has to be biased independently.

3.2.4- Cascode-based LNAs

The cascode topology is the most widely used configuration today in LNA design and is regarded as the state of the art topology. It overcomes the short comings of single transistor based LNAs since the presence of cascode transistor renders the input and output matching networks independent of each other [21]. Furthermore, cascode transistor suppresses miller capacitance which results in improved reverse isolation and cascode topology also provides higher gain due to higher output impedance compared to single-transistor based configurations. The most basic cascode topology is the common source/emitter amplifier designed using the inductor degeneration. Different variations of cascode topology which have been used over the years are presented in Figure 7. When a low supply voltage and advantages of cascode topology are needed, folded cascode configuration is used since in it both transistors are biased with supply voltage needed to bias one transistor only [21]. Resistive feed-back cascode LNAs are used to achieve wideband input matching at the expense of small degradation in noise figure of the amplifier.

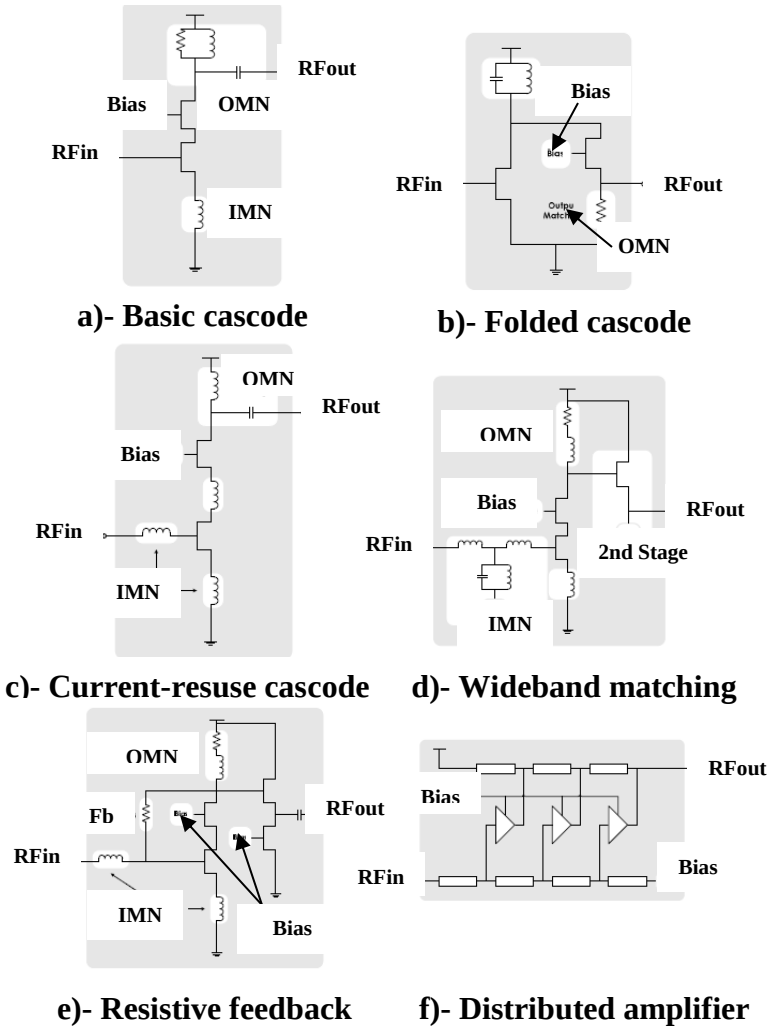


Figure 7- Cascode-based LNAs [21]

3.2.5- Wideband and Multi-band LNAs

As compared to narrowband LNAs, wideband LNAs should have a wide impedance bandwidth and flat gain across the whole bandwidth of operation. To obtain wideband impedance matching various techniques are used especially resistive feedback etc. as already been described above. Moreover, distributed elements such as transmission lines are used for matching over a wide frequency range instead of lumped components. Multi-band LNAs are constructed using several narrow band LNAs in parallel, each treating a separate narrow frequency band [21].

3.2.6- Comparative Analysis

The selection of a particular topology for LNA design hugely depends on the application for which it is being intended. The advantages and drawbacks of different LNA configurations are described above. Single-transistor based LNAs have the edge in terms of occupying lesser chip area and low supply voltage consumption over multi-stage or cascode based counterparts. On the

other hand, even though multi-stage LNAs occupy much larger chip area and need extra care for inter-stage matching networks design to guarantee stability, they have the edge in terms of providing high gain and linearity. Cascode-based LNAs offer the benefits of physical compactness along with other performance parameters improvement at the expense of high supply voltage for proper biasing of both transistors. The present work is aimed at designing LNA for base stations where high power consumption is not a strict limiting factor. Therefore, cascode topology is being preferred over other configurations for this work since it seems to be the best basic configuration for a good trade-off between low noise, high gain and stability [24].

3.3- Bipolar Junction transistor

The current controlled BJT remains the analog designer's transistor of choice over the years, due to its robustness, high voltage gain and ease of biasing. The bipolar transistor, both NPN and PNP type, is a three terminal device consisting of base, emitter and collector terminals as shown in Figure 8.

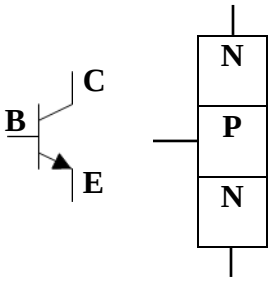


Figure 8- NPN bipolar transistor representation

The simplified small signal equivalent representation for NPN BJT using its simplified equivalent hybrid π-model indicating important small signal parameters are represented in Figure 9.

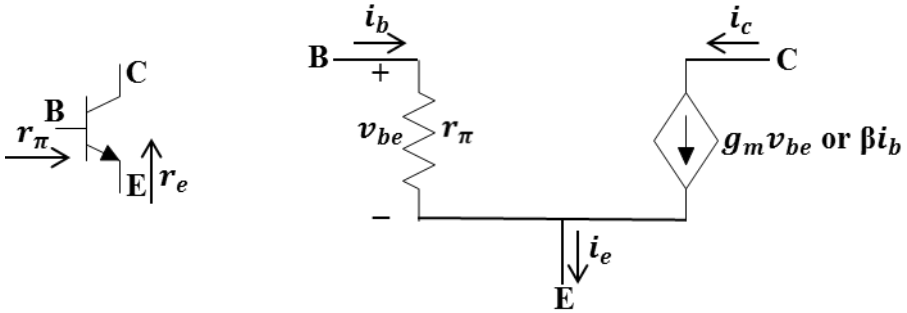


Figure 9- NPN BJT and simplified equivalent small signal hybrid π-model

The transconductance g_m depends linearly on bias current $I_c$and is given in Equation (3.5) as

$$g_m = \frac{I_c}{V_T} \quad \textbf{(3.5)}$$

Where $V_T = KT/q$ is thermal voltage having a value of 25mV at room temperature of 25 Cº. The small signal input and output resistances between base and emitter, as seen looking into the base r_π for CE configuration and emitter r_e for CB configuration are given using Equations (3.6) and (3.7).

$$r_\pi = \frac{\beta}{g_m} \quad \textbf{(3.6)}$$

$$r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m} \quad \textbf{(3.7)}$$

Where β and α are current gains for common emitter and common base BJT configurations respectively. The $r_\pi$and $r_e$have the following relation

$$r_\pi = (\beta + 1)r_e \quad \textbf{(3.8)}$$

3.3.1- Small signal model of cascode amplifier[1]

The cascode configuration combines the advantages of common emitter and common base configurations. The basic idea behind cascode amplifier is to overcome the limitation of the miller effect due to intrinsic collector-base capacitance in CE stage by adding a CB stage at its output. This way high input resistance and large transconductance of a CE amplifier is combined with current-buffering property and superior high-frequency response of common-base circuit reducing the miller effect [25]. The general cascode topology with emitter degeneration and its simplified small signal equivalent circuit are shown in Figures 10 and 11 respectively.

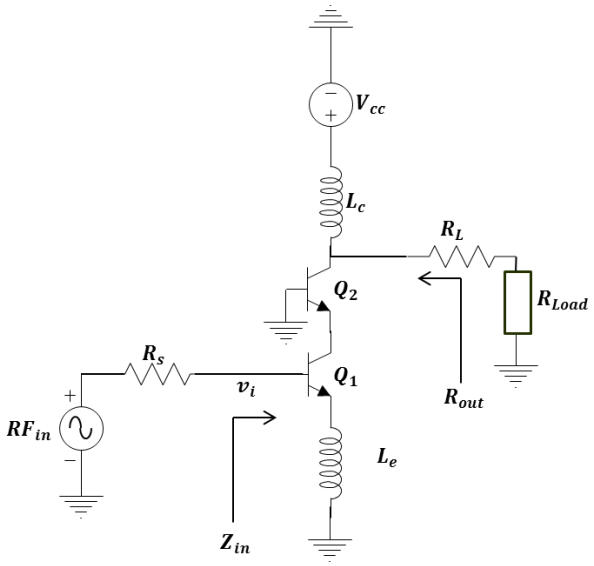


Figure 10- Cascode amplifier with emitter degeneration without biasing

[1] The derivations of analytical expressions used in this section are included in APPENDIX A.

A simplified qualitative description of the cascode amplifier operation can be explained using Figure 11. The CE stage transistor (Q_1) in response to the input signal v_i conducts a current signal $g_m v_{be}$ in its collector terminal which gets fed to the emitter terminal of CB transistor (Q_2). The CB transistor passes the signal to its collector terminal where it is supplied to a load resistance R_L at a very high output resistance R_{out}. Thus CB transistor (Q_2) acts as a buffer, presenting a low input impedance to the collector of CE transistor (Q_1) and providing a high resistance at amplifier output.

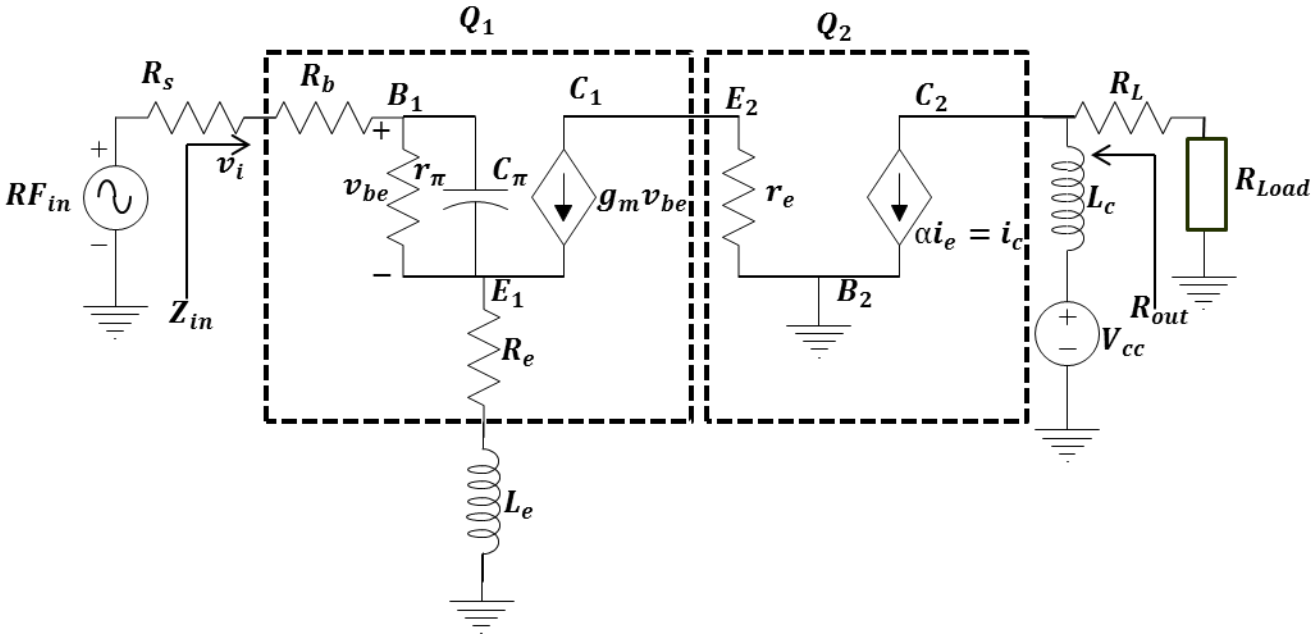


Figure 11- Simplified small signal hybrid π-model of Cascode amplifier with emitter degeneration

The CE stage in cascode amplifier is extremely important since the noise figure of this stage determines the overall noise figure of the amplifier. Furthermore, input impedance Z_{in} determines the input matching network. The input impedance Z_{in} seen looking in to the base of CE stage is given by Equation (3.9)

$$Z_{in} = \underbrace{R_b + R_e + \omega_T L_e}_{Real\ Part} + \underbrace{j\omega L_e + \frac{1}{j\omega C_\pi / 1 + g_m R_e}}_{Imaginary\ Part} \qquad \textbf{(3.9)}$$

Ideally for a source impedance of 50Ω, imaginary part gets canceled out and real part yields

$$L_e = \frac{50 - (R_b + R_e)}{\omega_T} \qquad \textbf{(3.10)}$$

The noise figure small signal analysis results in the expression given in Equation (3.11). It can be seen clearly that noise figure mainly depends on dominant contributions from base resistance R_b and collector current I_c along with inevitable internal resistance of the input source. Theoretically, base resistance R_b can be indefinitely reduced with increase in the emitter area by means of using multi-emitter transistors or placing a large number of transistors in parallel. In

practice, this also increases the base-collector capacitance C_{bc} resulting in limitation of lowest noise figure value that can be achieved this way.

$$F = \underbrace{1}_{Source\ term} + \underbrace{\frac{R_b + R_e}{R_s}}_{Base\ thermal\ noise} + \underbrace{\frac{1}{2\beta r_e}\frac{[R_s + R_b + R_e]^2}{R_s}}_{Base\ shot\ noise} + \underbrace{\frac{r_e}{2R_s}\left[\frac{\beta r_e + R_s + R_b + R_e}{\beta r_e}\right]^2}_{Collector\ shot\ noice} \quad \textbf{(3.11)}$$

Chapter 4

Low Noise Amplifier Design

4.1- Competitor Analysis

The LNA design specifications for the present work are given in chapter 1, Table 1. In order to align the specifications with current market trends, a thorough research has been done and NXP competitor's organizations products available for same frequency band have been studied to collect data. Table 6 summarizes the comparison among different commercially available products mentioning the technology used as well as performance parameters. It is clear that the specifications set for present work are very well aligned with current market trends.

Competitor Name	**Product name**	**Technology**	**Band-width (GHz)**	**V_{supply} (V)**	**I_{supply} (mA)**	**S11 /S22 (dB)**	**S12 /S21 (dB)**	**NF (dB)**	**IIP3 (dBm)**	**P1dB (dBm)**
NXP Semiconductors	Current project	0.25 µm BICMOS SiGe	3.4-3.8	3-5	50	-20 /-20	-30 /17	1	0	-7
Triquint	TQP3M 9041	Dual E-pHEMT	2.3-4	4.35	57	-	-/18	0.77	20	5.5
Mini-circuits	TAMP-362GLN +(2 stage)	E-pHEMT	3.3-3.6	5	100-140	-/-18	-42 /18	0.9-1.2	11	-4
Hittite	HMC491LP3	GaAS MMIC	3.4-3.8	3	9	-17 /-7	-33 /15	2-2.2	3	-7
	HMC593LP3	GaAS pHEMT MMIC	3.3-3.8	5	40	-23 /-13	-36 /19	1.2-1.6	10	-2
	HMC716LP3E	GaAs pHEMT MMIC	3.1-3.9	5	65	-28 /-16	-30 /18	1-1.3	15	0

Table 6- Competitor analysis summary of LNA for LTE standard

It is of significant importance to mention that there are no strict restrictions on supply current I_s and supply voltage V_s for present work. The supply voltage up to 5 V and if needed supply current of 50 mA or even more can be used to achieve the specified performance goals. However, the circuit was designed with intention of least power consumption possible to achieve the specified targets.

4.2- Circuit Design

As mentioned in detail in chapter 3 the cascode topology was selected for LNA design for the present work. This section describes the detailed procedure of circuit design starting from the transistor type selection for CE and CB stages in cascode configuration, their optimized sizes and bias point selection. Furthermore, detailed overview of hierarchical setup of the circuit is described before presenting the schematic simulation results, with and without package IC model, in the final section of the chapter.

4.2.1- Transistor selection

The 0.25 µm SiGe BiCMOS based QUBiC4Xi library contain five different NPN BJTs in both LV and HV version as listed in chapter 2, Table 4. As stated in chapter 2, transistors differ in terms of their layout style and hence performance. A simple test bench using ideal components was setup in Cadence SpectreRF for analysis of appropriate transistor type selection for both CB and CE stages. To have fair comparison between different transistor types, current density has kept constant while bias current is varied to compare the performance in terms of noise figure, gain and linearity. After extensive analysis, bnyhv transistor has been selected for both CE and CB stages due to its comparable performance in terms of noise figure, superior gain and high voltage handling capability compared to other transistors combinations. The bny low voltage transistor showed the best performance in terms of noise figure and should be selected for CE stage. However, bnyhv transistor was preferred instead due to the fact that bny HV-HV combination will provide high robustness against high supply voltage but at the cost of very minimal degradation in noise figure.

4.2.2- Transistor size and bias Point Selection

After selection of bnyhv transistors for both CE and CB stages, another test bench has been setup to investigate and select the optimum sizes for both transistors. The simple cascode circuit consisting of ideal components used for this purpose is shown in Figure 12. The passive components values of circuit were obtained using same set of equations (4.1-4.5) as discussed later in section 4.2.4. Analysis has been done keeping in mind the fact that for CE stage optimum noise figure performance is desired whereas for CB stage high gain and linearity performance is needed. The bias point of 4 V in the collector and 1.75 V in the base which falls within active region is selected for CB stage after plotting I-V characteristics curves. Throughout the analysis same biasing is used and only bias current has been varied from 3 to 50 mA. The transistors size

has been varied by changing the transistor length mainly while ensuring a constant current density for all bias currents. The simulated data was extracted from cadence to Microsoft Excel and were used to plot noise figure, gain, IIP3 and P1dB compression points versus emitter area as shown in Figure 13. It is clear from the plots that noise figure of 0.68 dB, 17 dB gain and

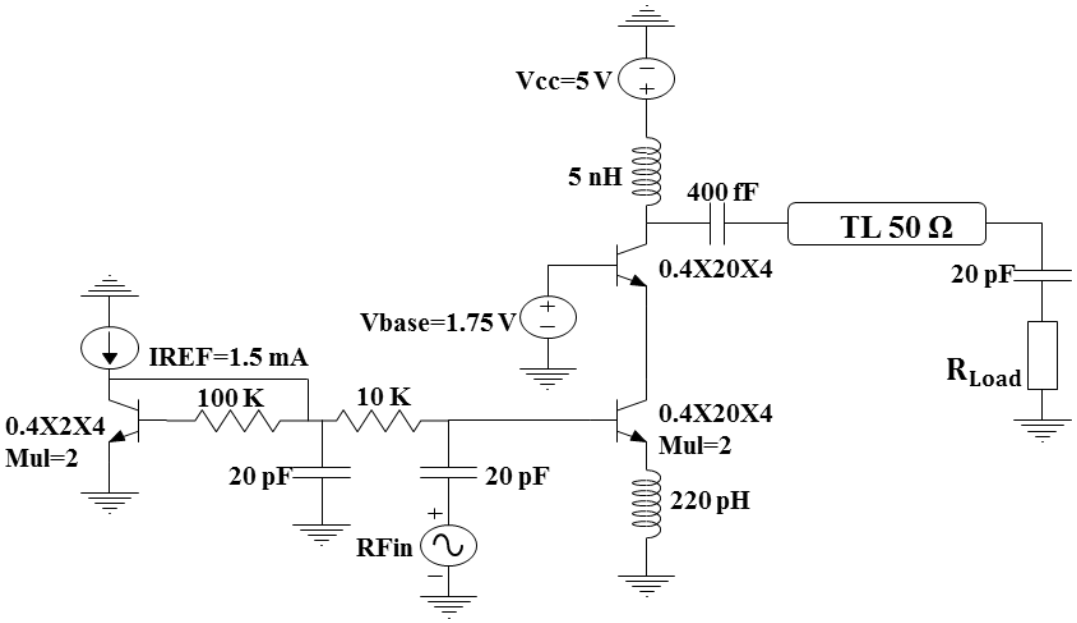


Figure 12- Cascode Circuit setup for optimum transistor size selection

-6 dBm P1dB compression point can be achieved with 2 transistors each of size $\underbrace{0.4 \times 20 \times 4}_{w \times L \times E}$ in parallel for CE stage and 1 transistor of same size for CB stage using 12 mA of collector current I_c. It is important to note that required target of 0 dBm for IIP3 is achieved with 40 mA of current, but instead of going for higher current to achieve improved IIP3 i stick with 12 mA of collector current. To meet IIP3 performance goal with 12 mA of current, a modification to the circuit represented in Figure 12 was implemented which will be discussed later in section 4.2.4. The noise figure of 0.5 dB can be achieved if a single transistor is used in CE stage instead of two in parallel but that gives slightly poor input match. Since we have very challenging input match goal, therefore, instead of selecting transistor size for optimum noise figure, a compromise has been made on noise figure to achieve excellent input match while still satisfying the noise figure requirement which was to stay below 1 dB. The available gain and noise circles along with input match curve are shown in Smith chart of Figure 14. It is obvious that 0.6 dB noise figure circle falls inside the 20 dB gain circle along with input match of 50 Ω at center frequency of 3.6 GHz. Thus, even though the circuit setup was ideal but nevertheless it gave a good starting point with optimum transistor sizes, supply voltage of 4 V and bias current of 12 mA. If needed, there is an option of increase in bias current and supply voltage since there is no strict restriction on power consumption. Furthermore, from Table 6 it is clear that using supply voltage of 5 V and higher bias currents in the range of 40-80 mA is norm in commercial products for base

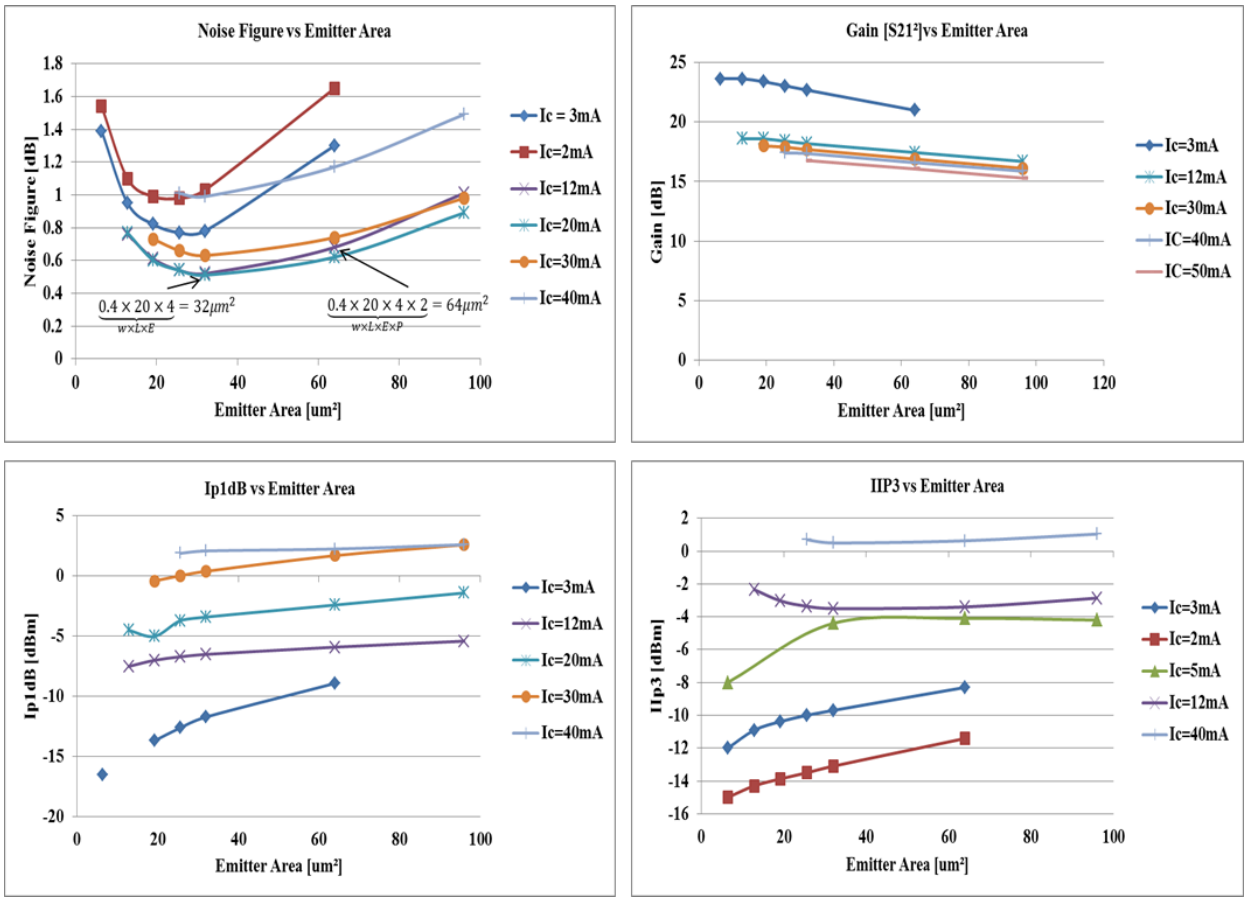


Figure 13- Optimum transistor size analysis results

stations LNAs.

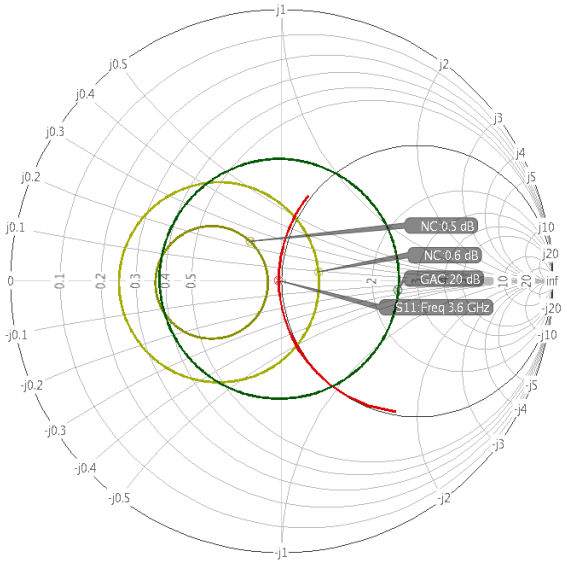


Figure 14- Available gain and Noise figure circles along with S11 curve at 3.6 GHz center frequency

4.2.3- Hierarchical setup of circuit

The complete packaged IC model used by LNA group at NXP semiconductors consist of two dies and occupies an area of 8x8 mm^2 as shown in Figure 15. The complete IC contains LNA in one die and VGA in the other. As this work is focused only on the design of LNA, therefore VGA and second die area of IC are out of the scope of this report.

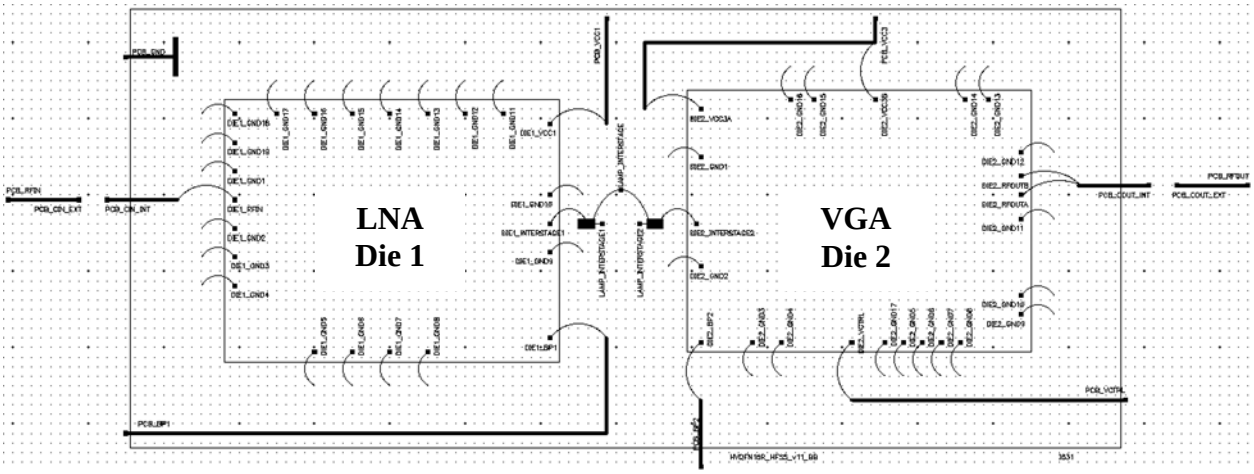


Figure 15- Complete packaged model IC having an area of 8x8 mm^2

The LNA circuit consists of three hierarchical levels starting from level which consist of core, coils, pad ring sections and going upwards till the test bench level where connections of RF input and output sources, DC and RF ground domains, external biasing including voltage supply and current sources coming out of top level of hierarchy are defined. This hierarchical setup is shown in Figure 16 in block level diagram for an intuitive understanding.

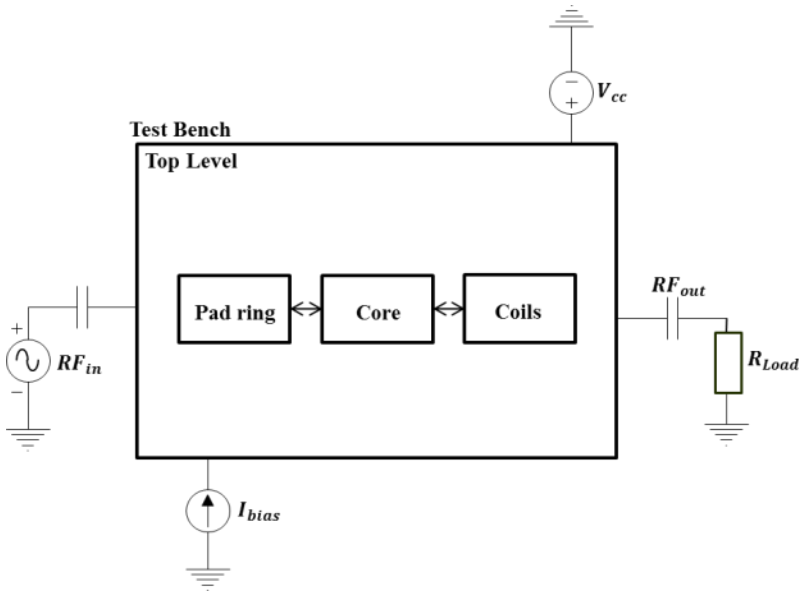


Figure 16- Block level diagram of hierarchical setup of LNA circuit

The pad ring section contains all the bond pads which are equally spaced with distance of 125 µm. Apart from having ESD protection using diodeDBV at RF input and output; two crowbars ESDCLAMP5V5 present in this section provide extra protection against large ESD events.

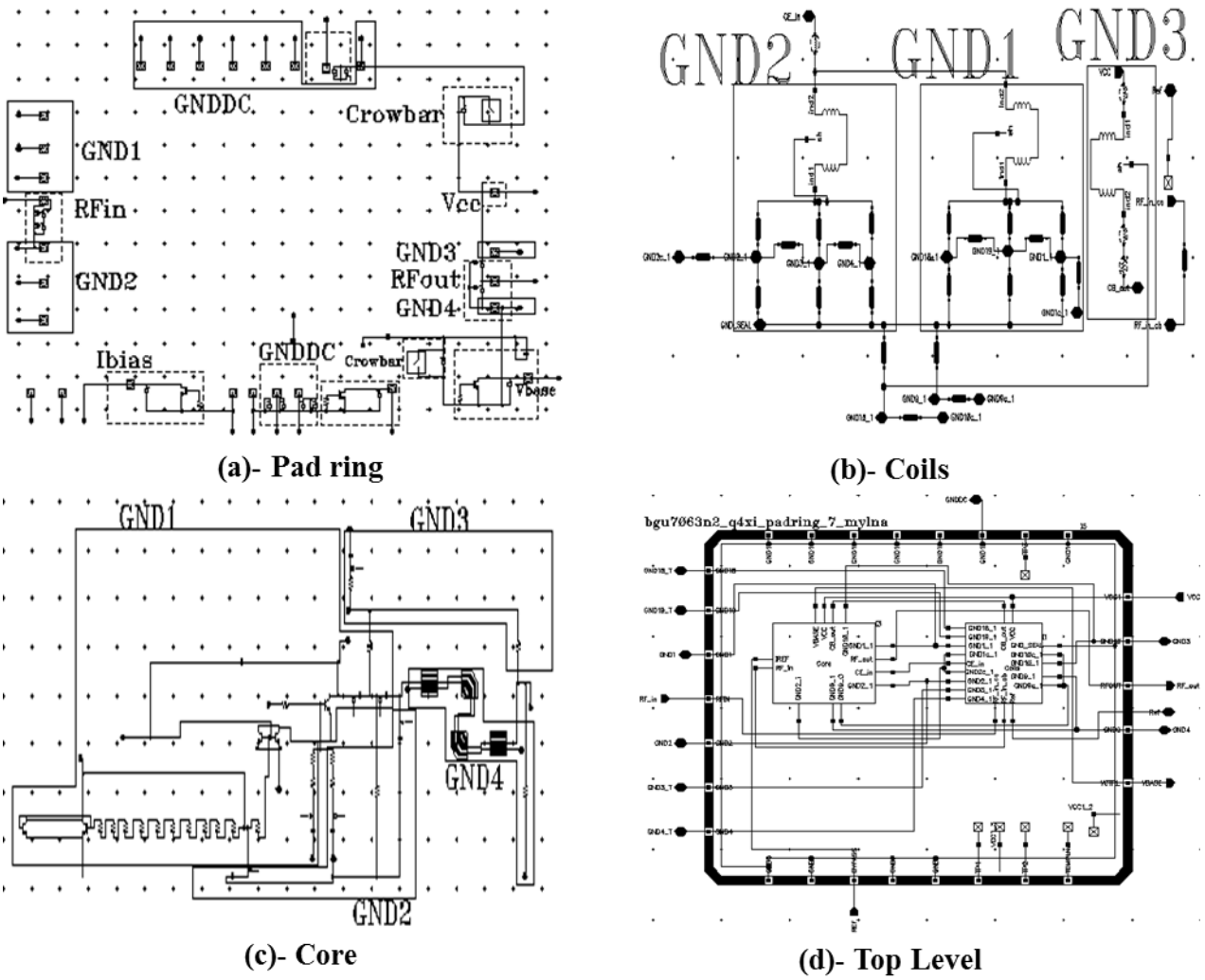


Figure 17- Hierarchical levels of LNA circuit

These are labeled in the Figure 17 (a) along with pads defined for RF, DC, ground paths and external biasing connections for current and voltage sources. In same level of hierarchy, there exist the coil and core sections as well. The coil section shown in Figure 17 (b) contains all the important RF paths and coils which can impact the RF performance of the LNA. By taking advantage of this hierarchical setup, the coil section has been simulated separately in Agilent ADS momentum to exactly characterize the behavior of coils, RF paths and their impact on LNA performance. The core section presented in Figure 17 (c), as the name suggests, consist of the main part of LNA circuit including transistors, all routing paths from input port to the output port and input, output matching networks. It also contains the current mirror setup which is used for current biasing with 1:10 ratio due to the protection it provides against temperature variations

and varying β of BJTs even of the same batch. The top level of hierarchy as shown in figure 17 (d), consist of interconnections between core, coil and pad ring sections. Furthermore, it acts as an interface between lower hierarchical level and test bench to provide connections with the DC and RF sources.

4.2.4- Design Approach

The following set of equations is used to get good starting values for CE stage of cascode amplifier circuit components. The transistor sizes as decided in section 4.2.2 for CE and CB stages are used.

$$f_T = \frac{g_m}{2\pi C_{be}} \quad \textbf{(4.1)}$$

$$g_m = \frac{I_c}{V_T} \quad with\ V_T = 25\ mV\ at\ 25C° \quad \textbf{(4.2)}$$

$$L_e = \frac{50\Omega - (R_b + R_e)}{\omega_T} \quad \textbf{(4.3)}$$

$$L_b = \frac{1}{4\pi^2 freq^2 C_{be}} - L_e \quad \textbf{(4.4)}$$

$$IIP3[dBm] = -11 + 30\log_{10}(1 + g_m Z_e) \quad \textbf{(4.5)}$$

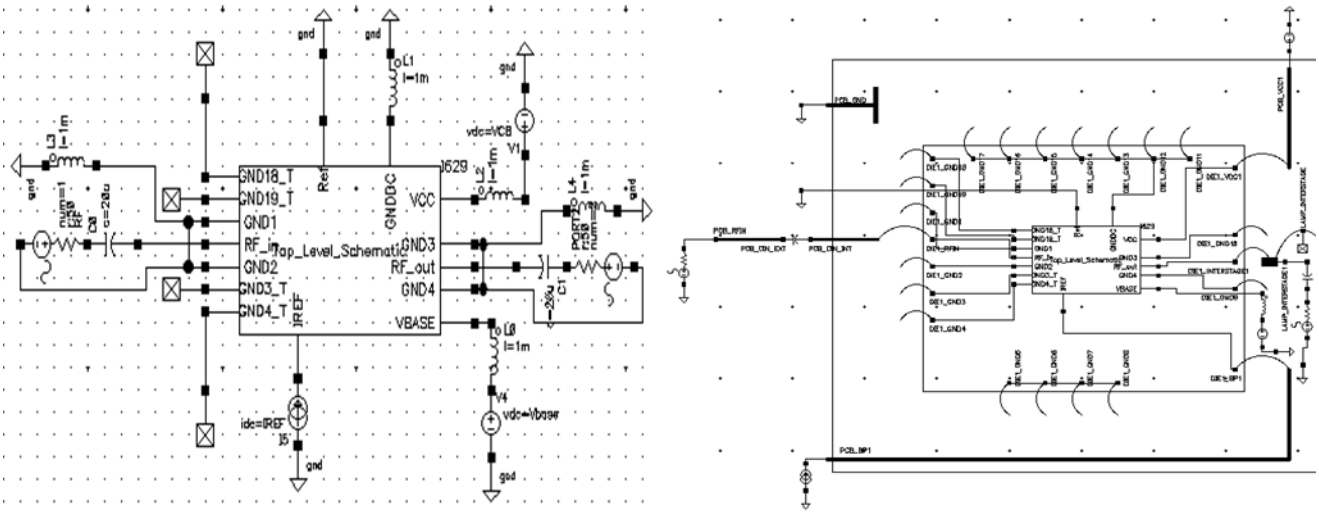
The intrinsic parameters $R_b,\ R_e$ and $C_{be}$are obtained from cadence. The input matching network consists of 1nH inductor and since bond wire of package IC model is modeled to be around 1nH it is utilized for input match. Output matching is achieved using a capacitor in series at the output port. After starting with values obtained from set of Equation (4.1-4.5) ideal components have been replaced with real QUBic4Xi components as discussed and listed in Table 4, chapter 2. To achieve IIP3 target of 0 dBm with 12 mA of collector current, a feedback capacitor from CB collector terminal to the CE base terminal has been implemented which improved the linearity of the amplifier as well as the input return loss while compromising on the reverse isolation. After performing several iterations according to the iterative procedure described in [26], key component parameter values, influencing the performance behavior of LNA, have been identified and optimized.

4.3- Simulation Results[2]

Four variants of LNA based on feedback cascode topology covering the frequency band of 3.4-3.8 GHz using different combinations of LV-HV bny transistors have been designed. The LNA variants were designed and optimized including the package IC model and its parasitics. To compare the simulated results with measurements which were performed on wafer level instead of packaged device, simulation results without package IC model has also been obtained but

[2] The compliance table listing results at all three temperatures of 27 Cº,-40 Cº and 100 Cº for two main variants are included in APPENDIX B.

since ultimately LNA has to be packaged along with VGA no optimization or tuning has been performed to improve the results in this case. The test bench setups for LNA circuit with and without package IC model are shown in Figure 18.



(a)- Without package IC model **(b)- With Package IC model**

Figure 18- Test bench setup of LNA circuit

The simulation results at room temperature of 27 C° of two main variants having 200 MHz bandwidth consisting of bny HV-HV combination with center frequencies of 3.5 and 3.7 GHz has been presented here. The results at all three temperatures of 27 Cº, -40 Cº and 100 Cº are compared and included in the form of compliance table in APPENDIX B. The supply voltage of 5 V and collector current of 15 mA have been selected finally after initial simulations with 4V and 12 mA to get maximum voltage swing at output collector terminal of CB stage. Furthermore, it is important to remember that since external biasing is used in the design; we have freedom of increasing the bias current if needed. APPENDIX B also includes the schematic simulation results of comparatively broadband HV-HV variant covering entire frequency band of interest from 3.4 to 3.8 GHz. For this variant, the specified performance parameters have been met using 32 mA of bias current which is more than twice the current consumed in 200 MHz bandwidth variants. It shows that bandwidth improvement comes at a cost of higher power consumption for this topology.

4.3.1- 3.5 GHz LNA

After optimization of design for 3.5 GHz center frequency results are evaluated for both with and without package IC model cases. Figure 19 shows the stability simulation results for both cases. It can be seen that for without package IC model case, LNA is not unconditionally stable since K-factor goes below 1 in 21-47 GHz frequency range. But with package IC model, simulation results clearly show that LNA is unconditionally stable for all frequencies.

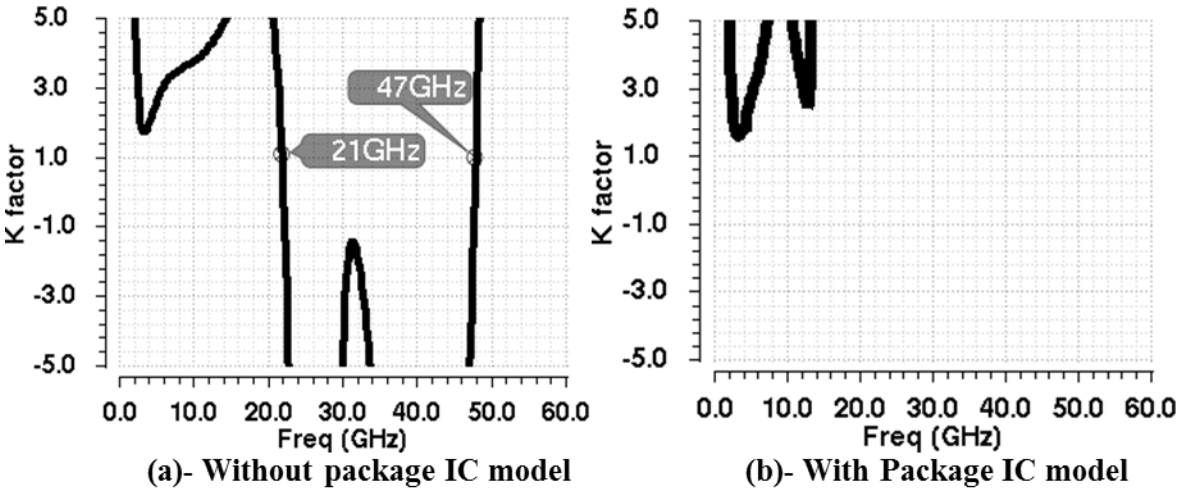


Figure 19- Stability simulation results on wafer and packaged device level

The noise figure simulation results are presented in Figure 20. It can be seen that noise figure is well below 1dB for both cases which was the required target. There is an increase in noise figure of under 0.1 dB for package model case compared to without the package IC model.

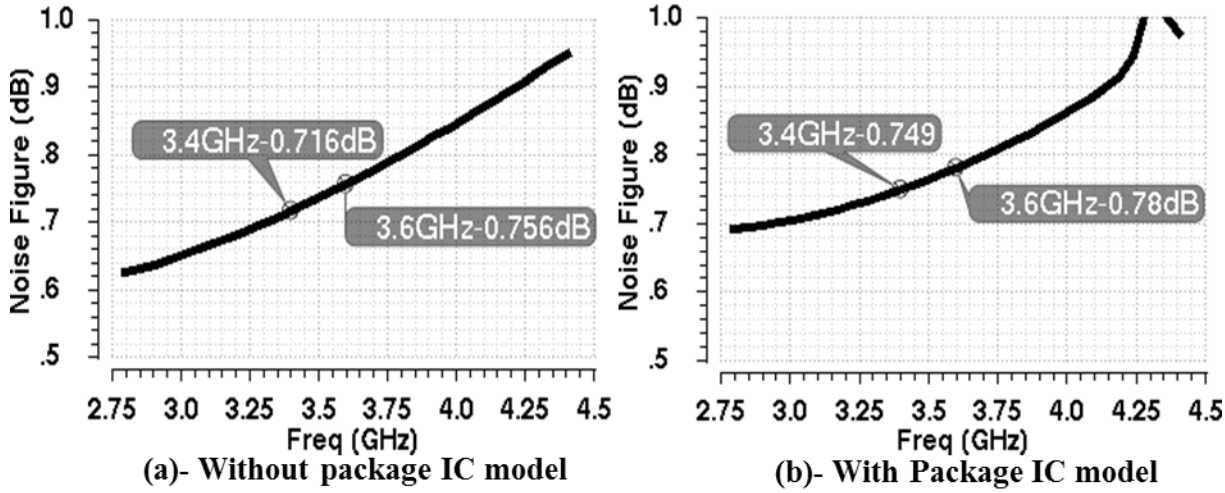
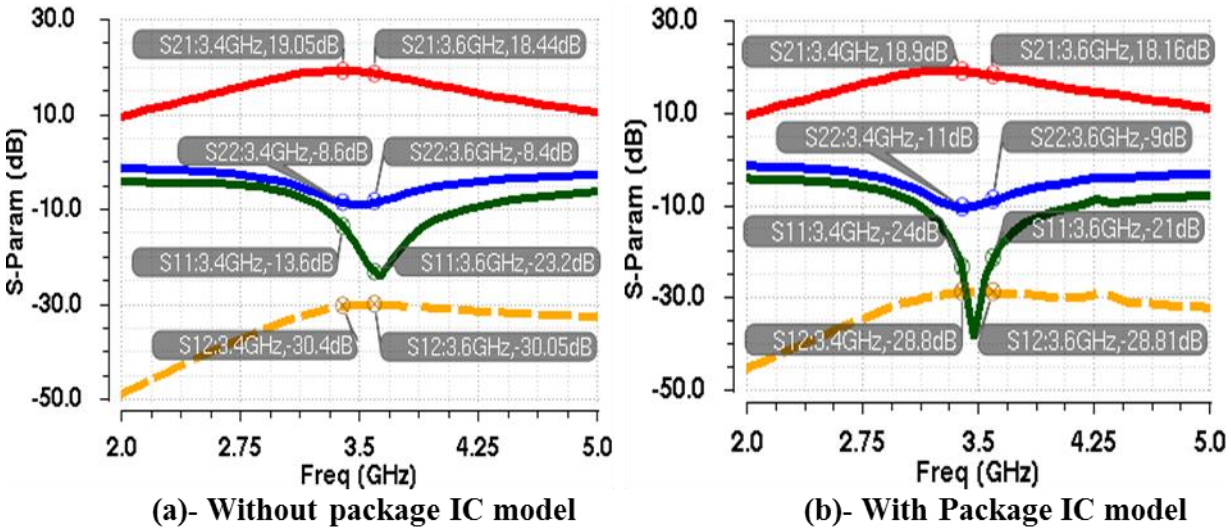


Figure 20- Noise figure simulation results at 27 C° room temperature

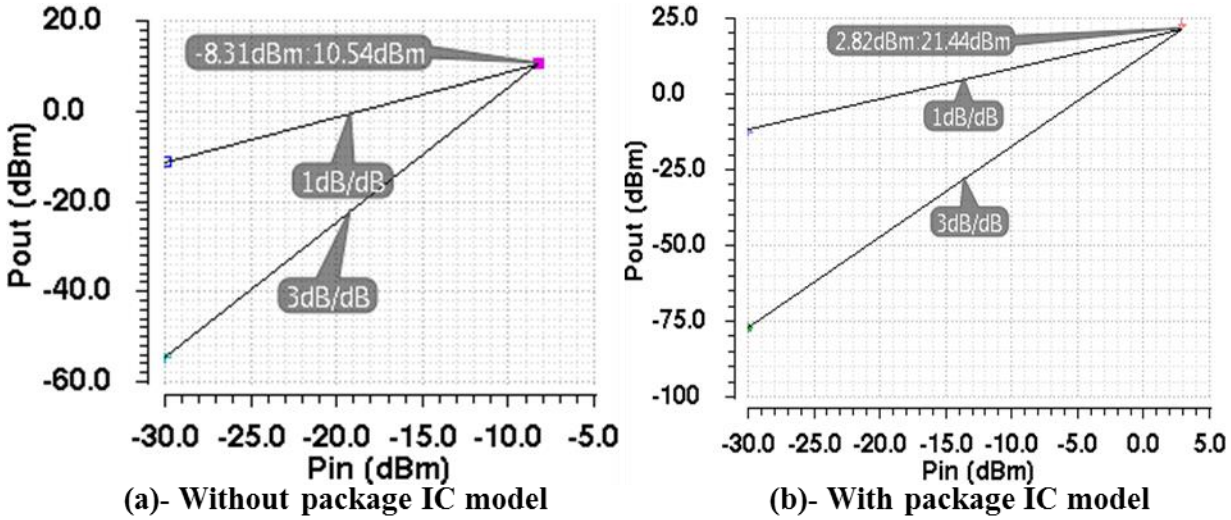
Figure 21 include the S-parameters results of the LNA. It can be seen that for IC package model case S11 of better than -20 dB, S21 of better than 18 dB with gain flatness of less than 1 dB and reverse isolation of around 29 dB is achieved. S22 varies from -11 to -9 dB over the frequency band of interest which is much higher than the desired -15 dB, but since LNA will be packaged together with VGA as explained in section 4.2.3, S22 results are accepted as it is and much effort was not spent on improving it further. The reason for this is that output port of LNA will eventually see impedance other than 50 Ω which is the case here.



(a)- Without package IC model (b)- With Package IC model

Figure 21- S-parameters simulation results at 27 C° room temperature

The linearity of the LNA is checked by performing third-order intermodulation distortion test



(a)- Without package IC model (b)- With package IC model

Figure 22- IIP3 point simulation results at 3.5 GHz and 27 C° room temperature

using two tones around 3.5 GHz separated by 1 MHz from each other at input power of -30 dBm. The ac analysis based "rapid IP3" test is chosen for IIP3 calculation because of its fast convergence and approximately accurate results compared to "qpss analysis" which gives more accurate results but at the cost of very long convergence time. The resulting IIP3 point graph is shown in Figure 22. Furthermore, Figure 23 shows the P1dB compression point result with reference to the input. It can be seen that IIP3 of 2.82 dBm which is better than the required target of 0 dBm and P1dB of around -10 dBm is achieved.

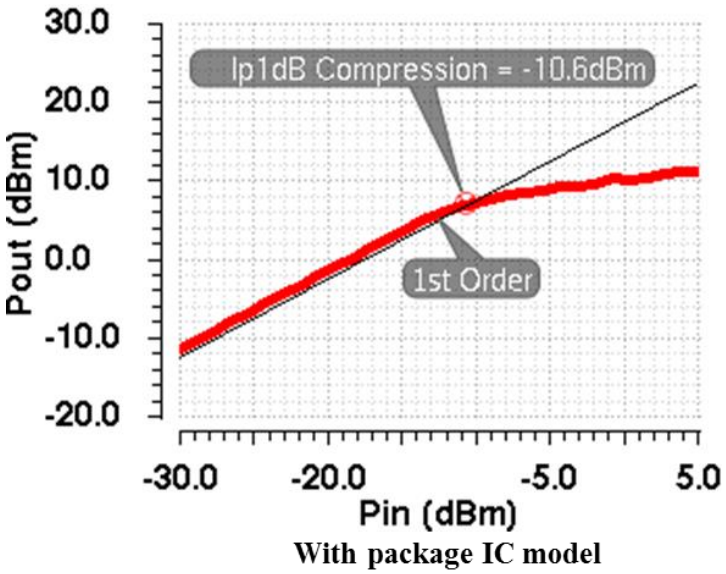


Figure 23- P1dB compression point simulation results at 3.5 GHz and 27 C° room temperature

4.3.2- 3.7 GHz LNA

The schematic simulated results for 3.7 GHz center frequency LNA with and without package IC model are presented in this section. The K-factor simulation results show similar behavior in this

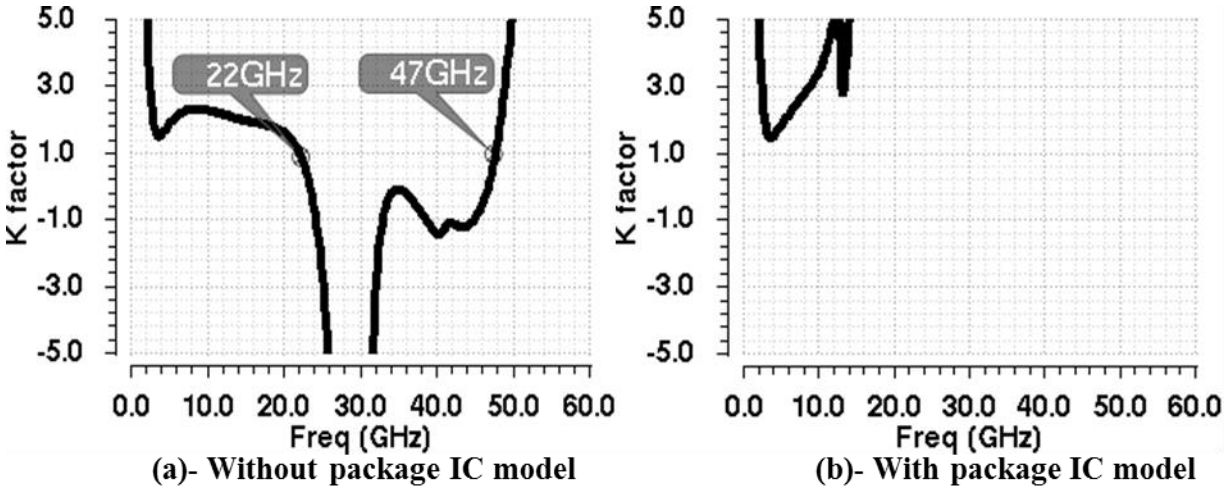


Figure 24- Stability simulation results on wafer and packaged device level

case as for 3.5 GHz LNA. It can be seen from Figure 24 that with package IC model K-factor simulations show unconditional stability whereas K-factor goes below 1 for frequency range of 22-47 GHz for without package IC model case.

Noise figure stays below 1 dB for both cases as presented in Figure 25. At highest frequency of 3.8 GHz, noise figure reaches 0.82 dB of value for simulations including package IC model.

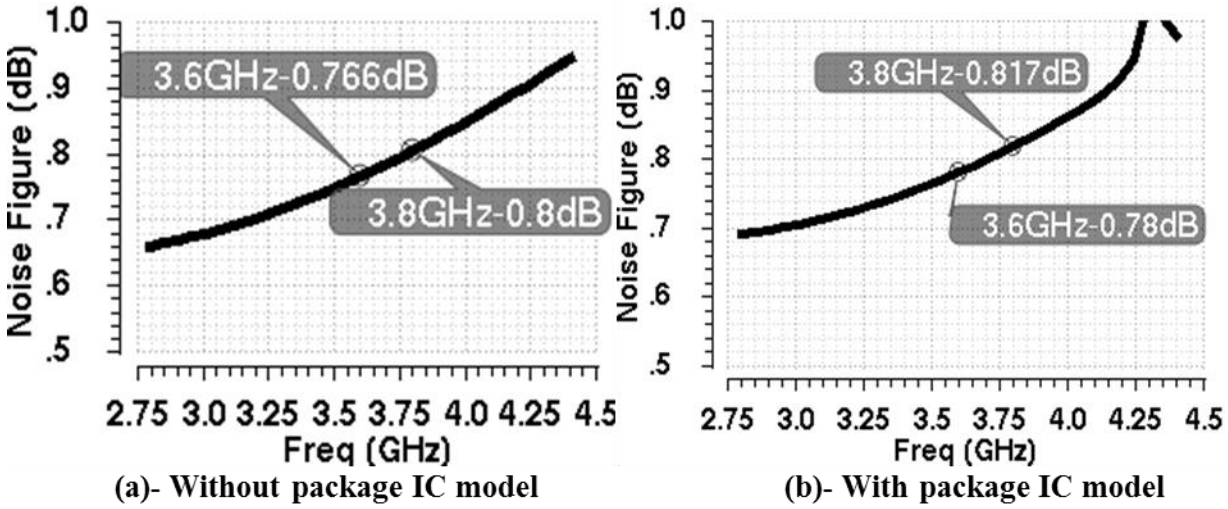


Figure 25- Noise figure simulation results at 27 C° room temperature

The S-parameters result including package IC model shows input and output return loss of better than 14 and 10 dB respectively for whole frequency range, gain of above 17 dB and reverse isolation of around 26 dB.

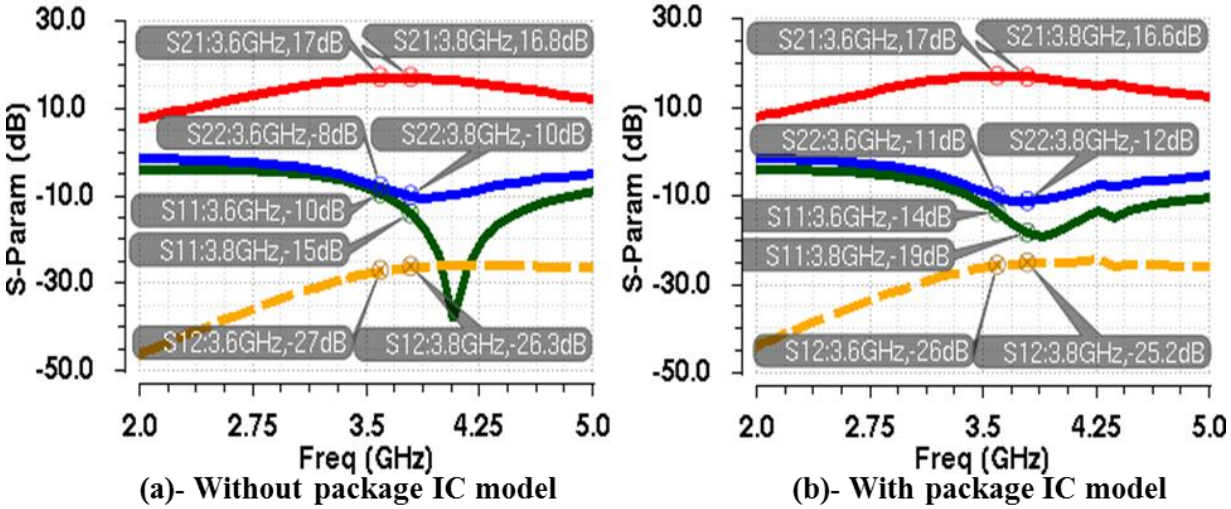
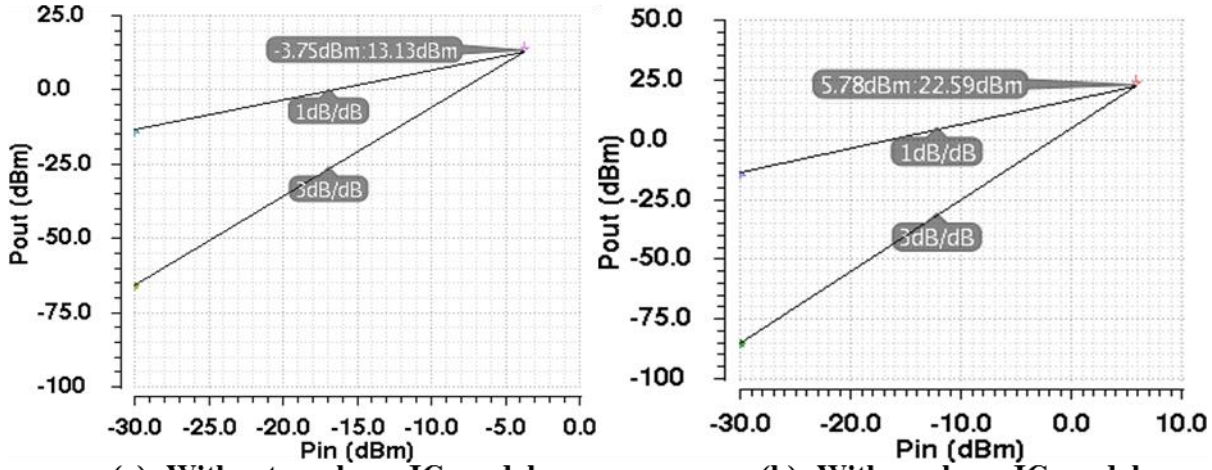


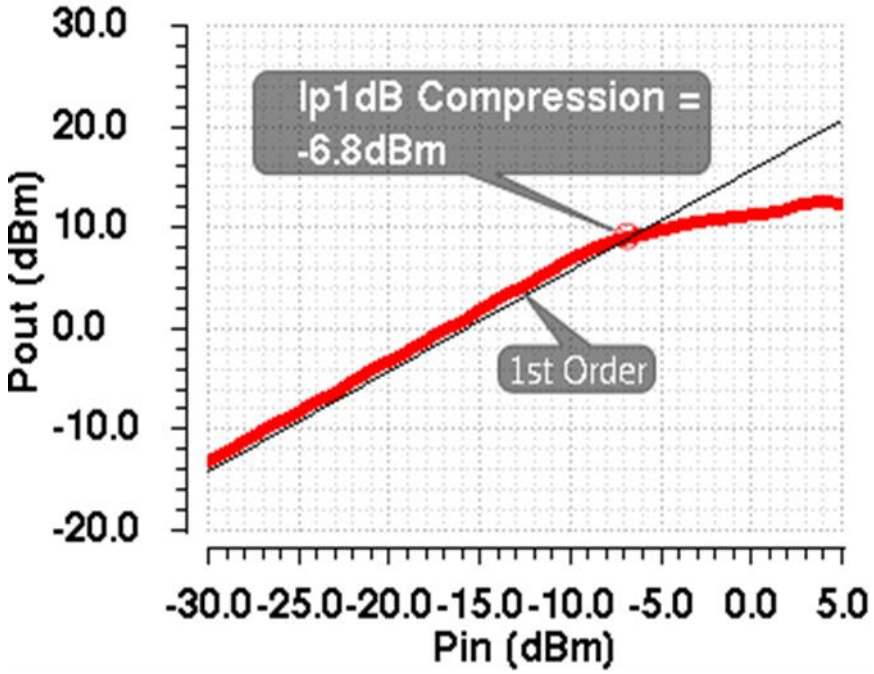
Figure 26- S-parameters simulation results at 27 C° room temperature

The LNA linearity results in terms of IIP3 and P1dB points are given in Figures 27 and 28 respectively. The same settings have been used for third-order intermodulation distortion test as before but with center frequency of 3.7 GHz. The IIP3 and P1dB points of around 5.78 dBm and -6.8 dBm are achieved respectively in package IC model simulation case.



(a)- Without package IC model (b)- With package IC model

Figure 27- IIP3 point simulation results at 3.7GHz and 27 C° room temperature



With package IC model

Figure 28- P1dB compression point simulation results at 3.7 GHz and 27 C° room temperature

Chapter 5

Layout and Simulation Results

The schematic level simulation results for QUBiC4Xi based LNA circuits were presented and discussed in detail in chapter 4 after optimizing the important circuit's parameters through iterative process to obtain desired performance. The first step to fabricate any integrated circuit is to create its layout according to the used technology process rules. Therefore, layout for both LNAs and other variants circuits was carried out using Cadence virtuoso layout editor [5]. The active, passive components and metal layers used in the layout were discussed in chapter 2. The layout procedure including floorplanning and subsequent simulated results taking into account the possible parasitics effects by means of RC extraction of core and momentum extraction of coils section are discussed in this chapter.

5.1- Floorplanning and layout

The floorplanning is the first step to create an optimal layout that can deliver close to desired circuit performance. Therefore, good time and effort is spent on floor planning by doing group discussions with in the LNA group at NXP semiconductors and placement of critical blocks of circuit and their routing was decided. The measurements will be performed on wafer level using external biasing and identical ground-signal-ground probes both at RF input and output pads. Therefore, maximum symmetry in components placements were implemented around the RF input pad specifically as can be seen in Figure 29. The CE and CB stage transistors are placed little away from RF input pad instead of right next to it, in order to realize this symmetry. The connection between RF input pad and base of CE transistor is made via highest metal 6 with lowest resistance to get negligible effect on noise figure performance as shown in Figure 30. Similarly, emitter degeneration coils and decoupling capacitors for CB stage transistor are also placed symmetrically. The emitter degeneration and collector coils are equipped with shields to prevent any parasitic coupling with silicon substrate and are checked in a separate test bench to verify that their resonance frequency is well above the design bandwidth of interest. The current mirror bias setup placed right next to base of current mirror transistors is realized using eleven identical resistors of 10 kΩ to obtain 1:10 ratio to mirror desired current in collector terminal of CB transistor. The feedback capacitor is placed such that it has the shortest return path from CB collector terminal to CE base terminal. Output matching network is placed right next to the CB collector terminal and a very well modeled 50 Ω transmission line is used to rout it to the RF out pad as shown in Figure 30. By taking advantage of symmetrical ground domains of transmission line, a clear return ground path for RF current from output to input port is defined by connecting input and out port ground domains together via transmission line grounds as labeled in Figure 29.

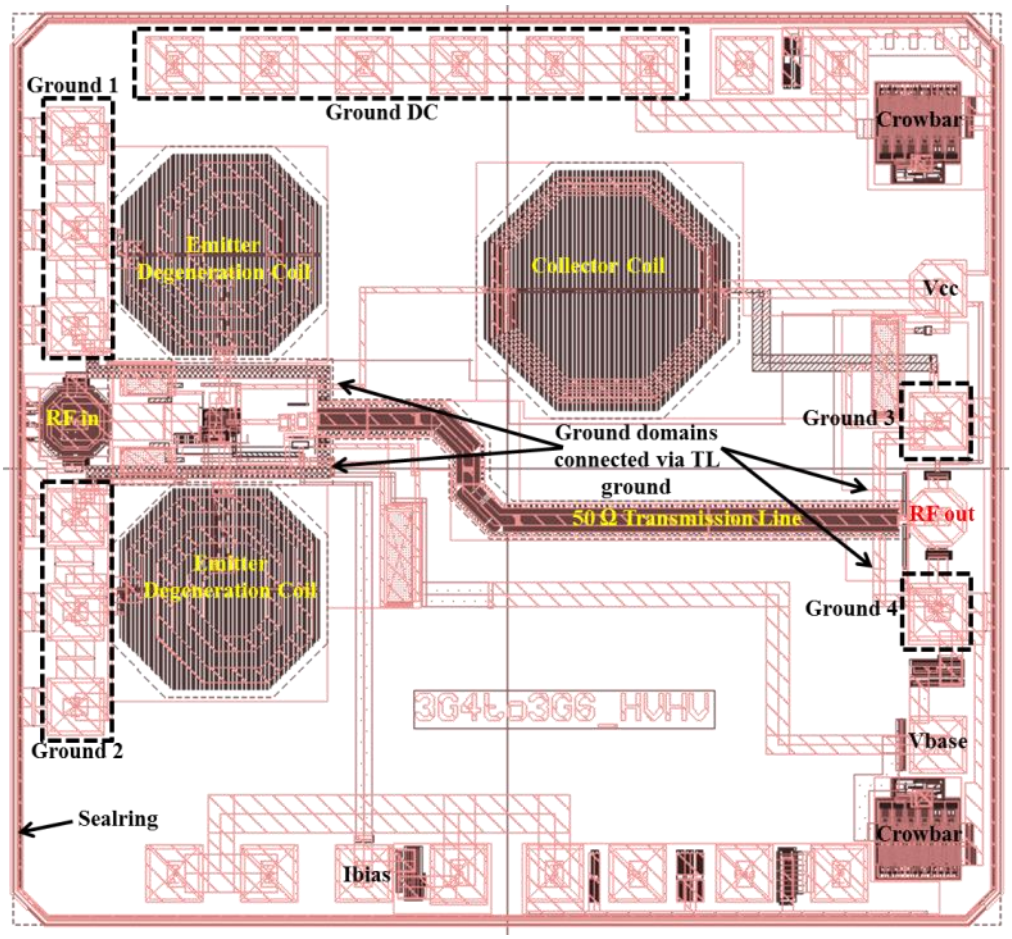


Figure 29- Top level layout view of complete LNA circuit

The 3 bond pads on each side of RF input bond pad are combined together to create RF input ground domains as labeled in Figure 29, to mitigate the effect of packaged bond wires getting connected together on PCB ground plane. All the routing paths wherever possible are created using high level metal 5 and 6 due to their lowest resistance. The interconnections between

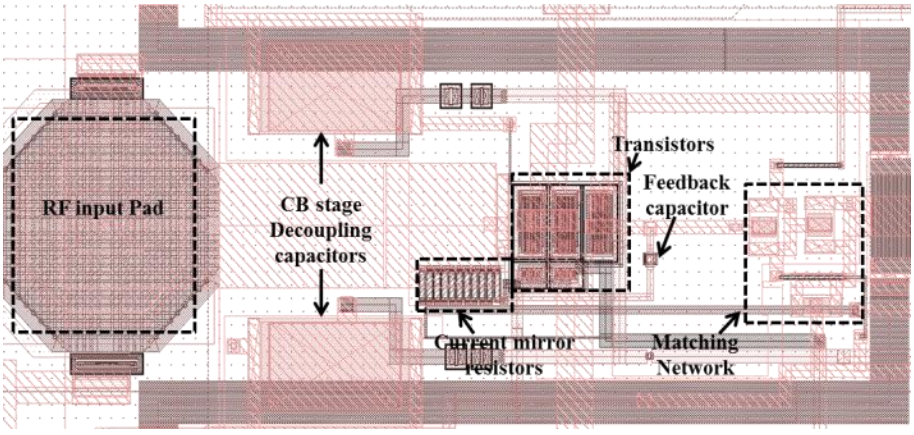


Figure 30- Zoomed view of LNA layout area close to RF input pad

different metal layers and transistors terminals are done using via stacks consisting of via 1-5. It is important to mention that layout is carried out using already existing pad ring designed for a fixed die size and used by LNA group for other frequency band LNAs. Thus, I was restricted in terms of layout area to comply with the die size area and usage of already defined bond pads for RF input, output, DC biasing and ground domain connections. The pad ring was updated only to make it compatible with QUBiC4Xi library since old pad ring was based on older version of QUBiC4X library. The decision to stick with already defined pad ring and die size area was taken so that the circuit can be packaged later on using already existing well modeled and tried PCB's.

Figure 29 shows the complete layout of top level of LNA circuit which occupies an area of 1204 x 1304 μm^2 and contain pad ring, core and coil sections. Each section is individually synchronized with corresponding schematic sections using LVS and DRC tools. The RC extraction of the core section is done using Assura tool in cadence virtuoso whereas coils section is used to obtain momentum view which is exported and simulated in ADS momentum to exactly characterize its RF behavior. The powerful "config" view of cadence is utilized to include the extracted versions of the core and coil sections results along with IC package model S-parameters to obtain the results which we expect to get from the fabricated circuits. After optimizing the circuit parameters, GDS files of the circuits layout were obtained after performing tiling operation on the top level of hierarchy excluding the matching networks, coils and important RF paths via "nontitle(drw)" since RF performance can get effected by tiling which is not desired. After performing tiling operation circuits are checked and verified again using LVS and DRC tools. Finally, the translated GDS files were sent to the foundry for fabrication.

5.2- Simulation results[3]

The simulation results with and without including the IC package model effect along with extracted views of core and coil sections for both 3.5 and 3.7 GHz LNAs at room temperature of 27 C° are presented here. The APPENDIX C contains the compliance table comparing the variation of performance parameters of LNA circuits over three temperatures of 27 C°, -40 C° and 100 C°.

5.2.1- 3.5 GHz LNA

The stability simulation results presented in Figure 31 exhibit trends similar to the schematic level simulations discussed in chapter4. With package IC model case, LNA is unconditionally stable whereas without package IC model simulation results shows that K-factor goes below 1 between 17-24 GHz frequency range.

[3] The compliance table listing results at all three temperatures of 27 C^{o},-40 C^{o} and 100 C^{o} for two main variants are included in APPENDIX C.

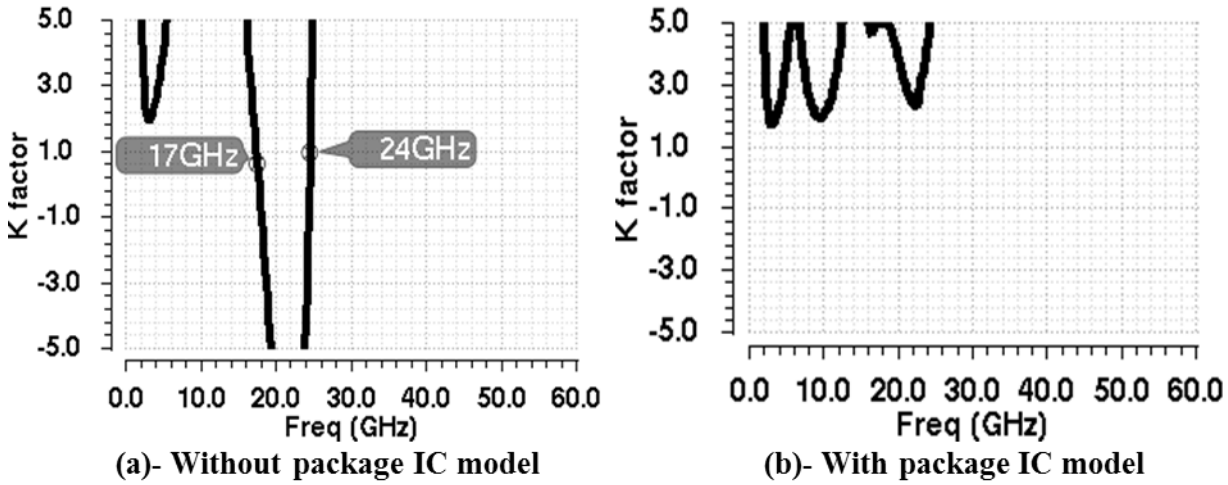


Figure 31- Stability simulation results on wafer and packaged device level

The noise figure simulation results shows a maximum noise figure of around 0.87 dB at highest frequency of 3.6 GHz for package IC model case. Furthermore, there is less than 0.05 dB difference in noise figure for package and without package cases.

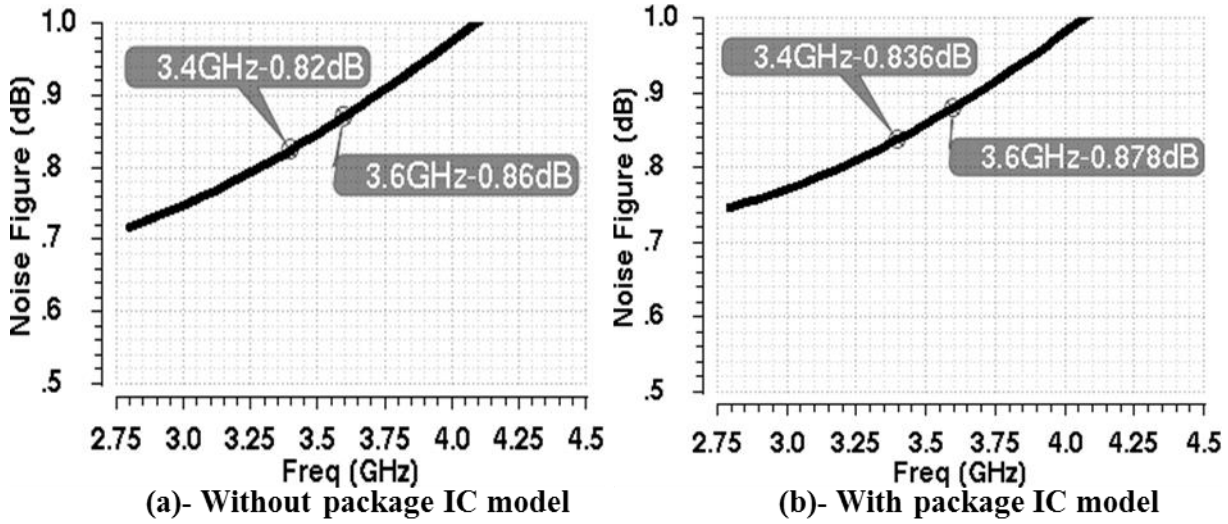


Figure 32- Noise figure simulation results at 27 C° room temperature

The S-parameters results gives input and output return loss of better than -20 dB and -6 dB respectively along with reverse isolation of 30 dB and 17 to 18 dB of gain variation over the frequency band for package IC model case as can be seen from Figure 33.

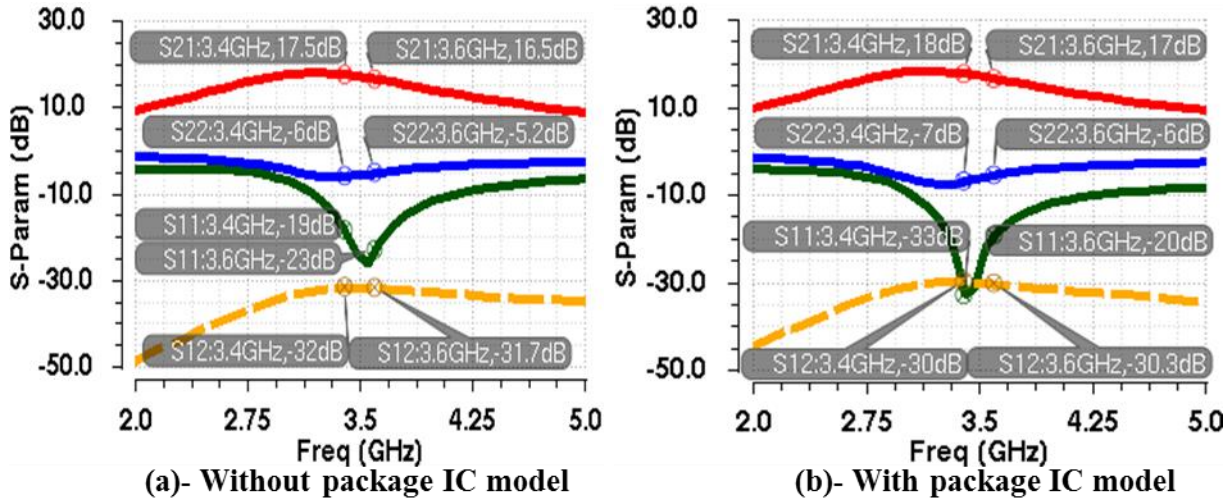


Figure 33- S-parameters simulation results at 27 C° room temperature

The ac analysis based "Rapid IP3" test with input power of -30 dBm and two tones around 3.5 GHz center frequency separated by 1 MHz is used to obtain IIP3 results and are shown in Figure 34. It can be seen that IIP3 of 8.45 dBm is obtained for package IC model case.

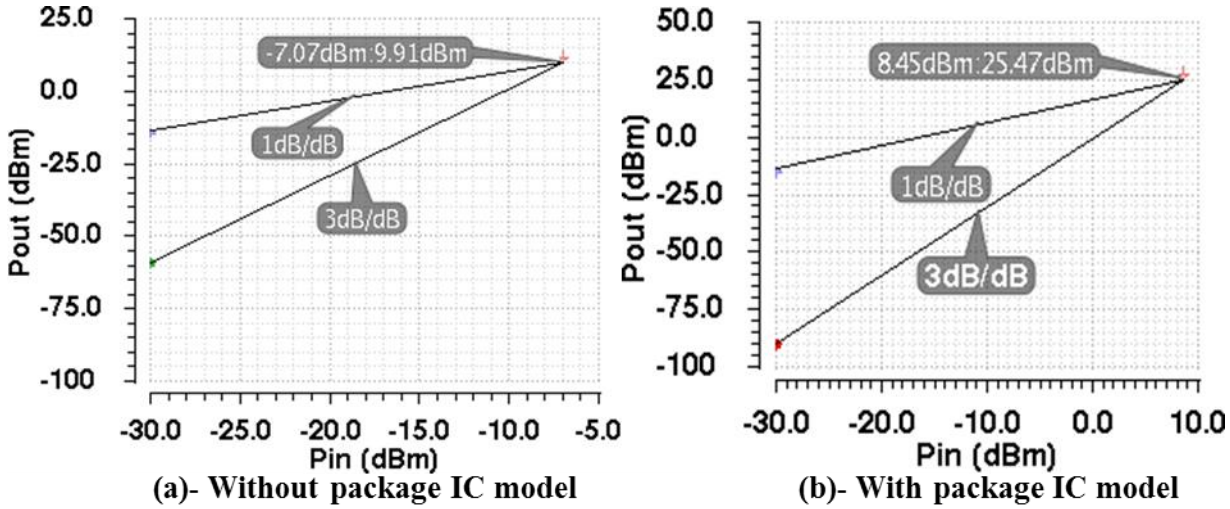


Figure 34- IIP3 point simulation results at 3.5 GHz and 27 C° room temperature

Figure 35 presents the P1dB compression point result at 3.5 GHz center frequency using periodic steady state analysis "Pss". The input power level is varied between -30 dBm to 5 dBm range and the resulting graph gives P1dB compression point value of around -9 dBm. The P1dB compression point result for without package IC model case is not included here since even after trying all different possible settings simulation fails to converge for it.

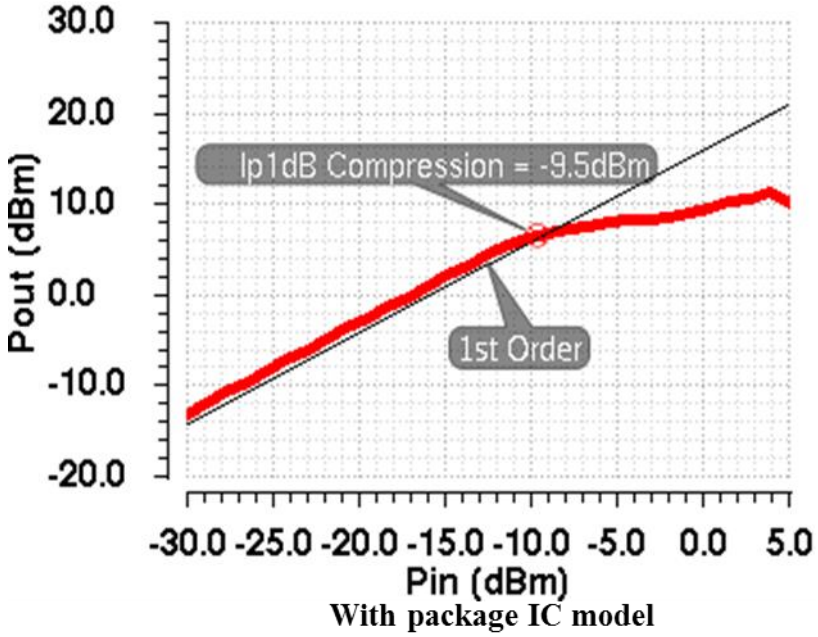


Figure 35- P1dB compression point simulation results at 3.5 GHz and 27 C° room temperature

5.2.2- 3.7 GHz LNA

The K-factor simulation results given in Figure 36 shows that LNA is unconditionally stable for package IC model case whereas unstable for without package IC model case.

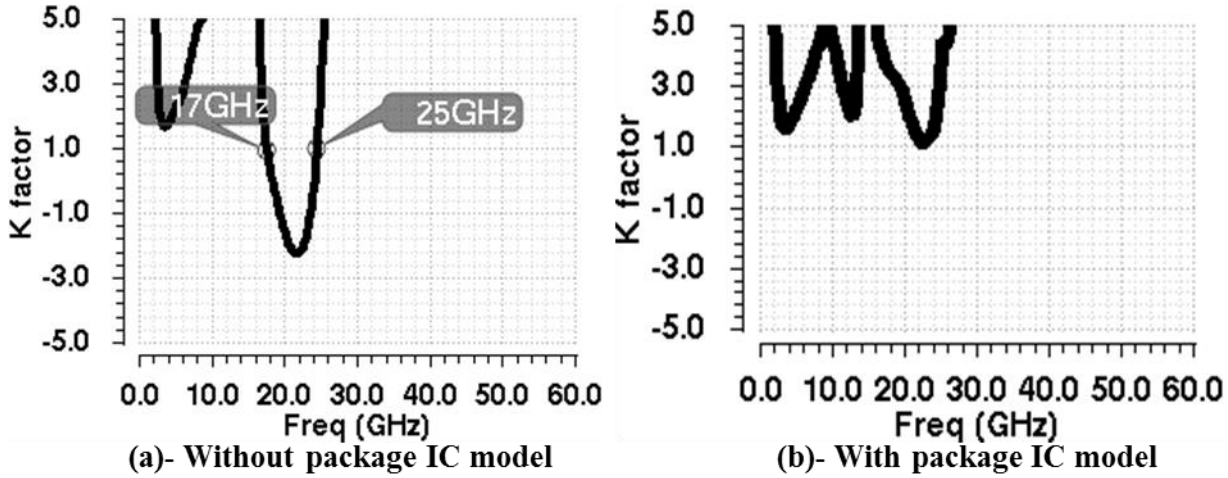


Figure 36- Stability simulation results on wafer and packaged device level

Noise figure analysis results presented in Figure 37 shows that highest noise figure of around 0.9 dB is obtained at highest frequency of 3.8 GHz at room temperature of 27 C°.

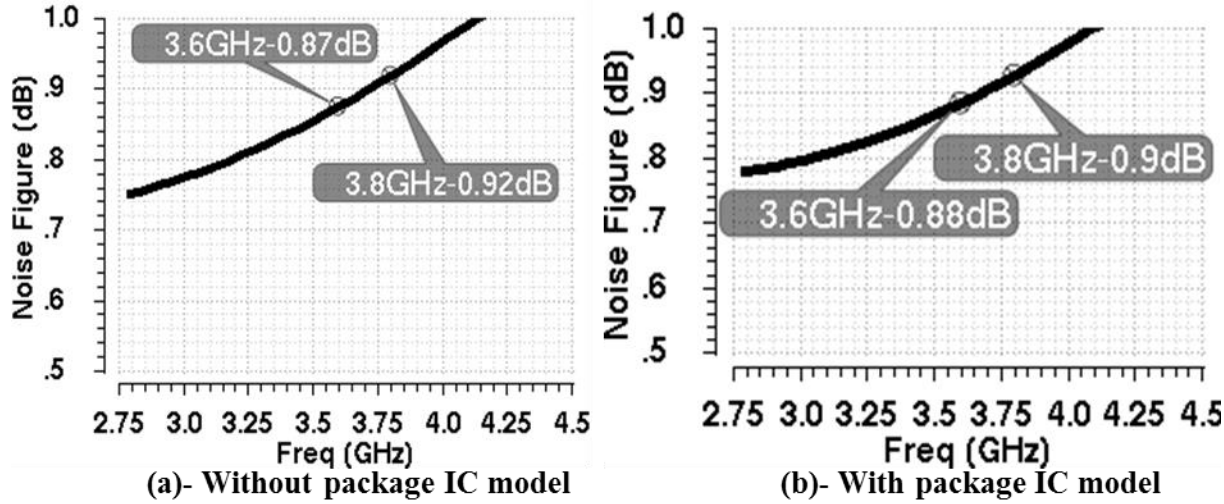


Figure 37- Noise figure simulation results at 27 C° room temperature

Figure 38 include the S-parameters simulation results for both cases. It is clear that S11 and S22 of better than -15 dB and -8 dB respectively are achieved for whole frequency band of 3.6-3.8 GHz for package IC model case. Furthermore, S21 of 16 dB and S12 of better than 26 dB is also obtained.

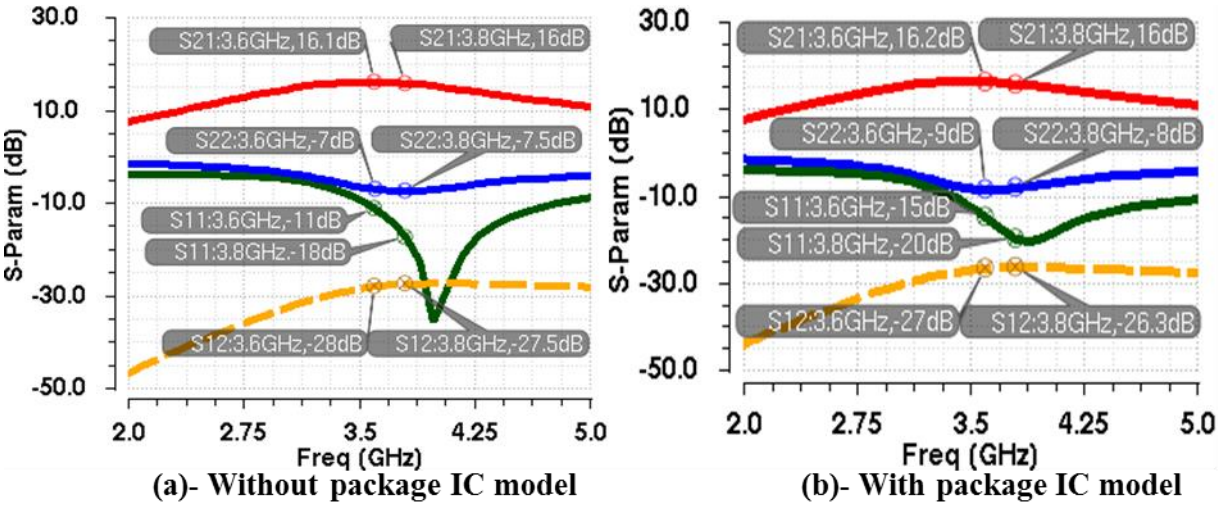


Figure 38- S-parameters simulation results at 27 C° room temperature

The 3.7 GHz LNA linearity results for IIP3 and P1dB compression points are presented in Figures 39 and 40 respectively. The same settings and analysis tests as described for 3.5 GHz

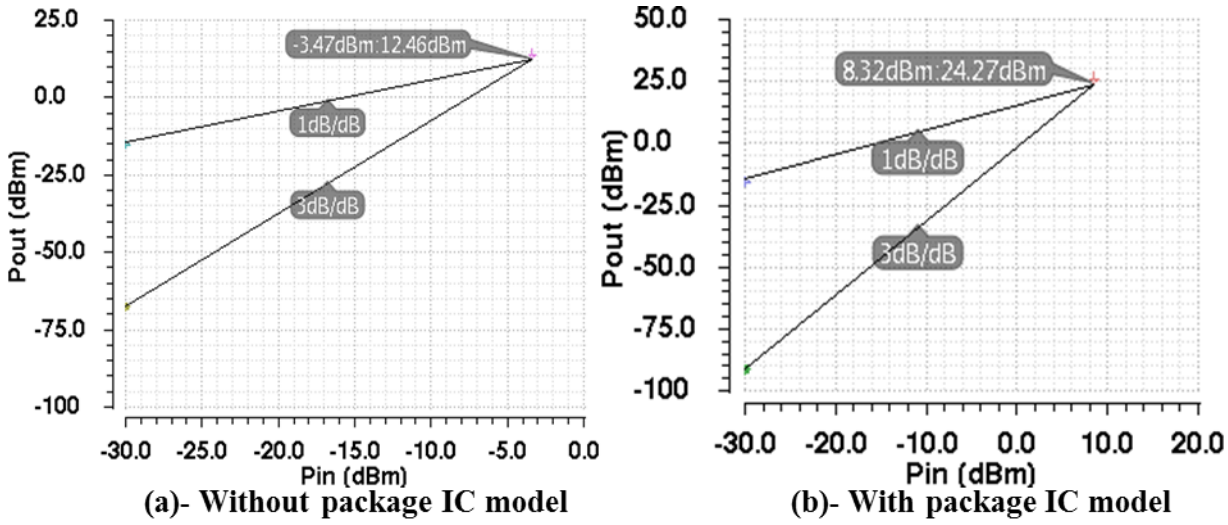


Figure 39- IIP3 point simulation results at 3.7 GHz and 27 C° room temperature

LNA case is used here. The P1dB compression point of -6.5 dBm is obtained for package IC model simulation case. The simulation results give IIP3 point of around 8 dBm for package IC model case and -3.47 dBm for without package IC case. The huge difference between the two cases cannot be explained and only the measurement results can be fully trusted. The LNA group at NXP also experienced few dBs of difference in IIP3 results between simulation and measurements.

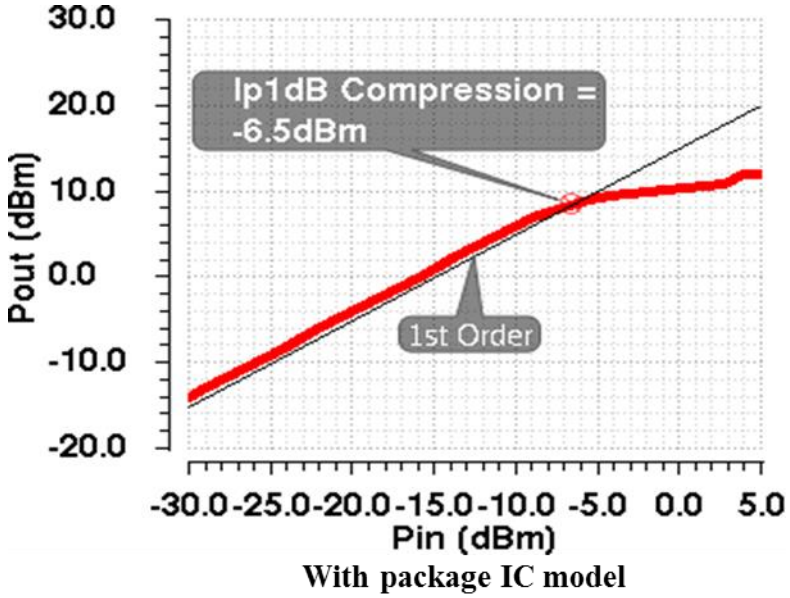


Figure 40- P1dB compression point simulation results at 3.7 GHz and 27 C° room temperature

Chapter 6

LNA Measurements

The GDS files of designed LNA circuit's layout as discussed in detail in the previous chapter were sent to foundry for fabrication. The fabricated LNA circuit of main variant without IC package model inclusion, from now on referred to as wafer level, is shown in Figure 41.

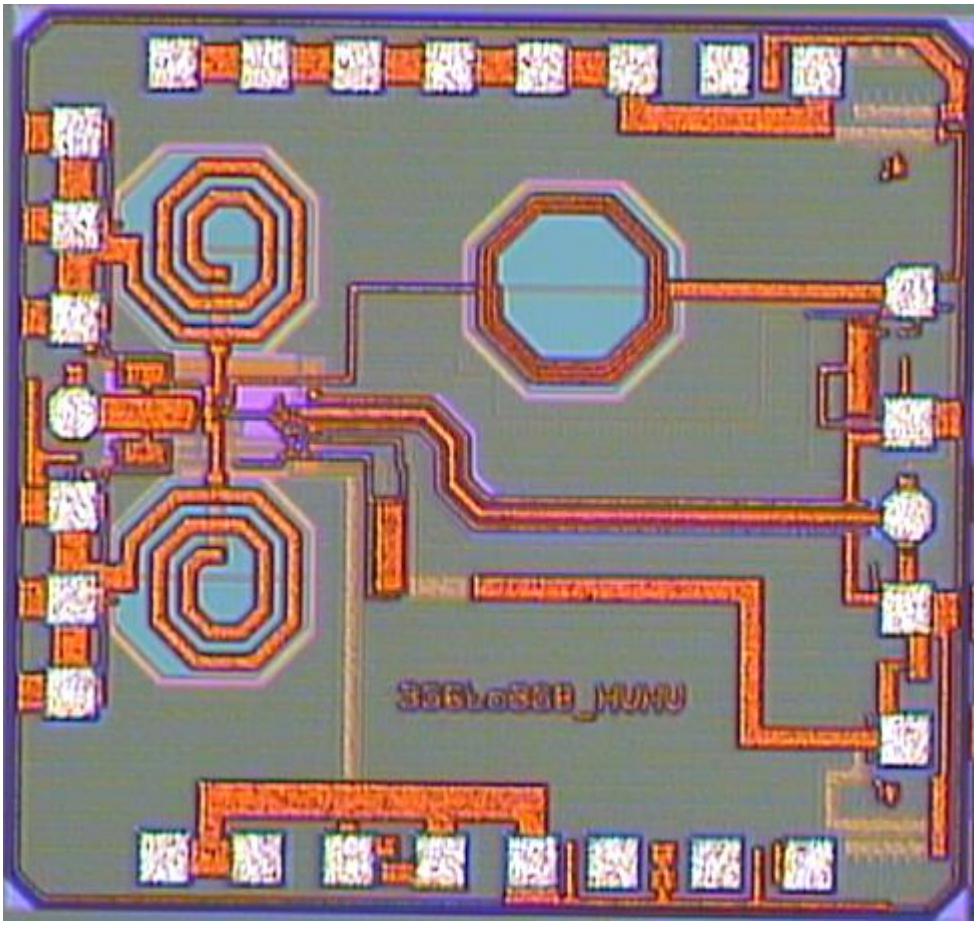


Figure 41- Fabricated LNA diagram used for wafer level measurements

To completely characterize the fabricated LNAs circuits, three different types of measurements; small signal S-parameters, linearity and noise figure using lab equipment at NXP semiconductors were performed on wafer level. The CascadeMicrotech [27] wafer probe station shown in Figure 42 is used for measurements and the results obtained were extremely promising and showed good agreement with the simulated results. Thus, the approach used to design the circuits is validated.

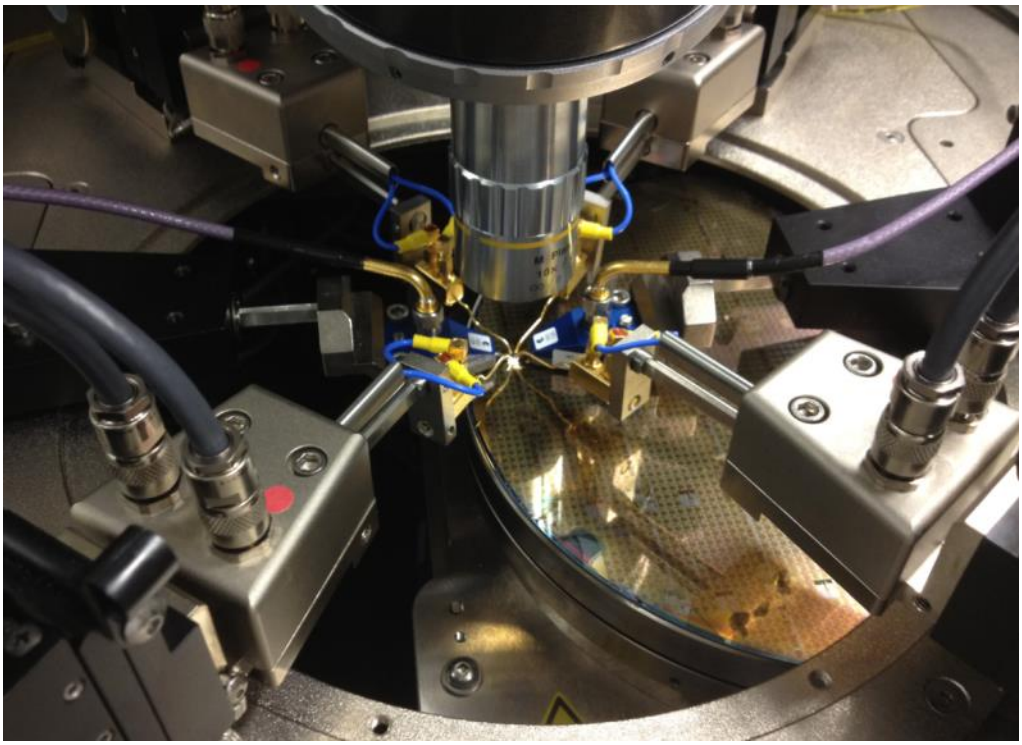


Figure 42- Wafer probe station measurement setup

6.1- S-parameters measurements

For small signal S-parameters measurements VNA covering frequency spectrum of 50 MHz to 13.5 GHz is being calibrated and used. The designed circuits are probed using identical GSG probes with 125 µm pitch at input and output bond pads. Four external dc sources are used to correctly bias the circuits. The measurements are done with different bias settings and data was collected for post processing in cadence. The measured and simulated results reported here are obtained with supply voltage of 5 V, 1.75 V of base voltage for CB stage and 15 mA collector current.

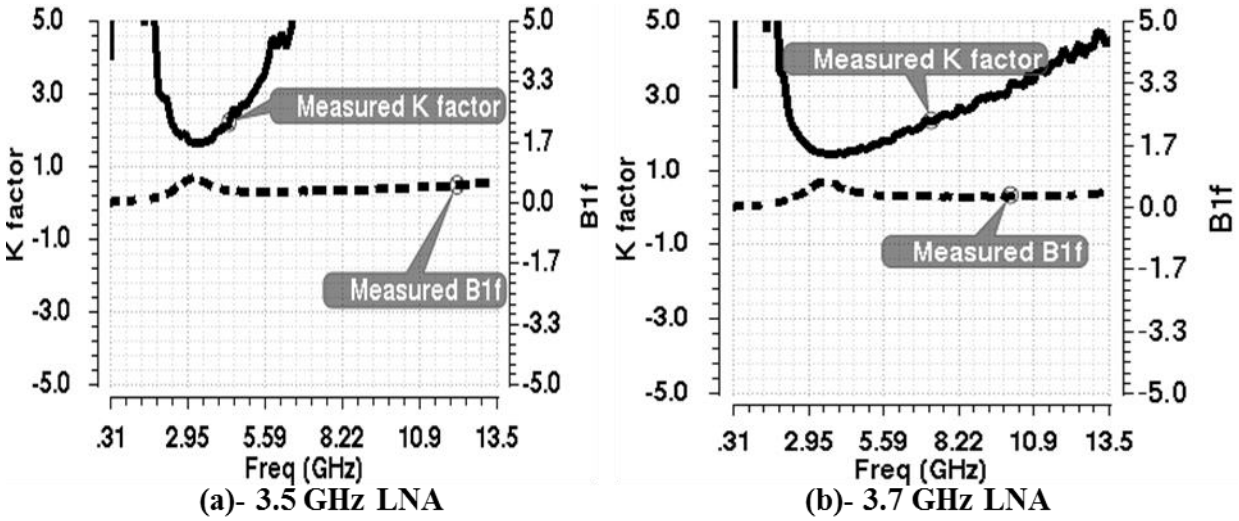


Figure 43- Measured Stability results of both LNAs

Figure 43 represents the measured stability results for both LNAs. It can be seen that circuits are unconditionally stable since K > 1 and B1f > 0 for the whole frequency range of VNA. Furthermore, before performing S-parameters measurements with calibrated VNA, a sanity check is done to see any possible oscillations by connecting output GSG probe to the Agilent SA (3 HZ – 26.5 GHz) and input GSG probe to the signal generator to provide RF input signal. No oscillations were observed in the whole frequency range from 3 Hz to 26.5 GHz which gives a good indication that circuit is stable for a wide frequency range.

The measured and simulated results for S11, S22, S21 and S12 for both LNAs are compared in Figures 44 and 45 respectively using cadence. It can be seen that there is good agreement between the simulated and measured results. The 3.5 GHz LNA has a measured input match of better than -21 dB for whole bandwidth with a gain variation of 18 – 17 dB from 3.4 – 3.6 GHz achieving gain flatness of 1 dB. The output of the amplifier is not very well matched and provides a return loss of better than -4 dB for the whole frequency band. The reverse isolation of better than -32 dB is measured over whole frequency band of 3.4 – 3.6 GHz.

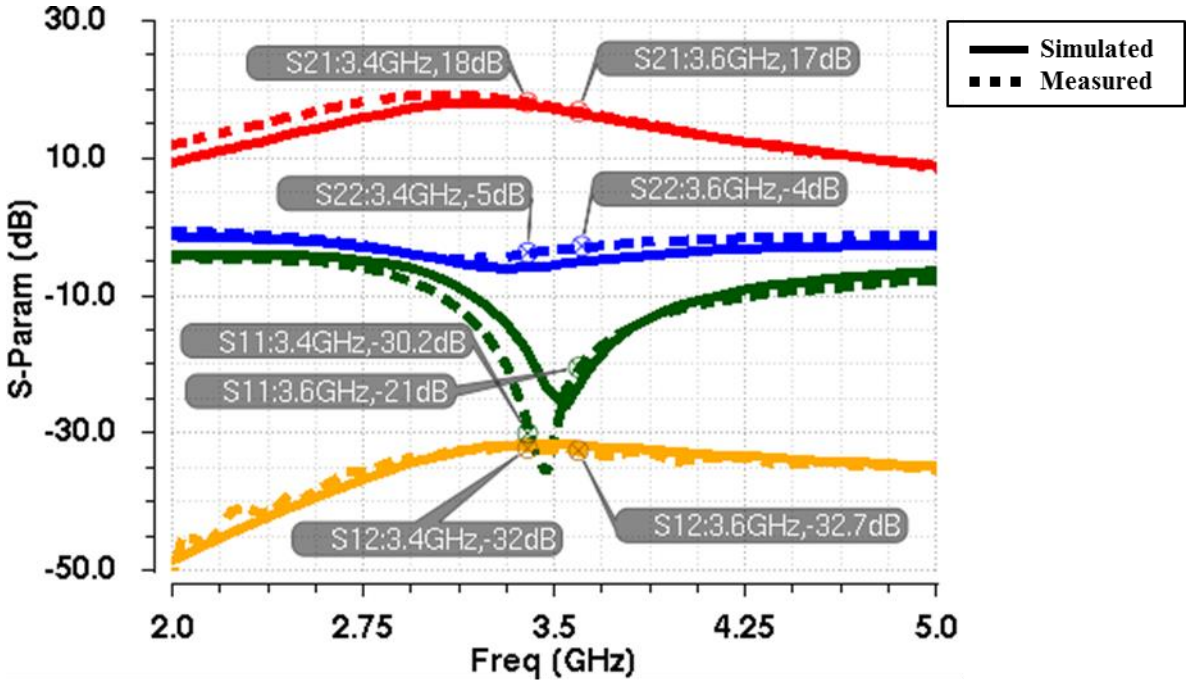


Figure 44- S-parameters simulated and measured results of 3.5 GHz LNA

The measured S11, S22 and S21 for 3.7 GHz LNA gives results better than -14 dB, -5 dB and 16.5 dB respectively for the whole bandwidth. Furthermore, reverse isolation of around -28 dB is measured.

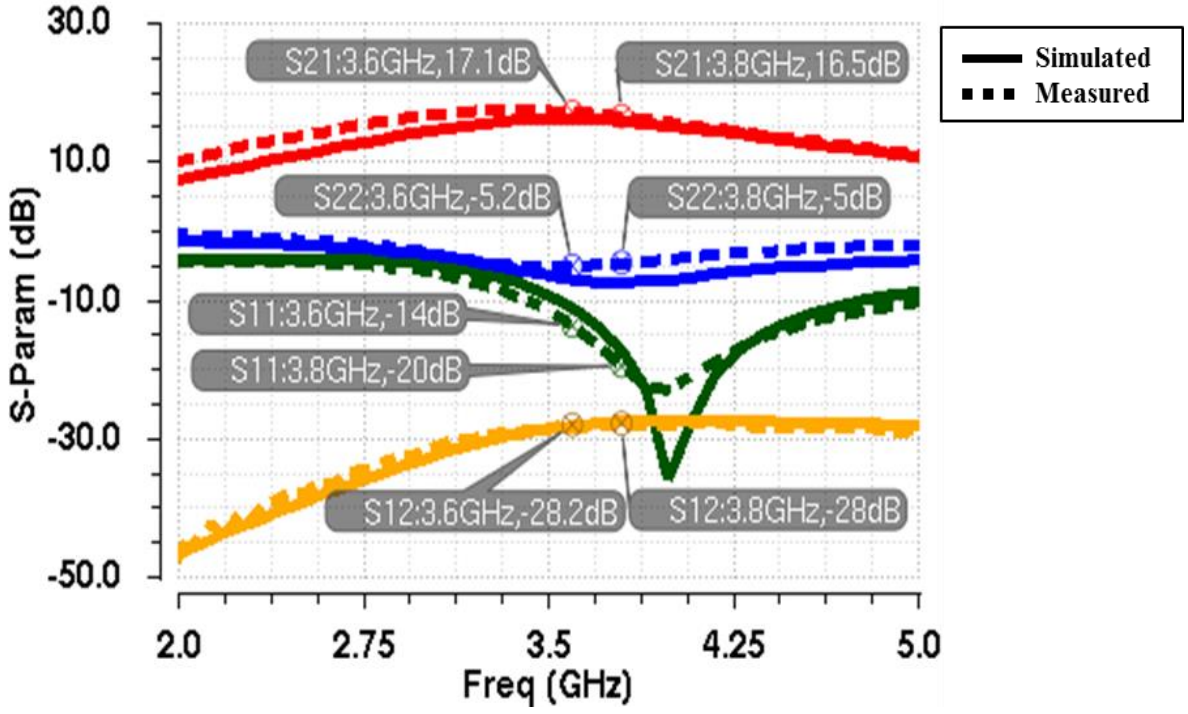


Figure 45- S-parameters simulated and measured results of 3.7 GHz LNA

6.2- Linearity measurements

The block diagram of the measurement test bench setup used to measure IIP3 and P1dB points is shown in Figure 46. The equipment involved for the linearity measurements include two Agilent vector signal generators (250 KHz – 6 GHz), power combiner (DC – 18 GHz) with very good isolation and Agilent SA (3 Hz – 26.5 GHz). The power calibration was done in order to correctly characterize the losses introduced by the cables used in the measurement test bench setup.

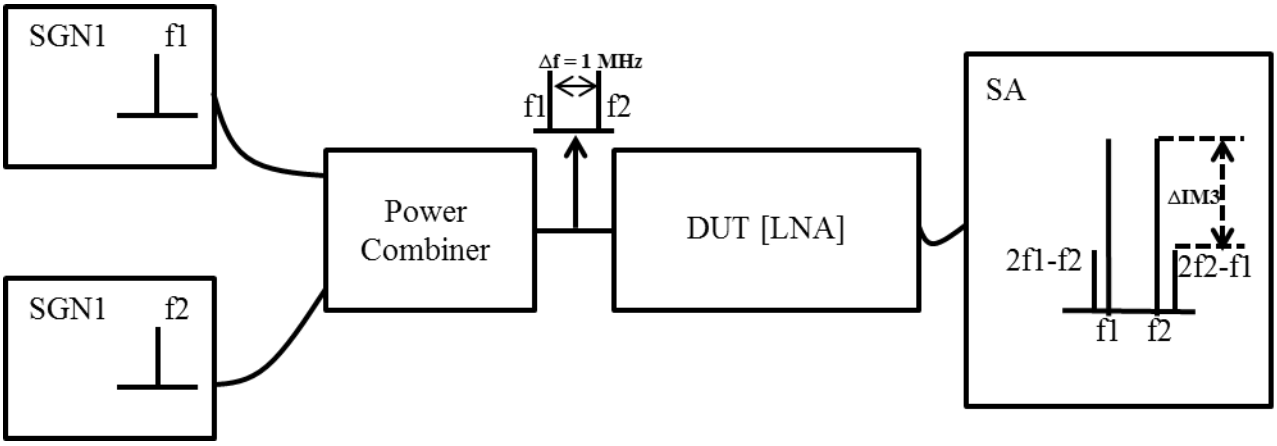


Figure 46- Block diagram of test bench setup for IIP3 and P1dB points measurement

For IIP3 measurements, two tones separated by 1 MHz were generated using the two signal generators. The two tones were then combined with the help of power combiner and fed in to the input of LNA. The corresponding power levels of fundamental and third order intermodulation distortion tones were observed and noted down using spectrum analyzer. Then the IIP3 point is calculated with the help of following equation

$$IIP3\ [dBm] = P_{in} + \Delta IM_3/2 \qquad \textbf{(6.1)}$$

Here ΔIM_3 is the difference in power levels of third order intermodulation product and main tone. The IIP3 points were calculated for both upper and lower side bands with input power level of -30 dBm and small variations in IIP3 values were found in both sideband cases. The input power level of -30 dBm is selected after performing power sweep from -30 dBm to 3 dBm and plotting IM3 versus input power level curve to select the input power level falling in the linear region. For P1dB compression point measurements same measurement setup was used but in this case, one signal generator was turned off and the input power level was swept from -30 dBm to 6 dBm and corresponding output power levels were read out from SA.

The IIP3 and P1dB measurements were performed for both LNAs. The resulting data was then used to plot IIP3 and P1dB curves versus input power for both 3.5 and 3.7 GHz LNAs with the help of Microsoft Excel. The P1dB and IIP3 versus input power graphs for 3.5 GHz LNA are

shown in Figures 47 and 48 respectively. It can be seen that P1dB compression point is reached at input power level of around -10 dBm whereas IIP3 of 0 dBm is obtained just fulfilling the required target of 0 dBm.

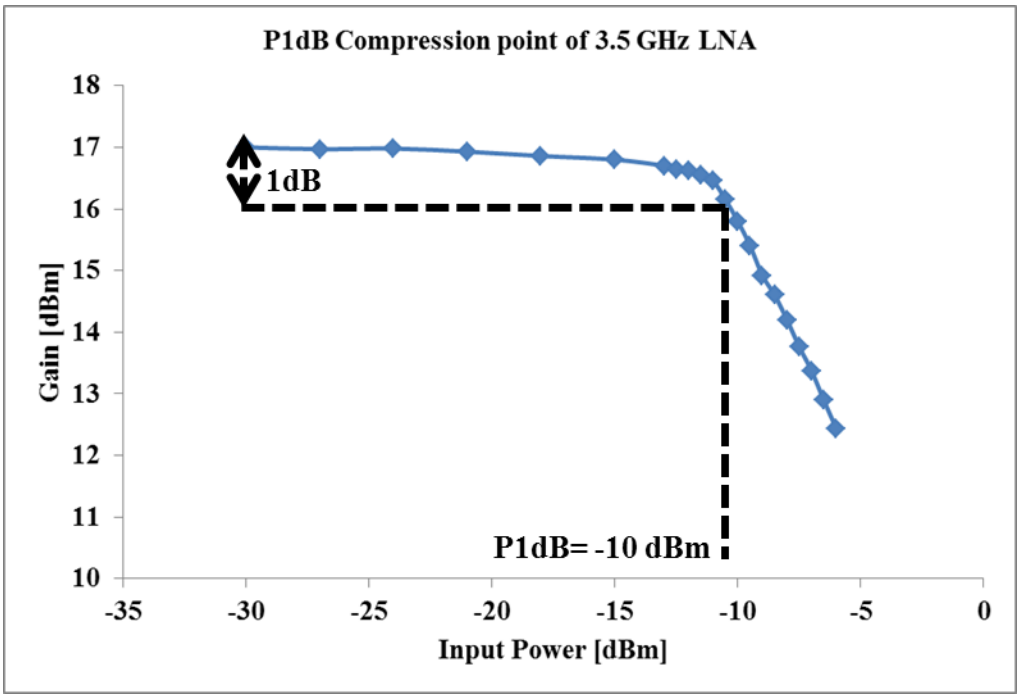


Figure 47- Measured P1dB compression point of 3.5 GHz LNA

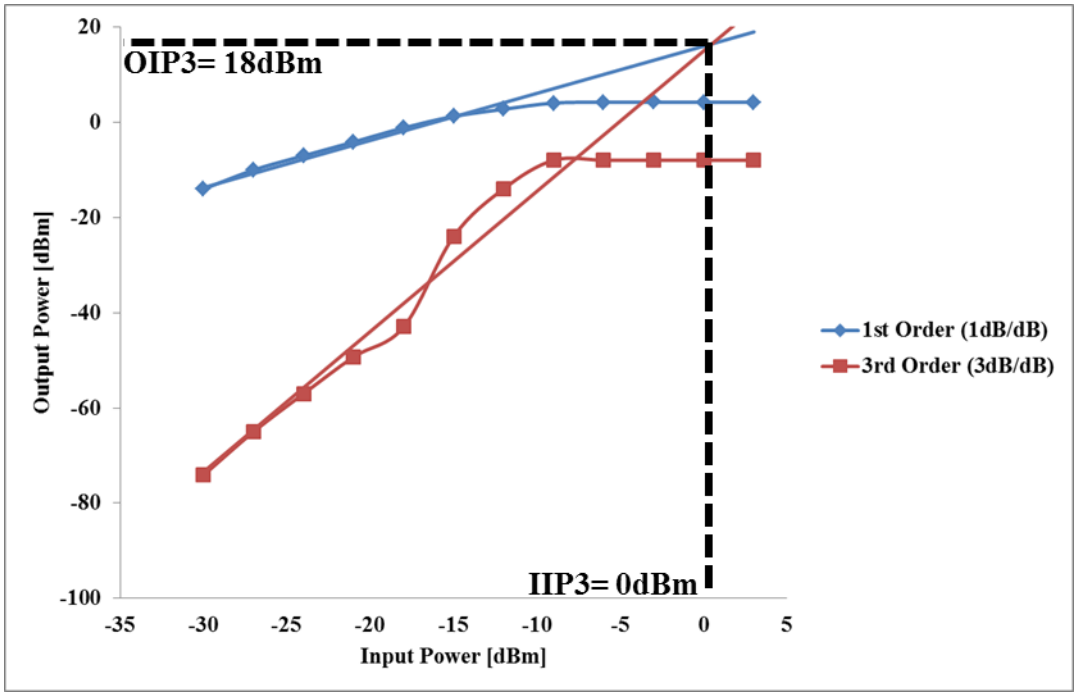


Figure 48- Measured IIP3 of 3.5 GHz LNA

It can be seen from Figures 49 and 50 respectively that P1dB compression point is reached at input power level of -7.2 dBm along with having 2.65 dBm of IIP3 in the case of 3.7 GHz LNA.

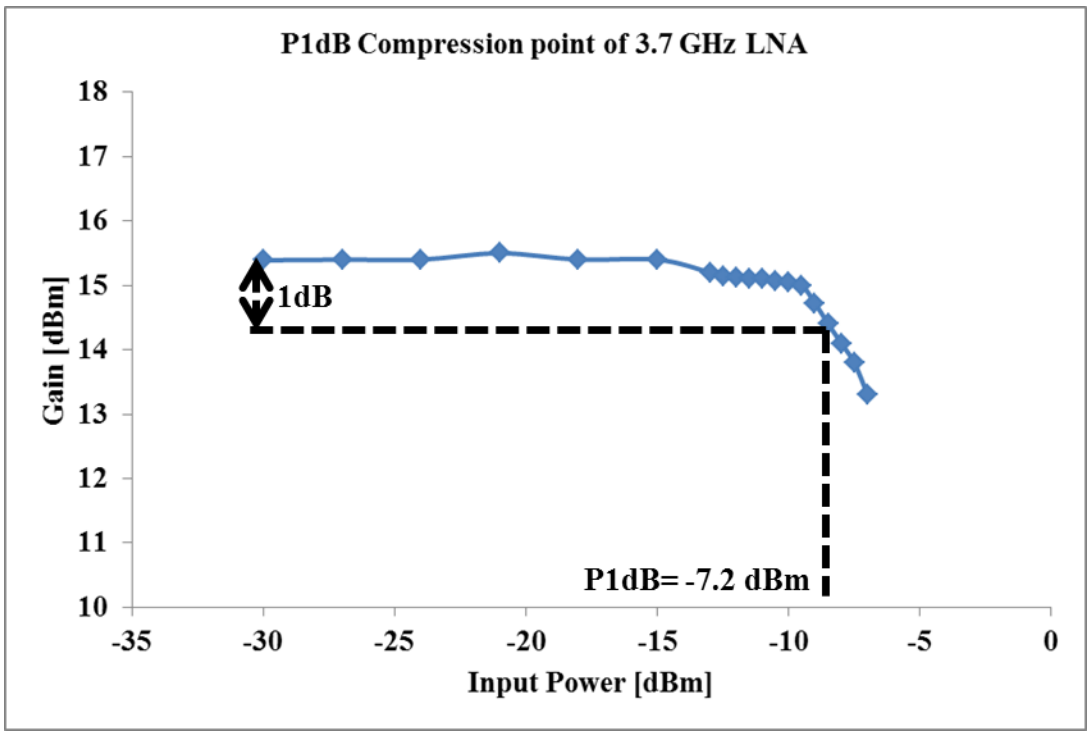


Figure 49- Measured P1dB compression point of 3.7 GHz LNA

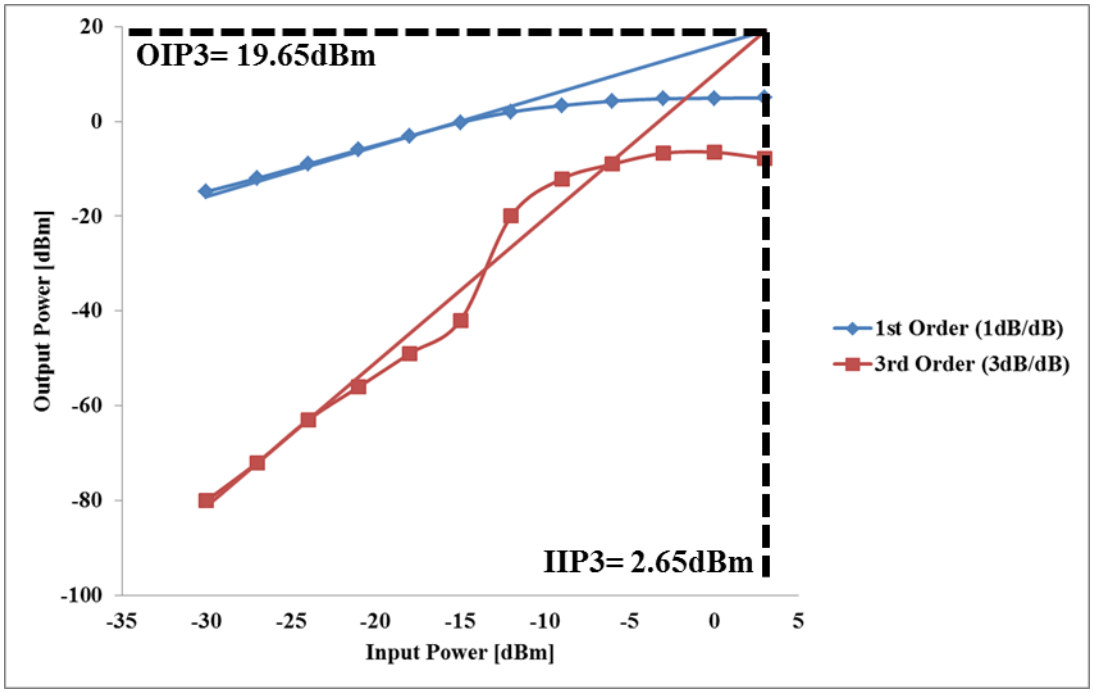


Figure 50- Measured IIP3 of 3.7 GHz LNA

6.3- Noise Figure Measurements

The noise figure of the designed LNAs was measured using the test bench setup depicted in Figure 51. The Rhode&Schwarz spectrum analyzer (20 Hz – 46 GHz) is used for this purpose along with Agilent noise source (0.01 GHz – 18 GHz) having ENR (4.96 dB – 4.61 dB). A pre-amplifier (2 GHz – 4 GHz) with 38 dB gain and 0.4 dB of noise figure is used for proper amplification of the output signal of LNA before being fed to the SA in order to bring the signal above the noise floor level of the SA.

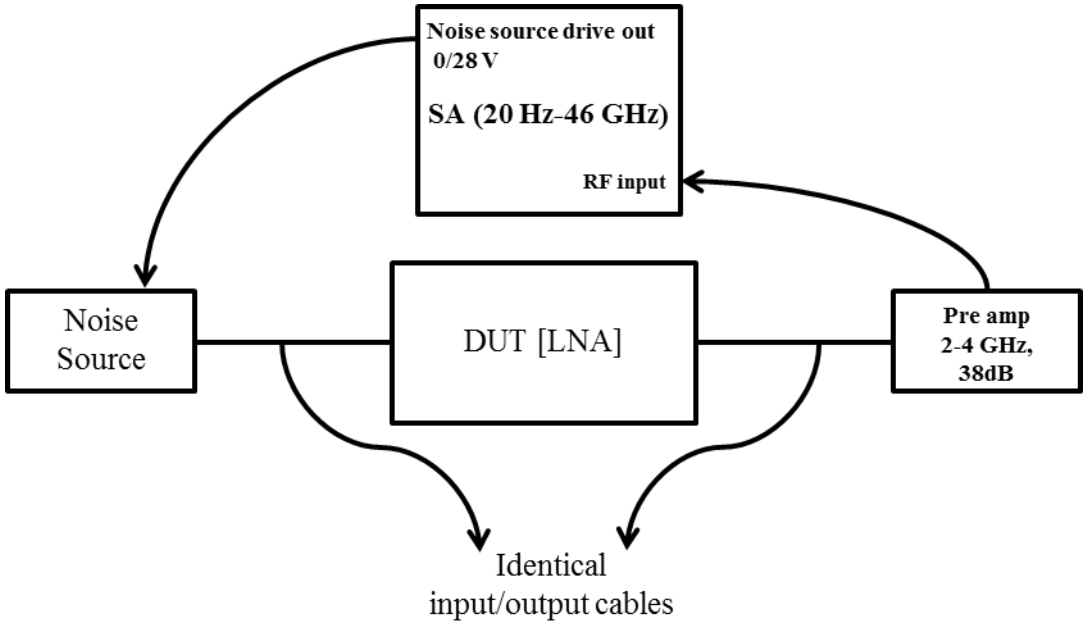


Figure 51- Block diagram of Noise figure measurement test bench setup

Two identical cables were used at input and output of LNA and their total loss was measured using VNA by performing through measurement on calibration substrate. This total loss was divided in half since the two cables were identical and input and output loss tables were filled out in SA for the frequency range of interest i.e 3.4 to 3.8 GHz before performing the calibration. The noise source was connected directly to the SA input via a through and after entering frequency range of measurement, calibration was performed. After calibrating the SA the through of the circuit was replaced with LNA to be measured. The noise source was derived at two different temperature levels with the help of 0/28 V pulse drive source of SA. The resulting noise figure corresponding to frequency band of interest was measured by SA and resulting data was exported to plot it together with the simulated noise figure using Microsoft Excel.

Figures 52 and 53 represent the comparison between simulated and measured noise figure performance for 3.5 GHz and 3.7 GHz LNA respectively. It can be seen that measured noise figure level is better than the simulated ones for both LNAs. The maximum noise figure of 0.78 dB is reached for 3.5 GHz LNA for whole 3.4 to 3.6 GHz band. Similarly, for 3.7 GHz LNA

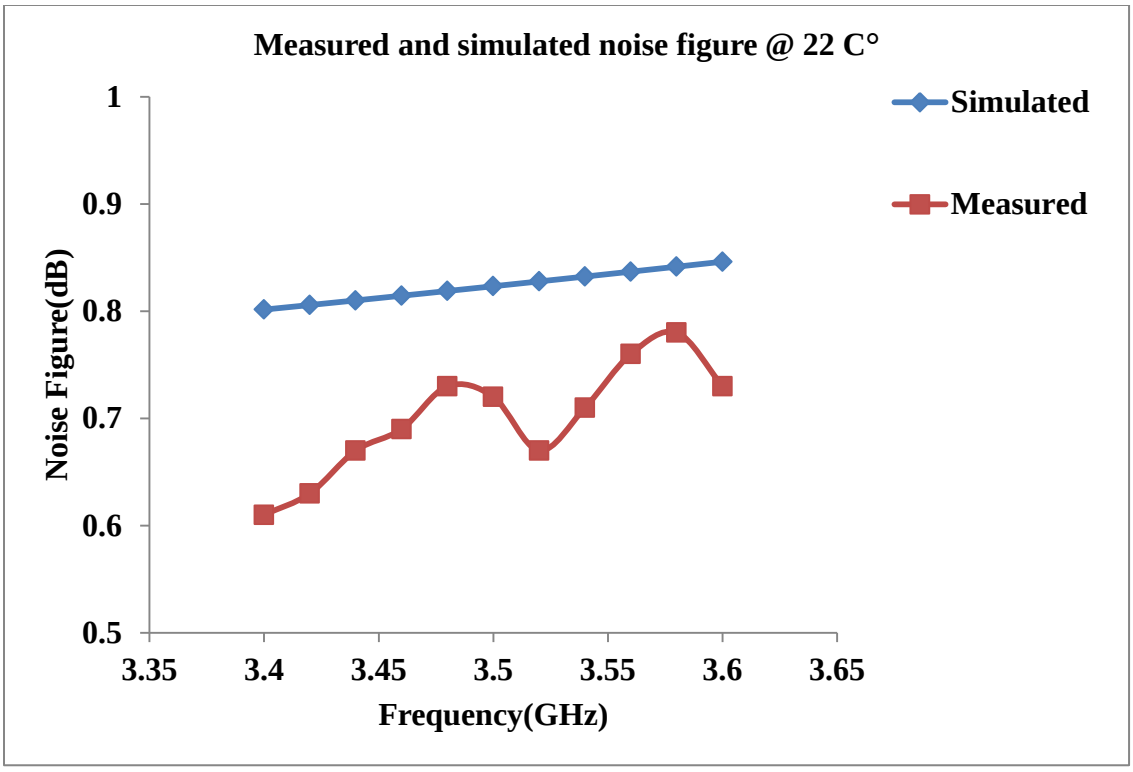


Figure 52- Simulated and measured noise figure of 3.5 GHz LNA

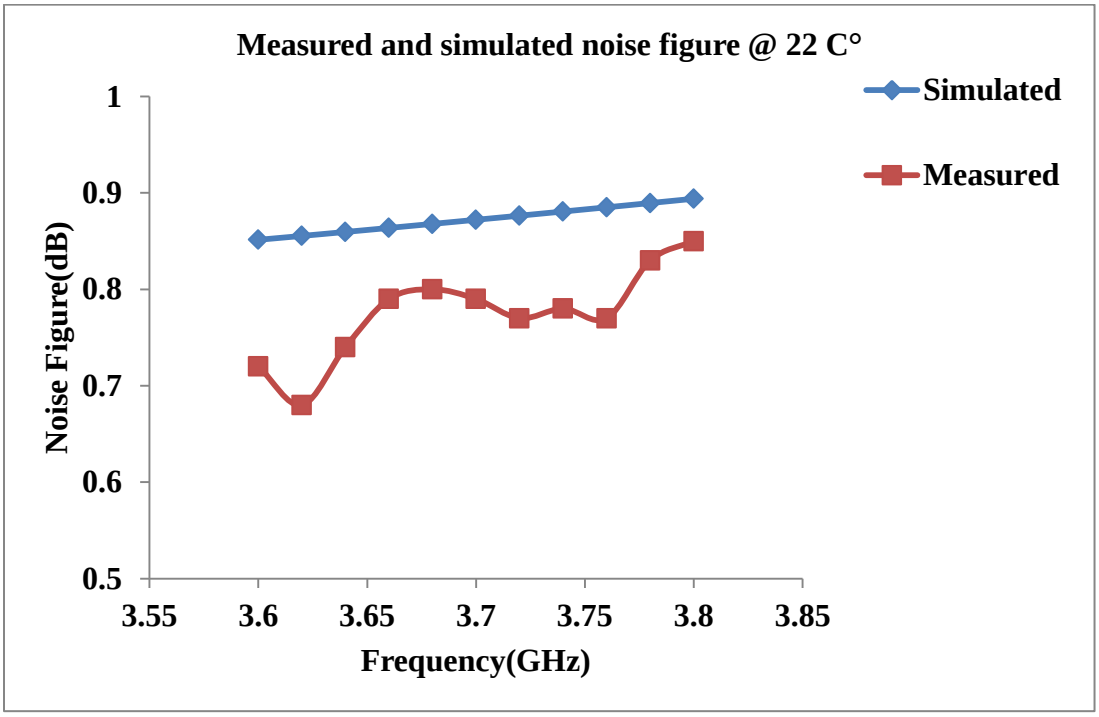


Figure 53- Simulated and measured noise figure of 3.7 GHz LNA

0.85 dB of maximum noise figure is measured throughout the 3.6 to 3.8 GHz band.

6.4- Summary

The specifications which were set at the start of the thesis work and achieved measured results are summarized in Table 7.

Parameters	Specifications	Measured Results	
V_{cc} [V]	3 – 5	5	
I_c [mA]	50	15	
Bandwidth [GHz]	3.4 – 3.8	3.4 – 3.6	3.6 – 3.8
Noise Figure [dB]	< 1 @ 100 Cº	0.78 @ 22 Cº	0.85 @ 22 Cº
Gain [dB]	> 17	> 17	> 16.5
S11 [dB]	< - 20	< -21	< -14
S22 [dB]	< - 15	< -4	< -5
Reverse Isolation [dB]	< -30	< -32	< -28
P1dB [dBm]	> -7	-10	-7.2
IIP3 [dBm]	> 0	0	2.65
Gain Flatness [dB]	1	< 1	< 1

Table 7- Summary of specifications and achieved results for the thesis work

It can be seen that most of the specifications which were set for the present work were met apart from the output return loss and P1dB compression point targets. A detailed discussion about the work done and achieved results will be done in next chapter.

Chapter 7

Conclusion and Future work

7.1- Conclusions

In this thesis work, LTE band of 3.4 GHz – 3.8 GHz was investigated with intention of designing small signal LNA for future mobile communication transceiver front end systems. After through study of literature about LNAs topologies, cascode configuration with capacitive shunt feedback was implemented in this work. Two LNAs each having bandwidth of 200 MHz around center frequencies of 3.5 GHz and 3.7 GHz were designed, fabricated and measured to cover the whole intended 3.4 GHz – 3.8 GHz band.

The new approach of symmetrical placement of RF components around the GSG domain along with separate RF and DC ground domains was implemented. The clear return ground path for RF current was defined on chip to ensure that RF current will flow via it rather than taking the substrate ground plane path between RF output and input bond pads. The good agreement between simulated and measured results validated this approach. The feedback capacitor and emitter degeneration inductor were found to be the most critical components in order to ensure stability along with achieving excellent input return loss, noise figure and linearity. From Table 7, it can be seen that the most of the target specifications were met with power consumption of 75 mw. It is mainly due to this low power consumption that it was not possible to cover the whole frequency band of 3.4 GHz – 3.8 GHz with just one LNA fulfilling the required parameters performance. In order to have one LNA covering the whole 400 MHz bandwidth, schematic level investigations were done and promising simulation results were obtained but at the cost of more than twice of power consumption compared to the comparatively narrowband 200 MHz bandwidth LNAs. Therefore, it can be concluded that bandwidth improvement comes at a cost of more power consumption.

7.2- Future Work

The measurements were performed on the wafer level without including the IC package model. The circuits were optimized including the package model bond wire inductances; therefore, it is strongly believed that results with packaging will further improve compared to the reported results in this report. Thus, packaging the designed circuits and performing measurements are needed to be done. Furthermore, since output return loss is not really good and even though LNA will be used together with VGA which might result in improved output return loss, there is still need of further investigation on how to improve it. The external biasing was used throughout this

work both during simulations and measurements. Thus, there is a need to design on chip biasing circuit. Last but not least, layout of the single LNA covering 3.4 GHz – 3.8 GHz band is required to be carried out for fabrication and measurements since schematic level simulations have shown extremely promising results.

References

[1] R. G. Meyer and W. D. Mack, “A 1-GHz Bi-CMOS RF front-end IC”, IEEE J. Solid-State Circuits, vol. 29, pp. 350-355, Mar. 1994.

[2] C.-Y. Wu and S.-Y. Hsio, “The design of a 3- V 900-MHz CMOS bandpass amplifier,” IEEE J. Solid-State Circuits, vol. 32, pp. 159-168, Feb. 1997.

[3] J. A. Macedo and M. A. Copeland, “A 1.9-Ghz silicon receiver with monolithic image filtering,” IEEE J. Solid-State Circuits, vol. 33, pp. 378-386, Mar. 1998.

[4] A. R. Shahani, D. K. Shaeffer, and T. H. Lee, “A 12-mW wide dynamic range CMOS front-end for portable GPS receiver,” IEEE J. Solid-State Circuits, bol. 32, pp. 2061-2070, Dec. 1997.

[5] www.cadence.com

[6] Pawlikiewicz, Adam H. and David Hess, “Choosing RF CMOS or SiGe BiCMOS in mixed-signal design”, www.rfdesign.com, pp. 36-44, Mar. 2006.

[7] www.eng.auburn.edu

[8] M.wilson, “GaAs and SiGe cost comparisons-Is SiGe always cheaper?,” in proc. IEEE 2003 int. Conf. Compound Semiconductor Manufacturing Technology, Scottsdale, AZ, May 2003.

[9] A. Podell, “GaAs…The Technology of the Future, Future, Future”, Proceedings of The IEEE GaAs IC Symposium, Montery, CA, Oct. 17 to 20, 1999, pg. 3-6.

[10] G. Bechtel, “The 1999 Outlook for GaAs IC Markets and Technology”, Proceedings of The IEEE GaAs IC Symposium, Montery, CA, Oct. 17 to 20, 1999, pg. 7-9.

[11] S. E. Gunnarsson et al., “60 GHz single-chip front-end MMICs and systems for multi-Gb/s wireless communication,” IEEE J. Solid-State Circuits, vol. 42, no. 5, pp. 1143–1157, May 2007.

[12] D. Barlas, “Application of Silicon-Germanium Technology for Wireless Handsets: A CDMA Tri-mode Chip Set”, Proceedings of The IEEE GaAs IC Symposium, Baltimore, MD, Oct. 21 to 24, 2001, pg. 29-32.

[13] V. Ilderem, et. al., “The Emergence of SiGe:C HBT Technology for RF Applications”, to be published in the Proceedings of the 2003 International Conference on Compound Semiconductor Manufacturing Technology, Scottsdale, AZ, May 19 to 22, 2003, pg. TBD.

[14] “QUBiC4 Design Platform Manual”, www.collabnet.nxp.com

[15] “QUBiC4 Device Document, bny-BNY NPN Transistor, Version 3.0, January 2013”, www.collabnet.nxp.com

[16] “QUBiC4Xi Design Manual, Version 3.03, March 2013”, www.collabnet.nxp.com

[17] I. Rosu, “LNA Design” http://www.qsl.net/va3iul/LNA%20design.pdf (Acc. "October 2013").

[18] David.M.Pozar, “Microwave and RF Design of Wireless Systems, John Wiley & Sons, Ltd., 2000, pg. 102.”

[19] S. Hazenboom, et al; "A Comparison of Substrate Noise Coupling in Lightly and Heavily Doped CMOS Processes for 2.4-GHz LNAs"; IEEE JSSC, Vol. 41, No. 3, Mar. 2006; pp. 574 – 587.

[20] D. J. Cassan, J. R. Long; "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS"; IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, March 2003; pp. 427 – 435.

[21] B. Godara, A. Fabre; "State of the art Low-Noise Amplifiers in wireless transceivers; Two new wideband all-active LNAS in SiGe-BiCMOS Technology"; Laboratoire IMS, Universite Bordeaux 1, Talence, France.

[22] A. M. P. George D. Vendelin and U. L. Rohde, "Microwave Circuit Design Using Linear and Nonlinear Techniques"; Wiley-interscience, 2005.

[23] I. Bahl, "Lumped Elements for RF and Microwave Circuits"; Artech House, inc., 2003.

[24] D.K. Shaeffer and T.H. Lee, "A 1.5-V, 1.5-GHzz CMOS low noise amplifier," IEEE J.Solid-State Circuits, vol. 32, pp. 745-759, May1997.

[25] Sedra Smith, "Microelectronics circuits, 5th edition"; OXFORD UNIVERSITY PRESS 2004.

[26] B. Kang, J. Yu, H. Shin, S.Ko, W. Ko, S. Yang, W. Choo, B. Park; "Design and Analysis of a Cascode Bipolar Low-Noise Amplifier with Capacitive Shunt Feedback under Power-Constraint"; IEEE Transactions on Microwave Theory and Techniques, Vol. 59, No. 6, June 2011; pp. 1539-1551.

[27] www.cascademicrotech.com

APPENDIX A

Cascode small signal model derivations

A.1- Input impedance derivation

The small signal hybrid-π model of CE stage in a cascode amplifier with emitter degeneration including parasitics is presented in following Figure.

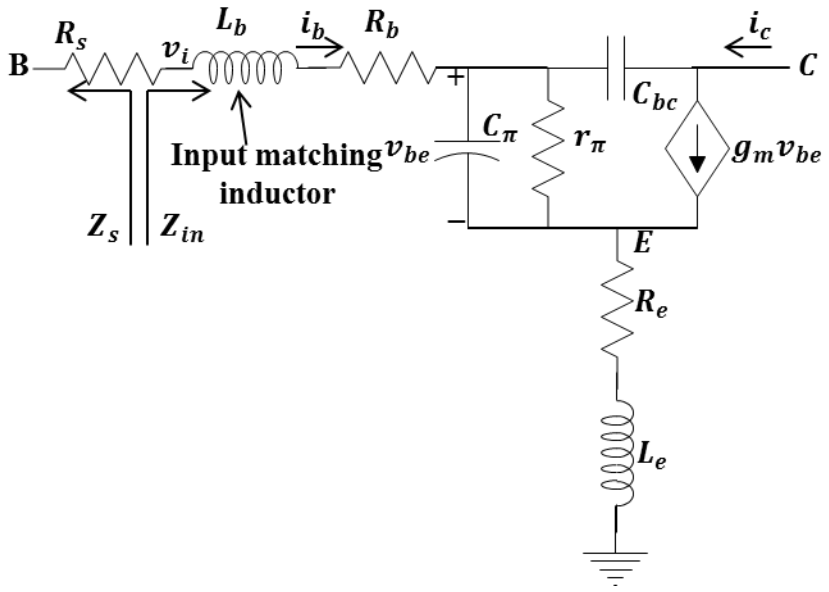


Figure 54- Small signal hybrid-π model of CE stage including parasitics

I have done the analysis without including collector-base capacitance C_{bc} for simplification purpose. The input impedance Z_{in} then can be written as

$$Z_{in} = R_b + Z_\pi + Z_e(1 + Z_\pi g_m)$$

$$Z_{in} = R_b + \underbrace{r_\pi \| C_\pi}_{Z_\pi} + Z_e(1 + Z_\pi g_m)$$

$$Z_{in} = R_b + \underbrace{\frac{r_\pi}{1 + j\omega C_\pi r_\pi}}_{r_\pi \| C_\pi} + Z_e(1 + \underbrace{\frac{r_\pi}{1 + j\omega C_\pi r_\pi}}_{Z_\pi} g_m)$$

$$Z_{in} = R_b + \underbrace{\frac{1}{j\omega C_\pi}}_{Since\ \omega \gg 1} + Z_e\left(1 + \underbrace{\frac{g_m}{j\omega C_\pi}}_{Since\ \omega \gg 1}\right)$$

$$Z_{in} = R_b + \frac{1}{j\omega C_\pi} + \underbrace{R_e + j\omega L_e}_{Z_e}\left(1 + \frac{g_m}{j\omega C_\pi}\right)$$

$$Z_{in} = R_b + \frac{1}{j\omega C_\pi} + R_e + j\omega L_e + R_e\frac{g_m}{j\omega C_\pi} + j\omega L_e\frac{g_m}{j\omega C_\pi}$$

$$Z_{in} = R_b + R_e + j\omega L_e + \frac{1}{j\omega C_\pi}(1 + R_e g_m) + \underbrace{\frac{g_m}{C_\pi}}_{\omega_T} L_e$$

$$Z_{in} = R_b + R_e + \omega_T L_e + j\omega L_e + \frac{1}{j\omega C_\pi}(1 + R_e g_m)$$

$$\boldsymbol{Z_{in} = \underbrace{R_b + R_e + \omega_T L_e}_{Real\ Part} + \underbrace{j\omega L_e + \frac{1 + g_m R_e}{j\omega C_\pi}}_{Imaginary\ Part}}$$

The base inductor $L_b$is tuned to cancel out the imaginary part and by equating real part to 50Ω; we get following relation for degeneration inductor

$$\boldsymbol{L_e = \frac{50 - (R_b + R_e)}{\omega_T}}$$

A.2- Noise figure derivation

The small signal noise model of CE stage with emitter degeneration of cascode amplifier is shown below. The contribution from the source internal noise, base thermal, base shot and collector shot noise in overall noise figure is calculated analytically with assumptions that all noise terms are statistically independent i.e. uncorrelated.

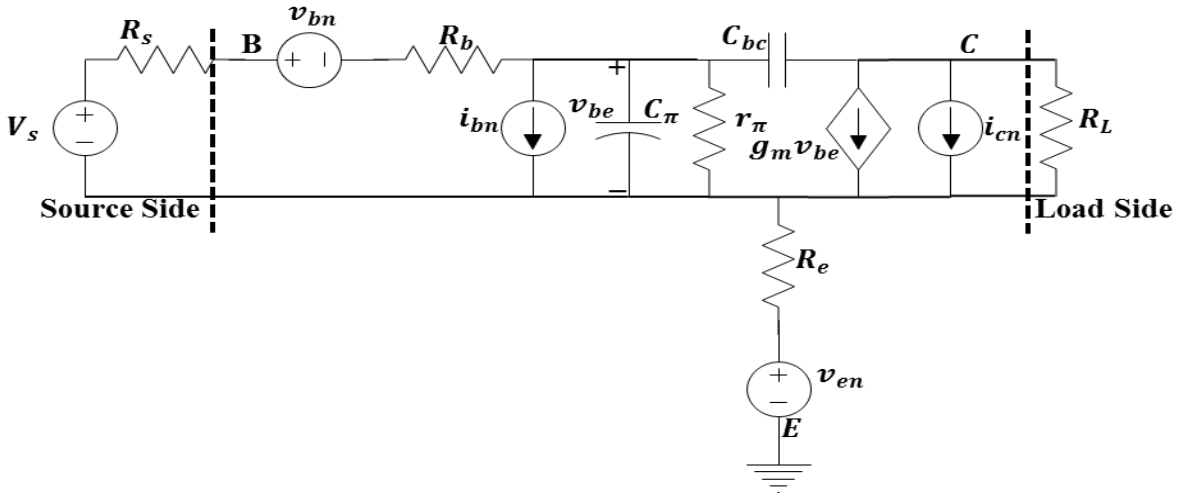


Figure 55- Small signal noise model of CE stage with emitter degeneration

I have not included the collector-base capacitance C_{bc} in analysis for simplification purpose. Also, first noise figure expression is derived without considering emitter resistance R_e and its contribution is included in the end.

Some small signal parameters and their relations and noise relations both for voltage and current sources are

$$r_e = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

$$r_\pi = (\beta + 1) r_e \approx \beta r_e$$

$$V_s = \underbrace{\sqrt{4KTR_s\Delta f}}_{rms\ noise\ voltage} = \underbrace{\sqrt{4KTR_s}}_{Noise\ voltage\ spectral\ density} \qquad (V/\sqrt{Hz})$$

$$V_b = \sqrt{4KTR_b}$$

$$i_{bn} = \sqrt{2qI_b\Delta f} = \sqrt{2qI_b}$$

$$i_{cn} = \sqrt{2qI_c}$$

a) Noise contribution at output due to source:

$$v_{out} = g_m v_{be} R_L$$

$$v_{out} = g_m R_L V_s \frac{r_\pi}{\underbrace{r_\pi + R_s + R_b}_{v_{be}}} = \overbrace{\frac{1}{r_e}}^{g_m} R_L \overbrace{\sqrt{4KTR_s}}^{V_s} \frac{\overbrace{\beta r_e}^{r_\pi}}{\underbrace{\beta r_e}_{r_\pi} + R_s + R_b}$$

$$P_{out} = \frac{{v_{out}}^2}{R_L} = 4KTR_s \left[\frac{\beta}{\beta r_e + R_s + R_b}\right]^2 R_L \qquad \text{i)}$$

b) Noise contribution at output due to base thermal noise:

Same analysis as above yields the following expression

$$P_{out} = \frac{{v_{out}}^2}{R_L} = 4KTR_b \left[\frac{\beta}{\beta r_e + R_s + R_b}\right]^2 R_L \qquad \text{ii)}$$

c) Noise contribution at output due to base shot noise:

$$v_{out} = v_{be} g_m R_L$$

$$v_{out} = \overbrace{i_{bn}[(R_s + R_b) \| (r_\pi \| C_\pi)]}^{v_{be}} g_m R_L$$

$$v_{out} = i_{bn}\left[(R_s + R_b)\| \underbrace{\frac{r_\pi}{1 + j\omega C_\pi r_\pi}}_{r_\pi \| C_\pi}\right] g_m R_L$$

$$v_{out} = i_{bn}\left[(R_s + R_b)\| \underbrace{r_\pi}_{since\ \omega \ll 1}\right] g_m R_L$$

$$v_{out} = i_{bn}\left[\frac{(r_\pi)(R_s + R_b)}{R_s + R_b + r_\pi}\right] g_m R_L$$

$$v_{out} = \underbrace{\sqrt{2qI_b}}_{i_{bn}}\left[\frac{\overbrace{\beta r_e}^{r_\pi}(R_s + R_b)}{R_s + R_b + \underbrace{\beta r_e}_{r_\pi}}\right]\underbrace{\frac{1}{r_e}}_{g_m} R_L$$

$$P_{out} = \frac{{v_{out}}^2}{R_L} = 2qI_b[R_s + R_b]^2\left[\frac{\beta r_e}{R_s + R_b + \beta r_e}\frac{1}{r_e}\right]^2 R_L$$

$$P_{out} = 2q\underbrace{\frac{I_c}{\beta}}_{I_b}[R_s + R_b]^2\left[\frac{\beta}{R_s + R_b + \beta r_e}\right]^2 R_L$$

$$P_{out} = 2q\frac{\overbrace{KT/qr_e}^{I_c \approx I_e}}{\beta}[R_s + R_b]^2\left[\frac{\beta}{R_s + R_b + \beta r_e}\right]^2 R_L$$

$$P_{out} = 2\frac{KT}{r_e\beta}[R_s + R_b]^2\left[\frac{\beta}{R_s + R_b + \beta r_e}\right]^2 R_L \qquad \text{iii)}$$

d) Noise contribution at output due to collector shot noise:

$$v_{out} = i_{cn}R_L = \overbrace{\sqrt{2qI_c}}^{i_{cn}} R_L$$

$$P_{out} = \frac{{v_{out}}^2}{R_L} = 2qI_cR_L = 2q\underbrace{\frac{KT}{qr_e}}_{I_c \approx I_e}R_L$$

$$P_{out} = \frac{2KT}{r_e}R_L \qquad \text{iv)}$$

The overall noise figure is calculated by using Equations i)-iv) as follows

$$F = \frac{Total\ noise\ power\ at\ output\ with\ noisy\ device}{Total\ noise\ power\ at\ output\ with\ noiseless\ device} = \frac{Eqs\ i) + ii) + iii) + iv)}{Eq\ i)}$$

$$\boldsymbol{F = \underbrace{1}_{Source\ term} + \underbrace{\frac{R_b}{R_s}}_{Base\ thermal\ noise\ term} + \underbrace{\frac{1}{2\beta r_e}\frac{[R_s + R_b]^2}{R_s}}_{Base\ shot\ noise\ term} + \underbrace{\frac{r_e}{2R_s}\left[\frac{\beta r_e + R_s + R_b}{\beta r_e}\right]^2}_{Collector\ shot\ noise\ term}}$$

Now, if we include the emitter resistance $R_e$and redo the same analysis again we will end up with the following equation which clearly shows that instead of just $R_b$we get $R_b + R_e$in above equation.

$$\boldsymbol{F = \underbrace{1}_{Source\ term} + \underbrace{\frac{R_b + R_e}{R_s}}_{Base\ thermal\ noise\ term} + \underbrace{\frac{1}{2\beta r_e}\frac{[R_s + R_b + R_e]^2}{R_s}}_{Base\ shot\ noise\ term} + \underbrace{\frac{r_e}{2R_s}\left[\frac{\beta r_e + R_s + R_b + R_e}{\beta r_e}\right]^2}_{Collector\ shot\ noise\ term}}$$

APPENDIX B

Schematic simulation results

B.1- 3.5 GHz compliance table

Parameters	**Conditions**	**Without Package IC model**			**With Package IC model**		
Temperature		-40 Cº	27 Cº	100 Cº	-40 Cº	27 Cº	100 Cº
V_{cc} [V]	5						
I_c [mA]	15						
Bandwidth [GHz]	3.4-3.6						
Stability	US						
Noise Figure [dB]		0.5	0.7	1.1	0.53	0.75	1.15
S11/S22 [dB]		-19.4 /-8.6	-18.5 /-8.8	-17.3 /-9.1	-34 /-9.7	-33 /-9.9	-29 /-10
S21/S12 [dB]		19.1 /-29.9	18.8 /-30.1	18.2 /-30.5	18.9 /-28.6	18.6 /-28.7	18 /-29
IIP3 [dBm]		-9.1	-8.3	-7.4	-2.5	2.8	2.9
P1dB [dBm]		-	-	-	-10.7	-10.6	-10.1
Gain Flatness [dB]		<1			<1		

Table 8- 3.5GHz LNA schematic version simulation results over temperature variation

B.2- 3.7 GHz compliance table

Parameters	Conditions	Without Package IC model			With Package IC model		
Temperature		-40 Cº	27 Cº	100 Cº	-40 Cº	27 Cº	100 Cº
V_{cc} [V]	5						
I_c [mA]	15						
Bandwidth [GHz]	3.6-3.8						
Stability	US						
Noise Figure [dB]		0.54	0.78	1.21	0.56	0.79	1.22
S11/S22 [dB]		-12 /-9	-11.6 /-9.2	-11.3 /-9.8	-17 /-10.6	-16.3 /-11.2	-16 /-11.8
S21/S12 [dB]		17.1 /-26.6	16.8 /-27	16.4 /-27.02	17.07 /-26	16.8 /-25.4	16.3 /-26
IIP3 [dBm]		-4.6	-3.7	-2.9	1.1	5.7	8.5
P1dB [dBm]		-	-	-	-7	-6.8	-6.6
Gain Flatness [dB]		<1			<1		

Table 9- 3.7 GHZ LNA schematic version simulation results over temperature variation

B.3- 3.4-3.8 GHz variant schematic simulation results

The simulation results presented here are on schematic level including the package IC model at room temperature of 27 Cº.

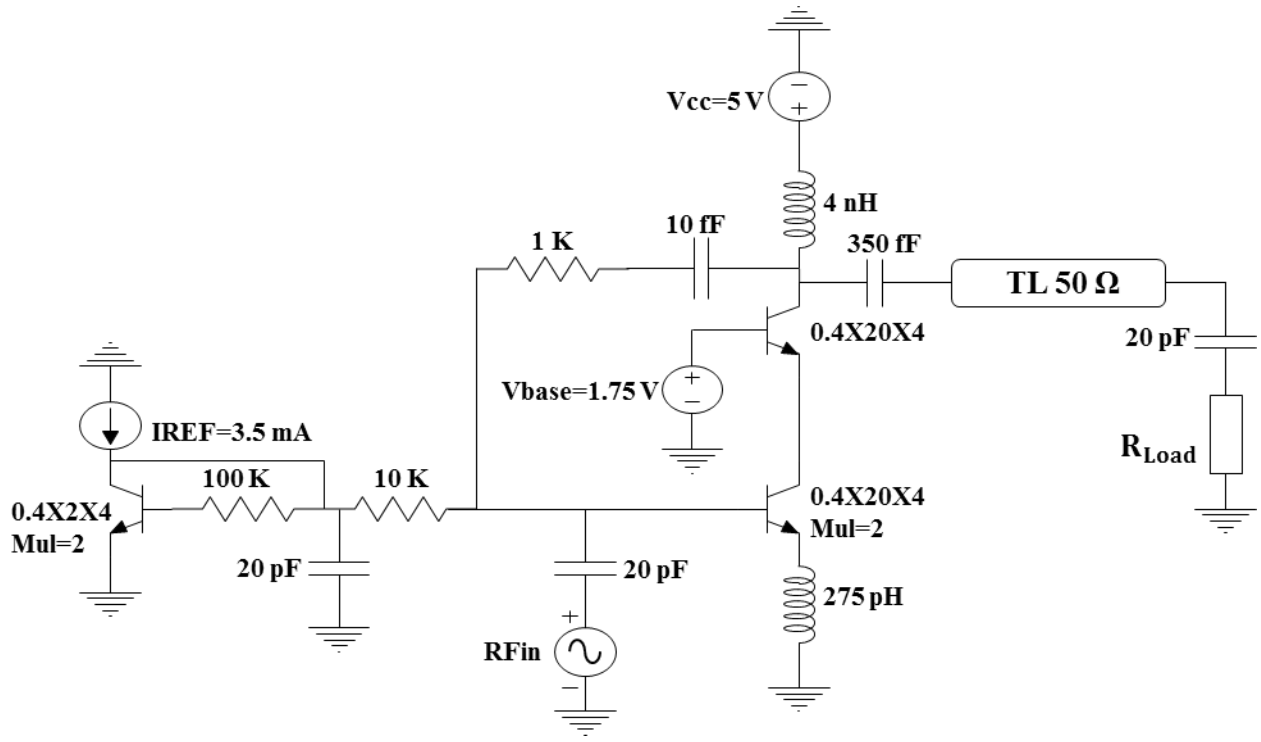


Figure 56- Circuit block diagram with component parameter values for 3.4 GHz – 3.8 GHz band

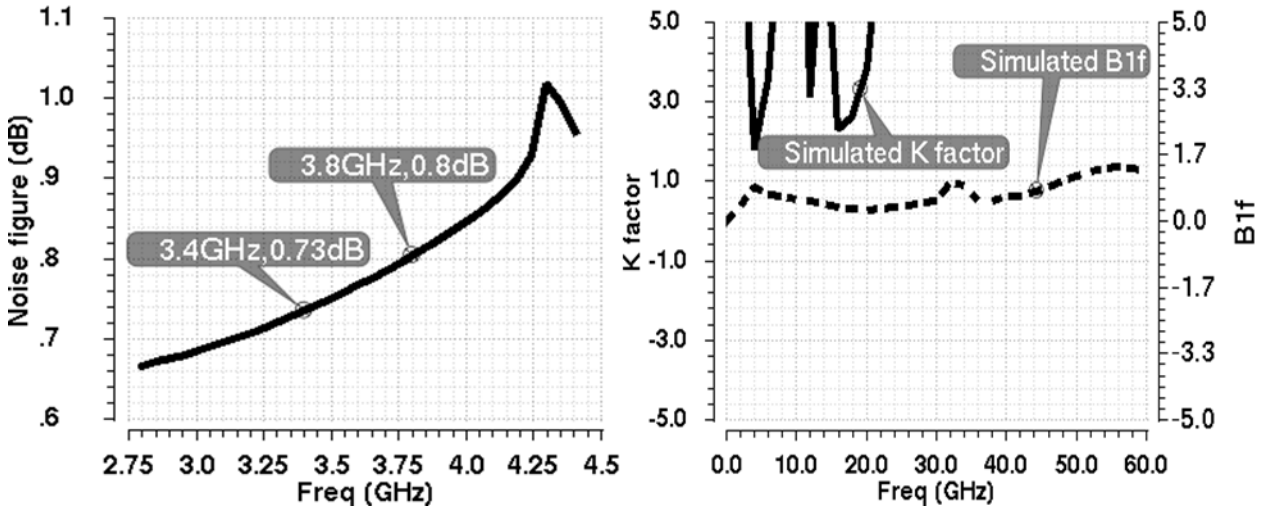


Figure 57- Stability and noise figure simulation results

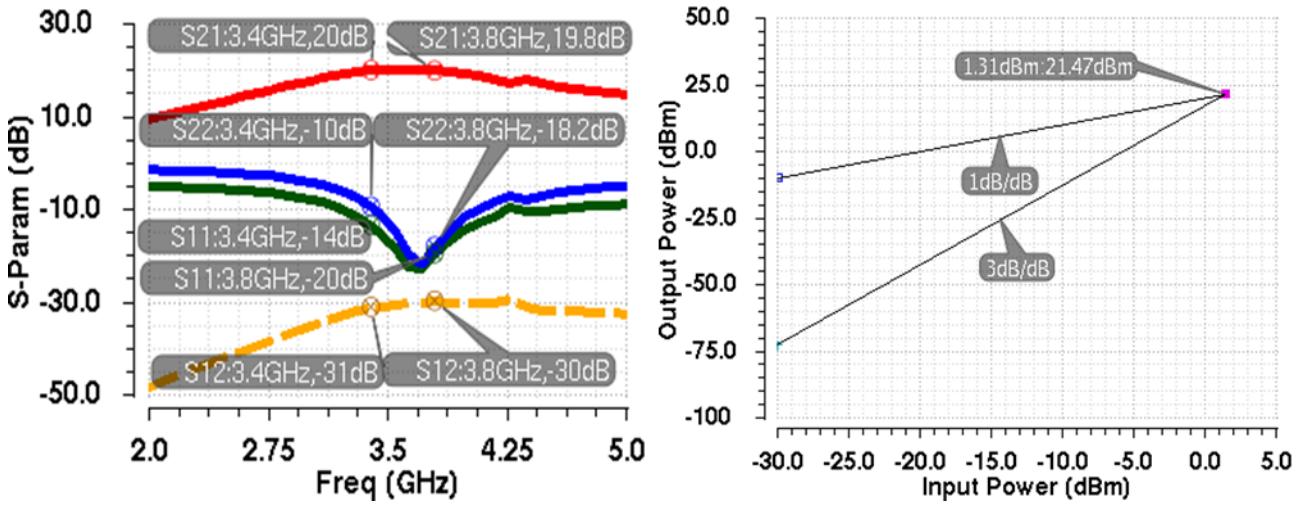


Figure 58- S-Parameters and IIP3 point simulation results

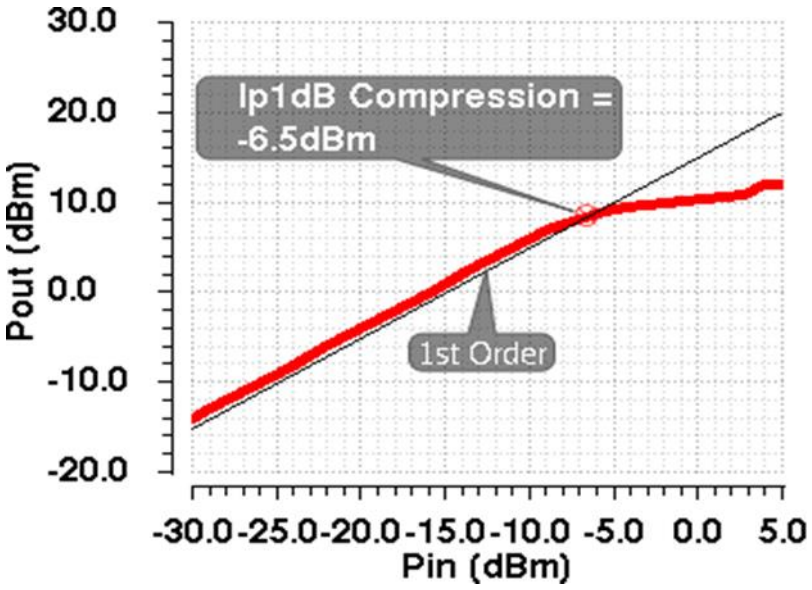


Figure 59- P1dB compression point simulation result

APPENDIX C

Extracted simulation results

C.1- 3.5 GHz compliance table

Parameters	**Conditions**	**Without Package IC model**			**With Package IC model**		
Temperature		-40 Cº	27 Cº	100 Cº	-40 Cº	27 Cº	100 Cº
V_{cc} [V]	5						
I_c [mA]	15						
Bandwidth [GHz]	3.4-3.6						
Stability	US						
Noise Figure [dB]		0.59	0.84	1.2	0.61	0.86	1.26
S11/S22 [dB]		-25 /-6	-24.5 /-5.6	-22 /-5.7	-22 /-6.2	-27.3 /-6.23	-31 /-6.2
S21/S12 [dB]		17.2 /-32	16.9 /-31.6	16.5 /-32	17.2 /-29.8	17 /-29.9	16.5 /-30.2
IIP3 [dBm]		-7.8	-7	-6.1	0.213	8.4	4.8
P1dB [dBm]		-	-	-	-9.7	-9.5	-9.2
Gain Flatness [dB]		<1			<1		

Table 10- 3.5 GHz LNA extracted version simulation results over temperature variation

C.2- 3.7 GHz compliance table

Parameters	Conditions	Without Package IC model			With Package IC model		
Temperature		-40 Cº	27 Cº	100 Cº	-40 Cº	27 Cº	100 Cº
V_{cc} [V]	5						
I_c [mA]	15						
Bandwidth [GHz]	3.6-3.8						
Stability	US						
Noise Figure [dB]		0.63	0.89	1.32	0.64	0.9	1.34
S11/S22 [dB]		-15 /-7	-14 /-7.3	-13 /-7.8	-19 /-8.2	-17 /-8.4	-16 /-8.8
S21/S12 [dB]		16.1 /-28	16 /-27.6	15.6 /-27.9	16.1 /-26.3	16 /-26.4	15.6 /-26.6
IIP3 [dBm]		-4.3	-3.4	-2.6	2.8	8.3	10.3
P1dB [dBm]		-	-	-	-6.6	-6.5	-6.3
Gain Flatness [dB]		<1			<1		

Table 11- 3.7 GHz LNA extracted version simulation results over temperature variation