THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Extending the Bandwidth of the Doherty Power Amplifier

DAVID GUSTAFSSON



Microwave Electronics Laboratory Department of Microtechnology and Nanoscience – MC2 Chalmers University of Technology Gothenburg, Sweden, 2014

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Microwave Electronics Laboratory Department of Microtechnology and Nanoscience – MC2 Chalmers University of Technology SE-412 96 Gothenburg, Sweden Phone: +46 (0) 31 772 1000

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Abstract

The Doherty power amplifier (DPA) is one of the most popular power amplifier (PA) architectures used to obtain high efficiency for modern communication signals having high peak-to-average power ratios. Its often narrowband performance does, however, make it difficult for the DPA to meet the increasing demands of frequency agility in modern wireless communication systems. This thesis examines the theoretical and practical bandwidth limitations of the DPA and presents new methods to overcome them.

A new type of output network topology that serves to reduce the influence of device output parasitics and to overcome manufacturing limitations, thereby extending the bandwidth, is proposed. The utility of the network is demonstrated by implementation in a gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) DPA. Measurements show that by doing so, a power added efficiency (PAE) higher than 30% at 9 dB output power back-off (OPBO) is obtained across a 6.7–7.8 GHz frequency range.

To overcome the inherent bandwidth limitations imposed by the impedance inverter, a modified DPA is proposed. A comprehensive theoretical analysis is presented which shows that the modified DPA has a significantly larger bandwidth compared to the standard DPA, as well as reconfigurable efficiency. The theoretical findings are validated by the design and characterization of two demonstrator circuits. The first circuit, having dual RF-inputs and using baredie GaN devices, has a drain efficiency higher than 48 % at both full output power and at 6 dB OPBO across a 1.5–2.4 GHz frequency range. The second circuit is a single RF-input GaN MMIC DPA that delivers a PAE higher than 30% at 9 dB OPBO from 5.8 to 8.8 GHz, constituting a fractional bandwidth of 41%.

To achieve bandwidths greater than one octave, a linear multi-harmonic analysis method based on a Doherty-outphasing continuum is proposed. By using this method a dual RF-input amplifier is designed. Measurements show that the amplifier provides more than 45% PAE at 6 dB OPBO over a 1.0– 3.0 GHz frequency range, corresponding to a 100% fractional bandwidth.

In summary, the results presented in this thesis shows that the DPA no longer needs be considered as a necessarily narrowband amplifier. This thesis is therefore an important contribution in the pursuit of high efficiency and frequency agile power amplifiers targeting the needs in future mobile communication systems.

Keywords: Broadband amplifiers, Doherty, gallium nitride, GaN, high efficiency, microwave, MMIC, power amplifier, wideband

List of Publications

Appended Publications

This thesis is based on the following papers:

- [A] D. Gustafsson, J. Chani Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A Wideband and Compact GaN MMIC Doherty Amplifier for Microwave Link Applications," *IEEE Transactions on Mi*crowave Theory and Techniques, vol. 61, no. 2, pp. 922–930, February, 2013.
- [B] D. Gustafsson, C. M. Andersson, and C. Fager, "A Modified Doherty Power Amplifier With Extended Bandwidth and Reconfigurable Efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 533–542, January, 2013.
- [C] D. Gustafsson, J. Chani Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC Modified Doherty PA with Large Bandwidth and Reconfigurable Efficiency," submitted to *IEEE Transactions on Mi*crowave Theory and Techniques, July 2014.
- [D] D. Gustafsson, C. M. Andersson, R. Hellberg, and C. Fager, "A 44 dBm 1.0–3.0 GHz GaN Power Amplifier with over 45% PAE at 6 dB Back-Off," *IEEE MTT-S International Microwave Symposium*, Seattle, U.S.A., June, 2013.
- [E] C. M. Andersson, D. Gustafsson, J. Chani Cahuana, R. Hellberg, and C. Fager, "A 1–3 GHz Digitally Controlled Dual-RF Input Power-Amplifier Design Based on a Doherty-Outphasing Continuum Analysis," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3743–3752, October, 2013.

Other Publications

The following papers have been accepted for publication but are not included in the thesis. The content partially overlaps with the appended papers or is out of the scope of this thesis.

- [a] D. Gustafsson, C. M. Andersson, and C. Fager, "A Novel Wideband and Reconfigurable High Average Efficiency Power Amplifier," *IEEE MTT-S International Microwave Symposium*, Montreal, Canada, June, 2012.
- [b] C. M. Andersson, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, "Theory and Design of Class-J Power Amplifiers with Dynamic Load Modulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 3778–3786, December, 2012.
- [c] D. Gustafsson, C. M. Andersson, and C. Fager, "An analysis of the suitability of using CW-theory when designing Doherty PAs for wideband or concurrent multi-band operation," *IEEE European Microwave Conference*, Nürnberg, Germany, October, 2013.
- [d] C. M. Andersson, M. Özen, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, "A Packaged 86 W GaN Transmitter with SiC Varactor-Based Dynamic Load Modulation," *IEEE European Microwave Conference*, Nürnberg, Germany, October, 2013.
- [e] J. Chani Cahuana, P. Landin, D. Gustafsson, C. Fager, and T. Eriksson "Linearization of Dual-Input Doherty Power Amplifiers," *IEEE Interna*tional workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Leuven, Belgium, April, 2014.

Patents

- [f] D. Gustafsson, and C. Fager, "Wideband and Reconfigurable Doherty Based Amplifier," WO2012149976 A1, 5 May, 2011.
- [g] C. M. Andersson, and D. Gustafsson, "High Efficiency Wideband Dynamic Load Modulation Power Amplifier Architecture" WO2013174411 A1, 21 May, 2012.

Theses

[h] D. Gustafsson, Theory and Design of Wideband Doherty Power Amplifiers, Gothenburg: Chalmers University of Technology, 2012, (Thesis for the degree of tekn.lic.).

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [h]. Figures, tables and text in [h] might therefore be fully or partly reproduced in this thesis.

Notations and abbreviations

Notations

| C_{out} | Device effective output capacitance |
|----------------|--|
| f | Frequency |
| \overline{f} | Normalized frequency |
| g_m | Device transconductance |
| I_a | Auxiliary amplifier output current |
| I_m | Main amplifier output current |
| Imax | Device maximum current |
| P_{BO} | Efficiency-peak back-off level |
| P_{DC} | Amplifier DC power consumption |
| P_{max} | Amplifier peak output power |
| P_{out} | Amplifier output power |
| R_L | Amplifier load resistance |
| R_{opt} | Class-B output power optimal load resistance |
| V_a | Auxiliary amplifier output voltage |
| V_{DS} | Device drain-to-source bias voltage |
| V_{GS} | Device gate-to-source bias voltage |
| V_k | Device knee-voltage |
| V_m | Main amplifier output voltage |
| V_T | Device threshold voltage |
| Z_C | Impedance inverter characteristic impedance |
| β | Input network amplitude balance |
| η | Drain efficiency |
| θ | Transmission line electrical length |
| ξ | Drive level |
| ξ_b | Drive level at onset of auxiliary amplifier |
| ρ | Signal probability density function |
| ϕ | Phase difference between the sub-amplifier output currents |
| ω | Angular frequency |

Abbreviations

| ACPR | Adjacent Channel Power Ration |
|---------------------|---|
| ALM | Active Load Modulation |
| CW | Continuous Wave |
| DC | Direct Current |
| DLM | Dynamic Load Modulation |
| DPA | Doherty Power Amplifier |
| EA | Envelope Amplifier |
| EER | Envelope Elimination and Restoration |
| ET | Envelope Tracking |
| GaN | Gallium Nitride |
| GMSK | Gaussian Minimum Shift Keying |
| GSM | Global System for Mobile Communications |
| HEMT | High Electron Mobility Transistor |
| LTE | Long Term Evolution |
| IMT | International Mobile Telecommunications |
| IP | Internet Protocol |
| ITU-R | International Telecommunication Union Radiocommunication sector |
| METIS | Mobile and wireless communications Enablers |
| | for Twenty-twenty (2020) Information Society |
| MIMO | Multiple Input Multiple Output |
| MMIC | Monolithic Microwave Integrated Circuit |
| NMSE | Normalized Mean Square Error |
| OPBO | Output Power Back-Off |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PAPR | Peak to Average Power Ratio |
| PDF | Probability Density Function |
| PTP | Point-To-Point |
| QAM | Quadrature Amplitude Modulation |
| QL | Quasi-Lumped |
| QFN | Quad-Flat No-leads |
| RBS | Radio Base Station |
| RF | Radio Frequency |
| VS-GMP | Vector Switched Generalized Memory Polynomial |
| WCDMA | Wideband Code Division Multiple Access |

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Chapter 1

Introduction

I remember how I as a young boy in the late 1980's tried to figure out what would be the next great invention. There were already TV, cars, video games, VCRs, airplanes, space rockets, and for a young boy it seemed like everything was invented. I was therefore proud when I told my mother that I had found an answer to my broodings; In the future everybody will have cable-TV. I don't remember if this was the result of a well-reasoned analysis or a manifest of my jealousness of my friends who always could watch the latest cartoons on their cable network. No matter what the reason was, the prediction was not that bad. The big invention was about to become known for the public, and one could say that cable-tv for everybody was part of it, it was an invention that would revolutionize how we create, share, and consume information, it was the Internet and the World Wide Web.

The introduction of the Internet and how it impacts our lives did however not happen overnight. There has been an ongoing evolution from a slow network mainly used for sharing text into an orders of magnitude faster network that enables high definition video streaming, cloud sharing, computer gaming, social networking, etc. We are now experiencing what very well may be the next leap in the evolution of Internet as we move from fixed line connections into wireless and mobile access. Fig. 1.1 shows that from having been less than 1% up to 2010, mobile Internet Protocol (IP) traffic is expected to account for more than 10% of the total IP traffic in 2018. In absolute values, the mobile IP traffic has increased from 91 PB/month in 2009 to 1487 PB/month in 2013 and is expected to exceed 15800 PB/month in 2018, that is 173 times more than in 2009 [1–7]. There is no doubt that such an evolution will enable inventions and applications that a young boy, despite loads of imagination, could not even dream of 25 years ago.

An important factor that has driven the rapid increase of the mobile data traffic is the introduction of portable devices such as smart phones and tablets. Many of these devices are however not utilized to their full capacity, often due to slow connections but also due to the data limitations many telecom operators have introduced to avoid overloading their networks. It is therefore reasonable to believe that the demand for mobile data is significantly larger than what can be supplied and that it is the capacity and speed of the mobile infrastructure that determines the amount of mobile data that is consumed.



Figure 1.1: Development and prediction of total amount of IP traffic and mobile IP traffic share of total IP traffic [1-7].

The wireless connections, such as the wireless access between the user and the radio base station (RBS), and the wireless point-to-point (PTP) links used to transfer data between system nodes, are often identified as bottlenecks of the mobile infrastructure. Increasing the capacity and speed of these connections is therefore essential in order to reach the predictions of a continuously and rapidly growing mobile data traffic. Three main methods can be identified for enabling this: smaller cell sizes, larger bandwidths, and higher spectral efficiency [8]. As is discussed below, all these methods set new requirements on the power amplifier (PA) needed in all mobile communication transmitters to amplify the information carrying signal to its required power level.

Smaller cell sizes imply that more wireless transmitters must be deployed. To make such investments affordable the transmitters must be designed for low cost, small size, and low complexity. A key factor to obtain this is to reduce their energy consumption, thereby giving lower electricity bills for the operators and reduced hardware complexity since less care has to be taken to thermal management. Reduced energy consumption can also increase the use of "power over Ethernet" solutions or the use of local energy sources, such as solar cells, thereby simplifying installation in rural areas with deficient electrical power-infrastructure. There are also environmental and ecological reasons why the energy consumption should be low. In [9] it is reported that in 2007 mobile networks alone represented 0.2% of the global CO₂ equivalent emissions and it is estimated that this number will increase to 0.4% in 2020. Because of these reasons, $METIS^1$ has settled on an agreement that the future 5G systems should have "a similar cost and energy dissipation per area as in today's cellular systems" [10]. A true challenge considering the high data rates aimed for in 5G. At the same time, it has been shown that up to 40-60% of the total transmitter energy consumption can be attributed to the PA. Increasing the energy efficiency of the PA is therefore essential to reduce cost and complexity of present systems, to enable future standards, as well as to

¹METIS, (Mobile and wireless communications Enablers for Twenty-twenty (2020) Information Society), is a consortium of 29 partners coordinated by Ericsson AB and is co-funded by the European Commission. The project objective is to lay the foundation for a future mobile communications system for 2020 and beyond (5G).

limit the effect on the environment and climate (and possibly also to avoid bad publicity for the telecom industry).

Increasing the capacity by extending the bandwidth requires that the PA is wideband in the sense that it can work properly over the signal frequency band. Furthermore, the scarcity of the frequency spectrum and the need of frequency planning has resulted in a wide spread of carrier frequencies. For example, the 4G standard Long Term Evolution² (LTE) utilizes carrier frequencies ranging from 703 MHz to 3.8 GHz [12]. To keep the complexity of transmitters low it is therefore important that the PA is wideband also in the sense that it can support a diversity of carrier frequencies.

It should be noted that the two definitions of the term *wideband*, the ability to support a large signal bandwidth, and the ability to support carrier frequencies over a large frequency range, do not always coincide [c]. Throughout this thesis, if not else is stated, the latter definition is used.

Increased spectral efficiency means that more information can be transmitted over a given bandwidth. One method to obtain this is to use multiple transmitter and receiver antenna systems. One such method is multiple input multiple output (MIMO) which is integrated in the LTE standard where up to four transmitter and receiver units can be used in the downlink [13]. It is today speculated that massive MIMO, where possibly hundreds or even thousands of transmitter and receiver units are employed, will be an important part of coming 5G standards [14]. However, such solutions require that each unit has small size, low complexity and low cost which again necessitates energy efficient and wideband PAs.

The spectral efficiency can also be increased by employing higher order modulation formats. However, as is discussed in the next sections, increasing the order of the modulation format can have large impact on how the PA should be designed to fulfill the requirements of e.g. high energy efficiency and wideband performance.

1.1 High efficiency PA requirements

Fig. 1.2 shows the output power probability density functions (PDFs) of a Global System for Mobile Communications- (GSM), Wideband Code Division Multiple Access- (WCDMA), and LTE-signal³. Compared to the GSM-signal which has a constant signal amplitude, the amplitudes of the WCDMA and LTE-signals varies significantly. The reason for this is that the WCDMA and LTE-standards utilize Quadrature Amplitude Modulation (QAM) that, in contrast to the Gaussian Minimum Shift Keying (GMSK) modulation used in the GSM-standard, is both phase and amplitude modulated which increases the spectral efficiency [15–17].

Fig. 1.2 also shows how the drain efficiency, defined as the ratio of the

²Although LTE in its original release not fulfill the requirements for 4G specified in International Mobile Telecommunications-Advanced (IMT-Andvanced), the International Telecommunication Union Radiocommunication Sector (ITU-R) has agreed that LTE still can be branded as 4G [11].

³Note that the exact properties of a signal varies depending on how it is generated. Other LTE- and WCDMA-signals can therefore have PDFs and PAPRs that deviate from what is shown in Fig. 1.2 and tabulated in Table 1.1.



Figure 1.2: Probability density functions (PDFs) of a GSM, WCDMA and LTE signal. Note that the PDF of the GSM signal ideally is a Dirac delta function and that it has been downsized for clarity. The figure also shows how the drain efficiency for an ideal class-B amplifier depends on output power.

radio frequency (RF) output power and the consumed direct current (DC) power $\eta = P_{out}/P_{DC}$, of an ideal class-B amplifier depends on the output power. As can be seen, the efficiency is high at the maximum power level where the GSM-signal operates but is significantly lower where the PDF of the WCDMA and LTE-signals is large.

The average drain efficiency η_{avg} when amplifying an amplitude modulated signal depends on the signal PDF and the efficiency of the PA according to,

$$\eta_{avg} = \frac{P_{out,avg}}{P_{DC,avg}} = \frac{\int_0^{P_{max}} P_{out} \cdot \rho(P_{out}) dP_{out}}{\int_0^{P_{max}} \frac{P_{out}}{\eta(P_{out})} \cdot \rho(P_{out}) dP_{out}},$$
(1.1)

where ρ is the signal PDF. Thus, η_{avg} for the ideal class-B amplifier can be calculated for the signals in Fig. 1.2. The result is reported in Table 1.1 together with the signal peak to average power ratio (PAPR), defined as the ratio between the peak power and the average power, P_{max}/P_{avg} . Due to its low back-off efficiency, the class-B amplifier has a considerably lower average efficiency for the amplitude modulated signals. For this reason, the introduction of amplitude modulated signals in mobile communication has triggered a strong interest for PAs with enhanced back-off efficiency.

Table 1.1: The peak to average power ratio for different signals and the theoretical average drain efficiency when amplifying them with an ideal class-B amplifier

| | GSM | WCDMA | LTE |
|-------------------|----------------------|-------|------|
| PAPR (dB) | 0 | 6.7 | 9.0 |
| $\eta_{avg}~(\%)$ | 78.5 | 41.4 | 31.5 |

1.2 Efficiency enhancement techniques

The efficiency behavior of the class-B amplifier in Fig. 1.2 can be qualitatively understood by examining its load-line in Fig. 1.3. As can be seen, the



Figure 1.3: The load-line of the class-B amplifier at full output power and at 6 dB back-off.

load-line utilizes the full voltage swing at full output power, thereby ensuring high efficiency. However, it can also be seen that the voltage swing is reduced in output power back-off (OPBO), resulting in an unnecessary high supply voltage V_{DS}^4 and consequently low back-off efficiency. For this reason, all efficiency enhancement techniques strives to, in one way or another, manipulate the load line to obtain full voltage swing also in back-off.

This section provides a brief discussion about the techniques that can be used to enhance the back-off efficiency, for a more thorough review see e.g. [18]. To facilitate the understanding of their different working principles, the load line of the class-B amplifier is used. It must however be noted that many of the techniques also can be implemented by using other modes of operation such as class-A, -AB, -C and -J; or different types of switch-mode operations such as class-E, -D, -F, and $-F^{-1}$. There are also more exotic efficiency enhancement techniques that are purely based on switch-mode operation. Example of such techniques are pulse width modulation [19,20], burst mode operation [21], and class-S [22,23]. However, in interest of focusing on the most commonly used techniques, these switch-mode efficiency enhancement techniques will not be further examined.

1.2.1 Supply modulation

The principle of supply modulation is illustrated in Fig. 1.4. By reducing the supply voltage V_{DS} when the output power is backed-off, e.g. by using an envelope amplifier (EA), the efficiency is maintained high also for small output powers. Depending on the control of the EA and the PA, supply modulation can be divided into the main categories Envelope Elimination and Restoration (EER), first proposed by Kahn in 1952 [24], Envelope Tracking (ET), and Polar [18]. All these techniques have the attractive feature that the design of the EA ideally is decoupled from the PA which in theory makes supply modulation very suitable for wideband and efficient transmitters [18]. However, it has also been shown that best performance still is obtained when the EA and PA are co-designed [25]. A drawback of supply modulation is that the performance of any supply modulated PA is much dependent on the

⁴All notations used throughout this thesis uses High Electron Mobility Transistor (HEMT)-terminology.



Figure 1.4: The supply modulation (a) load-line and (b) architecture principles.

EA efficiency, bandwidth, peak power, dynamic range, etc., thus making the design of high performance EAs a research topic of its own [26]. Nevertheless, supply modulation attracts much attention and very interesting results has indeed been reported, e.g. [25, 27–32] to mention a few. An example of how supply modulation has found its way to consumer products is the Samsung GALAXY Note 3 where ET is implemented in the radio unit [33].



Figure 1.5: Example of a load modulated load-line.

1.2.2 Load modulation

Full voltage swing in back-off may also be obtained by modulating the PA load impedance, thereby changing the slope of the load-line as shown in Fig. 1.5. One method to do this is dynamic load modulation (DLM) where tunable elements, such as varactors or switches, are used to dynamically change the PA load impedance as the signal envelope varies, see Fig. 1.6a. In contrast to supply modulation, the external circuit needed to control the tunable elements does not have to supply any significant amount of power thereby simplifying its design and reducing its negative influence on the overall performance.

DLM is still a rather new technique and has not gained the same attention as e.g. ET. Nevertheless, interesting results have recently been published, demonstrating that DLM can be used both to provide wideband performance [34] as well as high power [d]. Besides modulating the load for higher



Figure 1.6: The (a) dynamic load modulation, and (b) active load modulation architecture principles.

efficiency, theoretical studies show that DLM architectures also may be used to simultaneously adjust for changes in the antenna impedance [35]. This makes DLM very interesting for applications where large variation of the antenna impedance can be expected, e.g. in handheld devices.

Load modulation can also be obtained by active load-pull between two or more sub-amplifiers and is then referred to as active load modulation (ALM). Fig. 1.6b shows a generic topology for the most common case where two subamplifiers are used. By varying the amplitude and phase balance between the output currents I_1 and I_2 , the load impedances Z_1 and Z_2 can be modulated. Two of the most common ALM techniques are outphasing, originally proposed as an efficiency enhancement technique by H. Chireix [36]; and Doherty, originally proposed by W. H. Doherty [37].

In outphasing, I_1 and I_2 typically have the same amplitude, and load modulation is achieved by varying the phase between them as the signal envelope varies. However, this requires that the phase between the input signals can be quickly and accurately controlled. Outphasing amplifiers are therefore implemented with separate RF-drivers for each sub-amplifier, thus making the implementation fairly complex. Still, it seems like the interest for outphasing PAs is increasing and very interesting results have indeed been reported in recent time [38,39].

In contrast to the outphasing PA, the Doherty PA (DPA) relies on a static phase between the sub-amplifier output signals. Instead, load modulation is achieved by varying their amplitude relationship. The advantage of the DPA is that correct amplitude relations in most cases can be obtained by using a single RF-driver in combination with an analog power splitter and proper sub-amplifier gate-bias. This makes the DPA the only of the efficiency enhancement techniques that do not require any additional drivers or control circuits.

The combination of good efficiency and simple implementation has made the DPA the workhorse in many of today's commercial RF-transmitters for mobile communication. The DPA has, however, for a long time been regarded as a narrowband PA. For example, Cripps mentions a bandwidth limit of 10% in [18]. The DPA has therefore a hard time to meet the requirement of wideband performance that is desirable, or even required, for PAs in present and future communication systems.

1.3 Thesis contribution

This thesis investigates theoretical and practical bandwidth limitations of the DPA and presents new methods to overcome them. It is acknowledged that the device output parasitics, and the method used to compensate for them, in many cases is the main source of DPA-bandwidth degradation. It is therefore important that the parasitics are effectively compensated for in a broadband manner. However, non-ideal behavior of electrical components and limitations in manufacturing techniques often narrows the number of practical solutions available. This is extra problematic in monolithic microwave integrated circuit (MMIC) implementations where area and dimension restrictions, together with poor current handling capabilities and high losses, often constrains the design freedom. As a first contribution, the work in [A] suggests a practical solution that serves to reduce the influence of output parasitics and to overcome manufacturing limitations, thereby extending the DPA bandwidth. To demonstrate the utility of the presented technique, a gallium nitride (GaN) MMIC DPA aiming for microwave PTP communication applications is presented.

Besides the output parasitics, it is a well-known fact that the DPA has an inherent bandwidth limitation due to its required impedance inverter. A modification of the DPA that serves to significantly extend its inherent bandwidth is therefore presented in [B]. In addition, it is also shown that the introduced modification enables the efficiency to be reconfigured without the need of tunable elements. The suggested modifications and the theoretical findings are proven by a dual RF-input demonstrator circuit showing both excellent bandwidth and reconfigurable efficiency. The idea in [B] is further developed in [C] where it is theoretically shown that both the bandwidth enhancement and the efficiency reconfiguration can be obtained also in a single RF-input configuration. The utility of the presented theory is demonstrated by the design and fabrication of an amplifier made in the same commercial GaN MMIC process as the circuit in [A]. Measurements show that the amplifier can be biased to provide nearly twice the bandwidth compared to the circuit in [A], as well as state-of-the-art linearity.

Even though the bandwidth limitations imposed by the device output parasitics and the impedance inverter may be greatly reduced, the work in [A–C] shows that they still limit the achievable bandwidth. To achieve bandwidths even larger than one octave, [D] presents a novel design method based on a Doherty-Outphasing continuum. The method is supported by the design and characterization of a demonstrator circuit with more than 100% fractional bandwidth.

In summary, this thesis contributes with three distinct solutions that evolve the traditionally regarded narrow band DPA into an amplifier that provides significantly enhanced back-off efficiency for bandwidths extending beyond the octave bandwidth limit.

Chapter 2

The Doherty power amplifier

In the pursuit of increased bandwidth for the DPA, it is essential to understand the principle of its operation. In [18] a good introduction to the DPA is given, however, the theory only focuses on the specific configuration where the efficiency peaks at 6 dB OPBO, and bandwidth issues are not addressed. The purpose of this chapter is to provide a more complete theory including different configurations of the DPA as well as its frequency response.

In the first section a simple and straight forward theory for describing the DPA at the center frequency is presented and it is shown that the efficiency behavior in back-off is a design parameter that determines how to choose the load impedance and the driving conditions. In the second section, the analysis is extended to also include the frequency response and it is demonstrated how the DPA-architecture limits the efficiency bandwidth in back-off. The theory to be presented remains much idealized throughout this entire chapter. The main and auxiliary amplifiers are represented by ideal half-wave rectified voltage controlled current sources, having constant transconductance, short circuit harmonics, zero knee-voltage, and a drain-to-source bias V_{DS} . Hence, effects from using auxiliary amplifier class-C bias, non-ideal harmonic terminations, or limitations imposed by the input network, are not addressed.

2.1 Center frequency analysis

Fig. 2.1 shows the basic configuration of the DPA. The topology consists of a main and an auxiliary amplifier that are combined on the output via a $\lambda/4$ -transmission line impedance inverter¹ having a characteristic impedance Z_C [40]. The sub-amplifiers are thereafter connected to the common load R_L . The input consists of a power divider and a $\lambda/4$ -transmission line at the input of the auxiliary amplifier that serves to give the same phase delay through the two amplifier paths.

¹The $\lambda/4$ -transmission line impedance inverter is hereafter referred to as the $\lambda/4$ -impedance inverter.



Figure 2.1: Basic configuration of the Doherty power amplifier.



Figure 2.2: Schematic of the Doherty power amplifier output network. The main and auxiliary amplifiers are represented by the current sources I_m and I_a , respectively.

The output network of the DPA can be schematically illustrated as in Fig. 2.2. Note that, although not indicated in the figure, it is assumed that all harmonic frequencies are short circuited and that both sub-amplifiers have their drain terminals biased at V_{DS} . The amplifiers are represented by current sources having fundamental output currents I_m and I_a that depends on the amplifier voltage drive level $0 \le \xi \le 1$ as,

$$I_m = \xi \frac{I_{max,m}}{2},\tag{2.1}$$

$$I_{a} = \begin{cases} 0 & 0 \le \xi \le \xi_{b} \\ \frac{I_{max,m}}{2} \frac{\xi - \xi_{b}}{\xi_{b}} e^{j\phi} & \xi_{b} < \xi \le 1 \end{cases},$$
(2.2)

where the variable ξ_b is the drive level at the onset of the auxiliary amplifier and $I_{max,m}$ is the maximum current of the main amplifier. The phase balance ϕ^2 is given as $-\bar{f}\pi/2$ where $\bar{f} = f/f_0$ is the frequency normalized to the center frequency f_0 . The amplitudes of I_m and I_a are plotted versus drive level in Fig. 2.3 where it is shown how the value of ξ_b determines the auxiliary amplifier current onset, maximum value, and increase rate.

The main and auxiliary amplifiers output voltages, V_m and V_a (Fig. 2.2) are given by,

$$V_m = Z_{11}I_m + Z_{12}I_a \tag{2.3}$$

²Note that the sign of ϕ is changed compared to what is used in [B]. The reason for this is to make the definition consistent with what is used in [C–E].



Figure 2.3: The amplitudes of the output currents I_m and I_a , normalized to $I_{max,m}/2$, versus drive level for $\xi_b = 0.3$, 0.4, and 0.5, respectively.

$$V_a = Z_{21}I_m + Z_{22}I_a \tag{2.4}$$

where the impedance values are given by the impedance matrix (2.5) for the dashed two-port in Fig. 2.2 [41].

$$\mathbf{Z} = \begin{bmatrix} Z_C \frac{R_L \cos(\bar{f}\pi/2) + jZ_C \sin(\bar{f}\pi/2)}{Z_C \cos(\bar{f}\pi/2) + jR_L \sin(\bar{f}\pi/2)} & \frac{Z_C R_L}{Z_C \cos(\bar{f}\pi/2) + jR_L \sin(\bar{f}\pi/2)} \\ \frac{Z_C R_L}{Z_C \cos(\bar{f}\pi/2) + jR_L \sin(\bar{f}\pi/2)} & \frac{Z_C R_L \cos(\bar{f}\pi/2) + jR_L \sin(\bar{f}\pi/2)}{Z_C \cos(\bar{f}\pi/2) + jR_L \sin(\bar{f}\pi/2)} \end{bmatrix}.$$
(2.5)

Note that the voltage over the load R_L is equal to the auxiliary amplifier output voltage V_a .

The values of Z_C and R_L that optimizes the output power and efficiency at the center frequency are derived from (2.3)–(2.5) as follows: Starting with Z_C , we first observe from (2.4) and (2.5) that the auxiliary amplifier output amplitude becomes $|V_a| = |I_m|Z_C$ at the center frequency. The value of Z_C should therefore be set to maximize the efficiency of the auxiliary amplifier, that is, the amplitude $|V_a|$ should equal the drain-to-source bias V_{DS} at peak power. Hence, using the requirement of $|V_a| = V_{DS}$ when $\xi = 1$ and $\bar{f} = 1$ gives,

$$Z_C = \frac{2V_{DS}}{I_{max,m}} = R_{opt},$$
(2.6)

where R_{opt} is the optimum class-B load for a given transistor [18].

For drive levels where $I_a \neq 0$, the expression for V_m in (2.3) can at the center frequency be written as,

$$V_m = \frac{I_{max,m}}{2} Z_C \xi \left(\frac{Z_C}{R_L} - \frac{1}{\xi_b} \right) + \frac{I_{max,m}}{2} Z_C.$$
(2.7)

Thereby, by choosing,

$$R_L = \xi_b Z_C, \tag{2.8}$$

the first term in (2.7) becomes zero which gives $V_m = Z_C I_{max,m}/2 = V_{DS}$, for all drive levels $\xi \ge \xi_b$. Fig. 2.4 shows the normalized output voltage amplitudes $|V_m|/V_{DS}$ and $|V_a|/V_{DS}$ versus drive level when Z_C and R_L are set according to (2.6) and (2.8), and $\bar{f} = 1$. As expected, $|V_m|$ equals V_{DS} for all drive



Figure 2.4: The amplitudes of the output voltages V_m and V_a , normalized to V_{DS} , versus drive level ξ for $\xi_b = 0.3, 0.4$, and 0.5.

levels in the high power region, that is when $\xi_b < \xi \leq 1$, thereby ensuring high efficiency operation. Furthermore, the linear relationship between $|V_a|$ and ξ implies that the DPA provides perfectly linear gain.

The fact that R_L is a function of ξ_b implies that ξ_b most often is a fixed value since R_L otherwise has to be reconfigurable. This makes it important for the designer to understand at which output power levels high efficiency should be prioritized.

In order to calculate the efficiency of the amplifier, the output power and DC-power consumption are first identified to [18],

$$P_{out} = \frac{|V_a|^2}{2R_L} = \frac{Z_C |I_m|^2}{2\xi_b},$$
(2.9)

$$P_{DC} = \frac{2V_{DS}\left(|I_m| + |I_a|\right)}{\pi}.$$
(2.10)

The drain efficiency is thereafter given by,

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi Z_C |I_m|^2}{4V_{DS}\xi_b \left(|I_m| + |I_a|\right)}.$$
(2.11)

The result is shown in Fig. 2.5 where the drain efficiency is plotted versus the normalized load voltage $|V_a|/V_{DS}$, and versus OPBO. As can be seen, a smaller value of ξ_b gives a higher efficiency in back-off with a deeper efficiency-dip between the two efficiency peaks. The OPBO-level where the efficiency peaks in back-off, herein referred to as P_{BO} , depends on ξ_b as $P_{BO} = -20 \log (\xi_b)$, and is indicated in Fig. 2.5 for reference.

The theory presented in this section has shown how a simple combination of two sub-amplifiers, together with correct driving conditions and load impedance, can give very good efficiency performance while perfect linearity is maintained. It was also demonstrated how the value of ξ_b influences the efficiency, the driving conditions, and the choice of load impedance.

In the next section, the analysis is extended to also include the frequency response of the DPA and it is shown how the $\lambda/4$ -impedance inverter affects the bandwidth for different values of ξ_b .

Figure 2.5: The drain efficiency versus (a) normalized load voltage amplitude $|V_a|/V_{DS}$, and (b) output power back-off, for $\xi_b = 0.3$, 0.4, and 0.5. $P_{BO1} = 10.5 \text{ dB}, P_{BO2} = 8 \text{ dB}$, and $P_{BO3} = 6 \text{ dB}$, associated with $\xi_b = 0.3$, $\xi_b = 0.4, \xi_b = 0.5$, respectively, are indicated in (b)

2.2 Frequency response analysis

Using (2.5), the relation in (2.8), the current relations in (2.1) and (2.2), and the expressions for the main and auxiliary amplifiers output voltages in (2.3) and (2.4), the expression of V_m and V_a are derived as functions of ξ , ξ_b , and \bar{f} ,

$$V_{m} = \begin{cases} V_{DS} \left(\frac{\xi\xi_{b}\cos(\bar{f}\pi/2) + j\xi\sin(\bar{f}\pi/2)}{\cos(\bar{f}\pi/2) + j\xi_{b}\sin(\bar{f}\pi/2)} \right) & 0 \le \xi \le \xi_{b} \\ V_{DS} \left(\frac{(\xi\xi_{b} + \xi - \xi_{b})\cos(\bar{f}\pi/2) + j\xi_{b}\sin(\bar{f}\pi/2)}{\cos(\bar{f}\pi/2) + j\xi_{b}\sin(\bar{f}\pi/2)} \right) & \xi_{b} < \xi \le 1 \end{cases}$$
(2.12)

$$V_{a} = \begin{cases} V_{DS} \left(\frac{\xi \xi_{b}}{\cos(\bar{f}\pi/2) + j\xi_{b}\sin(\bar{f}\pi/2)} \right) & 0 \le \xi \le \xi_{b} \\ V_{DS} \left(\frac{\xi \xi_{b} + (\xi - \xi_{b})\cos(\bar{f}\pi/2)(\cos(\bar{f}\pi/2) - j\sin(\bar{f}\pi/2))}{\cos(\bar{f}\pi/2) + j\xi_{b}\sin(\bar{f}\pi/2)} \right) & \xi_{b} < \xi \le 1 \end{cases}$$
(2.13)

Fig. 2.6 shows how $|V_m|$ and $|V_a|$ from (2.12) and (2.13) depends on drive level at different frequencies when $\xi_b = 0.5$. As can be seen in Fig. 2.6a, the large voltage swing at the output of the main amplifier no longer is maintained in the high power region when the frequency diverges from the center frequency which indicates a reduced efficiency. In addition, the relationship between $|V_a|$ and ξ , depicted in Fig. 2.6b, is only linear at the center frequency which implies that linear gain is not maintained outside the center frequency.

Fig. 2.7 shows how the reduced voltage swing on the output of the main amplifier affects the efficiency. As observed, the efficiency in back-off is significantly reduced outside the center frequency. However, it is important to note that neither the efficiency, nor the gain, are affected by the frequency at peak power.

How the efficiency at P_{BO} depends on frequency for different settings of ξ_b is shown in Fig. 2.8. As can be seen, the frequency range where high efficiency is obtained in back-off becomes more narrow when ξ_b is decreased. For example,

Figure 2.6: The amplitudes of, (a) the main amplifier voltage $|V_m|$, and (b) the auxiliary amplifier voltage $|V_a|$, normalized to V_{DS} , versus drive level ξ for different frequencies.

Figure 2.7: The drain efficiency versus, (a) normalized load voltage amplitude $|V_a|/V_{DS}$, and (b) output power back-off, for different frequencies.

the drain efficiency at 6 dB OPBO is maintain larger than 70% over a 22% fractional bandwidth when $\xi_b = 0.5$, whereas for $\xi_b = 0.3$ the bandwidth is reduced to 10%.

Assuming a reference impedance Z_C , the electrical length of the $\lambda/4$ impedance inverter becomes equal to the phase of S_{21} . Hence, as long as S_{11} and S_{22} are zero, the drain efficiency is determined by $\angle S_{21}$ of the impedance inverter. The curves in Fig. 2.8 are therefore also plotted versus $\angle S_{21}$ which in following chapters makes it possible to estimate the feasible DPA-bandwidth when using non-ideal impedance inverters in real implementations.

How the frequency response of the back-off efficiency affects the average efficiency is calculated for the 6.7 PAPR WCDMA and 9.0 dB PAPR LTEsignal by using (1.1). Since the signals have different PAPR, the values of ξ_b have been set to $\xi_b = 0.5$ and $\xi_b = 0.4$ for the WCDMA-signal and the LTEsignal, respectively. The result in Fig. 2.9 shows two interesting things: Firstly, η_{avg} is lower for the LTE-signal than for the WCDMA-signal even though ξ_b has been optimized in both cases. The reason for this is that the efficiency at power levels between P_{BO} and P_{max} is reduced when ξ_b is increased, as shown in Fig. 2.7. Secondly, Fig. 2.9 shows that the LTE-signal gives a faster efficiency roll-off versus frequency. This is because of the increased signal PAPR that makes the average efficiency more dependent on the back-off efficiency, for

Figure 2.8: The drain efficiency at P_{BO} for different values of ξ_b plotted versus frequency and $\angle S_{21}$.

Figure 2.9: The average drain efficiency for the 6.7 dB PAPR WCDMA and 9.0 PAPR LTE-signals when $\xi_b = 0.5$ and 0.4, respectively.

which the frequency dependence is larger.

The reason for the increased inherent bandwidth limitation of the DPA can be qualitatively understood by the way the $\lambda/4$ -impedance inverter transforms Z_{mT} to Z_m ,

$$Z_m = Z_C \frac{Z_{mT} + jZ_C \tan(\bar{f}\pi/2)}{Z_C + jZ_{mT} \tan(\bar{f}\pi/2)}.$$
(2.14)

At peak power, Z_{mT} equals Z_C , and the numerator and denominator in (2.14) becomes equal which makes Z_m , and consequently also the efficiency and gain, independent of frequency. Conversely, in the low power region where $I_a = 0$, Z_{mT} equals R_L , which makes Z_m dependent on both the ratio Z_C/R_L and the electrical length of the impedance inverter $\bar{f}\pi/2$. This is a straightforward, yet powerful observation, that is used in Chapter 4 to find a method that extends the inherent DPA-bandwidth significantly.

2.3 Chapter summary

This chapter has presented an idealized theory describing the standard DPA. It has been shown how the performance and driving conditions depends on frequency and the choice of ξ_b . It was demonstrated that the DPA has an in-

herent bandwidth limitation that gives a drastically reduced back-off efficiency outside the center frequency, and consequently reduced average efficiency for modulated signals. It was also shown that this dependence becomes more severe for large signal PAPRs and small values of ξ_b .

The reason for the inherent bandwidth limitation is the behavior of the $\lambda/4$ -impedance inverter and it can therefore be argued that another type of impedance inverter with less frequency dependence could be used to increase the bandwidth. However, to the best of the author's knowledge, no such impedance inverter has been described in literature, nor have the studies preceding this thesis indicated that such impedance inverters can be realized. In fact, as is shown in the next chapter, real implementations of impedance inverters have even stronger frequency dependence than the ideal $\lambda/4$ -impedance inverter.

Chapter 3

Practical implementations of output networks

In the previous chapter it was shown that the back-off efficiency of the DPA is inherently bandwidth limited due to the need of the $\lambda/4$ -impedance inverter. However, it was also shown that the 6 dB OPBO drain efficiency is maintained higher than 70% over a fractional bandwidth larger than 20% when $\xi_b = 0.5$. There must therefore be other reasons why the DPA often has a significantly lower bandwidth in practice. Not surprisingly, it has been shown that it is the device output parasitics, and the method used to compensate for them, that in many cases degrade the DPA bandwidth the most [41,42].

In this chapter, three methods that are commonly used to compensate for the output parasitics are reviewed: offset-lines, compensating networks, and parasitic absorption. Their effects on the DPA-bandwidth are discussed and it is concluded that the parasitic absorption method should be beneficial in wideband designs. Many of the networks used to facilitate parasitic absorption are however hard to realize at high frequencies and for high impedance levels. To overcome such restrictions, a new type of network topology based on the parasitic absorption method is presented in [A]. The network is implemented in a GaN MMIC DPA and the design and characterization of this circuit is reviewed and discussed in the end of this chapter.

When analyzing different output networks, an equivalent circuit model of the device output is often needed. It is shown in several publications that the simplified model in Fig. 3.1, where the output parasitics are represented by an effective output capacitance C_{out} , often is sufficient for analysing DPA output networks [18, 41–44]. This simplified model is therefore used in this chapter and throughout the rest of this thesis.

3.1 Offset-lines

A common method to compensate for the output parasitics is to use output matching networks in combination with offset-lines as shown in Fig. 3.2. Note that both the offset-lines and the impedance inverter can be realized either by distributed or lumped elements, or combinations thereof, which is why they

Figure 3.1: Simplified model of the device output parasitics used for analyzing DPAs.

Figure 3.2: Block scheme of the output network for a DPA with offset-lines.

are represented as general two port networks.

The use of offset-lines was first proposed in [45] and has thereafter been used in numerous publications [46,47]. The advantage of the method is that it can provide impedance transformation between the impedances Z_i seen by the device intrinsic current sources and the impedances Z'_i seen from the output of the offset-lines¹. Offset-lines can thereby be used to scale Z_C to a more convenient value Z'_C in implementations where (2.6) otherwise would require a non-realizable characteristic impedance.

The analyses in e.g. [42,48] do, however, give good reasons to believe that the use of offset-lines, if possible, should be avoided in wideband designs. That said, it should be stressed that, to the best of the author's knowledge, there are yet no publications that fully proves that offset-lines restrict the bandwidth.

3.2 Compensating networks

Another method to deal with the output parasitics is to use compensating networks as shown in Fig. 3.3. The compensating networks serves to ensure that the impedances Z_i are identical to the impedances Z'_i . With a proper design of the compensation networks, the S-parameters of the dashed two ports in Fig. 3.3 should thereby become,

$$\mathbf{S}_{\mathbf{i}} = \begin{bmatrix} 0 & \pm 1\\ \pm 1 & 0 \end{bmatrix}. \tag{3.1}$$

¹Note that the index *i* refers to either *m* (main) or *a* (auxiliary).

Figure 3.3: Block scheme of the output network for a DPA where the output parasitics are eliminated by compensating networks.

One example where compensating networks have been used is [43] where they were realized with shunt inductors as shown in Fig. 3.4. When doing so, the value of the inductance should be chosen to resonate with the output capacitances at the design frequency. Hence,

$$L_i = \frac{1}{\omega_0^2 C_{out,i}},\tag{3.2}$$

where ω_0 is the angular center frequency. For future reference the specific network in Fig. 3.4 is referred to as the LC-network.

The LC-network is convenient since the inductors can be used as DC bias feed. However, in implementations where inductors typically have low currenthandling capabilities, e.g. in MMICs, bias feed through them might not be possible. Further, the bandwidth of the LC-resonant circuits affect the bandwidth of the DPA and in [41] it is shown that the method can reduce the DPA bandwidth more than necessary.

The applicability of using compensating networks depends on the possibility to realize the impedance inverter. For instance; wide band-gap technologies such as GaN, utilize high drain bias voltages and can in low and medium power applications require values of Z_C that are larger than 100 Ω . In such a case, the impedance inverter cannot be realized as a $\lambda/4$ -transmission line since it most certainly would require unrealistic line widths. The same problem may also arise when realizing the impedance inverter with lumped components due to the limited quality-factors of available inductors.

In order to ensure large bandwidth, the S-parameters in (3.1) should be as frequency independent as possible. For this reason, wideband compensating networks that serve to fulfil (3.1) over a 3.0–3.6 GHz frequency range are proposed in [49]. However, from the presented analysis it is not clear how the phase of S_{21} and S_{12} of the compensating networks behave versus frequency and despite good experimental results it is not fully validated that wideband compensating networks can be realized.

Figure 3.4: Example of how the compensating networks in Fig. 3.3 can be realized by shunt inductors. The device output parasitics are modeled as shown in Fig. 3.1.

3.3 Parasitic absorption

Due to the often narrowband performance when using offset-lines, and the lack of broadband compensations networks, the majority of the work presented in this thesis [A]–[C] has used a method suggested in [41]. The idea of the method is to compensate for the output parasitics by absorbing them into the impedance inverter as illustrated in Fig. 3.5. Designing the DPA output network thereby becomes a matter of finding a combining network that, together with the output capacitances, acts as an impedance inverter with the required characteristic impedance Z_C .

What is significant for this method is that it can be applied only when there are no series elements between the auxiliary current source and the common load R_L . Strictly speaking, series elements are always present, e.g. in terms of package parasitics or bond-wires. However, e.g. in MMIC implementations, or when using bare-die devices, such series elements can in many cases be neglected.

Three examples of commonly used combining networks that together with the output parasitics acts as impedance inverters are shown in Fig. 3.6: A quasi-lumped (QL) network, a lumped Π -network, and an LC-network. The

Figure 3.5: Schematic illustrating how the output parasitics are absorbed into the impedance inverter.

Figure 3.6: The (a) QL-network, (b) Π -network, and (c) LC-network, used to absorb the device output capacitances in DPAs.

LC-network in Fig. 3.6c is in fact identical to the LC-network discussed in the previous section and will not be further examined in this section.

3.3.1 Quasi-lumped network

The QL-network is illustrated in Fig. 3.6a. When $C_{out,m}$ and $C_{out,a}$ are equally large, the electrical length and impedance of the transmission line are given by,

$$\theta_n = \arccos\left(\omega_0 C_{out} Z_C\right),\tag{3.3}$$

$$Z_n = \frac{Z_C}{\sin\left(\theta_n\right)}.\tag{3.4}$$

The network is proposed in [41] as a more wideband alternative to the LCnetwork and is successfully implemented in a DPA with more than 40% drain efficiency at 6 dB OPBO from 1.7 to 2.1 GHz. The network does however have some practical limitations. Firstly, to ensure real values of θ_n and Z_n the relation $\omega_0 C_{out} Z_C < 1$ must be fulfilled. Hence, there is an upper frequency limit beyond which the network cannot be used. From (3.4) it can also be seen that $Z_n \geq Z_C$ and the method is therefore not suitable for applications where high values of Z_n implies non-realizable linewidths. It should also be noted that the QL-network requires additional bias circuitry which might degrade its performance and complicates the design procedure.

3.3.2 Π -network

Fig. 3.6b shows how the impedance inverter can be implemented as a Π -network. The inductance L_T and the reactance X_i can be derived from [50] and becomes,

$$L_T = \frac{Z_C}{\omega_0},\tag{3.5}$$

$$X_{i} = \frac{1}{\omega_{0}(C_{out,i} - C_{T})},$$
(3.6)

where

$$C_T = \frac{1}{\omega_0 Z_C}.\tag{3.7}$$

Note that, depending on the sign of X_i , the shunt elements are implemented as either an inductors or capacitors which is why they are modeled as reactances.

Compared to the QL-network, the Π -network is not limited by non-realizable linewidths when Z_C is large. However, combinations of ω_0 , Z_C and $C_{out,i}$ can result in large inductor values that are difficult to realize. In particular, it can be cumbersome to realize large inductor values in MMIC implementations due to their often limited current handling capabilities, high loss, and shunt-parasitics. These issues are addressed in [42, 46, 51] by implementing the inductors off-chip using bond-wires and slab inductors on a printed circuit board whereas [52] uses bond-wires for realizing the series inductance L_T .

3.3.3 Tee-line network

Figure 3.7: Tee-line impedance inverter. The impedances Z_{Ci} can be arbitrary chosen whereafter the electrical lengths θ_i can be calculated.

With respect to the previous discussion, a combining network that is not limited by the performance of inductors, or by narrow transmission lines, is desirable. In [A] we therefore propose the Tee-line network, depicted in Fig. 3.7. The network consists of three transmission lines with electrical lengths θ_n and characteristics impedances Z_{Cn} (the index *n* represents any of the three transmission lines). It is shown that each characteristic impedance Z_{Cn} can be pre-selected to a convenient value whereafter the electrical lengths are calculated for the given values of $C_{out,m}$, $C_{out,a}$, and Z_C . For example, Fig. 3.8 shows how the electrical lengths of the transmission lines in Fig. 3.7 depend on the normalized susceptance $\omega_0 C_{out,i} Z_C$ for different sets of normalized impedances $\bar{Z}_{Cn} = Z_{Cn}/Z_C$. The implications of Fig. 3.7 is that a Tee-line network with reasonable line lengths can be used as an impedance inverter for a large span of output capacitances and characteristic impedances.

The main advantage of the proposed network is that it is realizable also for large values of Z_C and that its applicability is not affected by the availability and performance of lumped inductors and capacitors. In addition, the network also offers convenient biasing through the short circuited transmission line. This makes the Tee-line network highly suitable for DPAs, especially when implemented in a GaN MMIC process.

3.4 Method for estimating frequency response

There are multiple techniques for analyzing how the output networks described in this chapter affect the bandwidth of the DPA. One can for instance analyze the frequency response of the load impedances seen by the current sources at peak power and at low power [42]. An important advantage of this technique

Figure 3.8: The plots show how the lengths θ of the transmission lines should be chosen for different capacitance values $C_{out,m}$ and $C_{out,a}$ and impedances Z_{Cn} in order to make the network in Fig. 3.7 behave as an impedance inverter. Due to symmetry θ_1 is given by setting i = m, j = a, and θ_2 is given by setting i = a, j = m. (a) and (b) show θ_i and θ_3 , respectively, for the configuration $\bar{Z}_{C1} = 1, \bar{Z}_{C2} = 1, \bar{Z}_{C3} = 1$. (c) and (d) shows θ_i and θ_3 , respectively, for the configuration $\bar{Z}_{C1} = 0.25, \bar{Z}_{C2} = 0.25, \bar{Z}_{C3} = 0.25$.

is that it can be applied to any type of output network. However, the result is much dependent on how the amplitudes and phases of the current sources are chosen and the analysis can therefore not isolate the effect of the output network. It can also often be hard to interpret how the resulting load impedances affect the performance of the DPA.

In this thesis, a different method that can be applied on output networks represented by the schematic in Fig. 3.5 is used: As discussed in Section 2.2, the efficiency the ideal DPA is determined by $\angle S_{21}^2$ of the $\lambda/4$ -impedance inverter. Hence, the impact an impedance inverting network has on the DPA bandwidth can be estimated from the frequency response of its $\angle S_{21}$ as long as long as S_{11} and S_{22} are small.

The outcome when comparing the frequency response of impedance inverting networks depends on the size of the output parasitics, the frequency, and the required characteristic impedance. It is therefore not possible to make a general comparison of the networks and they must instead be compared on a case-to-case basis. This is done in the next section for the specific design reported in [A].

²All S-parameters assumes Z_C reference impedance if not else is stated.

3.5 MMIC Doherty Power Amplifier

In order to demonstrate the utility of the Tee-line network, paper [A] presents a wideband DPA that is designed and fabricated in the commercial TriQuint 3MI 0.25 μ m GaN-HEMT MMIC process. This section will discuss why the Tee-line network is highly suitable for this design and its frequency response will be examined and compared to the other combining networks presented in this Chapter. The measurement results of the fabricated chip will thereafter be presented and discussed.

3.5.1 Design considerations

The targeted frequency range of the design was 7.0–8.0 GHz and was selected to target microwave PTP-link applications. As in many other applications, microwave links utilize modulation schemes with PAPR in the order of 7– 9 dB. To obtain high average efficiency it was decided to implement the design with a value of $\xi_b = 0.33$, giving $P_{BO} = 9.5$ dB, and $Z_C/R_L = 3$. The total gate-width of the main device was chosen to $4 \times 100 \ \mu\text{m}$, which in combination with a drain voltage of 20 V implies that $Z_C = 150 \ \Omega$ should be chosen for high power utilization. The combination of Z_C and ξ_b gives a convenient value of $R_L = 50 \ \Omega$ and implies that a peak output power of ≈ 35 dBm can be expected.

With $\xi_b = 0.33$, (2.2) shows that the auxiliary amplifier must be able to handle twice the current compared to the main amplifier. The auxiliary amplifier was therefore implemented with a 10 × 100 μ m device. For the given device sizes, the output capacitances were estimated to 0.15 pF and 0.44 pF for the main and auxiliary devices, respectively.

The widths of the Tee-line transmission lines in Fig. 3.7 were chosen to $w_1 = w_2 = 25 \ \mu \text{m}$ and $w_3 = 40 \ \mu \text{m}$, giving characteristic impedances of $Z_{C1} = Z_{C2} = 79 \ \Omega$, $Z_{C3} = 69 \ \Omega$. Using the equations derived in [A], the electrical lengths of the transmission lines were thereafter calculated to be $\theta_1 = 52.3^\circ$, $\theta_2 = 18.9^\circ$ and $\theta_3 = 17.0^\circ$.

To understand why the use of the Tee-line network is motivated it can be noted that the width of a transmission line with characteristic impedance $Z_C = 150 \ \Omega$ would be less than 0.3 μ m, far more narrow than what can be processed. The LC-network can therefore not be used for the reported design. Nor can the QL-network be used since $\omega_0 C_{out,i} Z_C > 1$ which violates the requirement for (3.3)-(3.4) to be valid. Furthermore, simulations of the amplifier indicated a maximum DC-current in the order of 420 mA. Using the II-network would therefore require spiral inductors with very large metal widths ($\approx 80 \ \mu$ m). Such inductors would consume a large area and have large parasitic capacitances that would degrade the performance.

Even though the LC- and Π -networks are unpractical, it is still of interest to investigate how their theoretical frequency responses compare with the Teeline network for this specific design. Fig. 3.9 shows the amplitude of S_{11} and the phase of S_{21} versus frequency. As can be observed, all networks give low S_{11} (and consequently S_{22}) between 7.0 and 8.0 GHz. It can also be seen that $\angle S_{21}$ for the Tee-line network and the LC-network network are very similar, whereas the Π -network shows a less frequency dependent $\angle S_{21}$.

Figure 3.9: (a) The magnitude of S_{11} (and consequently S_{22}) versus frequency, and (b) the phase of S_{21} versus frequency for the LC-, Π -, and Tee-line networks when assuming ideal lossless components. The reference impedance is 150 Ω .

Figure 3.10: Schematic of output network.

This could be interpreted as if the Π -network has the potential to provide more wideband DPAs compared to the Tee-line network. However, if the Π network could be realized, the physical inductors would be less ideal than the physical transmission lines in the Tee-line network. Consequently, the frequency response of the Π -network would be more degraded than for the Tee-line network.

3.5.2 Circuit realization and results

Fig. 3.10 shows the schematic of the realized output network width the lengths, widths, and impedances of TL1, TL2 and TL3 given in Table 3.1. A photo of the circuit is shown in Fig. 3.11 where it can be seen that a compact layout was achieved which resulted in a total chip-size of 2.1 mm \times 1.5 mm, small enough to fit in a quad-flat no-leads (QFN) 4 \times 4 package.

| | TL1 | TL2 | TL3 |
|------------|-------------------|---------------------|---------------------|
| Length: | $2800~\mu{\rm m}$ | $840~\mu\mathrm{m}$ | $750~\mu\mathrm{m}$ |
| Width: | $25~\mu{ m m}$ | $25~\mu{ m m}$ | $40~\mu{\rm m}$ |
| Impedance: | 79 Ω | 79 Ω | $69 \ \Omega$ |

Table 3.1: Tee-line Network Parameters

Figure 3.11: Photo of the realized circuit. The size measures $2.1 \text{ mm} \times 1.5 \text{ mm}$.

The results from continuous wave (CW) measurements are summarized in Fig. 3.12. The bias settings used for the measurements were³ $V_{GS,m} = -3.7$ V, $V_{GS,a} = -5.4$ V, and $V_{DS} = 20$ V.

Fig. 3.12a shows the power added efficiency (PAE) versus output power and Fig. 3.12b shows the PAE at different OPBO-levels versus frequency. As can be seen, there is a well pronounced efficiency enhancement in back-off across the target frequency band. For example, the PAE at 9 dB OPBO is maintained higher than 31% all across a 6.7–7.8 GHz frequency range, corresponding to 15% bandwidth. Fig. 3.12b also shows that the PAE is less frequency dependent at high output powers which is in good agreement with the theory.

The reported small signal gain in Fig. 3.12c and Fig. 3.12d is larger than 10 dB in the 6.5–7.5 GHz frequency range but decreases at higher frequencies. Fig. 3.12d also shows that the peak output power is maintained at 35 ± 0.5 dBm all across a 6.6–8.5 GHz frequency range.

Linearized modulated measurements, employing a vector switched generalized memory polynomial (VS-GMP) model [53], were performed in 100 MHz intervals over a 6.5–8.5 GHz frequency range using a 10 MHz 256-QAM signal with 7.8 dB PAPR. The result in Fig. 3.13 shows that the average PAE (PAE_{avg}) is larger than 35% all across the 6.8–8.5 GHz frequency range which is in good agreement with the CW measurements in Fig. 3.12. The figure also shows that the normalized mean square error (NMSE) and adjacent channel power ratio (ACPR) are better than -35 dB and -45 dBc, respectively.

As discussed in [A], the reported results verify the utility of the Tee-line network by clearly representing the state-of-the-art at the time of publication, both in terms of bandwidth and PAE — especially when considering the frequency and chip-size.

3.6 Chapter summary

This chapter has highlighted that the practical bandwidth of the DPA often is determined by the method used to compensate for the output parasitics of the

³The notation varies between the thesis and the papers.


Figure 3.12: Results from CW-measurements of the realized DPA. (a) PAE versus output power, (b) PAE versus frequency at different OPBO-levels relative the peak output power, (c) gain versus output power, (d) peak output power and small-signal gain versus frequency.

active devices. Several methods were reviewed and it was acknowledged that absorbing the output parasitics into the impedance inverter should be beneficial in wideband designs. However, it was shown that many of the commonly used networks based on the parasitic absorption method can be hard to realize. A new type of network, the Tee-line network, that is realizable also for high frequencies and/or high impedance levels was therefore proposed. The utility of the network was proven by implementing it in a GaN MMIC amplifier with state-of-the-art performance.



Figure 3.13: Measured PAE_{avg}, P_{out,avg}, NMSE, and ACPR after DPD.

Chapter 4

Extending the inherent bandwidth

The theory in Chapter 2 revealed one of the main drawbacks of the standard DPA, i.e. its inherent bandwidth limitation imposed by the $\lambda/4$ -impedance inverter. For this reason, a variety of techniques to extend the inherent bandwidth of the DPA have been proposed in recent years.

One of these techniques is the so called modified DPA which has a significantly larger inherent bandwidth compared to the standard DPA, as well as reconfigurable efficiency. The idea was first proposed in [a] where a dual-RF input 1.5–2.4 GHz demonstrator circuit with reconfigurable efficiency was presented. The theory, design and measurements presented in [a] were thereafter further examined in the extended article [B]. Shortly after the idea had been proposed in [a], the same idea was proposed by Wu and Boumaiza in an independent work [44] where a bandwidth of 0.7–1.0 GHz was obtained using a single RF-input configuration. Wu and Boumaiza thereafter empirically demonstrated that the efficiency of the modified DPA can be reconfigured also in a single RF-input configuration [54].

The presented theory in [44,54], [a,B] are all based on the same idealized assumptions as used in Chapter 2. The established theory can therefore not be used to analyze the single RF-input configuration of the modified DPA. For this reason, a theoretical analysis of the single RF-input modified DPA is presented in [C] where it is used to design a 5.8–8.8 GHz MMIC GaN DPA with reconfigurable efficiency.

This chapter presents a detailed examination of the modified DPA using both idealized theory and a more realistic single RF-input model. It is theoretically and empirically shown how the modified DPA can provide a significantly larger bandwidth compared to the standard DPA, as well as reconfigurable efficiency. However, before examining the modified DPA closer, a brief summary of other interesting techniques proposed to extend the inherent DPA-bandwidth is presented.

4.1 Literature survey

A successful and popular method to improve the inherent bandwidth of the DPA is to decrease the transformation ratio of the impedance inverter. The idea was first proposed in [55] where more than 41% drain efficiency at 5–6 dB OPBO over a 1.7–2.6 GHz frequency range is reported for a GaN DPA. The same idea is employed in [56] where more than 50% PAE at 6 dB OPBO is reported over a 1.7–2.25 GHz frequency range. A reduced transformation ratio is also used in [42] where an integrated INGaP/GaAs DPA with more than 30% average PAE over a 1.6–2.1 GHz frequency range is presented.

Another very interesting method is proposed in the papers [57–59] where it is shown how the inherent bandwidth can be significantly increased by cascading two $\lambda/4$ -transmission lines, with different characteristic impedances, on the output of the auxiliary amplifier. This enabled the design of a 350 W LD-MOS DPA with more than 48% drain efficiency from 790 to 960 MHz in [58], whereas a 700 W 470–803 MHz LDMOS DPA with more than 38% average drain efficiency is reported in [57]. In [59] the idea is used to design a 1.0–2.6 GHz GaN DPA with more than 35% drain efficiency at 6 dB OPBO.

Extending the bandwidth by using dual RF-inputs is proposed in [60] where it is shown how doing so extends the frequency range, for which more than 40% drain efficiency is achieved in 7 dB OPBO, from 2.04–2.22 GHz to 1.96– 2.46 GHz. It has also been proposed to use tunable devices to increase the bandwidth [61,62]. It is for example shown in [61] how MEMS-switches are used to design a GaN DPA than can be reconfigured for having more than 58% 6 dB OPBO drain efficiency at 1.9, 2.14, and 2.6 GHz, respectively.

4.2 The modified DPA



Figure 4.1: The output network of the modified DPA can ideally be represented by the same schematic as used for the standard DPA in Fig. 2.2.

The topology of the modified DPA is identical to the one of the standard DPA and its output network can thereby ideally be represented by the schematic in Fig. 4.1. What differentiates the modified DPA from the standard DPA is the relation between Z_C and R_L . In contrast to the standard DPA where $R_L = \xi_b Z_C$, the modified DPA uses $R_L = Z_C$, thereby ensuring that the main amplifier load impedance becomes independent of frequency when the auxiliary amplifier is turned off, see equation (2.14). As will be shown, this enables the modified DPA to provide a significantly larger bandwidth compared



Table 4.1: Design equations

Figure 4.2: The drain efficiency versus, (a) normalized load voltage amplitude $|V_a|/V_{DS,a}$, and (b) output power back-off, for different frequencies when $\xi_b = 0.5$.

to the standard DPA, both in terms of gain and efficiency.

For accurate functionality under the new condition $R_L = Z_C$, the equations describing bias voltages and driving conditions of the modified DPA have to be revised compared to the standard DPA. This is done in [B] where all calculations are based on the same assumptions and simplifications as the standard DPA-theory in Chapter 2. That is, the output network is represented by the schematic in Fig. 4.1 where the sub-amplifiers are modeled as ideal half-wave rectified voltage controlled current sources having identical transconductance, short circuit harmonics, zero knee-voltage, and drain bias voltages $V_{DS,m}$ and $V_{DS,a}$. The resulting design equations that govern the operation of the modified DPA are summarized in Table 4.1. Note that all equations are derived for maximum power utilization of the main amplifier and that the size of the auxiliary amplifier must be selected so that it can support the required current.

Using the derived design equations and calculating the drain efficiency yields the result in Fig. 4.2. As can be seen, the drain efficiency is independent



Figure 4.3: The drain efficiency at full output power for different values of ξ_b plotted versus frequency and $\angle S_{21}$.



Figure 4.4: The average drain efficiency for (a) the 6.7 dB PAPR WCDMAsignal when $\xi_b = 0.5$, (b) the 9.0 PAPR LTE-signal when $\xi_b = 0.4$.

of frequency in the low power region and it only shows a weak frequency dependence in the high power region. Comparing the results in Fig. 4.2 with Fig. 2.7 clearly shows that the modified DPA has a significantly larger inherent bandwidth than the standard DPA. In addition, as is shown in [B], the gain and peak power are independent of frequency.

The frequency response of the peak power drain efficiency is shown in Fig. 4.3 for different values of ξ_b . Comparing this result with the same plot for the standard DPA in Fig. 2.8 again shows the much larger theoretical bandwidth of the modified DPA. But maybe more interesting: As was shown in Chapter 3, the phase of S_{21} can have a very steep frequency response for practical implementations of impedance inverters. The relatively weak dependence on $\angle S_{21}$ in Fig. 4.3 is therefore an important result showing that the inherently more wideband performance makes the modified DPA less dependent on the frequency response of non-ideal impedance inverting networks.

The reason why the drain efficiency in Fig. 4.3 is not plotted over the entire frequency range when $\xi_b = 0.3$, 0.4, is that k in Table 4.1 only assumes real values when,

$$\frac{1-\xi_b^2}{1+\xi_b^2} \le \sin\left(\pi \bar{f}/2\right). \tag{4.1}$$

The derived theory is therefore not valid for all frequencies. For example, the



Figure 4.5: The drain efficiency versus, (a) normalized load voltage $|V_a|/V_{DS,a}$, and (b) output power back-off, at the center frequency. ξ_b is set to 0.5, 0.4 and 0.3 respectively.



Figure 4.6: The amplitudes of the normalized main and auxiliary amplifiers output voltages versus drive level ξ .

frequency range for which the equations in Table 4.1 can be used is $0.52 \leq \bar{f} \leq 1.48$ and $0.63 \leq \bar{f} \leq 1.37$, when $\xi_b = 0.4$ and $\xi_b = 0.3$, respectively. However, it is reasonable to believe that this is not an issue in practice since the frequency most likely is constrained by other factors before the theoretical bandwidth limit.

Fig. 4.4¹ shows how the increased efficiency bandwidth affects the average drain efficiency for the 6.7 PAPR WCDMA- and the 9.0 dB PAPR LTE-signals. For comparison, the figure also repeats the result for the standard DPA, previously shown in Fig. 2.9. The result shows that the modified DPA has a significantly lower frequency dependence compared to the standard DPA. It is interesting to note that because the modified DPA has such large efficiency bandwidth in back-off, the frequency response of the average drain efficiency is nearly unaffected when the signal PAPR is changed. Hence, the benefits of the modified DPA becomes even more pronounced when dealing with high PAPR signals.

It is interesting to note that the frequency responce

The design equations in Table 4.1 shows that $V_{DS,m}$ is lower than $V_{DS,a}$, which implies that the power capability of the main amplifier is not fully

¹It should be noted that Fig. 5 in [B], corresponding to Fig. 4.4a, shows a faulty average drain efficiency for the standard DPA. The author regrets this mistake.

utilized. However, the fact that ξ_b determines the relation between $V_{DS,m}$ and $V_{DS,a}$ rather than the relation between Z_C and R_L , also give interesting opportunities. As is shown in Table 4.1, $V_{DS,m}$ and I_a are the only parameters that depend on ξ_b . This implies that if I_a can be controlled, e.g. by using a dual RF-input configuration [41, 60, 63], the value of ξ_b and P_{BO} can be reconfigured by changing the main amplifier bias $V_{DS,m}$. Hence, the efficiency can be reconfigured versus output power.

The efficiency reconfiguration achieved by changing $V_{DS,m}$ and controlling I_a according to the equations in Table 4.1 is clearly visible in Fig. 4.5. It is also of interest to plot the output voltages when reconfiguring ξ_b . This is done in Fig. 4.6 which shows that the output voltage $|V_a|$, and thereby also the peak power and gain, is independent of ξ_b . This shows that the modified DPA, in theory, can be reconfigured for optimal performance for a large variety of modulation schemes without affecting output power or gain.

4.3 The single RF-input configuration



Figure 4.7: Schematic of the model used to analyze the single RF-input modified Doherty power amplifier [C].

As for the standard DPA-theory in Chapter 2, the theoretical analysis in [a,B], [44,54] are all based on the assumption that the sub-amplifiers are halfwave rectified current sources that can be ideally controlled. Although such an analysis gives valuable information about the theoretical limitations of the amplifier, it cannot be used to predict how the it behaves in a realistic single RF-input configuration. For this reason, the theory in [B] is further developed in [C] where a theoretical analysis of how to design a single RF-input modified DPA for best performance is presented.

4.3.1 Single RF-input model assumptions

The analysis is based on the single RF-input modified DPA model shown in Fig. 4.7. Although omitted for clarity in the figure, it is assumed that all harmonic frequencies are short circuited and that the sub-amplifiers have their gate and drain terminals biased at $V_{GS,m}$, $V_{GS,a}$, $V_{DS,m}$, and $V_{DS,a}$, respectively. In contrast to the model in Fig. 4.1, the input network is now accounted for by being represented by a lossless three-port having amplitude balance $\beta = |V_{in,a}/V_{in,m}|$ and phase balance $\phi = \arg(V_{in,a}/V_{in,m})$. Just as in Table 4.2: Technology parameters.

$$\frac{V_T (V)}{-3.1} \quad \frac{g_m (mS)}{250} \quad \frac{I_{max} (mA)}{750} \quad \frac{V_k (V)}{2.5}$$

Table 4.3: Parameter values used when calculating the curves in Fig. 4.8.

| Parameter | Value |
|------------------------|-------|
| ξ_b | 0.39 |
| $Z_C (\Omega)$ | 68 |
| $R_L (\Omega)$ | 68 |
| $\phi ~(\mathrm{deg})$ | -90 |
| eta | 1.2 |
| $V_{DS,m}$ (V) | 12.5 |
| $V_{DS,a}$ (V) | 28 |
| $V_{GS,m}$ (V) | -3.1 |
| $V_{GS,a}$ (V) | -4.37 |

Chapter 2 and [B], the sub-amplifiers are represented by voltage controlled current sources with transconductance $g_{m,i}$ and maximum output current $I_{max,i}$. However, they now have a non-zero knee voltage $V_{k,i}$, and a threshold voltage $V_{T,i}$. Furthermore, the sub-amplifiers do not need to be of the same size, or even the same technology. Hence the subscript *i* which relates to the main or auxiliary amplifier when replaced with *m* or *a*, respectively. Note that the model does not account for compression. To avoid unrealistic results it is therefore important that the output voltage swing of the sub-amplifiers never enters the knee-region.

4.3.2 Analysis

The equations needed for analyzing how the modified DPA depends on $V_{GS,i}$, $V_{DS,i}$, β , ϕ , etc., are derived in [C]. The equations are there used to analyze the modified DPA when the values of $V_{T,i}$, $g_{m,i}$, $I_{max,i}$, and $V_{k,i}$ are selected to correspond to $10 \times 100 \ \mu$ m devices from the TriQuint 3MI 0.25 μ m GaN-HEMT MMIC process, see Table 4.2. The analysis assumes equal size of the sub-amplifiers and the subscript *i* is therefore omitted. The most important results are shown in Fig 4.8 and are discussed below.

Fig. 4.8a shows the frequency response of the drain efficiency when using the parameter values in Table 4.3 where the phase balance $\phi = -90^{\circ}$ is assumed to be frequency independent. As can be seen, the drain efficiency is nearly independent of frequency over a 40% bandwidth. The ideal theoretical analysis in [B] suggested that the phase balance ϕ should be both power dependent and inversely proportional to the frequency. Such a behavior is however very difficult to obtain in a single RF-input configuration. The result in Fig. 4.8a is therefore important since it shows that the bandwidth also is large for a phase balance that easily can be obtained in a real implementation, e.g. by using a Lange coupler. It should be noted that the amplitudes of V_m and V_a associated with the $0.8f_0$ and $1.2f_0$ -curves in Fig. 4.8a exceed their maximum allowed values by 0.5 V and 0.6 V, respectively. Hence the drain



Figure 4.8: Calculated drain efficiency versus output power for, (a) different normalized frequencies, and (b) different combinations of $V_{DS,m}$ and $V_{GS,a}$. The technology-, circuit-, and bias-parameters are as given in Tables 4.2–4.3.

| Parameter | Modified DPA | Standard DPA |
|----------------|--------------|--------------|
| ξ_b | 0.39 | 0.39 |
| $Z_C (\Omega)$ | 68 | 123 |
| $R_L (\Omega)$ | 68 | 48 |
| $\phi \ (deg)$ | -90 | $-90f/f_{0}$ |
| β | 1.26 | 2.73 |
| $V_{DS,m}$ (V) | 12.5 | 28 |
| $V_{DS,a}$ (V) | 28 | 28 |
| $V_{GS,m}$ (V) | -3.1 | -3.1 |
| $V_{GS,a}$ (V) | -4.43 | -4.63 |

Table 4.4: Parameter values used when calculating the curves in Figs. 4.9-4.12.

efficiency is somewhat overestimated compared to the case when compression is included in the model. In this particular case, the overshoot is small and the effect on the calculated drain efficiency is nearly negligible. However, if the same calculations are performed for larger bandwidths the effect becomes more significant.

As discussed in the previous section, the efficiency of the modified DPA can be reconfigured if $V_{DS,m}$ and I_a can be controlled. For this reason it was suggested that a dual RF-input configuration might be useful since it enables control of I_a . However, I_a can also be controlled by adjusting $V_{GS,a}$ and it is therefore analyzed whether the efficiency can be reconfigured by changing the values of $V_{GS,a}$ and $V_{DS,m}$. The result is shown in Fig. 4.8b and clearly shows that the efficiency profile can be reconfigured to match the statistics of the signal being transmitted, also for the single RF-input configuration.

In summary, the results of this analysis show that the modified DPA indeed has interesting properties also in a single RF-input configuration. The analysis also gives useful indications on how to select the input network properties and the bias levels. These findings are used to design a MMIC GaN DPA as presented in [C]. The results from that design are reviewed later in this chapter.



Figure 4.9: The load-lines for the modified DPA when using the schematic in Fig. 4.7 together with the values in Table 4.2 and Table 4.4.



Figure 4.10: The load-lines for the standard DPA when using the schematic in Fig. 4.7 together with the values in Table 4.2 and Table 4.4.

4.3.3 Comparison with the standard DPA

The schematic in Fig. 4.7 is not only valid for the modified DPA but also for the standard DPA. The equations in [C] are therefore applicable for the standard DPA with the exception that equation (9) in [C] has to be replaced with equation (2.5). Hence, a comparison of the single RF-input standard and modified DPA can be made. To facilitate such a comparison, the device parameters in Table 4.2 are used, which implies that the maximum device size will be fixed to $10 \times 100 \ \mu$ m. The parameter values used for each amplifier are summarized Table 4.4 where the impedances of the standard DPA are selected so that the maximum current of the auxiliary amplifier equals $I_{max,a} = 750$ mA. It is important to note that the values of $V_{GS,a}$ and β for the modified DPA in Table 4.4 are slightly adjusted compared to the values used in Table 4.3. This done to ensure that none of the output voltages enter the knee-region when performing the analysis below.

The resulting load-lines are shown in Figs. 4.9–4.10. The figures show that the lower $V_{DS,m}$ of the modified DPA gives a lower voltage swing. As discussed in Section 4.2, this implies that the modified DPA has a lower peak power than the standard DPA. However, the modified DPA utilizes more of the available current, thereby to some degree compensating for the lower drain bias voltage.



Figure 4.11: The drain efficiency for, (a) the modified DPA, and (b) the standard DPA, when using the schematic in Fig. 4.7 together with the values in Table 4.2 and Table 4.4.



Figure 4.12: The voltage gain for, (a) the modified DPA, and (b) the standard DPA, when using the schematic in Fig. 4.7 together with the values in Table 4.2 and Table 4.4.

The result is that the calculated peak power is 38.3 dBm for the standard DPA and 36.8 dBm for the modified DPA. Thus, there is a 1.5 dB difference in peak power between the two amplifiers in this particular case.

The calculated drain efficiency for each amplifier is shown in Fig. 4.11. As can be seen, the modified DPA has a nearly frequency independent drain efficiency whereas the drain efficiency of the standard DPA is strongly frequency dependent. However, the standard DPA has a higher back-off efficiency at the center frequency. This is because the standard DPA has a larger ratio between $V_{DS,m}$ and V_k which makes its efficiency less affected by the knee-voltage. On the other hand, this difference may very well be less pronounced in real implementations due to knee walk-out effects associated with large drain bias voltages in GaN transistors [64].

It is also interesting to compare the gain of the two amplifiers. However, since the input impedances of the sub-amplifiers are assumed to be infinite, voltage gain has to be used instead of power gain. The result is shown in Fig. 4.12 where it can be seen that the modified DPA also has a significantly larger gain-bandwidth compared to the standard DPA. Moreover, it can also be seen that the center frequency gain is nearly identical for the two amplifiers.

This is somewhat surprising since the larger β of the standard DPA indicates that its voltage gain should be lower than for the modified DPA. However, the load impedance seen by the main amplifier is larger than for the modified DPA which in this example nearly perfectly counteracts the difference in β .

The conclusion from this comparison is that the single RF-input modified DPA has the ability to provide much more wideband performance compared to the single RF-input standard DPA at the cost of a slightly lower peak power and center frequency back-off efficiency.

4.4 Demonstrator circuits

To validate the theory and to demonstrate the utility of the modified DPA, [B] and [C] presents the design and measurements of two demonstrator circuits. This section reviews the reported measurement results and compares them to what is predicted by the theory.

4.4.1 Dual RF-input circuit

The purpose of the circuit presented in [B] is to provide a proof of concept of the modified DPA. The circuit is therefore implemented with dual RF-inputs which allows the circuit to be designed and operated in better agreement with the ideal theory in [B]. The design goal was to maximize performance over a widest possible bandwidth centered at 2.14 GHz.

As discussed in Chapter 3, the bandwidth of the DPA is to a large degree determined by its output network. So is also the case for the modified DPA and the impedance inverter is therefore designed using the QL-network described in Section 3.3.1. The targeted characteristic impedance of the impedance inverter is $Z_C = 28 \ \Omega$ and the output parasitics of the devices are represented by 0.9 pF shunt capacitances.

The simulated performance of the impedance inverter is shown in Fig. 4.13. Comparing the phase of S_{21} with the result in Fig. 4.3 indicates that it should be possible to obtain good performance over nearly the entire simulated frequency range of 1.7–2.6 GHz. The exception is frequencies in the higher side of the band where the phase of S_{21} starts to deviate significantly from values that according to Fig. 4.3 corresponds to high efficiency. The amplitude of S_{11} also shows that it cannot be assumed that the characteristic impedance is



Figure 4.13: Simulated S-parameters of the impedance inverter used in the circuit in Fig. 4.14. The reference impedance is set to 28Ω .



Figure 4.14: Photo of the dual RF-input 1.5–2.4 GHz hybrid circuit presented in [a,B].



Figure 4.15: The measured drain efficiency versus output power at different frequencies when $V_{DS,m} = 17.5$ V, $V_{DS,a} = 30$ V, $V_{GS,m} = -2.8$ V, and $V_{GS,a} = -4.5$ V.

28 Ω at frequencies in the lower end of the simulated band. Despite this, the circuit simulations presented in [B] still shows more than 47% PAE at both full output power and at 6 dB OPBO all across the 1.7–2.6 GHz frequency range. The assembled dual RF-input demonstrator circuit is shown in Fig. 4.14 and measures 140 mm \times 120 mm.

The measured drain efficiency at 1.6, 2.0 and 2.4 GHz is plotted versus output power in Fig. 4.15. The main and auxiliary amplifiers drain biases are set to 17.5 V and 30 V, respectively, thereby giving $\xi_b = 0.5$ if accounting for 5 V knee-voltage. As observed, the drain efficiency in back-off is almost identical at all three frequencies which is in good agreement with the theory.

Fig. 4.16 shows the drain efficiency and PAE versus frequency at full output power (42 dBm) and at 6 dB OPBO (36 dBm). The result shows that the drain efficiency is larger than 50%, at both full output power and at 6 dB OPBO, from 1.5 to 2.4 GHz. Unfortunately, the measured gain at 6 dB OPBO drops below 8 dB above 2.1 GHz which is not predicted by the simulations. For this reason, the back-off PAE is reduced above 2.1 GHz as shown in Fig. 4.16b.

The frequency band where best measured performance is obtained is shifted 5–10% down in frequency compared to the simulations. The reason for this is not fully understood but is most likely due to discrepancies between the passive and active models and their physical components. Despite this, the measurements confirm the wideband capabilities of the modified DPA.



Figure 4.16: The measured (a) drain efficiency, and (b) PAE at full output power (42 dBm) and at 6 dB output power back-off (36 dBm) versus frequency when $V_{DS,m} = 17.5$ V, $V_{DS,a} = 30$ V, $V_{GS,m} = -2.8$ V, and $V_{GS,a} = -4.5$ V.



Figure 4.17: The measured drain efficiency versus output power at 2.0 GHz for different main amplifier drain biases when $V_{DS,a} = 30$ V, $V_{GS,m} = -2.8$ V, and $V_{GS,a} = -4.5$ V.

The predicted efficiency reconfiguration is verified by measuring the drain efficiency versus output power for different values of the main amplifier bias $V_{DS,m}$. The result, shown in Fig. 4.17, demonstrates a distinct agreement with Fig. 4.2b thereby confirming the theory.

Modulated measurements of the demonstrator circuit are presented in [e] where different types of modulation schemes and sample rates are investigated. The measurements are made at 2.0 GHz and the signal used is a 5 MHz LTE-signal with 8.5 dB PAPR. Fig. 4.18 shows the spectrum before and after DPD when using a sample rate of 25 MHz. The corresponding average PAE is 42.4% and the NMSE and ACPR are measured to -43.7 dB and -55.8 dBc respectively.

The outcome of the measurements does indeed confirm both the wideband performance and the reconfigurability, predicted by the theory. In addition, even though more wideband designs have been presented [57, 59], [D, E] after the time of publication in [a,B], the fractional bandwidth is still among the largest reported for any DPA.



Figure 4.18: Measured spectrum before and after DPD for a 5 MHz 8.5 dB PAPR LTE-signal when $V_{DS,m} = 17.5$ V, $V_{DS,a} = 30$ V, $V_{GS,m} = -2.8$ V, and $V_{GS,a} = -4.5$ V [e].

4.4.2 Single RF-input circuit

The circuit in [C] is designed to demonstrate the utility of the single RFinput analysis presented in Section 4.3, and to show that the modified DPA is suitable for MMIC implementations. The circuit targets the same microwave PTP-link applications as the circuit in [A], and it is designed in the same GaN MMIC process, and aims for the same center frequency. Hence, a direct comparison between the circuits in [C] and [A] provides a good indicator of how the performance of the modified DPA compares to the standard DPA in a real implementation.

As for the circuits in [A] and [B], the overall performance of the circuit is much dependent on the impedance inverter. Unfortunately, since the modified DPA utilizes asymmetrical drain bias, the Tee-line network used in [A] cannot be directly used. However, good impedance inverter properties were obtained by cascading two Tee-line networks, each having an electrical length of $\approx 45^{\circ}$ at 7.3 GHz. The targeted characteristic impedance of the impedance inverter is $Z_C = 68 \ \Omega$ and the output parasitics of the devices are represented by 0.47 pF shunt capacitances.

The simulated S-parameters of the impedance inverter are shown in Fig. 4.19. As can be seen, $|S_{11}| < -13$ dB, and $\angle S_{21}$ varies from -41° to -130° , across a 5.8–8.8 GHz frequency range. Comparing the results in Fig. 4.19 with the theoretical efficiency dependence on $\angle S_{21}$ in Fig. 4.3 shows that the modified



Figure 4.19: Simulated S-parameters of the impedance inverter used in the circuit in Fig. 4.20. The reference impedance is set to 68Ω .



Figure 4.20: Photo of the single RF-input 5.8–8.5 GHz GaN MMIC circuit presented in [C].



Figure 4.21: The measured PAE versus output power (a), and frequency (b) when $V_{DS,m} = 12.5$ V, $V_{DS,a} = 28$ V, $V_{GS,m} = -2.52$ V, and $V_{GS,a} = -4.85$ V.

DPA thereby should be able to support a bandwidth considerably larger than what was obtain with the circuit in [A]. The fabricated MMIC chip measures $2.9 \text{ mm} \times 2.9 \text{ mm}$ and is depicted in Fig. 4.20.

The measured PAE is shown in Fig. 4.21. As can be seen, the PAE at 9 dB OPBO is larger than 31% all across a 5.8–8.8 GHz frequency range, constituting a 41% fractional bandwidth. This is considerably larger than the 6.7–7.8 GHz frequency range for which the circuit in [A] has a PAE larger than 31% at 9 dB OPBO, thereby clearly demonstrating the advantage of the modified DPA.

Modulated measurements are made with a 20 MHz 256-QAM signal having 8.5 dBm PAPR. The DPD employed the same VS-GMP behavioral model as used for the measurements in [A]. The result is shown in Fig. 4.22 where it can be seen that PAE_{avg} is larger than 32% across the 5.8–8.8 GHz frequency range, which is in good agreement with the results in Fig. 4.21. The corresponding ACPR and NMSE are lower than -46.6 dBc and -36.6 dB, respectively, over the same frequency range. The average output power $P_{out,avg}$ is maintained within 27.4 ± 0.4 dBm across the 5.8–8.8 GHz frequency range, corresponding to a peak power of 35.9 ± 0.4 dBm.

The efficiency reconfiguration is verified by measurements at several frequencies. Fig. 4.23 shows the result at 6.4 GHz and 7.8 GHz. As can be seen,



Figure 4.22: Measured PAE_{avg}, $P_{out,avg}$, NMSE and ACPR after DPD versus frequency for the 20 MHz 256-QAM signal with 8.5 dB PAPR. All measurements were made with the bias voltages $V_{DS,m} = 12.5$ V, $V_{DS,a} = 28$ V, $V_{GS,m} = -2.52$ V, and $V_{GS,a} = -4.85$ V.



Figure 4.23: Measured PAE versus output power at 6.4 GHz and 7.8 GHz for different combinations of $V_{DS,m}$ and $V_{GS,a}$. $V_{DS,a}$ and $V_{GS,m}$ were set to 28 V and -2.52 V, respectively, in all measurements.

the PAE is reconfigured in good agreement with the theoretical prediction in Fig. 4.8b.

The raw linearity was also investigated and measurements show that very good performance can be obtained by optimizing the bias-levels. The best result is found at 7.0 GHz where the bias setting $V_{DS,m} = 12.5$ V, $V_{DS,a} = 28.0$ V, $V_{GS,m} = -2.47$ V, and $V_{GS,a} = -4.35$ V, gives an ACPR = -41.0 dBc, NMSE = -34.2 dB, and PAE_{avg} = 35.2%.

Comparing the results with what is reported for other published GaN MMIC DPAs [65–67], [A] shows that the reported efficiency-bandwidth for the circuit in [C] is by far the largest reported (see Table V in [C]).

As discussed in the beginning of this section, it is particularly interesting to compare the results with what was obtained for the circuit in [A] since it is made in the same process and has nearly the same center frequency. The almost twice as large bandwidth reported in this section thereby clearly illustrates the qualities of the modified DPA.

4.5 Chapter summary

This chapter has addressed the inherent bandwidth limitation of the DPA. It has been shown that the modified DPA has both a significantly larger inherent bandwidth compared to the standard DPA as well as reconfigurable efficiency.

Two demonstrator circuits were presented in order to verify the theoretical findings. Measurements showed that both circuits provided state-of-the-art performance in terms of bandwidth. The measurements also convincingly verified the efficiency reconfigurability. The results thereby prove the utility of the modified DPA and shows that it is a serious candidate for designing wideband power amplifiers with high PAE in back-off.

Chapter 5

Reaching super-octave bandwidth

It was shown in the previous chapter that the modified DPA theoretically can support bandwidths larger than one octave. However, although the demonstrator circuits had state-of-the-art performance, their bandwidths were still clearly lower than the theoretical performance. The main reason for this is the non-ideal frequency response of the impedance inverter, imposed by the need of compensating for the device output parasitics. In addition, the theory of the modified DPA is based on an assumption of short circuit harmonics which seldom is practically achievable, especially not in wideband designs.

An alternative method to extend the DPA bandwidth is to utilize the Doherty-outphasing continuum, originally proposed in [68]. As will be shown, this ideally enables bandwidths even larger than the modified DPA. However, the idea is based on the same ideal assumptions as the modified DPA, i.e. short circuit harmonics and ideal current sources. Just as for the modified DPA, the output parasitics and harmonic terminations will therefore limit the practical bandwidth also for an amplifier based on the Doherty-outphasing continuum. To enable bandwidth larger than one octave, the work in [D,E] evolves the idea of the Doherty-outphasing continuum by presenting a linear multi-harmonic analysis method that also accounts for output parasitics and non-ideal harmonic terminations.

This chapter will first show how the Doherty-outphasing continuum is found and what its implications are. The linear multi-harmonic method proposed in [D,E] is thereafter presented and it is shown how the method is used to find output networks that enable practical bandwidths even larger than 100%. Finally, the design and characterization of a dual RF-input amplifier, designed according to the findings from the linear multi-harmonic analysis, is presented.

5.1 The Doherty-outphasing continuum

The schematic of the output network used to derive the Doherty-outphasing continuum is depicted in Fig. 5.1. As for the ideal theory describing the



Figure 5.1: Ideal output network schematic used to derive the Dohertyoutphasing continuum.



Figure 5.2: (a) Scatter plot of the drain efficiency versus output power for the network in Fig. 5.1 when $\theta_m = 90^\circ + m \cdot 180^\circ$ and $\theta_a = 0^\circ + n \cdot 180^\circ$, m, n = 0, 1, 2, ... (b) The current control functions corresponding to the optimum efficiency η_{opt} indicated by the red line in (a).

standard and modified DPAs, the sub-amplifiers are modeled as ideal half wave rectified voltage controlled current sources having identical transconductance, short circuit harmonics, zero knee-voltage, and drain-bias voltages $V_{DS,m}$ and $V_{DS,a}$.

The Doherty-outphasing continuum is found by analyzing how the average drain efficiency depends on θ_m and θ_a when the remaining circuit values are held constant. To facilitate such an analysis, a numerical brute-force method is used where the output power and drain efficiency are calculated for a large set of combinations of current amplitudes $|I_m|$, $|I_a|$, and phase balances $\phi = \angle I_a/I_m$. Doing so yields a scatter-plot of drain efficiency versus output power from where the optimum drain efficiency η_{opt} , and the corresponding values of $|I_m|$, $|I_a|$, ϕ , can be extracted versus output power.

For example, the standard DPA-parameters $\theta_m = 90^\circ$, $\theta_a = 0^\circ$, $Z_{C,m} = Z_{C,a} = R_{opt}$, $R_L = R_{opt}/2$, gives the result in Fig. 5.2. As can be seen, both the optimum efficiency η_{opt} , indicated by the red line, and the corresponding current control, are identical to what is analytically derived in Chapter 2.

Using the described method, η_{opt} is extracted for each combination of θ_m and θ_a when $Z_{C,m} = Z_{C,a} = R_{opt}$, $R_L = R_{opt}/2$, $V_{DS,m} = V_{DS,a}$. With η_{opt} known, (1.1) is used to calculate the average drain efficiency for the 6.7 dB PAPR WCDMA-signal, for each combination of θ_m and θ_a . The result is shown in Fig. 5.3 where it can be seen that the average efficiency varies from less than 45% up to more than 70%, depending on the values of θ_m and θ_a . It should be noted that the peak power is constant through out the figure.



Figure 5.3: The average drain efficiency as a function of θ_m and θ_a for the 6.7 dB WCDMA-signal under optimum current control. The diamonds (\diamondsuit) and squares (\Box) indicates Doherty and outphasing solutions, respectively.



Figure 5.4: Scatter plot of the drain efficiency versus output power for the network in Fig. 5.1 when $\theta_m = 60^\circ + m \cdot 180^\circ$ and $\theta_a = 120^\circ + n \cdot 180^\circ$, m, n = 0, 1, 2, ... (b) The current control functions corresponding to the optimum efficiency η_{opt} indicated by the red line in (a).

Assuming the electrical lengths θ_m and θ_a at the design frequency f_0 , the frequency response of η_{avg} is given by a straight line that passes through the origin and (θ_m, θ_a) . Hence, Fig. 5.3 can be used to find how the frequency response of η_{avg} depends on the f_0 -values of θ_m and θ_a . For example, the red trace that passes through (90,0) at f_0 represents the frequency response for the DPA. It should however be noted that the numerical method used to derive the result implies optimum current control at each frequency. The red trace in Fig. 5.3 should therefore be interpreted as what ideally can be achieved for a dual RF-input DPA.

Fig. 5.3 also shows a blue trace representing the frequency response when $\theta_m = 90^\circ$ and $\theta_a = 180^\circ$ at f_0 . As can be seen, the average drain efficiency is maintained high over a significantly larger range than for the red trace. A very interesting finding is made when analyzing how the mode of operation varies along the blue trace: For example, the mode of operation at f_0 is identical to what is shown in Fig. 5.2 due to the 180° periodicity of transmission lines. That



Figure 5.5: The average drain efficiency versus frequency for the red (Dual RF-input DPA) and blue (Doherty-outphasing continuum) traces in Fig. 5.3. For reference the results for the standard and modified DPAs are also shown (previously reported in Fig. 2.9 and Fig. 4.4). The signal used is the 6.7 dB PAPR WCDMA signal.

is, the amplifier behaves as a DPA. On the other hand, at $0.67f_0$ ($\theta_m = 60^\circ$, $\theta_a = 120^\circ$); and $1.33f_0$ ($\theta_m = 120^\circ$, $\theta_a = 240^\circ$), the optimum efficiency-trace and current control are as shown in Fig. 5.4. In this case, the amplifier behaves as an outphasing amplifier where the amplitudes of I_m and I_a are equal while the phase balance ϕ changes. Hence, the mode of operation varies from outphasing (\Box), to Doherty (\diamondsuit), and back to outphasing (\Box) when moving along the trace. This is referred to as the Doherty-outphasing continuum.

The cross-sections of η_{avg} for the dual RF-input DPA and the Dohertyoutphasing continuum traces in Fig. 5.3 are shown in Fig. 5.5. For comparison, Fig. 5.5 also includes η_{avg} for the standard and modified DPAs when $\xi_b = 0.5$, previously shown in Fig 2.9 and Fig 4.4. The figure clearly shows that the Doherty-outphasing continuum, for which $\eta_{avg} > 64\%$ across a 100% fractional bandwidth, has the most wideband performance of all the DPA-variants presented in this thesis. In fact, to the best of the author's knowledge, the Doherty-outphasing continuum has a larger theoretical bandwidth than any other variant of the DPA found in literature.

Finally, it is interesting to note that using $\theta_m = 90^\circ$, $\theta_a = 180^\circ$ to obtain large bandwidth shows large similarities to the recently proposed topologies [57–59] discussed in the introduction to Chapter 4.

5.2 Realistic conditions

As shown in the previous section, the Doherty-outphasing continuum gives an average drain efficiency that is maintained high over more than 100% bandwidth. However, the ideal conditions used when deriving the continuum cannot be expected in a real implementation. Hence, the practical bandwidth of the Doherty-outphasing continuum is limited by the output parasitics and the non-ideal harmonic terminations, just as for the modified DPA. In [D,E], a linear multi-harmonic calculation method for calculating the efficiency and output power under more realistic conditions is suggested. What differentiates this method from the one used in the previous section is that no assumption of harmonic terminations are made up to the harmonic order N > 1. All currents and voltages are therefore calculated up to this order. Also, the output



Figure 5.6: Schematic of the non-ideal output network used when performing the linear multi-harmonic calculations.

| Table 5.1: Design parameter values and | l bandwidth | performance of f | our differ- |
|--|-------------|------------------|-------------|
| ent circuits (A-D). | | | |
| | | | |

| Circuit | Signal (PAPR) | X_{Cout}/R_{opt} | $Z_{C,m}/R_{opt}$ | $Z_{C,a}/R_{opt}$ | R_L/R_{opt} |
|------------------|--------------------------|--|--|--|--|
| | | (a) f_0 | | | |
| А | WCDMA (6.7 dB) | 6.0 | 1.0 | 1.0 | 0.5 |
| В | WCDMA (6.7 dB) | 1.0 | 1.0 | 1.0 | 0.25 |
| \mathbf{C} | LTE (9.0 dB) | 6.0 | 0.5 | 1.0 | 0.5 |
| D | LTE (9.0 dB) | 1.0 | 0.5 | 1.0 | 0.25 |
| | | | | | |
| Circuit | $V_{DS,a}/V_{DS,m}$ | X_L/R_{opt} | $	heta_m$ | $	heta_a$ | $\eta_{avg} \ge 50\%$ |
| | | | ~ ^ | ~ ^ | |
| | | @ f_0 | @ f_0 | @ f_0 | BW (%) |
| A | 1.0 | 0.125 | $\frac{@ f_0}{31^{\circ}}$ | $\frac{@ f_0}{73^{\circ}}$ | BW (%) 108 |
| A B | 1.0 0.7 | $ \begin{array}{r} @ f_0 \\ 0.125 \\ 0.25 \\ \end{array} $ | | | BW (%) 108 56 |
| A B C | 1.0 0.7 0.7 | $\begin{array}{c c} @ f_0 \\ \hline 0.125 \\ 0.25 \\ 0.125 \\ \hline \end{array}$ | $ \begin{array}{c} @ f_0 \\ 31^{\circ} \\ 5^{\circ} \\ 135^{\circ} \end{array} $ | $ \begin{array}{c} @ f_0 \\ 73^{\circ} \\ 25^{\circ} \\ 60^{\circ} \end{array} $ | $ BW (\%) \\ 108 \\ 56 \\ 58 58 $ |
| A B C D | 1.0 0.7 0.7 0.5 | $\begin{array}{c c} @ f_0 \\ \hline 0.125 \\ 0.25 \\ 0.125 \\ 0.25 \\ 0.25 \\ \end{array}$ | $\begin{array}{c} @ f_0 \\ \hline 31^{\circ} \\ 5^{\circ} \\ 135^{\circ} \\ 10^{\circ} \end{array}$ | $ \begin{array}{c} @ f_0 \\ 73^{\circ} \\ 25^{\circ} \\ 60^{\circ} \\ 20^{\circ} \end{array} $ | $ \begin{array}{r} BW (\%) \\ 108 \\ 56 \\ 58 \\ 42 \\ \end{array} $ |

network, shown in Fig. 5.6, is made more realistic by introducing bond-wire inductances and by using the simplified device model in Fig. 3.1. Hence, scatter plots of the efficiency versus output power can be calculated in a similar way to what was done in the previous section but under more realistic conditions.

Using the proposed method, the frequency response for the circuit in Fig. 5.6 is calculated for a large set of circuit parameter values. Table 5.1 shows the optimum parameter values found for four different combinations of signal PAPR and output capacitances when assuming equally sized devices. The values of X_{Cout}/R_{opt} (1.0 and 6.0, respectively) are chosen to illustrate the dependence on different device technologies and/or frequencies. Note that all the values are given at the design frequency f_0 and are normalized to R_{opt} , thus making the result scalable and transferable in terms of power levels, drain bias conditions, and frequency. The corresponding frequency response of η_{avg} and P_{max} are reported in Fig. 5.7. Defining the bandwidth as the frequency range for which $\eta_{avg} \geq 50\%$ gives the bandwidths indicated tabulated in Table 5.1. The largest bandwidth is reported for Circuit A and measures 108% which is in-line with previous observations that low PAPR and small C_{out} gives larger bandwidths.

5.3 Circuit implementation

The validity of the results reported in the previous section are examined in [D,E] by the design and characterization of Circuit A. The circuit is implemented using 15 W GaN devices (Cree CGH60015D) having $R_{opt} = 27 \Omega$ and



Figure 5.7: The calculated average drain efficiency and peak power for the circuits in Table 5.1. The peak power is given relative to the peak power of a standard DPA using the same device sizes as used for the circuits in Table 5.1.

 $X_{Cout}/R_{opt} = 6$ at $f_0 = 1.15$ GHz. Implementing the circuit is straightforward since it is made in exact correspondence with Table 5.1. Hence, the output network consists of two transmission lines with the characteristic impedance $Z_{C,i} = 27 \ \Omega$ and the electrical lengths $\theta_m = 31^\circ$ and $\theta_a = 73^\circ$. The desired load impedance is realized by a stepped impedance transformer that transforms 50 Ω to $R_L = 13.5 \ \Omega$. Each of the input networks are realized with a stepped impedance inverter that together with a stabilizing network ensures stability without sacrificing to much gain. The required control of I_m and I_a is enabled using a dual RF-input configuration. The assembled circuit measures 166 mm \times 81 mm and is depicted in Fig. 5.8.



Figure 5.8: Photo of the assembled circuit.

5.4 Measurement results

The CW-measurements are made by sweeping the amplitude and phase of the RF-input signals over a large range of values. The result is shown for a



Figure 5.9: Measured PAE versus output power for different driving conditions and frequencies. The red lines shows the maximum PAE (PAE_{opt}) versus frequency.

Table 5.2: Summary of results from modulated measurements with DPD.

| Freq. | $P_{out,avg}$ | PAE_{avg} | NMSE | ACLR |
|--------------------|---------------------|-------------|---------|---------------------|
| $1.2 \mathrm{GHz}$ | 36.1 dBm | 50% | -46 dB | -61 dBc |
| $2.3~\mathrm{GHz}$ | $35.3~\mathrm{dBm}$ | 40% | -42 dB | $-57 \mathrm{~dBc}$ |

selection of frequencies in Fig. 5.9 and is used to identify the driving conditions that gives the optimum PAE (PAE_{opt}) at each frequency.

Fig. 5.10 shows the measured performance at 6 dB OPBO and at peak power, which varies between 43.1 and 44.9 dBm, versus frequency. The figure shows that the PAE at 6 dB OPBO is larger than 45% across the 1.0–3.0 GHz frequency range. Unfortunately, measured S-parameters of the amplifier indicates that the realized input matching network cannot provide a good input match above 3.0 GHz. The result is a rapidly dropping gain above 3.0 GHz and consequently decreased PAE. In addition, the low gain in combination with a lack of sufficient pre-drivers prevented measurements above 3.1 GHz. Despite this problem, the circuit is one of the most wideband PAs with enhanced back-off efficiency ever reported.

In order to evaluate the usefulness of the circuit in real applications, the PA is further characterized by modulated and linearized measurements at 1.2 and 2.3 GHz for the 6.7 dB PAPR WCDMA signal. Although the circuit was driven 2–3 dB below its peak power, the results in Fig. 5.11 and Table 5.2 clearly shows that it can be properly linearized



Figure 5.10: Measured power added efficiency and gain under optimum driving conditions.



Figure 5.11: Measured spectrum before and after DPD for the 5 MHz 6.7 dB PAPR WCDMA-signal.

5.5 Chapter summary

This chapter has addressed the issues of designing DPA with super-octave bandwidths in the presence of device parasitics and non-ideal harmonic terminations. It was shown that the Doherty-outphasing continuum ideally provides a bandwidth that is significantly larger than for both the standard and modified DPAs. However, since the Doherty-outphasing continuum is based on ideal conditions it does not solve the issue of device parasitics and non-ideal harmonic terminations. A linear multi-harmonic calculation method, inspired by the Doherty-outphasing continuum, that also accounts for output parasitics and non-ideal harmonic terminations was therefore proposed. By using this method, it was possible to design a circuit that provided high efficiency over a bandwidth significantly larger than one octave. The presented circuit utilizes dual RF-inputs and it can be argued that one of the largest benefits of the DPA has been sacrificed, i.e. its simplicity. However, it is reasonable to believe that there are applications where the increased complexity can be well motivated by the large bandwidth obtained.

Finally, it should be stressed that the presented circuit is a first try of utilizing the linear multi-harmonic calculation method. The full potential of the proposed method is therefore most certainly yet to come.

Chapter 6 Conclusions

The capacity and speed of the wireless data infrastructure constantly needs to be improved to meet the vast demand of wireless data. As discussed in the introduction, this has imposed new and more severe demands on the energy efficiency and frequency agility of the transmitter PAs.

The DPA has for many years been the workhorse in wireless transmitters thanks to its high energy efficiency and low complexity. The often narrowband performance does, however, make it difficult for the DPA to meet the increasing demands of frequency agility.

This thesis investigates the theoretical and practical bandwidth limitations of the DPA. It is acknowledged that the reasons why the DPA often becomes narrowband can be attributed to its inherent properties, and to the practical implementation of its output network. Three methods, that one-by-one enables the DPA to provide larger bandwidth, are therefore presented.

Experimental validation of the methods show that bandwidths larger than 40% are made possible for GaN MMIC single RF-input DPAs targeting microwave PTP-link applications. The excellent performance and high level of integration also makes integrated DPAs interesting candidates for use in massive MIMO-systems. Moreover, it is shown that enhanced back-off efficiency can be obtained for bandwidths larger than 100% when introducing dual RF-inputs. Although doing so inevitably increases the complexity of the transmitter, it is realistic to believe that it still can be motivated in applications with very high demands on performance.

The large bandwidths reported in this thesis shows that the DPA no longer needs to be considered as a necessarily narrowband amplifier and the major disadvantage of the DPA is thereby eliminated. Hence, the DPA might very well be the power amplifier of choice also in future wireless systems.

6.1 Future work

The bandwidth enhancing techniques proposed in this thesis are all implemented at low to medium power levels (<15 W) and their applicability in high power applications should be investigated. In particular, the parasitic absorbtion technique, used in the modified DPA circuits, might not be applicable at higher powers due to the associated large package and device parasitics. It should therefore be investigated how other parasitic compensation methods, that are more suitable for high power applications, affect the bandwidth of the modified DPA.

The linear multi-harmonic calculation method presented in [D,E] is better suited for high power levels since it can be adjusted to account for the necessary parasitics. The full potential of the method is however yet to explore. For example, its computational efficiency can be much improved by introducing more sophisticated optimization algorithms. This would for example enable the study of more complex output networks. The possibilities of applying the method on single RF-input configurations should also be investigated.

This thesis has not examined the frequency agility in terms of concurrent multi-band operations. The theoretical findings in [c] show that wideband performance not automatically implies correct functionality under such conditions. It should therefore be investigated how applicable the wideband techniques proposed in this thesis are for concurrent multi-band operation.

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Paper A

A Wideband and Compact GaN MMIC Doherty Amplifier for Microwave Link Applications

D. Gustafsson, J. Chani Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager

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Paper B

A Modified Doherty Power Amplifier With Extended Bandwidth and Reconfigurable Efficiency

D. Gustafsson, C. M. Andersson, and C. Fager

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Paper C

A GaN MMIC Modified Doherty PA with Large Bandwidth and Reconfigurable Efficiency

D. Gustafsson, J. Chani Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager

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Paper D

A 44 dBm 1.0–3.0 GHz GaN Power Amplifier with over 45% PAE at 6 dB Back-Off

D. Gustafsson, C. M. Andersson, R. Hellberg, and C. Fager

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Paper E

A 1–3 GHz Digitally Controlled Dual-RF Input Power-Amplifier Design Based on a Doherty-Outphasing Continuum Analysis

C. M. Andersson, D. Gustafsson, J. Chani Cahuana, R. Hellberg, and C. Fager

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