CHALMERS

Investigation and Implementation of a 10 MHz DC/DC Converter

For AESA Radar Applications

Master of Science thesis

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Gothenburg, Sweden 2014

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Abstract

The field of power electronics is under constant pursuit for devices with higher power density, improved efficiency, spectral purity, and low cost. In this thesis two DC/DC converter topologies converting 50 V to 30 V, with a maximum load of 6 W are implemented in hardware.

The two converter topologies implemented are a Buck converter and a ZVS-CV converter. The converters suitability to operate with a switching frequency of 10 MHz is evaluated. The Buck converter showed an overall peak efficiency of 80.8 %, with a switching frequency of 9.8 MHz. The Buck output power stage alone showed a peak efficiency of 87.2 %.

The ZVS-CV converter showed an overall peak efficiency of 76.1 % with a switching frequency of 9.0 MHz, and a peak output stage efficiency of 95.2 %. The higher efficiency for the output power stage of the ZVS-CV is a result of successful removal of switching losses in the switching transistor. The lower overall efficiency of the ZVS-CV converter is due to the need of a more complex control and driving circuit. However, it might be possible to improve the efficiency of the driver circuit in the ZVS-CV converter. The output voltage ripple in the Buck converter is approximately 500 mV compared to the 100 mV in the ZVS-CV converter.

The ZVS-CV converter is deemed well suited for 10 MHz operation. Future work should include implementation of a voltage regulator, development of a more efficient driver and control circuit, adaptive control of the dead time and an improved output filter to increase voltage quality.

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Erik Gustavsson
Niklas Hagman

Göteborg, Sweden, June 2014

List of Acronyms

AC – Alternating current

AESA – Active electronically scanned array

CAD – Computer-aided design

CCM – Continuous conduction mode

CV – Clamped voltage

DC – Direct current

DCM – Discontinuous conduction mode

ESR – Equivalent series resistance

FFT – Fast Fourier transform

GaN – Gallium nitride

IC – Integrated circuit

LDMOS – Laterally diffused metal oxide semiconductor

LDO – Low-dropout regulator

MOSFET – Metal oxide semiconductor field effect transistor

NMOSFET – N-type MOSFET

OP-amp – Operational amplifier

PCB – Printed circuit board

POL – Point of load

PWM – Pulse width modulation

Q-factor – Quality factor

rms – Root mean square

Si – Silicon

SMPS – Switched-mode power supply

ZCS – Zero current switched

ZVS – Zero voltage switched

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1 Introduction

This chapter gives a short background on why 10 MHz DC/DC converters are an interesting subject to investigate. The chapter also presents the purpose, aim and methods used for this thesis.

1.1 Background

The demand for high power density converters is high in applications where low weight and small physical size are important. The development and improvement of new and old converter topologies is under constant pursuit to improve power efficiency, reduce weight and size, and to improve voltage quality. Miniaturization of power converters through an increased switching frequency has been the work of decades and is responsible for the improved power density and reduced size of today's converters compared to those first introduced in the 1950s. By increasing the switching frequency energy storage elements, such as inductors and capacitors, can be decreased in both value and size. The use of smaller capacitors and inductors will result in converters with faster transient capabilities [1].

By reducing the size of converters it is possible to connect them closer to the loads they supply, this is called POL. The POL power architecture allows a higher system distribution voltage to be used since each load is supplied with a close connected converter; this will reduce resistive losses in the system [2].

Switching frequencies has moved from the kHz range into the MHz range of today's high performance power converters. This has been possible by the vast improvements made in semiconductor technology by reducing unwanted parasitic elements associated with high frequency switching losses and by taking advantage of circuit architectures absorbing the parasitic elements [3].

The use of switching frequencies in the 10-100 MHz range may open up for new methods of signal processing to improve spectral purity by limiting the effect of harmonics associated with the switching to propagate through the system. This is of special interest in an AESA radar system where disturbances can be interpreted as false radar echoes.

1.2 Purpose

The aim of this master thesis is to investigate suitable step down DC/DC converter topologies for a POL system architecture enabling the switching frequency to be raised to 10 MHz and beyond. A comparison between topologies should be performed and promising converter topologies will be implemented in hardware for further evaluation. Focus should lie on small physical size, high efficiency, high spectral purity and possibilities for voltage regulation.

A list of goals when designing the converter is

- 50 V input voltage
- 30 V output voltage
- ≥10 MHz switching frequency

- >80 % power efficiency
- 0-6 W output power
- <100 $mV_{peak\text{-}to\text{-}peak}$ output voltage ripple,
- <51 $dB\mu V_{rms}$ output voltage ripple for each frequency component. This equals <1 mV peak-to-peak voltage ripple for each frequency component.

1.3 Scope

Strategies for controlling and regulation of the output voltage will not be covered. Only converters able to regulate their output voltage with a constant switching frequency will be investigated. Furthermore, electromagnetic compatibility of the converter will not be covered and the necessary supply voltages for IC circuits in the converter are taken from the laboratory environment and will not be generated as a part of the converter.

Focus will lie on efficiency of the output stage of the converter. Driver and control circuit efficiency will not be optimized.

Since regulation of the output voltage is not investigated, converter functionality during pulsed loads will not be covered. A large filter is assumed to be connected between the DC/DC converter and the pulsed radar load. This results in a constant load as investigated in [4].

1.4 Method

A literature study will be carried out to review previous work and find suitable topologies for step down DC/DC converters. Promising converter topologies are further investigated through theory and simulations in the simulation software *LTspice*.

Components required for hardware implementation are selected and their electrical characteristics are mimicked in simulation models. Results from simulations are compared and evaluated to find the topologies most suited for hardware implementation.

The most promising topologies are implemented in hardware and evaluated through measurements. Results from measurements are compared with both theory and software simulations.

2 Theory

This chapter starts with a brief explanation on how the AESA radar system works and what that implies for the DC/DC converters. In the second part three DC/DC converter topologies are presented with their theoretical behavior and switching waveforms. Both advantages and disadvantages of each topology are identified and presented. The chapter ends with a theoretical background on important components, such as switching transistors and filter components.

2.1 AESA radar system

This section briefly explains the working principle of AESA radar and the system architecture.

2.1.1 Working principle

AESA radars are electronically scanned radars and does often have non-moving antennas. One advantage with AESA radar systems is the possibility to jump between different targets at different locations without moving the antenna. The working principle of an AESA radar is to use multiple transmitter elements, where each element is delayed in time and phase. A radar wave front is created through superposition of multiple radar waves from several radar elements; this is shown in Figure 1. An AESA radar antenna can be made of several hundreds or thousands of radar elements. These radar elements can be divided into smaller groups of elements where each group can scan for objects at different locations; several objects at different locations can be tracked simultaneously without moving the antenna head.

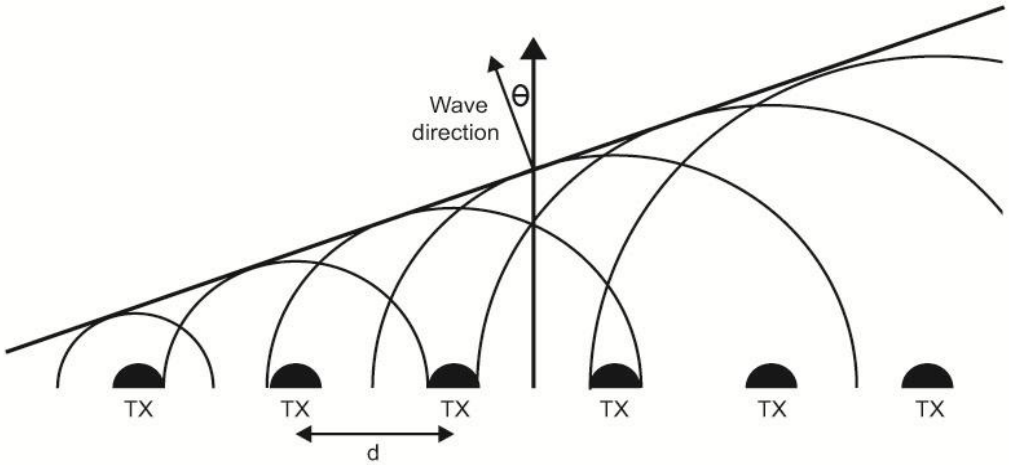

Figure 1. AESA radar wave formed through superposition of several antenna elements.

The load characteristic of a typical AESA radar element is shown in Figure 2. It is seen that the load is heavily pulsed. These pulses are reflected back into the power supply and can be harmful for the system, as well as give rise to false radar echoes. In order to deal with the radar pulses filters are often installed in the radar system. Often large capacitors are connected to both the in- and output of the DC/DC converter. The filter capacitors are bulky and for this reason unwanted, especially in airborne systems where weight and volume should be reduced. Instead of having large capacitors, active filters can be implemented to suppress reflected pulses. Active filters reduce

size and improve the performance compared to passive filters [4]. Another way to improve the performance of the DC/DC converter and reduce the need of large filters is to use a higher switching frequency. By raising the switching frequency both size and weight of the converter can be reduced.

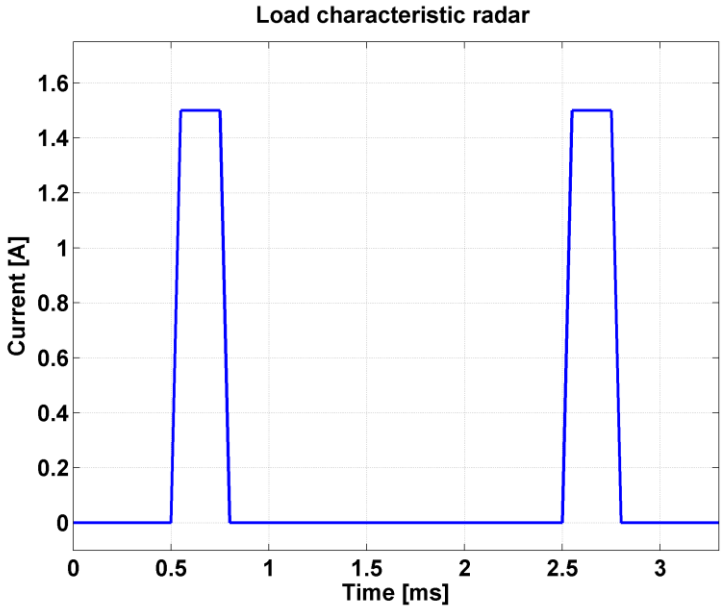

Figure 2. Typical load profile for an AESA radar element.

It is desired to have a DC/DC converter that uses PWM technique to regulate its output voltage since the switching frequency will be constant. A constant switching frequency will result in a simpler filter design and decrease the risk of false radar echoes.

If modulation techniques where variable frequencies are to be used to regulate the converter output voltage, the harmonics from the switching is not located at the same frequencies at all times. This would require a more complex filtering, as well as increased electromagnetic interference from the converter.

2.1.2 System architecture

An AESA radar system consist of several electric power converts, power amplifiers and radar elements. An overview of a simplified system architecture is seen in Figure 3.

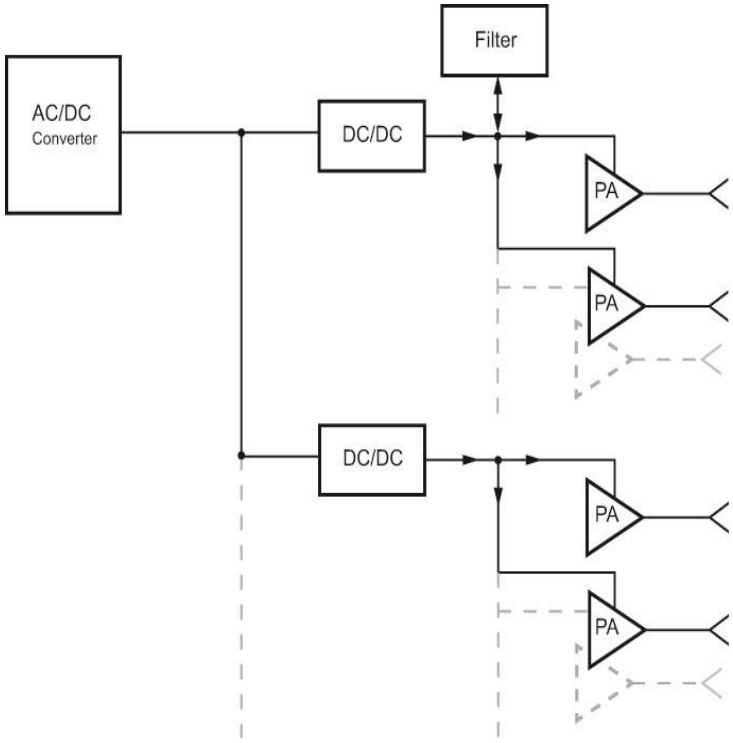

Figure 3. Overview of an AESA radar system architecture.

Often a high power AC/DC converter is used to convert electricity from the carrier's main power system into a DC distribution voltage. Connected to the larger converter are a lot of smaller DC/DC converters that further convert the voltage down to the voltage required by the radar elements. Each of the smaller converters supplies several radar elements through power amplifiers. Filters can be added to suppress the radar pulses from the radar elements and prevent them from reflecting back into the DC/DC converters and AC/DC converter. If the filter is added to the location shown in Figure 3, the output power from the DC/DC converter can be seen as constant [4].

2.2 DC/DC converter topologies

This section describes three different converter topologies that can be used for step-down voltage conversion. The first subsection describes the Buck converter. The second subsection continues with an investigation of a resonant-PWM Buck converter. The third subsection describes a ZVS-CV converter. Both the resonant-PWM Buck and the ZVS-CV converter are investigated due to their ability to remove switching losses and to regulate the output voltage with PWM.

2.2.1 Buck converter

The Buck converter is one of the most well-known step-down voltage converters. The Buck converter consists of a switch, a rectifying diode, an output inductor and an output capacitor as seen in Figure 4. The principle operation of the Buck converter

can be divided into two modes, CCM and the DCM. The current through the output inductor distinguishes the two modes; in CCM the current is continuous, while in DCM, the current will reach zero during the switching period [5].

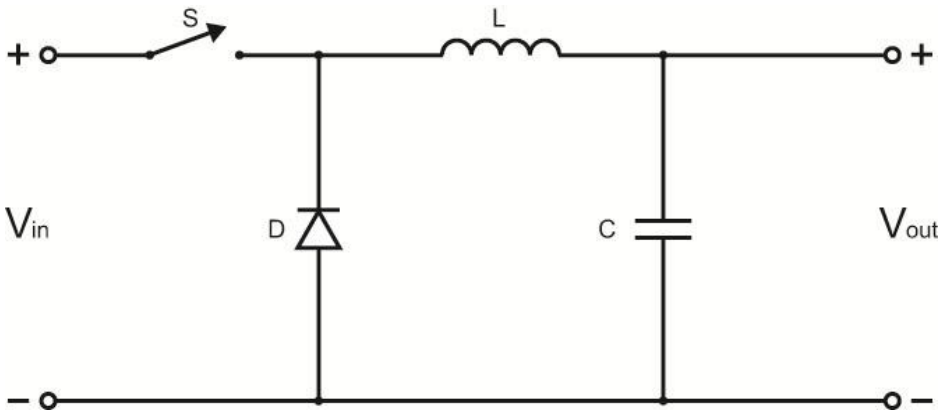

Figure 4. Buck converter.

2.2.1.1 Continuous Conduction Mode

A Buck converter operating in CCM has two different states, the on-state and the off-state. The on-state corresponds to when the switch is on and the voltage over the inductor is

$$V_L = V_{in} - V_{out} \tag{2.1}$$

The voltage applied over the inductor leads to a rise of the current according to

$$V_L = L\frac{di_L}{dt} \tag{2.2}$$

If the duration of the on-state is t_{on}, the change of the current through the inductor during the on-state is

$$\Delta i_L = \frac{V_L t_{on}}{L} = (V_{in} - V_{out})\frac{t_{on}}{L} \tag{2.3}$$

The current flows from the input, through the switch, inductor and to the load. In the on-state there is no current through the diode since it is reverse-biased. Figure 5 shows the on- and off-state, the inductor voltage and current for the Buck converter in CCM.

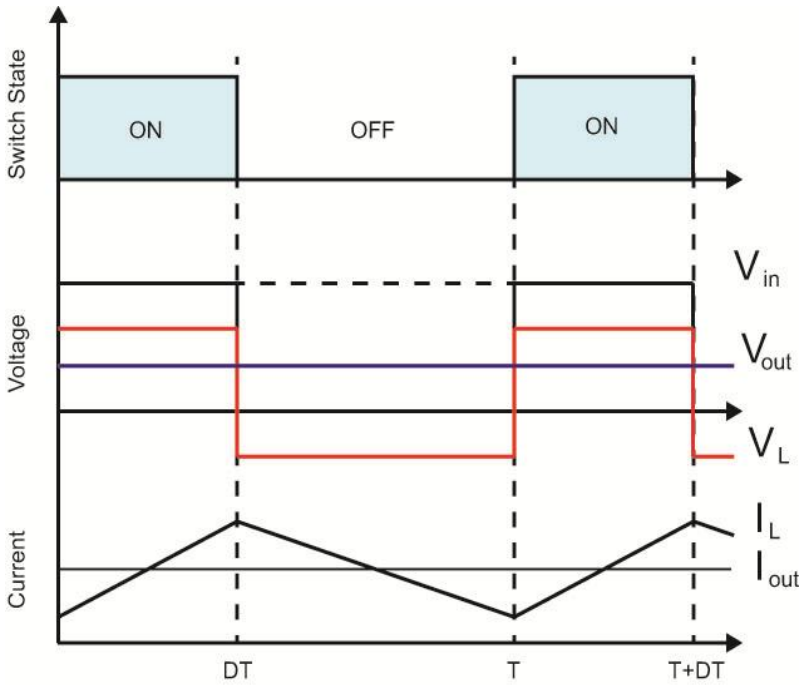

Figure 5. Voltage and current waveforms for the output inductor in a Buck converter operating in CCM.

The current paths during CCM are shown in Figure 6.

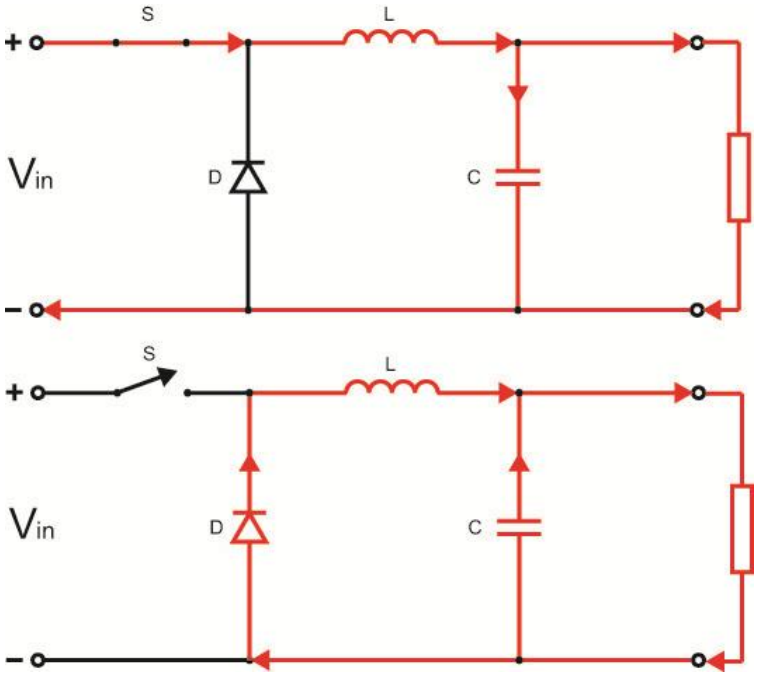

Figure 6. Current paths in the Buck converter during CCM.

During the off-state, the rectifying diode is forward-biased and the current freewheels through the diode, inductor and load. The voltage over the inductor during the off-state is

$$V_L = -V_{out} \tag{2.4}$$

The duration of the off-state is t_{off} and the current through the inductor changes as

$$\Delta i_L = -\frac{V_{out} t_{off}}{L} \tag{2.5}$$

The waveforms for the inductor current and voltage are shown in Figure 5, and the current path during the off-state is shown in Figure 6.

When the Buck converter is in steady state, the inductor current is equal in the beginning and the end of each switching period, this implies that (2.3) equals (2.5),

$$(V_{in} - V_{out})\frac{t_{on}}{L} = -\frac{V_{out} t_{off}}{L} \tag{2.6}$$

Writing t_{on} and t_{off} as

$$\begin{aligned} t_{on} &= DT_{sw} \\ t_{off} &= (1-D)T_{sw} \end{aligned} \tag{2.7}$$

where D is the duty-cycle and T_{sw} is the length of the switching period, (2.6) can be rewritten into

$$(V_{in} - V_{out})\frac{DT}{L} = -\frac{V_{out}(1-D)}{L} \tag{2.8}$$

or

$$V_{out} = DV_{in} \tag{2.9}$$

This results in an output voltage proportional to the duty-cycle in CCM.

2.2.1.2 Discontinuous Conduction Mode

If the average output current in the Buck converter is too low, the current through the inductor will be zero for some time during the off-state, the converter is in DCM. Figure 7 shows the switching states and the waveforms for the inductor voltage and current.

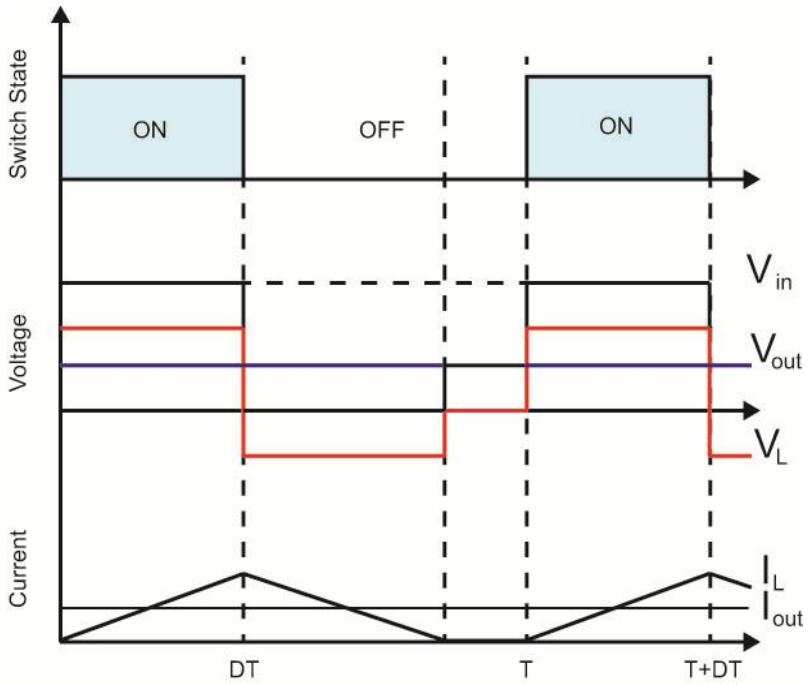

Figure 7. Voltage and current waveforms for the output inductor in a Buck converter operating in DCM.

It is observed that the on-state gives rise to an increasing inductor current and the off-state makes the inductor current fall again, just as for CCM. However, in DCM the current through the inductor falls to zero before a new switching period begins. The relation between input voltage, output voltage and duty-cycle in DCM can be expressed as

$$V_{out} = V_{in}\frac{D^2}{D^2 + \frac{1}{4}\frac{I_{out}}{I_{LB,max}}} \tag{2.10}$$

where I_{out} is the output current and $I_{LB,max}$ describes the magnitude of the current at the boundary between DCM and CCM with a duty-cycle of 0.5. $I_{LB,max}$ is expressed as

$$I_{LB,max} = \frac{T_{sw}V_{in}}{8L} \tag{2.11}$$

The boundary current for a D other than $D = 0.5$ is [5]

$$I_{LB} = 4I_{LB,max}D(1-D) \tag{2.12}$$

A difference between CCM and DCM is that the output voltage in CCM only depends on the input voltage and the duty-cycle, while the output voltage in DCM also depends on the output current, the length of the switching period and the inductance.

2.2.1.3 Output voltage ripple

In Sections 2.2.1.1 and 2.2.1.2, the output voltage has been assumed to be constant. This is not true since it would require an infinitely large capacitor at the output. In reality the voltage ripple is not zero and can be found by looking at the inductor current in Figure 8.

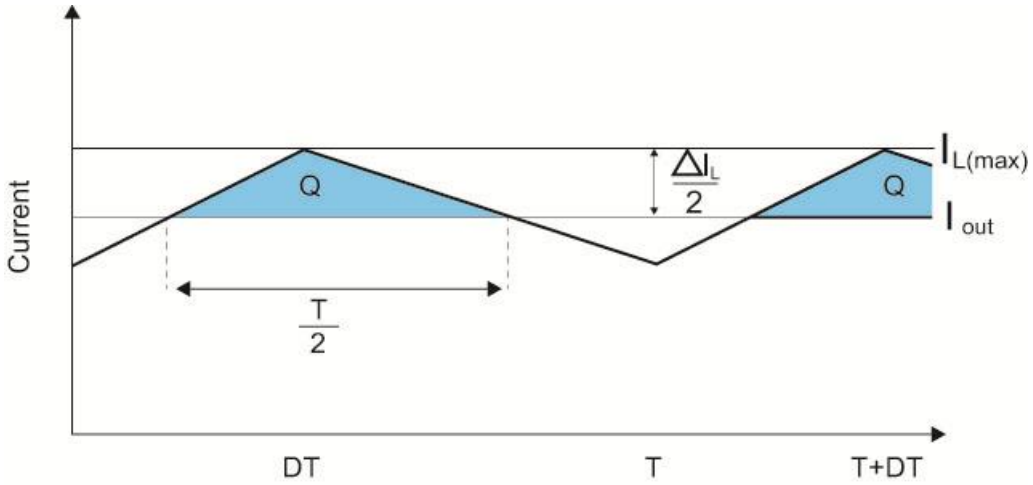

Figure 8. Inductor current in a Buck converter in CCM.

Assuming that the whole ripple current from the inductor flows through the capacitor implies that the charge that is accumulated during the time when the inductor current is above the average inductor current is

$$\Delta Q_C = \frac{1}{2}\frac{\Delta I_L}{2}\frac{T_{sw}}{2} = \frac{\Delta I_L T_{sw}}{8} \tag{2.13}$$

The voltage ripple in a capacitor due to an accumulation of charge is

$$\Delta V = \frac{\Delta Q}{C} \tag{2.14}$$

Combining (2.13) and (2.14) give the output voltage ripple

$$\Delta V_{out} = \frac{\Delta Q_C}{C} = \frac{1}{C}\frac{\Delta I_L T_{sw}}{8} \tag{2.15}$$

where ΔI_L is described in (2.5). The voltage ripple can be written as

$$\Delta V_{out} = \frac{T_{sw}^2}{8C}\frac{V_{out}}{L}(1-D) \tag{2.16}$$

A smaller T_{sw} results in a lower output voltage ripple; a higher switching frequency

reduces the ripple for the same C and L. Larger values of C and L also reduce the voltage ripple.

2.2.1.4 Pros and cons with the Buck converter

The Buck converter is a fairly simple type of step-down converter. It is easy to control, especially in CCM since the relationship between in- and output voltage is directly proportional to the duty-cycle. The Buck converter has a low number of parts, which means that the size of the converter can be made small.

One disadvantage with the Buck converter is the switching losses associated with the switching element. The losses will decrease the efficiency of the converter substantially, especially when the switching frequency increases into the multi-MHz-range. Another disadvantage with the Buck converter is the switching of the freewheeling diode, where the whole current through it should be turned on or off instantly, this makes the choice of a proper diode more difficult.

2.2.2 Resonant-PWM Buck converter

Because of the switching losses associated with traditional Buck converters, a resonant-PWM Buck converter is investigated. The purpose of the resonant-PWM Buck converter is to turn the switches on and off under either ZVS or ZCS. The investigated resonant-PWM converter is proposed in [6].

2.2.2.1 Converter function

The resonant-PWM Buck converter is basically built as the Buck converter, consisting of a switch S_1 and an output filter L_f and C_f, with the addition of a resonance leg with a small inductance L_r, a switch S_2 and a small capacitor C_r. An additional freewheeling diode D_4 and two diodes connected in anti-parallel with the two switches, D_1 and D_2 are also added. An overview of the resonant-PWM Buck converter is seen in Figure 9.

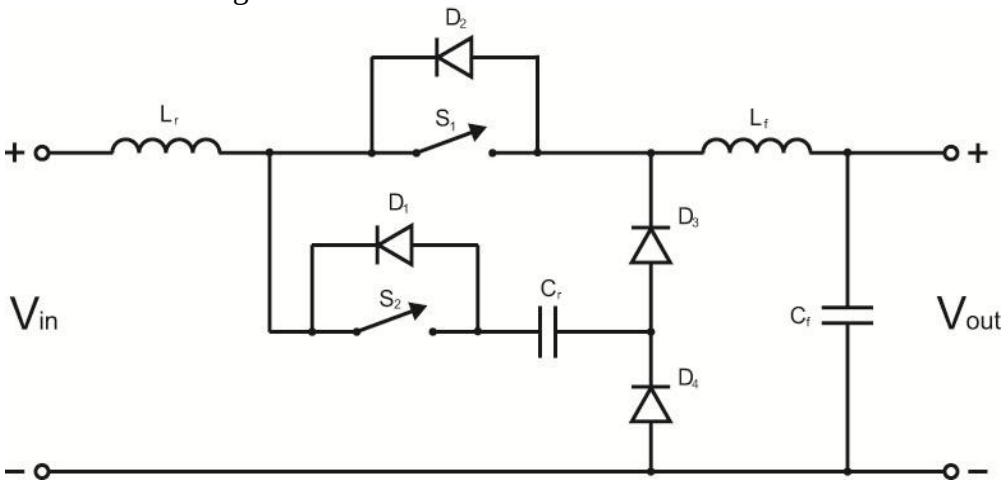

Figure 9. Resonant-PWM Buck converter

Instead of two or three different stages of operation as in a Buck converter, the resonant-PWM Buck has seven different operating stages during each switching period.

The following assumptions are made when describing the resonant-PWM Buck converter:

- The switches and diodes are ideal
- The current through the output inductor is constant.

The current paths for the six first operating stages are seen in Figure 10. Waveforms for current through the resonant inductor and voltage over resonant capacitor are seen in Figure 11.

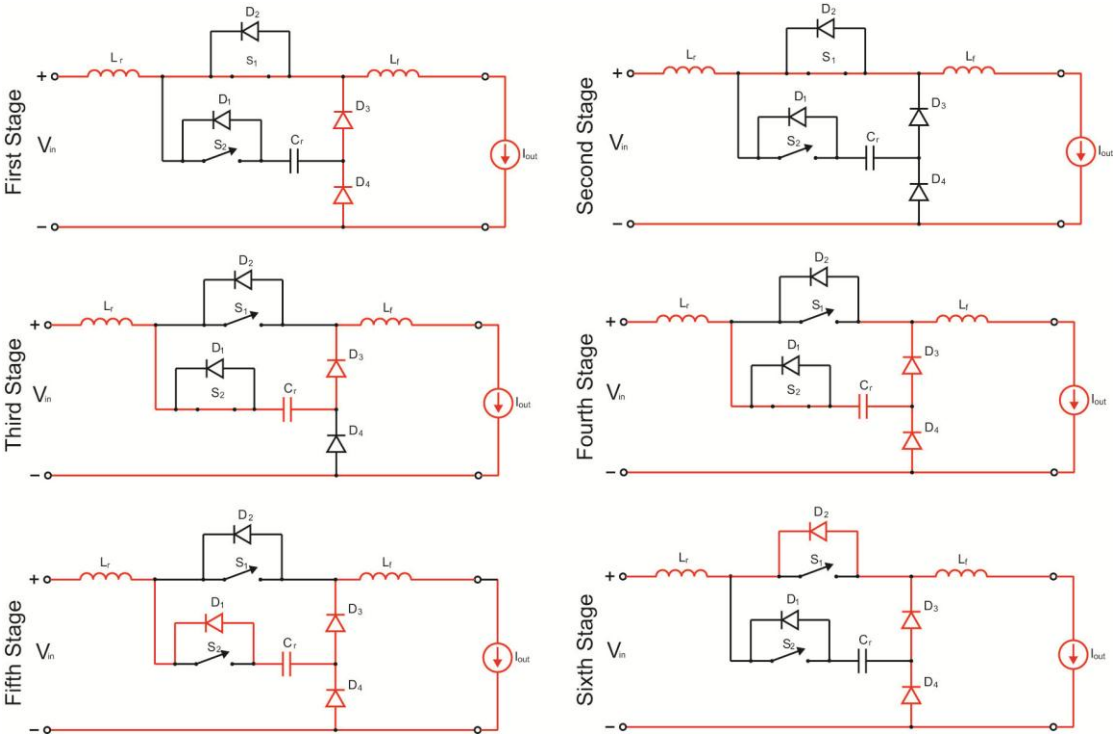

Figure 10. The six first operating stages in the resonant-PWM Buck converter.

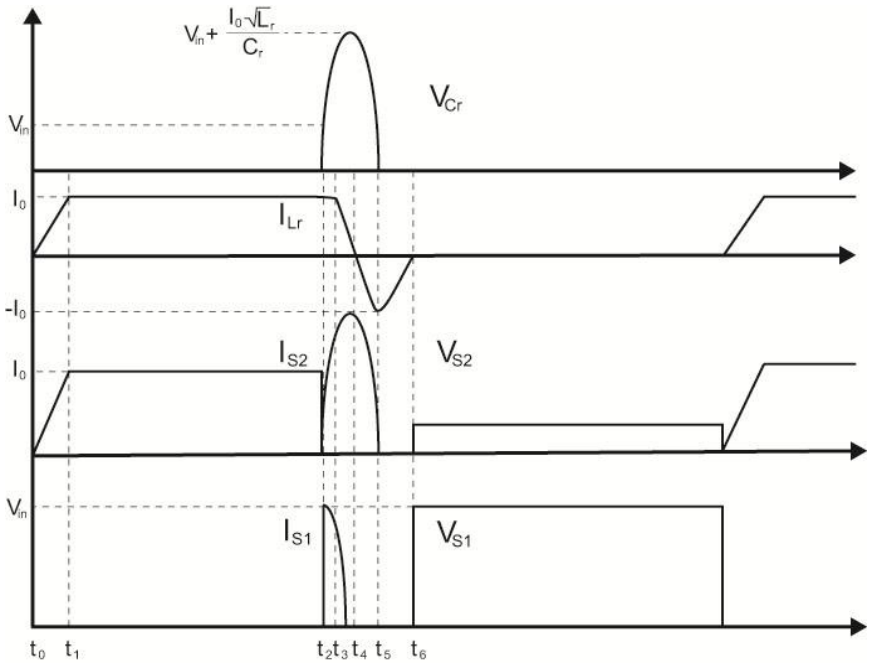

Figure 11. Switching waveforms in the resonant-PWM Buck converter.

To describe the lengths of the stages, voltages and currents two parameters are defined,

$$\alpha = \sqrt{\frac{L_r}{C_r}}\frac{I_0}{V_{in}} \tag{2.17}$$

which is a normalized voltage, and

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{2.18}$$

which is the resonance frequency of the resonance elements L_r and C_r.

Stage 1
Before stage 1, the output current freewheels through diodes D_3 and D_4 and both switches are off. Stage 1 begins when the main switch S_2 is turned on under zero current. The current through the resonant inductor L_r increases linearly until it reaches the output current I_0. During stage 1 the resonant switch S_1 can be turned on under zero current.

The length of stage 1 is

$$\Delta T_1 = \frac{\alpha}{\omega_0} = L_r\frac{I_0}{V_{in}} \tag{2.19}$$

and the current through L_r is

$$I(L_r) = \frac{V_{in}}{L_r}t \tag{2.20}$$

Stage 2
Stage 2 is the stage where the main power transfer from the supply to the load occurs and the output voltage is controlled by changing the length of the second stage. During this stage the output current I_0 flows through the main switch. The voltage over the resonant capacitor C_r is zero under the whole stage. Stage 2 ends when the main switch is turned off under zero voltage. The length of the second stage is

$$\Delta T_2 = \frac{D}{f_{sw}} \tag{2.21}$$

where *D* is the duty-cycle and f_{sw} is the switching frequency. The current through L_r during the second stage is equal to the output current,

$$I(L_r) = I_0 \tag{2.22}$$

Stage 3
After the main switch is turned off the current through L_r is forced to change path from going through the main switch to going through the resonant switch S_1. The voltage over the resonant capacitor increases linearly until the voltage reaches the input voltage V_{in}. The current through the resonant inductor is constant and equal to I_0 during the whole stage.

The length of the third stage is

$$\Delta T_3 = \frac{1}{\alpha\omega_0} = C_r \frac{V_{in}}{I_0} \tag{2.23}$$

and the resonant inductor current and resonant capacitor voltage are

$$I(L_r) = I_0 \tag{2.24}$$

$$V(C_r) = \frac{I_0}{C_r} t \tag{2.25}$$

Stage 4
After the voltage over the resonant capacitor has reached the input voltage, diode D_4 is turned on and the resonance between the resonant inductor and capacitor begins. The fourth stage is finished when the current through the resonant inductor reaches zero. At the same time the voltage over the resonant capacitor is at its maximum.

The length of the fourth stage is

$$\Delta T_4 = \frac{1}{\omega_0} \frac{\pi}{2} \tag{2.26}$$

and the resonant inductor current and resonant capacitor voltage are

$$I(L_r) = I_0 \cos(\omega_0 t) \tag{2.27}$$

$$V(C_r) = V_{in} + \sqrt{\frac{L_r}{C_r}} I_0 \sin(\omega_0 t) = V_{in}(1 + \alpha \sin(\omega_0 t)) \tag{2.28}$$

Stage 5
During stage 5 there is still resonance between the resonance inductor and capacitor, but the current through the inductor is now negative and flows through the diode D_1 which is connected in anti-parallel with the resonant switch S_1. During this stage the main switch can be turned off under zero current. The fifth stage ends when the voltage over the resonant capacitor reaches zero. The current through L_r is then negative.

The length of the fifth stage is

$$\Delta T_5 = \frac{1}{\omega_0}\left(\pi - \cos^{-1}\left(\frac{1}{\alpha}\right)\right) \tag{2.29}$$

and the resonant inductor current and resonant capacitor voltage are

$$I(L_r) = -I_0 \sin(\omega_0 t) \tag{2.30}$$

$$V(C_r) = V_{in} + \sqrt{\frac{L_r}{C_r}} I_0 \cos(\omega_0 t) = V_{in}(1 + \alpha \cos(\omega_0 t)) \tag{2.31}$$

Stage 6
During the sixth stage the current through the resonant inductor increases linearly (from a negative value) through diodes D_2, D_3 and D_4 until it reaches zero.

The length of the sixth step is

$$\Delta T_6 = \frac{\alpha}{\omega_0}\sqrt{1 - \frac{1}{\alpha^2}} \tag{2.32}$$

and the current through the resonant inductor is

$$I(L_r) = -I_0\sqrt{1 - \frac{1}{\alpha^2}} + \frac{V_{in}}{L_r} t \tag{2.33}$$

Stage 7
Stage 7 is the freewheeling stage when both switches are off, and the current freewheels through diodes D_3 and D_4.

The length of the seventh stage is

$$\Delta T_7 = \frac{1}{f_{sw}} - \sum_{i=1}^{6} \Delta T_i \tag{2.34}$$

2.2.2.2 Control of the switches and output voltage
Switch S_2 it turned on at the beginning of stage 1 and is turned off at the end of stage 2. In fact, it is the switching of S_2 that determines when stage 1 begins and when stage 2 ends. The total on-time of S_2 is then

$$T_{on,S2} = \Delta T_1 + \Delta T_2 \tag{2.35}$$

The on-time of S_2 has some flexibility, the important thing is to turn it one during stage 1 and to turn it off during stage 5 to enable ZVS and ZCS. Therefore the exact on-time of the switch cannot be stated but a choice of turning the switch on and off in the middle of the first and fifth stage could be reasonable. The on-time of S_1 is then

$$T_{on,S2} = \frac{\Delta T_1}{2} + \Delta T_2 + \Delta T_3 + \Delta T_4 + \frac{\Delta T_5}{2} \tag{2.36}$$

The relation between input and output voltage is

$$V_{in} = V_{in}(D + \frac{1}{4\pi}\frac{f_{sw}}{f_0}\frac{1}{\alpha}) \tag{2.37}$$

where

$$f_0 = \frac{\omega_0}{2\pi} \tag{2.38}$$

To enable ZVS and ZCS α must be greater than 1. Also, to have a short periods with resonance, $f_0 \gg f_{sw}$. The ratio between in- and output voltage is then simplified to

$$V_{in} = V_{in}D \tag{2.39}$$

And the ratio between in- and output voltage is solely determined by the length of the second stage.

2.2.2.3 Pros and cons with resonant-PWM Buck converter

The main purpose with the resonant-PWM Buck converter is that it is supposed to remove the switching losses associated with the traditional Buck converter. The removal of the switching losses and the potential higher efficiency is the main advantage for the resonant-PWM Buck converter. Another advantage over the Buck converter is that the turn-on and -off of the freewheeling diodes is done under ZCS, which makes the choice of the freewheeling diodes easier than for the Buck converter.

The disadvantages with the resonant-PWM Buck converter are the larger number of parts and the more complicated control required. Also, the length of the stages change with the output current, which means that not only should the duty-cycle be controlled, but also the delay between turning the two switches on and off. A more complicated control is needed compared to the Buck converter to maintain ZVS and ZCS.

The losses in the freewheeling stage are also increased since two diodes are used instead of the single one used in the Buck converter.

2.2.3 ZVS-CV converter

The ZVS-CV is a step down resonant converter where its resonance is deemed pseudo-resonant. The categorization of the ZVS-CV resonance is made since it is not part of the converter´s main power transfer. The ZVS-CV has two switches which are turned on and off under ZVS conditions and therefore removing switching losses. The voltage across the two switches is clamped either to the input voltage or to zero voltage, resulting in lower voltage stress [7].

2.2.3.1 Converter function

The fundamental components of the ZVS-CV converter are shown in Figure 12. The capacitors C_1 and C_2 in parallel with the switches and diodes can either be parasitic capacitances only or a combination of both parasitic and additional capacitances.

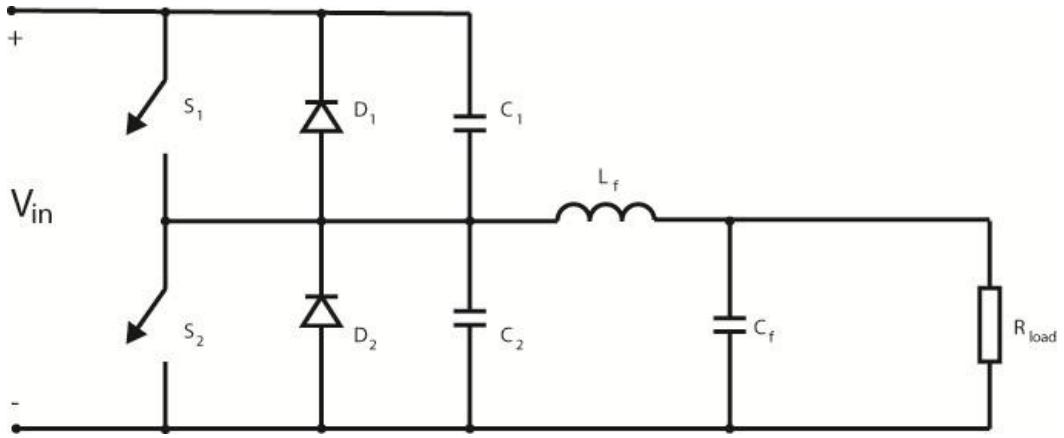

Figure 12. ZVS-CV converter.

The operation of the ZVS-CV converter is best described by dividing the switching period into seven operating stages. The ZVS intervals, high- and low-side capacitor voltages and inductor current of the ZVS-CV converter are shown in Figure 13.

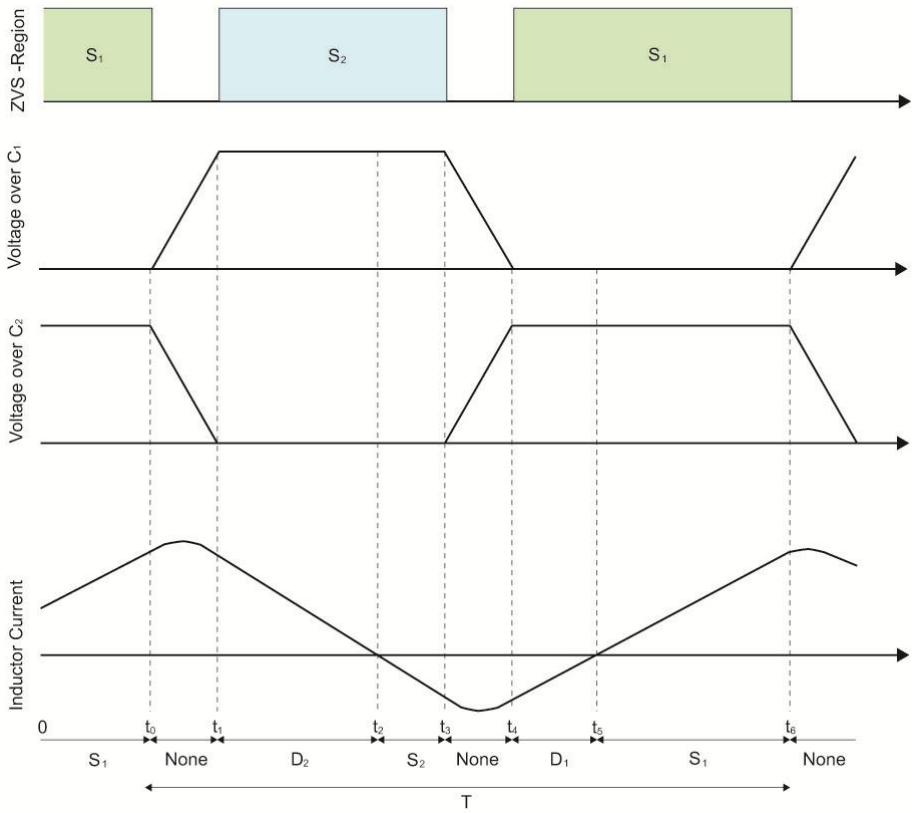

Figure 13. Regions where ZVS is possible for the two switches, capacitor voltages and inductor current for the ZVS-CV converter.

Stage 1

This description is valid between 0 and t_0 in Figure 13. In this stage the current flows through the switch S_1. No current flows through S_2 since the switch is off. The current in the inductor is positive and increasing due to the positive voltage $V_{in} - V_{out}$ over the inductor. At t_0 the switch S_1 is turned off under zero voltage since the capacitor C_1 parallel to the switch is voltage stiff and the voltage builds up slowly compared to the switching of S_1.

Stage 2

This description is valid between t_0 and t_1 in Figure 13. During this stage of the switching period the switch S_1 has just turned off and the switch S_2 is still off. During this stage, the circuit in Figure 12 can be redrawn into the circuit in Figure 14.

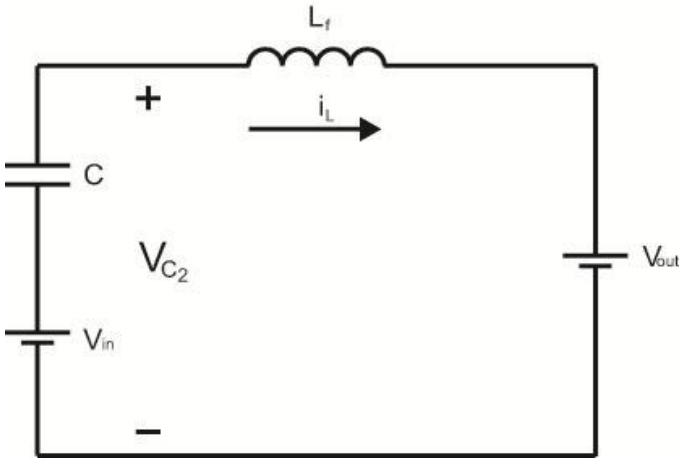

Figure 14. Equivalent circuit for the ZVS-CV converter during stage 2.

The capacitance C in Figure 14 is described by

$$C = C_1 + C_2 \tag{2.40}$$

where C_1 and C_2 are the capacitances seen in Figure 12.

During the time interval t_0 to t_1 a resonance transition will take place between C and the filter inductor L_f, the resonance frequency of this LC-network is described by

$$f_0 = \frac{1}{2\pi\sqrt{L_f C}} \tag{2.41}$$

The resonance frequency is an important design parameter when designing the ZVS-CV converter. If the converter is designed to have a resonance frequency much higher than the switching frequency the converter output voltage will be able to be regulated by PWM.

The impedance seen by the current in the inductor during the interval t_0 to t_1 is

$$Z_0 = \sqrt{\frac{L_f}{C}} \tag{2.42}$$

This impedance will be high since the inductance L_f will be much larger than C.

A result of this high impedance is a current with very low $\frac{di}{dt}$ during t_0 and t_1. The low $\frac{di}{dt}$ will result in a nearly constant $\frac{dv}{dt}$ across the capacitor C, resulting in a voltage across the capacitor with a linear rise. When the voltage over C_2 in Figure 12 reaches zero this stage is over and S_2 can be turned on under ZVS conditions.

Stage 3

This description is valid between t_1 and t_2 in Figure 13. When Stage 2 ends at t_1, the voltage across C_2 has reached zero resulting in D_2 being forward-biased, resulting in

the possibility to turn on S_2 under zero voltage. Switch S_2 is turned on as soon as the diode D_2 starts carrying current. The voltage over the inductor during t_1 to t_2 is $-V_{out}$ resulting in a linearly decreasing current. This stage ends at t_2 when the inductor current changes polarity and can no longer be conducted by the diode D_2.

Stage 4
This description is valid between t_2 and t_3 in Figure 13. This stage started when the current turns negative and can no longer be conducted through the diode D_2. The entire inductor current is conducted through the switch S_2. At t_3 the switch S_2 is turned off under ZVS conditions since the parallel capacitance C_2 is voltage stiff resulting in a change of voltage much slower than the time required to turn S_2 off.

Stage 5
This description is valid between t_3 and t_4 in Figure 13. In this stage S_1 is off and S_2 has just switch off. A similar resonance transition to the one described in stage 2 takes place during this time interval. Between t_3 and t_4 the inductor current is negative and nearly constant due to the high impedance described in (2.42). Thus, the $\frac{dv}{dt}$ for the capacitance C will be determined by the peak negative current instead of the positive peak current in stage 2.

Stage 6
This description is valid between t_4 and t_5 in Figure 13. The negative current will start to flow through the diode D_1 at which it is possible to turn on S_1 under zero voltage. The voltage across the inductor in this interval will be positive and equal to $V_{in} - V_{out}$. Since the inductor voltage is positive the current will start to increase, at t_5 the current will reach zero and the diode D_1 will become reversed biased and the entire inductor current will be conducted by S_1.

Stage 7
This description is valid between t_5 and t_6 in Figure 13. The inductor current is increasing due to the positive voltage $V_{in} - V_{out}$ and is conducted through S_1. At t_6 the switch S_1 is turned off under zero voltage due to the voltage stiffness of the parallel capacitor C_1. The turn off of S_1 marks the end of one switching period [7].

2.2.3.2 Pros and cons with ZVS-CV converter
The ZVS-CV converter is basically a Buck converter with a few more components, an extra diode and an extra switch is all that is required in the power stage.

The ZVS-CV converter eliminates the switching losses associated with the Buck converter. Hence, the ZVS-CV converter has potential of higher efficiency than the Buck converter. The ZVS-CV converter requires control of two switches, resulting in a more complex control circuits than in the Buck converter.

The need for a negative current to decrease the voltage over the switches before switching implies that a much larger current ripple is needed. The current ripple results in higher conductive losses in all resistive elements such as switches, diodes, inductor and capacitors.

An advantage with the ZVS-CV converter is that the relation between in- and output voltage is only dependent on the duty-cycle, even at very light loads, since the inductor current is continuous for all loads.

The output voltage ripple will increase, with the same output capacitor filter, compared to the Buck converter since the ripple current is much larger. But, since there is no instant turn-off or turn-on of any components, high-frequency transient peak-voltages due to parasitic elements will be lower than for the Buck converter.

2.3 Components in the power stage

The following section is a short theoretical overview of some of the components used in the output power stage of DC/DC converters. Important parameters are explained and the impact of the switching frequency is explained. The components covered are the switching transistor, the output inductor and the in- and output capacitance.

2.3.1 Switching transistors

The development of having more integrated power devices with smaller and smaller size makes the choice of switching transistor very important since a large part of the losses in any SMPS occur in the switching transistor.

Transistors made out of Si have been the dominating technology for decades. Newer technologies aim for improvements when it comes to high-power, high-frequency transistors. One of the more promising materials for future transistors is GaN. The critical electric field of GaN is 10 times higher, the electron mobility is 3 times higher and the charge density is 2 times higher than for Si. These properties give the opportunity to manufacture much smaller GaN-transistors then Si-transistors. The more compact design allows much higher switching frequencies, up to hundreds of MHz [3].

The product of gate charge and on-resistance for a transistor is an important measure since losses in the transistor are highly dependent on these two factors. GaN-transistors have a much lower $Q_g R_{on}$-product than Si-transistors for the same breakdown voltage, which makes them suitable for use in high frequency SMPS [8].

2.3.2 Inductors and capacitors

A benefit of increasing the switching frequency is the opportunity to reduce the size of the output inductor. With the same output current and the same ratio between average output current and ripple current, an increased switching frequency can reduce the size of the inductor, which is inversely proportional to the switching frequency. Magnetic components such as inductors are also heavy and an increased switching frequency will decrease the weight of the converter. Also, the magnetic material used in the core must have adequate magnetic permeability at these high frequencies [9].

Capacitors are needed in converters to maintain the output voltage at a constant level. They are also needed to decrease the input voltage ripple and to decouple ICs from other components. One big advantage when increasing the switching frequency is the possibility to reduce the in- and output capacitance while maintaining a low output voltage ripple. A lower value of capacitance means that smaller components can be used and that the size of the converter can be reduced [10].

3 Case set up

This chapter begins with a short section with results from simulations of the three converters investigated in Section 2.2. The second section compares and motivates the choice of the converters that are to be implemented in hardware. The chapter ends with a section explaining the complete converters.

3.1 Modelling and simulations

To be able to choose the most suitable DC/DC converter topology both theoretical studies and simulations of the different topologies were performed. Theoretical studies are crucial to get an understanding of how important parameters affect the performance of each topology, and how to derive such things as switching times for transistors. Simulations are used to confirm theory, to further investigate and evaluate the different topologies and to investigate how performance of the converter changes when non-ideal components, such as resistance and capacitance in transistors and diodes, and parasitic elements, such as stray inductance and capacitance, are introduced into the converter.

To model the transistors in the converter a transistor model with similar properties as the switching transistor chosen in Section 3.3.2.1 is used in the simulations. Modelling of diodes has been done by using built-in models of fast schottky diodes which are to be used in the implementation of the converter.

3.1.1 Results from simulations

The main goal with simulations was to get a better understanding of the converters and how different parameters change the performance of the converters. Simulated waveforms for the Buck and the ZVS-CV converter were very similar to the ones derived in theory in Sections 2.2.1 and 2.2.3, even when using non-ideal models of components and introducing parasitic elements.

For the resonant-PWM converter, the simulated voltages and currents had the same forms as derived from theory in Section 2.2.2 when ideal components were used. However, when non-ideal components were introduces into the simulations the simulated voltages and currents changes dramatically compared to theory, which is shown in Figure 15. The top part of Figure 15 shows the voltage and current over the resonant capacitor and through the resonant inductor respectively. The middle part shows voltage and current for the resonant switch and the bottom part shows the voltage and current for the main switch.

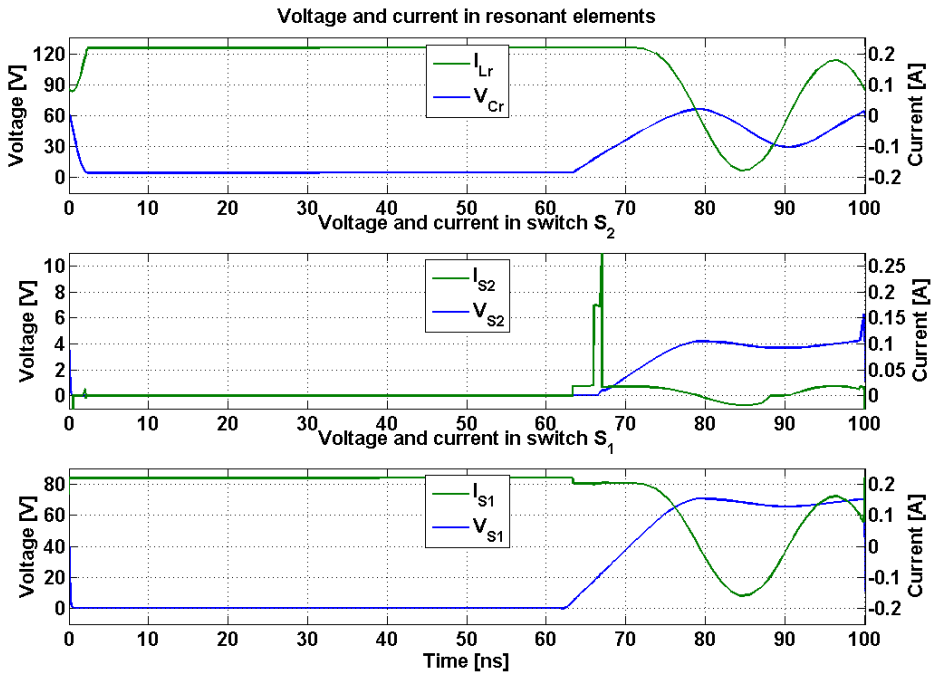

Figure 15. Simulated waveforms using non-ideal components in the resonant-PWM Buck converter.

All of the stages 1-6 described in Section 2.2.2.1 are affected by the additional capacitance from the transistors, this leads to changed lengths of the stages and that the ZVS and ZCS does not work as designed. The extra capacitance introduced from transistors could be taken into account when calculating the length of the stages and the switching scheme for the transistors. The worst part with introducing non-ideal components is however the oscillations of voltage and current during the off-stage. When the resonance inductor current has increased from its negative peak value to zero, both the voltage over the resonance capacitor and the current through the inductor is supposed to stay at zero until the switches is turned on again.

As seen in Figure 15, this is not the case, oscillating voltages and currents are seen for $t > 80\,ns$. The magnitude and frequency of the voltage oscillations are dependent on several factors, where the output capacitance of the transistors is the most important factor. These oscillations will impact the performance of the converter and make it much harder to turn the switches on and off at the right moment to maintain ZVS and ZCS.

The oscillations seem to be hard to get rid of, damping with the use of ferrite beads and tuning of the parameters of the converter has been carried out in simulations, but the oscillations are still present in some form and decreases the performance of the resonant-PWM converter.

3.2 Choice of topology

To further investigate which topology most suitable for 10 MHz, two of the converter are to be implemented in hardware. The primary reason for only implementing two converters in hardware is the limited amount of time available for this thesis.

One of the two converters that are to be implemented is the traditional Buck converter. The Buck converter is supposed to work as a reference for the other implemented converters. Performance measures such as power capability, line and load regulation, output voltage ripple and efficiency of the Buck converter is to be compared with the other converter chosen for implementation in hardware.

The choice of which of the other two converters, the resonant-PWM Buck or the ZVS-CV converter, that is to be implemented is based on a ranking of a series of important criteria, shown in Table 1. The criteria are not weighted against each other in terms of which of the criterion that is more important than another. The converters are ranked 1-3, where 1 is the best and 3 is the worst ranking.

The criterion *physical size*, reflects the potential of building a small converter, it includes both the power stage and the auxiliary circuits. The Buck converter has the lowest number of parts in the power stage together with the simplest control which means that the potential for a small converter is best among the compared topologies. The physical size increases with increased *complexity* since an increased complexity requires more components. The resonant-PWM Buck has the highest complexity since the length of almost all the stages changes with load as explained in Section 2.2.2. The need for a more complex control also increases the number of parts and the physical size of the converter. The ZVS-CV is more complex than the Buck converter but not as complex as the resonant-PWM Buck since the dead time of the switches can be set to a fixed value without changing the behavior of the converter too much.

The criterion *potential efficiency* does only include the output power stage since the majority of the power losses occur in the power stage. The Buck converter is hard-switched and has the least potential for a high efficiency. The main reason for building the resonant-PWM and the ZVS-CV converter is the potential for a high efficiency. The ZVS-CV has a lower number of parts in the output power stage compared to the resonant-PWM converter and has therefore also the highest potential for a high efficiency.

Robustness reflects how good the converter behaves when introducing non-ideal components in the converter. These non-idealities can be stray inductance and capacitance, errors in values for different parts and the dependence of stable and non-changing parameters of components in the converters. The resonant-PWM converter has large difficulties with oscillating voltages and currents in the free-wheeling stage as seen in Section 3.1.1. These oscillations results in that the ZVS and ZCS of the transistors might be lost. The ZVS-CV converter is somewhat dependent on the capacitance between drain and source for both the transistors and diodes. Both of these capacitance values changes with voltage and temperature [11] and therefore the robustness is lower than for the Buck converter which is more independent on such changing parameters since it is hard-switched.

The *output voltage ripple* criterion ranks how low the output voltage ripple might be with the same output capacitor bank. The ZVS-CV converter has a much larger current ripple than the other converters and therefore also has the largest output voltage ripple. The resonant-PWM converter has, as said above and explained in Section 3.1.1, some troubles with oscillating voltages and currents. These oscillations

propagate to the output stage and the voltage ripple is therefore a bit larger than for the traditional Buck converter. The output voltage ripple is much larger in the ZVS-CV converter than in both the resonant-PWM converter and the traditional Buck converter.

Line and load regulation ranks how the performance of the converts changes with changed input voltage and/or changed output power. The traditional Buck converter has two different modes, CCM and DCM as explained in Section 2.2.1. The transfer function is different for the two modes and the ability to control the Buck converter is decreased if the mode is changed without any change in the regulator. The same is true for the resonant-PWM converter with the addition of the changing stage times for different input voltage and output power. The ZVS-CV converter has the highest potential since it does not have any special conduction modes as the Buck or the resonant-PWM Buck converter. The magnitude of the inductor current ripple does only vary with input voltage, as in the two other converters, but since the converter is designed to have a negative inductor current for a period in each switching cycle, the limit between CCM and DCM does not exist. Therefore, the ZVS-CV ranks first in this criterion.

Table 1. Ranking of the three investigated converter ranked from first to last in each category. Lower number is better.

	Traditional Buck converter	Resonant-PWM-Buck converter	ZVS-CV converter
Physical size	1	3	2
Complexity	1	3	2
Potential efficiency (power stage only)	3	2	1
Robustness (errors in parameters)	1	3	2
Output voltage ripple	1	2	3
Line and load regulation	2	3	1
Total	9	16	11

With the argument above and support of Table 1, the two converters that are chosen for implementation are:

- Traditional Buck converter
- ZVS-CV converter

3.3 Building of the converters

When building the converters, practical design of the converters come into consideration. Some things to consider are size and packages of the components, decoupling capacitors, critical paths for switching currents, device density etc. This

section explains some of the choices that are made when it comes to components and layout. The converters will be built on a two-layer PCB with one component layer and one ground layer, since this in beneficial in high frequency applications.

3.3.1 Overview of the complete circuits

To implement the two converters in practice, there are many things to consider. A basic block diagram of the Buck converter being built is shown in Figure 16. The Buck converter consists of five building blocks with different functions. The power stage of the Buck converter was described in Section 2.2.1. In addition to the power stage there is one driver stage that turns the switching transistor on and off. The driver stage receives PWM control pulses from a comparator that compares the output from the regulator with a saw tooth wave from the saw tooth generator circuit. The regulator compares the output voltage from the power stage with a reference voltage to regulate the voltage that is transmitted to the comparator.

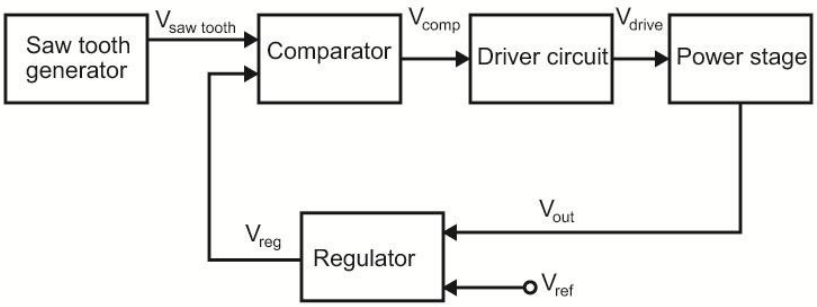

Figure 16. Block diagram of the different parts of the Buck converter.

The block diagram for the ZVS-CV converter, shown in Figure 17, has several building blocks in common with the Buck converter: the power stage, the saw tooth generator and the regulator. But, there are some differences when it comes to the driver circuit and the comparator. The comparator is replaced with a control circuit for controlling dead times in the converter and the driver circuit is more complex in the ZVS-CV converter than in the Buck converter.

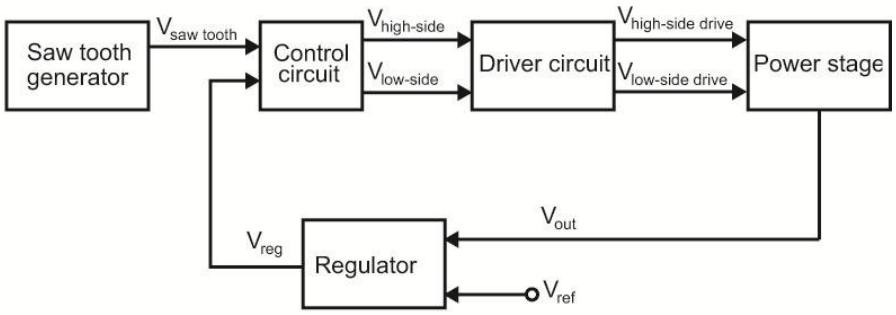

Figure 17. Block diagram of the different parts in the ZVS-CV converter.'

Complete schemes of both the Buck and the ZVS-CV converter are found in Appendix A. The following subsections explain each building block of the two converters.

3.3.1.1 Output power stage Buck

The output power stage is the main part of the Buck converter and the choice of components and values are important for good converter functionality. The converter is chosen to work in CCM since the output voltage is then directly proportional to the duty-cycle which leads to easier control. The harmonic content of the output voltage ripple will also become lower than for DCM [9].

The value of the output inductance L is calculated using (2.3) rearranged to

$$L = (V_{in} - V_{out})\frac{t_{on}}{\Delta i_L} = (V_{in} - V_{out})\frac{T_{sw}D}{\Delta i_L} \tag{3.1}$$

which in the case of an ideal converter where $D = \frac{V_{out}}{V_{in}}$ is equal to

$$L = (V_{in} - V_{out})\frac{T_{sw} * D}{\Delta i_L} = (V_{in} - V_{out})\frac{T_{sw}}{\Delta i_L}\frac{V_{out}}{V_{in}} \tag{3.2}$$

A current ripple of about 30 % is a normal choice which enables a good compromise between stresses in the converter and size of the inductor [9]. With an output power of 6 W, the output current is 200 mA and the corresponding ripple current 60 mA. The required inductance is then calculated as

$$L = (50 - 30)\frac{100 \cdot 10^{-9}}{0.06}\frac{30}{50} = 20\ \mu H \tag{3.3}$$

The value of the output capacitance is found by using (2.16)

$$C = \frac{T_{sw}^2}{8\Delta V_{out}} \frac{V_{out}}{L}(1 - D) = \frac{T_{sw}^2}{8\Delta V_{out}} \frac{V_{out}}{L}\left(1 - \frac{V_{out}}{V_{in}}\right) \tag{3.4}$$

A goal of having an output voltage ripple of less than 1 mV peak-to-peak was set up in Section 1.2. This leads to a value of C equal to

$$C = \frac{(100 \cdot 10^{-9})^2}{8 \cdot 1 \cdot 10^{-3}} \frac{30}{20 \cdot 10^{-6}}\left(1 - \frac{30}{50}\right) = 0.75\ \mu F \tag{3.5}$$

However, (3.5) only includes voltage ripple due to accumulated charge. The voltage ripple due to the ESR in capacitors is not included. By adding more capacitance the ESR decreases and the capacitance increases. The output voltage ripple due to both capacitance and ESR then decreases. The drawback of having more capacitors is that the size of the converter increases. But, to have a large margin, a large output capacitance of about 50 µF is chosen to be implemented in the Buck converter. The output voltage ripple is then almost completely determined by the ESR and current ripple as [12]

$$\Delta V_{out} = \Delta i_L R_{ESR} \tag{3.6}$$

The needed R_{ESR} is then, with a $\Delta i_L = 60\ mA$ and $\Delta V_{out} = 1\ mV$, calculated to

$$R_{ESR} = \frac{\Delta V_{out}}{\Delta i_L} = \frac{1 \cdot 10^{-3}}{60 \cdot 10^{-3}} = 16.7\ m\Omega \tag{3.7}$$

The choice of the actual capacitors is further explained in Section 3.3.2.2.

3.3.1.2 Output power stage ZVS-CV

The design of the output stage for the ZVS-CV converter consist of three part: choosing the needed dead time described in Section 2.2.3 to allow ZVS within the load range, calculating the value of the output inductor to provide sufficient current ripple to charge and discharge the capacitors in Figure 12, and calculating the required capacitance on the converter output to suppress the voltage ripple below the goal of 1 mV as stated in Section 1.2.

The values of the capacitors in parallel with the switches in Figure 12 consist solely of the parasitic output capacitance of the switching transistors and the diodes. The transistors used have an output capacitance of 14 pF, see Section 3.3.2.1, the diodes are *BAT46WJ* from *NXP*, with a capacitance of approximately 7 pF in the voltage range 0-50 V [13]. The relation between input and output voltage has from simulations been determined to be close to a linear function of the duty-cycle of the high-side transistor, if the dead times is short compared to the switching period. An input voltage of 50 V and an output voltage of 30 V result in a duty-cycle of 60 %, thus leaving 40 % of the switching period to the free-wheeling stage and dead time used to achieve zero voltage switching.

The required current to change the voltage over a capacitor during a time Δt is

$$i_C = C\frac{\Delta V_C}{\Delta t} \tag{3.8}$$

By choosing Δt to 10 ns and recognizing the voltage ΔV_C to be equal to the input voltage of 50 V a current i_C of 210 mA can be calculated. The choice of 10 ns is a compromise between short dead time and a large ripple current.

The charge and discharge of the capacitors are carried out during the dead time. The longest charging/discharging cycle will appear when the inductor current is negative and the load of the converter consumes rated power. The rated power of the converter is 6W, and the corresponding load current 200 mA. The current ripple needed for having a dead time of less than 10 ns is then twice the difference between the needed current of -210 mA and the average output current of 200 mA, i.e. 820 mA
The inductance needed in the output stage is then calculated as

$$L_f = V_L\frac{\Delta t}{\Delta i_{L,p-p}} = 20\frac{60\cdot 10^{-9}}{0.82} = 1.46\,\mu H \tag{3.9}$$

The voltage over the output inductor during the on-stage of the high-side transistor is 20 V, and the approximate on-time of the transistor is 60 ns. In order to have some margin, an inductance of 1.3 µH is considered to be suitable as an output inductor, since this will lead to a faster charge and discharge of the capacitors, with the price of higher conduction losses due to the higher ripple current.

The output capacitance of the ZVS-CV converter was chosen to be the same as the one used in the Buck converter from Section 2.2.1.3. This choice was done in order to be able to compare the negative effects of the larger current ripple in the ZVS-CV converter.

3.3.1.3 Driver and Comparator circuits Buck

The driver and comparator stages in the implemented Buck converter are not that complicated, in fact there are many readymade ICs on the market today that can be used. In order to make it as simple as possible a high frequency high voltage gate driver for NMOSFET-transistors readymade driver circuit named *LTC4444-5* from *Linear Technology* is used [14]. The driver is able to drive two different transistors for a synchronous Buck converter design. The Buck converter being implemented does only use the high-level output port of the driver since it uses a rectifying diode in the freewheeling stage instead of a transistor.

The comparator used for comparing the regulator output voltage with the saw tooth wave is an UltraFast™ comparator optimized for low power and voltages. The name of the comparator is *LT1719* and it is also manufactured by *Linear Technology* [15].

3.3.1.4 Control circuit ZVS-CV

Two switches are used in the ZVS-CV converter as described in Section 2.2.3. These switches are required to follow a predetermined switching pattern to enable the converter to turn both switches on and off under zero voltage. The required switching pattern for the ZVS-CV converter is seen in Table 2.

Table 2. Switching pattern for the ZVS-CV converter.

Converter stage	High-side switch	Low-side switch
On stage	1	0
Dead time	0	0
Freewheeling stage	0	1
Dead time	0	0

The states where both the low and high-side switch are off is denoted dead time in Table 2. The dead time provide protection against cross-conduction and enables the charging and discharging of the capacitors under ZVS as described in Section 2.2.3.

Figure 18 shows an overview of the circuit used to implement the switching pattern from Table 2. The circuit overview in Figure 18 shows that the regulator output is divided into two signal paths, one for the high-side switch and one for the low-side switch.

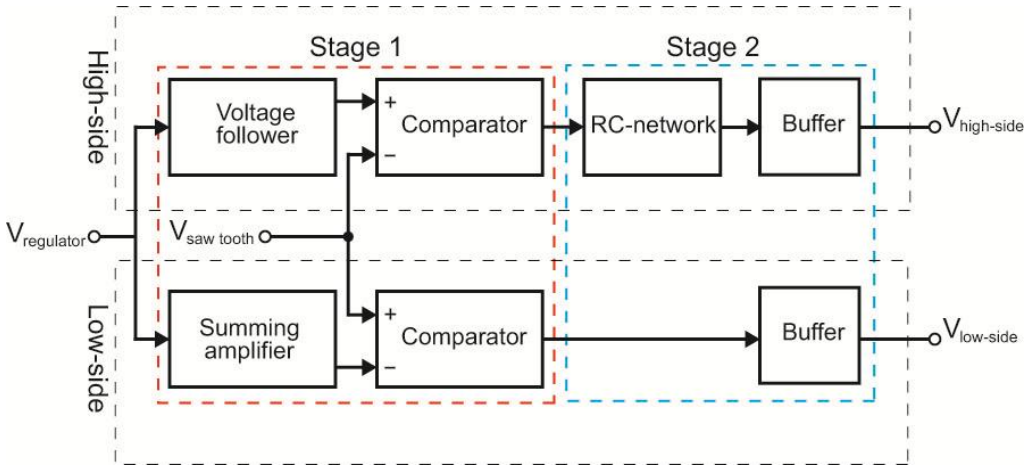

Figure 18. Overview of the control system for the ZVS-CV converter.

Figure 18 is divided into two stages by the dotted lines; these two stages provide different functions in the control circuit and will be explained separately.

Stage 1

In stage 1 an offset is added to the input of the comparator in the low-side signal path. This offset will reduce the duty-cycle of the low-side comparator output and thus provide dead time between the turn off of the high-side switch and the turn on of the low-side switch. The high-side comparator input is feed through a voltage follower and remains at the regulator output voltage.

The offset on the low-side comparator input is provided by a summing amplifier. Figure 19 shows the non-inverting summing amplifier circuit used to provide the offset on the low-side comparator input.

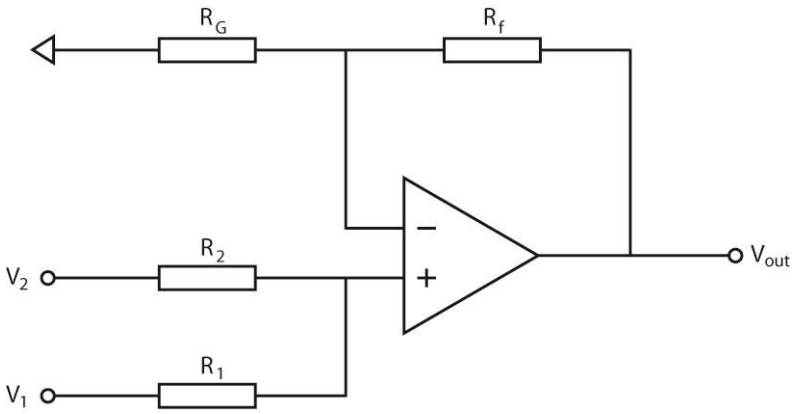

Figure 19 Non-inverting summing amplifier.

The transfer function of the summing amplifier is

$$V_{out} = 1 + \frac{R_f}{R_G}\frac{(V_1R_2 + V_2R_1)}{R_1 + R_2} \tag{3.10}$$

In this setup V_2 is connected to the regulator output and V_1 to the operational amplifier's supply voltage. By selecting the resistance values as

$$R_1 = R_G \tag{3.11}$$

and

$$R_2 = R_f \tag{3.12}$$

a fixed voltage independent of the regulator output voltage can be added to the summing amplifier output. The summing amplifier output is then described by

$$V_{out} = \frac{R_2}{R_1}V_1 + V_2 \tag{3.13}$$

The saw tooth wave designed in Section 3.3.1.6 has an amplitude around 3 V and in Section 3.3.1.2 a dead time of 10 ns for each dead time has been chosen. The total dead time of 20 ns corresponds to 20 % of the switching period. The summing amplifier is therefore needed to provide a voltage offset of 0.6 V to its output compared to its input from the regulator. The voltage V_1 is equal to the supply voltage of 5 V. By applying (3.13) the resistance values R_1 and R_2 can be determined. In this setup R_1 was chosen to 5.6 kΩ and R_2 was thereafter calculated to about 820 Ω. Figure 20 shows the simulated output waveforms of the comparator when a voltage offset of 0.6 V is added to the regulator output and compared to the saw tooth wave.

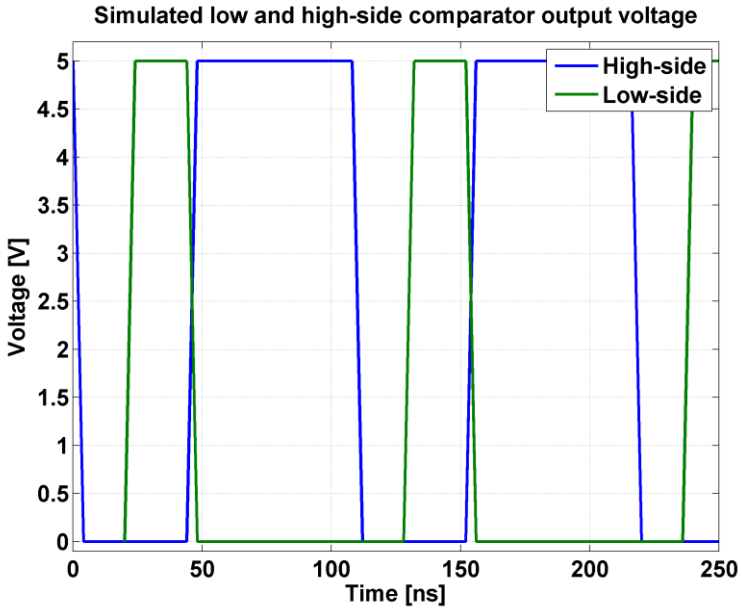

Figure 20 Output voltage waveforms from the two comparators.

Step 2

In step 2 a delay is introduced in the high-side signal path. The delay is introduced to divide the delay shown in Figure 20 symmetrically around both the high-side and low-side signals. This is done by a RC-network connected to a buffer. Figure 21 shows the RC-network connected to the buffer.

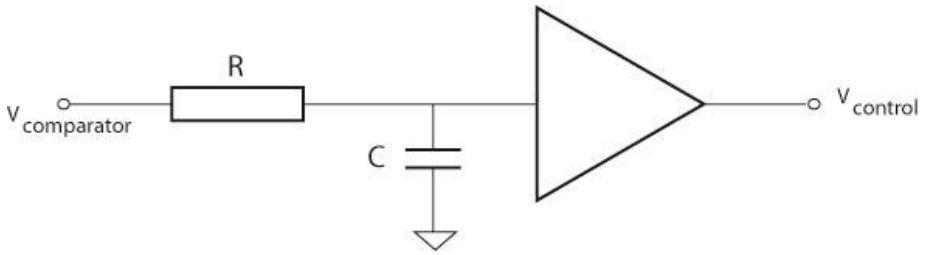

Figure 21 RC-network and buffer used to introduce a delay in the high-side signal path

The voltage across a capacitor in a RC-network is expressed by

$$V_c(t) = V_s(1 - e^{-\frac{t}{\tau}}) \tag{3.14}$$

where $\tau = RC$, which is the time constant of the RC-network.

The voltage V_s is equal to the comparator output voltage of 5 V and V_c is the input voltage to the buffer circuit. In this setup the buffer circuit *NC7SZ126* from *Fairchild Semiconductors* is used [16]. It has a high level threshold voltage of 3.75 V and a low level threshold voltage of 1.25 V at a supply voltage of 5 V. The delay introduced should equal 10 ns, which is described in Section 3.3.1.2.

By the use of (3.14), V_s and setting V_c equal to the threshold voltage of the buffer circuit, the required time constant τ can be calculated. A resistance of 100 Ω and capacitance of 100 pF was chosen to obtain the required delay in the high-side signal path. Figure 22 shows the simulation results from the setup with the calculated RC-network and buffer. It shows that the two dead time bands of 10 ns each have successfully been introduced to the control signals.

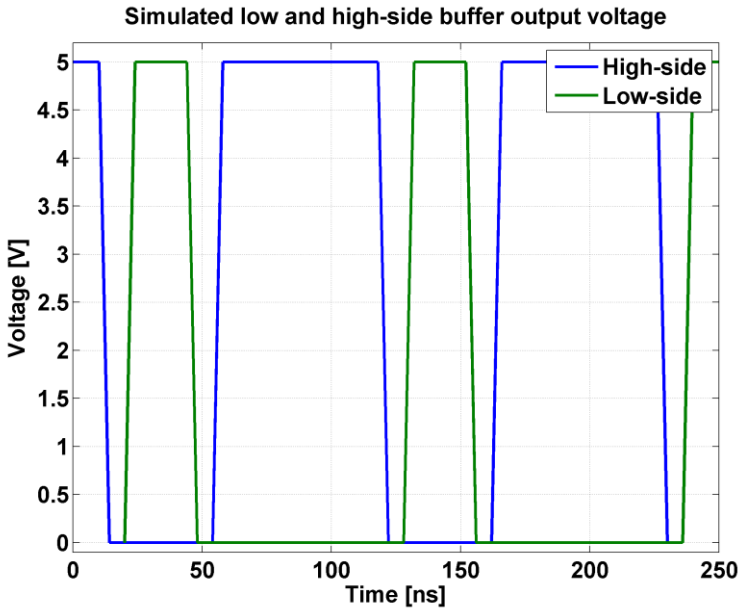

Figure 22 Control signals for the high-sider and low-side drive circuits.

3.3.1.5 Driver circuit ZVS-CV

A driver circuit is required when the control circuit's current capability is insufficient to source or sink the required charge enabling the transistor to turn on or off. The driver circuit acts like a power amplifier taking a low power control signal as input and providing a sufficient current output driving the switching device.

The ZVS-CV converter has two transistors in its output stage. The LDMOS transistor chosen for implementation in Section 3.3.2.1 is an enhancement mode transistor that requires a positive voltage of 10 V between the gate and the source terminals to be fully switched on.

The *EL7104* single channel low-side driver from *Intersil* was chosen as the driver circuits for both transistors in the ZVS-CV converter, since the *LTC4444-5* used in the Buck converter was unable to provide pulses shorter than about 30 ns, which are needed for the low-side transistor in the ZVS-CV converter. This driver is able to provide switching pulses with a duration of 10 ns, with the required voltage amplitude while having very fast rise and fall times. The *EL7104* is rated for a switching frequency of up to 10 MHz [17].

The two transistors in the ZVS-CV converter have their source terminals connected to different nodes in the converter, as seen in Figure 12. The low-side transistor has its source terminal connected to system ground, while the high-side transistor has its source terminal connected to the midpoint of the converter. The source node of the

high-side transistor will swing between the system input voltage of 50 V and ground during every switching period. Since the two transistors are connected to different nodes in the converter two different driving schemes are designed.

Figure 23 shows the driver scheme for the low-side driver configuration of the ZVS-CV converter. Since the low-side transistor has its source terminal connected to system ground the *EL7104* output can be connected directly to the gate of the transistor. The driver input, $V_{control}$, is the low-side control signal from the low-side buffer. The resistances R_1, R_2 and R_g are chosen to 4.7 Ω each to damp oscillations between the input capacitance of the transistor and the parasitic inductance between the driver output and the transistor gate.

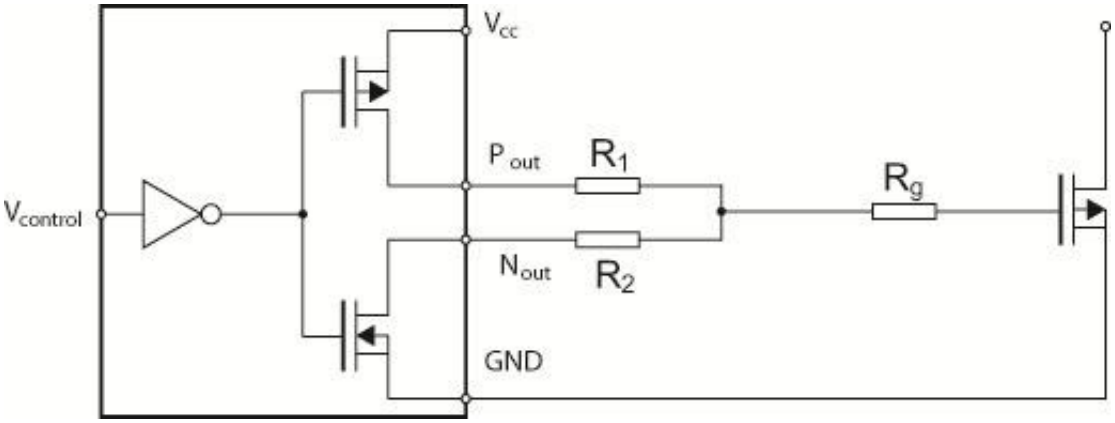

Figure 23. Simple overview of the configuration used to drive the ground-referenced transistor in the ZVS-CV converter.

Figure 24 shows the driving scheme for the high-side driver configuration. This circuit has been modified compared to the configuration for the low-side transistor shown in Figure 23. The high-side driver configuration consists of an AC-coupled transformer with a level-shifting circuit connected to its secondary side. This circuit allows the output from the high-side driver to be referenced to the midpoint of the converter instead of being referred to system ground. Transformer T_1 is a *PFD2015-122ME* from *Coilcraft* with an inductance of 1.2 µH and a coupling factor of 0.97 [18]. The capacitors C_1 and C_2 prevent the core of the transformer to become saturated, by assuring that the voltage-time product across the magnetizing inductance in the transformer equals zero over each switching period. The two capacitors have a capacitance of 82 nF each. Since the capacitor on the secondary side of the transformer is connected in series within the signal path, the gate-source voltage would normally be dependent on the duty-cycle as

$$V_{gs} = V_{driver,out} - DV_{driver,out} \tag{3.15}$$

To prevent V_{gs} to be dependent on the duty-cycle, the diode D_1 is connected between the capacitor and the transformer.

The PNP-transistor B_1 on the secondary side of the transformer is added to improve the turn-off performance of the driver circuit. The transistor B_1 is a *BFT93* from *NXP* [19]. The resistor R_g connected to the gate of the high-side transistor is used to damp the oscillations between the input capacitance of the transistor and the leakage

inductance of the transformer and from the parasitic inductance from the PCB trace. The resistance of R_g was chosen to 20 Ω.

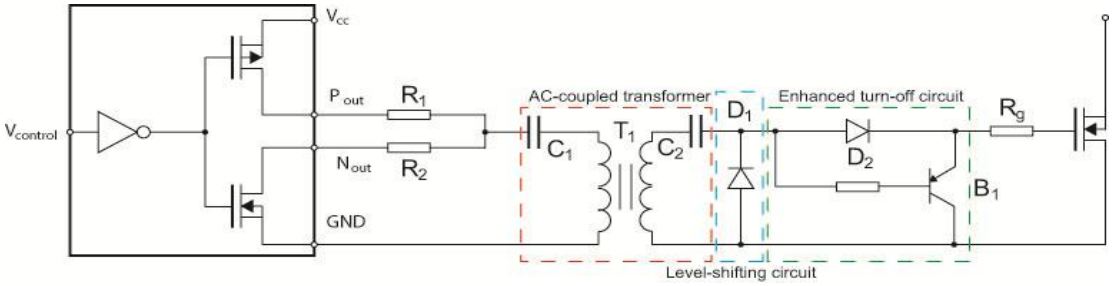

Figure 24. Overview of the configuration used to drive the high-side transistor in the ZVS-CV converter.

The two driver circuits with their corresponding components were evaluated in the simulations software *LTSpice*, the result of the simulations is shown in Figure 25. Both the high- and low-side gate-source voltages are well below the maximum gate-source voltage of 20 V that is allowed for the transistor chosen in Section 3.3.2.1. The high-side gate-source voltage has successfully been referred to the midpoint of the converter. The ringing on top of the high-side signal is damped to reasonable levels by the 20 Ω resistor R_g connected to its gate terminal, while the low-side gate-source voltage only experiences very small ringing.

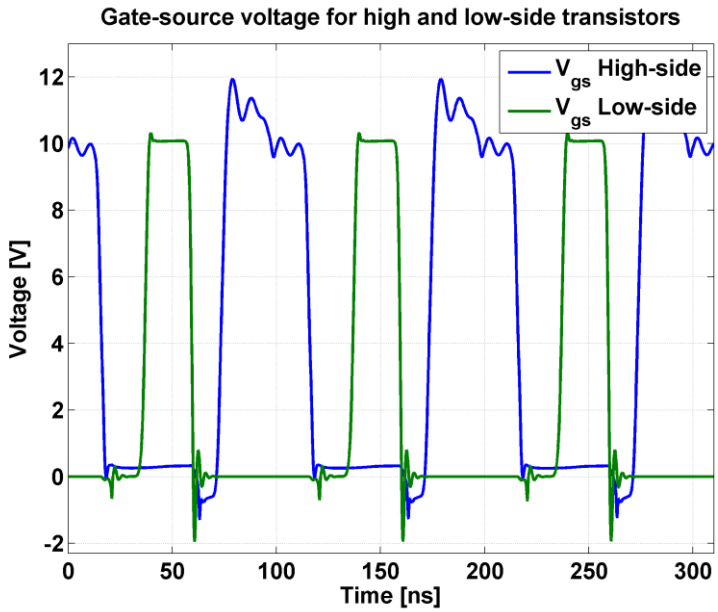

Figure 25. Simulated gate-source voltages for the two transistors in the ZVS-CV converter.

3.3.1.6 Saw tooth wave generator

To generate the PWM signals to the driver circuits in both topologies, a saw tooth wave with a frequency of 10 MHz is compared to the output from the regulator. The saw tooth wave is generated with the use of one comparator and one operational amplifier, four resistors, two diodes and a capacitor. Reference voltages to the negative input of the comparator and to the positive input of the OP-amp are also

required, for simplicity this reference voltage is the same. A schematic of the saw tooth wave generator is shown in Figure 26.

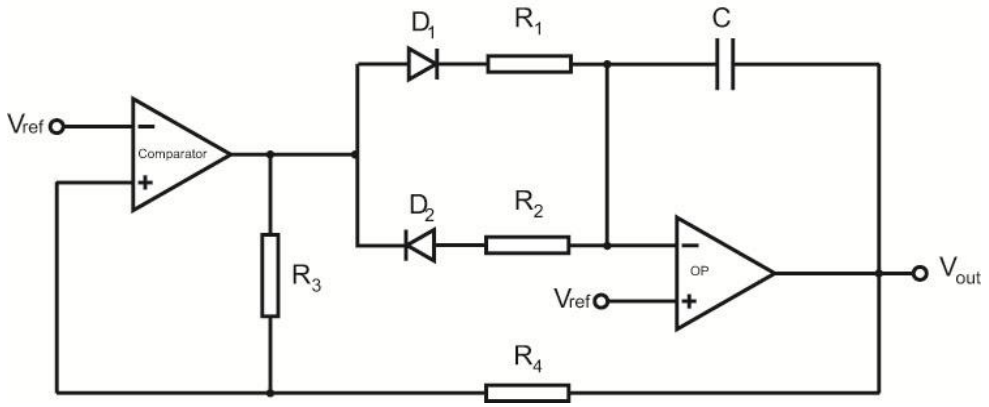

Figure 26. Saw tooth wave generator.

The output voltage from the comparator has two possible stages, high or low, depending on if the voltage at the positive input is lower or higher than the reference voltage applied at the negative input. The output voltage from the comparator and the output voltage from the OP-amp form a voltage divider that determines the positive input voltage to the comparator,

$$V_{ref} = V_{comp,out} + \frac{R_3 + R_4}{R_3}(V_{out} - V_{comp,out}) \tag{3.16}$$

where V_{ref} is the reference voltage, $V_{comp,out}$ is the comparator output voltage and V_{out} is the output voltage from the OP-amp. Depending on the state of the comparator there is a current flowing either through the combination of diode D_1 and resistor R_1or through diode D_2 and resistor R_2. If the OP-amp is assumed to be ideal, the whole current will flow through the capacitance C and charge or discharge it depending on the direction of the current. The magnitude of the current is constant and equal to

$$i_C = \frac{V_{comp,high} - V_{D1} - V_{ref}}{R_1}, \quad V_{comp,in+} > V_{ref} \tag{3.17}$$

$$i_C = \frac{V_{comp,low} - V_{D2} - V_{ref}}{R_2}, \quad V_{comp,in+} < V_{ref} \tag{3.18}$$

Where V_{D1} and V_{D2} are the forward voltage drop of the two diodes and $V_{comp,in+}$ is the positive input voltage at the comparator. A constant current through the capacitor results in a constant rise and fall time of the voltage over the capacitor. The output voltage of the saw tooth wave generator is the voltage at the output of the OP-amp, which is equal to the difference between the reference voltage and the voltage over the capacitor.

The voltage over the capacitor will either decrease or increase depending on the state of the output of the comparator. When the output of the comparator is high, the capacitor is charged and the output voltage from the OP-amp decreases until the combination of R_3 and R_4 makes the voltage at the positive input of the comparator to

fall below V_{ref}. The output of the comparator will then change state from high to low, the current through the capacitor becomes negative, the capacitor is being discharged and the voltage at the output of the OP-amp will increase. The output voltage of the OP-amp increases until the combination of R_3 and R_4 makes the voltage at the positive input of the comparator to rise above V_{ref}. When the voltage rises above V_{ref} the output of the comparator changes state to high, the procedure starts a new cycle.

The changes of the output of the comparator occur when the voltage at the positive input is equal to the negative input, V_{ref}. Using (3.16) determines both the maximum and minimum voltages of V_{out},

$$\hat{V}_{out} = (V_{ref} - V_{comp,low})\frac{R_3 + R_4}{R_3} + V_{comp,low} \tag{3.19}$$

$$\check{V}_{out} = (V_{ref} - V_{comp,high})\frac{R_3 + R_4}{R_3} + V_{comp,high} \tag{3.20}$$

The output voltage swings between $\hat{V}_{out}$ and $\check{V}_{out}$ around the average value

$$V_{out,avg} = \frac{(\hat{V}_{out} + \check{V}_{out})}{2} = V_{ref} + \frac{R_4}{R_3}(V_{in} - \frac{V_{comp,high} + V_{comp,low}}{2}) \tag{3.21}$$

The peak-to-peak value of the output voltage is

$$V_{out,pp} = \hat{V}_{out} - \check{V}_{out} = \frac{R_4}{R_3}(V_{comp,high} - V_{comp,low}) \tag{3.22}$$

By using the basic formula for the charging of a capacitor,

$$i_c = C\frac{dV}{dt} \tag{3.23}$$

the times between the changes of states can be determined. Using (3.22) and (3.23) gives the function

$$t = C\frac{V_{out,pp}}{i_c} \tag{3.24}$$

The rise and fall times are calculated using (3.17), (3.18) and (3.24) as

$$t_{rise} = \frac{\frac{R_4}{R_3}(V_{comp,on} - V_{comp,off})}{V_{in} - V_d - V_{comp,off}}R_2C \tag{3.25}$$

$$t_{fall} = \frac{\frac{R_4}{R_3}(V_{comp,on} - V_{comp,off})}{V_{comp,on} - V_d - V_{in}} R_1 C \tag{3.26}$$

The frequency of the output voltage is then

$$f_{sw} = \frac{1}{t_{rise} + t_{fall}} \tag{3.27}$$

The frequency is dependent both on the ratio between R_3 and R_4, the output states of the comparator, the voltage drop over the diodes, V_{ref}, R_1, R_2 and C. The comparator and diodes are first chosen to some devices with a relatively constant parameters. Thereafter, the ratio between R_3 and R_4 is chosen to get the desired voltage swing. This leaves R_1, R_2 and C to set the rise time, fall time and frequency. This is done by choosing, for instance, C first to some arbitrary value and thereafter R_1 and R_2 to get the correct rise and fall times. The fall time of an ideal saw tooth wave is infinitely short, but this is not possible in practice since other non-idealities will have to be taken into consideration. Some non-idealities are reverse recovery of the diodes, the finite rise and fall time of the comparator and limitations on output currents in the comparator and OP-amp.

The saw tooth wave generator used is designed to have a voltage swing between 1 and 4 Volts, with a rise time of 90 ns and a fall time of 10 ns, which gives a frequency of 10 MHz. The values in the saw tooth wave generator are presented in Table 3.

Table 3. Parts and values used in the saw tooth wave generator.

Part	Value/description
Comparator	LT1719
OP-amp	LT1818
D_1, D_2	BAT46
R_1	10 Ω
R_2	600 Ω
R_3	3900 Ω
R_4	1800 Ω
C	100 pF

3.3.2 Component selection

When dealing with frequencies in the multi-MHz range, through-hole components are seldom used. There are two main reasons, the larger size of the devices that will make the converter larger, and increase stray inductances in the converter, due to both the component legs and the larger size of the converter. Surface mount devices are smaller and allow the use of a separate ground layer; this is beneficial when designing SMPS [20].

3.3.2.1 Switching transistor

As explained in Section 2.3.1, the switching transistors often have the highest losses of the components used in a DC/DC converter. Therefore, the choice of transistors that result in low losses are of high importance. Section 2.3.1 showed that GaN-transistor have the lowest combination of on-resistance and output capacitance. This would theoretically lead to the lowest losses, as both conduction and switching losses are reduced. However, GaN-transistors designed for SMPS are not easily found on the market and the ones found have some disadvantages over traditional Si-transistors. One disadvantage is that most of the GaN-transistors on the market are depletion mode transistors. Depletion mode transistors have a negative threshold voltage and are *normally-on*, this put higher demand on the driver circuits for the transistors which would need negative voltages to turn the transistors off. Other disadvantages with GaN-transistors are the sensitivity to overvoltages, the relatively high price and their small size. Normally, a small size is advantageous but this makes them difficult to handle without correct equipment.

Even if GaN-transistors have better electrical performance in terms of lower on-resistance and output capacitance, the disadvantages, with the more complicated driving of the transistor, the sensitivity to overvoltages, the higher price and the smaller size, become too large for this thesis.

The market of Si-transistors is huge; there are a lot of transistors to choose from, in the end the LDMOS transistor *PD57006-E* was chosen for implementation [11]. The chosen transistor has a low combination of on-resistance and output capacitance and is therefore suitable for use in this thesis. Table 4 summarizes the most important parameters of the *PD57006-E* transistor.

Table 4. Parameters of the PDE57006-E transistor chosen for implementation.

Parameter	Value
$V_{ds,max}$	65 V
$V_{gs,max}$	± 20 V
$I_{D,max}$	1 A
V_{th}	2-5 V
R_{on}	1.8 Ω
C_{OSS}	14 pF
C_{ISS}	27 pF

3.3.2.2 In- and output capacitors

Both input and output capacitors are needed in a converter to filter voltage and current spikes. The output capacitors mainly filter the output voltage to a DC-value, and the input capacitors filter the current drawn from the voltage supply to a DC-value.

The output capacitor bank is built up of several different capacitors with different size, which has various dielectrics and values of the capacitance. Large tantalum capacitors provide a large capacitance value at lower frequencies. But, since the self-resonance frequency of the tantalum capacitors is quite low, lower than 10 MHz, other capacitors with higher self-resonance frequency are also used to provide capacitance at higher frequencies. These high frequency capacitors are ceramic capacitors that are smaller in both size and value compared to the tantalum capacitor. Smaller ceramic capacitors have a much higher self-resonance frequency than tantalum and other electrolytic capacitors. The combination of both large tantalum and small ceramic capacitors gives a low impedance of the capacitance bank over a larger span of frequencies [9].

The designed output filter consists of one tantalum capacitor at 47 µF and a combination of five different ceramic capacitors in the range from 4.7 nF to 4.7 µF. Some of the ceramic capacitors are used twice to provide enough capacitance. A simulation of the impedance in the output capacitor bank versus frequency has been carried out in *KEMET-Spice*. It showed a high capacitance at frequencies up to 50-60 MHz, and a low ESR of around 10 mΩ at 10 MHz.

Because the current from the input is not smooth neither in the Buck or the ZVS-CV converter, input capacitors are also required to decouple the converter from the voltage supply. As for the output capacitors, several different capacitors are used to cover a wider band of frequencies and to share the ripple current. The size of the input capacitance is a few µF, much lower than the output capacitance and is standard practice [9].

3.3.2.3 Inductors

Both the Buck and the ZVS-CV converters use output inductors. There are however a large difference between the output inductance in the Buck converter and in the ZVS-CV converter. The Buck converter uses a larger inductor to smoothen the output current, while the ZVS-CV converter requires a smaller inductor to allow a larger ripple and a negative current through it as explained in Section 2.2.3.

In Buck converter

The required value of the output inductor in the Buck converter was found in Section 3.3.1.1 to be around 20 µH. There are a lot of different suitable inductors on the market. The inductor series *1812PS* and *LPS6235* from *Coilcraft* are used since they provide the required inductance without taking up too much space on the board. The two inductors have a series resistance of 330 and 145 mΩ respectively. With a current of 200 mA the losses in the inductors are

$$P_{loss,DC} = R_{DC} I_{DC}^2 = \begin{cases} 0.33 \cdot 0.2^2 = 13\ mW, for\ 1812PS \\ 0.45 \cdot 0.2^2 = 6\ mW, for\ LPS6235 \end{cases} \quad (3.28)$$

The losses due to the ripple current of 60 mA peak-to-peak are estimated with *Coilcraft's* design guide [21] to be

$$P_{loss,AC} = \begin{cases} 55\ mW, for\ 1812PS \\ 21\ mW, for\ LPS6235 \end{cases} \tag{3.29}$$

The total estimated losses are 68 mW for the 1812PS inductor and only 27 mW for the *LPS6235* inductor. Since the *LPS6235* inductor has lower losses it is chosen for implementation in the Buck converter.

In ZVS-CV converter

The ZVS-CV-topology has special and high demands on the output inductor. The combination of the relatively low inductance of 1.3 µH, the high frequency, and the large ripple current of 800 mA peak-to-peak excludes most of the inductors on the market.

The Q factor is an important parameter when it comes to inductors. The Q factor is defined as

$$Q = \tan\theta = \frac{Im\{Z\}}{Re\{Z\}} = \frac{\omega L}{R_{eq}} \tag{3.30}$$

where L is the inductance of the inductor and R_{eq} is the equivalent series resistance. An ideal inductor has no equivalent series resistance i.e. a θ of 90° and an infinite Q. The Q factor is highly dependent on frequency since both the reactance and the equivalent series resistance varies with frequency.

The equivalent series resistance is a measure that is meant to quantify the losses that could be expected for a certain current and frequency. It is made up of several different factors such as eddy current and hysteresis losses in the core, and DC and AC resistance in the winding and also capacitive effects both between different turns, and between turns and the core.

The best inductors in the range 1-1.5 µH that are available on the market have a Q factor of around 35 at 10 MHz [22]. According to (3.30) this equals a $R_{eq}$of 2.2 Ω. The total rms current of the inductor current consist of two parts, a DC current of 0.2 A and the AC ripple current of 0.8 A peak-to-peak. The rms value of a triangular wave with a peak-to-peak value of 0.8 A is

$$I_{rmsAC} = \frac{I_{p-p}}{2\sqrt{3}} = \frac{0.8}{2\sqrt{3}} = 0.23\ A \tag{3.31}$$

This current give rise to a loss of

$$P_{loss,AC} = R_{eq} I_{rms,AC}^2 = 2.2 \cdot 0.23^2 = 120\ mW \tag{3.32}$$

The losses from the DC current are calculated using the DC resistance which is about 0.7 mΩ for inductors in the class [22]. The power loss is

$$P_{loss,DC} = R_{DC} I_{DC}^2 = 0.7 \cdot 0.2^2 = 30\ mW \tag{3.33}$$

The total losses are then around 150 mW, 2.5 % of the output power, and are considered to be too high for implementation.

Instead of having an inductor with high losses in the ZVS-CV converter, a specially designed inductor that is built on the PCB is used. The inductor windings consist of copper traces directly on the PCB. The core consists of a high frequency material from *Ferroxcube* called *4F1* [23]. In order to construct the inductor some parameters were to be determined for an optimal design in terms of low losses. The core is an E22-core with a flat plate on top. The losses P_{core} in the used inductor core are determined from the data sheet of the core material [24].

The peak flux density is in turn described as

$$\hat{B} = \frac{N\hat{I}}{\mathcal{R}A} \tag{3.34}$$

where N is the number of turns, $\hat{I}$ is the amplitude of the ripple current, $\mathcal{R}$ is the reluctance of the inductor and A is the cross section area of the magnetic path.

The required reluctance for a specific number of turns in the inductor and a specific inductance is

$$\mathcal{R} = \frac{N^2}{L} \tag{3.35}$$

The reluctance of a core with air gap is

$$\mathcal{R} = \frac{\frac{l_e}{\mu_r} + l_{air}}{A\mu_0} \tag{3.36}$$

where l_e is the length of the magnetic path, μ_r is the relative permeability of the core material, l_{air} is the air gap of the core and μ_0 is the permeability of vacuum.

Combining (3.34), (3.35) and (3.36) means that for a certain inductance with a certain number of turns, the needed air gap and the peak magnetic flux, which is directly proportional to the losses, can be calculated as

$$l_{air} = \frac{N^2 A_e \mu_0}{L} - \frac{l_e}{\mu_r} \tag{3.37}$$

$$\hat{B} = \frac{L\hat{I}}{NA_{min}} \tag{3.38}$$

In addition to the core losses there are also losses due to conduction in the copper traces and described by

$$P_{Cu} = \rho \frac{l}{wh} \tag{3.39}$$

where ρ is the resistivity of copper, l is the length of the copper trace and w and h are the width and height of the copper trace. The space available for copper winding in the E22 core is approximately 5 mm (with some margin) including isolation between the windings. The average length of each winding is approximately 65 mm [24]. A usual thickness of the copper layer on PCBs is 35 µm [20]. The skin depth of copper at 10 MHz is around 20 µm [5], which means that the skin effects only has a minor effect on the resistance. If an isolation of about 200 µm between each winding is used the resistance of the windings in the inductor can be calculated as

$$R_{Cu} = \rho \frac{l_{avg} N}{\frac{5 - 0.2(N-1)}{N} h} \tag{3.40}$$

And the resistive losses in the windings are

$$P_{Cu} = R_{Cu} I_{rms}^2 \tag{3.41}$$

where I_{rms} consist of both the DC and the AC part of the inductor current according to

$$I_{rms} = \sqrt{I_{DC}^2 + I_{AC,rms}^2} = \sqrt{0.2^2 + 0.23^2} = 0.31\ A \tag{3.42}$$

The total power loss in the core and the windings are

$$P_{tot} = P_{core} + P_{Cu} \tag{3.43}$$

The losses for a certain inductance and core are only dependent on the number of turns, there are a certain number of turns that gives the lowest losses.

The core losses, copper losses and total losses of the inductor as a function of the number of turns are shown in Figure 27.

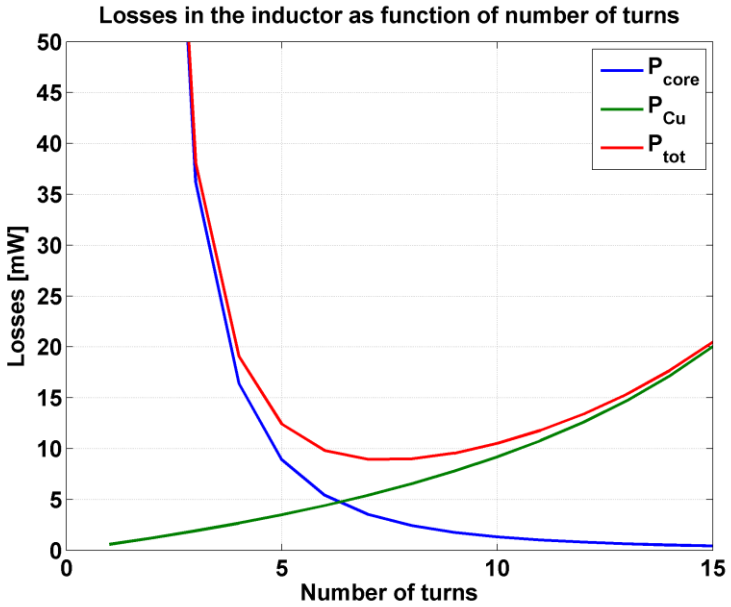

Figure 27. Core losses, copper losses and total losses in the inductor as function of the number of turns. The inductance is fixed at 1.3 µH.

As seen in Figure 27, the lowest losses occur when 7 turns are used, only 9 mW. But for all number of turns in the range 4-14 turns, the power loss is less than 20 mW. A fewer number of turns is easier to design in the CAD software and decreases the risk of errors in the production of the boards. Therefore, 5 turns will be used for the inductor. The air gap needed when using 5 turns is, using (3.42), 1.50 mm. The calculated power loss in the inductor is then 12 mW.

3.3.3 PCB design

The design of the PCB is important in all DC/DC converter applications, but especially in high-frequency applications. The most critical parts when designing are the parts where there are large and fast changes of current. The most critical paths in the Buck and the ZVS-CV converters are:

- Ground - input capacitors - transistor - inductor – output capacitors - ground
- Ground - rectifying diode - inductor - output capacitors - ground.

These traces form current loops which should be as small as possible to minimize voltage spikes that arise when the current swings from on to off, or vice versa, in a short period of time due to stray inductance. A way to reduce the inductance of the loops is to have a grounding layer below the component layer. The current is then able to mirror itself just under the current traces at the component side. The current always tries to follow the path with the lowest impedance, which is the path where the current mirrors itself. It is important to have a grounding layer that is completely filled, without any slits, to enable the current to take the path with the lowest possible impedance [20].

With the same argument as above, it is important to place the input capacitors as close to the drain of the transistor and ground as possible. The output capacitors should be as close to the inductor and ground as possible.

When drawing the layout of the PCB, room for diode snubbers close to the rectifying diode has been added as it is important that they are located close to the diodes in order to function properly.

All of the components are mounted on the same side of the boards, the top side. The top sides also carry all of the signal paths and supply rails. The bottom side of the Buck board is completely, except for some connectors for supply voltages, covered with copper as a grounding layer. The bottom layer in the ZVS-CV converter is almost covered with copper, the exception is two traces, one from the inner side of the inductor to the output voltage area, and the other is a signal out from the saw tooth wave generator to the low side control circuit. The PCB layout for both the Buck converter and the ZVS-CV converter are found in Appendix B. Pictures of the converters with mounted components are seen in Appendix C

4 Results and Discussion

This chapter presents results and discussion of measurements on the implemented Buck and ZVS-CV converters and their building blocks. The chapter presents measurements on converter function, converter efficiency and output voltage ripple. Thermal analysis of both converters has also been carried out to further investigate the losses in the converters. The chapter ends with a comparison between the two converters. A list of the equipment used during measurements is found in Appendix D.

4.1 Saw tooth wave generator

The implemented saw tooth wave generator has been investigated in Section 3.3.1.6. It was shown that the frequency, amplitude and DC-offset of the saw tooth wave was dependent on several factors, including comparator output levels and diode forward voltage drop. To ensure that the wave generator works as in theory, simulations with models of real components were carried out in *LTSpice*. However, when implementing the saw tooth wave generator with the values from Table 3, it was seen that the actual frequency in the real generator was much lower than in the simulations. In order to increase the frequency to 10 MHz, the value of resistor R_2 was lowered down to 600 Ω.

The main reasons for obtaining the wrong frequency is believed to be that the comparator does not output a fixed high voltage of 4.5 V that was stated in [15]. The actual measured voltage was about 3.2 V, leading to a slower current charging the capacitor and the frequency become much lower. Other factors are the finite slew rate of the comparator when changing from on state to off state, the forward-voltage drop over the diodes, that is slightly different than expected and the reverse recovery of the diode which is also seen in both simulations and in practice. The measured waveform for the saw tooth wave obtained from real measurements is seen in Figure 28. The measured frequency of the saw tooth wave is 9.8 MHz.

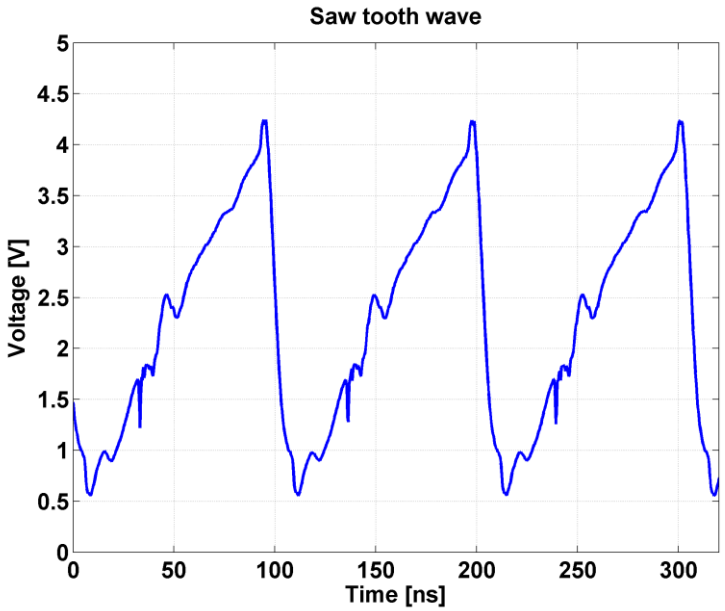

Figure 28. The generated saw tooth wave.

The measured voltage swing is very close to the designed swing between 1 and 4 V, there is only a small over- and undershoot of 0.2 and 0.4 V respectively. The measured DC-offset is almost exactly as the designed 2.5 V.

4.2 Buck converter

This subsection shows results of measurements on the implemented Buck converter. Measurements on converter functionality, output voltage ripple and efficiency has been carried out. Also, a thermal analysis of the converter has been carried out.

4.2.1 Functionality

To make sure that the Buck converter works as expected, measurements on signals in the converter has been carried out. The measurements were performed under a full load of 6 W, with a fixed regulator output voltage provided from an external voltage supply unit, to regulate the output voltage to 30 V. Signals in the signal path of the Buck converter is shown in Figure 29, the top graph shows the input signals to the main comparator which is the regulator output voltage and the saw tooth wave. The comparator output is supposed to change during the crossing of the regulator voltage and the saw tooth wave. The middle graph of Figure 29 shows the output from the comparator, which looks like a PWM signal. There is a small delay between the crossing and the change of the comparator output. This is both due to the built-in hysteresis of the comparator, the internal delay and the finite slew rate of the comparator. In total, the delay from the crossing of the regulator output and the saw tooth wave and the time when the regulator output voltage has decreased to a value lower than 2.5 V is 5-6 ns.

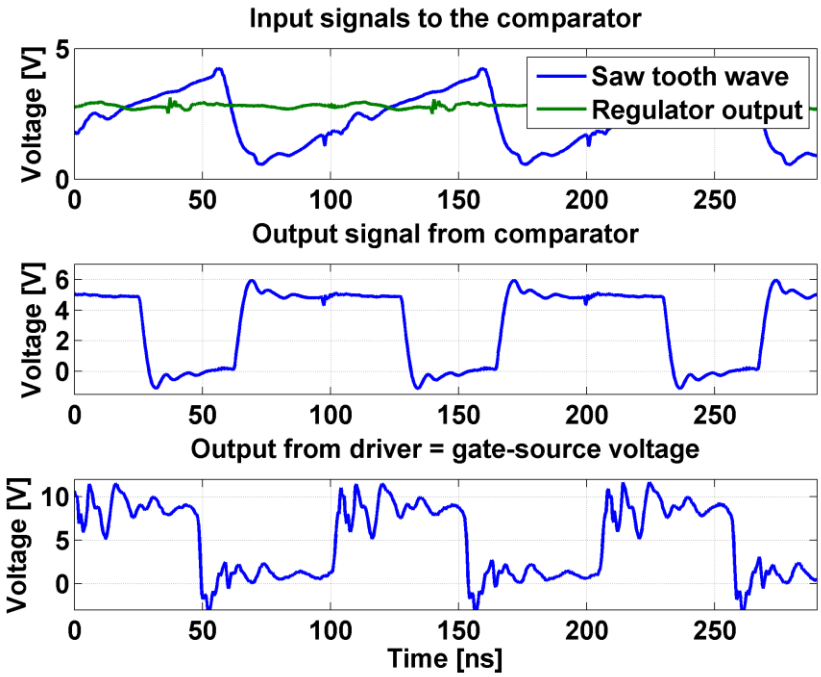

Figure 29. Signals in the Buck converter.

The comparator output is connected to the input of the driver circuit. Ideally, the driver circuit would change its output directly when the input changes, but it is seen in the middle graph and the bottom graph of Figure 30 that there is a delay of approximately 35 ns before the

driver output changes. This dramatically changes the phase marginal in the converter and could lead to instability if the regulator is not designed in a good way. The driver output has large oscillations which also could decrease the performance of the converter since the transistor might not be fully on for the whole duty-cycle. The oscillations of the driver output could be a result of both insufficient damping on the output of the driver and that the driver circuit is working on its limit. The oscillations could probably be decreased if damping resistors were added, if the layout of the PCB traces could be redesigned in a better way, or if a better driver circuit was implemented. Another possibility is that the measurement equipment used influences the measurements. This could be reduced by using voltage probes designed for high frequency measurements.

To investigate the switching behavior of the Buck converter, the gate-source and drain-source voltage of the switching transistor has been measured under full load, which is shown in Figure 30. It is seen that the transistor switches on while the drain-source voltage is 50 V, this leads to significant switching losses, especially at such high frequencies as 10 MHz.

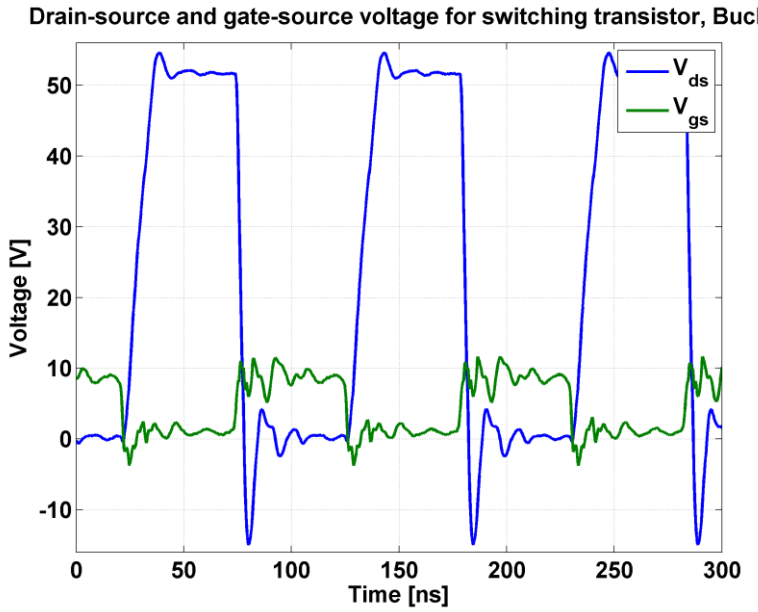

Figure 30. Measured drain-source and gate-source voltages for the switching transistor in the Buck converter.

The Buck converter performed well for loads above 1.8 W. But, when the output load decreased below 1.8 W the output voltage changed rapidly. It seems like the driver from *Linear Technology* is not able to turn on the transistor in the correct way and the ability to regulate the output voltage is lost. The reason for losing the control of the converter has not been investigated in detail.

4.2.2 Converter efficiency

An evaluation of the efficiency of the Buck converter was done by measuring input power from the main 50 V supply, input power from the 10 V supply, for powering of the driver and control circuits, and output power. A fixed regulator output voltage from an external supply was used to manually change the output voltage to 30 V.

The input power from the two supplies as a function of output power is shown in Figure 31. It is seen that the power from the 50 V supply increases with increased output power. This is

expected as this is the main supply of the output power. The power delivered from the 10 V supply is independent of output power at a level of about 570 mW. This is also expected as the 10 V supply does not supply the main power stage with power, but only the IC-circuits such as comparators, OP-amps and driver circuit. All ICs but the transistor driver operates with a supply voltage of 5 V. The LDO used to supply these ICs with 5 V has an efficiency of 50 % [25], which means that the loss in the LDO is equal to the power lost in all of the ICs supplied at 5 V combined.

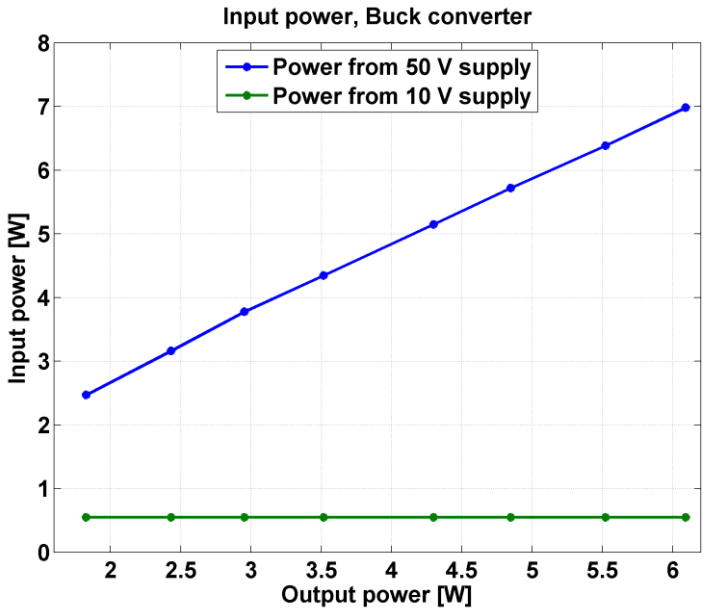

Figure 31. Measured input power from both the main 50 V supply and the 10 V supply as a function of output power.

The total efficiency of the Buck converter is presented in Figure 32 along with the efficiency of the power stage alone. The maximum efficiency, for both the complete converter and for the power stage, is achieved at the maximum output power of 6 W. The efficiency of the complete converter is then 80.8 %, while the efficiency of the power stage alone is 87.2 %.

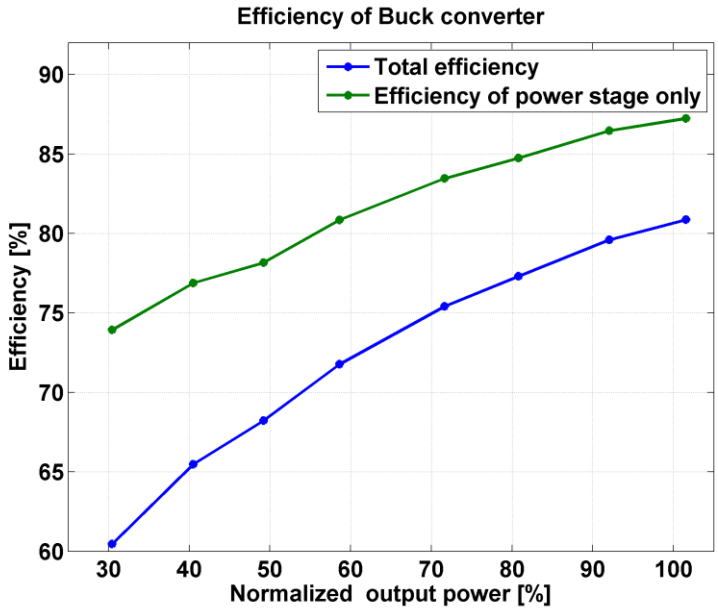

Figure 32. Calculated total efficiency of the Buck converter and the efficiency of the output power stage alone.

4.2.3 Output voltage ripple

The output voltage ripple of the Buck converter has been measured and is presented in Figure 33. The impact from the switching is easily seen as one large and one small voltage spike. The peak-to-peak value of the voltage ripple is about 500 mV which is much higher than the goal of 100 mV set in Section 1.2. The total output capacitance used when measuring was around 25 µF, built up of several sizes of ceramic capacitors. Probably, a larger value and a better choice of capacitors would decrease the voltage ripple.

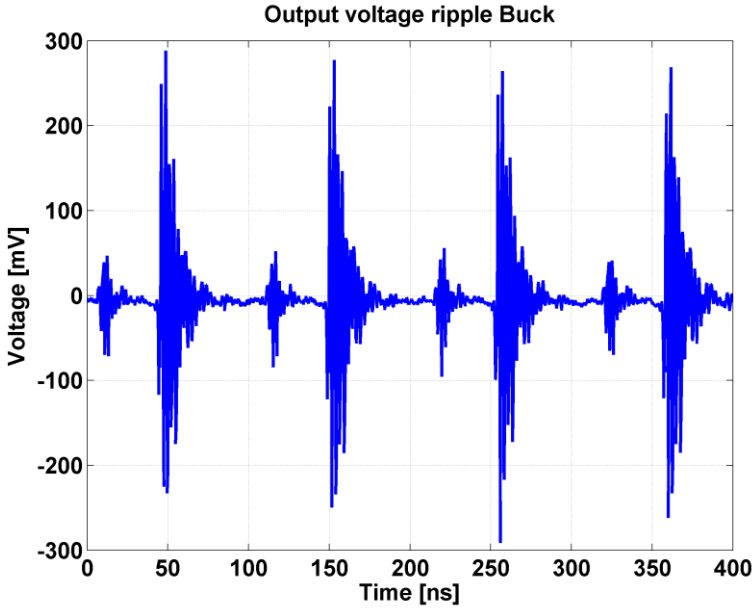

Figure 33. Measured output voltage ripple in the Buck converter.

The harmonic content of the output voltage, for frequencies up to 40 MHz, is seen in Figure 34. It is obvious that there is a large component at 9.8 MHz, which is the switching component. The amplitude of that component is about 40 dBµV_{rms}, which is lower than the

51 $dB\mu V_{rms}$ that was set as a goal in Section 1.2. The magnitude of the harmonics are lower than 20 $dB\mu V_{rms}$ for frequencies in the span 3-10 MHz, and is getting larger for lower frequencies. This is probably due to errors when performing the FFT.

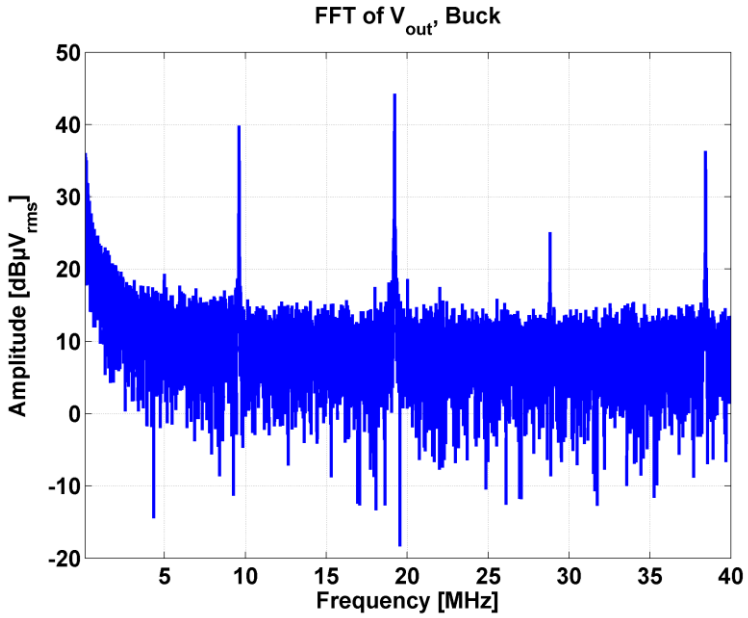

Figure 34. FFT of the output voltage, Buck converter.

4.2.4 Thermal analysis

To get a picture of where most of the losses in the Buck converter occur, a thermal image showing the temperature of the components in the converter, has been taken at full load and is shown in Figure 35.

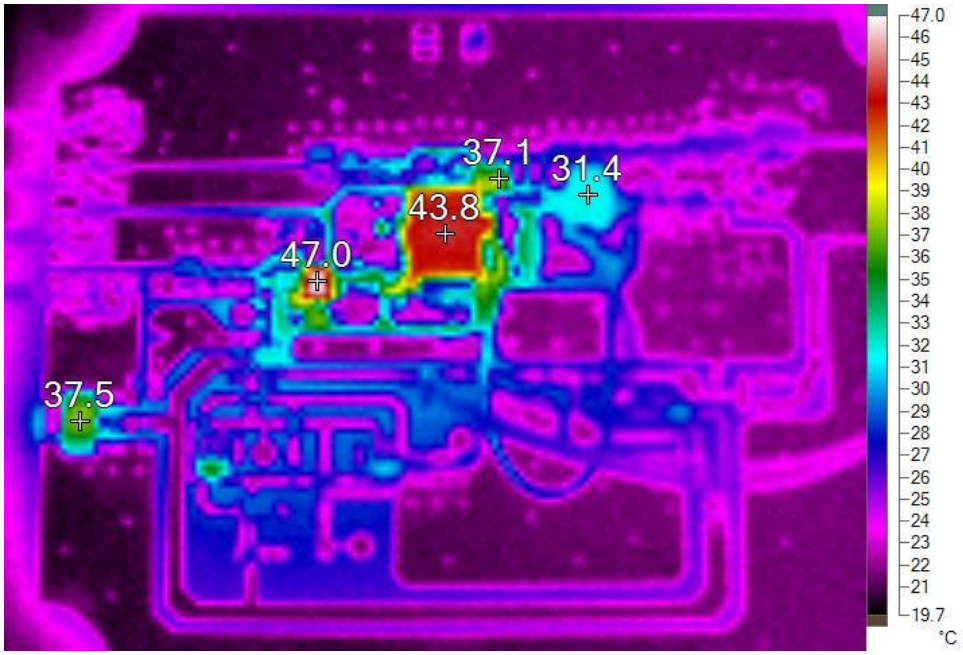

Figure 35. Thermal image of the Buck converter.

The figure clearly shows the temperature for different components. The components with the highest temperature are the transistor in red with a temperature of 43.8 °C, the driver in red-

white at a temperature of 47.0 °C and the LDO to the left in green with a temperature of 37.5 °C, the freewheeling diode on the top-right of the transistor has a temperature of 37.1 °C. The three smaller warmer components in the bottom of the picture are the OP-amp in the saw tooth wave generator and the comparator in the saw tooth wave generator. The output inductor has a temperature of 31.4 °C.

The losses in some of the components can be estimated using the thermal resistance of each of the components from their datasheets. For some of the components, the thermal resistance is not applicable for the mounting used or because they are mounted on places where several components dissipate their heat. Therefore, only losses in the output inductor, driver circuit and the LDO are estimated through thermal analysis.

Table 5. Estimation of power losses, Buck converter.

Component	**Thermal resistance [°C/W]**	**Estimated loss [mW]**
Output inductor	85	110
Driver circuit	40	550
LDO	110	115

Since the LDO has an efficiency of 50 %, the total losses for all of the components connected to the 5 V supply is the same as the loss in the LDO, 115 mW. The sum of the estimated losses for the driver, LDO and all of the components with 5 V supply is then around 680 mW, which is quite close to the measured loss of 570 mW.

The losses in the output inductor are around 1.9 % of the output power at full load, if another better inductor would have been used the losses could have been decreased. The drawback of changing the inductor is that the size would probably need to be made larger.

4.3 ZVS-CV converter

This section shows results of measurements on the implemented ZVS-CV converter. Measurements on converter functionality, output voltage ripple and efficiency has been carried out. Also, a thermal analysis of the converter has been carried out.

4.3.1 Control circuit functionality

In order to evaluate the designed control circuit from Section 3.3.1.4, measurements on the signals in the control circuit has been performed. Figure 36 shows the measured waveforms from the ZVS-CV converter´s control system.

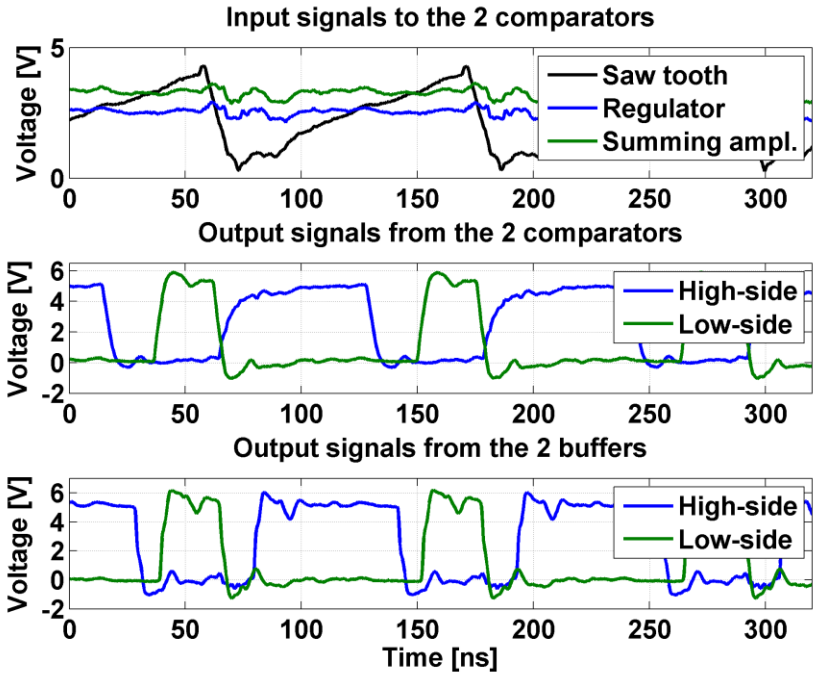

Figure 36. Measured signals in the control circuit of the ZVS-CV converter.

In the top part of Figure 36 the saw tooth wave, the regulator output and the summing amplifier output voltages are shown. It is seen that the summing amplifier acts as designed providing an offset roughly comparing to 20 % of the amplitude of the saw tooth wave.

The waveforms in the middle of Figure 36 are the high and low-side comparator outputs.
It is observed that the offset provided by the summing amplifier reduces the duty-cycle of the low-side comparator output, and provides the dead time expected from Section 3.3.1.4.

In the lower part of Figure 36 the output from the high and low-side control paths are shown. The dead time introduced by the offset between regulator and summing amplifier output voltage has successfully been divided between the turn on and off for both signals by the RC-network described in Section 3.3.1.4. The measured waveforms from Figure 36 shows that the control circuit works as designed providing around 10 ns dead time between both turn on and turn off for both the high and low-side signals.

4.3.2 Driver functionality

The gate-source voltage for the high and low-side transistor in the ZVS-CV converter was measured to evaluate the functionality of the driver circuit and compare it to the results obtained from simulations. Figure 37 shows the measured gate-source voltage with an input voltage of 50 V and an output voltage of 30 V. The load connected to the converter output consumed 6 W during the measurements.

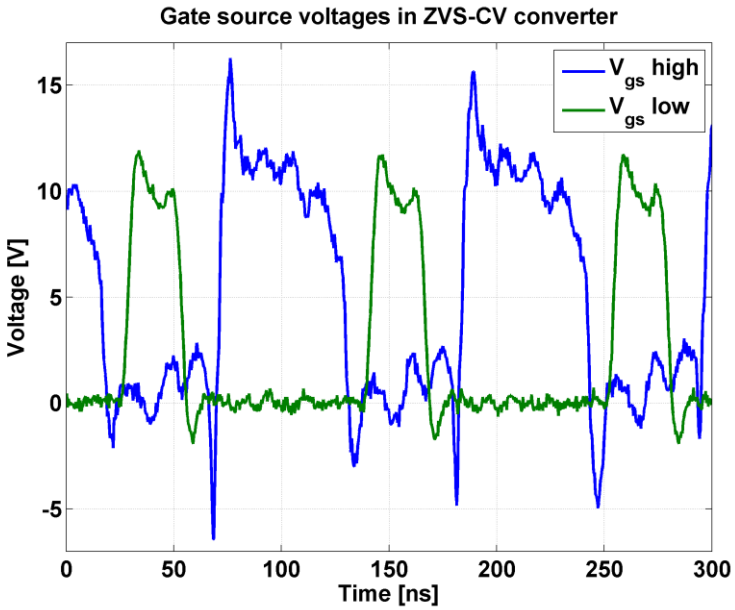

Figure 37. Measured gate-source voltages in the ZVS-CV converter.

The waveforms in Figure 37 correspond well with the simulated voltages from Figure 25, but with a slightly lower switching frequency of 9.0 MHz. The reason for decreasing the switching frequency from 10 to 9.0 MHz is that the low-side driver had some troubles with transmitting such short pulses. If the length of the dead times would be changed, the low-side driver could probably function at 10 MHz as well.

The high-side gate-source voltage suffers from higher ringing than the low-side gate-source voltage. This is due to the leakage inductance from the transformer in the high-side signal path and was identified in simulation. The measured voltages overall suffers from higher ringing than the simulated waveforms, this is most likely due to higher parasitic inductances and capacitances than used when evaluating the circuit in simulation.

4.3.3 Removal of switching losses

To investigate how the ZVS-CV converter performs in terms of removing the switching losses from the transistors, measurements of the drain-source and gate-source voltages for the two transistors has been carried out.

The voltage waveforms are measured with an input voltage of 50 V and an output voltage of 30 V. The load is set to 2.5 W since this output power stage reaches its maximum efficiency at this load, as seen in Section 4.3.4. The voltage waveforms for both transistors are shown in Figure 38 together with the inductor current.

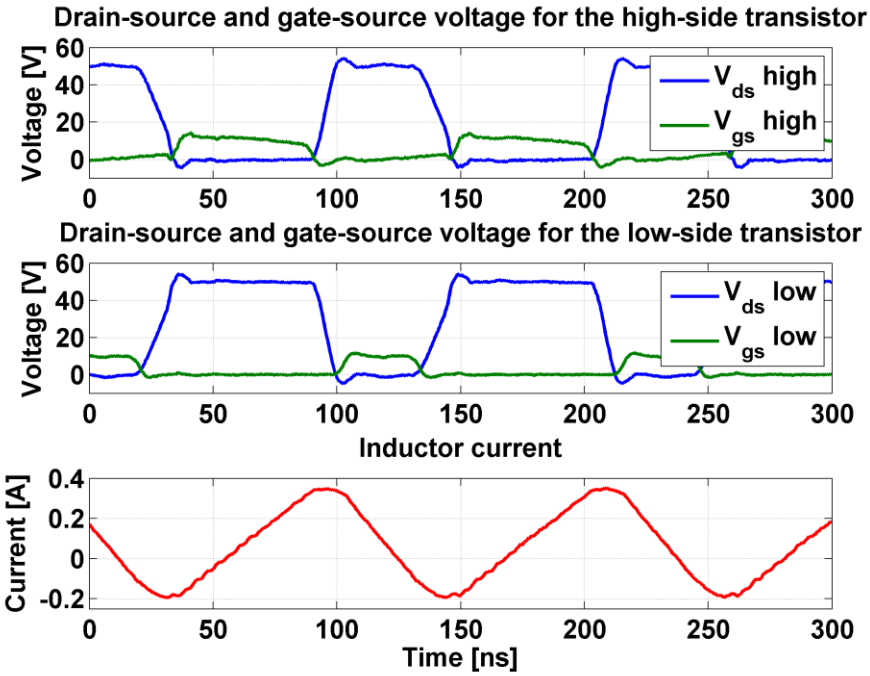

Figure 38. Measured drain-source and gate-source voltages for the two transistors.

It is observed that both the high and low-side transistors are turned on and off under ZVS, thus reducing the switching loss significantly.

The inductor current ripple was calculated in Section 3.3.1.2 to 0.80 A, which is 45 % higher than the measured current ripple of 0.55 A. The decreased current ripple is likely to be a result of having a higher inductance than calculated. The decreased current ripple will change the load range where zero voltage switching is possible since the voltage rise and fall of the midpoint will become slower. Other than the lower current ripple, the measured waveforms correspond well with the theoretical results from Section 2.2.3.

4.3.4 Converter efficiency

Similar to the Buck converter, measurements on input and output power, and calculations of the efficiency of the converter has been carried out. A fixed regulator output voltage from an external supply was used to manually change the output voltage to 30 V.

The input power of the ZVS-CV converter is seen in Figure 39. The power from the 50 V supply increases with increased output power; this is expected as this is the main power supply from which the output power is delivered. The 10 V supply supplies the two drivers with their power, and all of the other ICs through the LDO. The power from the 10 V supply is 1.2 W and is constant over the whole operating range. This is more than twice of the power delivered from the 10 V supply in the Buck converter. The reason for the increased power is the increased number of components that are used at 10 and 5 V. The two driver circuits are responsible for the major power loss, as seen in Section 4.3.6, and the LDO that supplies all the comparators, OP-amps and buffers. The efficiency of the LDO is 50 %, and the power lost in the LDO is equally large as for all of the 5 V ICs combined.

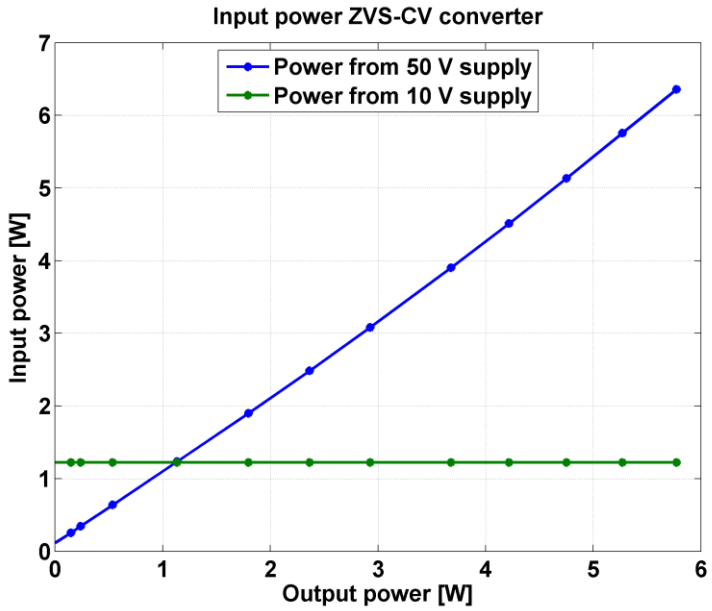

Figure 39. Measured input power from the two voltage supplies as a function of output power.

The total efficiency of the ZVS-CV converter is shown in Figure 40. The maximum total efficiency is achieved at full load, 6W, and is 76.1 %. The total efficiency increases with load, which is expected since the constant power delivered from the 10 V supply becomes a smaller portion of the total input power. If only the power stage alone is considered, the maximum efficiency is 95.2 %, at a normalized output power of 40 %, which is equal to 2.4 W.

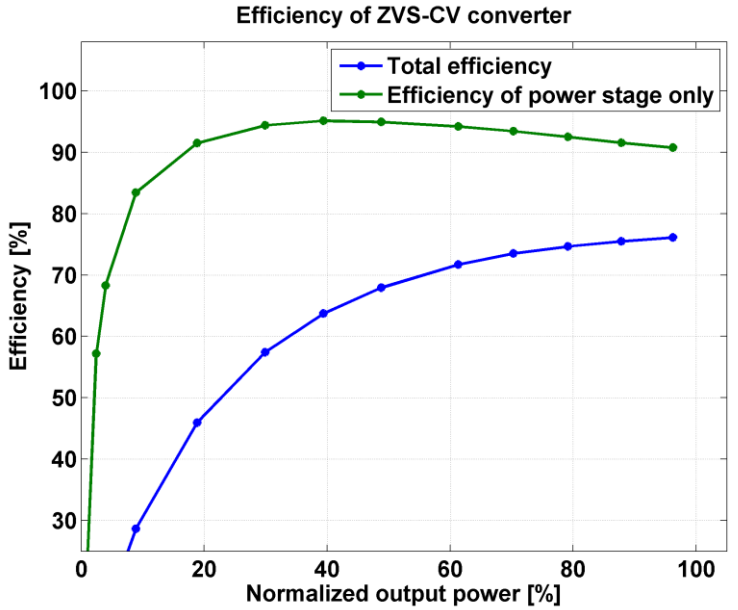

Figure 40. Calculated efficiency of the ZVS-CV converter, both for the power stage alone and for the complete converter.

4.3.5 Output voltage ripple

The output voltage ripple for the ZVS-CV converter is measured and presented in Figure 41. The switching pattern of the converter is easily seen as the underlying square wave, with a peak-to-peak value of about 40 mV. On top of the square wave there are high frequency voltage spikes with a magnitude of 60 mV. The total peak-to-peak voltage ripple of the converter is around 125 mV, only slightly higher than the goal of 100 mV set in Section 1.2. The output voltage ripple is dependent on the types and values of the capacitors in the output filter. Adding additional fast capacitors and decreasing the ESR of the capacitor bank would result in a decreased output voltage ripple.

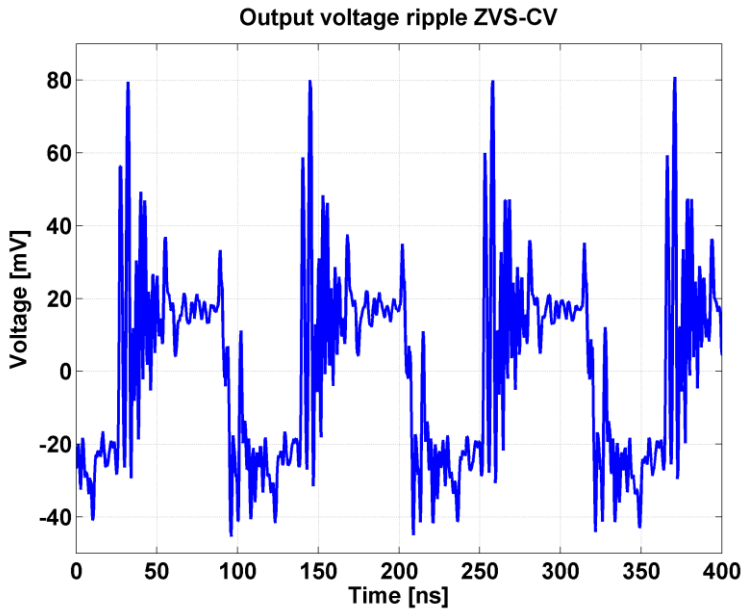

Figure 41. Measured output voltage ripple in ZVS-CV at full load.

The harmonic content of the output voltage is seen in Figure 42. The largest harmonic is the harmonic at the switching frequency of 9.0 MHz. The amplitude of the voltage at 9.0 MHz is 61 $dB\mu V_{rms}$, which is larger than the goal of 51 $dB\mu V_{rms}$ for all frequencies up to 10 MHz, set in Section 1.2. The harmonic content of multiples of the switching frequencies is above 50 $dB\mu V_{rms}$ for all harmonics up to the forth harmonic at 36 MHz. However, for frequencies below 10 MHz there is no component with a magnitude above 30 $dB\mu V_{rms}$. The magnitude of the 9.0 MHz component could probably be made smaller if the output capacitors were chosen with more care, i.e adding fast capacitors with a low ESR.

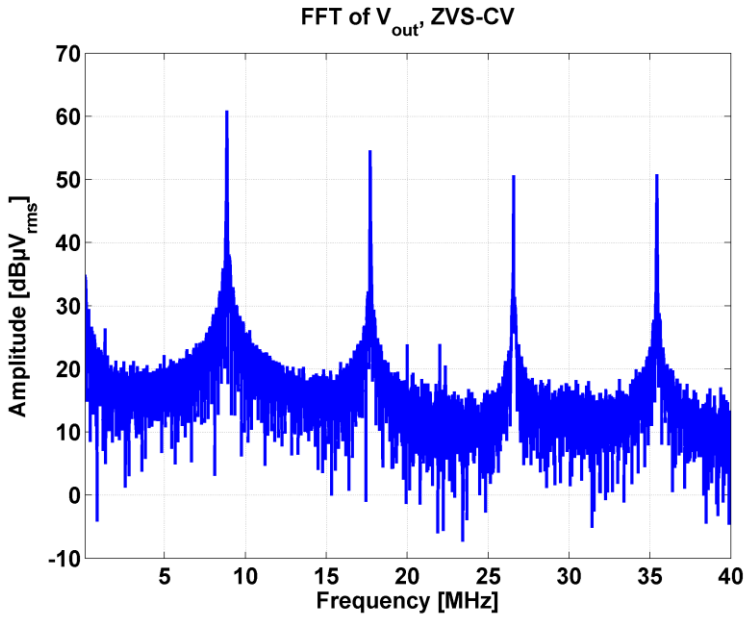

Figure 42. Harmonic content of the output voltage in the ZVS-CV converter.

4.3.6 Thermal analysis

As for the Buck converter, a thermal analysis of losses has also been performed for the ZVS-CV converter, a thermal image of the converter is shown in Figure 35.

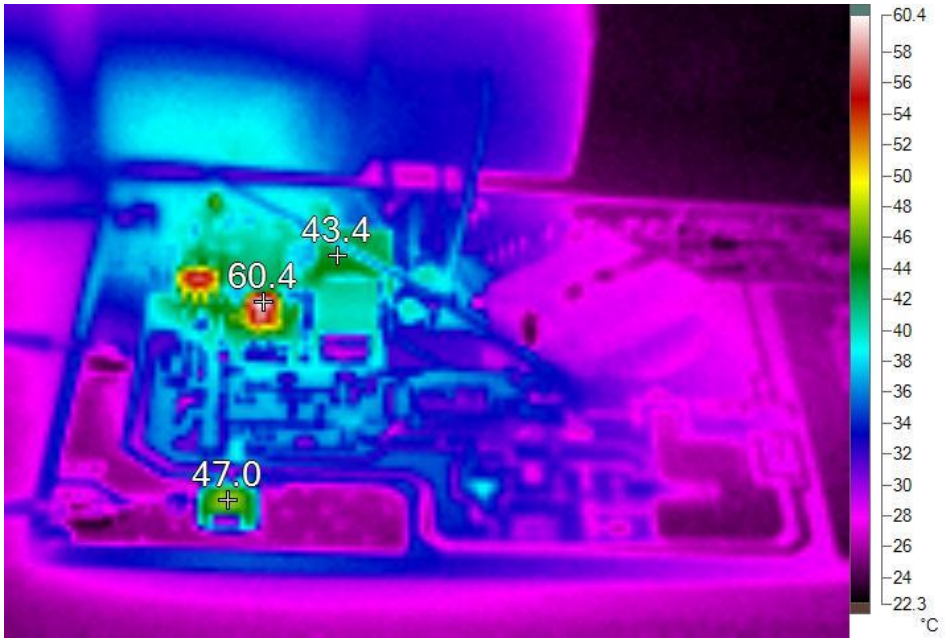

Figure 43. Thermal photo of the ZVS-CV converter at full load.

The figure clearly shows the components with the highest temperatures, it is the high-side transistor in green with a temperature of 43.4 °C, the drivers in red-white with a temperature of around 60 °C, the LDO at the bottom in green with a temperature of 47.0 °C, and also the transformer in the high side driving circuit to the top-left with a temperature of approximately 45 °C. Like for the Buck converter, estimations of losses cannot be performed for all components, but estimated losses for the components with a reasonable result are shown in Table 6.

Table 6. Estimation of power losses, ZVS-CV converter.

Component	Thermal resistance [°C/W]	Loss [mW]
Driver circuit x2	175	200 each
LDO	110	200
Transformer	275	75

Since the LDO has an efficiency of 50 %, the total losses for all of the components connected to the 5 V supply is the same as the loss in the LDO, 200 mW. The sum of the estimated losses for the driver, LDO, all of the components with 5 V supply and the transformer is around 875 mW, which is a bit lower than the measured power loss of 1200 mW. But, there are many components which have not been taken into consideration e.g. resistors, diodes and the PNP-transistor in the driver circuit. Therefore, the estimation of the losses in the drivers, LDO and transformer is considered to be a good estimation of the actual losses in these components.

4.4 Comparison of the two converters

Results from measurements of the Buck and the ZVS-CV converters are presented in Sections 4.2 and 4.3. This section compares the results from measurements on the two converters and points out the most important differences. The comparison is done with a switching frequency of 9.8 MHz for the Buck converter and 9.0 MHz for the ZVS-CV converter. The reason for having only 9.0 MHz in the ZVS-CV is explained in Section 4.3.2.

4.4.1 Load range, stability and controllability, voltage ripple

The performance of the implemented Buck and the ZVS-CV converter differs when it comes to load range, stability and controllability. The ZVS-CV converter performs well in all categories, it is able to function very well at light loads and the output voltage can be regulated to 30 V for all loads up to full and with different input voltages. The Buck converter on the other hand has only a limited load range before much of the control of the converter is lost. For loads below 1.8 W, the control of the converter is lost. As explained in Section 4.2.1 it seems like the driver circuit loses its ability to turn the switching transistor fully on.

The output voltage ripple is much lower in the ZVS-CV converter than in the Buck converter. The voltage ripple is around 125 mV for the ZVS-CV compared to around 500 mV for the Buck converter. The reason for the lower output ripple is probably the more smooth current and voltage waveforms in the ZVS-CV converter. The Buck converter is hard-switched and the fast switching of the transistor seems to propagates to the output, resulting in high voltage ripple.

If the frequency spectra of the output voltage are compared, the Buck converter performs better, it has a voltage ripple of only 40 $dB\mu V_{rms}$ at its switching frequency, compared to 61 $dB\mu V_{rms}$ for the ZVS-CV converter at its switching frequency. The higher voltage ripple at the switching frequency components in the ZVS-CV converter is likely a result from the much higher inductor current ripple that is needed in the converter and the ESR of the output capacitors. The ripple could be decreased with adding more capacitors at the output of the converter, but with the disadvantage of increasing the size of the converter.

4.4.2 Efficiency

The efficiency of both the Buck and the ZVS-CV converters are shown in Figure 44. It is seen that the Buck converter has better total efficiency in the output load range between 35 and 100 %; this is especially true at higher loads. However, the differences are small, between 0-5 % over the entire load range. If only the efficiency of the output power stage is considered, the ZVS-CV converter has much higher efficiency, above 90 % for all normalized loads above 20 %. The efficiency of the power stage in the Buck converter is maximum 87 % at full load and decreases fast with decreased load, while the efficiency in the ZVS-CV converter actually increases with decreases load, up to 95 % at 40 % load.

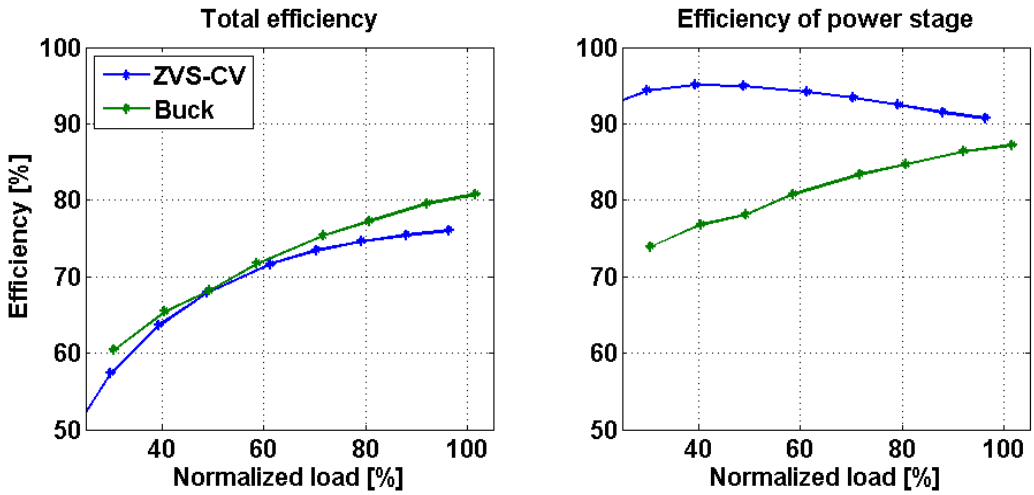

Figure 44. Comparison between the efficiency of the Buck and the ZVS-CV converters, both total efficiency and efficiency of the power stage alone.

The result of the increased efficiency in the power stage of the ZVS-CV converter compared to the Buck converter indicates that the switching losses actually have been removed to a large extent in the ZVS-CV converter. The prize of the increases efficiency in the power stage is paid with increased losses in the ICs, control and driver circuits in the ZVS-CV converter. The losses from these components are about as large as the removed losses in the power stage. Therefore, the total efficiency of the two converters is almost the same for the Buck and the ZVS-CV converter. If the auxiliary components were chosen with more care in the ZVS-CV converter, the total efficiency could probably be made higher than in the Buck converter.

One obvious improvement would be to change the LDO that converts the 10 V supply voltage to 5 V, which is used by several of the ICs. If a 10/5 V converter with an efficiency of 90 % would have been used, 100 mW would have been saved in the Buck converter and 180 mW would have been saved in the ZVS-CV converter. The overall efficiency of the Buck converter would increase with 1.7 % at full load, and even more at lighter loads, to a maximum of 80.5 %. The overall efficiency of the ZVS-CV converter would increase with 3.0 % at full load, up to 79.1 %.

Another possibility to increase the efficiency of the converters is to use transistors that could be fully on at a gate-source voltage of 5 V, thus removing the need for the LDO, or to use auxiliary components with a supply voltage of 10 V.

5 Conclusions

During this master thesis different converter topologies suitable for a switching frequency of 10 MHz have been investigated. Two different topologies, a Buck converter and a ZVS-CV converter have successfully been implemented in hardware. A reference saw tooth wave generator, a control and a driver circuit for the ZVS-CV converter have also been designed and implemented.

The implemented saw tooth wave generator shows good performance, but the measured frequency was not exactly the same as the designed. The frequency of the saw tooth wave is however easily changed by changing only one resistor.

The control circuit and driver network designed and built for controlling the switching scheme for the two transistors in the ZVS-CV converter works as designed, but the driver circuit used for driving the switching transistor in the Buck converter has troubles when driving light loads. Therefore, the Buck converter only works as intended for loads greater than 1.8 W.

Both converters show a maximum efficiency above 75 %, the Buck converter has a maximal total efficiency of 80.8 % and the ZVS-CV has a maximum efficiency of 76.1 %. The lower efficiency of the ZVS-CV converter is explained by the power lost in the extra control and driver circuits added to the converter.

The measurements of the ZVS-CV converter show that the switching losses occurring in the Buck converter have been removed to a large extent. The measured efficiency of the power stage alone in the ZVS-CV converter has been raised to a maximum of 95.2 %, compared to a maximal efficiency of 87.2 % in the power stage of the Buck converter.

The drawbacks of the ZVS-CV converter are the increased complexity of the control of the two transistors and the higher voltage ripple component at the switching frequency, due to the larger current ripple associated with the topology. The size of the ZVS-CV converter is also larger since more components are needed. However, this thesis has not been focused on decreasing the size of the two converters, since a larger converter is easier to work with in practice.

Unfortunately, no regulators have been implemented in the converters. The regulating capabilities have not been investigated further than by ensuring that the output voltage can be controlled by changing the regulator output voltage.

5.1 Further work

Even though both the Buck and the ZVS-CV converter are working properly, there is room for improvement in both converters. The driver circuit in the Buck converter does not work properly at light loads and a better driver circuit could probably improve the converter operation at light loads.

The efficiency of the ZVS-CV converter could be further increased if switching transistors with a lower on-resistance than 1.8 Ω was used. However, this would require some changes in the switching scheme, since the rise and fall time for the voltage of the midpoint of the converter would change. An adaptive control of the dead times in the ZVS-CV converter

could increase the efficiency and the load-range of the converter. But, this would lead to increased complexity and maybe the need for a very fast digital control.

Another way to improve efficiency of the converters is to use better transistors based on GaN. GaN-transistors have both lower resistance which reduces conductive losses, and lower capacitance which means that driver circuits rated for lower power could be used.

Since no regulator has been implemented, there is a need for investigation and implementation of a regulator scheme before the converters can be used in real applications. Also, the converters have not been tested under pulsed loads which could also be an interesting topic for further work. Future work could also include decreasing the size of the converters.

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Appendix

A. Complete schematics

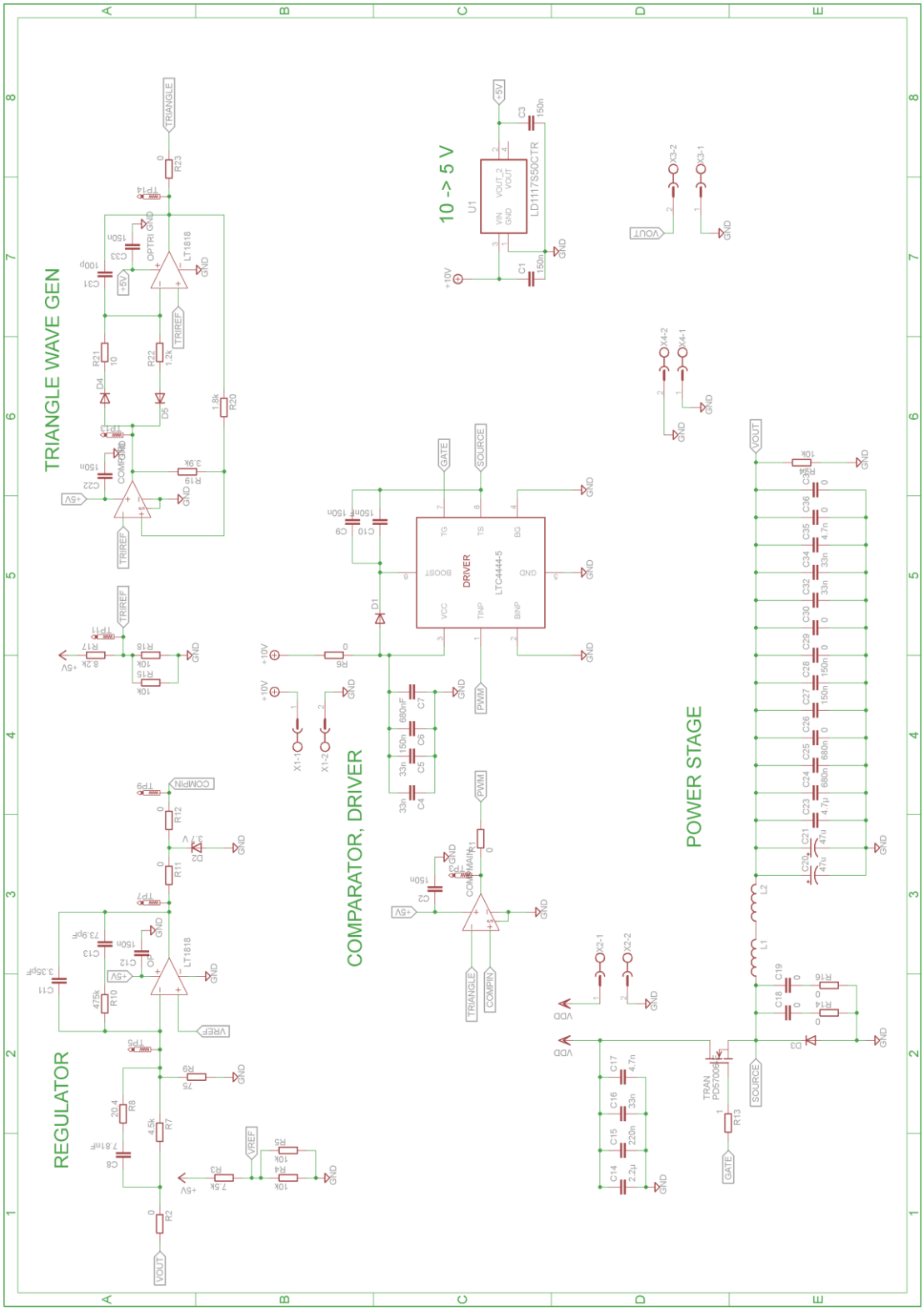

Figure 45. Complete schematic, Buck converter.

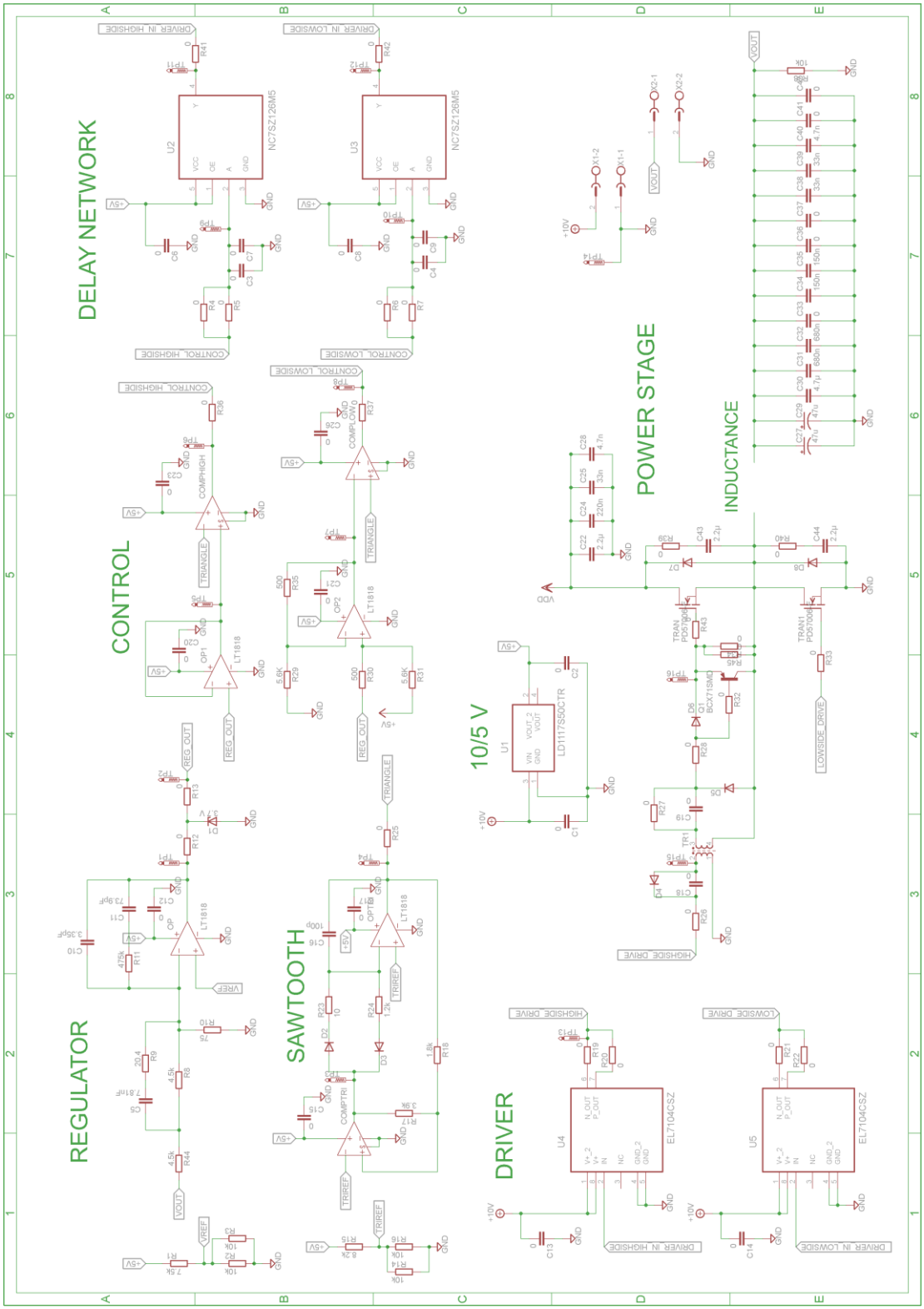

Figure 46. Complete schematic, ZVS-CV converter.

B. PCB layouts

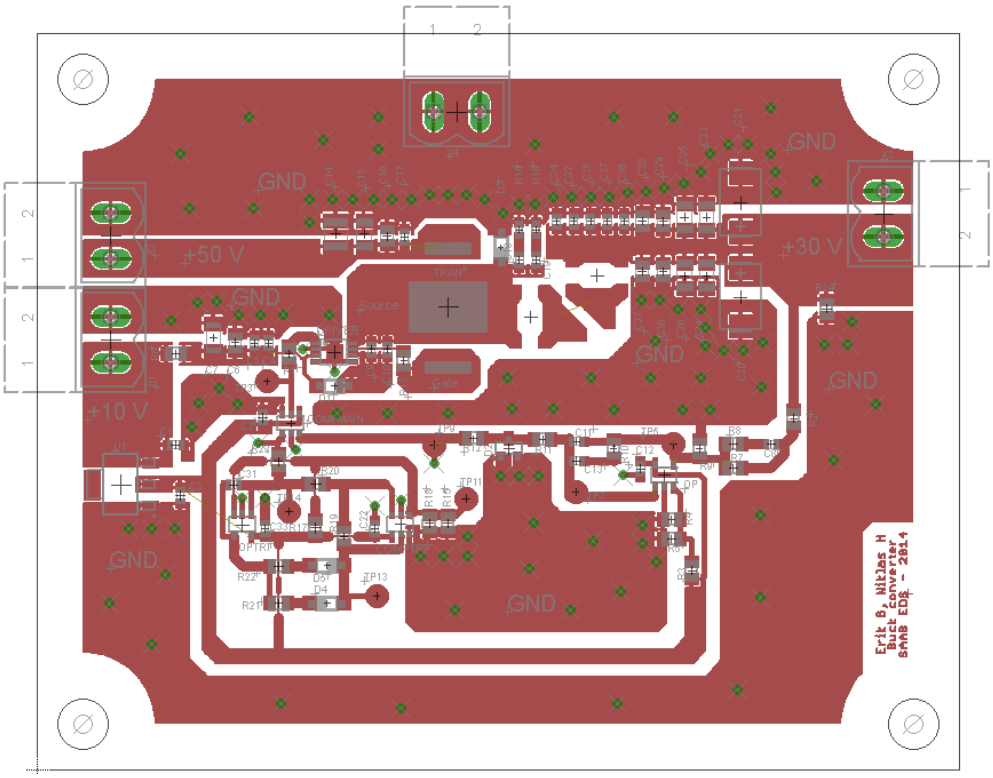

Figure 47. Layout of the top layer, Buck converter. The board is 100x80 mm.

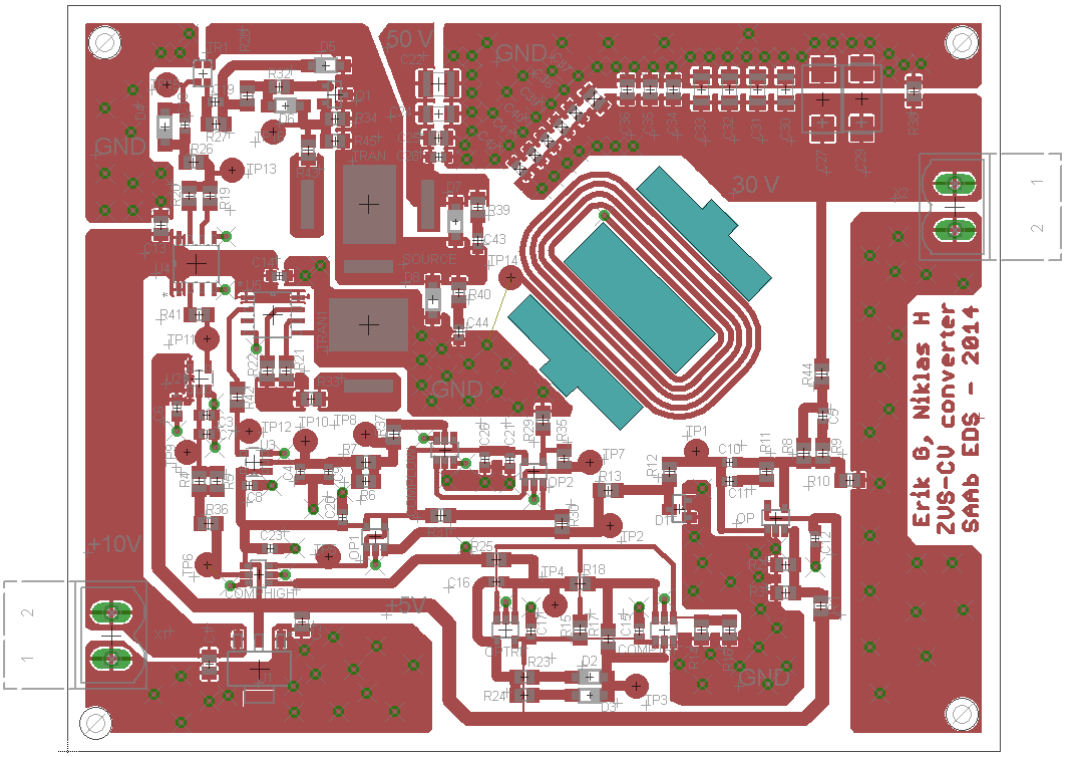

Figure 48. Layout of the top layer, ZVS-CV converter. The board is 100x80 mm.

C. Pictures of converters

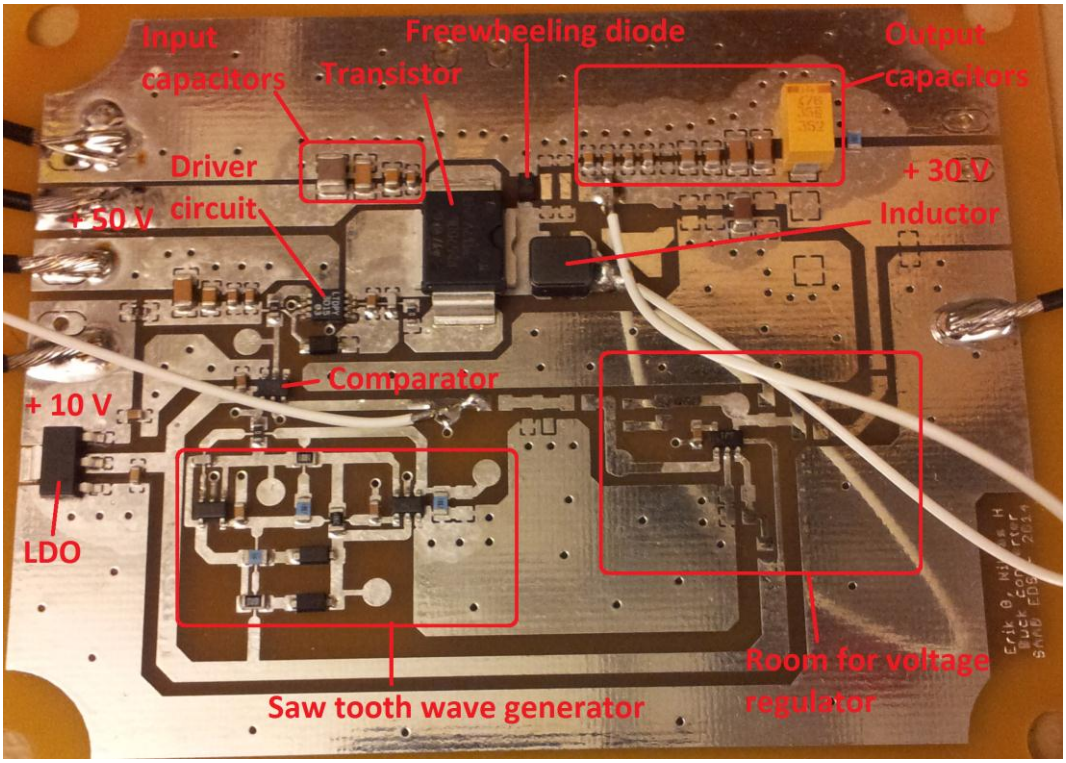

Figure 49. Buck converter.

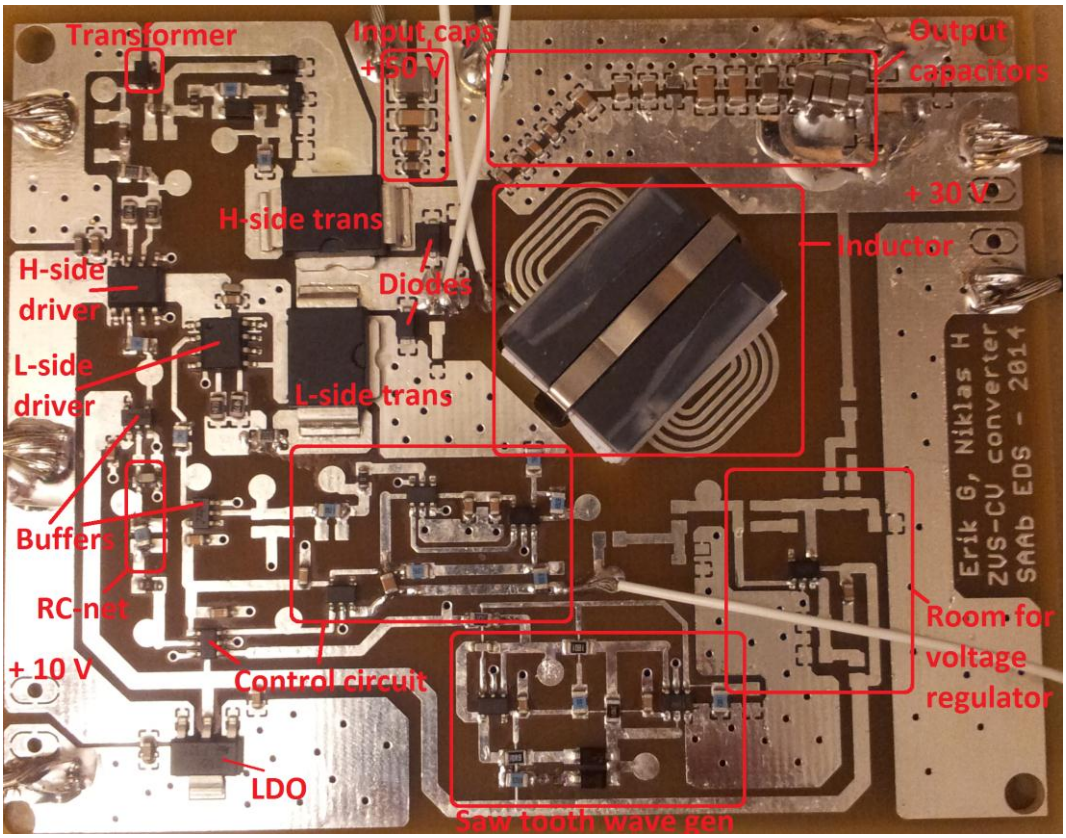

Figure 50. ZVS-CV converter.

D. Laboratory equipment

Table 7. Equipment used during measurements.

Type	Manufacturer	Model
Oscilloscope	Teledyne LeCroy	HDO6104
Current probe	Teledyne LeCroy	AP015
Voltage probes	Teledyne LeCroy	PP018
50 V supply	Delta Elektronika	SM7020-D
10 V supply, regulator output supply	Powerbox	PB3100
Electronic load	Powerbox	PB3310
Isolating transformer	Rätt Kraftförsörning	RDS500
Multimeters	Fluke	87-V true rms
Infrared camera	Fluke	TiR32