Thesis for The Degree of Licentiate of Engineering

Microwave characterisation of electrodes and field effect transistors based on graphene

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Abstract

The isolation of the two-dimensional material graphene, a single hexagonal sheet of carbon atoms, is believed to trigger a revolution in electronics. Theory predicts unprecedented carrier velocities in ideal graphene, from which ultrahigh speed graphene field effect transistors (GFETs) are envisioned.

In this thesis, the prospects of GFETs for microwave receivers are investigated with the emphasis on low noise amplifiers (LNAs). A microwave amplifier at 1 GHz with 10 dB small-signal gain and 6.4 dB noise figure was realised using a mechanically exfoliated graphene flake on a SiO_2 substrate. Comparable GFET performance was demonstrated with large-area graphene grown by chemical vapour deposition (CVD) on copper and transferred to SiO_2. From a device level noise characterisation, the CVD GFET minimum noise figure (F_{min}) in the frequency range 2-8 GHz was measured to be 2.5-5 dB and estimated by de-embedding parasitics to be 1-4 dB for the intrinsic device. However, the GFET noise is sensitive to impedance mismatch as the noise resistance is high. In addition, subharmonic resistive GFET mixers utilising the symmetry of electron and hole conduction in graphene were assessed. Conversion loss (CL) and noise figure were approximately equal and $\geq$20 dB and the input third order intercept point (IIP3) was $\leq$3.9 dBm at a local oscillator power of 2 dBm, less linear then fundamental resistive mixers.

Finally, the properties of graphene and metal-graphene contacts were investigated by parameter extraction based on measurements at both DC and microwave frequencies. Using a palladium based contact, a contact resistance as low as $< 100\ \Omega\mu$m was reached. An associated contact capacitance was extracted, for which a geometrical model was proposed. The implications of this capacitance on device performance is presumably negligible up to at least several hundred gigahertz. It is inferred, however, that the sheet resistance of graphene in this work must be reduced two orders of magnitude to improve performance of acoustic resonators when using graphene as an electrode.

Keywords: Graphene, CVD graphene, graphene electrodes, microwave FETs, microwave amplifiers, nanofabrication, noise measurements, noise modelling, small-signal FET modelling, subharmonic resistive mixers, FBARs.

List of publications

Appended papers

This thesis is based on the following papers:

[A] M. A. Andersson, A. Vorobiev, J. Sun, A. Yurgens, S. Gevorgian, and J. Stake, "Microwave characterization of Ti/Au graphene contacts", in *Applied Physics Letters*, vol. 103, no. 17, pp. 173111-173111-4, October 2013.

[B] M. Tanzid, M. A. Andersson, J. Sun, and J. Stake, "Microwave noise characterization of graphene field effect transistors", in *Applied Physics Letters*, vol. 104, no. 1, pp. 013502-013502-4, January 2014.

[C] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier", in *Electronics Letters*, vol. 48, no. 14, pp. 861-863, July 2012.

[D] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Resistive Graphene FET Subharmonic Mixers: Noise and Linearity Assessment", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4035-4042, December 2012.

Other papers and publications

The following papers and publications are not appended to the thesis, either due to contents overlapping of that of appended papers, or due to contents not related to the thesis.

[a] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Noise Figure Characterization of a Subharmonic Graphene FET mixer", in *IEEE MTT-S International Microwave Symposium Digest, IMS*, Montreal, Canada, 2012.

[b] M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Towards Practical Graphene Field Effect Transistors for Microwaves", in *Giga-Hertz Symposium*, Stockholm, Sweden, 2012.

[c] M. A. Andersson, A. Vorobiev, J. Sun, A. Yurgens, and J. Stake, "Towards Graphene Electrodes for High Performance Acoustic Resonators", in *37th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)*, Warnemünde, Germany, 2013.

Notations and abbreviations

Notations

C	Gate-drain noise correlation coefficient
C_c	Contact capacitance
C_g	Gate capacitance
C_{ds}	Drain-source capacitance
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{ox}	Gate oxide capacitance per area
C_{pg}	Gate pad capacitance
C_{pd}	Drain pad capacitance
C_Q	Quantum capacitance of graphene
Δf	Noise bandwidth
d_{m-g}	Metal to graphene separation
E	Energy
$\mathcal{E}$	Electric field
E_F	Fermi energy
E_g	Bandgap
ε	Dielectric permittivity
$\overline{e^2}$	Noise voltage
F	Noise figure
F_{min}	Minimum noise figure
f_{IF}	Intermediate frequency
f_{LO}	Local oscillator frequency
f_{max}	Maximum frequency of oscillation
f_{RF}	RF signal frequency
f_T	Cutoff frequency
Γ_{opt}	Optimum source reflection coefficient
Γ_s	Source reflection coefficient
G_T	Transducer power gain
g_{de}	Extrinsic output conductance
g_{di}	Intrinsic output conductance
g_{me}	Extrinsic transconductance
g_{mi}	Intrinsic transconductance
h_{21}	Short circuit current gain

h	Planck constant
$\hbar$	Reduced Planck constant
I_{ds}	Drain source current
I_g	Gate leakage current
$IIP3$	Third order intercept point
$\overline{i^2}$	Noise current
k_B	Boltzmann constant
L_a	Ohmic contact to channel access length
L_d	Drain inductance
L_g	Gate length / Gate inductance
L_s	Source inductance
l_t	Contact transfer length
m^* (m_0)	Carrier effective mass (electron rest mass)
μ_e (μ_h)	Electron (hole) mobility
μ_c	Chemical potential
n	Electron concentration
n_0	Residual carrier concentration
n_{imp}	Impurity concentration
n_{th}	Thermally generated carriers
P	Drain noise coefficient
p	Hole concentration
q	Electron charge
R	Gate noise coefficient
R_c	Contact resistance
R_D	Drain parasitic resistance
R_{ds}	Total drain to source resistance
R_G	Gate resistance
R_i	Intrinsic gate-source resistance
R_n	Noise resistance
R_{pd}	Drain pad resistance
R_{pg}	Gate pad resistance
R_S	Source parasitic resistance
R_{sh}	Sheet resistance
ρ	Electrical resistivity
ρ_c	Contact resistivity
σ	Electrical conductivity
σ_{min}	Conductivity at Dirac voltage
T_a	Ambient temperature
T_d	Drain noise temperature
T_g	Gate noise temperature
T_{min}	Minimum noise temperature
T_n	Equivalent noise temperature
U	Mason's unilateral gain
V_{Dirac}	Dirac voltage
V_{ds}	Drain source voltage
V_{gs}	Top gate source voltage
v_{drift}	Carrier drift velocity
v_F	Fermi velocity (10^8 cm/s)
v_{sat}	Carrier saturation velocity
W_g	Gate width
Y_s	Source admittance
Y_{opt}	Optimum source impedance

Abbreviations

2DEG	Two-dimensional electron gas
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
Ar	Argon
Al	Aluminium
Au	Gold
CG	Conversion gain
CL	Conversion loss
CNT	Carbon nanotube
CTLM	Circular TLM
Cu	Copper
CVD	Chemical vapour deposition
DOS	Density of states
FBAR	Film bulk acoustic wave resonator
FET	Field effect transistor
GaAs	Gallium arsenide
GaN	Gallium nitride
GFET	Graphene field effect transistor
GHz	10^9 Hz
GNR	Graphene nanoribbon
hBN	Hexagonal boron nitride
HEMT	High electron mobility transistor
IF	Intermediate frequency
IM3	Third order intermodulation distortion
InGaAs	Indium gallium arsenide
InP	Indium phosphide
kHz	10^3 Hz
LNA	Low noise amplifier
LO	Local oscillator
MESFET	Metal-semiconductor field effect transistor
MHz	10^6 Hz
MOSFET	Metal oxide semiconductor field effect transistor
mHEMT	Metamorphic HEMT
Ni	Nickel
NFA	Noise figure analyser
NW	Nanowire
Pd	Palladium
pHEMT	Pseudomorphic HEMT
Pt	Platinum
RF	Radio frequency
SEM	Scanning electron microscope
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
TLM	Transfer length method
THz	10^{12} Hz
Ti	Titanium
VCO	Voltage controlled oscillator

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Chapter 1

Introduction

Numerous applications use high frequency electromagnetic waves within the microwave (300 MHz−300 GHz) and terahertz (THz, loosely defined as 100 GHz−10 THz) frequency regions of the spectrum, and the number is continuously increasing. Wireless technology operating in the lower-GHz range is in many aspects a defining factor of life today, as an enabler of the rapidly increasing amounts of information and data exchanged in modern society [1]. In the THz regime, traditionally, niche applications in spectroscopy, earth remote sensing and radio astronomy were dominating [2]. More recently, however, interest and practical implementation of THz in fields closer to everyday life, including security and surveillance [3], medicine and disease diagnostics [4] and future high speed communication networks [5] have emerged. This requires compact, room temperature and low-cost sources able to bridge the so called THz gap, a part of the electromagnetic spectrum where output power is scarce. The challenge of realising such hardware has been approached going up in frequency from the electronics side by the use of diode multiplier chains [6] and down in frequency from the photonics side by quantum cascade lasers [7].

A key component from the electronics side is the microwave field effect transistor (FET), which is today used to feed power to inputs of multiplier chains and for intermediate frequency low noise amplifiers (LNAs) in THz receivers. The first microwave transistor operating in the GHz range was a GaAs metal-semiconductor FET (GaAs MESFET) [8]. Since, a rule-of-thumb in achieving higher frequencies has been to scale to as short transistor channels as possible and to use channel materials with as high carrier mobilities and saturation velocities as possible. A great breakthrough was the introduction of the GaAs high electron mobility transistor (GaAs HEMT) [9], utilising a 2DEG channel to separate the carriers from the impurity dopants. Now, the leading technology is the InP HEMT with maximum frequency of oscillation $f_{max} > 1$ THz and a record cutoff frequency $f_T = 688$ GHz, as can be seen in Fig. 1.1, which enable amplifier circuits with > 3 dB gain at 650 GHz [10]. Consequently, direct FET THz sources [6] and THz LNAs appear feasible [11].

However, the InP HEMT matures, reaching the scaling limits in terms of gate length and channel carrier mobility with 30 nm pure InAs channels. Furthermore, it is an expensive and comparatively low-yield technology. Consequently, the microwave device community is constantly scrutinising new con-

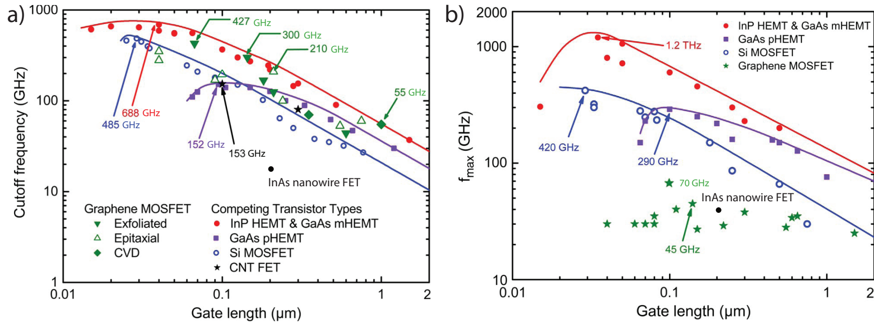

Fig. 1.1: State-of-the-art GaAs and InP HEMTs, Si CMOS and CNT FET technology against reported GFETs [13, 28–30]. De-embedded a) f_T and b) f_{max}.

cepts and new materials with high carrier velocities for FETs to reach further into the THz range. In this context, 1D semiconducting carbon nanotubes (CNTs) [12] and InAs nanowires (NWs) [13] have been explored. These materials are not yet encompassing expectations and not competitive with the established technologies in Fig. 1.1 in terms of high frequency performance.

In this thesis, the recently discovered 2D carbon material graphene [14] is studied for use in high frequency FETs. Graphene belongs to a group of 2D materials currently attracting significant attention due to their electrical and mechanical properties [15, 16]. Until recently, such planar, low-dimensional materials were thought to be thermodynamically unstable. This notion changed with the micromechanical cleavage of graphite into graphene in 2004, for which Andre Geim and Konstantin Novoselov were awarded the Nobel Prize in physics in 2010. It was followed by several other layered 3D lattices used to produce few layer crystals, including insulating hexagonal boron nitride (hBN) and semiconducting molybdenum disulfide (MoS_2) [17], which is an option for logic circuits. In addition, there have been experimental demonstrations of silicene (2D silicon), which in theory has similar electronic properties as graphene [18], and germanane [19] (2D germanium).

These 2D materials are considered promising for numerous applications. Graphene is researched to enhance the performance of photonics and optoelectronics [20], energy storage [21] and sensors [22] as well as an enabler for new applications via spintronics [23] and plasmonics [24]. In graphene, new possibilities are found through the combination of attributes in for example low weight and great mechanical strength for composites [25] and high electrical conductivity, bendability and transparency for touch screens, light emitting diode (LED) electrodes and bendable electronics [26, 27]. Graphene represents a candidate for the next level of high speed transistors [28] by intrinsically offering several times higher mobility compared to the best HEMT channels, especially for mass market devices intended for room temperature operation.

The reported state-of-the art high frequency GFET performance is included in Fig. 1.1. Clearly from Fig. 1.1a), graphene has an edge to CNTs and NWs in terms of high frequency performance, reaching a record intrinsic cutoff frequency f_T = 427 GHz [30]. Although the f_T data of GFETs reported so far is comparable even to some III-V HEMTs, the maximum frequency of

oscillation in Fig. 1.1b) is lagging behind, with a record value for intrinsic $f_{max} = 70$ GHz [29]. This is explained in part by the poor current saturation in GFETs, resulting from the absence of a bandgap in graphene. Still, the movement of carriers in GFET channels is greatly impeded by oxide substrates and gate oxides sandwiching graphene. This issue can be addressed by the use of hBN layers [31] to eventually exploit the full potential of graphene.

In addition to the high frequency gain performance of GFETs, represented by f_T and f_{max}, knowledge of the device noise level is important to realise LNAs. The LNA is a vital component in that it ultimately sets the sensitivity of a receiver chain. Similar requirements hold for a low noise FET compared to high frequency operation in that low carrier scattering is required, i.e. high mobility channel materials are required. In this respect, graphene intrinsically represents an interesting option to today's low noise technology [32].

However, the noise performance of GFETs at microwave frequencies has been missing in the literature, in contrast to studies of the low frequency $1/f$ noise in graphene [33]. This thesis presents the first complete noise parameter data and emphasises the importance of the FET minimum noise figure (F_{min}) together with f_T and f_{max}. Working towards practical graphene devices exhibiting gain to enable the noise measurements, a small-signal GFET amplifier made on a mechanically exfoliated graphene flake was demonstrated. The GFET process was adapted to the highly scalable and comparatively cheap graphene grown by chemical vapour deposition (CVD) [34]. A device level noise characterisation was performed for these CVD GFETs. The CVD process potentially offers a high degree of integration with Si CMOS for single-chip solutions, combining CMOS logic and graphene microwave circuitry [35]. These are persuasive benefits in potential large-volume THz products such as short range, high speed communication links operated above 100 GHz [5]. To complement the GFET LNA in a graphene receiver, the thesis also investigates the performance of subharmonic resistive GFET mixers. The mixers utilise the unique electron-hole conduction symmetry in graphene for subharmonic mixing in a single FET. Finally, graphene sheets and metal contacts to graphene are characterised at both DC and microwave frequencies, important for the use of graphene as electrodes in LEDs [27] and acoustic resonators [36].

1.1 Thesis outline

The thesis introduces graphene and the publications set in a wider context, via the structure outlined below. *Chapter 2* provides the relevant background on the theoretical electronic properties of graphene and practical limitations. *Chapter 3* describes the synthesis of graphene and the further processing steps into test structures and devices. In addition, it discusses the results of the material and ohmic contact characterisation. *Chapter 4* presents the background on microwave FET operation and the device status of GFETs for low noise amplifiers. *Chapter 5* presents the performance of a GFET amplifier and GFET mixers for microwave circuits. It also provides a discussion for graphene as a resonator electrode. *Chapter 6* draws summarising conclusions out of which future work directions are identified. *Chapter 7*, finally, includes a summary and describes the content of the papers upon which this thesis is based.

Chapter 2

Properties of graphene for high frequency devices

Fast microwave FETs are core building blocks i.e. in high speed communication networks. To realise such a device, the carrier transit time under the gate must be short. This necessitates a short gate length transistor and a channel material with highest possible carrier velocity. This chapter presents the theoretical potential and practical limitations of graphene in this context to understand the current performance and future improvements of GFETs.

2.1 Graphene band structure

Graphene consists of a single-layer of carbon atoms in a hexagonal lattice, connected via sp^2-hybridisation, shown in Fig. 2.1a). In graphene each atom has three neighbours, connected by strong covalent, in-plane σ-bonds. While these electrons are localised, defining the carbon-carbon binding distance of $a_{C-C} = 1.42$ Å, the remaining valence electrons are delocalised in out-of-plane covalent π-bonds as illustrated in Fig. 2.1b). The span of the latter orbitals limit the thickness of graphene to 0.34 nm. The σ-bonds constitute the mechanical strength of graphene, whereas the electrons in π-bonds account for its electrical conductivity. In principle, the π-electrons move in a plane outside the graphene lattice, allowing negligible collision rate and thus excellent carrier velocity in an applied electric field. In the literature, often *single-layer* graphene is clearly emphasised, to distinguish it from bilayer or few-layer graphene (> 2 layers), with different properties. Unless explicitly stated, in this thesis graphene refers to a single-layer material.

Understanding the unique electrical properties graphene starts with a knowledge of its energy dispersion (electronic band structure), i.e. the energy momentum relation for electrons and holes, a work which dates back to 1947 [37]. Using a nearest neighbour tight binding (NNTB) approximation of the honeycomb lattice, the dispersion of the π electrons [38] is expressed as

$$E(\mathbf{k}) = \pm\gamma\sqrt{1 + 4\cos\frac{\sqrt{3}a}{2}k_x \cos\frac{a}{2}k_y + 4\cos^2\frac{a}{2}k_y}, \tag{2.1}$$

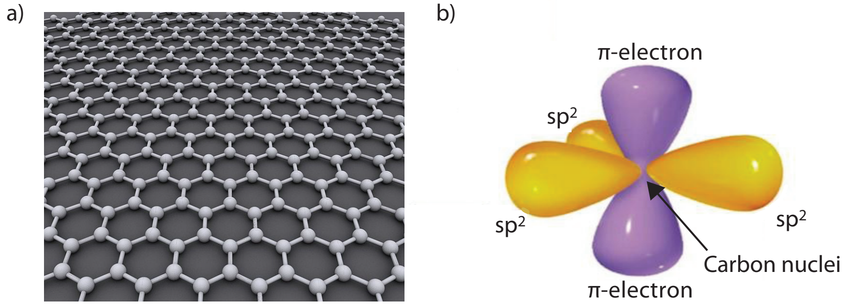

Fig. 2.1: a) Graphene honeycomb lattice. b) Visualisation of electron clouds in sp^2-hybridisation, localised in plane σ-bonds and out of plane delocalised π-electrons [39].

where $\gamma = 2.8$ eV is the nearest neighbour overlap energy and $a = \sqrt{3}a_{C-C} = 2.46$ Å. In Eq. 2.1, which is derived under the assumption of electron and hole symmetry, the plus and minus signs correspond to the conduction (π^*) and valence (π) bands, respectively. This model compares well with *ab initio* calculations within $\pm$ 1 eV of the intrinsic Fermi energy $E_F = 0$ eV, where the conduction and valence bands touch without bandgap, illustrated in Fig. 2.2.

The performance of graphene based electronic devices is governed mainly by the dispersion when $|E| < 0.4$ eV, the E_F range reachable by field- or impurity induced carriers (see further Section 2.2.1). This corresponds to the regions closest to the six K (K′) points of the first Brillouin zone, where the energy-momentum relation is further simplified to a cone (inset Fig. 2.2)

$$E(\mathbf{k}) = \pm\hbar v_F\sqrt{k_x^2 + k_y^2}. \tag{2.2}$$

In Eq. 2.2, $\hbar$ is Planck's constant and $v_F = 3\gamma a/2\hbar \simeq 10^8$ cm/s the Fermi velocity (upper limit of the carrier velocity) in graphene within the tight binding approximation. A linear dispersion indicates massless particles described by the *Dirac equation*, giving the names *Dirac points* where the conduction and valence bands meet. These massless particles, the so called *Dirac fermions*, represent the origin of the superior carrier mobilities expected in graphene.

2.2 Carrier transport in graphene

The high frequency performance of FETs depend on the carrier dynamics in the channel, quantified by the mobility and saturation velocity, i.e. the response of the carriers to an applied electric field. Graphene is compared to Si, III-V semiconductors and single-layer MoS_2 in Table 2.1. The intrinsic cut-off frequency, i.e. the high frequency limit of a material, can be directly related to these properties. In principle, for a *long gate length* $f_{T,int} \propto \mu/L_g^2$, whereas for a *short gate length* $f_{T,int} \propto v_{sat}/L_g$. In practice, the importance of v_{sat} gradually increases when scaling gate length. Clearly, graphene is an outstanding candidate to reach extremely high frequencies. In GFET fabrication, however, a substrate and a gate dielectric are required, leading to increased scattering of the out of plane electrons and degradation of the ideal values in graphene.

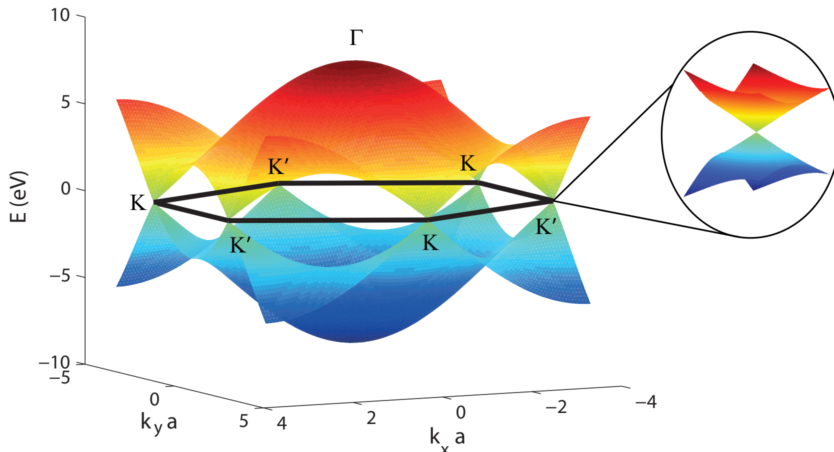

Fig. 2.2: Band structure in the tight binding approximation of graphene within the 1st Brillouin zone (Eq. 2.1). Inset shows the famous Dirac cone (Eq. 2.2).

Table 2.1: Effective mass, low-field mobility, saturation velocity and bandgap of low-doped semiconductors used for FETs. *Freestanding, $n \sim 10^{12}$ cm^{-2}.

	MoS_2	Si	GaN	GaAs	InAs	InSb	Graphene*
m_e^*/m_0	0.6	0.98	0.19	0.063	0.023	0.015	0
μ_e (cm^2/Vs)	400 [40]	1,400	1,600	8,000	33,000	88,000	200,000 [41]
μ_h (cm^2/Vs)	-	500	200	400	500	850	200,000
v_{sat} (10^7 cm/s)	0.3 [42]	1	1.1	1.5	3.5	5	$\sim 4-5$ [43]
E_g (eV)	1.8	1.12	3.4	1.43	0.36	0.18	0

Depending on the conditions, both ballistic [44] and diffusive [14,45] (Drude-Boltzmann) transport conditions have been reported in the literature. This is identified by the dependence of conductivity on carrier concentration, $\sigma(n)$, or equivalently on gate voltage, $\sigma(V_G)$, observed. In the diffusive limit the conductivity is given by $\sigma^{-1} = (nq\mu_C + \sigma_{min})^{-1} + \rho_s$ [31,46]. Here, μ_C models the mobility due to long-range Coulomb scattering and ρ_s the short range scatterers, i.e. lattice point defects. Further, σ_{min} is the residual conductivity due to remaining carriers when biasing for the Fermi level to lie at the Dirac point of the electronic spectrum. In samples with high impurity concentration, $\sigma \propto n$ at high carrier densities, with Coulomb scattering being the dominant mechanism [45]. On the other hand, in cleaner samples a sublinear $\sigma(n)$ is found, attributed to short range scattering [47]. Similarly, a sublinear $\sigma \propto \sqrt{n}$ was interpreted as ballistic transport in suspended graphene with a micrometre mean free path ($l = \mu\hbar\sqrt{\pi n}/q$) comparable to the sample dimensions [44].

2.2.1 Carrier concentrations

In single-layer graphene, the one-to-one relations between the carrier concentrations and the Fermi level position are given by

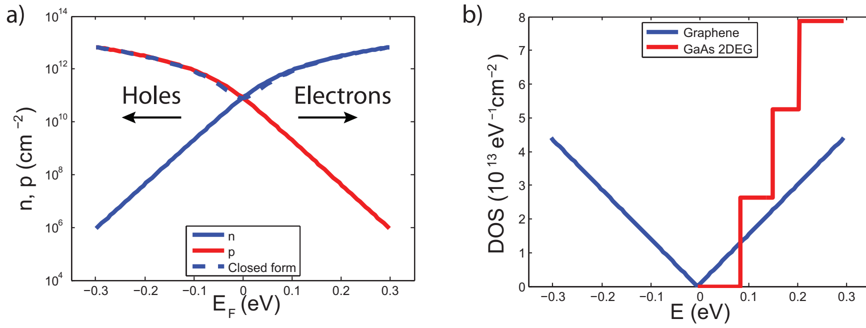

Fig. 2.3: a) Carrier concentrations versus E_F at RT. Solid lines from Eq. 2.3 and Eq. 2.4, while dashed line combines expressions of Eq. 2.7 and Eq. 2.8. b) DOS in graphene compared to AlGaAs/GaAs 2DEG with $n_s = 0.67 \cdot 10^{12}$ cm^{-2} [48].

$$n\left(E_F\right) = \int_0^\infty g(E) f(E - E_F) dE \tag{2.3}$$

for electrons and by

$$p\left(E_F\right) = \int_{-\infty}^0 g(E)(1 - f(E - E_F)) dE \tag{2.4}$$

for holes [38]. In principle, $E_F > 0$ and $E_F < 0$ correspond to a majority of electrons and holes respectively. The shift in Fermi level may originate from attraction of electrons or holes in graphene by the field effect [14], charge transfer from metal contacts [49, 50] or adsorbed molecules such as water molecules [22, 51]. Therein, the density of states (DOS) is given by

$$g(E) = \frac{g_s g_v |E|}{2\pi \left(\hbar v_F\right)^2}, \tag{2.5}$$

where $g_s = g_v = 2$ are the spin degeneracy and valley degeneracy (non-equivalency of the K and K′ points), respectively. Further, the Fermi-Dirac distribution function is defined as usual:

$$f(E_F) = \frac{1}{1 + e^{\frac{E - E_F}{k_B T}}}. \tag{2.6}$$

The integrals have simple analytical solutions given $E_F = 0$, corresponding to thermal carrier generation, given by

$$n_{th} = \frac{\pi}{6} \left(\frac{k_B T}{\hbar v_F}\right)^2 \tag{2.7}$$

and for the high carrier concentration case when $|E_F| \gg k_B T$ where

$$n = \frac{1}{\pi} \left(\frac{E_F}{\hbar v_F}\right)^2. \tag{2.8}$$

The carrier concentration versus Fermi level in graphene at room temperature, based on the exact and closed form expressions, and the DOS are plotted in Fig. 2.3. The carrier density can easily exceed that of a two-dimensional electron gas (2DEG) where $n_s \sim 10^{12}$ cm^{-2} [48]. In fact, $n = 1 \cdot 10^{13}$ cm^{-2} is easily attained at a voltage $V_g \lesssim 5$ V with the Al_2O_3 gate oxide in [Paper B, C, D], unless dielectric breakdown occurs first. Note that the term intrinsic graphene refers to completely filled valence band and empty conduction band, i.e. perfectly clean graphene at $T = 0$ K. Graphene at room temperature is considered extrinsic due to thermal carriers, even when $E_F = 0$.

2.2.2 Residual carrier concentration

For any graphene encountered experimentally, an additional parameter is required to explain the behaviour at the minimum conductivity point, i.e. the gate voltage which most closely corresponds to the Dirac point of the electronic spectrum. In particular, σ_{min} at room temperature exhibits a wider plateau [45] and a weaker temperature dependence (upon cooling) than expected solely from thermal generation [44]. These phenomena are linked to an inhomogeneous carrier concentration induced by impurities in the vicinity of the graphene sheet, in the substrate or at the interface, with concentration n_{imp} [47]. This electron-hole puddle landscape has been mapped by direct experiments [52]. Understandably, the residual carrier density n_0 is a highly substrate dependent property. It ranges from $10^{11} - 10^{12}$ cm^{-2} on SiO_2/Si samples [45] to $\sim 10^{10}$ cm^{-2} on hBN [31] to $\sim 10^8$ cm^{-2} in a current annealed, suspended sample [46]. For comparison, $n_{th} = 8 \cdot 10^{11}$ cm^{-2} at room temperature is masked on a SiO_2 substrate. As a rule of thumb, temperature dependence of σ_{min} is suppressed unless $k_BT > E_{puddle} = \hbar v_F \sqrt{\pi n_0}$.

2.2.3 Low-field mobility

At low electric fields, the carrier drift velocity is linear in field strength with the proportionality constant defined as the low-field mobility, $v_{drift} = \mu\mathcal{E}$. In the case of graphene, the conductivity mobility defined by $\mu = \frac{\sigma}{nq}$ [53] is often determined experimentally in a field-effect transistor configuration [14]. In this context, σ is attained from a 4-probe measurement of the resistance of a graphene patch with known length and width, $R = \rho\frac{l}{w}$ and $\sigma = 1/\rho$ (note that ρ in the 2D conductor case has units of $\Omega/\Box$). The carrier density is mapped to the gate voltage, V_g, via the gate capacitance, C_g, as $n = C_gV_g/q$. In samples limited by charged impurity scattering (such as on SiO_2) where $\sigma \propto n$ this yields a carrier density independent conductivity mobility. This justified the field effect transistor DC model proposed in [54], used for extraction of a single mobility value for each carrier type in devices under this condition.

$$R = 2R_c + R_{channel} = 2R_c + \frac{L_g}{W_g q\mu\sqrt{n_0^2 + \left(\frac{C_g(V_g - V_{Dirac}}{q}\right)^2}}, \tag{2.9}$$

In Eq. 2.9, R_c is the drain/source contact resistance and V_{Dirac} the gate voltage corresponding to the Fermi level being positioned at the Dirac point.

Another option is to use a Hall bar or van der Pauw structure in a transverse magnetic field. After measuring the resistivity (sheet resistance), the Hall coefficient R_H (proportional to the measured Hall voltage) provides the Hall mobility as $\mu_H = |R_H|/\rho$ and the carrier concentration as $n = 1/|R_H|q$ [53]. The sign corresponds to the carrier type, with $R_H < 0$ for electrons and $R_H > 0$ for holes. It is important to note the conductivity- and Hall mobilities may differ, as $\mu_H = r\mu$ with $1 < r < 2$, where r depends on the scattering mechanism involved [53]. In reporting Hall mobilities, often $r = 1$ is assumed.

The carrier scattering mechanisms recognised to limit the mobility of graphene are listed below starting from the fundamentals, moving on to limitations of the common SiO_2 substrates and finally its possible replacement.

- **Longitudinal acoustic phonons (LAP) [41,55]**: The theoretical upper bound for mobility is set by the LAP interaction, which contributes with the resistivity of $30\Omega/\square$ at room temperature independent of concentration [41]. While this results in a mobility $\mu \sim 200,000$ cm^2/Vs at a carrier concentration $n = 10^{12}$ cm^{-2}, it drops rapidly as $\mu \propto 1/n$.

- **Charged impurities (Coulomb) [45,47]**: For graphene on SiO_2 the phonon scattering is masked by typical impurity densities which limit the experimental mobility to $\sim 10,000$ cm^2/Vs [14,54].

- **Remote interfacial phonons (RIP) [41,56]**: Even in the extreme case of no charged impurities, the lowest RIP mode of SiO_2 (59 meV) would set an upper limit of 40,000 cm^2/Vs at room temperature [41]. Exchanging the SiO_2 substrate for a high-κ substrate screens the impurities, but at the expense of low energy surface optical phonons. This increases RIP scattering and results in a small improvement at 300 K [56].

- **Resonant scattering centres [57]**: Resonant scattering centres from from adsorbates and vacancies have been shown to play a role on high-κ substrates, on which they are shown to map to the carrier mean free path. The corresponding map on low-κ substrates is to impurity scattering [58].

- **Flexural phonons (FP) [59]**: Represents a dominant scattering mechanism in free standing graphene. Consists of static ripples introduced on rough substrate surfaces and frozen in when suspending the graphene.

In this context, hBN provides an alternative pathway with a number of valuable properties [31]. It has the same hexagonal lattice as graphene and a mismatch of only ~ 2 %, with an inert surface drastically reducing the attachment of impurities. As a result, one benefits from the higher RIP modes of hBN (>100 meV), while keeping the gating ability of SiO_2 ($\varepsilon_{hBN} \sim \varepsilon_{SiO_2}$) and without losing performance due to the weak impurity screening. At room temperature, graphene on hBN [31] may even show higher mobility than suspended graphene [59], since graphene conforms to the extremely smooth surface therefore limiting scattering on graphene ripples.

The temperature dependence on resistivity in a certain temperature interval is indicative of the dominant scattering mechanism as summarised in Table 2.2. In the high carrier concentration regime, or for dirty samples with high residual concentration, n is independent of T and thus the mobility has an inverse dependence compared to the resistivity.

Table 2.2: Temperature dependence of resistivity, ρ, as a result of important scattering mechanisms in graphene. E_0 is energy of the surface optical phonon mode.

Scattering mechanism	T interval	T dependence
Longitudinal acoustic phonons [55]	$T > 20$ K	$\rho \propto T$
Charged impurities (Coulomb) [41]	$\forall\, T$	None
Remote interfacial phonons [41]	$\forall\, T$	$\rho \propto \frac{1}{e^{E_0/k_B T} - 1}$
Flexural phonons [59]	$\forall\, T$	$\rho \propto T^2$

2.2.4 Saturation velocity

In high electric fields the linear transport relation is no longer valid, as the velocity reaches a maximum value. Instead, it can be approximated by

$$v_{drift} = \frac{\mu \mathcal{E}}{\left(1 + (\mu \mathcal{E}/v_{sat})^{\gamma}\right)^{1/\gamma}}, \tag{2.10}$$

where μ is the low-field mobility and v_{sat} is the saturated carrier velocity, ultimately bound by the Fermi velocity, v_F [60]. In graphene, the saturated velocity is eventually set by its optical phonon energy $\hbar\omega_{OP} = 160$ meV, while on SiO_2 it is deteriorated as a result of the substrate surface optical phonon mode with lower energy, $\hbar\omega_{OP} = 55$ meV [43, 61]. Furthermore, the maximum drift velocity is decreased at higher carrier concentration and higher temperature as a result of phonon occupation, quantified by the model

$$v_{sat} = \frac{2\omega_{OP}}{\pi\sqrt{\pi n}} \sqrt{1 - \frac{\omega_{OP}^2}{4\pi n v_F^2}} \frac{1}{N_{OP} + 1}, \tag{2.11}$$

where $N_{OP} = 1/(e^{\hbar\omega_{OP}/k_B T} - 1)$ is the phonon occupation. The resulting v_{sat} on SiO_2 is in the range $1 - 2 \cdot 10^7$ cm/s, which is comparable to epitaxial graphene on SiC having an intermediate $\hbar\omega_{OP} = 116$ meV [62], while twice as high velocities can be reached if the substrate limitation can be overcome.

2.3 Bandgap engineering

In GFETs, a bandgap in graphene is desirable for improved device performance. Two main routes are to induce it either by lateral confinement in a graphene nanoribbon (GNR) or by a perpendicular field in bilayer graphene.

In GNRs, theoretical studies suggest that the bandgap depends inversely on the width w, as $E_g = \alpha/w$ [63]. The proportionality, α [eV·nm], is influenced by the edges being of either the armchair, zigzag or mixed type. The general trend was first verified experimentally in ribbons prepared by electron beam lithographic patterning. Oxygen plasma etching of patterned, mechanically exfoliated graphene, is limited to $w > 15$ nm and $\alpha = 0.2$ eV·nm [64]. Subsequently, thermally exfoliated ribbons from graphite enabled $w < 10$ nm and $\alpha = 0.8$ eV·nm [65], with a record $E_g \sim 0.4$ eV and an I_{ON}/I_{OFF} ratio $\sim 10^6$ at room temperature. Mixed (zigzag and armchair) edges are suggested

to induce allowable states within the bandgap allowing tunneling currents and resulting in reduced on-off ratios [66].

However, the mobility in graphene severely degrades as a sizeable bandgap is opened. Hitherto, the highest mobility and bandgap combination reported at room temperature for a 20 nm GNR is 2000 cm^2/Vs and $E_g = 0.1$ eV. Although the sample was suspended and rigourously cleaned (annealed thermally and in high current) [67], this is considerably lower mobility than in large-area graphene under the same conditions. For a wider GNR, $w = 50$ nm, $\mu \sim 3000$ cm^2/Vs was reported on substrate [68], although no associated bandgap was presented. Consequently, atomic precision lithography is required for narrow ribbons, enabling simultaneous bandgap and high quality carrier transport. Nevertheless, the effective mass is theoretically predicted to depend linearly on bandgap in GNRs [69], with an inverse dependence of mobility on bandgap, $\mu \propto E_g^{-3/2}$. Conventional semiconductors (Si, III-Vs) also follows a fundamental inverse relationship, but GNRs till date exhibit comparatively lower mobilities at a certain bandgap [28]. The same trend is true for other low-dimensional materials such as MoS_2 presented in Table 2.1, which is comparable to Si in terms of bandgap and transport properties.

Another approach is the use of symmetry breaking in between the two layers of bilayer graphene [70]. This is achieved by introducing different amounts of carriers n_1 and n_2 ($n = n_1 + n_2$), chemically or electrically, from the top and bottom sides of the bilayer, respectively. Bilayer graphene on SiC with substrate induced carriers and varying amount of potassium (electron donor) on the non-substrate side [70], backgate voltage combined with ammonia (electron donor) [71] and double-gated FETs [72,73] have all been used to introduce a tunable bandgap. In the latter, both the carrier density and bandgap are tuned with the electric fields of the two gates, via their difference and average, respectively [72]. A gap up to 0.25 eV [72] and an on-off ratio ~ 100 at room temperature [73] was achieved using combined top- and backgates. Once more, though, the intrinsic mobility is severely degraded by a re-shaped bandstructure to $\sim 10,000$ cm^2/Vs at this bandgap [74]. Including impurity scattering on SiO_2 it reduces further to 1,000 cm^2/Vs, in line with [72].

2.4 Quantum capacitance

As a consequence of the vanishing DOS at $E = 0$ of the electronic spectrum in Fig. 2.3, the quantum capacitance in graphene [75] must be considered in devices with ultrathin gate dielectrics. In ideal, disorder free graphene

$$C_Q(E_F) = \frac{2q^2 k_B T}{\pi(\hbar v_F)^2} \ln\left(2 + 2\cosh\left(E_F/k_B T\right)\right). \tag{2.12}$$

In any sample with a residual carrier concentration $n_0 > 0$ the value of C_Q is increased compared to the ideal case as has been confirmed by experiment [76]. Since $C_Q \sim 2 - 10$ μF/cm^2 for typical n_0 presented in Fig. 3.6, and with reasonable oxide thicknesses $C_{ox} < 1$ μF/cm^2, the condition $C_Q \gg C_{ox}$ is generally fulfilled and serves as a good approximation in this thesis. However, the quantum capacitance defines the ultimate achievable gate capacitance as it is in series with the gate oxide capacitance, $C_g = \frac{C_{ox}C_Q}{C_{ox}+C_Q} \to C_Q$ if $C_{ox} \gg C_Q$.

Chapter 3

Fabrication, material and contact characterisation

This chapter describes the fabrication procedures of test structures and GFETs based on exfoliated and CVD graphene. In addition, the characterisation of graphene sheets and ohmic contacts to graphene are presented.

3.1 Graphene synthesis

Alternatives for both industry or research scale production of graphene have been developed; mainly mechanical exfoliation, chemical vapour deposition (CVD) and sublimation of silicon carbide (SiC), enabling wafer-scale fabrication of graphene based devices [29, 77] and circuits [35, 78].

3.1.1 Mechanical exfoliation

The Scotch tape method, i.e. peeling of single-layers from bulk graphite, was first demonstrated systematically in 2004 [14]. It still produces the highest mobility and lowest defect density (see Fig. 3.2) graphene. The highest experimental mobilities both in suspended samples at near room temperature (T = 240 K) of ~100,000 cm^2/Vs [44] and at 5 K of 1,000,000 cm^2/Vs [59] as well as on substrate (hexagonal boron nitride) at near room temperature (T = 230 K) of ~100,000 cm^2/Vs [79] and at 4 K of ~140,000 cm^2/Vs [79] are made using mechanically exfoliated material at a carrier density of 10^{11} cm^{-2}. Translated to mean free path this means micrometre scale ballistic transport. The GFETs in [Paper C] and [Paper D] are fabricated on exfoliated graphene. A flake made by mechanical exfoliation of good size is shown in Fig. 3.1a).

3.1.2 Chemical vapour deposition

A promising scalable technique is growth of graphene on Cu foils. As opposed to Ni, where carbon is dissolved at high temperature and segregates to the surface during cooling, the carbon solubility in Cu is extremely low [80]. Instead, CVD graphene formed on Cu is a surface catalysed reaction self-limited to a single-layer [81]. Once a layer of carbon covers the surface the catalytic effect

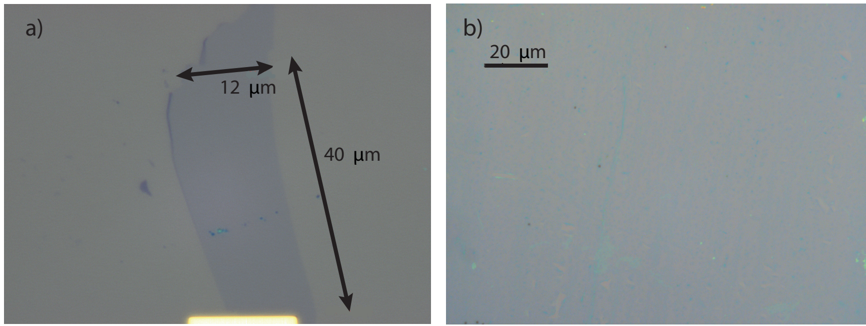

Fig. 3.1: Optical identification of single-layer graphene on SiO_2/Si substrate produced by a) exfoliation and b) CVD growth on Cu catalyst in a virtually hole-free [82].

ceases, which makes the growth insensitive to timing and cooling conditions. Indeed, $> 95\%$ of areas grown can be single-layer [34].

Graphene in [Paper A] and [Paper B] was grown on Cu foil (50 μm thickness, 99.995+ % purity) by CVD based on the recipe in [82] by Sun et. al. The foils are cleaned in acetone and isopropanol to remove organic contaminants and acetic acid to remove native oxides, respectively. Before growth, the copper is annealed 5 min in 20 sccm H_2 and 1,000 sccm Ar at $1,000\,°C$. In addition to further etching away any remaining oxide it increases the grain size of the Cu, improving the quality of the grown graphene. Finally, the carbon precursor gas, 30 sccm methane (CH_4) diluted to 5% in Ar, is introduced. After 5 min, while maintaining a temperature of $1,000\,°C$, the carbon containing gas is turned off and the catalyst cooled to room temperature.

Nucleation of many graphene grains with different orientation occur in parallel, which coalesce into a continuous film even across Cu grain boundaries [80]. A typical grain size in our process is $\lesssim 10$ μm [83], in between which grain boundaries act as line defects increasing scattering and deteriorating mobility [84]. In the literature, efforts have been undertaken to decrease nucleation density and grow large single-domain graphene crystals. Optimising the pre-annealing to reduce nucleation with remaining native oxide, growth pressure and CH_4/H_2 gas ratio, grains up to 5 mm were reported [83], although the growth time was 48 h. The mobility on SiO_2 in the absence of grain boundaries reached $\sim 15,000$ cm^2/Vs at room temperature. A recent report even passivated the surface with external O_2 to grow centimetre grains [85].

A main advantage of the CVD graphene process is the flexibility in that it can be transferred from the catalyst to an (in principle) arbitrary host substrate making graphene in turn compatible with CMOS processing [35]. Commonly, a temporary PMMA resist film is spun onto the graphene surface, while the copper is etched away [80, 82] or separated by the H_2 bubbling process [86] used in this thesis. Utilising a semi-rigid plastic frame reduces the occurrences of wrinkles and holes, while facilitating convenient handling. Resulting transferred graphene to SiO_2/Si is presented in Fig. 3.1b). A transfer related issue of CVD graphene is the extrinsic reduction of mobility from water trapped at the graphene substrate interface during the process [87]. The water molecules act as acceptors resulting in sometimes strongly p-type films [88].

3.1.3 Sublimation of SiC

Epitaxial graphene can be grown by sublimation of Si from an SiC surface at high temperature. A main advantage is the direct growth on an insulating substrate, without the need for a possibly defect inducing transfer process.

Growth on the Si-face is relatively easy to control, both monolayer and Bernal stacked bilayer are feasible [89]. First attempts in vacuum atmosphere and $T \sim 1200\,°\mathrm{C}$ resulted in small flakes across a rough sample surface. Later it was found that the presence of an inert gas, typically 1 atm Ar, limits the Si desorption rate and allows an increased growth temperature to 2000 °C. The different growth kinetics results in a smoother surface covered by uniform domains over large areas [89]. Room temperature mobility values of Si-face epitaxial graphene are limited by low energy phonons to below $1,000$ cm^2/Vs at an electron concentration of $\sim 10^{13}$ cm^{-2} [90]. This can be enhanced by hydrogen intercalation to $3,000$ cm^2/Vs [91], which effectively transforms the graphene monolayer and buffer layer into bilayer graphene [92]. In addition, it reduces the electron transfer from SiC, resulting in p-type films.

Growth on the C-face, on the other hand, stacks of decoupled monolayers are formed and the synthesis of single-layer graphene is more challenging. Still, C-face epitaxial graphene displays an order of magnitude higher mobility at room temperature $\sim 20,000$ cm^2/Vs [93] than the Si-face, as a result of a different interface structure, proving its potential for high frequency electronics.

3.1.4 Identification of single-layer graphene

Starting from the pioneering work [14], the identification of single-layer graphene flakes for research has relied mostly on the contrast of bare areas of SiO_2/Si substrates to areas covered by graphene [94]. Mathematically, the contrast is defined as $C = {}^{(I(n_{air})-I(n_{graphene}))}/_{I(n_{air})}$, where $I(n)$ is the reflected light intensity. Using an appropriate combination of light wavelength and oxide thickness the contrast is maximised. For example, in white light illumination, oxide thicknesses of 90 nm or 300 nm are recommended [94].

On the other hand, for quality control or verification of single-layer graphene on arbitrary substrates with lower contrast, the distinct signature in the Raman spectrum is useful [95, 96]. In Raman spectroscopy, incoming photons from a monochromatic laser light are inelastically scattered and the intensity versus outgoing photon wavelength is measured (after filtering out the Rayleigh scattered light). The result is generally presented as the Raman inverse wavelength (equivalently energy) shift, i.e. $1/\lambda_{in} - 1/\lambda_{out}$. Independent of the number of layers, the presence of sp^2 hybridised carbon is found in the G peak at ~ 1590 cm^{-1}, while single-layer graphene presents a symmetric 2D peak at ~ 2650 cm^{-1} fitted by a single Lorentzian [95], see Fig. 3.2. Bilayer is clearly distinguishable, since the splitting of the π/π^* bands give additional transitions which necessitates four Lorentzians. In addition, the defect induced D peak at ~ 1350 cm^{-1} results from structural disorder in the graphene sheet. As can be seen in Fig. 3.2a), the D peak was not resolved on exfoliated graphene, while the CVD graphene in Fig. 3.2b) has an $I_D/I_G \sim 0.3$. Both samples exhibit $I_{2D}/I_G \sim 2$, which together with a FWHM of the 2D peak ~ 30 cm^{-1} [34] are reasonable for high quality graphene. The exact positions of the peaks depend on laser wavelength [96], in Fig. 3.2 $\lambda = 638$ nm (red).

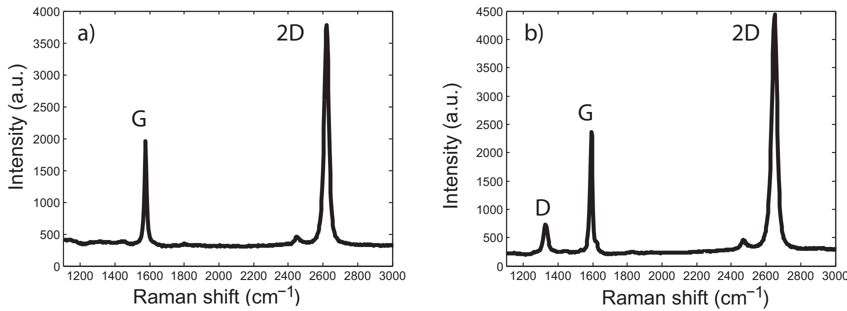

Fig. 3.2: Raman spectra of representative single-layer graphene used in this thesis where a) exfoliated flake with a 2D peak FWHM $\sim$ 30 cm^{-1} and b) CVD graphene grown on Cu foil with a 2D peak FWHM $\sim$ 34 cm^{-1}.

3.2 Device fabrication

After synthesising and transferring the graphene to the intended host substrate, an electron beam (e-beam) lithography based process is used to fabricate test structures and GFETs. The general steps are illustrated in Fig. 3.3 on a SiO_2 (thermal)/Si substrate. Ohmic contacts (1 nm Ti/ 15 nm Pd/ 100 nm Au) are evaporated and lifted-off using a bilayer resist stack consisting of ZEP 520A and MMA EL10. Thin Ti is used as adhesion layer, while the contact properties is determined by Pd. Annealing in Ar gas at $T = 200 - 230\,°\mathrm{C}$ cleans the graphene channel region from resist residue [97] before oxide formation and can possibly decrease contact resistance [87,98]. Gate oxide is formed by stepwise natural oxidation of thin layers (1-2 nm) of evaporated Al on a hotplate, a principle used for seed layer formation of atomic layer deposition (ALD) oxides on inert graphene [54]. A typical low-leakage GFET gate oxide used in this work has a thickness $\sim$ 10 nm. A negative resist (ma-N 2405) is used to pattern mesas, the oxide is wet etched in hydrochloric acid (HCl) and the graphene dry etched in a mild O_2-plasma. Gate fingers are patterned and a metal stack of 10 nm Ti / 300 nm Au evaporated and lifted-off. Finally, clamping probing pads overlapping the ohmic contact metal are formed on the SiO_2 surface. Devices on flake and CVD graphene are shown in Fig. 3.4.

3.3 Material and contact DC characterisation

The GFET microwave performance is directly related to the achievable contact resistance and mobility. Curve fitting using the model of [99], allows the extraction of contact resistance, mobility and residual carrier concentration (sample cleanliness) in a manner similar to Eq. 2.9, once the gate capacitance is known. To gain further insight into the contact properties, i.e. the resistance value approached at high gate voltage, the transfer length method (TLM) is required [53]. In addition, Hall measurements on van der Pauw structures provide an immediate way to extract the mobility and carrier concentration in a film. This is important to understand the potential of graphene electrodes.

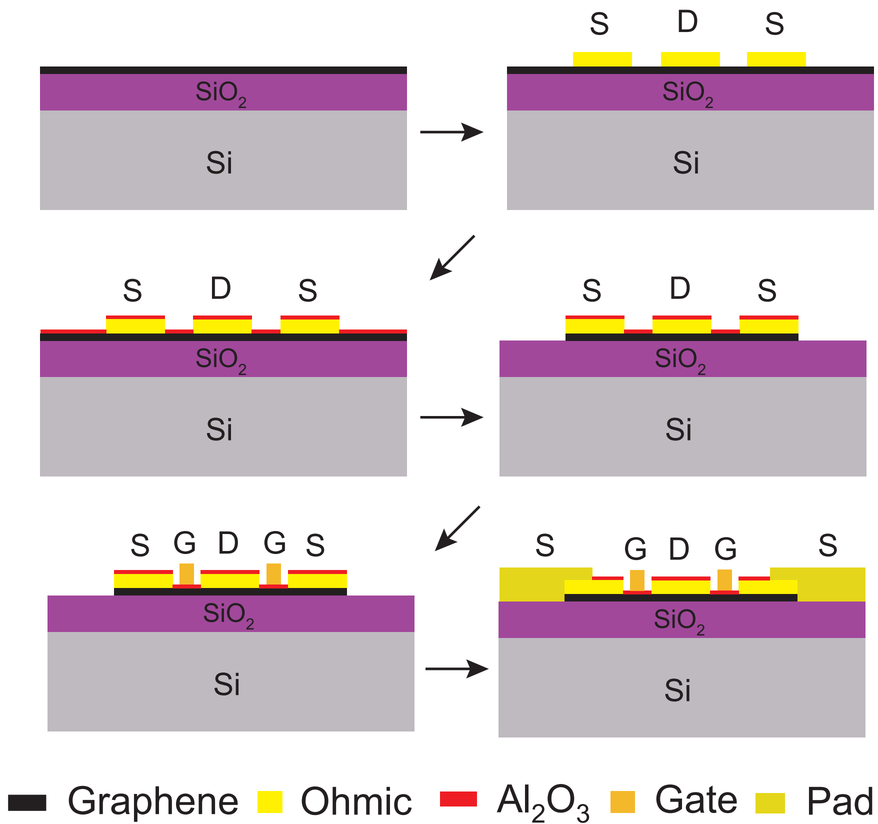

Fig. 3.3: Schematics of the fabrication steps for a two-finger GFET.

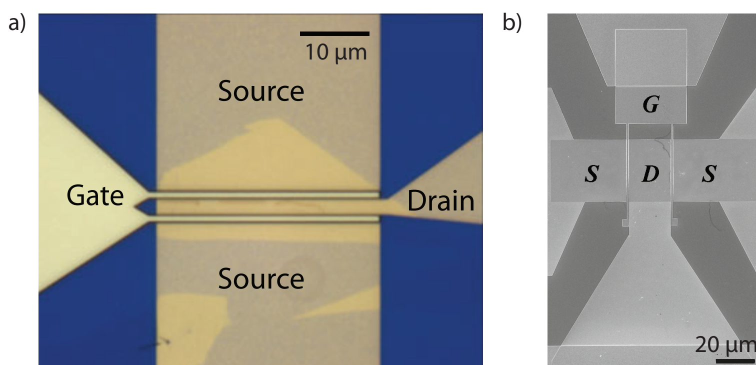

Fig. 3.4: Finalised GFETs with $L_g = 1$ μm and $W_g = 2 \times 30$ μm. a) Optical image of GFET on a clearly visible flake [Paper C]. b) SEM image of CVD GFET with a discernible wrinkle [Paper B].

3.3.1 Ohmic contacts and TLM measurements

To realise high performance FETs it is important to fabricate high quality ohmic contacts and low sheet resistance graphene. For instance, the parasitic source and drain resistances in a symmetric FET layout are equal and may be expressed as $R_S = R_D = (R_c W + R_{sh} L_a)/W_g$, i.e. the knowledge of both metal-graphene interface resistance ($R_c W$) and sheet resistance (R_{sh}) are necessary. Achieving a good ohmic contact to graphene has been the subject of extensive study and the mechanisms are still under debate.

- For pristine graphene, contacts with higher work function difference to graphene show better performance, i.e. Pd/Pt/Ni ($\sim$ 100-300 $\Omega\mu$m [100–102]) compared to Ti ($\sim$ 1 k$\Omega\mu$m [50, 103]), as a result of charge transfer from the metal into the graphene [104]. This trend is reproduced in this thesis (see Fig. 3.5), an indication of a metal-graphene interface clean from polymer residues. In this work it is possibly a result of well-developed e-beam resist compared to photolithographic processing where sacrificial layers [105] or ozone cleaning are required [106].

- A high carrier concentration in pristine graphene provides a comparatively lower ohmic contact resistance, an inherent property of epitaxial graphene [101]. The same explanation is proposed for the state-of-the-art Pd based contacts in [Paper B], $R_c W = 80$ $\Omega\mu$m on CVD graphene. Unfortunately, also the channel is affected with suppressed gating capability, where a selective doping of graphene is desired to produce a device structure similar to cap layers in HEMTs [48].

- Contacts to defected graphene by O_2 ashing of resist show negligible work function dependence and consistently low $R_c W$ [107]. In fact, controllably defected graphene under the contact is suggested to reduce the contact resistance due to enhanced carrier injection from metal at graphene edges. This has been realised by lithographic patterning [108] and metal-catalysed etching [102], reaching $R_c W < 100$ $\Omega\mu$m.

Circular TLM (CTLM) structures are used in [Paper A] to study Ti contacts to graphene, see Fig. 3.5a). This structure circumvents the problem of edge effects and current crowding [53, 109]. The sheet resistance of the graphene within the ring, $R_{sh,ring}$, and the contact resistance, R_c, are obtained from the slope and intercept at zero gap, respectively. The total resistance is

$$R_{tot} = \frac{R_{sh,ring}}{2\pi a} \left[s + 2l_x \right] \times \frac{a}{s} \ln \left(\frac{b}{a} \right), \tag{3.1}$$

where the dimensional quantities are defined in the inset of Fig. 3.5a). The mentioned charge transfer in between metal and graphene can make the sheet resistance under the contact significantly different from within the ring. As a result, the extraction of contact transfer length l_t requires additional measurements, i.e. $l_t \neq l_x$. A new method using microwave measurements on the same CTLM structures is proposed in [Paper A].

With Pd based contacts, accurate determination of a small $R_c W$ with a large R_{sh} and an inhomogeneous material becomes a delicate task [105]. A small error in the slope can give even negative values. Consequently, the TLM

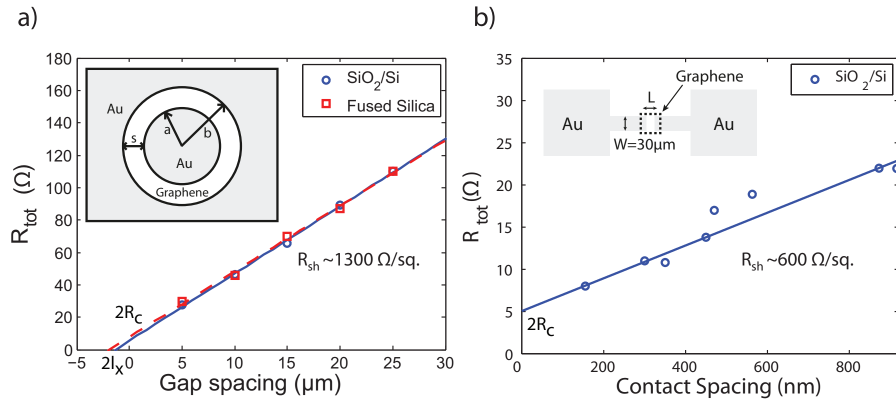

Fig. 3.5: Transfer length method (TLM) results on SiO_2/Si substrates for a) Ti based contact with $R_cW = 900\ \Omega\mu$m [Paper A] and b) Pd based contact with $R_cW = 80\ \Omega\mu$m [Paper B]. The insets illustrate the TLM structure layout used in each case.

layout was changed as shown in the inset of Fig. 3.5b) to have smaller R_{tot}. The contact spacings were measured with SEM. Further, the small gaps mimics the access region of a FET more closely. The smaller sheet resistance of these structures is attributed to a more homogenous graphene over smaller areas. The total resistance versus contact spacing is given as $R_{tot} = 2R_c + R_{sh}L/W$.

The contact resistances act to degrade the extrinsic transconductance, g_{me}, and the extrinsic output conductance, g_{de}, measured at the GFET terminals as compared to the intrinsic ones in Eq. 4.3 and Eq. 4.4. The gain capabilities of a device from a high mobility material with large intrinsic transconductance can thus be severely impaired by high contact resistances. Mathematically, this is expressed in the form [110]

$$g_{mi} = \frac{g_m^0}{(1 - (R_S + R_D)g_{de}(1 + R_S g_m^0))} \tag{3.2}$$

and

$$g_{di} = \frac{g_d^0}{(1 - R_S g_{me}(1 + (R_S + R_D)g_d^0))}, \tag{3.3}$$

where $g_m^0 = \frac{g_{me}}{1 - R_S g_{me}}$ and $g_d^0 = \frac{g_{de}}{1-(R_S+R_D)g_{de}}$, respectively.

3.3.2 Graphene sheets and gated IV-curves

Typical top gated transfer characteristics of GFETs fabricated in this thesis from exfoliated and CVD graphene, on SiO_2 with Al_2O_3 gate oxide, are presented in Fig. 3.6a). Also shown are model fits to extract a concentration independent mobility. A summarising plot of mobilities versus residual carrier concentrations extracted are given in Fig. 3.6b). Mobility values up to 8,000 cm^2/Vs in exfoliated graphene sandwiched between SiO_2 and Al_2O_3 has been demonstrated by ALD deposition techniques [54]. In comparison to the exfoliated sample the CVD device suffers from lower mobility, higher residual

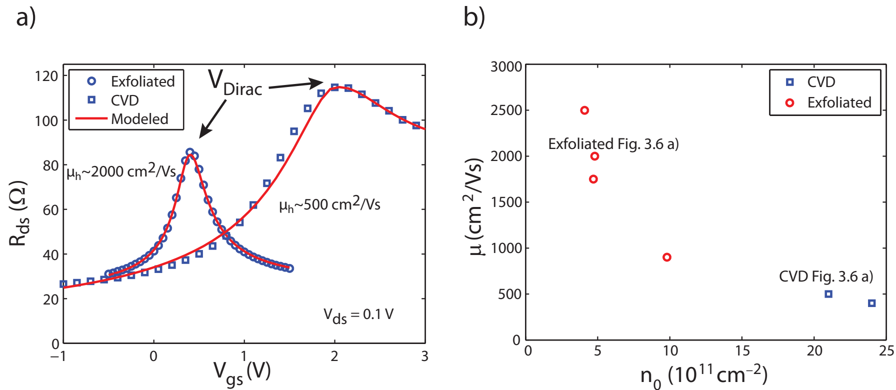

Fig. 3.6: a) Transfer characteristics of CVD [Paper B] and exfoliated GFETs on SiO_2 ($W_g = 60\ \mu$m, $L_g = 1\ \mu$m). b) Extracted mobility and residual concentrations.

carrier density and larger Dirac voltage offset V_{Dirac} (the devices have similar gate capacitance). Using the classification of [45] the exfoliated sample is considered "clean" (low n_{imp}), while the CVD sample is "dirty" (high n_{imp}). The p-type channels of ungated devices indicates wet transfer processing with water to be the difference, suggesting a post-transfer anneal in vacuum is necessary [87], although [86] indicates otherwise. Literature is ambiguous, even suggesting annealing to have a deteriorating effect for graphene on SiO_2 [31]. A drawback as discussed above is that a lower carrier concentration increases contact resistance, exemplified by exfoliated GFETs in this work typically exhibiting $R_cW = 400 - 600\ \Omega\mu m$. The range of mobility values and carrier concentrations of transferred, ungated CVD films on SiO_2 (fused silica glass) were in essence confirmed by Hall measurements to reside in the range $p \sim 10^{13}\ cm^{-2}$ and $\mu \sim 300\ cm^2/Vs$ ($r = 1$). Effectively taking average over a larger area explains the lower mobility in the Hall measurement.

Furthermore, the transfer characteristics of the CVD sample manifest a strong asymmetry in between electron and hole branches, also displayed in GFETs from exfoliated graphene (mainly seen in [Paper C, D]). This phenomena is explained by an extra pn-junction resistance for one carrier type [50]. For the clean exfoliated samples it results from charge transfer from the contact to the graphene underneath the contact. In this work, high work function Pd results in p-type graphene and the extra resistance is formed when the channel is n-type (positive gate voltage). As a result of the low DOS in graphene, the charge transfer region extends into the channel and may dominate conductance to produce unipolar devices in the case of short gate lengths ($L_g < 150$ nm) [111]. In the CVD sample the effect is enhanced by the p-type channel.

3.4 Microwave characterisation of contacts

Owing to its gapless nature, the metal-graphene contact is similar to a *metal-metal* rather than a metal-semiconductor interface. As a consequence, it is implied that no energy barrier exists at the interface [50]. A barrier associated

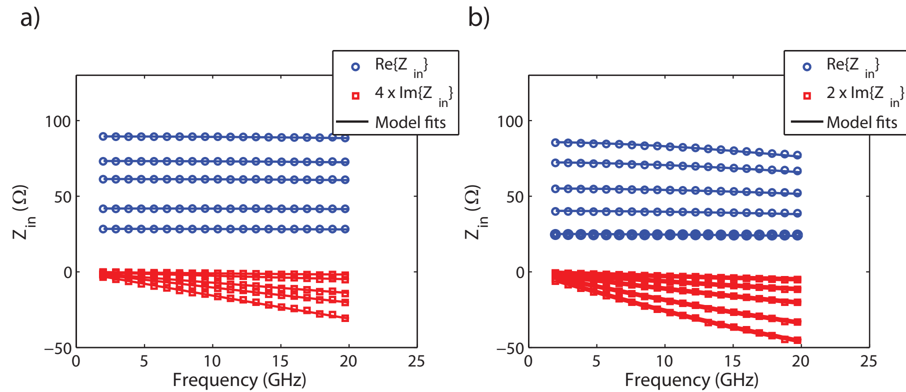

Fig. 3.7: Real part of input impedance (CTLM structure gap 5 − 25 μm from bottom to top) and imaginary part of input impedance (CTLM structure gap $5-25$ μm from top to bottom) of CTLM structures on a) fused silica glass and b) SiO_2/Si.

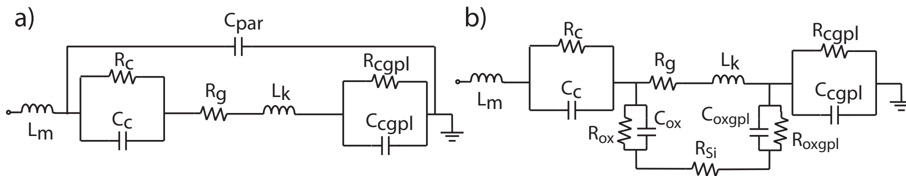

Fig. 3.8: Equivalent circuits for CTLM structures on a) fused silica and b) SiO_2/Si.

capacitance, as has been considered for standard ohmic contacts [112], is thus ruled out. Still, a contact capacitance for metal-graphene contacts has been reported [113, 114], interpreted to stem from resist residues at the interface.

In [Paper A], a clean interface was obtained by the e-beam patterned CTLM structures in the inset of Fig. 3.5a). The high quality interface is evidenced by the low contact resistance for the Ti/Au contacts [103]. Contacting using a standard ground-signal-ground (GSG) probe, S_{11} is measured in the frequency range 2-20 GHz for structures on both fused silica and SiO_2/Si substrates. The resulting input impedances are shown in Fig. 3.7a) and b), respectively, together with the fits using the equivalent circuits of Fig. 3.8a) and b). Details on the determination of the equivalent circuit elements are given below.

3.4.1 Extraction of contact capacitance

The pad-to-pad capacitance (C_{par}) in the fused silica case is calculated using methods of moments in ADS momentum. However, the conductive Si surface (modelled by R_{Si}) and lossy oxide (described by C_{ox} and R_{ox}) required us to measure identical dummy structures of the same layout without graphene.

The graphene conductance is modelled by an intraband scattering process. This is characterised by the chemical potential (μ_c) and a phenomenological scattering time (τ). The former is equivalent to Fermi level or carrier concentration, while the latter incorporates the mobility into the model [115] as

$$\sigma_{gr} = -j\frac{q^2 k_B T}{\pi\hbar^2(\omega - j/2\tau)}\left[\frac{\mu_c}{k_B T} + 2\ln\left(1 + e^{-\frac{\mu_c}{k_B T}}\right)\right] = \frac{k(\mu_c)}{j(\omega - j/2\tau)}. \quad (3.4)$$

Finally, to model the contact a parallel RC-combination is used. Here, R_c is set (close) to its DC value and C_c is modeled by a parallel plate capacitance

$$C_c = \frac{\varepsilon_0 \times A_c}{d_{m-g}} \approx \frac{\varepsilon_0 \times 2\pi a l_t}{d_{m-g}}. \quad (3.5)$$

The quantities in Eq. 3.5 are defined as follows:

- d_{m-g} is an effective metal to graphene separation, where the spacing is assumed to have the permittivity of vacuum $\varepsilon = \varepsilon_0$.
- A_c is the active contact area defined by the transfer length $l_t = \sqrt{\rho_c/R_{sh}}$ for edge current transfer from contact metal into graphene [53] and the CTLM radius a in Fig. 3.5a). The active contact area defines in turn the contact resistivity calculated as $\rho_c = A_c \times R_c = 2\pi a l_t \times R_c$.

The corresponding ground plane contact quantities are related to the centre contact counterparts via $R_{cgpl} \simeq a/b \times R_c < R_c$ and $C_{cgpl} \simeq b/a \times C_c > C_c$. In the above, $l_t \ll a, b$ is assumed, where a and b are the dimensional quantities of the CTLM structures shown in Fig. 3.5a).

The contact parameters are found via an optimisation in:

- The contact capacitance C_c via the parameters l_t and d_{m-g}.
- The graphene sheet impedance $Z_g = R_g + j\omega L_k = Z_{gr}/2\pi \ln(b/a)$ via τ and μ_c. Here, the graphene sheet impedance is $Z_{gr} = (\sigma_{gr})^{-1} = [2\tau k(\mu_c)]^{-1} + j\omega/k(\mu_c) = R_{sh} + j\omega L_{sh}$.

In [Paper A], $\mu_c \simeq 0$ is assumed and thus the sheet inductance $L_{sh} = 1/k(\mu_c)$ is set, while τ acts as the remaining optimisation variable to fix the sheet resistance R_{sh}. This was motivated by the extracted residual carrier concentration, which was estimated from a back gated transfer characteristics on the SiO_2/Si sample to be $n_0 \simeq 4 \cdot 10^{11}$ cm^{-2}. This resulted in $|E_F| \sim 0.1$ of the ungated film, which is in reasonable agreement with the literature on the graphene growth and transfer processes used [82,86]. Subsequent Hall measurements on fused silica and strontium titanate (STO) and the CVD GFETs fabricated for [Paper B], however, indicated a wider process related distribution of carrier concentrations in the range $p = 10^{12} - 10^{13}$ cm^{-2}. For completeness, additional simulations with corresponding $\mu_c = 0.1 - 0.3$ eV were performed for the fused silica data, which yield slightly decreased C_c values (within 20%) as a result of reduced kinetic inductance in $L_{sh} = 1/k(\mu_c)$.

In Table 3.1, a summary of the extracted contact parameters are given. The generated transfer lengths from microwave measurement compare well with literature [73]. Although the binding distance of Ti on graphene is predicted from theory to be 2Å $< d_{m-g}$ [49], the flatness of a graphene sheet is limited to a large extent by the underlying substrate roughness [31, 59]. This makes the extracted values for metal-graphene separation reasonable.

Table 3.1: Extracted Ti/Au contact parameters from microwave measurements for graphene on fused silica. Similar values apply to the SiO_2/Si case [Paper A].

l_t	C_c	ρ_c	d_{m-g}
90−270 nm	0.4−1.6 μF/cm^2	$0.6 - 3 \cdot 10^{-6}$ Ωcm^2	0.7−2.1 nm

In conclusion, the contact capacitance is estimated to be negligible if the operation frequency $f < f_c = (2\pi R_c C_c)^{-1} \simeq 100$ GHz, in contrast to previous reports [113, 114]. This is clearly satisfied for the GFETs reported in this thesis. Its significance decreases further with the smaller contact resistivity found for Pd based contacts to graphene.

3.4.2 Drude model for graphene sheets

To further verify the extraction accuracy, a Drude model was considered for the frequency dependence of the graphene sheet impedance [116],

$$Z_{gr} = \left(\frac{\sigma_0}{1 + j\omega\tau}\right)^{-1} = \frac{1}{\sigma_0} + j\frac{\omega\tau}{\sigma_0} = \frac{1}{q\mu n} + j\frac{hf}{q^2 v_F}\sqrt{\frac{\pi}{n}}. \tag{3.6}$$

In Eq. 3.6, h is Planck constant, v_F is the Fermi velocity in graphene, q is the electron charge and f is the frequency. This model confirmed the range of contact capacitance values in [Paper A]. Using Eq. 3.6 allows the separation of carrier concentration and mobility, compared to only the product in the form of sheet resistance. This mitigates the issue of choosing μ_c in Eq. 3.4 from an independent measurement. However, the carrier type (electron or hole) still requires to be determined i.e. by a Hall measurement.

Chapter 4

Microwave characterisation of GFETs

A device level characterisation of gain and noise is necessary to benchmark the performance of GFETs for microwave receivers. This chapter deals primarily with the details of GFET noise parameter measurements and modelling.

4.1 Graphene for microwave FETs

As part of their seminal paper in 2004 [14], Novoselov and Geim demonstrated the field-effect in graphene, i.e. the ability to alter its conductivity capacitively using a perpendicular electric field via a *gate* electrode. In this way, the resistance of a well-defined part of a graphene sheet forming a *transistor channel* between the *drain* and *source* electrodes can be varied. This enables field-effect transistors [117] based on graphene channels [118]. Especially, the properties of graphene are suitable to realise extremely fast FETs. Microwave transistors used for amplification of analog signals are benchmarked in terms of their gain and noise performance. This requires knowledge of the device S-parameter matrix and noise parameters versus DC bias. Both depend on the impedance levels presented to the device [119], as exemplified below.

4.1.1 High frequency FET figure-of-merits

The high frequency performance of microwave FETs are benchmarked via the cutoff frequency (f_T) and the maximum frequency of oscillation (f_{max}) which can be calculated from measured S-parameters [48]. The cutoff frequency is found when the short-circuit current gain ($|h_{21}|$) equals unity, where

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}. \tag{4.1}$$

Correspondingly, the maximum frequency of oscillation occurs when the unilateral power gain (Mason's gain, U [120]) is unity, where

$$U = \frac{|S_{12}-S_{21}|^2}{det(\mathbf{I}-\mathbf{SS}^*)}. \tag{4.2}$$

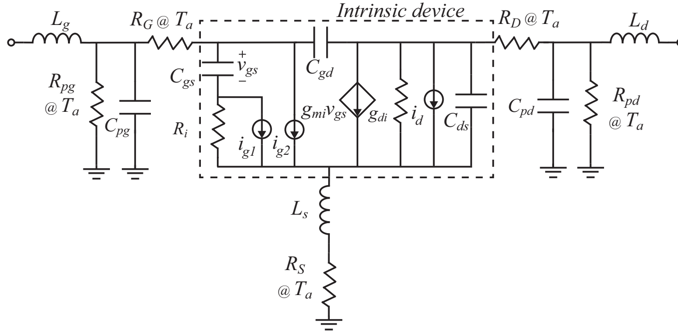

Fig. 4.1: Equivalent FET small signal circuit. Included are the noise currents in the Pospieszalski (i_{g1}) [121] and PRC (i_{g2}) [122] models of the GFET in [Paper B].

Insights into important device aspects for high frequency operation can be inferred from the small-signal equivalent circuit of a FET as shown in Fig. 4.1

$$f_T = \frac{g_{mi}}{2\pi} \frac{1}{(C_{gs} + C_{gd})(1 + g_{di}(R_D + R_S)) + C_{gd}g_{mi}(R_D + R_S) + C_{pg}} \tag{4.3}$$

and (excluding pad capacitances and inductances from the analysis)

$$f_{max} = \frac{g_{mi}}{2\pi(C_{gs} + C_{gd})} \frac{1}{2\sqrt{g_{di}(R_i + R_S + R_G) + g_{mi}R_G \frac{C_{gd}}{C_{gs}+C_{gd}}}}. \tag{4.4}$$

A high carrier mobility directly reflects on a large g_{mi}, which is the change in drain current with gate voltage, $g_{mi} = dI_{dsi}/dV_{gsi}$. Inspection of Eq. 4.3 and Eq. 4.4, further, reveals the importance of minimising the parasitic resistances R_S, R_D and R_G of source, drain and gate, respectively. The source and drain resistances constitute transition resistance from metal to graphene and access resistance. They are technology specific and discussed in more detail in Section 3.3.1. The gate resistance, on the other hand, is simply the geometrical resistance of a metal stack after accounting for small-signal operating conditions, $R_G = R_{G,DC}/3 = \rho_G \frac{W_g}{3L_g h_g}$ [48], where L_g (W_g) is the gate length (width) and ρ_G the resistivity of the gate metallisation. Similar to mature FET technologies, it can be decreased even for short gate lengths by the use of mushroom gates [48] (not required at $L_g = 1$ μm in [Paper B,C]).

The value of f_{max} is the highest frequency a transistor can provide power gain under idealised conditions. Typically, however, values of f_T and f_{max} should be several times higher compared to the intended application frequency for the device to exhibit gain at practical impedance levels. The actual gain of an amplifier is the so called transducer power gain, which at a certain bias point and from the S-parameter matrix at a certain frequency is given by

$$G_T = \frac{P_{load}}{P_{source}} = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{in}\Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}. \tag{4.5}$$

In Eq. 4.5, Γ_{in} is the reflection coefficient looking into the device input, while Γ_s and Γ_L are the reflection coefficients looking from the device towards the source and load, respectively. A device with $|S_{21}| > 1$ is an important requirement to fabricate an amplifier. With the starting point of $|S_{21}|^2$, the amplifier gain is further enhanced by designing input and output impedance matching networks, quantified by source- and load reflection coefficients, Γ_s and Γ_L, respectively [119]. The matching networks are implemented either by distributed transmission lines or by lumped inductors and capacitors as is the case in [Paper C]. Ideally, the matching networks should be lossless.

4.1.2 State-of-the-art GFET benchmark

From Fig. 1.1, the intrinsic cutoff frequencies ($f_{T,int} = \frac{g_{mi}}{2\pi(C_{gs}+C_{Cgd})}$) of GFETs compare well with III-V HEMTs, while the f_{max} values are not as impressive. Optimising R_G can improve the f_T/f_{max} ratio [29], but the lack of bandgap gives large g_{di} due to poor current saturation. Further, the comparison in Table 4.1 displays a large deviation in as-measured (extrinsic) and de-embedded (in the case of GFET the same as intrinsic) values. This is explained by narrow devices resulting in a high ratio of parasitic gate pad capacitance to intrinsic gate capacitance $C_{pg}/(C_{gs} + C_{gd})$ for short gate length devices. This is especially true for flakes on high resistive Si substrates, which yield higher pad capacitance compared to semi-insulating III-V substrates. Extracting a large value from a small one makes the de-embedding error prone. The highest extrinsic f_T of 55 GHz ($f_{T,int} = 72$ GHz) is thus realised on an insulating glass substrate [123]. In addition, for GFETs, R_S and R_D are often de-embedded in a questionable way using separate open and short structures without graphene (TLM measurements necessary, see Section 3.3.1). This is since standard cold FET measurements [124] are not possible on a GFET as it has no distinct off state. In fact, the contact resistances are not removed for the de-embedded f_T's of III-V HEMTs, but considered as a parasitic delay [125]. For GFETs in general, in particular with small gate width, this contribution can be prominent to boost the intrinsic f_T's in Fig. 1.1 [126], bringing another factor of uncertainty into the comparison to other technologies.

The transistors fabricated in this thesis are designed to operate with small-signal power gain ($S_{21} > 1$) in the frequency region 1-10 GHz. Consequently, a gate length $L_g = 1$ μm was chosen to achieve efficient gate modulation of the drain current and thus a higher transconductance. However, this means the gate capacitance will be large. As such, the devices have $f_T = 10.5$ GHz and $f_{max} = 13$ GHz [Paper B] and $f_T = 5$ GHz and $f_{max} = 7$ GHz [Paper C] from measured S-parameters with intrinsic values in the same range.

4.2 Noise performance of GFETs

The noise figure (F) is used to quantify the noise performance of microwave FETs. It is defined as the degradation in signal-to-noise ratio from the input to the output of the device and must be low to design a sensitive receiver. The noise figure relates to the equivalent noise temperature (T_n) referred to the device input as $F = 1 + T_n/T_0$ [127], where $T_0 = 290$ K. The FET noise figure depends on the source admittance presented to device [127] according to

Table 4.1: Extrinsic versus intrinsic f_T and f_{max} (in GHz) of state-of-the-art GFETs. Given are also the transistor channel length and width.

	$f_{T,ext}$	$f_{T,int}$	$f_{max,ext}$	$f_{max,int}$	L_g	W_g
Exfoliated [111]	2.4	300	-	-	144 nm	< 10 μm
CVD [77]	9	300	-	17	40 nm	20 μm
Epitaxial [29]	41	110	38	70	100 nm	7 μm

$$F(Y_s) = F_{min} + \frac{R_n}{G_s} \cdot |Y_s - Y_{opt}|^2, \tag{4.6}$$

where F_{min} is the minimum achievable noise figure used for benchmark [48]. Further, Y_{opt} is the optimum admittance for which F_{min} is realised and the noise resistance, R_n, describes sensitivity in F to mismatch when $Y_s \neq Y_{opt}$. Empirically, it was noted early on that at a fundamental level the design of a low noise FET parallels that of high f_T/f_{max} device [128], specifically $F_{min} = 1 + kf/f_T\sqrt{(R_S + R_G)g_{mi}}$ where k is a fitting factor. In other words, high mobility and saturation velocity is a pre-requisite for a low noise FET.

The most important sources of noise in microwave FETs are thermal noise from the resistive part of the channel and parasitic resistances and high-field diffusion noise from the velocity saturated part of the channel [127]. As such, the minimum noise figure displays typically an optimum value at low drain current and decreases at cryogenic temperatures if scattering is decreased. In the presence of a significant DC gate leakage current, the shot noise has to be considered as well, $\overline{i_{gs}^2} = 2qI_g\Delta f$. In this thesis, the Al_2O_3 gate oxide provides devices with $I_g < 1$ nA, a negligible level with the current GFET noise performance. In certain applications, such as oscillators, $1/f$ noise with corner frequency of ~ 100 kHz in graphene [33], is also of importance.

4.2.1 Noise modelling of FETs

From a noise modelling point of view one considers the intrinsic FET as a two-port, described by gate (input) and drain (output) noise sources. These are inserted in the intrinsic part of a standard small-signal circuit of a FET, as shown within the dashed rectangle in Fig. 4.1 for the two models considered, namely PRC [122] and Pospieszalski [121].

- The PRC model has three model coefficients, namely P for the drain noise current i_d and R for the gate noise current i_g, which are correlated with purely imaginary correlation coefficient C. The feedback capacitance C_{gd} is neglected in the analysis. This is a reasonable assumption since $\overline{i_{d,C_{gd}}^2} = \overline{i_d^2}\left(1 + \left(\frac{f}{f_0}\right)^2\right) \approx \overline{i_d^2}$, where $f_0 = g_{di}/2\pi C_{gd}$ [129].
- In the Pospieszalski model, equivalent temperatures are assigned to all dissipative elements in the intrinsic FET, i.e. T_g of R_i for the gate noise and T_d of R_{ds} for the drain noise. It is essentially equal to the PRC model provided $C = \sqrt{R/P}$, which was noted at an early stage [121].

Table 4.2: Definition of the FET noise currents shown in Fig. 4.1.

	$\overline{i_g^2}$	$\overline{i_d^2}$	C
Pospieszalski	$4k_B\Delta f T_g/R_i$	$4k_B\Delta f T_d g_{di}$	-
PRC	$4k_B T_a \omega^2 C_{gs}^2 R\Delta f/g_{mi}$	$4k_B T_a g_{mi} P\Delta f$	$j\frac{Im(\overline{i_g \cdot i_d^*})}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}}$

The relations between model parameters and noise currents are given in Table 4.2. The parasitic resistances contribute thermal noise at the ambient temperature, $\overline{e^2} = 4k_B T_a R\Delta f$, in both models. The two models provide slightly different information on the noise performance of a certain device. The Pospieszalski model is more "practical" while the PRC model is more geared towards physics and early work by van der Ziel on FET noise [130, 131].

4.2.2 Device level noise characterisation

The determination of all four noise parameters is done by measuring noise figure for different source impedances (diverse Γ_s) and making a least-square fit to Eq. 4.6. On-wafer measurements were performed with a commercial NP5 test set, an electronic tuner and the cold source method. The DUT noise temperature (T_n) is determined from the output noise power (P_{out}) by

$$T_n(\Gamma_s) = \frac{P_{out}(\Gamma_s)}{k_B G_{DUT}(\Gamma_s)\Delta f} - T_{in}, \tag{4.7}$$

where T_{in} equal to room temperature for all Γ_s is assumed. A network analyser determines independently the tuner states, receiver reflection coefficient and DUT S-parameters which yields G_{DUT}. The receiver noise parameters are established in a calibration step [132], which makes it possible to find P_{out}.

The noise parameters for a 2×30 μm device with $L_g = 1$ μm at $I_{ds} = 370$ mA/mm are shown in Fig. 4.2 in the range 2-8 GHz. The noise resistance decreases from $\sim 300\Omega$ at 2 GHz to $\sim 200\Omega$ at 8 GHz [Paper B]. As a result of the high R_n, the $NF_{50\Omega} \sim 8-9$ dB is large. The fundamental conditions on measured noise parameters derived from correlation of noise sources in a FET, $|Cor| < 1$ and $\mathrm{Re}(Cor) > 0$ [121], are shown to be satisfied in Fig. 4.3a).

Knowledge of all four noise parameters allows for a systematic, direct extraction of the model parameters in Section 4.2.1, once the small-signal circuit elements are known. These are found according to the following procedures.

- The pad capacitances, resistances and inductances are extracted from separate open and short structures excluding the graphene channel in a manner similar to standard cold FET measurements [133].
- The series resistances are determined from TLM measurements, described in Section 3.3.1, to be $R_S = R_D = 135$ $\Omega\mu$m.
- DC end-to-end measurements [48] yields a gate resistance of 54 Ω/mm.
- The parasitics are subsequently de-embedded [124] and closed form expressions for the intrinsic component values used [134].

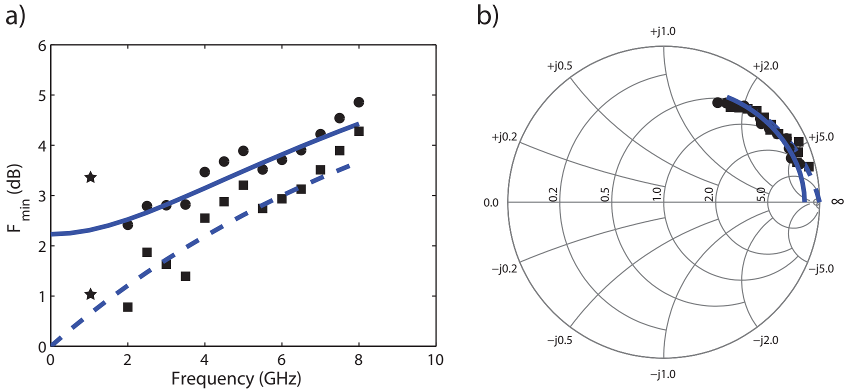

Fig. 4.2: a) Measured (•) and intrinsic (■) F_{min} of a 2×30 μm device at $I_{ds} = 370$ mA/mm [Paper B]. Values from [Paper C] given by ($\star$). b) Measured (•) and intrinsic (■) optimum source reflection coefficient (Γ_{opt}) with model lines [Paper B].

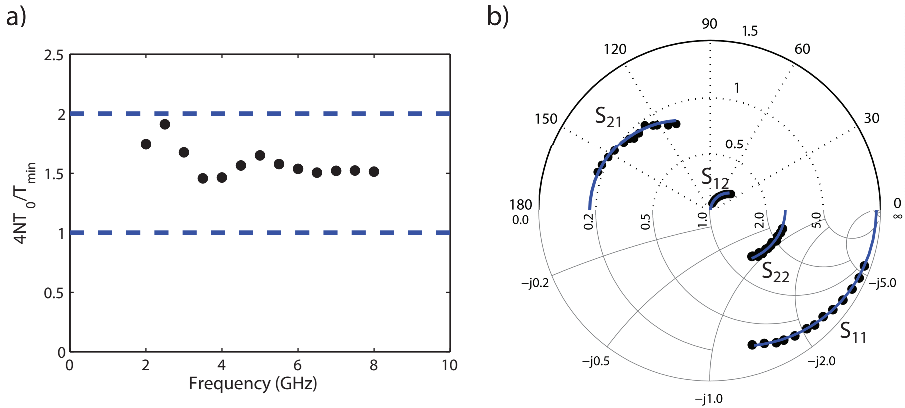

Fig. 4.3: a) The measured noise parameters fulfils $1 < 4NT_0/T_{min} < 2$ [121]. b) Measured (symbols) and modelled (solid line) S-parameters of the GFET [Paper B].

Lastly, a post-optimisation of the S-parameter fit is performed, with the final result shown in Fig. 4.3b). The subsequent main steps in the noise model extraction and adequate references are listed below.

- Determine the chain noise correlation matrix at each frequency of the device from the measured noise parameters according to (11) in [135].
- De-embed the noise contribution of the parasitics using the admittance matrices derived from the circuit in Fig. 4.1 to find the intrinsic noise correlation matrix of the subcircuit within dashed rectangle [136].
- Extract the noise model parameters from the intrinsic noise correlation matrix at each frequency point [137]. The result is shown in Fig. 4.4.

For comparison, the values of T_g and T_d in the Pospieszalski model were found by least-square optimisation to closed form expressions for the intrinsic

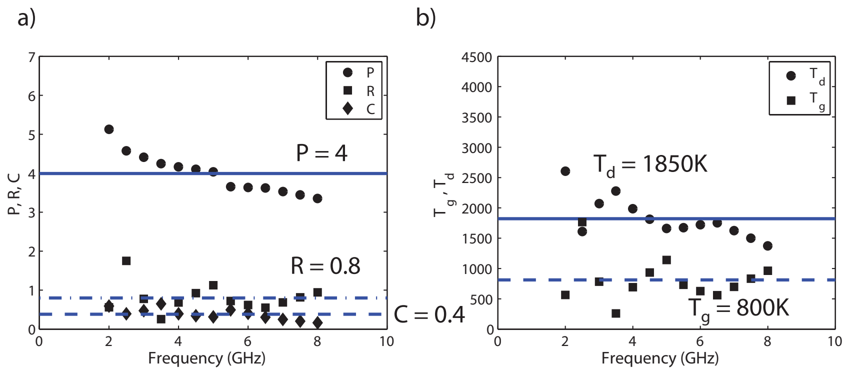

Fig. 4.4: a) Extracted P (●), R (■) and C (◆) coefficients of PRC model versus frequency. b) Extracted T_g (●) and T_d (■) of Pospieszalski model versus frequency. Lines and labels show mean values over all frequency points.

noise parameters following [121], after the inclusion of C_{gd}. The resulting values, $T_g = 700$ K and $T_d = 1950$ K, are close to the mean values from the direct extraction (which neglects C_{gd}) shown as lines in Fig. 4.4. The resulting model curves are shown on top of the measurement points in Fig. 4.2. A main limiting factor of the GFET are the pad resistances, resulting from the lossy substrate. Currently, noise figures less than 1 dB up to 2 GHz and below 3 dB up to 8 GHz appear quite feasible with the intrinsic device performance. For comparison, InP HEMTs provide room temperature $F_{min} < 1$ dB up to ~ 90 GHz [138], as can be seen from the extensive comparison in Fig. 4.5.

4.2.3 Graphene in the context of FET noise

Substraction of the gate noise from the drain noise (reflected in a high C) is one reason behind the outstanding low noise performance of HEMTs, where $C > 0.9$ [129]. In the GFET, however, the C-factor is considerably lower. This indicates an inferior gate control over the channel despite the high aspect ratio L_g/d_{G-ch}, where d_{G-Ch} is the gate to channel distance. This pinpoints again the lack of high quality gate stacks for GFETs. Similarly, $T_g > T_a$ is extracted, possibly a consequence of device self-heating due to the high current density resulting in hot carriers in the channel. Pospieszalski clearly highlights the importance of "quality-of-pinch-off" for low noise performance [139], specifically minimising $T_{min} \propto \sqrt{I_{ds}}/g_m$. The GFET does not pinch and the bias dependence remains an open issue. In [Paper B], the gate bias is for highest gain, e.g. 11 dB associated gain at Γ_{opt} at 2 GHz, to measure the noise most accurately. However, optimum noise most likely occurs at lower drain current densities. A deeper understanding of the relation of noise processes and transport on a microscopic level remains.

Finally, the benefit of cooling on mobility and noise levels is supposedly small with the high impurity densities at the graphene/SiO_2 interface (see Section 3.3.2). In combination with small grains, this limits the mobility in the current CVD GFETs to $\lesssim 1,000$ cm^2/Vs at room temperature. As a consequence of the low mobility, regardless of the high average field in the

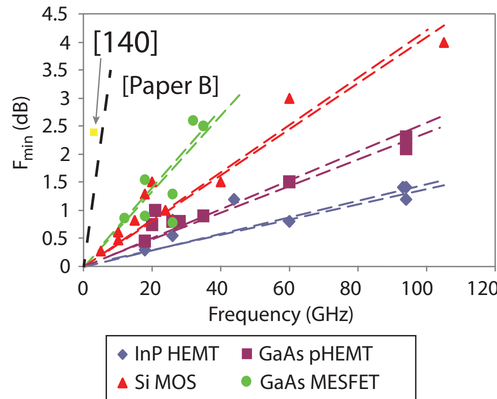

Fig. 4.5: Intrinsic F_{min} of the $L_g = 1$ μm GFET from [Paper B] compared to Si and III-V technologies [32] and a SiC GFET result with a $L_g = 150$ nm device [140].

channel ~ 1.4 V/μm, the carriers are most likely in a linear transport regime with $v_{drift} < 10^7$ cm/s. Nevertheless, when normalised to gate length, the GFET is already competitive comparing to recent Si CMOS nodes [141]. The challenge lies in scaling the gate length with maintained normalised performance. Normalised $T_{min}/f/L_g$ (K/GHz/μm) data is presented in [Paper B], where the SiC GFET from [140] with $L_g = 150$ nm is missing. In the latter study, the optimum result was $F_{min} = 2.4$ dB at 3 GHz as extracted from 50 Ω noise figure measurements, which is very close to the measured curve in Fig. 4.2. The GFET in [Paper B] thus shows larger potential judging from the considerably longer gate length used as compared to [140].

4.3 GFET reliability on SiO_2 substrates

A somewhat overlooked issue in the literature is the reliability and stability of GFETs. An example of the evolution of the transfer characteristics for the amplifier GFET in [Paper C] is shown in Fig. 4.6. At the time of the RF characterisation, the S-parameters and noise figure were stable on a time-scale of 10's of minutes (with result shown in Fig. 5.2), corresponding to the DC of the blue circles in Fig. 4.6. After storage in N_2-environment for one month and then re-exposure to air, another measurement resulted in the black squares in Fig. 4.6. Further iterating the procedure, the characteristics represented by the red diamonds is the outcome of the measurement. Similar changes are not observed in the mixer devices, which are only biased at low currents with $V_{ds} < 0.1$ V. This suggests influence of high current resulting in self-heating, which can be significant on SiO_2 [43], or effects at higher lateral fields.

Speculating, this might be related to hysteresis and doping effects from charge trapping at the SiO_2 surface [142]. A heat treatment in vacuum was initially shown to clean the graphene sheet, whereas re-exposure to an H_2O/O_2 gas mixture severely increased the doping and hysteresis compared to the original state. Various degree of GFET hysteresis is observed also in this work, as exemplified in Fig. 4.7a). Clearly from Fig. 4.6, the change in device characteristics is a shift of the Dirac voltage towards positive voltage

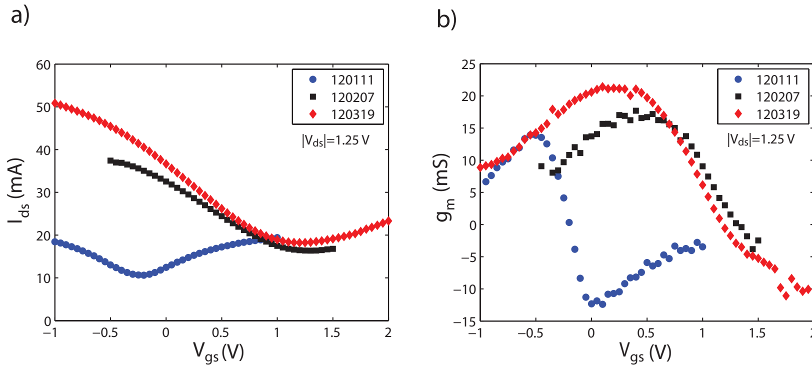

Fig. 4.6: Successive changes in the transfer characteristics with time of the GFET from [Paper C], after high drain voltage and current bias for amplifier characterisation. The device was stored in N_2−environment between the different occasions.

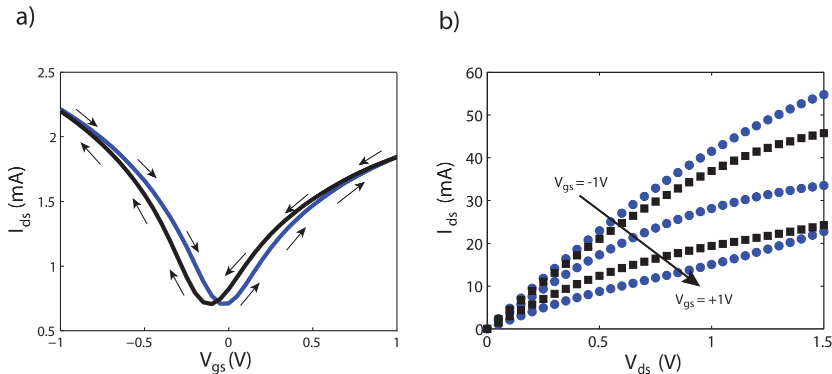

Fig. 4.7: a) Hysteresis of GFET on SiO_2 substrate in air ambient. b) GFET output characteristics [Paper C] in consistency with red diamonds of Fig. 4.6a).

accompanied by a strong asymmetry in n- and p-branch contact resistances and a comparatively unchanged residual carrier concentration. All in all, this indicates increasingly p−type graphene for each measurement occasion. In [Paper C], high contact resistances for both branches ($R_S = R_D = 17\ \Omega$) were extracted. Subsequent desire to include a complete output characteristics, reproduced in Fig. 4.7b), resulted in a delicate task to achieve consistency in between different measurement occasions. In passing, partial channel pinch-off is observed, while the change of carrier type from hole to electron prevents complete current saturation [143]. For this reason, it is impossible to bias at a point simultaneously most favorable for g_m and g_d, unless saturated velocity transport can be achieved at lower fields, i.e. with higher mobility samples.

For comparison, the data in [Paper B] on CVD GFETs was accumulated at a continuous bias for almost one hour with a drift in S_{21} below 2%. On the contrary to Fig. 4.6, the transfer characteristics for these devices slightly degraded in g_m. The carrier concentration remained mostly constant after one month in N_2−box and re-exposure to air. This is possibly a consequence of the higher initial p-type carrier concentration of the CVD graphene compared

to the exfoliated case, as discussed in relation to Fig. 3.6.

Introducing BN supporting layers have been shown to eliminate the hysteresis effects [144]. Also, graphene on hBN has been cleaned by high temperature annealing in H_2/Ar to increase mobility without degrading after re-exposure to air, contrary to SiO_2 [31]. It may thus, in addition to higher carrier velocities and frequencies, improve reliability and stability of GFETs.

Chapter 5

Graphene based microwave circuits

This chapter outlines the thesis contributions in circuit applications of GFETs. In the first part we discuss the power gain and noise performance of a GFET amplifier [Paper C]. The second part describes a GFET single-ended resistive mixer assessed in terms of noise and linearity [Paper D]. Finally, a discussion relating to graphene as an electrode material is presented.

5.1 Small-signal GFET amplifier

Field effect transistor based small-signal amplifiers, especially low noise amplifiers (LNAs), are key components in RF and microwave receivers. As discussed in Section 4.1.2 the main focus in GFET research has rather been the demonstration of high de-embedded f_T's. This is achieved by gate length downscaling, i.e. a miniaturised gate capacitance ($C_{gs}+C_{gd} < 5$ fF), rather than a high transconductance ($g_{mi} < 4$ mS) [30, 111]. Consequently, the devices exhibit no power gain at low frequency and a system impedance $Z_0 = 50\ \Omega$,

$$|S_{21}| = \frac{2Z_0 g_{me}}{1 + Z_0 g_{de}} > 1, \tag{5.1}$$

where the extrinsic transconductance and output conductance are used. These are the derivatives of the measured DC drain current with respect to the applied gate voltage and drain voltage, $g_{me} = dI_{ds}/dV_{gs}$ and $g_{de} = dI_{ds}/dV_{ds}$, respectively. Keeping the other voltage fixed, this results in a family of curves for each. The low gain is further enhanced by the fact $g_{me} < g_{mi}$ and $g_{de} > g_{di}$, resulting from the contact resistances as from Eq. 3.2 and Eq. 3.3.

In a short channel GFET, the resistance modulated by the gate is shadowed by the contact resistances, resulting in lower on-off ratio. In addition, even g_{mi} (expressed in mS/mm) decreases for short channels $L_g \lesssim 1\ \mu$m, attributed to charge traps in the gate oxides [145]. Consequently, the previous reports of $S_{21} > 1$ both utilised $L_g \geq 0.5\ \mu$m [146, 147]. Respectable DC transconductance of $1-2$ mS/μm, comparable to III-V HEMTs [48], have been reported in both CVD and epitaxial graphene [146, 148] at longer gate

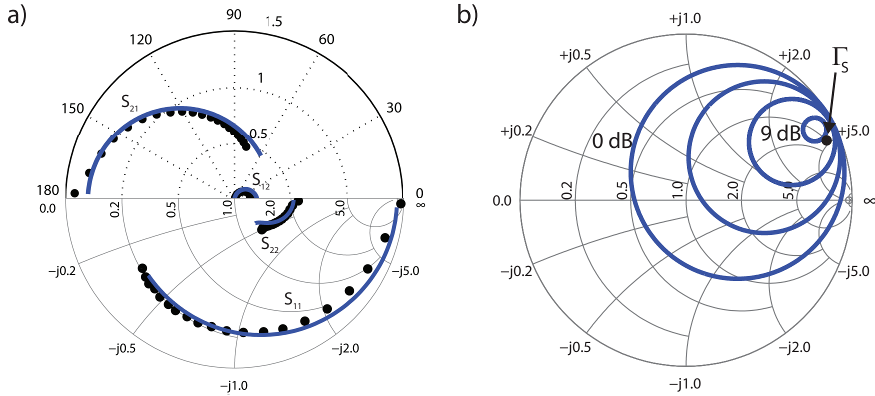

Fig. 5.1: a) Measured (symbols) and modeled (solid line) S-parameters for the amplifier GFET. b) Available power gain circles and the chosen source reflection coefficient for the amplifier design shown by bold bullet.

lengths. The challenge is to maintain the performance to sub-100 nm gates. Herein, achieving high uniformity graphene synthesis enables wider devices, thus decreasing parasitic resistance and increasing absolute transconductance. A remedy for short channel effects can be hBN gate dielectric, which also aids current saturation resulting in lower g_{di} [144].

5.1.1 Amplifier design and characterisation

The first demonstration of a matched small-signal amplifier exhibiting substantial power gain at microwave frequencies, in this case 1 GHz, was presented in [Paper C]. Previously, only voltage gain at gigahertz frequencies was reported [148]. Based on the above discussion, a gate length $L_g = 1$ μm and gate width $W_g = 60$ μm were chosen, as optimised by the large-signal GFET model in [99] with the available maximum exfoliated flake size in mind. This represents a trade-off between contact to channel resistance (i.e. transconductance), current saturation (i.e. output conductance) and gate capacitance (high enough f_{max}/f_T). With this device layout, at a gate bias for optimum gain with $V_{ds} = -1.25$ V, a $g_{me} > 15$ mS and a $g_{de} = 10$ mS were achieved. This yields $|S_{21}| \approx 1.25$ at low frequency from Eq. 5.1. The carrier mobility extracted was $\sim 2,000$ cm^2/Vs. All in all, the result is a useful transistor, albeit not competitive in terms of state-of-the-art high frequency performance.

The amplifier design is based on the measured GFET S-parameters shown in Fig. 5.1a). It utilises an inductance $L = 36$ nH ($Q \approx 44$ at 1 GHz) on the gate port to achieve the available power gain $G_A = 9$ dB at $\Gamma_s \approx 0.9\angle 23\,°$, marked in Fig. 5.1b). The discrete matching topology was chosen since a distributed matching network on a silicon substrate at this low frequency would be impractically large. Leaving the drain at 50 Ω only reduces the achievable transducer gain ~ 0.5 dB and an output match is thus disregarded.

The fabricated amplifier is depicted in Fig. 5.2a), while the measured and

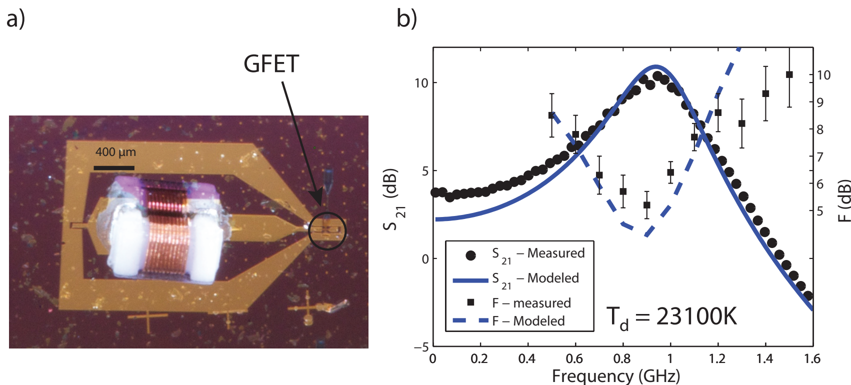

Fig. 5.2: a) Photo of the fabricated amplifier, with the GFET encircled. b) Measured (symbols) and modeled (lines) transducer gain and noise figure of the amplifier.

modeled power gain and noise performance are shown in Fig. 5.2b). The measurement yields $|S_{21}|^2 = G_T = 9.7$ dB (see Eq. 4.5) and $F = 6.4 \pm 0.4$ dB at the design frequency 1 GHz. The uncertainty of the Y-factor noise measurement was estimated according to [149]. Details on the noise modelling of the amplifier is given below.

5.1.2 Amplifier noise analysis

The amplifier noise figure was measured directly with a noise figure analyser (NFA) utilising the method of Y-factor, which is defined by

$$Y = \frac{P_H}{P_C} = \frac{T_H + T_n}{T_C + T_n}. \tag{5.2}$$

In Eq. 5.2, P_H/T_H (P_C/T_C) are the hot (cold) noise powers/temperatures, respectively, from which the device noise temperature T_n is solved. To distinguish the DUT and receiver noise figures via the cascade formula for noise figure, a measurement of noise powers with (primed) and without (unprimed) the DUT provides the DUT gain $G_{DUT} = (P'_H - P'_C)/(P_H - P_C)$.

The Pospieszalski noise model extraction is based on the notion that with $T_g = T_a$ (typical FETs [150]); only the noise figure at a single source impedance is required for the direct algebraic extraction of the second model parameter T_d [151]. Measuring the inductor S_{11} separately provides an estimate of Γ_s versus frequency. A small-signal circuit excluding R_{pg}/R_{pd} in Fig. 4.1 was used in the analysis and an optimum $T_d \sim 23,000$ K was found, giving the model line in Fig. 5.2b). While the fit is satisfactory, the value of T_d is significantly higher compared to previous reports ($< 10,000$ K) [121, 151]. This indicates lumping of several noise mechanisms into the drain current source. Another GFET noise study in the literature [152] used the same approach as in [Paper C], reporting intrinsic $F_{min} \sim 0.3$ dB at 1 GHz. The device was based on SiC graphene providing a semi-insulating substrate, which results in an extracted $T_d = 1700$ K. This indicates the Si substrate in [Paper B] was at least partly responsible for the high T_d. The slope of F_{min} versus frequency is thus possibly

overestimated, and the model inherently narrow band. Further decomposition of the noise contributions within the device requires the determination of all four noise parameters. The predicted minimum noise figures at 1 GHz are given for completeness in Fig. 4.2a). Further uncertainties are introduced by the source resistance extraction in GFETs on exfoliated graphene [99] and the large C_{pg} from the gate pad extending to the non-ideal inductor ($R \approx 5\ \Omega$).

5.2 Subharmonic resistive GFET mixer

A *mixer* is a frequency translating component for information carrying signals, intended for either upconverting the frequency in a transmitter or downconverting it in a receiver. Exemplifying, in this work the GFET operating as downconverting mixer takes two inputs, the frequency to be translated is that of the radio frequency (RF) signal, at f_{RF}, and the local oscillator (LO) is the reference signal, at f_{LO}. The output in this case is at the intermediate frequency (IF), f_{IF}. Mathematically, the operation principle is understood as the product of two sinusoids has the sum and difference frequencies, i.e. $\cos(\omega_{RF}t) \times \cos(\omega_{LO}t) = \frac{1}{2}[\cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t]$.

In practice, the RF voltage is imposed on a time-varying conductance of a diode or FET, modulated (or pumped) by the LO. This generates a current at multiple frequencies including the IF. Resistive (passive) mixing in diodes or FET channels results in a conversion loss, $CL = P_{RF}/P_{IF} > 1$. Transconductance (active) mixing in a FET, with the RF signal input on the gate and the IF extracted at the drain, can provide a conversion gain, $CG = P_{IF}/P_{RF} > 1$.

In addition to the fundamental mixing described above, subharmonic mixing is performed at an harmonic of the LO frequency, i.e. $f_{IF} = f_{RF} - 2 \times f_{LO}$ for a $\times 2$ subharmonic mixer. As the time-varying conductance is periodic, the efficiency of a resistive FET mixer can be analysed via Fourier series expansion such as a conversion matrix approach [153],

$$i_{ds}(t) = g(t) \times v_{RF}(t) = \left(g_0 + 2\sum_{n=1}^{\infty} g_n cos(n\omega_{LO}t) \right) \times v_{RF}(t). \tag{5.3}$$

In Eq. 5.3, g_0, g_1 and g_n gives the output related to the input frequency, fundamental mixing and $\times n$ subharmonic mixing, respectively. A unique feature of the channel conductance of GFETs, such as that of the clean exfoliated sample in Fig. 3.6a), is that it is symmetric around V_{Dirac} and inherently presents a large g_2. As a consequence of the electron-hole duality, GFETs offer subharmonic mixing in a single device [154]. A summary of realised GFET frequency translating devices is presented below and compared to other technologies.

- In [Paper D], a $CL \approx 20$ dB up to $f_{RF} = 5$ GHz was achieved as shown in Fig. 5.3a). This GFET had $L_g = 1\ \mu$m. While resistive mixing is decoupled from f_T and f_{max}, a shorter gate length reduces capacitance and thus the RC time constant. A 30 GHz GFET subharmonic mixer with $CL = 18$ dB was demonstrated in [155] with $L_g = 0.5\ \mu$m.
- Unipolar SiC GFETs permit fundamental resistive mixing with $CL = 18$ dB up to 20 GHz [156], compared to $CL = 5.3$ dB in GaAs HEMTs [157].

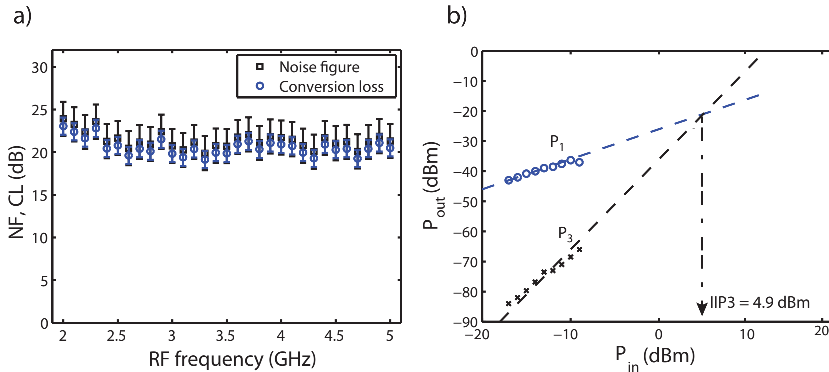

Fig. 5.3: a) Two-tone measurement for mixer linearity (P_{LO} = 2 dBm). b) Conversion loss and noise figure are approximately equal (P_{LO} = 0 dBm) [Paper D].

- With unipolar HEMTs, a configuration has been shown using two FETs for subharmonic mixing, which had the LO fed 180° out of phase to the devices. The design allowed a $CL = 6.5$ dB at $f_{RF} \sim 10$ GHz [158].
- Transconductance GFET mixers are limited by small g_m to $CL \gtrsim 14$ dB [159] up to 10 GHz, while GaAs FETs provide $CG \sim 10$ dB [153].
- The conduction symmetry has also been used in GFET frequency doublers with high spectral purity but also high conversion loss [123, 160].

All above results should be compared to the theoretical minimum conversion loss of 3.9 dB in a resistive FET mixer [157]. To approach this value in GFETs, the introduction of a distinct off state is necessary, which requires a bandgap.

5.2.1 Mixer noise and linearity performance

The introduction of the *resistive FET* mixer was mainly motivated by its potentially higher linearity compared to diode mixers [161]. The LO at the gate sweeps the channel resistance between on- and off-states. The drain is biased at $V_{ds} \approx 0$ V, so the FET operates in the linear regime of its output characteristics, where the harmful third order intermodulation (IM3) products are suppressed. In practice, the RF signal is applied to the drain and the IF signal extracted from the drain via filters or utilising a directional coupler. The advantage of this arrangement can be understood if the conversion is expressed as a Taylor series with the RF voltage assumed to be a small signal

$$i_{ds} = \frac{dI_{ds}}{dV_{ds}} \cdot v_{RF} + \frac{d^2 I_{ds}}{dV_{ds}^2} \cdot v_{RF}^2 + \frac{d^3 I_{ds}}{dV_{ds}^3} \cdot v_{RF}^3 = g_d \cdot v_{RF} + g_{d2} \cdot v_{RF}^2 + g_{d3} \cdot v_{RF}^3. \quad (5.4)$$

In Eq. 5.4, the coefficient g_{d3} is responsible for the IM3 products at $2f_1 - f_2$ and $2f_2 - f_1$ which are close to f_1 and f_2 and thus impossible to filter out. The FET resistive mixer is expected to be highly linear if g_{d3} is small *for all time instances or equivalently all gate voltages* in the LO sweep [162].

In [Paper D], the linearity of the subharmonic GFET mixer was assessed in terms of the third order intercept point referred to the input ($IIP3$). This was extrapolated from a two-tone measurement [153], as the intercept of the linear output which rises 1 dB/dB and the third order response which increases 3 dB/dB as seen in Fig. 5.3b). Since IIP3 improves with increased LO power [155], like the CL decreases, the $IIP3$ quality factor $Q(IIP3) = IIP3/P_{LO}$ can be used for benchmark. A comparison to literature is outlined below.

- The highest linearity in this work is $IIP3 = 4.9$ dBm at $P_{LO} = 2$ dBm, which corresponds to $Q(IIP3) = 2.9$ dB, as shown in Fig. 5.3b).
- The GFET mixers in [Paper D] and [155] does not show the full potential of FET resistive mixers for linearity, also compared to e.g. a subharmonic CMOS design with $IIP3 = 17$ dBm and $Q(IIP3) = 13$ dB [163].
- The fundamental GFET mixer in [156], on the other hand, is already comparable to GaAs technology [161] in terms of $Q(IIP3) \sim 20$ dB.
- Wide bandgap semiconductors such as GaN can provide supreme linearity ($IIP3 \sim 30$ dBm) due to its high LO power handling capabilities. However, it comes at comparatively low $Q(IIP3) = 7$ dB [164].

An additional advantage of the FET resistive mixer is the slightly lower noise figure compared to diode mixers. As long as the gate is not driven into conduction, there is no penalty from shot noise enhancement [161]. In [Paper D], the attenuator noise model for mixers [127] was considered, which results in $NF \approx CL$ for pure thermal noise at room temperature. This was in essence, within measurement uncertainty, verified as reproduced in Fig. 5.3a). Cryogenic studies can clarify deviations from this behaviour. To improve the CL and NF levels, the pumped GFET resistance must closer resemble a square wave with even on- and off-state times, i.e. by the introduction of a bandgap.

5.3 Graphene for FBAR electrodes

Besides increasing data rates, modern cell phones combine several functionalities at different frequency bands, such as wireless LAN and GPS. Voltage controlled oscillators (VCOs) for frequency generation and switchable or tunable filters are desirable for this purpose. In VCOs, a tunable resonance and high quality factor (Q-factor) module is required for low phase noise, increasingly important to avoid interference between bands in a crowded spectra. An appealing alternative to existing varactor based LC tanks is the tunable film bulk acoustic wave resonator (FBAR) based on either $Ba_xSr_{1-x}TiO_3$ (barium strontium titanate) [165] or $(1-x)BiFeO_3$-$xBaTiO_3$ (bismuth ferrite - barium titanate) [166] ferroelectrics. In practice the FBAR provides two resonances, the series resonance at f_s which is mainly tunable with relative tunability n_{fs} and at slightly higher frequency the parallel resonance at f_p with minor relative tunability n_{fp}. Already today, fixed frequency AlN FBARs with $Q > 1000$ are used i.e. in switchable filter banks in communication systems [36].

In contrast to electromagnetic resonators, FBARs utilise the confinement of an acoustic wave in between two reflective interfaces. In the solidly mounted

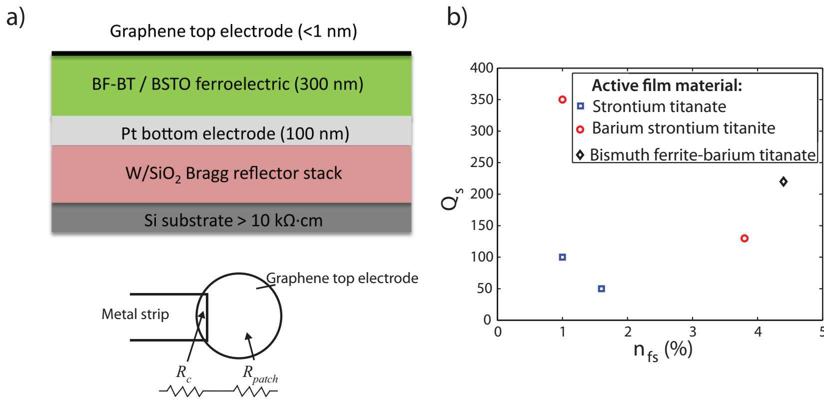

Fig. 5.4: a) FBAR cross section and top electrode series resistance illustration. b) Series resonance tunability and Q-factor of selected FBARs [36, 166].

type in Fig. 5.4a), these consist of air and a Bragg reflector consisting of alternating low- and high acoustic impedance materials (i.e. SiO_2/W). Ferroelectric films in paraelectric phase provide a stiffness and thus acoustic velocity tunable with an electric field applied in between the top and bottom electrodes sandwiching the active film, which enables a tunable resonance frequency. This enables smoothly tunable filters and high performance VCOs for agile communication systems. While the Q-factors of these resonators can exceed 200, already exceeding LC tanks using varactors in VCOs [167], the frequency tunability limited to $< 5\%$ is insufficient for the demanding multi-channel transceiver requirements. A selection of recent results is collected in Fig. 5.4b), where the lack of combined high-Q and large n_{fs} is evident.

5.3.1 Graphene for enhanced tunability

Besides improvement in ferroelectric film crystallinity and surface roughness [166], a modification of the resonator electrodes may mediate these issues. Quantitatively, the effective series resonance tunability ($n_{fs,eff}$) of a contacted FBAR is reduced compared to a bare ferroelectric film ($n_{fs,i}$) as [168]

$$n_{fs,eff} = n_{fs,i} \times \frac{t_p/v_p}{t_p/v_p + t_b/v_b + t_t/v_t}, \tag{5.5}$$

where v_t/v_b and v_p are the acoustic velocities of the top/bottom electrode and ferroelectric layer, respectively. Reducing the electrode thicknesses (typically $t_t = 100$ nm Al and $t_b = 100$ nm Pt [165]) to zero, the resonance frequency and relative tunability may be enhanced. In this context, atomically thin graphene enables, in a first step, to reduce the *top* electrode thickness to virtually zero. Pulsed laser deposition of ferroelectric film on top of the *bottom* electrode at $T > 600\,°C$ in O_2-rich environment, however, likely introduces defects in graphene, especially in CVD graphene with higher intrinsic defect density [169]. In contrast to graphene electrodes for GaN light emitting diodes necessitating a combination of low R_{sh} and high optical transmittance [27],

Table 5.1: R_{sh} of graphene versus # layers and chemical treatment.
[a] Layer-by-layer transfer, Cu foil catalyst. [b] Direct growth on thin film Ni. [c] SiC.

# layers	Treatment	R_{sh}
1-3[a]	As grown	800-300 Ω/□ [27,82]
4[a]	HNO_3	30 Ω/□ [170]
∼ 8[b]	As grown	∼280 Ω/□ [171]
2[c]	H_2-intercal.	∼200 Ω/□ [101]

electrical conductivity and ultimate thinness are the decisive properties to consider graphene for FBAR electrodes.

5.3.2 Prospects of graphene electrodes

In practice, the sheet resistance of graphene is considerably higher than that of Al and an ohmic metal interface is introduced in the structure, which increases the FBAR series resistance (R_s) compared to metallic electrodes. It can be approximated as $R_s \approx R_c + R_{patch} = R_c + R_{sh}/2\pi$, assuming a circular top electrode illustrated in Fig. 5.4a). The current Pd contacts allow $R_cW < 100$ $\Omega\mu m$ and thus $R_c \sim 1$ Ω is feasible. To maintain an appreciably high Q-factor of series resonance $R_s < 5$ Ω is desirable [36], which requires $R_{sh} \approx 25$ Ω/□. This represents a 1-2 orders of magnitude improvement to the current levels of *single-layer* graphene in Fig. 3.5. It is similar to the criteria for replacement of indium tin oxide (ITO) with $R_{sh} \sim 30$ Ω/□ in GaN laser electrodes [27]. The most viable pathway towards this end is application of multilayered graphene, either direct growth of few-layer graphene on nickel or transferring multiple single layers on top of each other. A summary of available results from the literature is presented in Table 5.1. The efficiency, reproducibility and permanency of carrier enhancement via chemical processes, e.g nitric acid (HNO_3) [170] or iron chloride ($FeCl_3$) [172], are questionable as graphene is commonly exposed to them as etchants used in the transfer process from CVD growth catalyst to final substate.

In any case, the parallel resonance is practically unaffected by increased series resistance. Although offering less tunability to start with [165], it improves similarly to the series resonance with reduced loading of the electrodes.

Chapter 6

Conclusions and future outlook

In this thesis, the GFETs have been explored for microwave circuit applications, using both mechanically cleaved and CVD grown graphene transferred to SiO_2 substrates. Focus was mainly on practical devices exhibiting power gain for LNAs, rather than extreme gate length scaling to pursue high intrinsic f_T and f_{max}. Starting from an exfoliated flake, the first GFET small-signal amplifier, with 10 dB gain and 6.4 dB noise figure, was successfully fabricated and characterised. Although yielding comparatively lower mobilities, $\lesssim 1,000$ cm^2/Vs, than exfoliated samples, $\gtrsim 2,000$ cm^2/Vs, the CVD GFETs present a lower parasitic source resistance, $R_S \sim 150$ $\Omega\mu$m, and finally a similar performance. Accordingly, the first device level graphene microwave noise characterisation was feasible using CVD GFETs. Sub-1 dB and sub-3 dB noise figures up to 2 GHz and 8 GHz appear achievable in the near future, by applying established methodology for FET small-signal and noise modelling.

To improve these results and approach Si CMOS and III-V:s in performance and yield, graphene transport must be improved using highly scalable and reliable processing technologies. Large grain size and high mobility CVD graphene has been demonstrated, although in time-consuming and presumably costly processes. Suspended graphene is impractical on a large scale, but boron nitride remains an attractive substrate option, in aspects ranging from transport to reliability. So far, the promising works on graphene transport on hBN employ cleaved material and improvement on RF devices has been limited [173]. Furthermore, the ultimate aim of catalyst free hBN/graphene/hBN structures grown *in situ* by CVD is in its infancy [174], with smaller grains and lower mobility [175]. In addition, the limitations on power gain and gate length scaling due to the lack of a bandgap are yet to fully emerge.

Presumably, the most likely commercial applications of GFETs are in mass market, large volume products such as high-speed communications, rather than cost insensitive and extremely performance demanding fields such as LNAs for radio astronomy. Novel concepts such as the subharmonic resistive mixer assessed in this work and the enhanced integration possibilities with Si CMOS [35] as compared to III-V:s for system-on-chip are important in this context. Here, graphene can be used to implement the RF circuitry.

In addition, an initial DC and microwave characterisation of material and contacts for the feasibility of utilising a graphene electrode in FBARs has been performed. As part of this work, a geometrical model for the contact capacitance of a metal-graphene interface was presented. Based on the majority of values for sheet resistance of graphene in the literature, $R_{sh} > 100\ \Omega/\square$, it remains difficult to reach the target resonator series resistance. The feasibility lies in using multilayer graphene together with an efficient and reproducible doping process for graphene layers, where so far only a single report reaches the required $R_{sh} = 30\ \Omega/\square$ [170]. In general, the wafer-scale homogenous growth of graphene need be complemented by the selective control of its properties, and subsequent passivation from being affected by the ambient. This includes for example high doping of contact areas, while maintaining a pristine channel to enable good current modulation and a symmetric transfer characteristics by the electron-hole symmetry in graphene.

Finally, the unique properties of graphene can pave the way for applications in bendable high frequency electronics and THz electronics. Even under high strain, graphene can sustain higher mobility compared to other materials and provide a cut-off frequency up to 25 GHz [26]. Successful on-wafer rectification of millimetre waves up to 110 GHz with an epitaxial GFET [176] and proof-of-concept antenna coupled self mixing at 300 GHz [177], with large room for improvement, in graphene have both been demonstrated. In addition, tuning the carrier concentration in graphene sheets can accomplish attenuation and modulation of THz radiation [178]. The latter are all interesting and less explored future directions to proceed with graphene to bridge the THz gap.

Chapter 7

Summary of appended papers

The appended papers on which this thesis is based are summarised in this chapter, along with my personal contributions to each.

Paper A

Microwave characterization of Ti/Au graphene contacts

Microwave measurements of circular TLM structures on CVD graphene are used to model the capacitance of metal-graphene contacts, besides contact- and sheet resistance extraction. My contributions include processing and measurements, data analysis with co-authors, and finally writing the paper.

Paper B

Microwave noise characterization of graphene field effect transistors

In this paper, the results from multiple impedance measurements in the frequency range 2-8 GHz of GFETs on CVD graphene are reported. The resulting complete noise parameter set allows a deeper analysis with noise de-embedding and modelling techniques, predicting the possibility of sub-1 dB noise figure up to 2 GHz. The work was performed in the form of a master thesis, which I supervised on daily basis. My contributions accordingly include fabrication guidance, arrangement of noise measurements, assistance in selection of analysis methods and taking significant part in the preparation of the paper.

Paper C

10 dB small-signal graphene FET amplifier

The first report of a matched GFET amplifier based on exfoliated graphene, exhibiting 10 dB small-signal gain and 6.4 dB noise figure at 1 GHz, is presented. Tentative GFET noise modelling using the Pospieszalski model is performed. My contributions include main parts of the design, fabrication, noise modelling and writing of the letter, as well as taking part in the characterisation.

Paper D

Resistive Graphene FET Subharmonic Mixers: Noise and Linearity Assessment

Conversion loss, noise figure and linearity of resistive subharmonic GFET mixers made on exfoliated graphene, within the RF frequency range 2-5 GHz, is reported in this paper. My contributions include fabrication, participation in the measurements and data analysis, as well as writing the paper.

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