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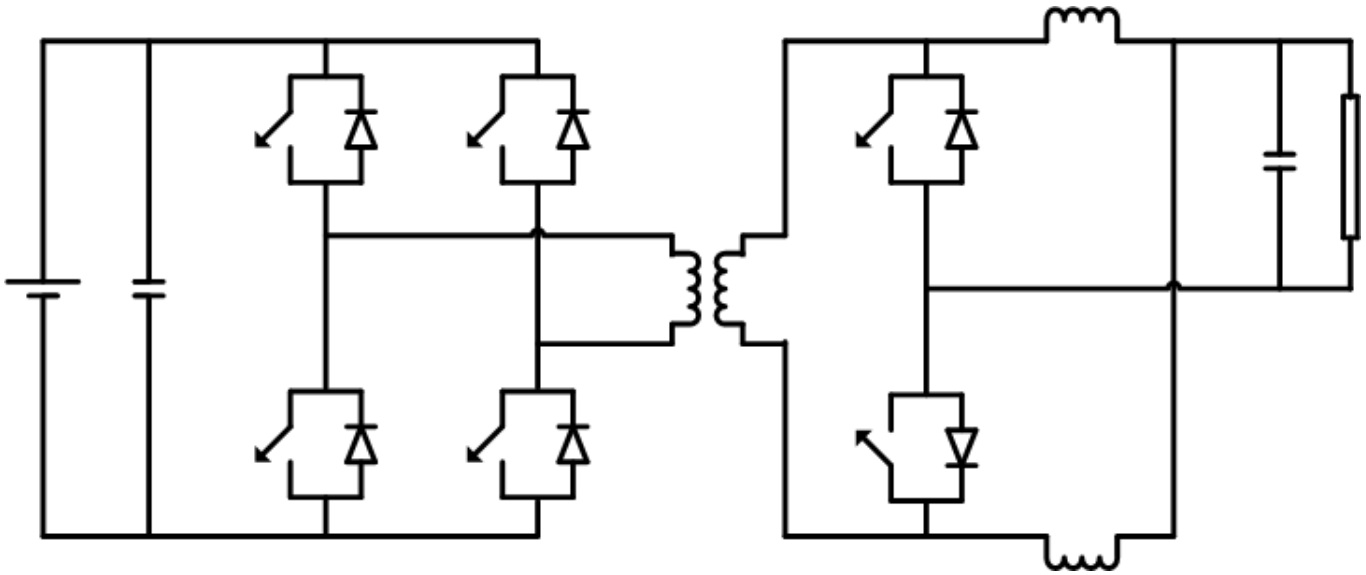

Chalmers Master's Thesis

Energy Efficiency Investigation of a 3kW DC/DC Converter for Electric Vehicle Applications using Full Wave and Current Doubler Synchronous Rectification

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Abstract

- The Master's Thesis is devoted to quantify and verify the performance of two full-bridge DC/DC converter topologies that are suitable for usage in a hybrid electric vehicle, whereas possible improvements should be proposed and implemented. The two topologies investigated are the full bridge with full wave rectification and full bridge with current doubler synchronous rectification. The idea is that the converter topologies should be implemented in Allegro AMS and a loss calculation script should be written in Matlab. It should be possible to simulate and study the converters' performance in the ideal and real cases. In the project two different topologies were investigated and built in Allegro AMS. Simulations have been performed in Allegro AMS and calculations carried out in Matlab. Zero-voltage switching (ZVS) technique has been implemented and verified. A suitable transformer has been designed and the whole procedure has been presented in the report. Losses have been determined and the efficiency plots have been created and presented.

- The performed simulations have shown that it is possible to utilize both converters in a HEV and the normal performance has been verified. ZVS switching technique has been successfully implemented that has reduced switching losses significantly, which has improved the efficiency of the converters. A calculation script for loss determination has been successfully written and losses have been determined, which are included in the results section. A transformer has been designed and the size of it has been minimized with the appropriate core being chosen. Efficiency has been determined and for the full wave topology it reached a maximum value at 95.4 % at the load level of 35% and for the current doubler it has reached 96.5 % at the load level of 30 %. It has been shown that the current doubler is more efficient than the full wave topology.

- Full bridge DC/DC converter, modeling, zero-voltage switching, current doubler, synchronous rectification, switching loss, conduction loss, transformer design, efficiency

Acknowledgments

We are grateful to Volvo Car Corporation, specially to Karl Klang for giving us the opportunity to perform our project at their premises. We would like to express special gratitude to all the guys who were helping and supporting us throughout the project, especially to Mats Nilsson, Anders Magnusson and Leif Karlsson.

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1

Introduction

Growing concerns over environmental impact lead to the development of more eco-friendly technologies in almost all industrial branches. Automotive industry is highly concerned over governmental continuous legislation adjustments towards the reduction of exhaust gas emissions. However, pollution is not the only vital aspect that must be considered, another fact is that fossil fuels are depleting, hence the road transportation sector has high dependency on it and convenient alternatives must be identified to maintain efficient and reliable performance.

All major car manufacturers have taken a new direction towards sustainable transportation, thus integrating electric powertrains in conventional ones or replacing it totally with fully electrical. These changes infer to absolutely all new and different concepts of perception for automotive industry sector. This all unique concept is called hybrid electric vehicles, which already devised 100 years ago. The research in this particular area has been accelerated in a rapid pace during recent years. A lot of development strategies have been elaborated, relevant experiments have been performed and practical models have been built.

However, new technologies are always supported by complex systems comprised of power electronic devices, which enable more controllability whilst they contribute towards robust, reliable performance of a particular object. Therefore, vehicles are not exceptions, a bunch of power electronic devices are involved, where converters play a tremendous role, allowing reliable workability of the hybrid electric vehicles.

Consequently, the following discussion and analysis will be devoted to investigate and to quantify several DC/DC converter topologies used for auxiliary purposes inside the hybrid electric vehicles.

1.1 Background

There are several different electrified vehicle topologies that are known today. All of them come with rechargeable batteries that can be restored to almost full state of charge by either connecting the vehicle plug to an external power source or by an internal generator on board in the car. However, to achieve a smart control and efficient charging, a good utilization of the power electronic converter is highly required. Therefore, all the following analysis will be oriented on deep investigation, validation and quantification of DC/DC converters, needed for auxiliary purposes in a hybrid electric vehicle. Formerly, it was the alternator that has been generating power to the internal power network inside the car, but now manufacturers are heading towards utilization of more innovative decisions, those like DC/DC converters. Those power electronic devices are much more efficient, allow better controlability, safer and more powerful. They are fed from the main battery package of the car. There is a massively growing tendency towards replacing the power supply for the auxilitary purposes with the DC/DC converters instead. Various topologies are utilized for this particular purpose nowadays. Every manufacturer has their own design and arrangement of such a DC/DC converter, which corresponds to the particular requirements every producer should strictly follow. In the project, two different topologies that are quite common in electrified vehicle applications were investigated and their performance quantified. Those are full bridge DC/DC converters with full wave and current doubler synchronous rectification.

1.2 Aim/Purpose

The aim of the thesis is to investigate, quantify and validate the performance of the full-bridge DC/DC converter used in an electrified vehicle. The purpose, which is implied in the project, is referred to quantification of losses and efficiency of both converter topologies as well as verification of DC/DC converter functionalities for a hybrid electric vehicle. The tasks to be performed in the project can be divided into the following subtasks, where each will be further analyzed:

- Simulation object
- Waveforms attainment
- Analysis & comparison
- Validation & quantification
- Cost estimation

1.3 Simulation object

The objects simulated are full bridge DC/DC converters with different types of rectification and the location of it in the car is shown in Fig. 1.1. In this particular project two different topologies of DC/DC converters will be implemented. One of them is with full wave rectification and the another one is with current doubler rectification. The converters are supposed to transform the voltage level, from 355 VDC to 14 VDC, which is to be used in a hybrid electric vehicle internal power network needed to supply auxiliary services. The converter will be fed from a 355 VDC voltage source. It will have a transformer for galvanic insulation and full-bridge rectifier on the output with a LC filter to reduce output ripple as much as possible.

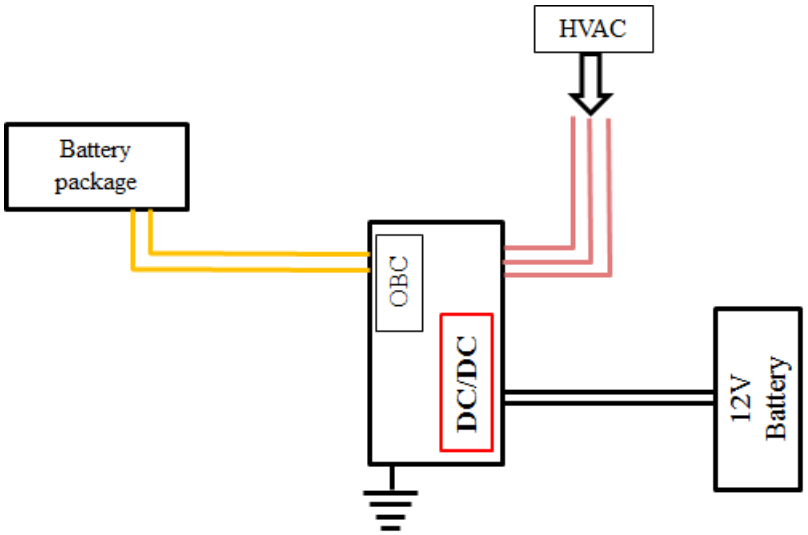

Fig. 1.1: Part of the architecture of an electric vehicle, the investigated DC/DC converter is marked red

1.4 Method

- Study relevant equipment, literature and documentation
- Get familiar with Allegro AMS software, hence build up different DC/DC converter topologies in the software
- Analyze the performance of the converters and problems, which might arise and ways of solving those problems

- Compare the ideal and real converters, verify the simulated performance through studying relevant waveforms
- Determine the appropriate switching technique, among hard- or soft-switching
- Determine and quantify important parameters, ex. efficiency, losses etc.
- Analyze and verify the obtained results, maybe suggest possible improvements, if necessary.

2

Theory overview

This chapter is devoted to give a short overview of the equipment being used and implemented in the project.

2.1 Various topologies

There are several converter topologies that have been investigated and implemented in the project. In order to understand the behavior and the performance of the converter, coherent explanations and fundamentals of them are included in the following sections. In the meantime, DC/DC converters are the devices that change one level of DC voltage to another (either higher or lower) level . They are basically used in battery-powered applications and devices that require different levels of voltage. A DC/DC converters allow such an equipment to be powered from a battery with a single voltage level, avoiding the bulky and heavy battery packs required for various individual purposes.

There are many topologies for DC/DC conversion, such as buck, boost, buck-boost, forward, cuk, flyback, push-pull converters etc. Additionally, usually a distinction is made between isolated and non-isolated converters. In many applications multiple outputs are required, safety standards need to be met and impedance matching must be provided, therefore output isolation may be required to be implemented. Since the thesis is dealing with an application in a hybrid electric vehicles, there are several topologies that are utilized nowadays. However, this project will stick to two of them, which are commonly exploited. They are the conventional full-bridge with full wave synchronous rectification and the current doubler topology with synchronous rectification.

2.1.1 Conventional full bridge DC-DC converter with full wave synchronous rectification

High power bi-directional DC/DC converters are required for applications such as battery charges, hybrid electric vehicles, uninterruptible power systems [1]. The bi-directional DC/DC converter is great for electric vehicle applications. The most fundamental of the existing high power bi-directional DC/DC converter topologies is depicted in Fig. 3.1, which can be operated alternately as a step-down or a step-up converter. It is characterized by a traditional full bridge inverter, isolation transformer and high current rectifier with synchronous rectification on the low voltage side. The input to the converter could be either fixed or it could be varying magnitude DC voltage. The output voltage can be controlled with either duty cycle control or phase-shifting technique. Similarly, the magnitude and the direction of the output current can be controlled [2].

2.1.2 Full bridge DC-DC converter with current doubler rectification

One of the most common alternative topologies for vehicle applications is current doubler. The inverter side of this topology is the same as conventional full bridge converter with four switches in two different legs. The difference is in the rectifier side which has only two switches instead of four. Each switch sees the output current when it is switched on, but this output current is divided between transformer and one of the output inductors. Therefore, only half of the output current flows through the transformer and that's why it is called current doubler. Less current in the transformer means less losses. This circuit has one additional filter inductor in the output side compared to the conventional topology, but each of those inductors carries only half of the output current. Indeed, there is always current in these two inductors and these currents will be integrated and flow to the load. Comparing to other alternative topologies, which have center-tapped transformer, this circuit has simpler structure of transformer which results in smaller size. The topology is shown in Fig. 3.2 [7].

2.2 Zero voltage switching

Conventional LC loop shaping circuit also called resonant circuit is often used in shaping the switch voltage and current in order to yield zero-voltage and/or zero-current switching. These techniques have been developed using resonant switch concept to tackle the switching losses in power devices as well as to suppress electromagnetic interference (EMI) produced, due to large di/dt and dv/dt caused by switch-mode operation. The zero-voltage-switching (ZVS) can reduce the total switching losses by more than half, while zero-current-switching (ZCS) reduces them by about 25 % when compared to hard switching. Hard switching can be described by simple switching trajectory (loci) that is represented in Fig. 2.1.

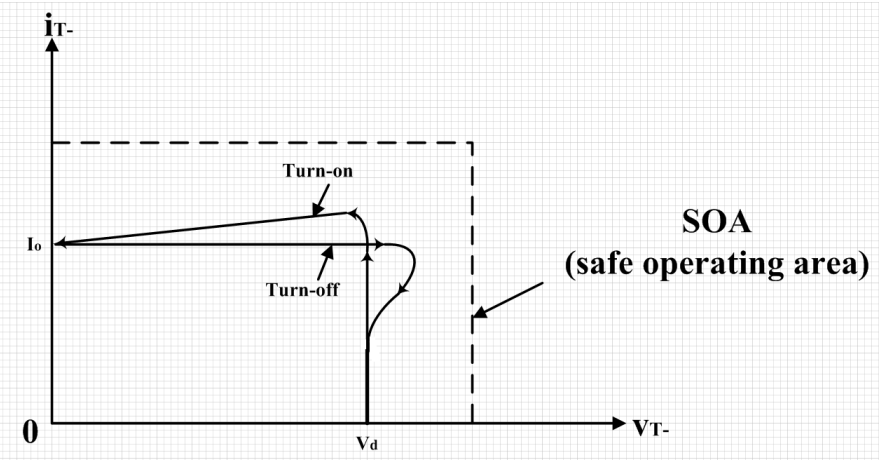

Fig. 2.1: Switch mode inductive current switching

The area under this trajectory represents the switching loss, hence it must be reduced. This might be done in different ways. To relieve these switch stresses, dissipative snubber circuits may be connected in series or parallel with the switches in the switch-mode converters. However, these snubbers do not decrease the overall switching power loss, because it is simply shifted from the switch to the snubber circuit. Consequently, to overcome these unwelcome stresses one may utilize the technique of turning on and off each of the converter switches when either the switch voltage or current is zero. Ideally, the switching transition must occur when both voltage and current are zero, thus results in the following switching trajectory depicted in Fig. 2.2, where the losses would be reduced.

ZVS topology is constituted, when the switch turns on and off at zero voltage. The peak resonant voltage appears across the switch, but the peak switch current remains the same as in its switched-mode counterpart. In contrast to ZCS, the

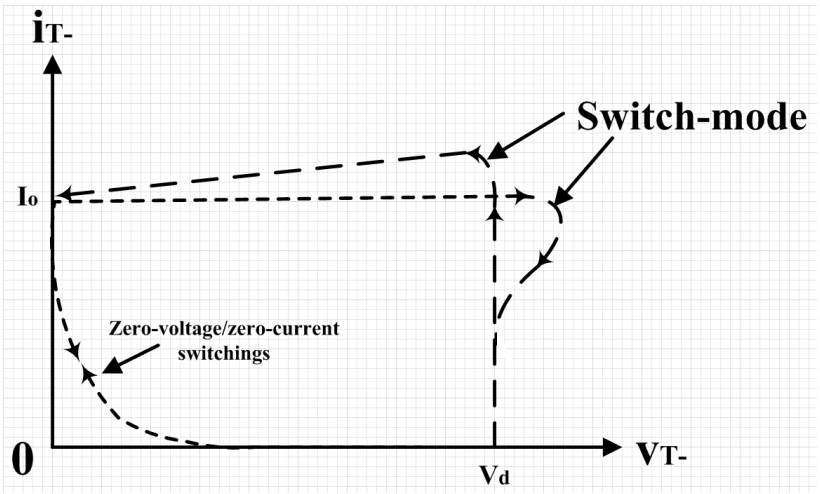

Fig. 2.2: ZVS or ZCS switching loci that represent improved pattern

ZVS technique eliminates switching loss and di/dt noise due to the discharging of MOSFET's junction capacitances and the reverse recovery diodes, and enables the converters to operate at yet high switching frequencies.

2.3 Transformer

It is a static electric power device that transfers energy by inductive coupling between its windings circuits. The principle of energy transfer is based on the magnetic law of induction. In the particular application, where low output voltage and very high output current are required for supplying the auxiliary network of the car, the transformer is required not only for isolation purposes, but to downscale the high input voltage of 355 V to 14 V at the output. The size of the transformer is minimized, since it will be working in high-frequency switched-mode power supplies. The chosen current and voltage limits are selected based on safety reasons and regulations of the requirements for this particular application.

3

Set-up description

This chapter is devoted to the thorough description of the converter circuits being investigated in the thesis work. The coherent analysis is conducted with simulated results and an explicit explanation of the converters' performance is carried out through obtained waveforms.

3.1 Case I

3.1.1 Full-bridge DC-DC converter with synchronous full wave rectification

In the circuit below the full-bridge DC-DC converter with full wave rectification on the secondary side is depicted. It is commonly utilized in different applications, mostly power supplies for various purposes. The proposed topology is investigated since it is conventional and formerly was widely used; hence the comparison with innovative ones would be important and perceptive. First, the topology shown in Fig. 3.1 is discussed.

In this full-bridge converter, the input is a dc link with varying magnitude DC voltage V_s and the input capacitor. The primary side consists of two legs, one active and one passive; where in each leg there are two primary switches and their diodes in anti-parallel to allow freewheeling, when there is no power transfer interval. The secondary side has the same configuration as the primary, but diodes are connected in parallel to the switches, to allow current flow when some switch is not conducting (current commutation interval). Both sides are coupled through a transformer for safety purposes and to have galvanic insulation.

On the output of the converter, an output filter is installed to prevent high current and voltage ripple, consisting of an inductor and a capacitor. The performance of the converter was investigated utilizing unipolar and bipolar switching technique, whereas implementing hard and soft switching as well.

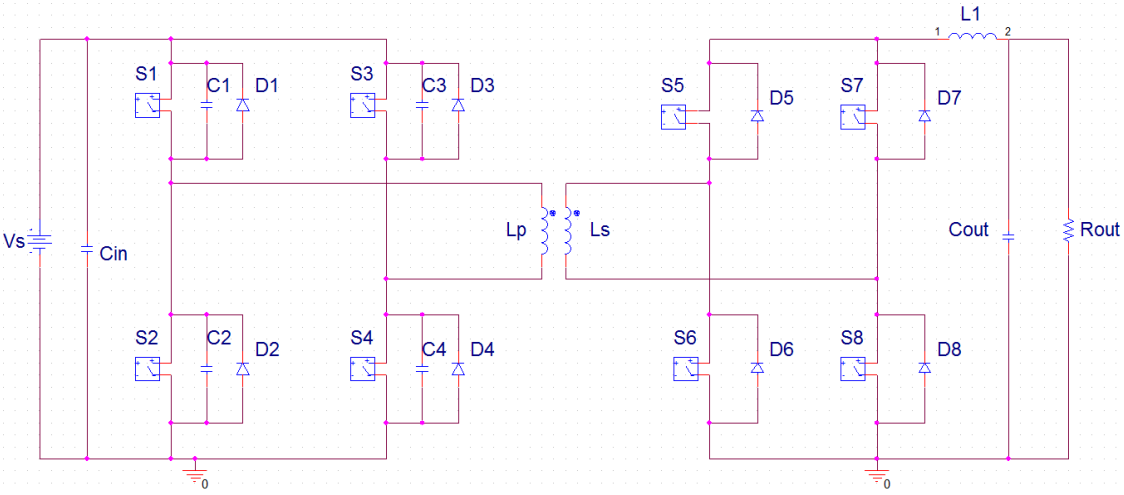

Fig. 3.1: Conventional full-bridge DC-DC converter with synchronous rectification

3.2 Case II

3.2.1 Full-bridge converter with current doubler synchronous rectification

There are different possible topologies which can be studied and compared with conventional full wave rectification converter. One of these choices is a full bridge converter with current doubler rectification on the secondary side. By having a current doubler structure, the secondary side of the transformer only sees half of the output current with no center tapping need. Different topologies also exist in order to achieve current doubling characteristics. They are made by changing the location of switches and inductors on the secondary side and also by choosing diodes or other semiconductors as switches. Using switches instead of diodes at the rectifier side is preferred in order to achieve synchronous (active) rectification for improving the efficiency.

On the other hand, the output voltage in this particular application is not high and the diode voltage drops will be a high percentage of the output voltage in case

of using diodes which is not reasonable. A full bridge converter with a current doubler synchronous rectification with ideal components is shown in Fig. 3.2.

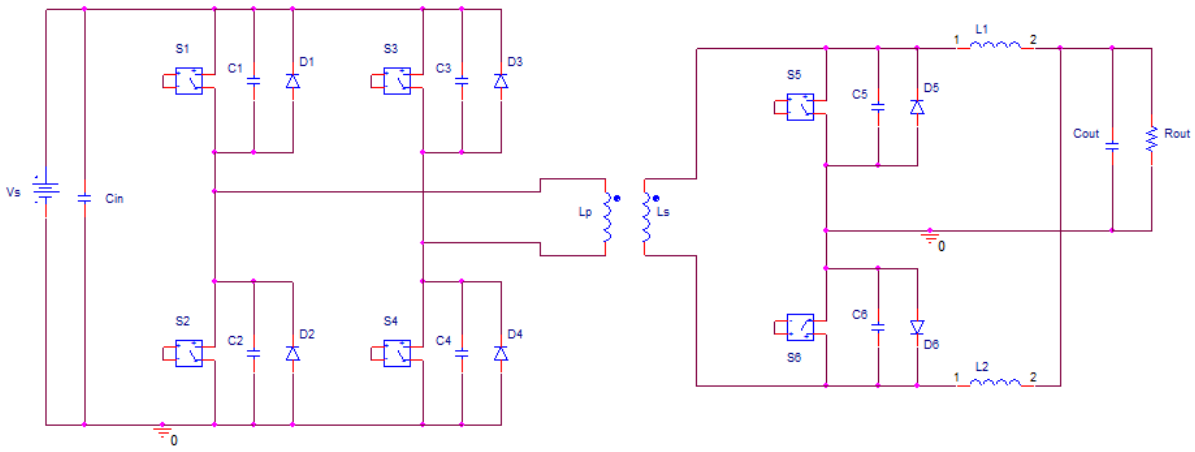

Fig. 3.2: Full-bridge DC-DC converter with current doubler synchronous rectification

3.3 Switching pattern

There is a big variety of switching patterns utilized in modern switching converters. Depending on the purpose, the converter must be operated using appropriate switching technique. Concerning the project's application purpose, one may say that there is a vital need to deliver regulated low ripple voltage to the battery, having a big freedom in controlling the output voltage. Therefore, the unipolar switching technique based on enhanced phase-shifted controller (UCC2895 TEXAS Instruments) has been implemented. However, for the analysis purposes, another switching pattern has been implemented using almost 50% duty cycle which is called bipolar switching.

3.3.1 Switching pattern of Case I

When operating with a bidirectional DC-DC converter there is desire to reduce the size of it, therefore conventional topologies with hard-switching operate at high frequencies. However, higher switching frequencies result in an increase of switching losses, which have to be minimized. In this case, a switching frequency of 100 kHz (T = 10μs) was used. The duty cycle is chosen to be slightly lower than 50%, due to the fact that there is a need to have a small blanking time between switches to prevent a short-circuit of a leg. To be able to analyze and compare, two

different switching modes were implemented, considering hard and soft switching techniques.

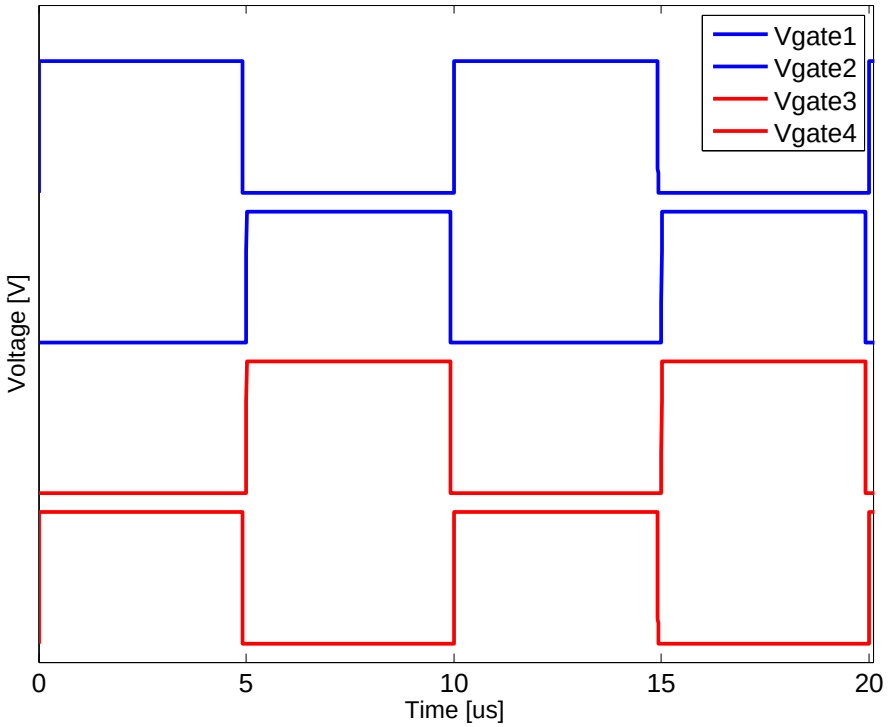

Fig. 3.3: Bipolar switching pattern, gate drive signals

Hard switching implies that power switches must cut off the load current within turn on and turn off time intervals, resulting in severe stress on the semiconductors. The switching trajectories for different switching techniques may be illustrated according to Fig. 3.3 and Fig. 3.6. During the switching intervals, the power semiconductor device should withstand high voltage and high current at the same time, resulting in substantial stress and switching losses. This causes many additional problems, like heat dissipation, exaggerated components' ratings etc. Therefore, the concept is to move to resonant converter operation, incorporating zero voltage (ZVS) or zero current (ZCS) switching with the help of a resonant tank, consisting of inductances and capacitors. This creates oscillatory (usually sinusoidal) voltage and/or current that enables to accommodate ZVS or ZCS, hence reducing the switching losses.

As it is seen from the circuit, the secondary side is implemented with controlled switches; such a configuration is called synchronous rectification. It eliminates the body diode conduction and reduces the rectifier conduction loss, hence improves

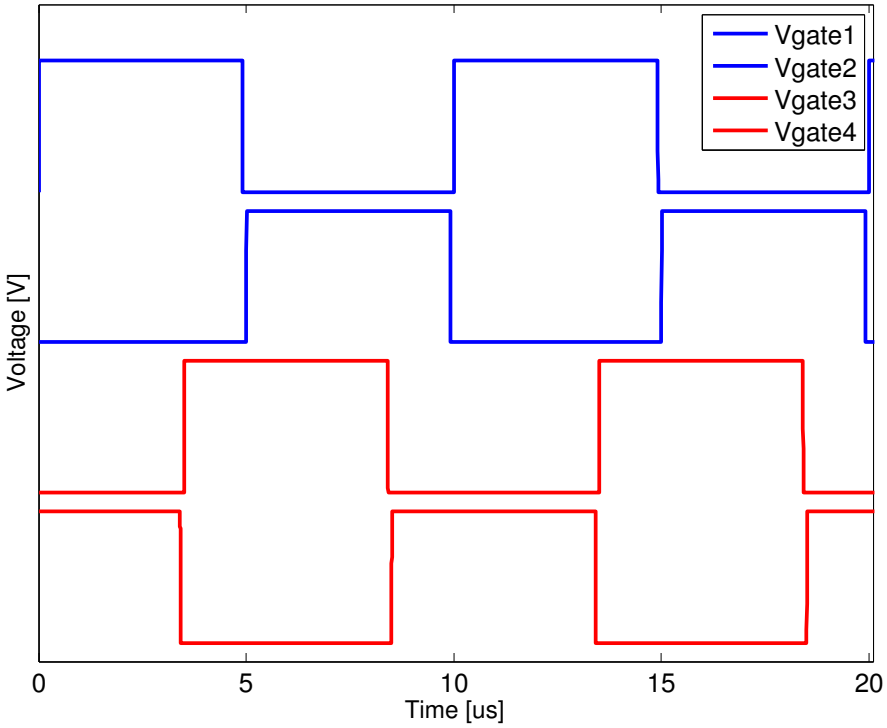

Fig. 3.4: Unipolar switching pattern, gate drive signals

converter efficiency. However, there is a time instant when the parasitic body diode unavoidably will carry the load current, which decreases the converter's efficiency because of the higher voltage drop over the body diode than over the switch itself. Moreover, problems like increased switching losses and electromagnetic interference (EMI) occurring due to reverse recovery of body diodes arise. Consequently, introducing a resonant LC-tank allows avoiding conduction of the body diode during the switching transitions. Therefore, with the help of the energy released from the resonant tank, the switch junction capacitance is discharged, which allows the power switch to turn on at ZVS.

3.3.2 Switching pattern of Case II

On the full bridge side, the same pattern as mentioned in case I is implemented. Bipolar switching, which means two pairs of diagonal switches work respectively and unipolar switching, when diagonal switches work with a certain delay relative to each other that is also called the phase shift. The difference between this case and the previous one is the secondary side, where four switches are replaced by two. In the bipolar pattern two secondary switches are working in the same manner as

the primary passive leg switches with the same duty cycle of slightly below 50%. The gate voltages of the six switches are shown in Fig. 3.5.

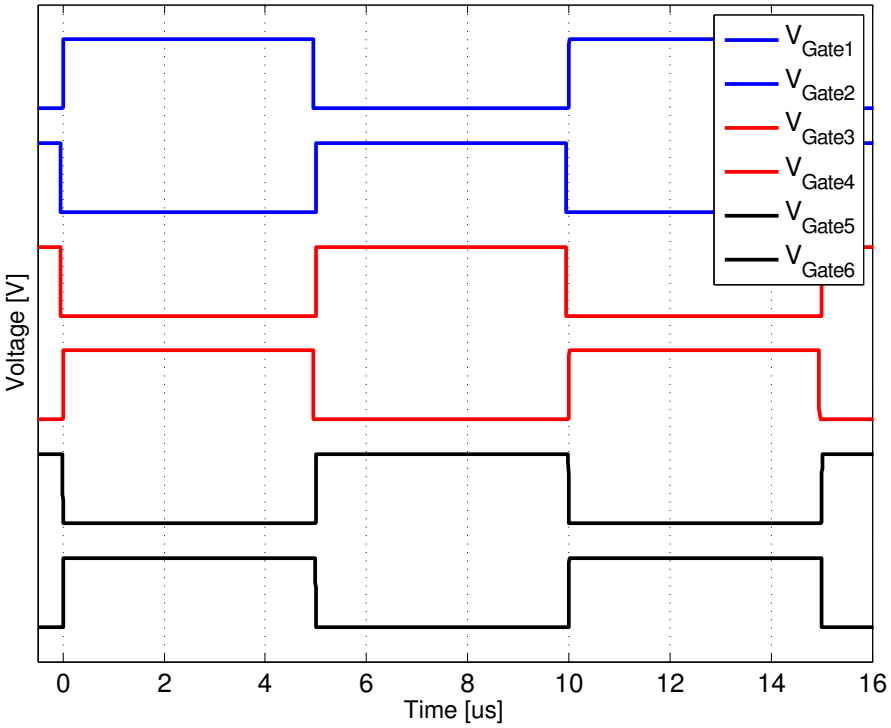

Fig. 3.5: Bipolar switching pattern in the current doubler converter

In the phase shifted pattern, two secondary switches S5 and S6 start conducting together with the switches S1 & S3 or S2 & S4. As it can be seen in Fig. 3.6, the duty cycle for rectifier switches is more than 50% because they both need to be on, during free-wheeling period, where the upper (S1 & S3) or the lower (S2 & S4) primary switches are working at the same time. On the other hand, S6 should not be turned off before S1 and similarly S5 can be turned off after S2 stops conducting.

3.4 Components selection

For choosing the appropriate rating for the semiconductor devices, a 200 % current margin and 100 % voltage margin have been selected, due to the high power application of 3 kW. To use the peak value for the voltage and the average value for the current is sufficient due to the safety margin.

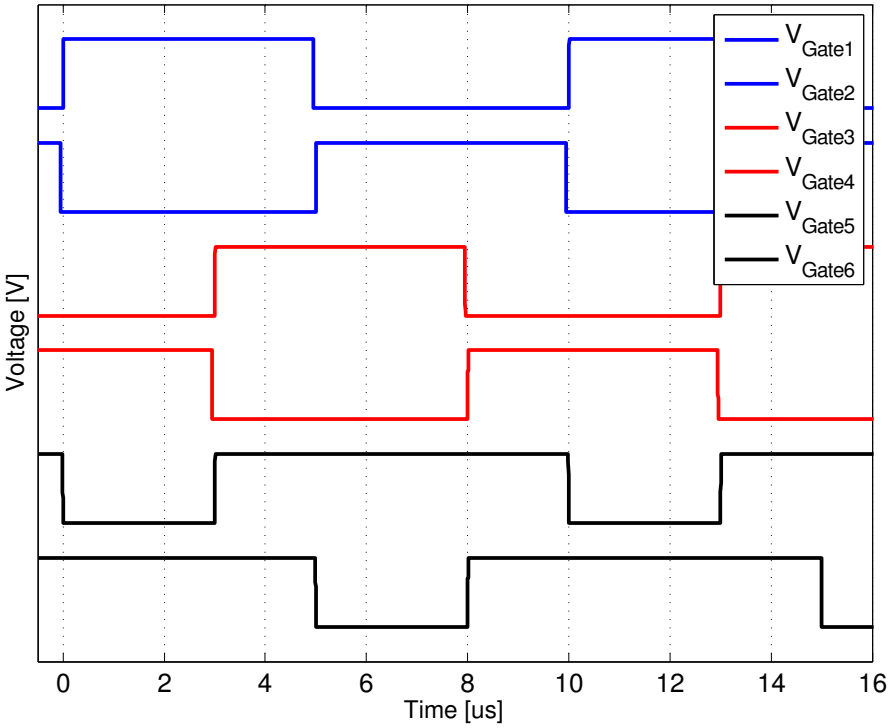

Fig. 3.6: Phase shifted switching pattern in the current doubler converter

3.4.1 MOSFET

The rated current is calculated using obtained data from the simulations in Allegro AMS with maximum power output and then imported to Matlab, where the relevant calculations have been performed. Consequently, according to the carried out calculation, the primary side rated current is I_{rated}=8.9A for both investigated topologies, full wave and current doubler converters, since they both have conventional full-bridge arrangement on the primary side. The transistors must conduct at least twice the current regarding general safety instructions. However, in this particular application, the DC/DC converter serves as a main source of power supply to the inner auxiliary network of the car, which means that if fault happens auxiliary network will be out, which is of course not allowed.

Therefore, it is a bit unsafe to use just 18 A switch, hence a switch with a higher current rating of 27 A was implemented. The voltage that the transistor must withstand is 355 V, but some overvoltage is allowed for a short time. Then the maximum voltage that the MOSFET has to withstand is 710 V. The switches that were chosen are STB57N65M5 and STW69N65M5 from ST Microelectronics for

the full wave arrangement. For the current doubler, IPW65R080 from Infenion with almost the same ratings was chosen.

The same procedure has been conducted for the secondary side, but the ratings are different. The current measured and calculated at full load equals 210A and the output voltage is 14V. The switches chosen were FDP8440 and FDP020N06B from Fairchild for the full wave topology. Even though the secondary side of the transformer in the current doubler does not experience the full load current, the switches do. Therefore, the switches that were chosen are Fairchild FDP027N08B and Vishay SUM110N06.

After having performed simulations and a relevant verification, a quanitification is carried out and the most suitable semiconductor devices are chosen according to the highest efficiency reached in the converter, which is justified in the following sections.

4

Analysis

4.1 Waveforms verification

The following chapter is devoted to the description of the operation principles of the full-bridge DC-DC converter with full wave and current doubler synchronous rectification.

4.1.1 Full wave synchronous rectification

The following analysis is performed based on the circuit shown in Fig. 3.1; different modes of operation are considered and explained by presenting waveforms obtained from the simulations with the help of Fig. 4.1 to Fig. 4.3. This case is considered to be closely related to the real one, since the transformer is not perfectly coupled, which implies having some leakage inductance in the circuit. The operation represents zero voltage switching on both sides of the transformer, which was one of the aims in the project.

Mode I: initiation of normal active power exchange

Prior to t_0, diagonal switches on both sides of the converter are turned on, which corresponds to the initiation of the active power transfer. The voltage V_{in} is immediately exerted on the transformer primary side, transferred to the secondary side with transformer's turns ratio. However, secondary voltage does not simultaneously follow the primary side, because of the negative current in the transformer due to the leakage inductance. Therefore, it requires some time to reverse the polarity of the current and to start the active power exchange.

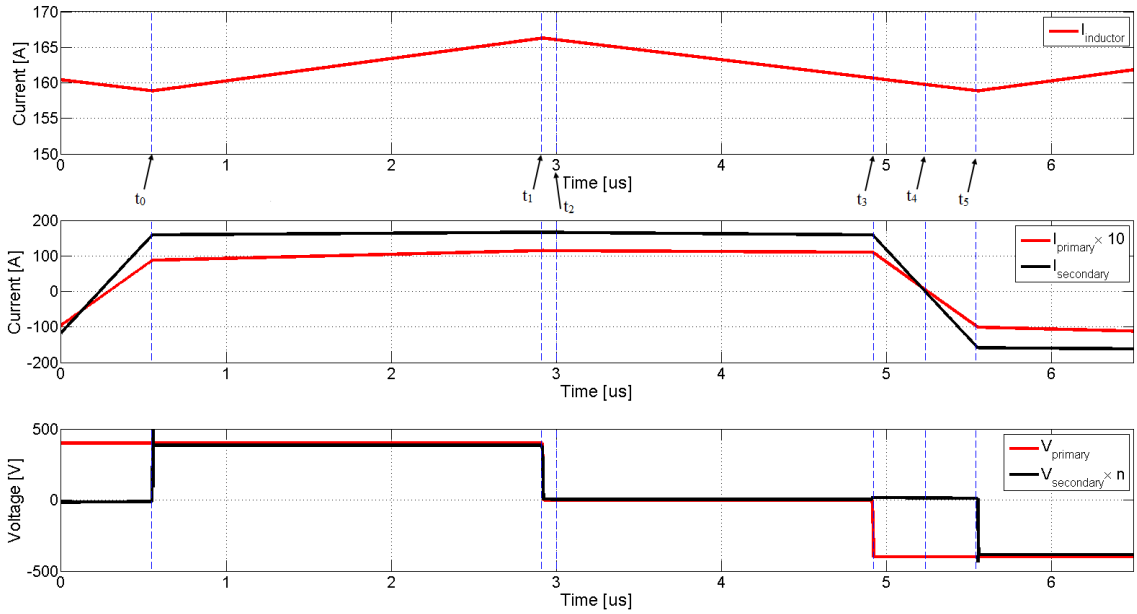

Fig. 4.1: Primary and secondary sides currents and voltages in the transformer as well as output inductor current

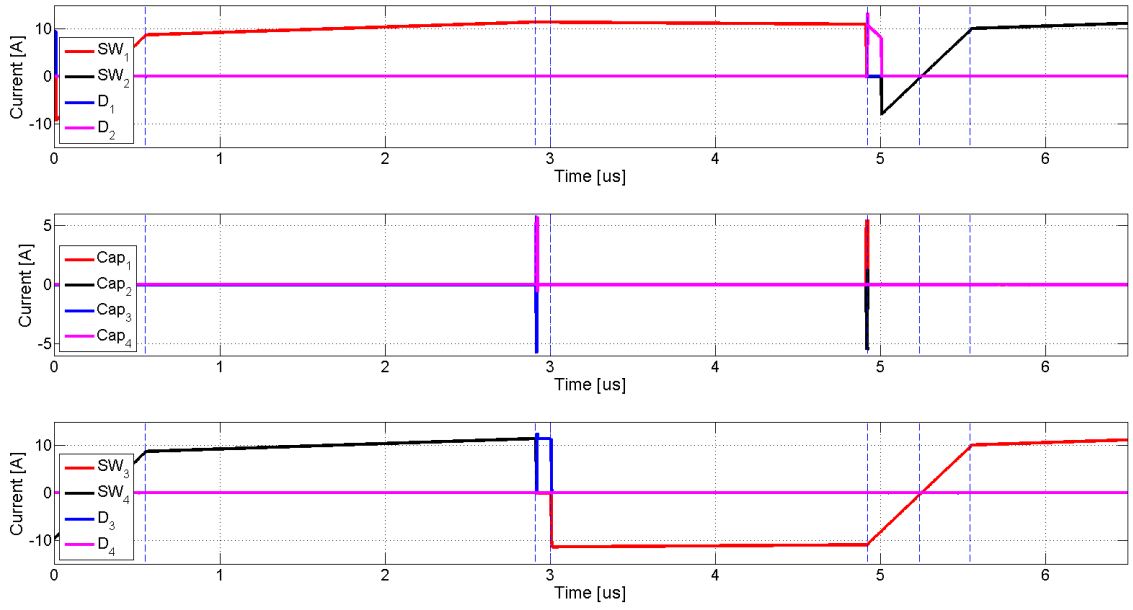

Fig. 4.2: Inverter side currents

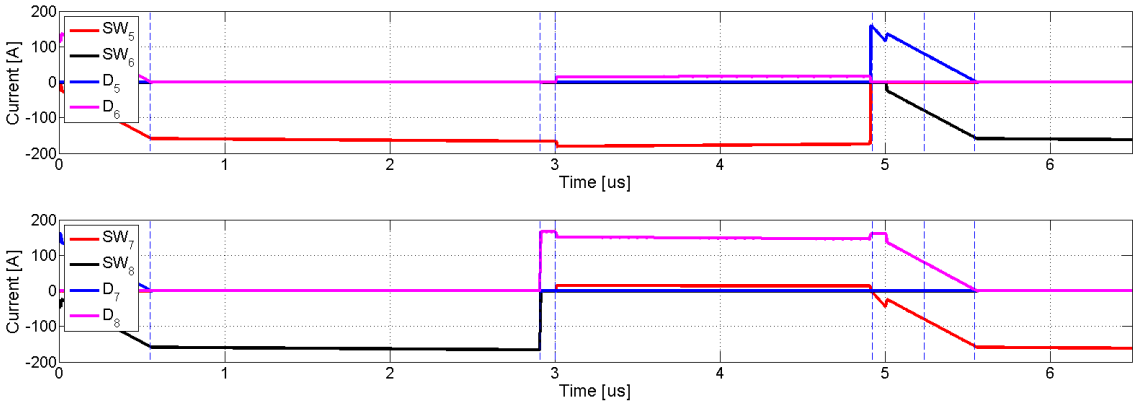

Fig. 4.3: Rectifier side currents

Mode II: (t_0-t_1) active power exchange interval

At t_0, when currents in diodes D6 and D7 have died naturally out, the secondary voltage has reached its reference value, which means that the active power transfer interval was fully initiated. Current in the transformer continues to rise, but with a smaller slope. The output inductor L_7 starts charging (current in the inductor starts to increase with a certain slope that is constituted by its inductance value and the voltage applied across it) and feeding the load with the full current. The entire ripple created by the inductor is absorbed by the capacitor C_3, allowing the load to have almost pure DC current. This process sustains when running the normal active duty cycle in the circuit.

Mode III: (t_1-t_2) transition interval

At t_1, switches S4 and S8 have been turned off, the potential of the common point swings from the upper part to the lower with the load current charging and discharging the parasitic capacitances of switches S4 and S3 respectively. This can be noticed by the observation that diode D3 started conducting. This small time interval corresponds to the transition interval (dead time between the switch operations). The voltage over both sides of the transformer ceases and reaches zero at t_1, prior to the freewheeling interval starts. At t_2, the transition of current has been ended by turning on switches S3 and S7.

Mode IV: (t_2-t_3) freewheeling interval

Since switches S3 and S7 have been turned on at t_2, the freewheeling interval

has been initiated. However, there is no energy exchange between primary and secondary sides of the transformer, which is indicated by zero voltage over it, but there is a current that is flowing in the transformer, due to some leakage inductance in the circuit. This corresponds to the output inductor discharge, hence leading to inductor current decrease. On the secondary side, switch S5 and diode D8 conduct the same full current, sharing the current between switch S7 and diode D6 respectively. At t_3, the freewheeling interval finishes because of S1 and S5 turning off, thus the next transition of the current is initiated.

REMARK

The important observation has to be noticed that there is a positive current flowing through S7, which might seem doubtful from the first sight. However, there is a coherent explanation to this phenomenon. This could be explained by the fact that the direction of the current through S7 is strongly dependant on the operating point (loading) of the converter at that particular time instant and the size of the leakage inductance of the transformer. The justification is brought down in Table 4.1. It is seen that the voltage potential over S7 is changing with respect to the load change, seen from Fig. 4.4. At some load conditions, the direction of the current flow through S7 during freewheeling interval may also change (indicated by different voltage polarity), which might seem unreasonable, but it is actually how the circuit operates.

Table 4.1: Potential over different semiconductors

New transformer model

	Case 1 *Vdc=14 V, L=nom*	**Case 2** *Vdc=13.5 V, L=nom*	**Case 3** *Vdc=14 V, L=1.5*Lnom*
diLout/dt	-3.19 A/us	-3.09 A/us	-3.18 A/us
diLp/dt	-0.36 A/us	-0.5 A/us	-0.192 A/us
diLs/dt	-5.51 A/us	-7.7 A/us	-2.96 A/us
Ptransfer	67 A	96.17 A	46.7 A
Vs1	0.207 V	0.275 V	0.144 V
Vs3	-0.207 V	-0.275V	-0.144 V
Vp	1.09 V	1.5 V	0.877 V
Vs	0.071 V	0.098 V	0.057 V
VL1	-1.505 V	-2.055 V	-1.16 V
VL2	-0.099 V	-0.135 V	-0.077 V
Vs5	-0.176 V	-0.246 V	-0.13 V
Vs7	-0.0048 V	-0.013 V	0.0041 V
Vs6	-0.836 V	-0.813 V	-0.843 V
Vs8	-1.0081 V	-1.047 V	-0.978 V
VLout	-15.013 V	-14.56 V	-14.97 V

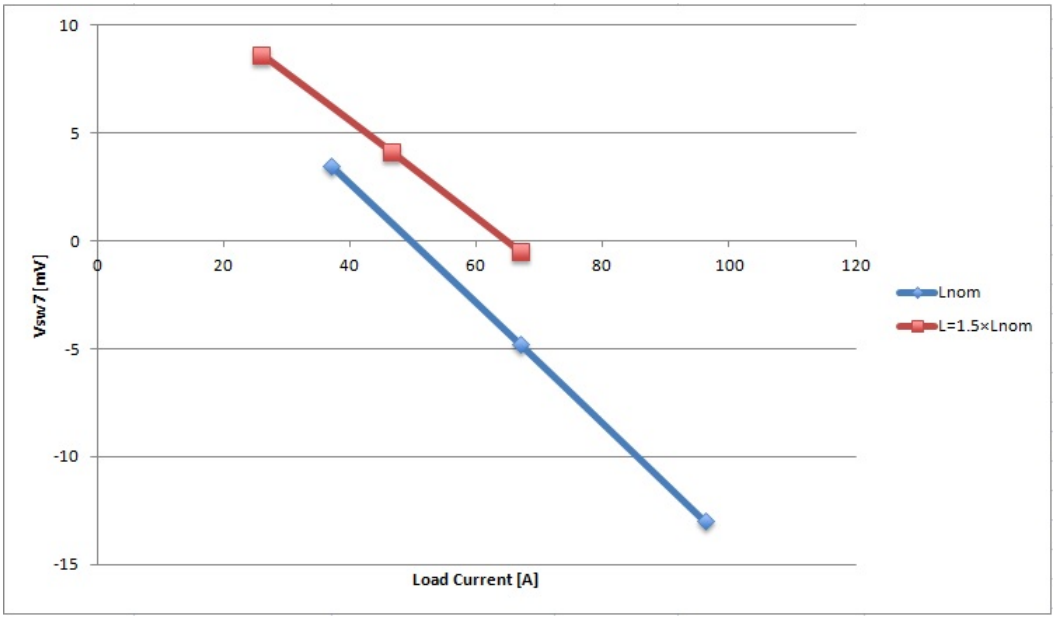

Fig. 4.4: Power transfer with different voltage level and transformer inductance values

Mode V: (t_3-t_5) transition interval

At t_4, the same principle applies as for the Mode II, but the parasitic capacitances of switches S1 and S2 start charging and discharging respectively, thus the current in the transformer starts decreasing, because of the negative voltage applied over it. Consequently, diode D2 is conducting that allows to turn on switch S2 at zero voltage over it. Once switches S2 and S6 are on, the current through diodes D5 and D8 on the secondary side die naturally out, the voltage over the secondary side becomes also negative, which corresponds to the current flow through other diagonal switches, the currents in the transformer stop severe increase, hence negative active duty cycle is initiated.

4.1.2 Current doubler synchronous rectification

This part describes different modes of operation for the full-bridge dc-dc converter with current doubler synchronous rectification. As it will be explained later, the best condition from soft switching viewpoint is using phase shifted switching pattern and incorporating leakage inductance in the transformer representation when simulating. That is why unipolar switching pattern has been used for the analytical part and a coupling factor of 0.99 is chosen to represent the leakage inductance inside the transformer. Different vertical magenta dashed-lines have been shown in Fig. 4.5 and Fig. 4.6 which separate operational modes.

Mode I: (t_0-t_1)

This mode starts from t_0 where S4 is turned off and the transformer voltages are falling to zero. Before starting this mode, S1 and S4 were conducting and the input voltage was applied to the transformer and energy was exchanging from the primary to the secondary side. By turning off S4, the stored energy in L_1 charges the capacitance of C_4 and discharges C_3 which makes D3 to conduct. Conducting D3 beside S1 prepare free-wheeling mode even before turning on S3 and results in zero voltage switching as it was mentioned in the soft switching part. By turning on S3 the current starts flowing through it and it should be considered that this current is negative according to the switch positioning.

The transformer current starts decreasing, the same as inductors currents which show their discharging behavior and results in supplying the output energy. There is no energy exchange between the two sides of the transformer in this mode.

The output current starts to free wheel through the rectifier switches. The lower switch (S6) is already on at this moment and can carry the free-wheeling current,

but S5 is not turned on yet. Since the voltage over the transformer is zero and the secondary lower switch is conducting, there is zero voltage over S5, and D5 does not need to conduct for achieving ZVS. By turning on S5 at the same time as S2 the current starts to flow through it, but this current is much smaller than S6 current which was on before.This mode of operation ends up with turning off S1 at t_1.

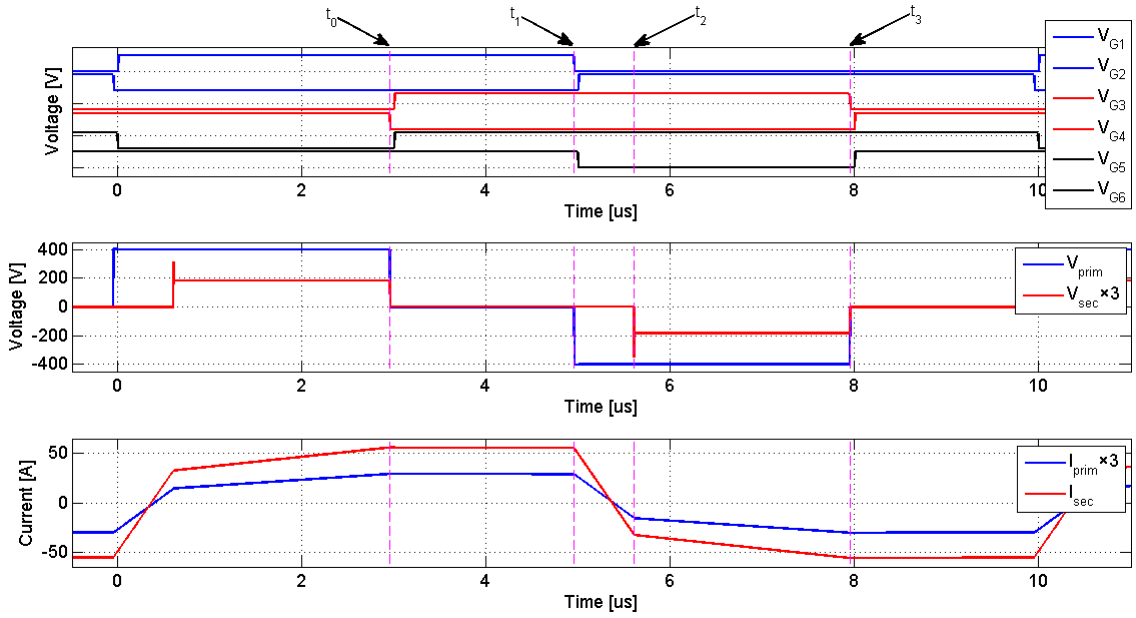

Fig. 4.5: Modes of operation in the current doubler converter

Mode II: (t_1-t_2)

There is a transition time at the beginning of this mode. At t_1 by turning off S1, the stored energy in the leakage and magnetizing inductances charge the capacitance C_1 and discharge C_2 which makes D2 to conduct. Conduction of S3 and D2 at the same time applies the input voltage on the primary side of transformer inversely, but because of conducting S5 and S6 the voltage over the secondary of the transformer is still zero. The current magnitude in both secondary switches is decreasing with a higher slope compared to the free-wheeling mode which is equal to the transformer secondary current slope. After some instants, S6 is turned off and naturally its current is falling to zero. Therefore the current flows into the anti-parallel diode (D6) and remains the secondary voltage on zero. The next event is turning on S2, so the current of D2 is moved to the anti-parallel switch (S2).

The decrease of the secondary current continues and crosses zero, then the polar-

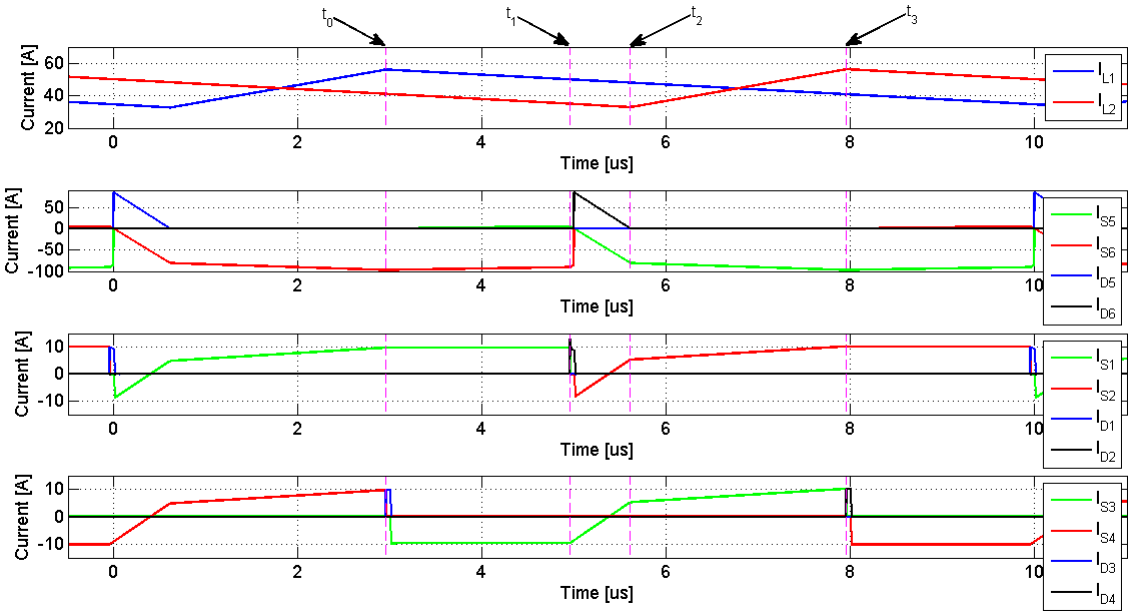

Fig. 4.6: Modes of operation in the current doubler converter

ity of the current in the transformer changes and this results in a current polarity change in S2 and S3 as well. During the whole time of this mode, the rectifier inductors currents are decreasing linearly until t_2 which is the ending point.

Mode III: (t_2-t_3)

As it can be observed, this mode is starting at the time t_2 where the current in D6 reaches zero and the transformer secondary current magnitude is equal to the lower inductor (L_2) current, which is increasing linearly. The transformer secondary voltage is trying to reach to the final value. The primary voltage is equal to the input voltage thanks to the S2 and S3 conduction. It can be said that at this mode the power exchange period starts and energy is delivered to the load from the source side until t_3 where the next free-wheeling period will be initiated and sequence of events will be repeated as it occurred in the mode I.

4.2 Switching techniques

This chapter is devoted to the description of the three cases which result in different switching behaviors. The analysis starts from the most idealized case, utilizing bipolar switching with no leakage inductance in the transformer (coupling factor = 1). Next case will be unipolar switching pattern with the same coupling factor.

The last case corresponds to the unipolar pattern with added external elements such as resonant components. In this case the leakage inductance is represented by changing the coupling factor of the transformer to 0.99.

4.2.1 Full wave synchronous rectification - hard switching

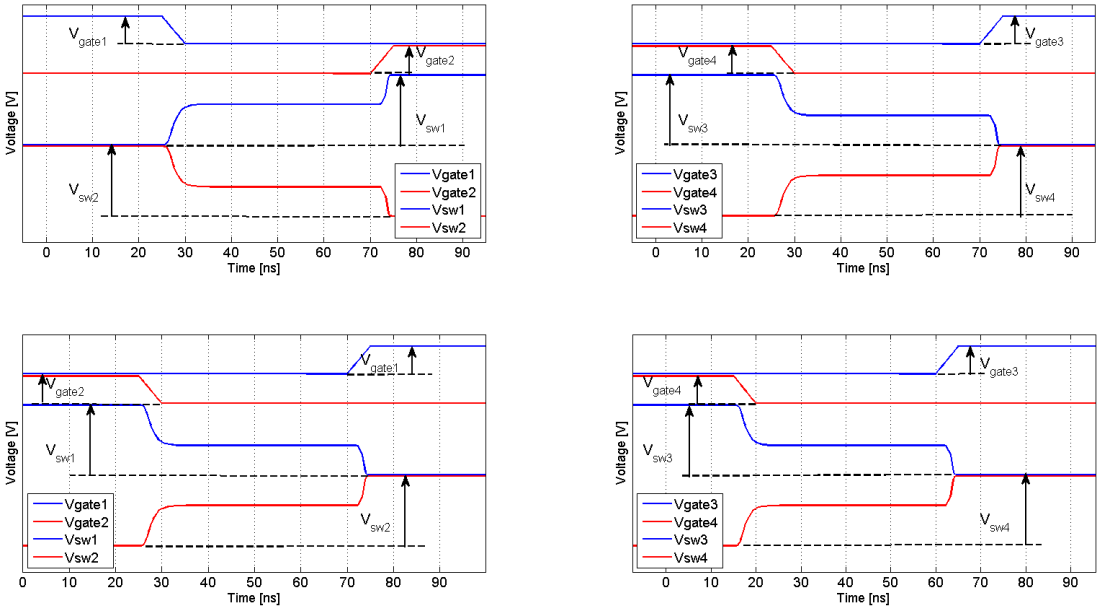

Fig. 4.7: Bipolar hard switching for conventional DC/DC, primary side switches

As it is depicted in Fig. 4.7 and Fig. 4.8 turn on of the switches in the primary side do not satisfy zero voltage condition, therefore switches are forced to commutate the full load current by the control device, resulting in high voltage stress over the switch while turning on, hence increased switching losses. Furthermore, turn-on high voltage levels induces a severe switching noise phenomenon known as the Miller effect (increase in the equivalent input capacitance due to amplification of the effect of capacitance between the input and output terminals) which is coupled into the drive circuit, leading to significant noise and instability.

Nevertheless, the same is happening on the secondary side switches, which is understandable because primary and secondary sides are coupled through a transformer. Everything that is happening on the primary is reflected to the secondary sides, but with a certain delay, due to the leakage inductance in the transformer, if it is not perfectly coupled.

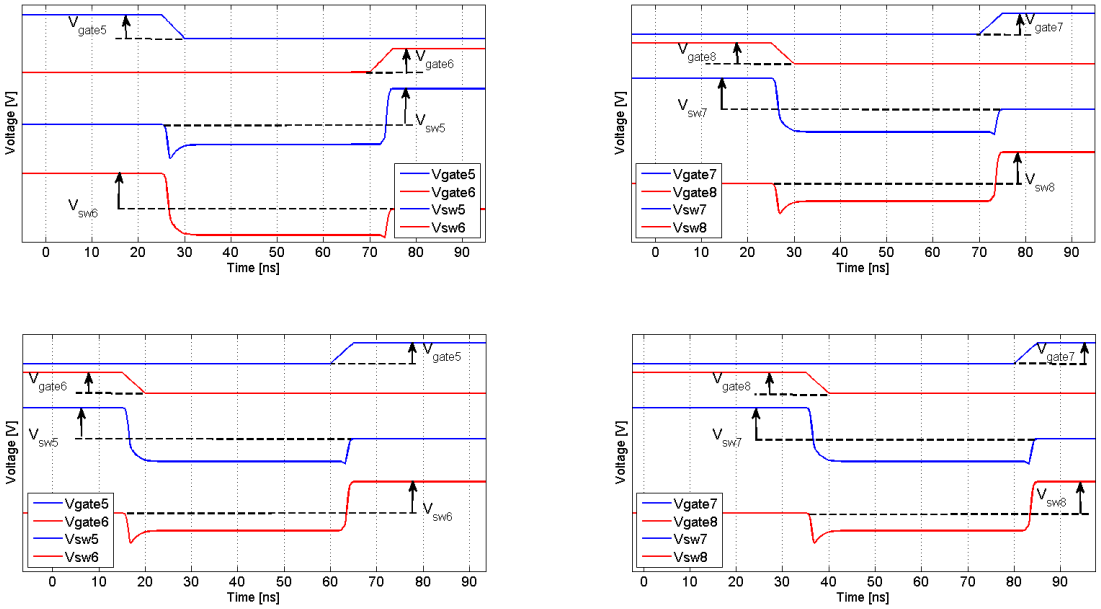

Fig. 4.8: Bipolar hard switching for conventional DC/DC, secondary side switches

The overlap that is created during voltage/current transition causes energy loss and it may be minimized by increasing di/dt and dv/dt. However, quick changing of di/dt and dv/dt will lead to EMI generation; consequently they must be optimized to avoid EMI issues as much as possible. These rise/fall times may be reduced by introducing dissipative passive snubber circuits, and they are usually implemented in real power devices. Meanwhile, those snubbers transit switching loss and stress into their circuit, but do not decrease the total losses. Therefore, introducing only snubber circuits is not the best alternative; further analysis is to be performed. Thereafter, the unipolar switching on the basis of UCC28950 from TEXAS Instruments is implemented and the converter's performance analyzed, which is depicted in Fig. 3.6. This switching pattern is applied to justify if soft switching is achievable and sufficient for this particular configuration.

As it is seen from Fig. 4.9 and 4.10, just implementing unipolar switching pattern does not guarantee soft switching. The active leg switches turn on at maximum voltage over it, conducting the full load current. It has to be avoided, if there is a need of reducing the switching losses and stress over the semiconductor devices. The secondary side switches behave almost the same as the primary, but in this case, the active leg switches and the passive leg upper switch turn on in a hard way as it is seen from the 4.10, when there is a voltage applied over them, but the voltage is quite low and it is negative. To overcome this action the transformer's leakage or external inductances and MOSFET's parasitic capacitances are effec-

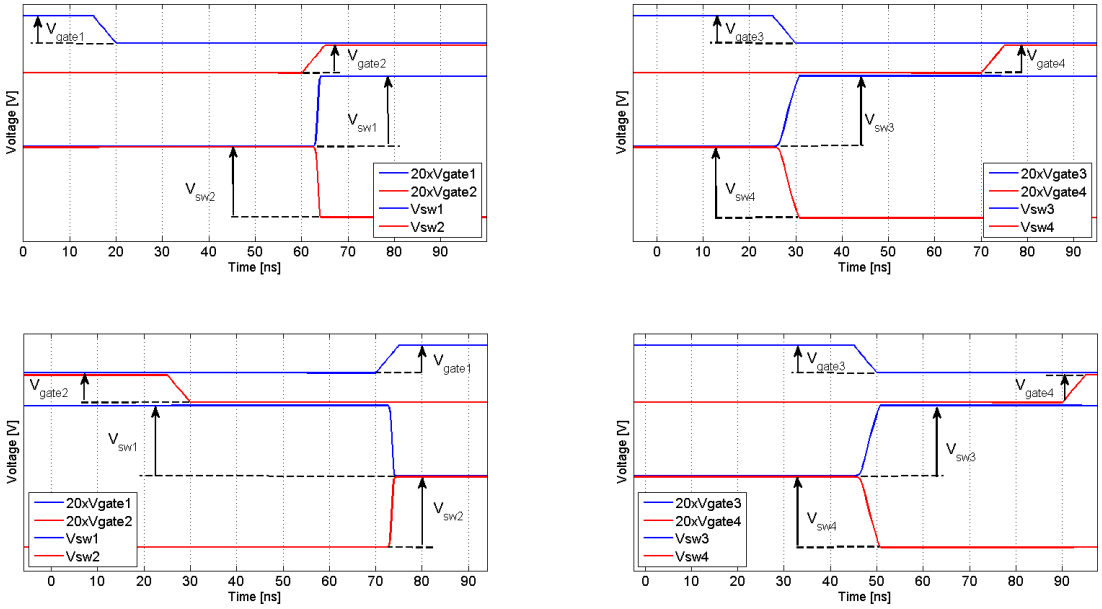

Fig. 4.9: Phase-shifted hard switching for conventional DC/DC, primary side switches

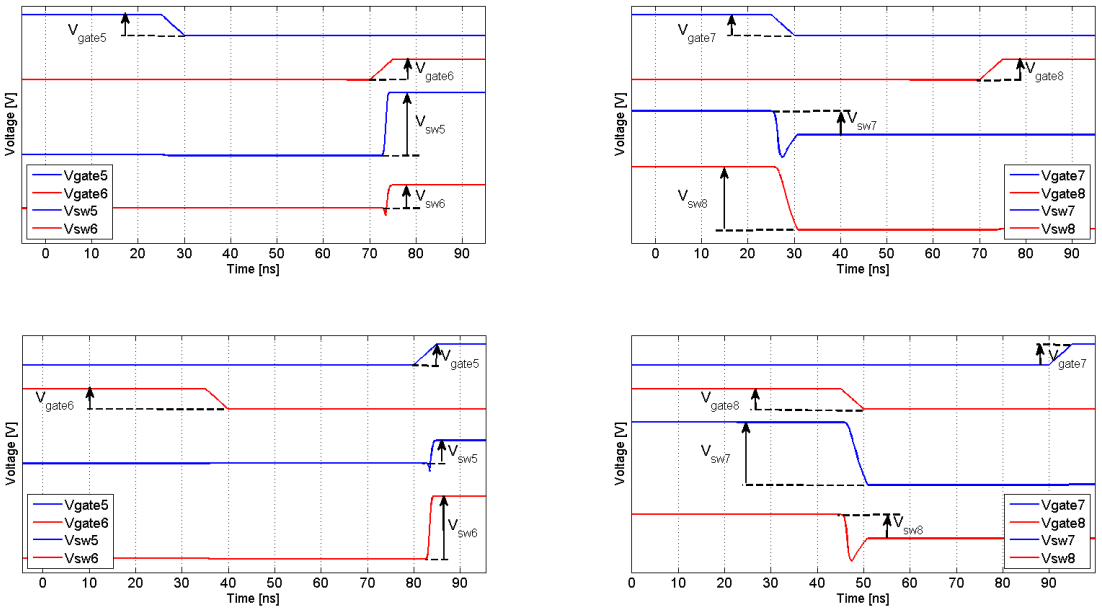

Fig. 4.10: Phase-shifted hard switching for conventional DC/DC, secondary side switches

tively utilized to offer the soft switching possibility.

Here it may be observed that during the transient, there is an undershoot of the voltage over the switches in the passive leg, which is due to the reverse recovery of the diodes, connected in parallel.

In order to achieve zero voltage switching over the switches, move on to adding some external inductance, additionally changing the coupling factor of the transformer to introduce leakage inductance that is usually present in the real transformer. The conducted experiments and simulated waveforms are presented in the next section.

4.2.2 Current doubler synchronous rectification - hard switching

As it can be seen in the simulation results in Fig. 4.11 and Fig. 4.12, all switches are turned on when the voltage over them are not zero. So, there is no soft switching in any switches during turn-on duration. The upper parts of the each subplot show the gate pulse voltages in different switches and the lower parts show the voltages over the switches.

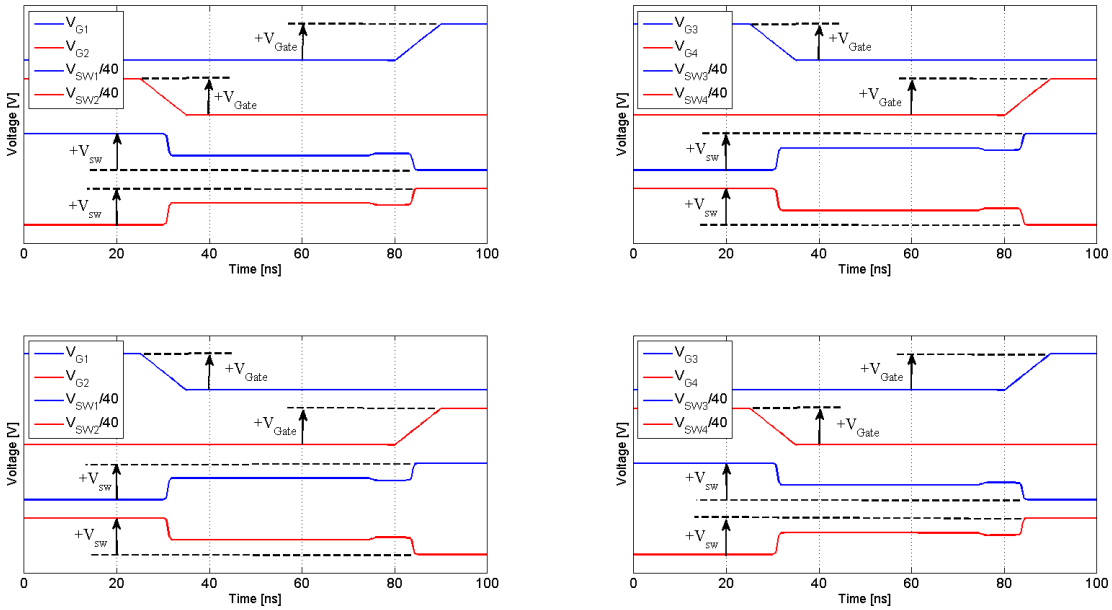

Fig. 4.11: Hard switching in the primary side switches of the current doubler converter in case of bipolar switching pattern

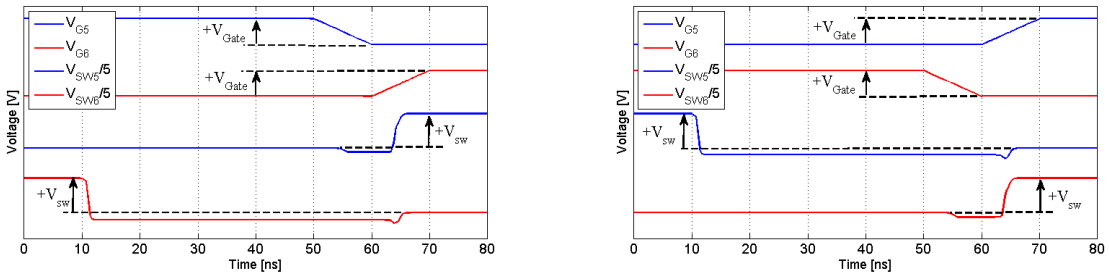

Fig. 4.12: Hard switching in the secondary side switches of the current doubler converter in case of bipolar switching pattern

In order to solve the hard switching problem, unipolar switching pattern as the second case has been performed and results have been compared with previous case. The hard switching problem during turn-on is removed in four switches (3-6), but there are still some problems in switch 1 and 2 which are located in active legs. Zero voltage switching is not achieved yet in these two switches even with phase shifting pattern. All switching waveforms can be seen in Fig. 4.13 and Fig. 4.14.

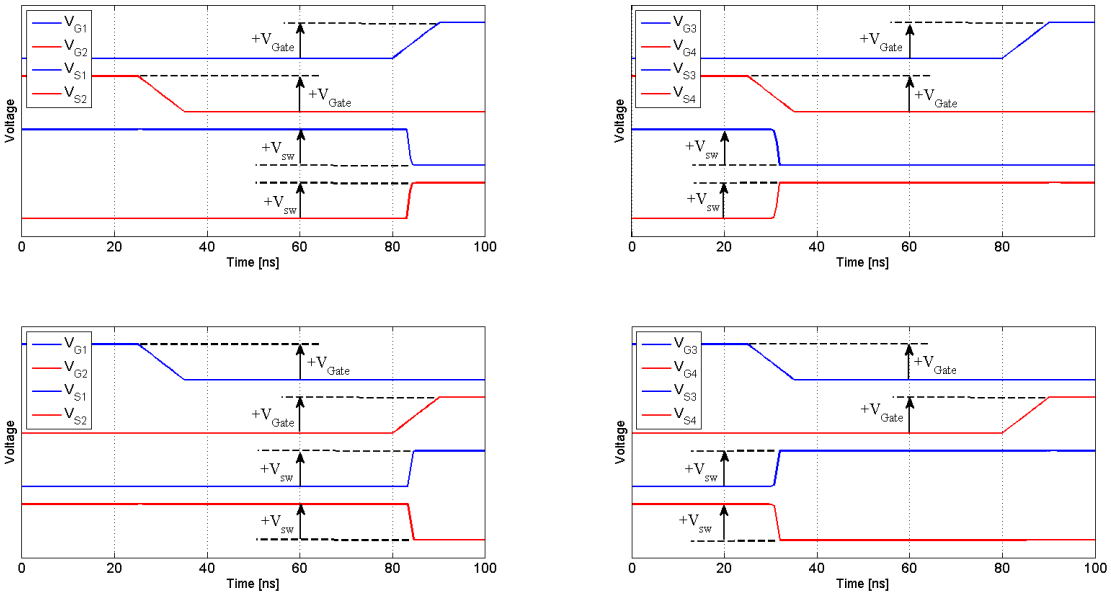

Fig. 4.13: Hard switching in the primary side switches of the current doubler converter in case of phase shifted switching pattern

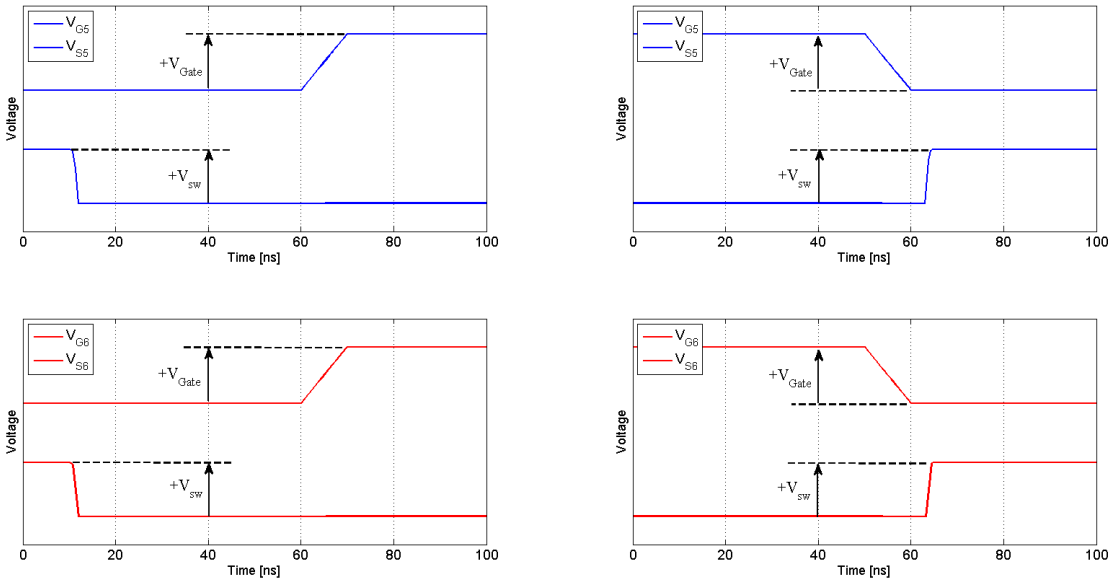

Fig. 4.14: Hard switching in the secondary side switches of the current doubler converter in case of phase shifted switching pattern

4.2.3 Full wave synchronous rectification - soft switching

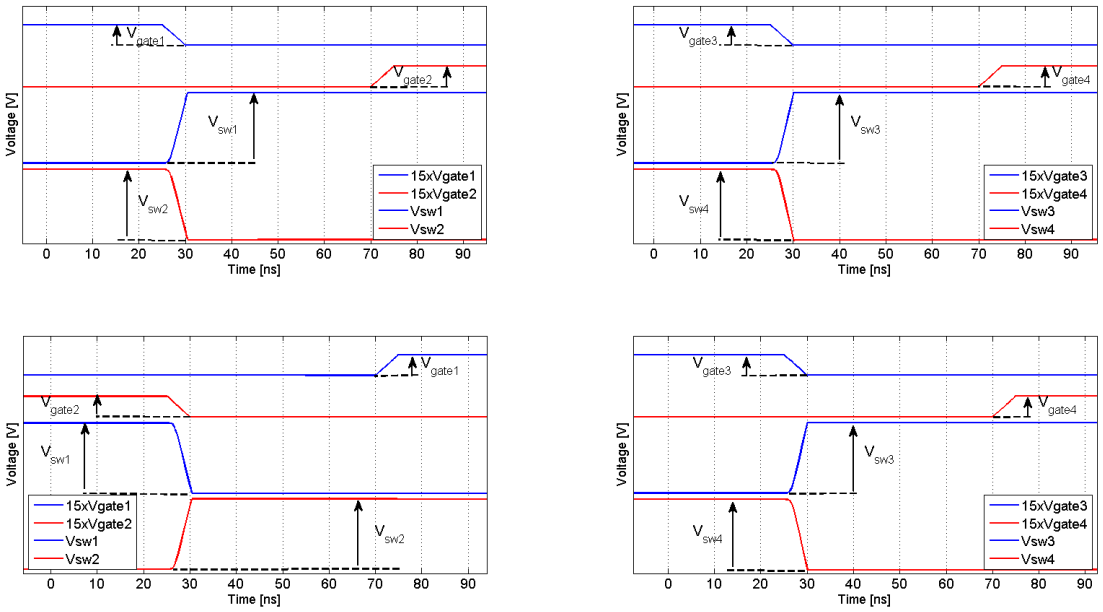

Fig. 4.15: ZVS switching with phase-shifted switching pattern for full wave DC/DC, primary side switches

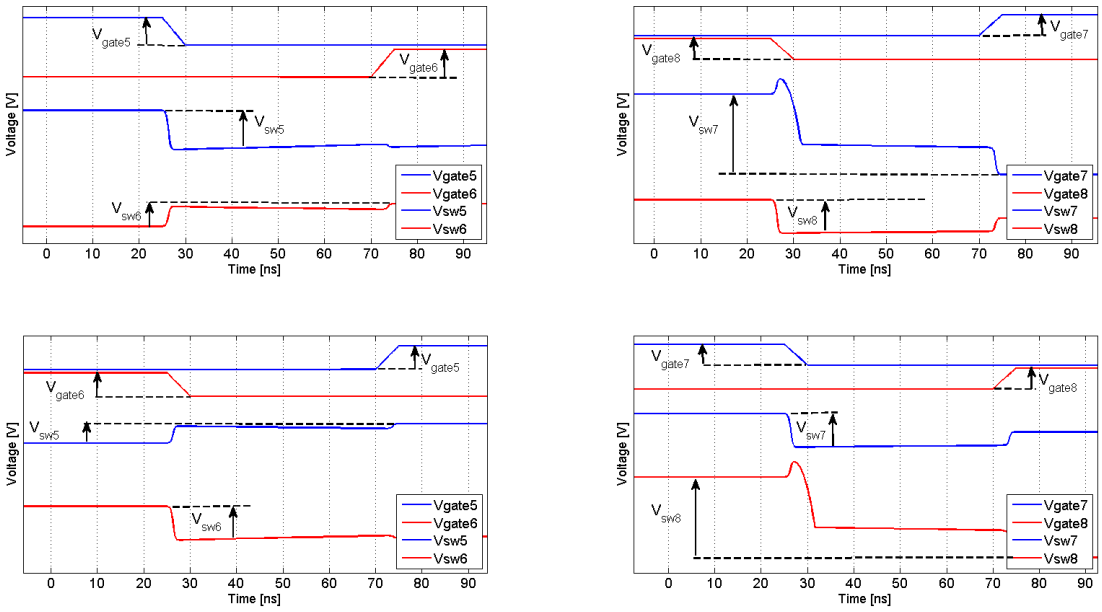

Fig. 4.16: ZVS switching with phase-shifted switching pattern for full wave DC/DC, secondary side switches

According to the performed simulations and obtained waveforms ZVS is successfully achieved on the primary as well as on the secondary side switches, which can noticed in Fig. 4.15 and Fig. 4.16. This was achieved by modeling the power semiconductor devices with parallel diodes, parasitic capacitances, and leakage transformer's inductance of 1.5% and external secondary side resonant inductance of 120 nH.

All parasitic capacitances in the circuit including winding and heat sink capacitance have been lumped together as a switch capacitance. For example, when the switch S4 turns off, the inductor current charges capacitance C_4 and discharges capacitance C_3 until the voltage across C_3 reaches zero, and the body diode D3 conducts current and after that the switch S3 turns on with zero voltage and the inductor current freewheels through the switch instead.

All other switches operate according to the same principle described, but utilizing different magnetic energy storages for different converter's legs. To implement a proper switching transition, the inductor energy stored at the start of the transition must be large enough to completely charge the switch capacitance from the initial to the final voltage V_{sw}.

In the meantime, if the delay time determined is too high, the interval when

the voltage across the switch is zero would be missed, which would lead to the capacitance being repeatedly recharged and the possibility of zero voltage switching would be lost. Therefore, this has to be avoided by using proper duty cycle and gate drive delay time determination. Another point corresponding to the proper circuit operation would be body diode conduction prior to turn-on of the switches.

4.2.4 Current doubler synchronous rectification - soft switching

There are several ways to achieve zero voltage switching. One method which was used above was changing the switching pattern that was mentioned as the second case at the beginning of this chapter. Thanks to the phase shifting pattern the hard switching problem was solved partially but not in all switches. Another solution was using transformer leakage inductance. The next step is changing the coupling factor to a value less than one which represents the leakage inductance in the transformer. Leakage inductance can be also be modelled by putting an inductance in series with the primary winding of transformer.

It can be observed that leakage inductance will help to achieve zero voltage switching in all switches during turn on and off. The waveforms are depicted in Fig. 4.17 and Fig. 4.18. It should be mentioned again that the upper parts of the each subplot show the gate pulse voltage in different switches and the lower parts show the voltage over the switches.

A deeper study is needed on the zero voltage switching in order to undertand how it is achieved in some conditions and not in the other. For this purpose two transition points have been chosen and are depicted in Fig. 4.19 and 4.20 by vertical dashed-lines in magenta color.
The first point is corresponding to the instant at which S4 turns off but S1 is still conducting. Indeed, the power transfer is stopped here and the free-wheeling period starts by turning on S3. According to the graphs, there is a delay between turning off S4 and turning on S3. At this instant after turning off S4, the stored energy in L_1 charges the capacitance of C_4 and discharges C_3 which makes D3 to conduct. S1 and D3 are on and the free-wheeling mode has started. Conduction of D3 prepares a zero voltage over S3 and then by turning on S3, current will flow through it under soft switching conditions. It should be mentioned that the current flowing through the switch is considered negative according to the switch positioning. The same story can happen while turning off S3 and turning on S4. In this case D4 is conducting first and then S4 turns on under zero voltage condition.

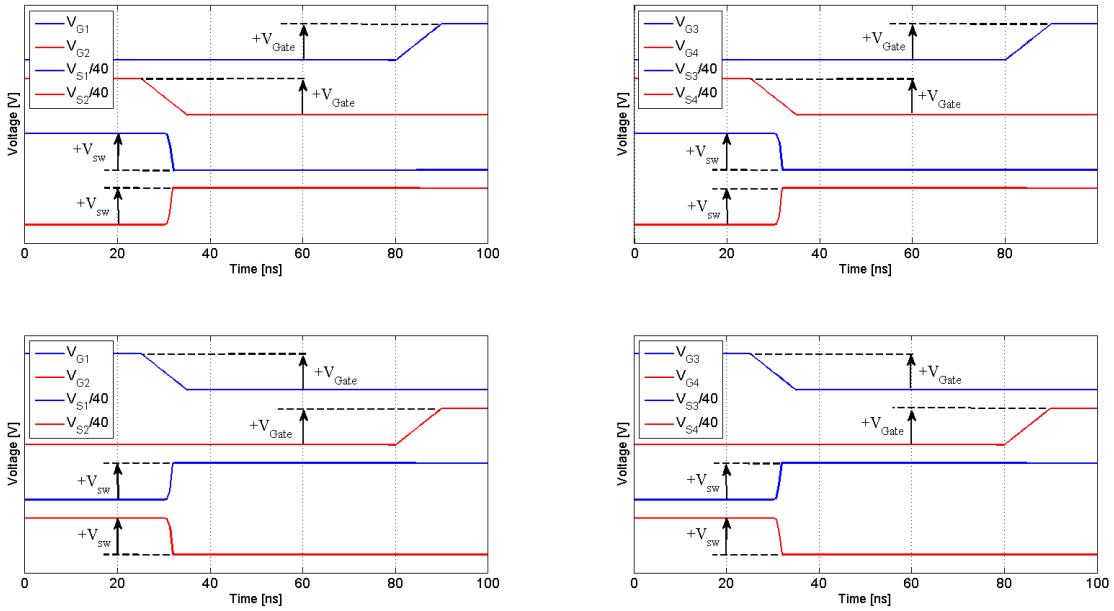

Fig. 4.17: Zero voltage switching in the primary side switches of the current doubler converter in case of phase shifted switching pattern and coupling factor=0.99

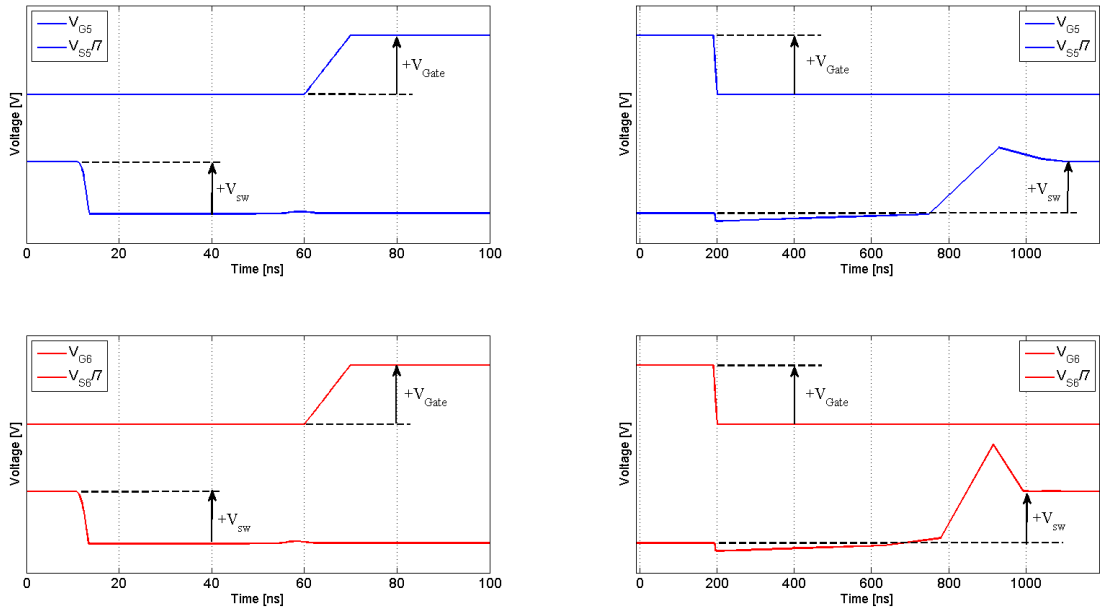

Fig. 4.18: Zero voltage switching in the secondary side switches of the current doubler converter in case of phase shifted switching pattern and coupling factor=0.99

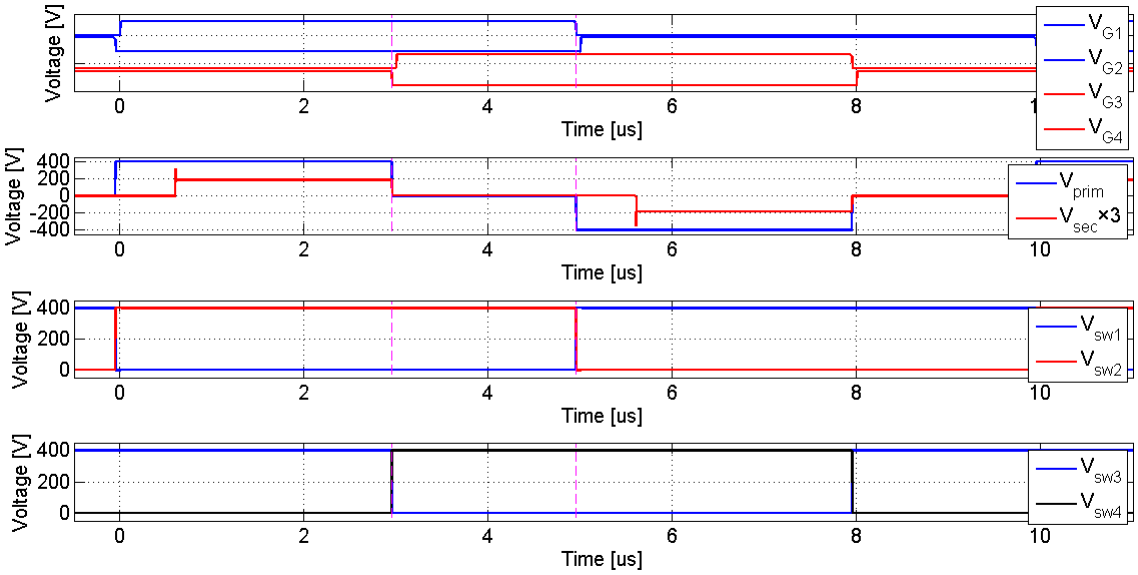

Fig. 4.19: Zero voltage switching behavior analysis in the current doubler converter

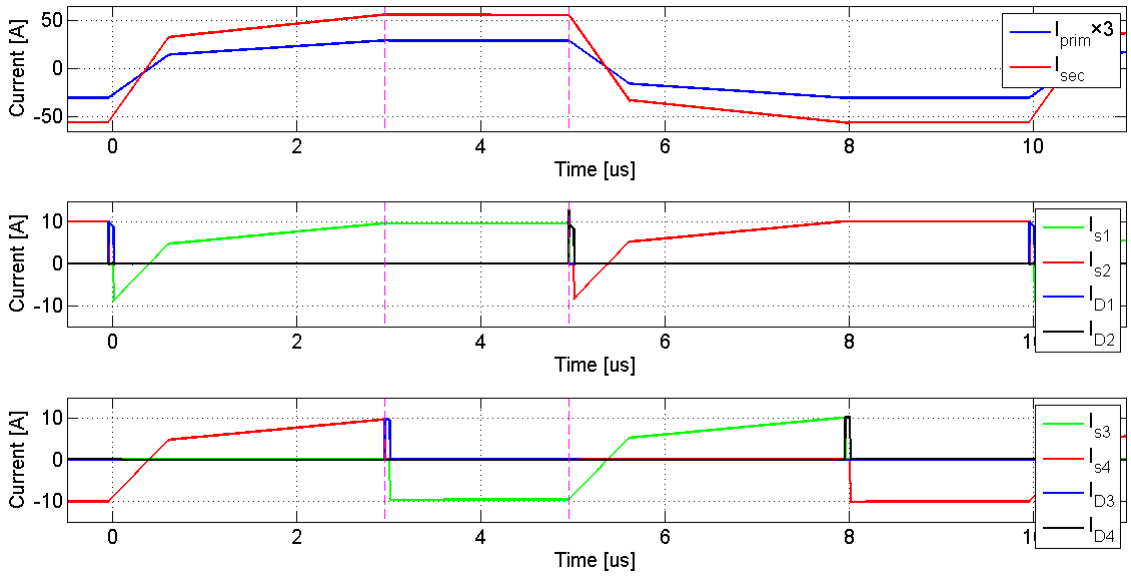

Fig. 4.20: Zero voltage switching behavior analysis in the current doubler converter

The other magenta dashed-line corresponds to S1 turning off instant. At this point the free-wheeling period is over and S2 will be on though. At this transition time the energy which is stored in the leakage and magnetizing inductance charges the capacitance C_1 and discharge the C_2 and makes D2 to conduct. Another power

exchange period between the primary and secondary sides of the transformer starts at this point. After some instants the gate pulse voltage is applied to S2 and it will be turned on and the current transferred from diode to the anti-parallel switch. Again thanks to the anti-parallel diode there is a zero voltage switching over S2 since it will be turned on when its voltage is zero. The same sequence of events will occur between turning off S2 and turning on S1.

As it can be seen and was mentioned before, S6 should not be turned off before S1 since it is needed to have both rectifier switches on during the free-wheeling period. There is the same story for S5 and S2 during next free-wheeling time interval. It was seen before that in case of having no leakage inductance there was not any soft switching in the active leg switches during turn on. For the comparison purpose, the waveforms are obtained and analyzed at the same instants as previous case and are shown by magenta dashed-lines in Fig. 4.21 and 4.22. The first point is showing the same behavior as before. When S4 is turned off, the stored energy in secondary inductor charges and discharges C_4 and C_3 and D3 starts conducting. So the voltage over the transformer and S3 voltage fall to zero, and then by turning on S3 zero voltage switching will be achieved. The story is different for the next instant where the active leg switch S1 is turned off. Because of not having any stored energy in the leakage inductance, C_1 and C_2 are not charged and discharged, D2 does not conduct and the voltage over the other active leg switch S2 stays constant at the input voltage value. Turning on S2 while it has the maximum voltage is called hard switching which results in high switching losses.

This interval continues until turning off S6 which completes the free-wheeling mode. The current flows through the secondary side of the transformer and primary side subsequently. Since S3 is still turned on, the primary current which is negative goes through it. This negative current should close the circulation loop and there is no way except passing through D1. With turning on S2 the current moves from D1 to S2.

As it was explained before when there is switching in one of the active leg switches, the energy in the leakage and magnetizing inductances charge and discharge the parallel capacitors and forces the anti-parallel diode to conduct which makes zero voltage switching to take place in the related switch. Since this stored energy is not big, there is a limited time to achieve soft switching. There is a time between turning off S1 and turning on S2 which is called dead time. This time can be calculated according to the characteristics of the switch. In the last simulations, this time is set to 45 ns. In Fig. 4.23 it is obvious that this time has been increased in order to see how it affects the soft switching operation.

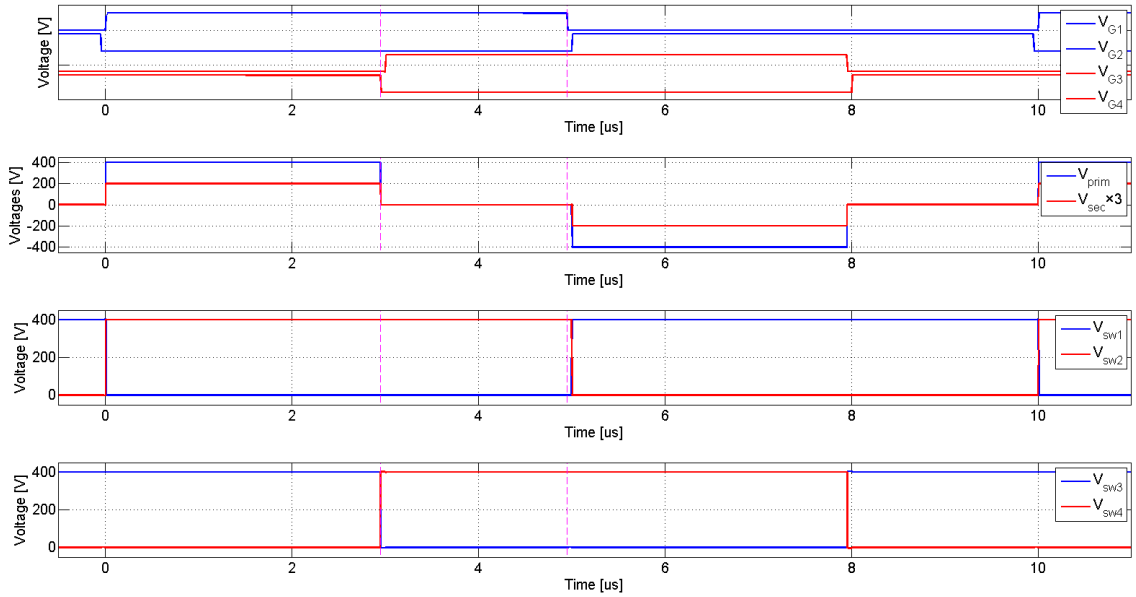

Fig. 4.21: Hard switching behavior analysis in the current doubler converter

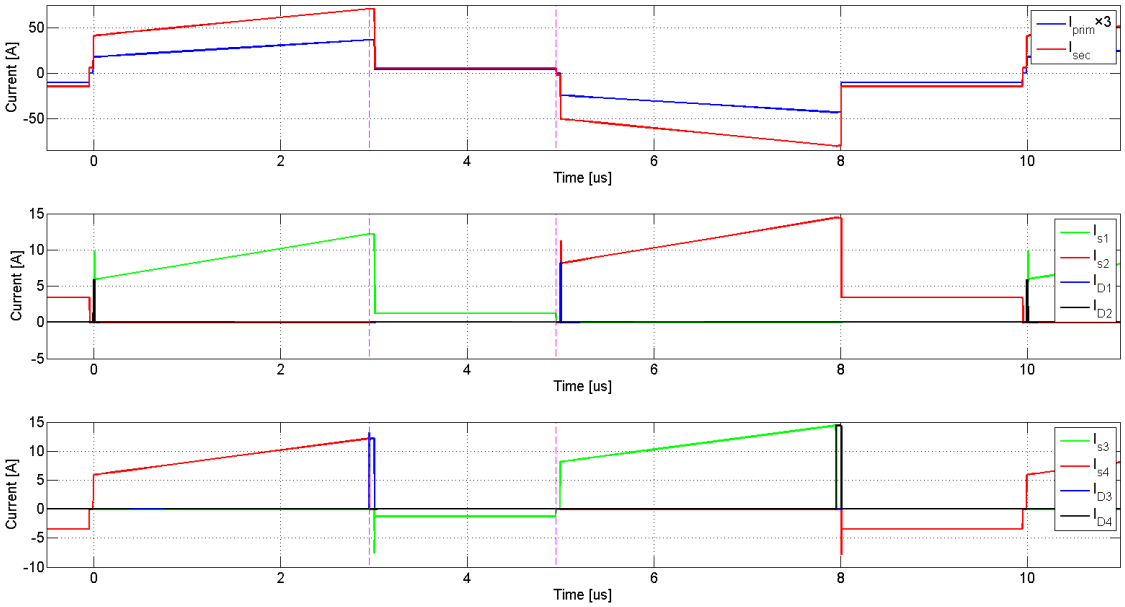

Fig. 4.22: Hard switching behavior analysis in the current doubler converter

When S1 is turned off, the energy charges and discharges the capacitors, D2 conducts and the voltage over S2 goes to zero. Since this energy is not that much big

the current through D2 decrease to zero after a while. On the other hand, S3 is on and its free-wheeling current closes the loop with D1 (The green curve which is magnified 5 times higher). Therefore, the voltage over S2 is back to the input voltage and the voltage over S1 reaches to zero. Under these circumstances if S2 turns on the switching will happen under the maximum voltage and this means zero voltage switching opportunity is lost.

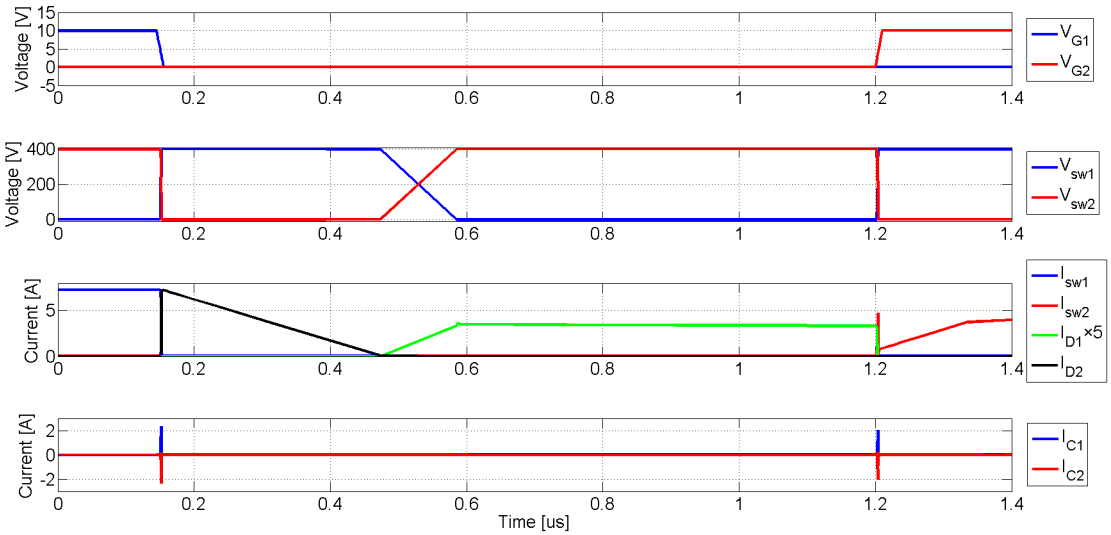

Fig. 4.23: Limited range for soft switching in case of having longer dead band in the current doubler converter

In the case of switching in one of the passive leg switches this problem does not occur since there is a bigger source of energy in the output filter which can help to achieve soft switching even with high dead band between S3 and S4 turning on and off. Indeed the anti-parallel diode can conduct until the related switch is turned on.

4.3 Loss determination

The following chapter is devoted to the determination of losses in the converter and the choice of appropriate transformer for the particular application being described in the project. The transformer design procedure and loss calculation script have been conducted and implemented in Matlab.

4.3.1 Transformer design procedure

The design of a transformer is quite cumbersome and complicated, but at the same time highly required, since the selection and design of magnetics can affect the selection and cost of all the other power components of the converter, besides dictating the overall performance and size of the converter itself [3]. The design must be carried out carefully so that the losses in the transformer are minimized. The transformer's loss can be divided into mainly copper and core losses, which are quantified and investigated in the proposed topologies of the project.

The procedure started with the determination of number of turns, since there are two or more windings, depending on the application, that have to be designed. When determining the number of turns on the primary side, one must bear in mind the magnetic flux density of the material to be used, so that the core would not be saturated, since the number of primary turns also determine the peak flux density in the core $\hat{B}_{core}$.

Consequently, the primary number of turns or flux can be determined with the help of Faraday's law,

$$e(t) = N\frac{d\phi}{dt} \tag{4.1}$$

$$\Rightarrow V(t) = N\frac{dB}{dt}A_m \tag{4.2}$$

$$B = \hat{B}cos\omega t \Rightarrow V_1(t) = N_1 A_m \frac{d\hat{B}}{dt}cos(wt) \tag{4.3}$$

$$\Rightarrow V_1(t) = N_1 A_m \omega B sin(wt) \tag{4.4}$$

$$\Rightarrow V_1 = N_1 A_m \omega B_{core} \tag{4.5}$$

The magnetic flux is given by

$$\Phi = A_m \hat{B}_{core} \tag{4.6}$$

where V_1(t) is the time-varying voltage on the primary side, A_m is an effective area of the core, $\frac{d\phi}{dt}$ is the time derivative of the magnetic flux in the core.

Inserting (4.6) into (4.2), gives

$$\int_0^{DT_s} V_1 dt = N_1 A_m \int_{-B_{core}}^{B_{core}} dB \tag{4.7}$$

The voltage applied over the primary side, when there is an active power transfer interval, is V_1, which is the input voltage. This voltage will create the peak flux density $\hat{B}_{core}$ in the transformer, which will be changing from negative to positive peak flux density, since this work deals with bidirectional operation of the full-bridge converter. This results in the following relation,

$$\Rightarrow N_1 = \frac{V_d D T_s}{2 A_m \hat{B}_{core}} \tag{4.8}$$

According to the (4.7), the peak flux density also depends on the input voltage that is applied over the transformer. Therefore, by changing the duty cycle DT_s the peak flux density in the core $\hat{B}_{core}$ or N_1 will also be changing, depending on the method through which it was calculated.

In order to define the appropriate core for the transformers, the maximum input voltage and the maximum duty cycle is considered.

$$\Rightarrow N_1 = \frac{V_{d,max} D_{max} T_s}{2 A_m \hat{B}_{core}} \tag{4.9}$$

However, by changing the duty cycle, the maximum flux density will change, and that will result in a smaller core loss respectively.

Two different ways to choose appropriate transformer's size have been implemented:

- define the number of turns, calculate flux levels and then check if they occur in the core or not;
- define flux levels, calculate number of turns and then check if they fit in the core or not.

An important observation seen from (4.9) that has to be known is that increasing the number of turns on the primary side the peak flux density will decrease respectively. Therefore, the core losses will decrease, however copper losses will increase. Apparently, there is always a trade-off between core and copper losses. Ideally, transformer loss should approximately split equally into core and copper losses, but in practice it is hardly achievable, hence the balance between them has to be maintained and the difference that results in the smallest deviation would guarantee the most efficient transformer utilization. In applications, where the transformer is under heavy load conditions, a design with larger core-losses and smaller resistive losses could be favourable for example.

In order to calculate the cross-sectional area of the wiring, one must know the RMS currents on the primary and the secondary sides of the transformer, which are found with help of the fundamental equation described in [2]. Since the operating frequencies used in this project are quite high, in order to reduce the skin and proximity effects losses in conductors Litz wire is utilized. It consists of many thin wire strands, individually insulated and twisted or woven together, following one of several carefully prescribed patterns often involving several levels.

Since we have relatively high currents in the transformer, a Litz wire with $0.94mm^2$ is used. In the project two different current densities have been chosen, 3 A/mm^2 and 4 A/mm^2. This was done in order to see the difference in the copper loss and identify the discrepancies. They were mounted in a bundle in order to withstand those high currents and the number of wires in the bundle was calculated according to.

The number of wires in the bundle for the primary side of the transformer

$$X_{pri}bundledwires = \frac{I_{pri,rms}}{JA_{litz}} \tag{4.10}$$

where J is the current density in the wire.
Now the diameter of the bundled conductor can be determined accordingly

$$A_{1,bundle} = X_{pri}A_{litz} \tag{4.11}$$

The number of wires in the bundle for the secondary side of the transformer is

$$X_{sec}bundledwires = \frac{I_{sec,rms}}{JA_{litz}} \tag{4.12}$$

Consequently, the diameter of the bundled conductor can be determined accordingly

$$A_{2,bundle} = X_{sec}A_{litz} \tag{4.13}$$

Furthermore, the total winding area can now be determined, which is carried out as following and justification, if it fits in the core or not, is performed as well. The copper filling factor is assumed to be k_{cu}=0.5, and the total winding area could be found accordingly.

$$A_{winding} = \frac{A_m 1,bundleN_1 + A_{2,bundle}N_2}{k_{cu}} \tag{4.14}$$

Core loss determination

The core loss in the transformer is due to the physical behavior of the magnetic material, which the core is made of. They are basically called hysteresis loss and eddy currents loss. It is demanded that the power loss in the transformer core should remain even at high frequencies. The ferrites are usually preferred material when it comes to define the core. According to Undeland book, the core losses per unit weight or per unit volume can be expressed as:

$$Corelossdensity = k \times f_{sw}^{a} \times (\triangle B_{max})^{b} \tag{4.15}$$

The core loss density must be scaled in terms of flux density and frequency, where switching frequency f is given in kHz and B is the peak flux density in T, k depends on the type of the material. The losses are closely proportional to the switching frequency (a=1) and to the square of the flux density (b=2) for ferrite materials.

Copper loss determination

In order to calculate the copper loss in the transformer, one must determine the length of one L_{turn} turn that could be found in the core datasheet. Therefore, having the number of turns of the windings, one can define the total length of the conductors in the primary and secondary sides. Consequently,

$$L_{pri,wind} = L_{turn}N_1; L_{sec,wind} = L_{turn}N_2 \tag{4.16}$$

The next step is to calculate the resistance in the wires on each side of the transformer, which is given by

$$R_1 = \frac{\rho_{cu} L_{pri,wind}}{A_{1,bundle}} \tag{4.17}$$

$$R_2 = \frac{\rho_{cu} L_{sec,wind}}{A_{2,bundle}} \tag{4.18}$$

where ρ_{cu}=1.7 $\times$ 10^{-8} Ωm is the resistivity of the copper.

Eventually, the total resistive losses in the transformer can be quantified with the help of the following equation

$$P_{cu} = R_1 I_{1,rms}^2 + R_2 I_{2,rms}^2 \tag{4.19}$$

Finally, the maximum power dissipated in the transformer can be calculated as

$$P_{tot} = P_{cu} + P_{core} \tag{4.20}$$

4.3.2 Semiconductors loss

The semiconductor losses can be divided into two different parts. Switching losses which occur during turning on and off the switch, and the conduction losses which occur when the switches are conducting.

Switching loss

By having the voltage and current waveforms over the switch during turn on and off intervals, the dissipated power over the switch can be calculated, which is considered as switching losses. The left plot in Fig. 4.24 shows the voltage and current waveforms over the switch during turn on. The voltage goes to zero from maximum value and the current increases from zero to the maximum value during the turn on interval.

The right plot in Fig. 4.24 depicts the product of the voltage and current during the same period. One triangle is formed which shows the instantaneous power over the switch. By integration of this power versus time the dissipated energy will be obtained. Finally, the average of dissipated power over the switch can be calculated by dividing this energy by the switching period.

$$p(t) = v(t) \times i(t) \tag{4.21}$$

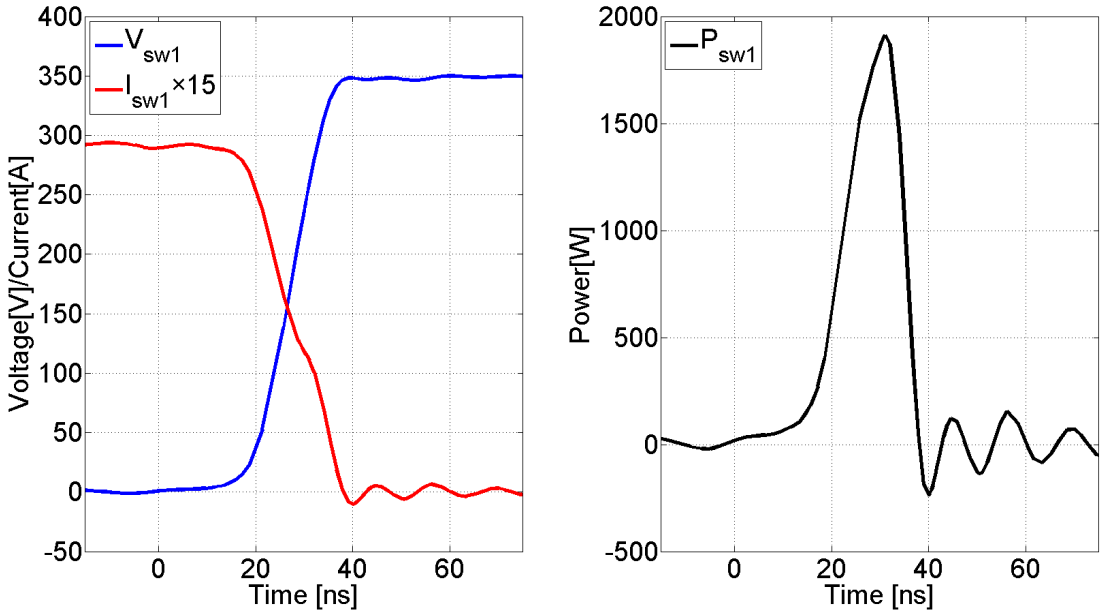

Fig. 4.24: Graphical representation for switching loss calculation

$$W_{loss} = \int p(t)dt \tag{4.22}$$

$$P_{loss} = \frac{W_{loss}}{T_{period}} = W_{loss} \times f_{sw} \tag{4.23}$$

Conduction loss

Since the MOSFET is behaving like a resistor during the conduction period it produces some conduction losses, which are dependent on the value of the MOSFET on-state resistance and the current that flows through it.

$$P_{on-state} = R_{dson} I_{on}^2 \tag{4.24}$$

In reality, usually there is a body diode inside the switch module, which is located in anti-parallel with respect to the MOSFET and carries the current with reverse polarity. It is the diode that conducts before turning on the MOSFET and prepares zero voltage switching. Since there is a forward voltage drop across the diode when it is on, some on-state losses can be produced and should be added to the MOSFET on-state losses to form the total conduction losses for the switch module,

$$v_{on-state} = V_{sd} + R_{dson} i_{on} \tag{4.25}$$

$$P_{on-state} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{on}(V_{sd} + R_{ds} i_{on}) dt =$$

$$= \frac{V_{sd}}{T_{sw}} \int_0^{T_{sw}} i_{on} dt + \frac{R_{dson}}{T_{sw}} \int_0^{T_{sw}} i_{on}^2 dt = \tag{4.26}$$

$$= V_{sd} I_{on(avg)} + R_{dson} I_{on(rms)}^2$$

The forward voltage drop and the on-state resistance of the switch module can be obtained from the switch datasheet and the rms and average value of the current can be calculated separately.

5

Results

The following chapter is devoted to the results that have been obtained in the project. Relevant comparisons and justifications were performed and conclusions were drawn as well as presenting the results.

5.1 Transformer selection

In this section the core for the transformer has been selected based on the flux that is occuring in it and the volume of the winding that fits inside the core window. The results are presented in Table 5.1.

Table 5.1: Peak flux density in different cores as a function of primary number of turns at 100 kHz for the full wave converter

Core Type	A_w	**B [T]**						
	$[cm^3]$	**N1=10**	**N1=20**	**N1=30**	**N1=40**	**N1=50**	**N1=60**	**N1=70**
ETD 29/16/10	210,56	1,056	0,528	0,352	0,264	0,211	0,176	0,151
ETD 34/17/11	304,56	0,826	0,413	0,275	0,207	0,165	0,138	0,118
ETD 39/20//13	398,56	0,642	0,321	0,214	0,160	0,128	0,107	0,092
ETD 44/22/15	492,56	0,464	0,232	0,155	0,116	0,093	0,077	0,066
ETD 49/25/16	586,56	0,380	0,190	0,127	0,095	0,076	0,063	0,054
ETD 54/28/19	680,56	0,287	0,143	0,096	0,072	0,057	0,048	0,041
ETD 59/31/22	774,56	0,218	0,109	0,073	0,055	0,044	0,036	0,031

Where A_w is the effective core area. Each cell represents different number of turns in the secondary side and the magnetic flux magnitude formed in the core with respect to the primary side. According to the datasheet of the magnetic material

chosen, which is N87 FERRITE, the maximum flux density of it is 0.36 T, so that it will not be saturated. Therefore, red color represents exceeding that limit, whereas green shows accepted flux density.

Table 5.2 shows the fitting of the windings inside the transformer bobbin. Values that are positive (red) mean that the winding size is bigger than the bobbin, consequently it will not fit in. On the contrary, values that are negative (green) mean that the winding will fit inside the bobbin. Therefore, the cells that are marked green are potentially suitable for the application used in the project. However, in order to have more accurate selection of the core, the copper and the core losses in the transformer have been calculated. The results of transformer's loss calculation are presented in Tables 5.3 and 5.4. Where V_e stands for effective magnetic volume and l_N for average length of one turn.

Table 5.2: Difference between the copper winding area and the tranformer box

Core Type	Area difference [mm2]						
	N1=10	N1=20	N1=30	N1=40	N1=50	N1=60	N1=70
ETD 29/16/10	-13,77	103,06	219,89	336,72	453,55	570,38	687,21
ETD 34/17/11	-54,27	62,56	179,39	296,22	413,05	529,88	646,71
ETD 39/20/13	-117,47	-0,64	116,19	233,02	349,85	466,68	583,51
ETD 44/22/15	-161,77	-44,94	71,89	188,72	305,55	422,38	539,21
ETD 49/25/16	-226,55	-109,72	7,11	123,94	240,77	357,60	474,43
ETD 54/28/19	-294,97	-178,14	-61,31	55,52	172,35	289,18	406,01
ETD 59/31/22	-356,17	-239,34	-122,51	-5,68	111,15	227,98	344,81

Table 5.3: Transformer core losses in the fullwave at 100 kHz

Core Type	V_e	P_{core} [W]						
	$[cm^3]$	N1=10	N1=20	N1=30	N1=40	N1=50	N1=60	N1=70
ETD 29/16/10	5.35	111,790	27,947	12,421	6,987	4,472	3,105	2,281
ETD 34/17/11	7.63	97,670	24,417	10,852	6,104	3,907	2,713	1,993
ETD 39/20/13	11.5	88,829	22,207	9,870	5,552	3,553	2,467	1,813
ETD 44/22/15	17.8	71,780	17,945	7,976	4,486	2,871	1,994	1,465
ETD 49/25/16	24.1	65,332	16,333	7,259	4,083	2,613	1,815	1,333
ETD 54/28/19	35.6	54,804	13,701	6,089	3,425	2,192	1,522	1,118
ETD 59/31/22	51.2	45,630	11,407	5,070	2,852	1,825	1,267	0,931

Table 5.4: Transformer winding losses in the fullwave at 100 kHz

Core Type	l_N [mm]	P_{cu} [W]						
		N1=10	N1=20	N1=30	N1=40	N1=50	N1=60	N1=70
ETD 29/16/10	52.8	0,839	1,678	2,517	3,356	4,195	5,034	5,873
ETD 34/17/11	60.5	0,961	1,923	2,884	3,845	4,806	5,768	6,729
ETD 39/20/13	69	1,096	2,193	3,289	4,385	5,482	6,578	7,674
ETD 44/22/15	77.7	1,235	2,469	3,704	4,938	6,173	7,407	8,642
ETD 49/25/16	86	1,366	2,733	4,099	5,466	6,832	8,199	9,565
ETD 54/28/19	96	1,525	3,051	4,576	6,101	7,627	9,152	10,677
ETD 59/31/22	106.1	1,686	3,372	5,057	6,743	8,429	10,115	11,801

In Table 5.5 the total losses in the transformer are presented, since they are consisting of winding and core losses.

Table 5.5: Total transformer losses in the fullwave at 100 kHz

Core Type	P_{total} [W]						
	N1=10	N1=20	N1=30	N1=40	N1=50	N1=60	N1=70
ETD 29/16/10	112,629	29,625	14,938	10,343	8,666	8,139	8,154
ETD 34/17/11	98,631	26,340	13,736	9,949	8,713	8,481	8,722
ETD 39/20/13	89,925	24,400	13,159	9,937	9,035	9,045	9,487
ETD 44/22/15	73,014	20,414	11,679	9,425	9,044	9,401	10,107
ETD 49/25/16	66,699	19,066	11,358	9,549	9,446	10,013	10,898
ETD 54/28/19	56,329	16,752	10,665	9,527	9,819	10,674	11,796
ETD 59/31/22	47,316	14,779	10,127	9,595	10,254	11,382	12,732

It is known that in order to have ultimate design and selection of the transformer the balance between the resistive transformer losses and the core losses must be maintained. This means that the difference between them has to be minimized, thus resulting in the most effective transformer design. In the ideal case, the difference must be 0, but it is hardly achievable in the real life. In Table 5.6 the sort of balance between resistive and core losses is shown. It is preferable to choose the core that has the lowest difference, which is marked with colors.

A good approximation for that balance to be maintained is 20% and as it is seen from the table that all marked cells satisfy this condition, but not all of them are suitable, since they may not fit in or may be over-saturated. According to all aforementioned conditions in the project, the core **ETD 59/31/22** with N_1=30 turns seems appropriate, therefore it has been selected. The size of the transformer is 60x62x22 mm, since it consists of two pieces of ETD cores.

Table 5.6: Difference between transformer core and copper losses in the fullwave at 100 kHz

Core Type	Losses difference [W]						
	N1=10	N1=20	N1=30	N1=40	N1=50	N1=60	N1=70
ETD 29/16/10	110,951	26,270	9,904	3,631	0,277	-1,928	-3,591
ETD 34/17/11	96,709	22,495	7,968	2,259	-0,900	-3,055	-4,736
ETD 39/20/13	87,732	20,014	6,581	1,166	-1,929	-4,111	-5,862
ETD 44/22/15	70,545	15,476	4,272	-0,452	-3,302	-5,414	-7,177
ETD 49/25/16	63,966	13,600	3,160	-1,383	-4,219	-6,384	-8,232
ETD 54/28/19	53,278	10,650	1,513	-2,676	-5,435	-7,630	-9,559
ETD 59/31/22	43,944	8,036	0,013	-3,891	-6,604	-8,847	-10,869

As it was mentioned earlier, for the current doubler case another approach has been chosen for determining the proper number of turns in the transformer. By having the maximum allowable flux density according to the material datasheet, different steps from zero to this maximum value have been chosen and based on these steps, different number of turns for primary side are determined. These values are shown in Table 5.7 and 5.8 for different flux densities, which are given in [T] and various core types. As it can be seen, the **EPCOS PQ** cores have been chosen for this topology, which is different from the full wave rectification case. All parameters have been calculated at the maximum load power which is obtained by setting the duty cycle and shifting the delay to the maximum possible value.

Table 5.7: Primary number of turns as a function of different flux density in the current doubler at 100 kHz

Core types	A_e	N_1						
	$[mm^2]$	B=0,05	B=0,1	B=0,15	B=0,2	B=0,25	B=0,3	B=0,35
PQ16/11.6	42,1	421,6	210,8	140,5	105,4	84,3	70,3	60,2
PQ20/20	62,9	282,2	141,1	94,1	70,5	56,4	47,0	40,3
PQ26/25	122	145,5	72,7	48,5	36,4	29,1	24,2	20,8
PQ32/30	153,8	115,4	57,7	38,5	28,9	23,1	19,2	16,5
PQ35/35	169,7	104,6	52,3	34,9	26,1	20,9	17,4	14,9
PQ40/40	188,3	94,3	47,1	31,4	23,6	18,9	15,7	13,5
PQ50/50	330	53,8	26,9	17,9	13,4	10,8	9,0	7,7

Table 5.9 and 5.10 depict the values for the core and copper losses for different cores in different flux densities. In order to keep the aforementioned balance between core and copper losses inside the transformer the green cell in Table 5.11, **PQ32/30**, has been chosen to be the proper core for this case. The difference between copper and core losses for this operating point is in the desired range but maybe not the

Table 5.8: Secondary number of turns in the current doubler at 100 kHz

Core types	A_e	N_2						
	$[mm^2]$	**B=0,05**	**B=0,1**	**B=0,15**	**B=0,2**	**B=0,25**	**B=0,3**	**B=0,35**
PQ16/11.6	42,1	47,2	23,6	15,7	11,8	9,4	7,9	6,7
PQ20/20	62,9	31,6	15,8	10,5	7,9	6,3	5,3	4,5
PQ26/25	122	16,3	8,1	5,4	4,1	3,3	2,7	2,3
PQ32/30	153,8	12,9	6,5	4,3	3,2	2,6	2,2	1,8
PQ35/35	169,7	11,7	5,9	3,9	2,9	2,3	2	1,7
PQ40/40	188,3	10,6	5,3	3,5	2,6	2,1	1,8	1,5
PQ50/50	330	6	3	2	1,5	1,2	1	0,9

minimum possible. Indeed, there might be some other cores which have better balance between the two loss components but from the fitting viewpoint this core is the best choice for this current doubler converter, where the core and copper losses are 4.4 W and 3.83 W respectively. The primary and secondary number of turns corresponding to this choice are about 38 and 4 turns.

Table 5.9: Transformer core losses in the curerent doubler at 100 kHz

Core types	V_e	$P_{core}[W]$						
	$[cm^3]$	**B=0,05**	**B=0,1**	**B=0,15**	**B=0,2**	**B=0,25**	**B=0,3**	**B=0,35**
PQ16/11.6	1,14	0,053	0,213	0,479	0,852	1,331	1,917	2,609
PQ20/20	2,84	0,133	0,533	1,199	2,132	3,332	4,798	6,530
PQ26/25	6,53	0,306	1,224	2,755	4,898	7,652	11,019	14,999
PQ32/30	10,44	0,489	1,958	4,404	7,830	12,234	17,618	23,979
PQ35/35	13,44	0,630	2,520	5,670	10,080	15,750	22,680	30,870
PQ40/40	17,43	0,817	3,268	7,353	13,073	20,426	29,413	40,035
PQ50/50	37,27	1,747	6,988	15,723	27,953	43,676	62,893	85,605

Table 5.10: Transformer copper losses in the curerent doubler at 100 kHz

Core types	l_N	$P_{cu}[W]$						
	$[mm]$	**B=0,05**	**B=0,1**	**B=0,15**	**B=0,2**	**B=0,25**	**B=0,3**	**B=0,35**
PQ16/11.6	20	13,548	6,774	4,516	3,387	2,710	2,258	1,935
PQ20/20	44	19,950	9,975	6,650	4,987	3,990	3,325	2,850
PQ26/25	56	13,091	6,545	4,364	3,273	2,618	2,182	1,870
PQ32/30	62	11,497	5,748	3,832	2,874	2,299	1,916	1,642
PQ35/35	76	12,772	6,386	4,257	3,193	2,554	2,129	1,825
PQ40/40	87	13,177	6,588	4,392	3,294	2,635	2,196	1,882
PQ50/50	100,5	8,685	4,343	2,895	2,171	1,737	1,448	1,241

Table 5.11: Transformer total losses in the curerent doubler at 100 kHz

Core types	$P_{total}[W]$						
	B=0,05	**B=0,1**	**B=0,15**	**B=0,2**	**B=0,25**	**B=0,3**	**B=0,35**
PQ16/11.6	13,60157	6,987	4,995	4,239	4,040913	4,175	4,545
PQ20/20	20,08311	10,508	7,849	7,119	7,321609	8,123	9,379
PQ26/25	13,39688	7,769	7,118	8,171	10,2705	13,201	16,869
PQ32/30	11,98606	7,705	8,237	10,704	14,534	19,534	25,623
PQ35/35	13,4023	8,906151	9,927	13,27308	18,305	24,809	32,695
PQ40/40	13,99372	9,85647	11,745	16,36667	23,061	31,609	41,917
PQ50/50	10,43243	11,33082	18,618	30,12385	45,413	64,341	86,845

5.2 Semiconductor losses

There are always losses in semiconductor devices and they are presented in the following section. Each part of these losses have been calculated separately, switching and conduction losses, according to the equations that were introduced before. Although the switch module Allegro AMS model has been used in the simulation and just one current waveform for each switch module can be observed, it is important to split the current between the body diode and MOSFET in order to calculate the right value of conduction losses for each switch. This can be done by looking at the gate pulse voltage of each switch. The results for the converter with full wave rectifier are depicted in Appendix B and in Fig. 5.3.

According to the results, it is clear that the main dominant part of the total losses is the conduction losses, especially at the secondary side because of higher current rating. Therefore, a big improvement is achieved in reducing the losses and consequently increasing the efficiency, if some methods are used to decrease the conduction losses. One of these methods is paralleling the switches. If we consider just one switch in Fig. 5.4 and write the equations for conduction losses for both cases.

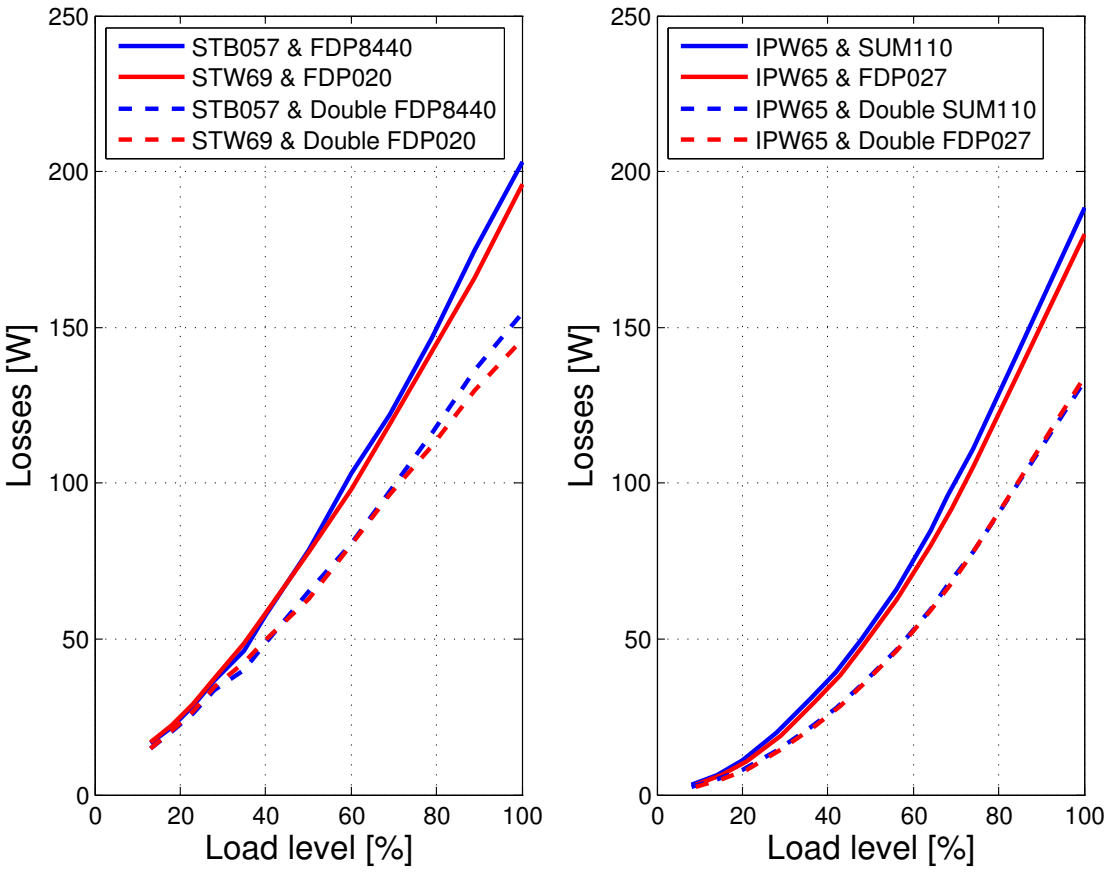

Fig. 5.1: Total conduction converter losses for full wave and current doubler topologies

$$P_{con1} = R_{dson1}.I^2_{MOS-rms1} + V_{f1}.I_{D-avg1} \tag{5.1}$$

In case of having two switch modules in parallel, we have

$$P_{con2} = 2 \times [R_{dson2}.I^2_{MOS-rms2} + V_{f2}.I_{D-avg2}] \tag{5.2}$$

$$I_{MOS-rms2} = \frac{I_{MOS-rms1}}{2} \tag{5.3}$$

$$I_{D-avg2} = \frac{I_{D-avg1}}{2} \tag{5.4}$$

$$R_{dson2} = R_{dson1} \tag{5.5}$$

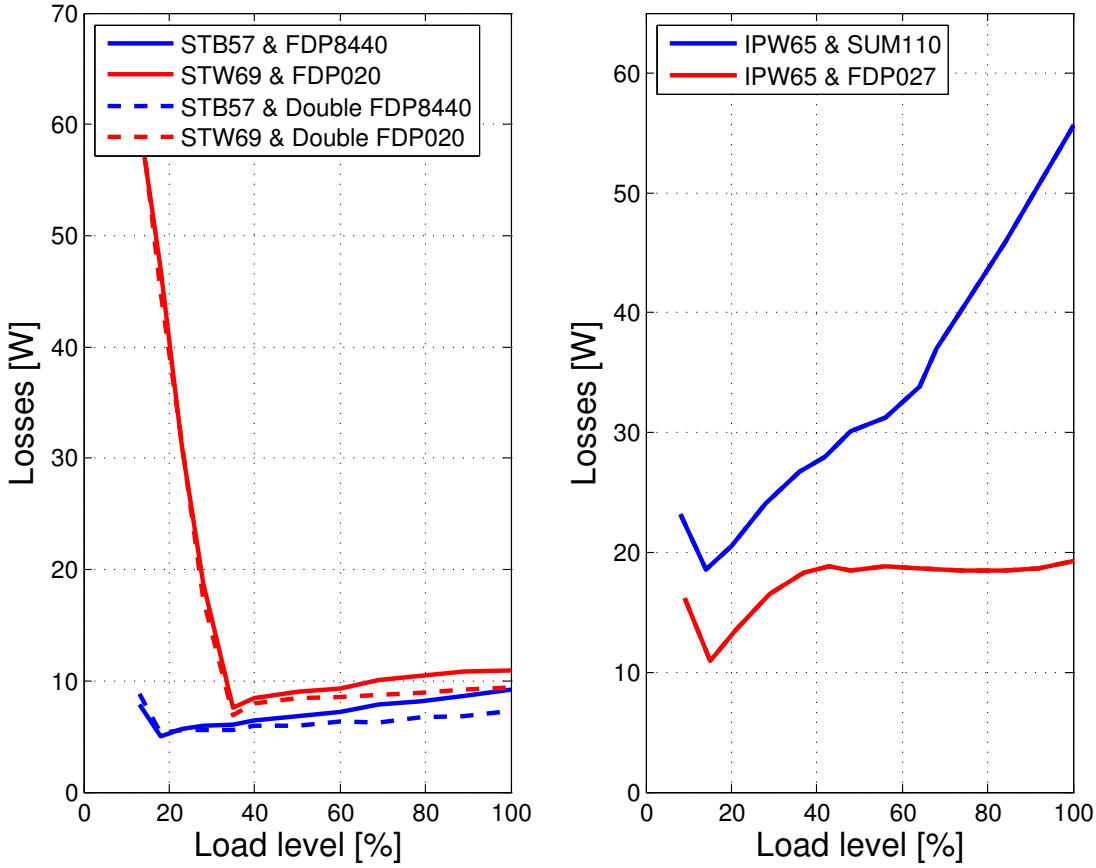

Fig. 5.2: Total switching converter losses for full wave and current doubler topologies

$$V_{f2} = V_{f1} \tag{5.6}$$

$$P_{con2} = 2\times[R_{dson1}.(\frac{I_{MOS-rms1}}{2})^2+V_{f1}.\frac{I_{D-avg1}}{2}] = 0.5\times R_{dson1}.I^2_{MOS-rms1}+V_{f1}.I_{D-avg1} \tag{5.7}$$

So it means that by paralleling two switches and making a new module we have managed to halve the on state resistance of the MOSFET and therefore reduce the total conduction losses to a high extent. By this method some new results were obtained, which imply lower conductions losses in the semiconductors and consequently lower total losses in the device.

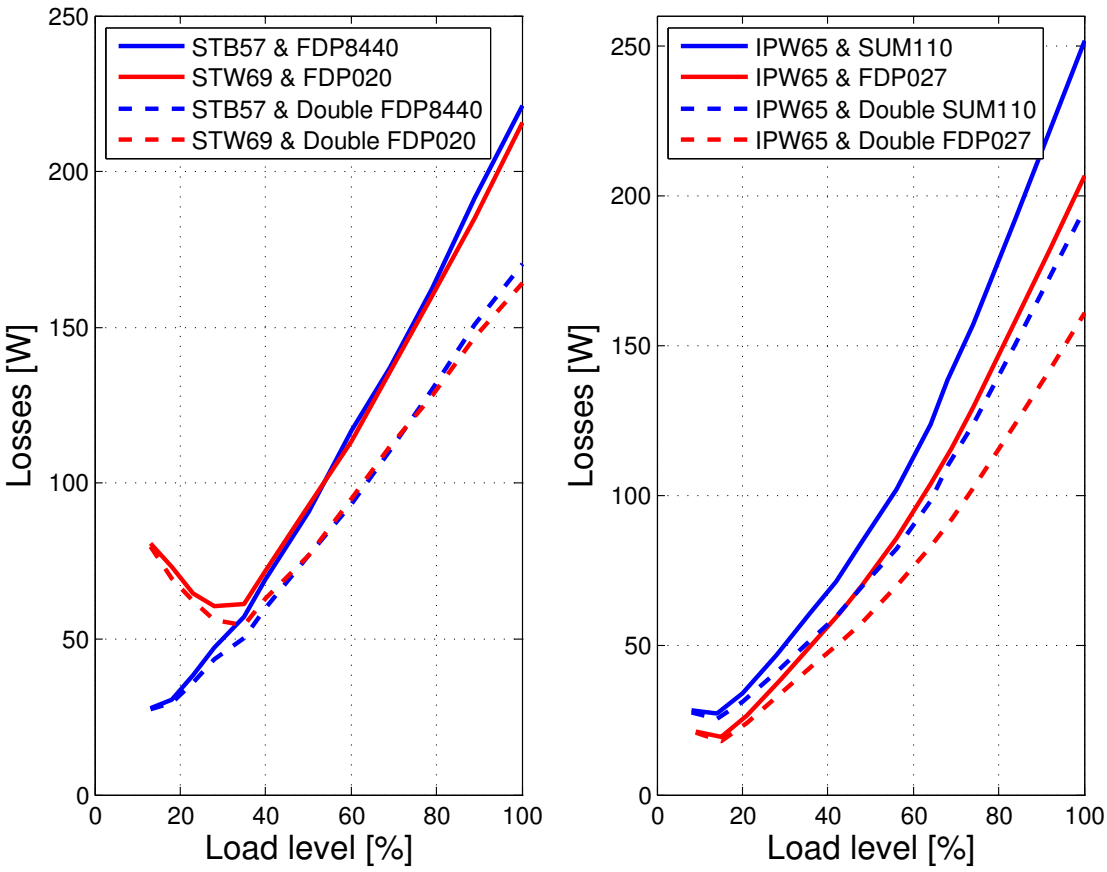

Fig. 5.3: Total converter losses for full wave and current doubler topologies

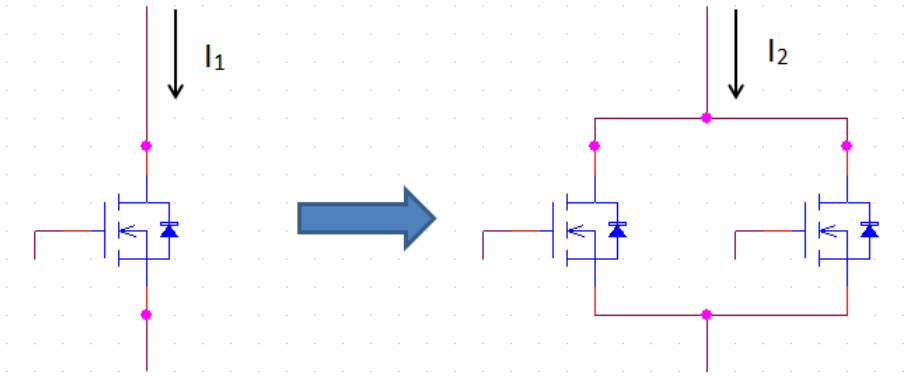

Fig. 5.4: Paralleing the switches to the lower conduction losses

Comparing the waveforms in Fig. 5.1, 5.2 and 5.3, it must be noticed that the loss difference is not that dramatic, but there is a small deviation in total losses in both cases. This is justified that the switches used have different performance characteristics. From Table A.2 and Fig 5.2 it is seen that switching losses for STW69N65M5 has increased significantly after reducing the load to 30%. This can be explained by the fact that the ZVS on the primary side is lost. After implementing the switch paralleling method the conduction losses in the secondary side has been reduced by around 50 W for maximum load that is presented in Appendix B and Fig. 5.3 with the dashed line, which is a quite significant fraction from the initial result. Tables A.7, A.8 and Fig. 5.1 also show the changes in conduction losses by paralleling two switches in the current doubler converter. Consequently, the overall efficiency has been improved, but the present-worth analysis should be carried out in order to check if the measure is cost-effective.

5.3 Efficiency

The following section represents the final results obtained from the simulations with the real components in Allegro AMS. For the comparison reasons, both full wave and current doubler topologies are plotted together in order to have explicit understanding in the efficiency discrepancies.

All calculated efficiencies for all arrangements are depicted in Fig. 5.5 that have been simulated in the project. It is noticeable that having two parallel switches instead of one increases efficiency by around 1 %, which is significant improvement. It is also seen that efficiency in the current doubler is greater than that in the full wave set-up by around 1.5 %. This is a great achievement and it coincides with the theory behind it.

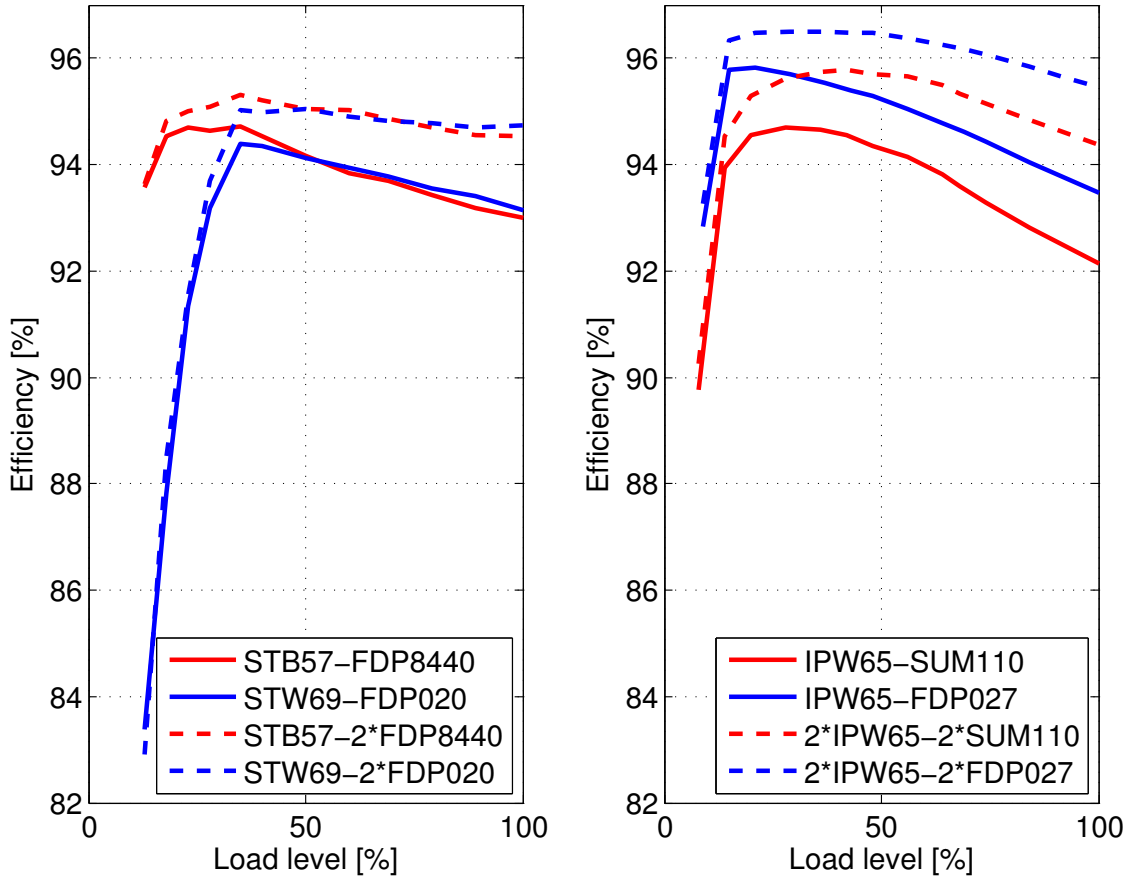

Fig. 5.5: Efficiency plots for both full wave and current doubler arrangements

In Fig. 5.6 the two best of achieved efficiency curve are depicted for single switches on the primary, single and double switches on the secondary sides. It is quite clear that even paralleling only on the secondary side increases the total efficiency substainally.

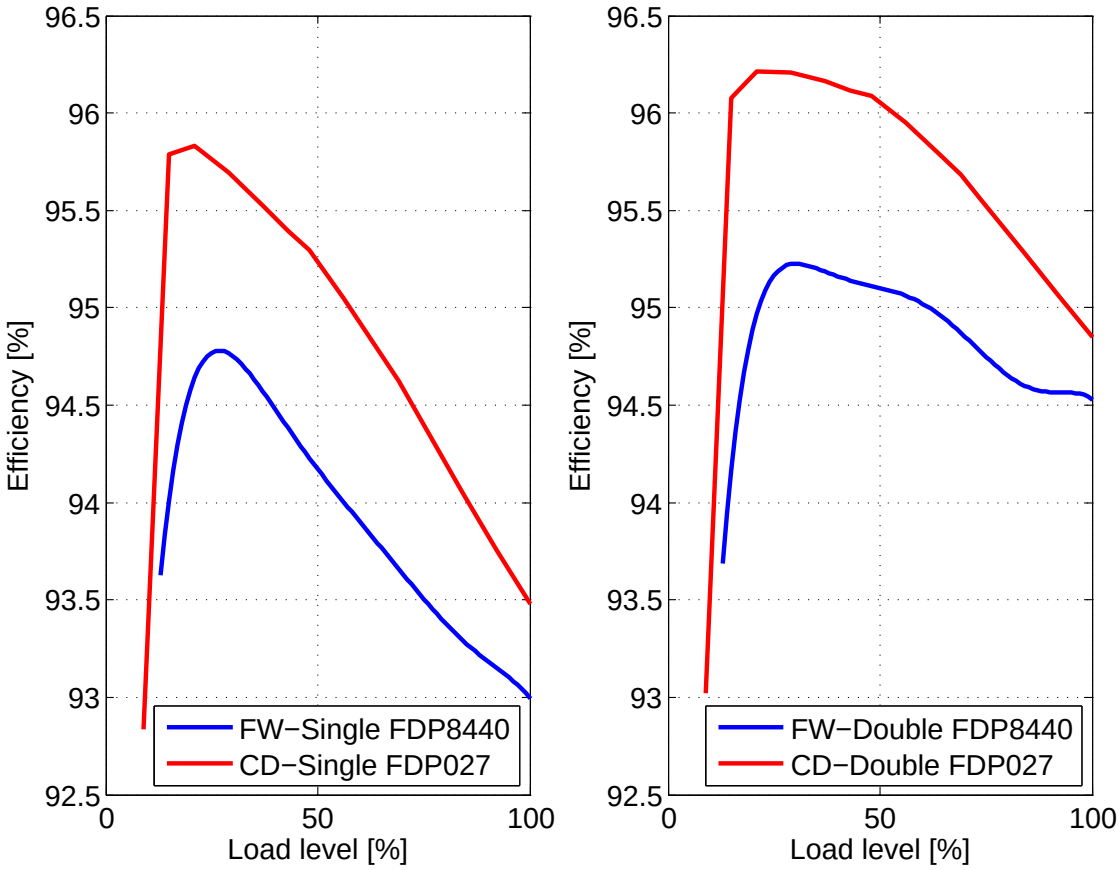

Fig. 5.6: Best efficiency plots for both full wave and current doubler arrangements with single and double switches on the secondary side

In Fig. 5.7 it is seen that the maximum efficiency is achieved with placing two switches in parallel on both sides of the converter. Apparently, this is logical since paralleling decreases the on-state resistance of the MOSFET, hence the conduction loss of the switch, which comprise a significant portion of the total converter losses.

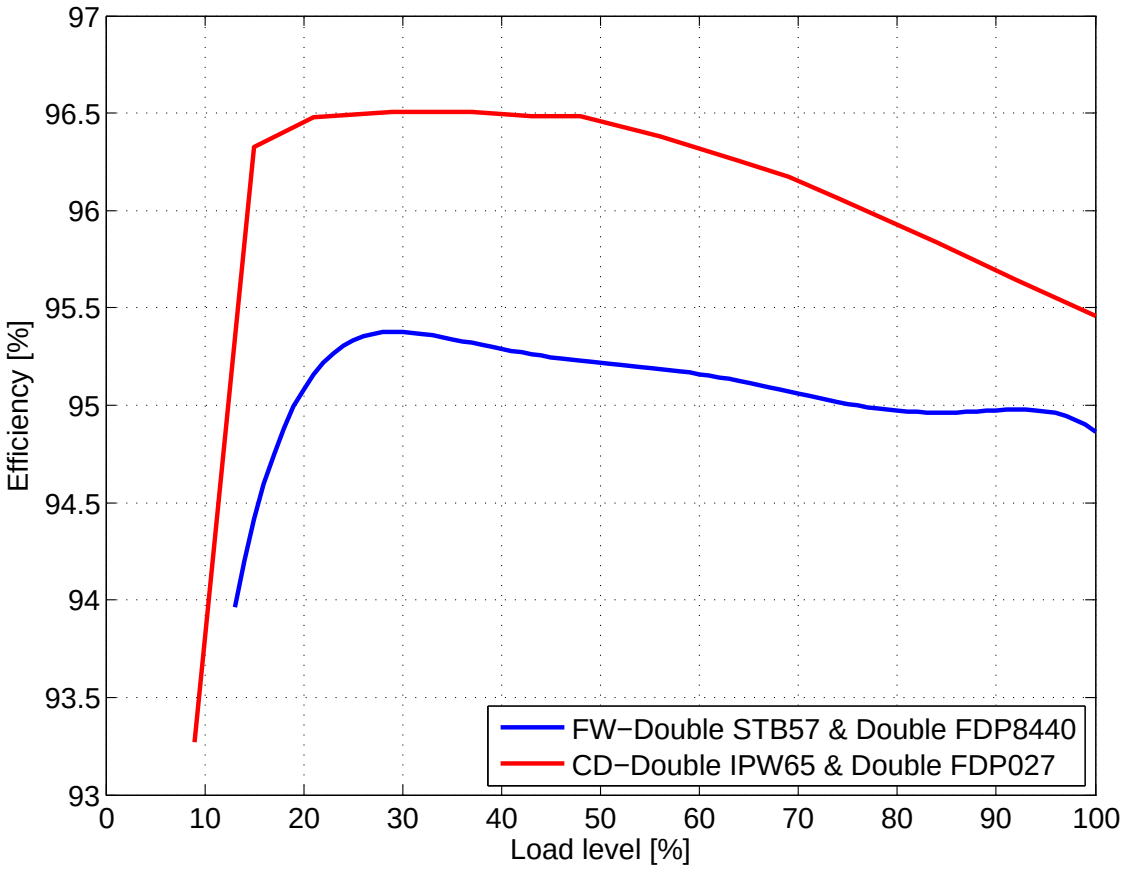

Fig. 5.7: Efficiency plots for both full wave and current doubler arrangements with double switches on both sides

5.4 Cost estimation

Since it is not the most efficient way to utilize just a single switch arrangement, the decision towards paralleling of the switches has been implemented. However, it has to be checked if this measure is cost-effective. Therefore, a present worth analysis was carried out and the calculated results are presented in the following section.

Calculations were performed taking into consideration the load cycle of the converter, using current distribution throughout almost one hour that is depicted in Fig. 5.8 with three different modes being driven, which are city, highway and heavy cycles.

Fig. 5.9 shows the distribution plot which is obtained by the data from Fig. 5.8. By having the distribution histogram the probability for different currents can be

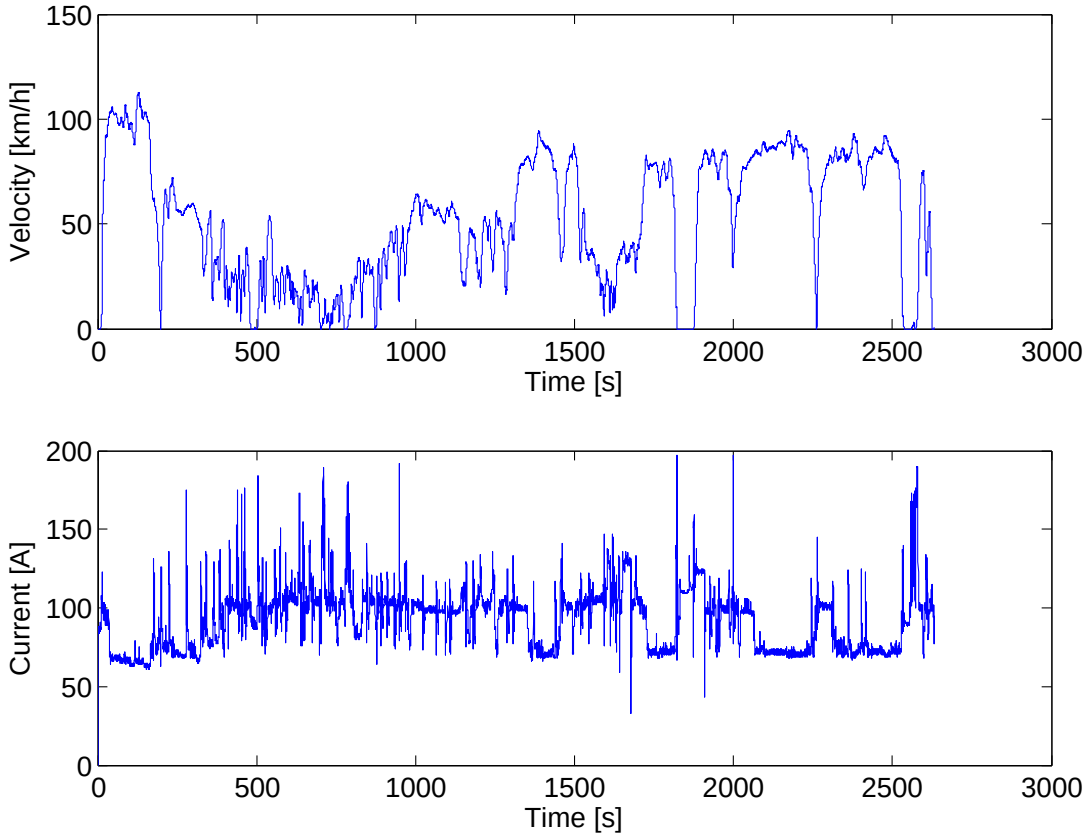

Fig. 5.8: Converter loading cycle, taken from the real test

obtained, which is shown in the lower plot of Fig. 5.9 that must also be considered in order for the analysis to be more accurate.

After replacing the single switches with double ones on the secondary side, the conduction losses have been decreased. The differences between the total losses in two different cases, single and double switches at the secondary part of the converter, have been plotted and shown in Fig. 5.10 and 5.11 for two different topologies. It can be seen that the difference is around 15 W at 50% of the maximum load which can be considered as the converter most common operating point.

Concerning the loss differences and probability plots for different load currents the normalized power loss differences can be obtained and can easily be converted to the energy, which is shown in Fig. 5.12 and 5.13. This energy can be saved throughout the operating time if the paralleling method is used instead of single switches in the rectifier side of the converter. In this calculation it was assumed

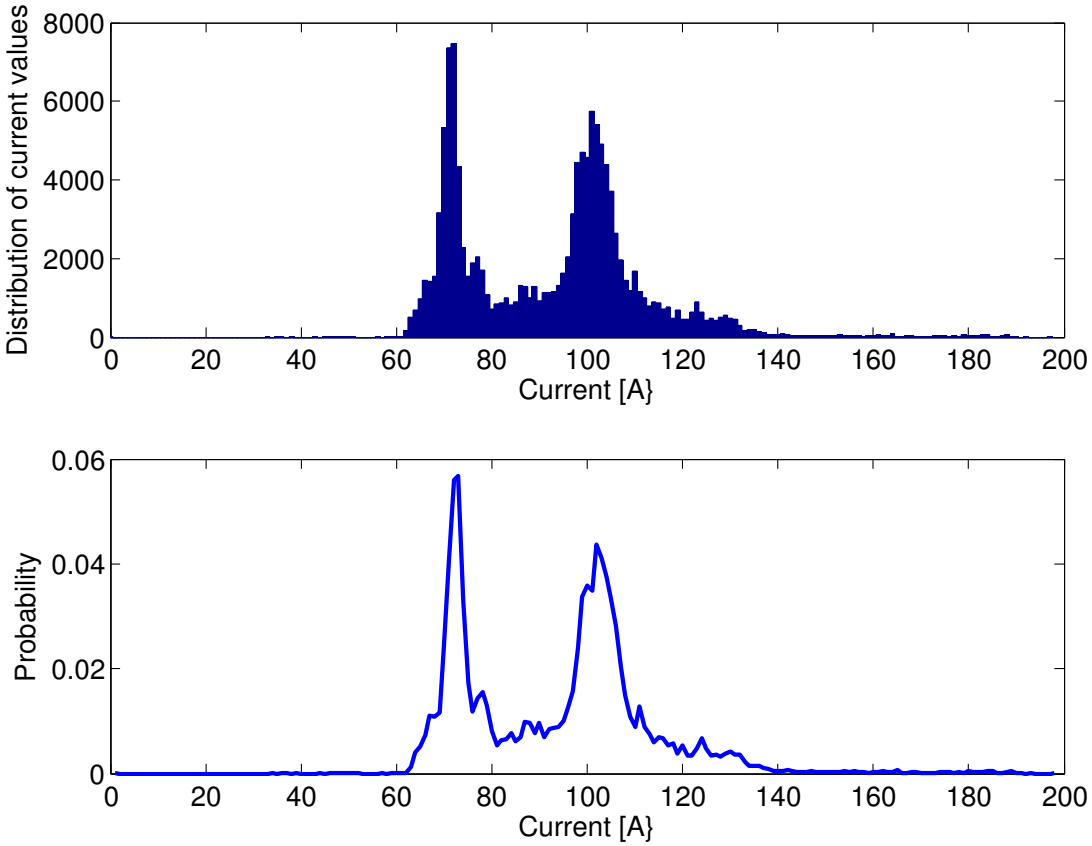

Fig. 5.9: Distribution of current values and their probability

that the typical driving duration is 1.5 hours per day.

According to the performed calculations, the energy saved in the full wave and current doubler converters equal 8.93 kWh/year and 5.93 kWh/year respectively. Regarding the data obtained from the specification, the converter must operate for 15 years. Therefore, the energy saved throughout the overall lifetime will be 133.95 kWh and 88.95 kWh respectively. In order to check if those measures are cost-effective one must carry out the worth analysis. Converting the energy saved to the money equivalent, one must consider the energy price including taxes for the final customer, which is 1.72 SEK per kWh in Sweden according to [4] and it is assumed to follow the inflation throughout the whole lifetime of the converter.

This gives the saved money in 15 years, which are 230.4 SEK and 153 SEK for the full wave and current doubler converter. If this amount of money is higher than the investment payment for having extra switches, then the proposed approach is

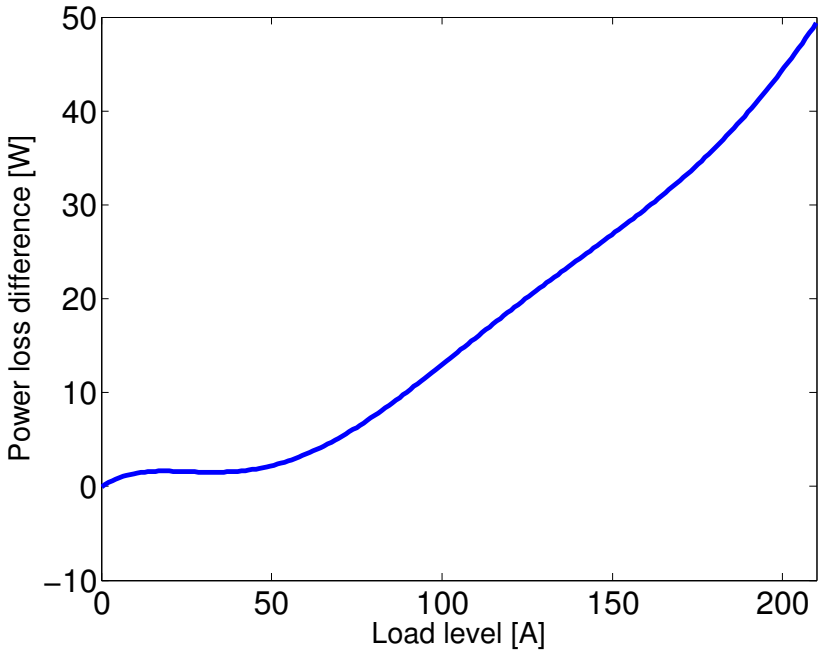

Fig. 5.10: Total power loss difference between single and double switches at the secondary side of the full wave converter

cost-effective. The switches prices are given in Table. 5.12 according to the suppliers websites. The future worth price analysis is based on Compound Interest Factor (CIF) calculation that is shown in 5.8.

$$CIF = (1 + i)^n \tag{5.8}$$

where i is the interest rate, which is assumed to be 5% and n is the number of years and it equals 15. Consequently, the CIF equals 2.0789. The future price can be calculated by 5.9.

$$F = CIF \times P \tag{5.9}$$

where P is the present price and F is the future worth value.

Table 5.12 depicts the cost-efficiency of paralleling the switches in the secondary side of the converters. Since the saved energy is higher than the future worth price of the extra switches, the presented approach is cost-effective. However, in the full wave case it can be observed that the difference is not that tangible because the driving duration is assumed to be 1.5 hours per day. Any duration extension in the driving time will contribute to the better profitability margin.

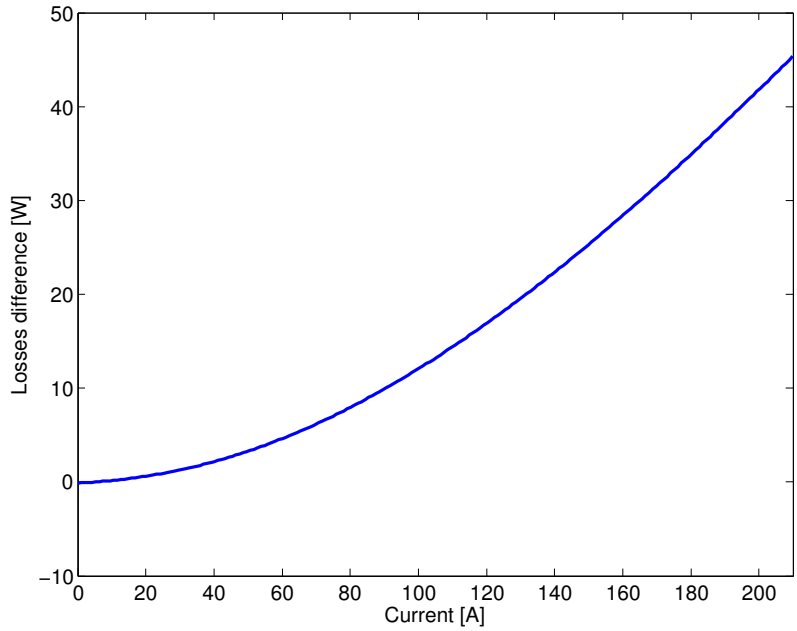

Fig. 5.11: Total power loss difference between single and double switches at the secondary side of the current doubler converter

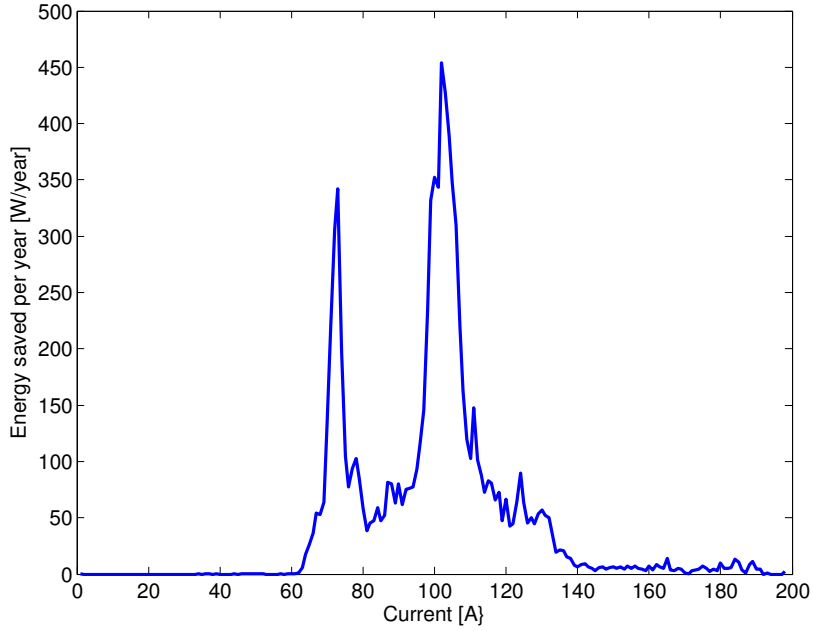

Fig. 5.12: Energy saved throughout a year in the full wave converter

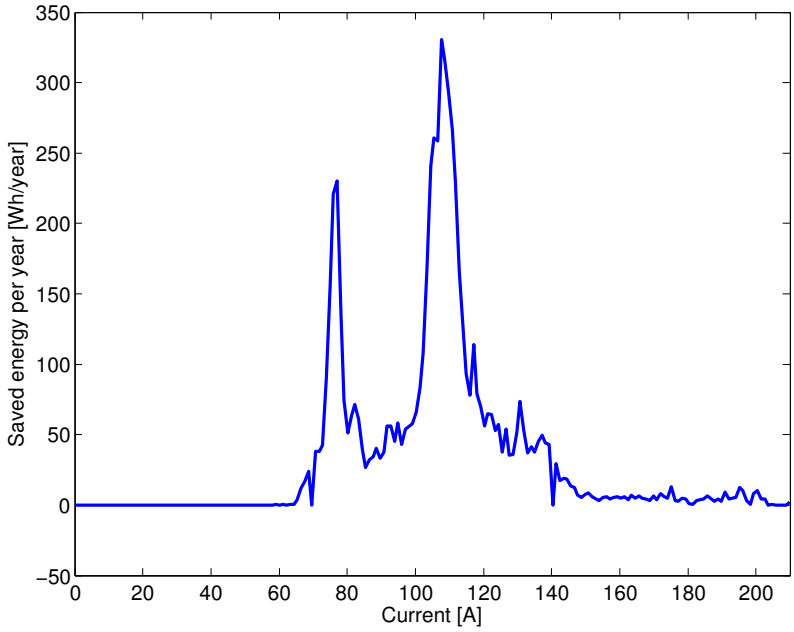

Fig. 5.13: Energy saved throughout a year in the current doubler converter

Table 5.12: Switch pricing

Semiconductor	**Cost [$]**	**Cost [SEK]**	**Total cost [SEK]**	**Future worth price [SEK]**	**Saved energy [SEK]**
FC FDP8440 - *Full Wave*	4,12	27,14	108,56	225,6	230,4
FC FDP027N08B - *Current doubler*	3,3	21,74	43,48	90,36	153

6

Circuit improvements

One of the aims of the following project was to investigate the performance of the converter and suggest some improvements, if issues were identified. Therefore, the following chapter is devoted to the description of the procedure that was applied to get the presented results.

6.1 Spike killer

The whole analysis is carried out on both investagated converter topologies with real components. It is clearly observed in Fig. 6.1 that during turn-off interval voltage over the switch on the secondary side overshoots its reference value and starts to oscillate. We think that this occurs because of the diode reverse recovery current that is conducting prior to the switch. Diode snaps off, resulting in an overshoot and causes a ringing effect inside the module, which brings parasitic influence. This ringing may generate significant noise and it may be sustained for many cycles after the spike has happened, which may damage the switch, consequently it has to be suppresed. Since the amount of time to suppress its oscillations is not sufficient, steady-state cannot be reached, therefore those oscillations must be damped. One way to damp them is to implement the RC snubber in parallel to every switch module on the secondary side.

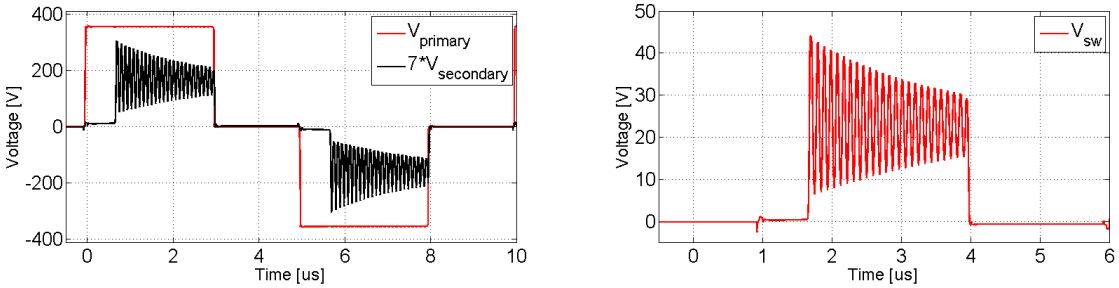

Fig. 6.1: Voltage over the switch, ringing effect representation

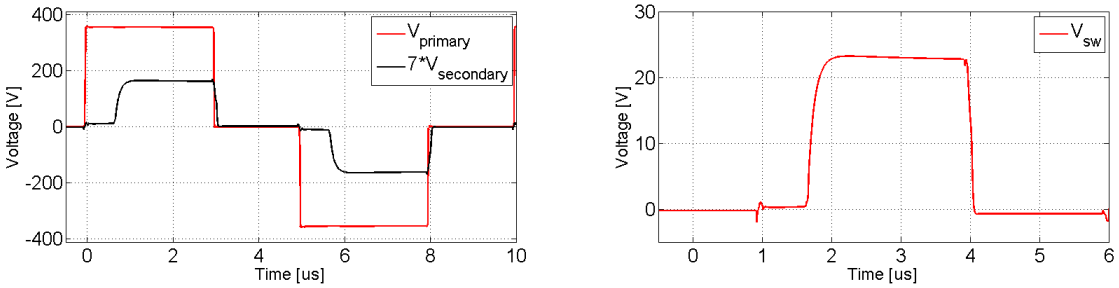

Fig. 6.2: Voltage over the switch after snubber was implemented, ringing effect eliminated

7

Conclusions and Future work

7.1 Conclusion

The set aim of the project has been successfully fulfilled, models of two different DC/DC converters utilized in an electrified vehicle were built and their performance investigated. Relevant analysis and comparison have been carried out and presented in the report. Phase shifted switching pattern and leakage inductance contributed significantly in achieving zero voltage switching, so that switching losses were minimized. Losses in the converters have also been determined with help of Matlab, where the calculation script was fully written. By using parallel main switching components, less conduction losses were achieved, which was the dominant part of total losses. The transformer design was carefully performed and the core was appropriately selected, considering core and copper losses and the condition of reducing the size and the volume of it.

After loss calculation, the efficiencies of both converters have been quantified and they are in agreement with the theoretical justification behind it that the current doubler topology is more efficient than the full wave one. Present worth analysis has been conducted and proved that the paralleling of the switches is cost-effective in both cases. Since some oscillations were observed in the simulation, a snubber circuit was implemented to supress the spikes and smooth the voltage waveforms.

7.2 Future work

Concerning the future work that could be done as continuation of the project, we think that the following tasks could be carried out:

- Use alternative semiconductors devices in simulations, those like GaN and SiC
- Verify the simulated results on a real converter
- Suggest more efficient topology for bidirectional applications
- Investigate converter's performance with different frequencies

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0

Appendices

A

Results - Tables

In this chapter the explicit results from the simulations with real components are presented. All calculations were performed by the devised script within the project.

Table A.1: Converter losses in [W] for fullwave at 100 kHz with STB57N65M5 as primary switches and FDP8440 as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
13	7,350	0,511	0,672	15,724	0,529	3,127	27,914	406,981
18	4,434	0,617	0,896	20,808	0,689	3,216	30,660	531,062
23	4,906	0,767	1,280	27,213	0,884	3,342	38,392	684,943
28	5,042	0,954	1,780	34,968	1,082	3,397	47,223	831,664
35	4,920	1,175	2,418	43,730	1,317	3,583	57,143	1023,005
40	5,082	1,390	3,224	54,293	1,548	3,678	69,215	1196,276
50	5,081	1,736	4,781	73,721	1,926	3,813	91,058	1470,640
60	5,142	2,100	6,739	96,411	2,331	4,030	116,753	1774,646
69	5,505	2,377	8,351	113,700	2,644	4,274	136,852	2030,427
79	5,428	2,729	10,480	136,475	3,000	4,525	162,637	2314,128
89	5,537	3,101	12,890	161,807	3,374	4,804	191,513	2617,437
100	5,720	3,532	14,962	188,129	3,793	5,070	221,206	2937,920

Where $P_{sw,tot,P}$ is the total switching losses in the primary side, $P_{sw,tot,S}$ is the total switching losses in the secondary side, $P_{cond,tot,P}$ is the total conduction losses in the primary side, $P_{cond,tot,S}$ is the total conduction losses in the secondary side, P_{copper} is the copper losses in the transformer, P_{core} is the core losses in the transformer, P_{out} is the output power and the load level is expressed in percentage of

the output current.

Table A.2: Converter losses in [W] for fullwave at 100 kHz with STW69N65M5 as primary switches and FDP020N6B as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
13	59,680	0,513	0,633	16,110	0,528	3,127	80,591	404,583
18	46,291	0,627	0,760	21,509	0,686	3,216	73,090	527,484
23	30,234	0,769	0,965	28,333	0,881	3,342	64,524	681,033
28	17,859	0,906	1,249	36,121	1,080	3,397	60,613	829,401
35	6,551	1,083	1,747	46,864	1,336	3,546	61,127	1030,770
40	7,209	1,242	2,181	56,081	1,549	3,659	71,922	1198,245
50	7,500	1,562	3,154	74,946	1,939	3,813	92,915	1490,679
60	7,386	1,903	4,273	93,654	2,280	4,030	113,525	1761,436
69	7,791	2,241	5,462	113,318	2,624	4,274	135,710	2041,507
79	7,953	2,542	6,840	135,435	2,975	4,525	160,271	2329,564
89	7,964	2,847	8,338	157,738	3,310	4,804	185,002	2619,003
100	7,738	3,230	10,127	185,810	3,695	5,070	215,670	2932,378

Table A.3: Current Doubler converter losses in [W] at 100 kHz with IPW65R080CFD as primary and SUM110N06 as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
8	15,635	7,592	1,571	1,571	0,319	1,381	28,069	246,384
14	10,395	8,167	2,408	4,007	0,542	1,482	27,000	418,222
20	13,118	7,418	3,501	7,501	0,764	1,586	33,888	589,487
28	16,281	7,807	5,563	14,330	1,083	1,748	46,811	835,710
36	18,039	8,656	7,964	22,760	1,388	1,919	60,726	1073,818
42	18,480	9,504	9,869	29,616	1,596	2,037	71,102	1235,314
48	18,554	11,553	12,134	37,881	1,819	2,158	84,099	1403,755
56	18,414	12,842	15,545	50,594	2,123	2,347	101,865	1639,326
64	18,191	15,612	19,368	65,350	2,434	2,544	123,499	1876,868
68	18,214	18,844	21,695	74,331	2,609	2,680	138,373	2021,544
74	18,173	22,135	24,715	86,313	2,830	2,819	156,984	2183,773
84	18,008	27,789	30,532	109,929	3,230	3,108	192,594	2491,040
100	18,764	36,908	39,808	148,764	3,825	3,568	251,635	2947,893

Table A.4: Current Doubler converter losses in [W] at 100 kHz with IPW65R080CFD as primary and FDP027N08B as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
9	15,514	0,697	1,577	1,675	0,355	1,381	21,199	274,596
15	10,419	0,558	2,383	3,920	0,568	1,482	19,329	439,574
21	12,947	0,536	3,480	7,118	0,786	1,586	26,452	608,230
29	16,192	0,346	5,564	13,517	1,105	1,748	38,472	855,004
37	18,066	0,257	8,086	21,650	1,419	1,919	51,396	1097,964
43	18,521	0,312	10,082	28,383	1,634	2,037	60,970	1262,956
48	18,168	0,345	12,063	35,019	1,823	2,158	69,577	1410,262
56	18,463	0,362	15,476	47,024	2,129	2,347	85,801	1648,889
64	18,282	0,397	19,324	60,723	2,440	2,544	103,711	1886,005
69	18,195	0,342	21,846	70,055	2,633	2,680	115,752	2037,728
74	18,081	0,404	24,654	80,532	2,836	2,819	129,326	2193,634
84	18,017	0,474	30,489	102,896	3,236	3,108	158,220	2501,381
92	18,127	0,558	35,106	121,169	3,538	3,334	181,833	2731,863
100	18,615	0,646	39,769	140,031	3,832	3,568	206,462	2959,688

Table A.5: Converter losses in [W] for full wave at 100 kHz with STB57N65M5 as primary switches and eight switches of FDP8440 in the secondary side

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
13	8,505	0,315	0,630	14,260	0,517	3,181	27,408	403,635
18	4,911	0,373	0,901	19,379	0,694	3,216	29,474	539,161
23	5,146	0,431	1,261	24,889	0,882	3,270	35,879	682,717
28	5,087	0,534	1,786	31,766	1,101	3,306	43,580	843,219
35	4,990	0,639	2,340	37,585	1,317	3,490	50,361	1023,943
40	5,260	0,729	3,124	45,604	1,543	3,546	59,806	1188,270
50	5,102	0,902	4,755	60,695	1,938	3,678	77,070	1477,785
60	5,260	1,065	6,537	74,158	2,314	3,931	93,266	1782,532
69	5,026	1,202	8,393	89,105	2,663	4,070	110,460	2037,376
79	5,358	1,346	10,725	105,243	3,032	4,274	129,978	2322,839
89	5,306	1,525	13,203	122,951	3,420	4,482	150,888	2618,364
100	5,584	1,698	15,849	138,753	3,783	4,804	170,472	2944,207

Table A.6: Converter losses in [W] for fullwave at 100 kHz with STW69N65M5 as primary switches and eight switches of FDP020N6B in the secondary side

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
13	61,055	0,311	0,583	14,208	0,501	3,145	79,804	387,333
18	44,404	0,424	0,739	19,853	0,690	3,216	69,324	532,719
23	30,841	0,451	0,966	25,890	0,876	3,270	62,293	673,702
28	16,753	0,562	1,282	33,199	1,096	3,306	56,198	835,476
35	6,298	0,656	1,734	40,827	1,343	3,490	54,348	1037,149
40	7,315	0,691	2,180	47,544	1,545	3,565	62,840	1191,917
50	7,640	0,855	3,080	59,731	1,900	3,755	76,962	1474,447
60	7,471	1,030	4,335	76,000	2,306	3,872	95,014	1770,192
69	7,554	1,169	5,607	90,585	2,665	4,030	111,609	2041,052
79	7,626	1,294	6,989	105,024	3,009	4,274	128,216	2327,839
89	7,738	1,464	8,601	121,024	3,374	4,482	146,682	2617,065
100	7,793	1,598	10,279	135,946	3,731	4,804	164,152	2948,298

Table A.7: Current Doubler converter losses in [W] at 100 kHz with double switches, IPW65R080CFD as primary and SUM110N06 as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
8	15,635	7,592	0,786	0,914	0,319	1,381	26,627	246,384
14	10,395	8,167	1,205	2,387	0,542	1,482	24,177	418,222
20	13,118	7,418	1,753	4,505	0,764	1,586	29,143	589,487
28	16,281	7,807	2,784	8,641	1,083	1,748	38,345	835,710
36	18,039	8,656	3,988	13,760	1,388	1,919	47,749	1073,818
42	18,480	9,504	4,941	17,949	1,596	2,037	54,507	1235,314
48	18,554	11,553	6,077	23,004	1,819	2,158	63,165	1403,755
56	18,414	12,842	7,785	30,845	2,123	2,347	74,356	1639,326
64	18,191	15,612	9,699	40,023	2,434	2,544	88,504	1876,868
68	18,214	18,844	10,867	45,589	2,609	2,680	98,803	2021,544
74	18,173	22,135	12,383	53,104	2,830	2,819	111,443	2183,773
84	18,008	27,789	15,294	68,036	3,230	3,108	135,464	2491,040
100	18,764	36,908	19,946	92,888	3,825	3,568	175,898	2947,893

Table A.8: Current Doubler converter losses in [W] at 100 kHz with double switches, IPW65R080CFD as primary and FDP027N08B as secondary switches

load [%]	$P_{sw,tot,P}$	$P_{sw,tot,S}$	$P_{cond,tot,P}$	$P_{cond,tot,S}$	P_{copper}	P_{core}	$P_{tot,loss}$	P_{out}
9	15,514	0,697	0,789	1,082	0,355	1,381	19,817	274,596
15	10,419	0,558	1,192	2,535	0,568	1,482	16,754	439,574
21	12,947	0,536	1,742	4,604	0,786	1,586	22,200	608,230
29	16,192	0,346	2,785	8,761	1,105	1,748	30,938	855,004
37	18,066	0,257	4,050	14,061	1,419	1,919	39,771	1097,964
43	18,521	0,312	5,050	18,479	1,634	2,037	46,033	1262,956
48	18,168	0,345	6,038	22,874	1,823	2,158	51,407	1410,262
56	18,463	0,362	7,751	30,831	2,129	2,347	61,883	1648,889
64	18,282	0,397	9,682	39,977	2,440	2,544	73,322	1886,005
69	18,195	0,342	10,942	46,259	2,633	2,680	81,052	2037,728
74	18,081	0,404	12,350	53,367	2,836	2,819	89,858	2193,634
84	18,017	0,474	15,276	68,625	3,236	3,108	108,736	2501,381
92	18,127	0,558	17,588	81,209	3,538	3,334	124,354	2731,863
100	18,615	0,646	19,926	94,309	3,832	3,568	140,896	2959,688